XHSC 小华半导体 XIAOHUA SEMICONDUCTOR

HC32A448 Series

32-bit ARM® Cortex®-M4 Microcontroller

Datasheet

Rev1.00 May 2024

Features

ARM Cortex-M4 32bit MCU+FPU, 250DMIPS, 256KB Flash, 68KB SRAM, 2CAN FD, EXMC, 15Timers, 3ADCs, 2DACs, 4CMPs, 6UARTs, 3SPIs, 2I2Cs, QSPI, AES, HASH (SHA256)

- **ARMv7-M architecture 32bit Cortex-M4 CPU, integrated FPU, MPU, DSP supporting SIMD instructions, and CoreSight standard debugging unit. The highest operating frequency is 200MHz, reaching the computing performance of 250DMIPS or 680Coremarks**
- **Built-in memory**
  - Flash memory up to 256KB
  - Maximum 68KB single-cycle access to high-speed SRAM
- **Power, Clock, Reset Management**
  - System power supply (Vcc): 1.8-3.6V
  - 7 independent clock sources: external main clock crystal oscillator (4-25MHz), external secondary crystal oscillator (32.768KHz), internal high-speed RC (16/ 20MHz), internal medium-speed RC (8MHz), internal low-speed RC (32KHz), PLL, Internal WDT dedicated RC (10KHz)
  - 15 kinds of reset sources including power-on reset (POR), low voltage detection reset (PVD1R/ PVD2R), port reset (NRST), each reset source has an independent flag bit
- **Low power operation**
  - Peripherals can be turned off or on independently
  - Three low power consumption modes: Sleep mode, Stop mode, Power Down mode
- **Peripheral operation support system significantly reduces CPU processing load**
  - 12-channel dual-host DMAC
  - 4 Data Computing Units (DCUs)
  - Support mutual triggering of peripheral events (AOS)
- **High Performance Simulation**
  - 3 independent 12bit 2.5MSPS ADCs
  - 2 independent 12bit DACs
  - 4 independent voltage comparators (CMP)
- **Timer**
  - 2 multifunctional 16bit PWM Timers (Timer6)
  - 3 16-bit motor PWM Timers (Timer4)
  - 1 32bit general-purpose Timers (TimerA)
  - 4 16bit general-purpose Timers (TimerA)
  - Two 16bit basic timers (Timer0)
  - Real time clock Timer (RTC)
  - 2 WDTs, supporting internal dedicated clocks
- **Up to 67 GPIOs**
  - Up to 62 5V-tolerant IOs
- **Maximum 14 communication interfaces**
  - 6 USART, support ISO7816-3 protocol
  - 3 SPIs
  - 2 I2C, support SMBus protocol
  - 1 QSPI, support 100Mbps high-speed access (XIP)
  - 2 CAN FD controller (MCAN), compatible with CAN2.0A/B
- **External Memory Controller EXMC**
  - Support for static memory controllers
- **Data encryption function**
  - AES/ HASH (SHA256)/ TRNG
- **Encapsulation form:**
  - LQFP80 (12×12mm)
  - LQFP64 (10×10mm)
  - LQFP48 (7×7mm)

Support Model:

HC32A448JCTI-LQ48	HC32A448MCTI-LQFP80
HC32A448KCTI-LQFP64	-

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1 Overview

The HC32A448 series is a high-performance MCU based on ARM® Cortex®-M4 32-bit RISC CPU with a maximum operating frequency of 200MHz. The Cortex-M4 core integrates a floating-point arithmetic unit (FPU) and a DSP to implement single-precision floating-point arithmetic operations, supports all ARM single-precision data processing instructions and data types, and supports the complete DSP instruction set. The kernel integrates the MPU unit and superimposes the DMAC dedicated MPU unit at the same time to ensure the safety of system operation.

The HC32A448 series integrates high-speed on-chip memory, including a maximum of 256KB of Flash and a maximum of 68KB of SRAM. Integrated Flash access acceleration unit to achieve single cycle program execution of the CPU on Flash. The polled bus matrix supports multiple bus hosts to access memory and peripherals simultaneously, improving performance. The bus master includes CPU, DMA. In addition to the bus matrix, it supports data transfer between peripherals, basic arithmetic operations and mutual triggering of events, which can significantly reduce the transaction processing load of the CPU.

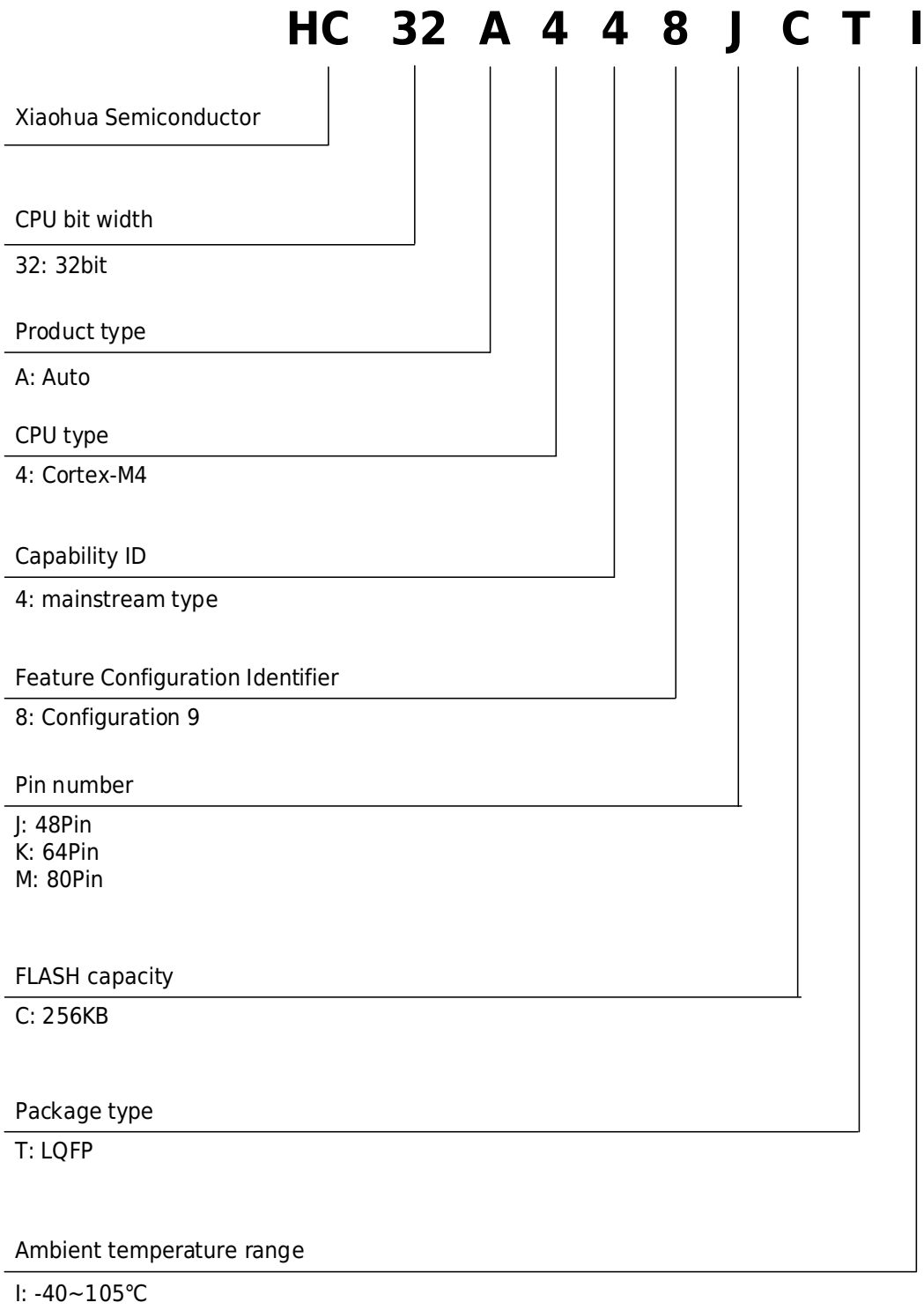
The HC32A448 series integrates a wealth of peripheral functions, including: 3 independent 12bit 2.5MSPS ADCs; 2 12-bit DACs; 4 high-speed voltage comparators (CMP); 2 multifunctional PWM Timers (Timer6), supporting 4 1 complementary PWM output; 3 motor PWM Timers (Timer4), supporting 24 complementary PWM outputs; 4 16bit general-purpose Timers (TimerA) and 1 32bit general-purpose Timer (TimerA), supporting quadrature encoding input and 40 duty cycles PWM output can be set; 11 serial communication interfaces (I2C/UART/SPI); 1 QSPI interface; 2 CAN FD controller (MCAN); 1 external expansion bus controller, including SMC controller.

The HC32A448 series supports wide voltage range (1.8~3.6V), wide temperature range (-40~105℃) and various low power consumption modes. Support fast wake-up from low-power mode, the fastest wake-up from Power Down mode is 25μs.

Typical Application

The HC32A448 series provides 48pin, 64pin, 80pin LQFP packages for automotive electronic node applications such as seat controllers, tailgate controllers, air conditioning control panels, AVAS low speed alarms, etc.

1.1 Part Naming Rules



1.2 Model Function Comparison Table

Table 1-1 Model Function Comparison Table

Function		Product Model		
		HC32A448 JCTI	HC32A448 KCTI	HC32A448 MCTI
Pin number		48	64	80
Number of GPIOs		38	52	67
5V Tolerant Number of GPIOs		36	47	62
Encapsulation		LQFP	LQFP	LQFP
Temperature range		-40~105℃		
Supply voltage range		1.8~3.6V		
Storage	Flash	256KB	256KB	256KB
	OTP	9KB		
	SRAM	68KB		
DMA controller		2unit * 6ch		
External port interrupt		EIRQ * 16		
Communication Interface	USART	6ch		
	SPI	3ch		
	I2C	2ch		
	CAN FD	2ch		
	QSPI	1ch		
Timers and Counters	Timer0	2unit		
	TimerA	5unit		
	Timer4	3unit		

Function		Product Model		
		HC32A448 JCTI	HC32A448 KCTI	HC32A448 MCTI
	Timer6	2unit		
	WDT	1ch		
	SWDT	1ch		
	RTC	1ch		
Simulation	12bit ADC	3unit, 11ch	3unit, 17ch	3unit, 24ch
	12bit DAC	2ch	2ch	2ch
	CMP	4ch		
Data Computing Unit (DCU)		✓		
Encryption and decryption algorithm processor (AES256)		✓		
Secure Hash Algorithm (HASH SHA256)		✓		
True random number generator (TRNG)		✓		
External Memory Controller (EXMC)		not support	✓	✓
Frequency Monitoring Module (FCM)		✓		
Programmable voltage detection function (PVD)		✓		
Debug controller (DBGC)	SWD	✓		
	JTAG	✓		

1.3 Functional Block Diagram

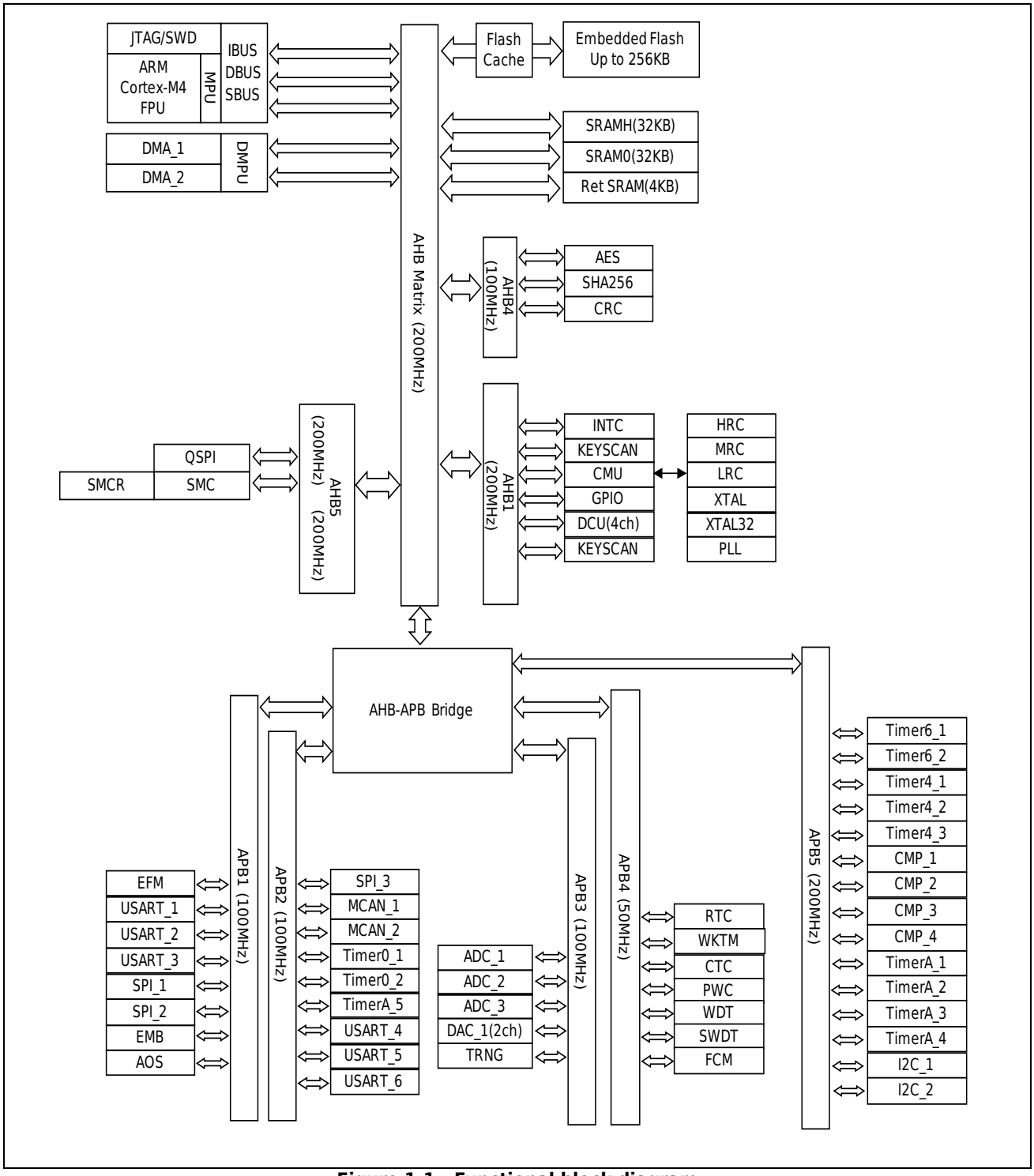


Figure 1-1 Functional block diagram

1.4 Feature Brief

1.4.1 CPU

The HC32A448 series integrates the latest generation of embedded ARM® Cortex®-M4 with FPU 32bit simplified instruction CPU, which realizes fewer pins and lower power consumption while providing excellent computing performance and rapid interrupt response capability. The memory capacity integrated on the chip can give full play to the excellent instruction efficiency of Cortex-M4. The CPU supports DSP instructions, which can realize efficient signal processing operations and complex algorithms. The single-precision FPU (Floating Point Unit) unit can avoid instruction saturation and speed up software development.

1.4.2 Bus Architecture (BUS)

The main system is composed of 32-bit multilayer AHB bus matrix, which can interconnect the following host bus and slave bus.

- Host bus
  - Cortex-M4 core CPU-I bus, CPU-D bus, CPU-S bus
  - System DMA_1 bus, system DMA_2 bus
- Slave bus
  - Flash ICODE bus
  - Flash DCODE bus
  - Flash MCODE bus (the bus that hosts other than the CPU access the Flash)
  - High-speed SRAMH (SRAMH 32KB) bus
  - System SRAM (SRAM0 32KB) bus
  - System SRAM (Ret SRAM 4KB) bus
  - APB1 Peripheral Bus (EMB/ SPI/ USART/ EFM/ AOS)
  - APB2 Peripheral Bus (TimerA/ Timer0/ SPI/ USART/ MCAN)
  - APB3 Peripheral Bus (ADC/ DAC/ TRNG)
  - APB4 Peripheral Bus (FCM/ WDT/ SWDT/ PWC/ CTC/ RTC/ WKTM)
  - APB5 Peripheral Bus (TimerA/ Timer4/ Timer6/ CMP/ I2C)
  - AHB1 Peripheral Bus (DCU/ CMU/ GPIO/ DMA/ INTC/ KEYSCAN/ DMPU)
  - AHB4 Peripheral Bus (AES/ HASH/ CRC)
  - AHB5 Peripheral Bus (SMC/ SMCR/ QSPI)

With the help of the bus matrix, high-efficiency concurrent access from the host bus to the slave bus can be realized.

1.4.3 Reset Control (RMU)

The chip is configured with 15 reset modes.

- Power On Reset (POR)
- NRST pin reset (NRST)
- Brown-out Reset (BOR)
- Programmable Voltage Detect 1 Reset (PVD1R)
- Programmable Voltage Detect 2 Reset (PVD2R)
- Watchdog Reset (WDTR)
- Special watchdog reset (SWDTR)
- Power-down wake-up reset (PDRST)
- Software Reset (SRST)
- MPU error reset (MPUR)
- RAM Parity Reset (RAMPR)
- RAMECC reset (RAMECCR)
- Clock Exception Reset (CKFER)
- External high-speed oscillator abnormal shutdown reset (XTALER)
- Cortex-M4 Lockup reset (LKUPR)

1.4.4 Clock Control (CMU)

The clock control unit provides a series of frequency clock functions, including: an external high-speed oscillator, an external low-speed oscillator, a PLL clock, an internal high-speed oscillator, an internal medium-speed oscillator, an internal low-speed oscillator, a SWDT dedicated internal low-speed oscillator, clock prescaler, clock multiplexing and clock gating circuits.

The clock control unit also provides a clock frequency measurement function. The clock frequency measurement circuit (FCM) uses the measurement reference clock to monitor and measure the measurement target clock, and interrupts or resets when the clock frequency exceeds the set range.

The AHB, APB and Cortex-M4 clocks are all derived from the system clock. The maximum operating clock frequency of the system clock can reach 200MHz, and there are 6 optional clock sources:

1) External high-speed oscillator (XTAL)
2) External low-speed oscillator (XTAL32)
3) PLLH clock (PLLH)
4) Internal high-speed oscillator (HRC)
5) Internal Medium Speed Oscillator (MRC)
6) Internal low-speed oscillator (LRC)

For each timer, you can turn it on and off separately when not in use to reduce power consumption. SWDT has an independent clock source: SWDT dedicated internal low-speed oscillator (SWDTLRC).

The real-time clock (RTC) uses the external low-speed oscillator, the internal low-speed oscillator or the XTAL fractional frequency clock as the clock source.

1.4.5 Power Control (PWC)

The power controller is used to control the power supply, switching and detection of multiple power domains of the chip in multiple operating modes and low power consumption modes. The power controller is composed of power control logic (PWC) and power voltage detection unit (PVD).

The operating voltage (VCC) of the chip is 1.8V to 3.6V. The voltage regulator (LDO) supplies power to the VDD domain and the VDDR domain, and the VDDR voltage regulator (RLDO) supplies power to the VDDR domain in power-down mode. Through the power control logic (PWC), the chip provides two operating modes of high speed and ultra low speed, and three low power modes of sleep, stop and power down.

The power voltage detection unit (PVD) provides functions such as power-on reset (POR), power-down reset (PDR), brown-out reset (BOR), programmable voltage detection 1 (PVD1), and programmable voltage detection 2 (PVD2). Among them, POR, PDR, and BOR control the reset action of the chip by detecting the VCC voltage. PVD1 detects the VCC voltage and resets or interrupts the chip according to the register settings. PVD2 detects VCC voltage or external input detection voltage, and generates reset or interrupt according to register selection.

When the chip enters the power-down mode, the VDDR area maintains the power supply through RLDO and keeps the 4KB Ret SRAM data.

The analog blocks are equipped with dedicated supply pins for improved analog performance.

1.4.6 Initialization Configuration (ICG)

After the chip reset is released, the hardware circuit will read the FLASH address 0x0000 0400~0x0000 045F and load the data into the initialization configuration register. Addresses 0x0000 0408~0x0000 040B, 0x0000 0410~0x0000 041F, 0x0000 0438~0x0000 045F are reserved addresses, please write all 1s to ensure the normal operation of the chip. When the FLASH boot exchange is invalid, there is a FLASH block 0 sector 0 in this area; when the FLASH boot exchange is valid, and the OTP of the FLASH block 0 sector 0 is not latched (0x0300 0A80~0x0300 0A83 data are all 1), there is a FLASH block in this area 0 sector 1; otherwise, there is FLASH block 0 sector 0 in this area. User can modify Initialization Configuration Register (ICG) by programming or erasing Sector 0. The address 0x0000 0420~0x0000 0437 is the data security protection enable area. The register reset value is determined by the FLASH address data.

1.4.7 Embedded Flash Interface (EFM)

The FLASH interface accesses the FLASH through the ICODE, DCODE and MCODE buses, and can perform programming, erasing and full erasing operations on the FLASH; it accelerates code execution through the instruction prefetch and cache mechanism.

Main features:

- Maximum OTP space of 9KBytes
- ICODE bus 16Bytes prefetching
- Two independent buffer areas: ICODE bus buffer space 1KBytes; DCODE bus buffer space 128Bytes
- Support boot swap function
- Support data security protection

1.4.8 Built-in SRAM (SRAM)

This product has 64KB system SRAM (SRAMH/ SRAM0) and 4KB power-down mode retention SRAM (Ret SRAM).

Each SRAM can be accessed by byte, halfword (16 bits) or full word (32 bits). All SRAM read and write operations can be performed at the fastest speed of the CPU (200MHz).

Ret SRAM can provide 4KB of data retention space in Power Down mode.

SRAM0 and Ret SRAM have ECC check (Error Checking and Correcting), ECC check is a correction code, that is, it can correct one error and check two errors; SRAMH has a parity check (Even-parity check) , each byte of data has a parity bit.

1.4.9 General IO (GPIO)

Main Features of GPIO:

- Each port group has 16 I/O Pins, which may be less than 16 depending on actual configuration
- Support pull-up and pull-down
- Support push-pull, open-drain output mode
- Supports high, medium and low drive modes
- Support CMOS/ Schmitt two input modes to switch freely
- Support for external interrupt input
- Support I/O pin peripheral function multiplexing, each I/O pin has up to 41 optional multiplexing functions
- Individual I/O pins can be programmed independently
- Each I/O pin can select 2 functions to be valid at the same time (does not support 2 output functions to be valid at the same time)

1.4.10 Interrupt Control (INTC)

The interrupt controller (INTC) selects an interrupt event as an interrupt request and sends it to NVIC to wake up WFI; selects an interrupt event as an event input (RXEV) to wake up WFE; selects an interrupt event to wake up the system from low-power modes (sleep mode and stop mode); controls external interrupts and software interrupts.

The main specifications of INTC are as follows:

- NVIC interrupt request: INTC is equipped with 257 interrupt events, which are sent to NVIC as interrupt requests (IRQs) after processing, supporting 130 IRQs, and each IRQ corresponds to one or more interrupt events
  For more instructions on exceptions and NVIC programming, please refer to "Arm Cortex-M4 Processor Technical Reference Manual"
- Programmable Priority: 16 Programmable Priorities (using 4-bit Interrupt Priority Register)
- Non-maskable interrupts: Multiple system interrupt events can be independently selected as non-maskable interrupts, and each interrupt event is equipped with independent enable selection, flag, and flag clear registers
- Equipped with 16 external pin interrupt events
- Equipped with multiple interrupt events, please refer to the interrupt event table in the interrupt controller chapter of the reference manual for details
- Equipped with 32 software interrupt events
- Interrupts can wake up the system from sleep mode and stop mode

1.4.11 Automatic Operating System (AOS)

The automatic operation system (Automatic Operation System) is used to realize the linkage between peripheral hardware circuits without the help of the CPU. Use the events generated by the peripheral circuit as the AOS source (AOS Source), such as timer comparison matching, timing overflow, RTC periodic signal, various states of the communication module's sending and receiving data (idle, receiving data full, sending data end, send data empty), ADC conversion end, etc., to trigger other peripheral circuit actions. The triggered peripheral circuit action is called AOS target (AOS Target).

AOS is also equipped with 4 programmable logic operation units (PLU) for logic operation of PORT and AOS source. Users can select one or more AOS sources to trigger the same AOS target according to their needs.

1.4.12 Memory Protection Unit (MPU)

The MPU can provide protection to the memory, and can improve the security of the system by preventing unauthorized access.

This chip has built-in 1 MPU unit for CPU, 1 MPU unit for CPU main stack pointer, 1 MPU unit for CPU thread stack pointer, 2 MPU units for DMA and 1 MPU unit for IP.

Among them, the ARM MPU provides the access control of the CPU to the entire 4G address space.

MSPMPU/ PSPMPU respectively provide protection for the CPU's main stack pointer/thread stack pointer. When the pointer exceeds the set range, the MPU action can be set as non-maskable interrupt/reset.

SMPU1/ SMPU2 respectively provide system DMA_1/system DMA_2 with read and write access control to the entire 4G address space. When accessing the prohibited space, the MPU action can be set to ignore/bus error/non-maskable interrupt/reset.

The IPMPU provides access control to system IP and security-related IP in non-privileged mode.

1.4.13 Keyboard Scanning (KEYSCAN)

This product is equipped with a keyboard control module (KEYSCAN) 1 unit. The KEYSCAN module supports keyboard array (row and column) scanning, the column is driven by an independent scan output KEYOUTm (m=0~7), and the row KEYINn (n=0~15) is input as EIRQn (n=0~15) is detected. This module realizes the key recognition function through the line scan query method.

1.4.14 Internal Clock Calibrator (CTC)

The Clock Trimming Controller (CTC) automatically calibrates the internal high-speed oscillator (HRC). Because the influence of working environment on HRC frequency may cause deviation, CTC can automatically adjust HRC frequency by hardware based on external high precision reference clock to obtain an accurate HRC clock.

The main features of CTC are as follows:

- Three external reference clock sources: XTAL, XTAL32, CTCREF
- 16-bit calibrated counter for frequency measurement with reload function
- 8-bit calibration offset value and 6-bit calibration value for frequency calibration
- Error interrupt for calibration failure

1.4.15 DMA Controller (DMA)

DMA is used to transfer data between memory and peripheral function modules, and can realize data exchange between memories, between memory and peripheral function modules, and between peripheral function modules without CPU participation.

- DMA bus is independent of CPU bus and transmitted according to AMBA AHB-Lite bus protocol.
- With 2 DMA control units, a total of 12 independent channels, which can independently operate different DMA transfer functions
- For each channel, the source of the boot request is configured via a separate trigger source

- One block per request
- The minimum data block is 1 data, and the maximum is 1024 data
- The width of each data can be configured as 8bit, 16bit or 32bit
- 1~65535 or unlimited transmissions can be configured
- The source address and target address can be independently configured as fixed, self-incrementing, self-decreasing, looping, or jumping with a specified offset
- Three kinds of interrupts can be generated: block transfer complete interrupt, transfer complete interrupt and transfer error interrupt. Each interrupt can be configured with a mask or not. Among them, the completion of block transmission and the completion of transmission can be used as event output, which can be used as the trigger source of other peripheral modules
- Support for linked transmission to enable multiple blocks of data to be transmitted at a time
- Support channel reset triggered by external events
- You can set the module stop state to reduce power consumption when not in use
- The HPROT value in the AHB bus during DMA access can be set by register

1.4.16 Voltage Comparator (CMP)

A voltage comparator (Comparator, hereinafter referred to as CMP) is a peripheral module that compares two analog voltages and outputs a comparison result. This product is equipped with two sets of 4 comparison channels: CMP1/ CMP2, CMP3/ CMP4.

CMP has the following main features:

- 4 comparison channels can perform voltage comparison independently
- The combination of two comparison channels in the same group can realize up to 2 groups of window comparisons
- There are multiple input sources (IO/ DAC) for the positive/ negative terminal voltage of each comparison channel
- The noise filter can filter the output of the comparator, and 7 sampling clocks are optional
- Comparator output blank window control using timer PWM
- Can generate interrupts, trigger other peripherals, and wake up from STOP mode on the edge of the comparison result
- The comparison result can be monitored by the register, and can also be output to the external pin VCOUT
- Comparison results can be used for emergency braking (EMB) control events

1.4.17 Analog-to-Digital Converter (ADC)

12-bit ADC is an analog-to-digital converter with successive approximation. This MCU is equipped with 3 ADC units, unit 1 supports a maximum of 16 channels, unit 2 supports a maximum of 8 channels, and unit 3 supports a maximum of 12 channels, which can convert analog signals from

external pins and inside the chip. The analog input channels can be combined into a sequence arbitrarily, and a sequence can be converted by single scan or continuous scan. It supports multiple consecutive conversions on any specified channel and averages the conversion results. The ADC module is also equipped with an analog watchdog function to monitor the conversion result of any specified channel and detect whether it exceeds the range set by the user.

The main features of the ADC are as follows:

- High performance
  - Configurable 12-bit, 10-bit and 8-bit resolution
  - The frequency ratio of ADC digital interface clock PCLK4 and conversion clock PCLK2 (also known as ADCLK) can be set to 1:1, 2:1, 4:1, 8:1, 1:2, 1:4
    PCLK2 can choose the PLL clock that is asynchronous with the system clock HCLK, and the frequency ratio at this time is PCLK4:PCLK2=1:1
  - PCLK2 frequency up to 60MHz
  - Sampling rate: 2.5MSPS (PCLK2=60MHz, 12 bits, sampling 11 cycles, conversion 13 cycles)
  - The sampling time of each channel is independently programmed
  - Channel-independent data register
  - Data register configurable left/right alignment
  - Consecutive multiple conversion average function
  - Oversampling function
  - Simulation watchdog, monitoring conversion results
  - The ADC module can be set to stop when not in use
- Analog input channel
  - Maximum 24 external analog input channels
  - 1 internal analog input: internal reference voltage
- Conversion start condition
  - Software Setup Conversion Started
  - Start of Peripheral Device Synchronization Trigger Conversion
  - External Pin Triggering Start
- Conversion mode
  - 2 scan sequences A and B, optionally specifying a single or multiple channels
  - Sequence A single scan
  - Sequence A continuous scanning
  - Sequence A multiple data cache mode
  - Double sequence scanning, sequence A and B independently select trigger source, sequence B has higher priority than A
  - Cooperative mode (for devices with two or three ADCs)
- Interrupt and Event Signal Output
  - Sequence A Scan End Interrupt and Event ADC_EOCA

- Sequence B Scan End Interrupt and Event ADC_EOCB
- Analogwatchdog 0 compared interrupt and event ADC_CMP0
- Simulation watchdog 1 comparing interrupt and event ADC_CMP1
- All four of these event outputs can start the DMA

1.4.18 Digital to Analog Converter (DAC)

This MCU is equipped with a digital-to-analog converter unit DAC with 12-bit conversion accuracy. The DAC unit contains two D/A conversion channels, and the two channels can be converted independently or synchronously. There are two levels of analog voltage output range can be set. Each conversion channel is equipped with an output amplifier that can directly drive an external load without an external op amp.

The main features of the DAC are as follows:

- Two D/A conversion channels
- 12-bit conversion data can be configured as left-justified or right-justified format
- Simultaneous Conversion of Two Conversion Channels
- The data of the conversion data computing unit (DCU) can output triangle wave and sawtooth wave
- The output can be used as the negative input of the voltage comparator (CMP)
- Outputs are amplified to directly drive external loads
- A/D conversion priority mode can reduce interference with ADC conversion

1.4.19 Advanced Control Timer (Timer6)

Advanced Control Timer 6 (Timer6) is a high-performance timer with a 16-bit count width, which can provide rich and flexible combinations and various interrupts, events, and PWM outputs in various complex application scenarios. The timer supports two counting waveform modes of sawtooth wave and triangular wave, and can generate various PWM waveforms (unilaterally aligned independent PWM, bilaterally symmetrical independent PWM, bilaterally symmetrical complementary PWM, bilaterally asymmetrical PWM, etc.); software synchronization between units can be achieved Synchronized with hardware (synchronous start, stop, clear, refresh, etc.); each reference register supports cache function (single-level cache and double-level cache); supports pulse width measurement and period measurement; supports 2-phase quadrature encoding counting and 3 Phase quadrature encoding count; support EMB control. This series of products is equipped with 2 units of Timer6.

1.4.20 General Control Timer (Timer4)

General control timer 4 (Timer4) is a timer module for three-phase motor control. It provides three-phase motor control schemes for various applications. The timer supports two counting waveform

modes of triangle wave and sawtooth wave, and can generate various PWM waveforms; supports buffer function; supports EMB control. 3 unit of Timer 4 is carried in this product family.

1.4.21 Emergency Brake Module (EMB)

The emergency brake module is a functional module that generates a control event and outputs it to the timer when certain conditions are met, so as to control the timer to stop or change the output PWM signal to the external motor. The following factors are used to generate the control event:

- Change of input level of external port
- Level of PWM output port occurs in phase (same high or same low)
- Voltage comparator comparison results
- System error occurred
- Write register software control

1.4.22 General Timer (TimerA)

General-purpose TimerA is a timer with 16/32-bit count width and 8 PWM outputs. The timer supports two counting waveform modes of triangular wave and sawtooth wave, and can generate various PWM waveforms (unilaterally aligned PWM, bilaterally symmetrical PWM); supports counter synchronous start; comparison reference value register supports cache function; supports cascaded counting between units; Support 2-phase quadrature code count and 3-phase quadrature code count. This series of products is equipped with 5 units TimerA (unit 1 is a 32-bit timer, and units 2~5 are 16-bit timers), which can realize up to 40 channels of PWM output.

1.4.23 General Timer (Timer0)

General-purpose Timer0 is a basic timer that can realize synchronous counting and asynchronous counting. The timer contains 2 channels (CH-A and CH-B), which can generate comparison match events and count overflow events during the counting period. This event can trigger an interrupt, and can also be used as an event output to control other modules. This series of products is equipped with 2 units of Timer0.

1.4.24 Real Time Clock (RTC)

A real-time clock (RTC) is a counter that stores time information in BCD format. Record the specific calendar time from 00 to 99. Supports 12/24 hour time format, and can automatically calculate the number of days 28, 29 (leap year), 30 and 31 according to the month and year.

1.4.25 Watchdog Counter (WDT/SWDT)

This product has two watchdog counters, one is the counting clock source is a dedicated internal RC (SWDTLRC: 10KHz) dedicated watchdog counter (SWDT), and the other is a general-purpose watchdog counter (WDT) whose count clock source is PCLK3. Both the dedicated watchdog and the general watchdog are 16-bit down counters, which are used to monitor software failures due to

external disturbances or unforeseen logic conditions that deviate from the normal operation of the application program.

Both watchdogs support window compare function. The window interval can be preset before the count starts, and when the count value is within the window interval, the counter can be refreshed and the count restarted.

1.4.26 General Synchronous Asynchronous Transceiver (USART)

This product is equipped with 6 units of Universal Synchronous Asynchronous Transceiver (USART) module, which can flexibly perform full-duplex data exchange with external devices. The USART equipped on this product supports universal asynchronous serial communication interface (UART), clock synchronous communication interface, smart card interface (ISO/IEC7816-3) and LIN communication interface; supports modem operation (CTS/RTS operation), processor operation. Cooperate with Timer0 module to support UART receive timeout function. USART_1 supports wake-up function through RX pin STOP mode.

The specific functions are allocated as follows:

- UART: full channel support
- Multiprocessor communication: full channel support
- Clock synchronous communication: full channel support
- RX pin wakes up Stop mode function: USART_1 support
- Fractional baud rate: full channel support
- LIN: USART_3, USART_6 support
- Smart Card: USART_1, USART_2, USART_4, USART_5 supported
- UART receive timeout function: USART_1, USART_2, USART_4, USART_5 support

1.4.27 Integrated Circuit Bus (I2C)

I2C (Integrated Circuit Bus) is used as an interface between the microcontroller and the I2C serial bus. Provide multi-master mode function, which can control the protocol and arbitration of all I2C buses. Standard mode and fast mode are supported. SMBus is also supported.

This product is equipped with 2-channel integrated circuit bus I2C.

I2C main features:

- I2C bus mode and SMBus bus mode are optional. Host mode and slave mode are optional. Automatically ensures various prepare times, hold times, and bus idle times relative to the transfer rate
- Standard mode up to 100Kbps, fast mode up to 400Kbps
- Automatically generate start condition, restart condition and stop condition, and can detect bus start condition, restart condition and stop condition

- Maximum support for 128 slave addresses. Support 7-bit address format and 10-bit address format. Can detect broadcast call address, SMBus host address, SMBus device default address, SMBus alarm address
- Answer bits can be automatically determined when sent. Acknowledgment bit can be sent automatically when receiving
- Handshake function
- Arbitration function
- Timeout function, can detect SCL clock stop for a long time
- SCL input and SDA input built-in digital filter, filter capability can be programmed
- Communication error, received data is full, sent data is empty, a frame is sent, and the address match is interrupted
- 2-stage transmit FIFO and 2-stage receive FIFO

1.4.28 Serial Peripheral Interface (SPI)

This product is equipped with a serial peripheral interface SPI with 3 channels, supports high-speed full-duplex serial synchronous transmission, and can easily exchange data with peripheral devices. Users can set the range of 3/4-wire, host/slave and baud rate as needed.

Main Features of SPI:

- Serial communication function
  - Supporting 4-wire SPI mode and 3-wire clock synchronization mode
  - Support full-duplex and send-only communication methods
  - Polarity and phase of adjustable communication clock SCK
- Data format
  - Selectable data shift order: MSB start/LSB start
  - Selectable data width: 4/ 5/ 6/ 7/ 8/ 9/ 10/ 11/ 12/ 13/ 14/ 15/ 16/ 20/ 24/ 32 bits
  - A maximum of 32 bits of data can be transmitted or received ifn four single frame
- Baud rate
  - In host mode, the baud rate can be adjusted through the built-in dedicated baud rate generator, and the baud rate range is divided by 2 to 256 of PCLK1
  - The maximum baud rate allowed in slave mode is divided by 6 of PCLK1
- Data buffer
  - Data buffer area with 16 bytes
  - Supports double buffering
- Error monitoring
  - Mode fault error monitoring
  - Data overload error monitoring
  - Data underload error monitoring

  - Parity error monitoring
- Chip selection signal control
  - Each channel is configured with excluding chip-selected signal line
  - The relative timing relationship between the chip select signal and the communication clock can be adjusted
  - The invalid time of the chip select signal between two consecutive communications can be adjusted
  - Polarity adjustable
- Transmission Control in Host Mode
  - Start transmission by writing data to the data register
  - Communication auto suspend function
- Interrupt
  - Accept data area is full
  - Sending data area is empty
  - SPI error (mode/overload/underload/parity)
  - SPI vacant
  - Transfer complete (event source only)
- Low power control
  - Configurable module stop
- Other functions
  - SPI initialization function

1.4.29 Quad-wire Serial Peripheral Interface (QSPI)

The Quad Serial Peripheral Interface (QSPI) is a memory control module designed to communicate with serial ROMs with an SPI-compatible interface. Its objects mainly include serial flash memory, serial EEPROM and serial FeRAM.

1.4.30 External Memory Controller (EXMC)

The external memory controller EXMC (External Memory Controller) is an independent module used to access various off-chip memories and realize data exchange. Through configuration, EXMC can convert the internal AMBA protocol interface into various types of dedicated off-chip memory communication protocol interfaces, including SRAM, PSRAM, NOR Flash, etc.

1.4.31 Controller Area Network (MCAN)

This product is equipped with two unit MCAN communication interface modules (MCAN1 and MCAN2), and is equipped with 2KB RAM for the two MCAN controllers.

Both CAN modules (MCAN1 and MCAN2) comply with ISO 11898-1: 2015 (CAN Protocol Specification Version 2.0 Part A, B) and CAN FD Protocol Specification Version 1.0 (CAN with Flexible Data-Rate Specification Version 1.0).

The 2KB message RAM memory can realize the functions of receiving filter (Rx Filter), receiving FIFO (Rx FIFO), receiving buffer (Rx Buffer), sending event FIFO (Tx Event FIFO), and sending buffer (Tx Buffer). This message RAM is shared between the MCAN1 and MCAN2 modules.

1.4.32 Cryptographic Coprocessing Module (CPM)

The encryption co-processing module (CPM) includes three sub-modules: AES encryption and decryption algorithm processor, HASH secure hash algorithm, and TRNG true random number generator.

The AES encryption and decryption algorithm processor follows the new data encryption standard officially announced by the National Institute of Standards and Technology (NIST) on October 2, 2000. The block length is fixed at 128 bits, and the key length supports 128/ 192/ 256 bits.

The HASH secure hash algorithm is the SHA-2 version of SHA-256 (Secure Hash Algorithm), which complies with the national standard "FIPS PUB 180-3" issued by the National Institute of Standards and Technology, and can generate 256bit message digest output.

TRNG true random number generator is a random number generator based on continuous analog noise, providing 64bit random numbers.

1.4.33 Data Computing Unit (CRC)

Data Computing Unit DCU (Data Computing Unit) is a module that simply processes data without the help of a CPU. Each DCU unit has 3 data registers, which can perform addition and subtraction of 2 data and size comparison, as well as window comparison function, and can also provide continuously changing digital quantities to the digital-to-analog conversion module (DAC) through timer triggers to generate Triangle and sawtooth output. This product is equipped with 4 DCU units.

1.4.34 CRC Unit (CRC)

The CRC algorithm of this module complies with the definition of ISO/ IEC13239, using 32-bit and 16-bit CRC respectively. The generating polynomial of CRC32 is $X^{32}+ X^{26}+ X^{23}+ X^{22}+ X^{16}+ X^{12}+ X^{11}+ X^{10}+ X^{8}+ X^{7}+ X^{5}+ X^{4}+ X^{2}+ X+ 1$, and the initial value of 32 bits is 0xFFFF FFFF. The generating polynomial of CRC16 is $X^{16}+ X^{12}+ X^{5}+ 1$, and the initial value of 16 bits is 0xFFFF.

1.4.35 Debug Controller (DBGC)

The core of this MCU is Cortex-M4, which contains hardware for advanced debugging functions. With these debugging features, you can stop the kernel when fetching fingers (instruction breakpoints) or accessing data (data breakpoints). When the kernel is stopped, the internal state

of the kernel and the external state of the system can be queried. After the query is completed, the kernel and system will be restored and program execution will resume.

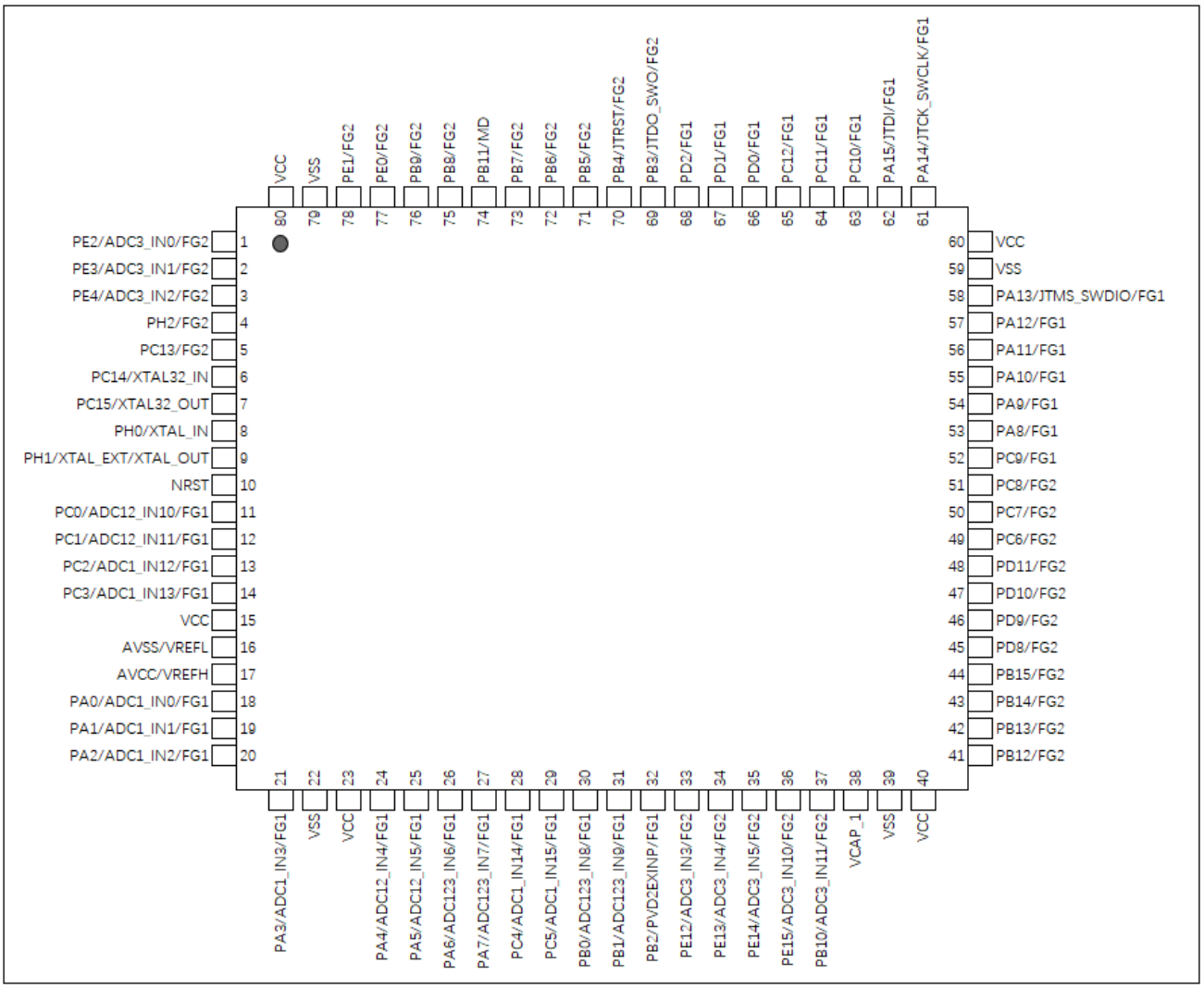
Two debugging interfaces are provided:

- Serial Debugging Tracking Interface SWD
- Parallel debug trace interface JTAG

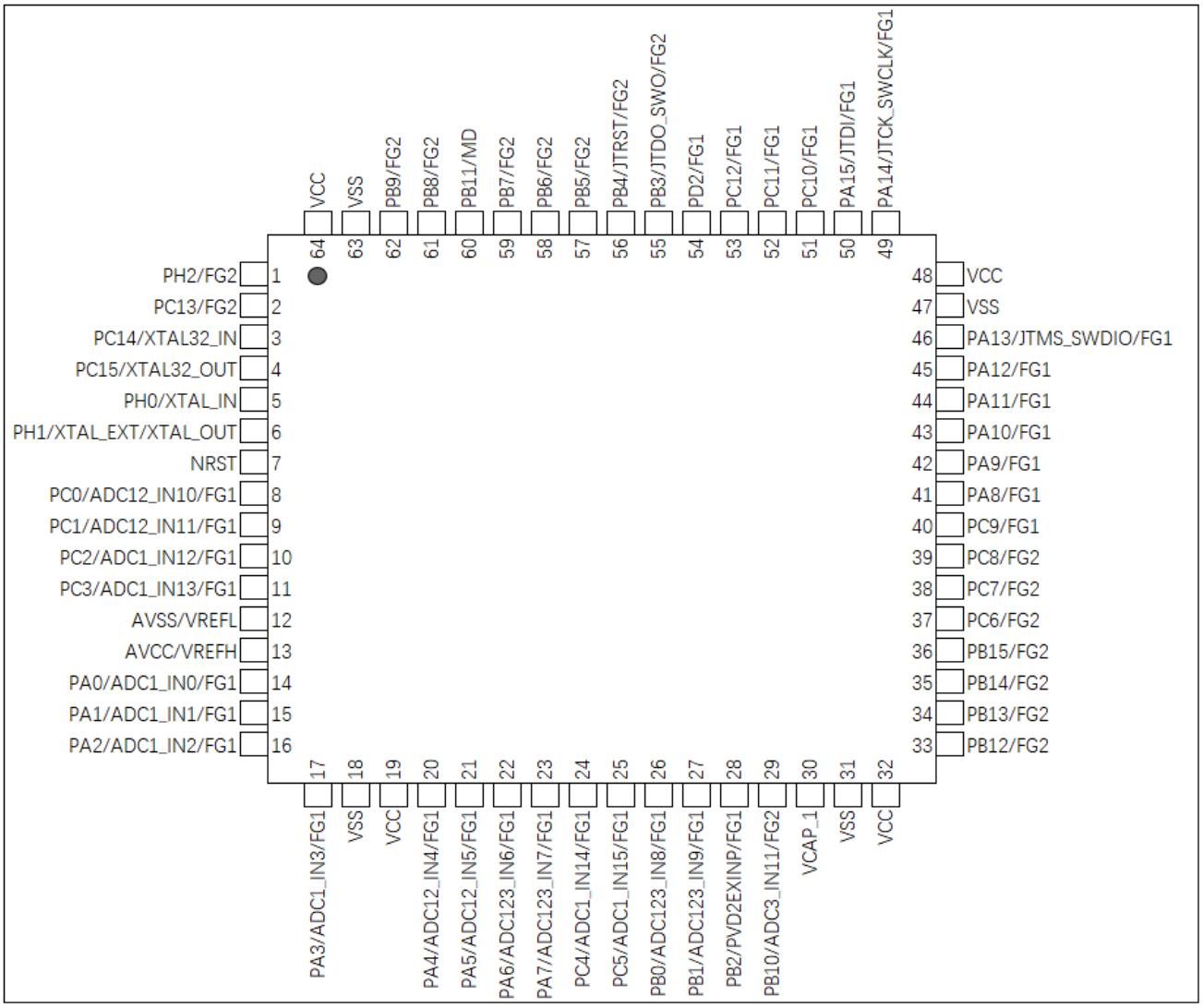
2 Pin Configuration and Functions (Pinouts)

2.1 Pin Configuration Diagram

LQFP80



LQFP64


1 PH2/FG2
2 PC13/FG2
3 PC14/XTAL32_IN
4 PC15/XTAL32_OUT
5 PH0/XTAL_IN
6 PH1/XTAL_EXT/XTAL_OUT
7 NRST
8 PC0/ADC12_IN10/FG1
9 PC1/ADC12_IN11/FG1
10 PC2/ADC1_IN12/FG1
11 PC3/ADC1_IN13/FG1
12 AVSS/VREFL
13 AVCC/VREFH
14 PA0/ADC1_IN0/FG1
15 PA1/ADC1_IN1/FG1
16 PA2/ADC1_IN2/FG1
17 PA3/ADC1_IN3/FG1
18 VSS
19 VCC
20 PA4/ADC12_IN4/FG1
21 PA5/ADC12_IN5/FG1
22 PA6/ADC123_IN6/FG1
23 PA7/ADC123_IN7/FG1
24 PC4/ADC1_IN14/FG1
25 PC5/ADC1_IN15/FG1
26 PB0/ADC123_IN8/FG1
27 PB1/ADC123_IN9/FG1
28 PB2/PVD2EXINP/FG1
29 PB10/ADC3_IN11/FG2
30 VCAP_1
31 VSS
32 VCC
33 PB12/FG2
34 PB13/FG2
35 PB14/FG2
36 PB15/FG2
37 PC6/FG2
38 PC7/FG2
39 PC8/FG2
40 PC9/FG1
41 PA8/FG1
42 PA9/FG1
43 PA10/FG1
44 PA11/FG1
45 PA12/FG1
46 PA13/JTMS_SWDIO/FG1
47 VSS
48 VCC
49 PA14/JTCK_SWCLK/FG1
50 PA15/JTDI/FG1
51 PC10/FG1
52 PC11/FG1
53 PC12/FG1
54 PD2/FG1
55 PB3/JTDO_SWO/FG2
56 PB4/JTRST/FG2
57 PB5/FG2
58 PB6/FG2
59 PB7/FG2
60 PB11/MD
61 PB8/FG2
62 PB9/FG2
63 VSS
64 VCC

LQFP48

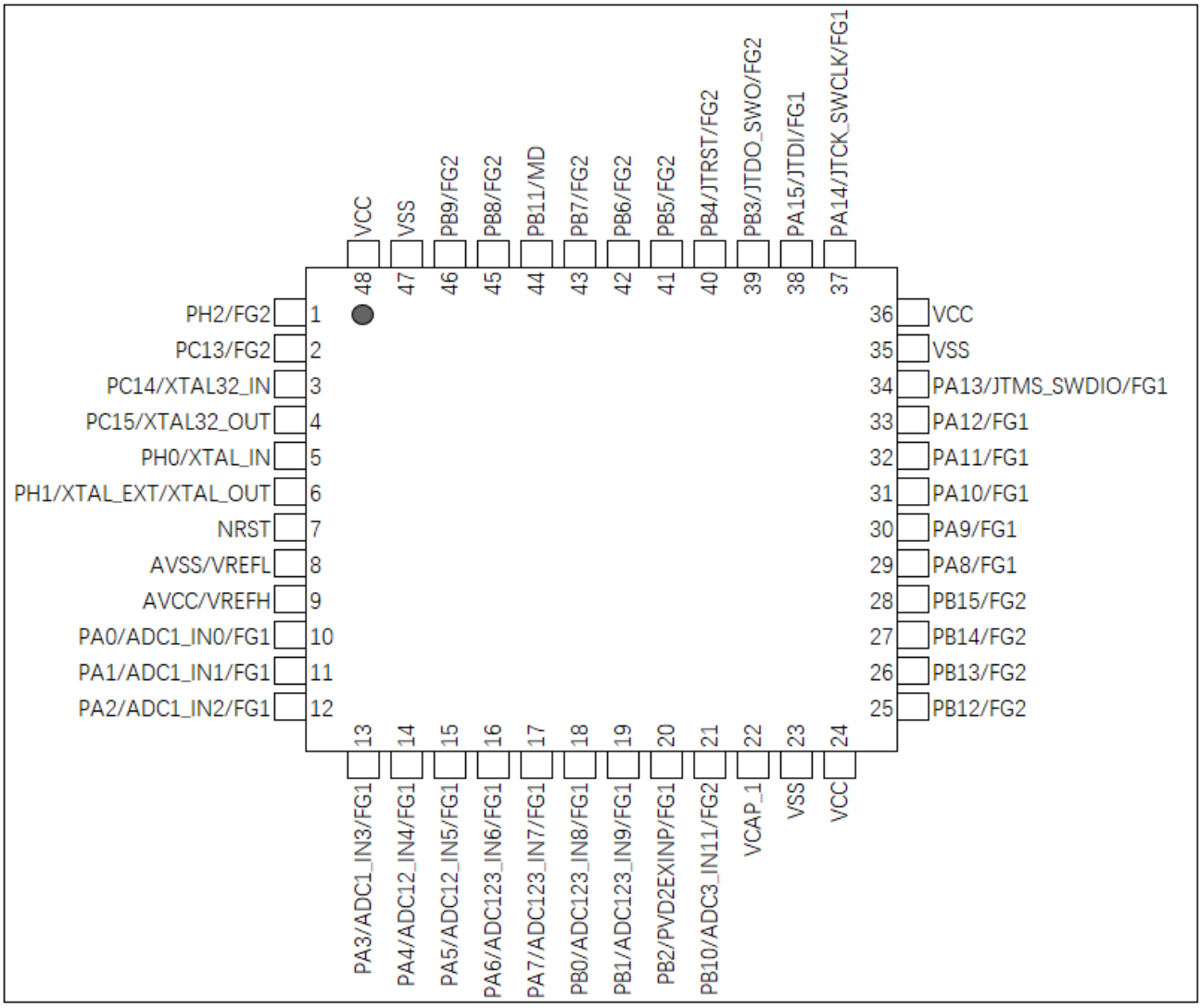


Figure 2-1 Pin Configuration Diagram

2.2 Pin Function Table

Table 2-1 Pin Function Table

LQFP 80	LQFP 64	LQFP 48	PinName	Analog	EIRQ /WKUP	TRACE /JTAG	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func 9~10	Func11	Func12	Func13	Func14	Func15	Func 16~20	Func21	Func22	Func 23~31	Func Group
							GPO	other	TIM4, VCOUT	TIM4, TIM6	TIMA	TIMA	EMB, TIMA	USART,SPI, QSPI	KEY, USART	-	TIM4, TIMA	EXMC, TIMA	TIM6, TIMA	EVNTPT	EVENTOUT	-	PLUIN	PLUOUT		
1	-	-	PE2	ADC3_IN0	EIRQ2	TRACE CLK			TIM4_2_PCT		TIMA_3_PWM5			USART3_CK	USART6_RTS						EVENTOUT		PLU0_INA	PLU0_OUT		FG2
2	-	-	PE3	ADC3_IN1	EIRQ3	TRACE D0			TIM4_2_ADSM		TIMA_3_PWM6			USART4_CK	USART5_RTS						EVENTOUT		PLU0_INB	PLU1_OUT		FG2
3	-	-	PE4	ADC3_IN2	EIRQ4	TRACE D1		CTCREF	TIM4_1_PCT	TIM4_2_OWL	TIMA_3_PWM7			USART6_CK							EVENTOUT		PLU0_INC	PLU2_OUT		FG2
4	1	1	PH2		EIRQ2	TRACE D2		FCMREF	TIM4_2_CLK		TIMA_4_PWM7	TIMA_3_TRIG	EMB_IN4	USART4_CK	USART6_CTS		TIMA_4_TRIG				EVENTOUT		PLU0_IND	PLU3_OUT		FG2
5	2	2	PC13		EIRQ13	TRACE D3		RTC_OUT	VCOUT4	TIM4_1_OXL	TIMA_4_PWM8	TIMA_2_PWM2/CLKB		USART5_CK	USART6_RTS		TIM4_1_ADSM	EXMC_AD D16		EVNTP313			PLU1_INA	PLU0_OUT		FG2
6	3	3	PC14	XTAL32_IN	EIRQ14			CTCREF	TIM4_1_OVH	TIM4_3_OXH	TIMA_4_PWM5				USART5_CTS		TIM4_1_OXH	EXMC_BA A		EVNTP314			PLU1_INB	PLU1_OUT		
7	4	4	PC15	XTAL32_OUT	EIRQ15				TIM4_1_OWH	TIM4_3_OXL	TIMA_4_PWM6				USART5_RTS		TIM4_1_CLK	EXMC_ALE		EVNTP315			PLU1_INC	PLU2_OUT		
8	5	5	PH0	XTAL_IN	EIRQ0				TIM4_3_OXL			TIMA_5_PWM3											PLU1_IND	PLU3_OUT		
9	6	6	PH1	XTAL_EXT/XTAL_OUT	EIRQ1				TIM4_3_CLK			TIMA_5_PWM4											PLU2_INA	PLU0_OUT		
10	7	7	NRST																							
11	8	-	PC0	ADC12_IN10+CMP3_INP3+CMP4_INP3	EIRQ0				TIM4_3_PCT		TIMA_2_PWM5							EXMC_RB 0		EVNTP300	EVENTOUT		PLU2_INB	PLU1_OUT		FG1
12	9	-	PC1	ADC12_IN11	EIRQ1				TIM4_3_ADSM		TIMA_2_PWM6							EXMC_CLK		EVNTP301	EVENTOUT		PLU2_INC	PLU2_OUT		FG1
13	10	-	PC2	ADC1_IN12	EIRQ2				TIM4_3_OXH		TIMA_2_PWM7		EMB_IN3					EXMC_CE 4		EVNTP302	EVENTOUT		PLU2_IND	PLU3_OUT		FG1
14	11	-	PC3	ADC1_IN13+CMP1_INM2	EIRQ3			MCO_2	TIM4_3_OXL		TIMA_2_PWM8							EXMC_CE 5		EVNTP303	EVENTOUT		PLU3_INA	PLU0_OUT		FG1
15	-	-	VCC																							
16	12	8	AVSS/ VREFL																							
17	13	9	AVCC/ VREFH																							
18	14	10	PA0	ADC1_IN0 +CMP1_INP1	EIRQ0+WKUP0_0			TIM4_1_OVH	TIM4_2_OUH		TIMA_2_PWM1/CLKA	TIMA_1_PWM1/CLKA	TIMA_2_TRIG	SPI1_NSS1	USART3_CTS			EXMC_AD D17		EVNTP100	EVENTOUT		PLU3_INB	PLU1_OUT		FG1
19	15	11	PA1	ADC1_IN1 +CMP1_INP2	EIRQ1				TIM4_2_OUL		TIMA_2_PWM2/CLKB	TIMA_3_TRIG		SPI1_NSS2	USART5_CTS			EXMC_AD D18		EVNTP101	EVENTOUT		PLU3_INC	PLU2_OUT		FG1

LQFP 80	LQFP 64	LQFP 48	PinName	Analog	EIRQ /WKUP	TRACE /JTAG	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func 9~10	Func11	Func12	Func13	Func14	Func15	Func 16~20	Func21	Func22	Func 23~31	Func Group
							GPO	other	TIM4, VCOUT	TIM4, TIM6	TIMA	TIMA	EMB, TIMA	USART,SPI, QSPI	KEY, USART	-	TIM4, TIMA	EXMC, TIMA	TIM6, TIMA	EVNTPT	EVENTOUT	-	PLUIN	PLUOUT		
20	16	12	PA2	ADC1_IN2 +CMP1_INP3	EIRQ2				TIM4_2_OVH		TIMA_2_PWM3	TIMA_5_PWM1/CLKA		SPI1_NSS3	USART6_CTS			EXMC_AD D19		EVNTP102	EVENTOUT		PLU3_IND	PLU3_OUT		FG1
21	17	13	PA3	ADC1_IN3 +CMP1_INP4 +CMP2_INP4	EIRQ3				TIM4_2_OVL		TIMA_2_PWM4	TIMA_5_PWM2/CLKB		USART5_CK	USART3_RTS			EXMC_AD D20		EVNTP103	EVENTOUT		PLU0_INA	PLU0_OUT		FG1
22	18	-	VSS																							
23	19	-	VCC																							
24	20	14	PA4	ADC12_IN4 +CMP2_INP1 +CMP3_INP4 +DAC_OUT1	EIRQ4			TIM4_1_OWH	TIM4_2_OWH			TIMA_3_PWM5		USART2_CK	KEYOUT0			EXMC_CE 0		EVNTP104	EVENTOUT		PLU0_INB	PLU1_OUT		FG1
25	21	15	PA5	ADC12_IN5+CMP2_INP2+DAC_OUT2	EIRQ5				TIM4_2_OWL		TIMA_2_PWM1/CLKA	TIMA_3_PWM6	TIMA_2_TRIG	SPI3_NSS1	KEYOUT1			EXMC_DA TA7		EVNTP105	EVENTOUT		PLU0_INC	PLU2_OUT		FG1
26	22	16	PA6	ADC123_IN6+CMP2_INP3	EIRQ6				TIM4_2_ADSM	TIM4_1_PCT		TIMA_3_PWM1/CLKA	EMB_IN2	SPI3_NSS2	KEYOUT2			EXMC_DA TA0		EVNTP106	EVENTOUT		PLU0_IND	PLU3_OUT		FG1
27	23	17	PA7	ADC123_IN7+CMP1234_INM1	EIRQ7				TIM4_1_OUL	TIM6_1_PWMB	TIMA_1_PWM5	TIMA_3_PWM2/CLKB	EMB_IN3	SPI3_NSS3	KEYOUT3			EXMC_DA TA1		EVNTP107	EVENTOUT		PLU1_INA	PLU0_OUT		FG1
28	24	-	PC4	ADC1_IN14 +CMP2_INM2	EIRQ4				TIM4_2_OUH			TIMA_3_PWM7		USART1_CK				EXMC_DA TA8		EVNTP304	EVENTOUT		PLU1_INB	PLU1_OUT		FG1
29	25	-	PC5	ADC1_IN15 +CMP3_INM2	EIRQ5				TIM4_2_OUL			TIMA_3_PWM8						EXMC_DA TA9		EVNTP305	EVENTOUT		PLU1_INC	PLU2_OUT		FG1
30	26	18	PB0	ADC123_IN8+CMP3_INP1	EIRQ0				TIM4_1_OVL	TIM6_2_PWMB	TIMA_1_PWM6	TIMA_3_PWM3		USART4_CK	KEYOUT4			EXMC_DA TA2		EVNTP200	EVENTOUT		PLU1_IND	PLU3_OUT		FG1
31	27	19	PB1	ADC123_IN9+CMP3_INP2+CMP4_INP2	EIRQ1+WKUP0_1			CTCREF	TIM4_1_OWL		TIMA_1_PWM7	TIMA_3_PWM4	TIMA_4_PWM4	QSPI_NSS	KEYOUT5			EXMC_DA TA3		EVNTP201	EVENTOUT		PLU2_INA	PLU0_OUT		FG1
32	28	20	PB2	PVD2EXINP	EIRQ2+WKUP0_2			VCOUT	TIM4_1_PCT	TIM6_TRIGB	TIMA_1_PWM8	TIMA_5_PWM2/CLKB	EMB_IN1	QSPI_IO3						EVNTP202	EVENTOUT		PLU2_INB	PLU1_OUT		FG1
33	-	-	PE12	ADC3_IN3	EIRQ12				TIM4_1_OWL		TIMA_1_PWM7			SPI1_NSS1				EXMC_DA TA10			EVENTOUT		PLU2_INC	PLU2_OUT		FG2
34	-	-	PE13	ADC3_IN4	EIRQ13				TIM4_1_OWH		TIMA_1_PWM3			SPI1_NSS2				EXMC_DA TA11			EVENTOUT		PLU2_IND	PLU3_OUT		FG2
35	-	-	PE14	ADC3_IN5	EIRQ14			ADTRG1	TIM4_1_CLK		TIMA_1_PWM4			SPI1_NSS3				EXMC_DA TA12			EVENTOUT		PLU3_INA	PLU0_OUT		FG2
36	-	-	PE15	ADC3_IN10	EIRQ15			ADTRG3			TIMA_1_PWM8	TIMA_5_TRIG	EMB_IN2	USART4_CK				EXMC_DA TA13			EVENTOUT		PLU3_INB	PLU1_OUT		FG2
37	29	21	PB10	ADC3_IN11	EIRQ10			ADTRG2	TIM4_2_OVH	TIM4_1_OXL	TIMA_2_PWM3	TIMA_5_PWM8	TIMA_1_PWM3	QSPI_IO2				EXMC_DA TA4		EVNTP210	EVENTOUT		PLU3_INC	PLU2_OUT		FG2
38	30	22	VCAP_1																							
39	31	23	VSS																							
40	32	24	VCC																							
41	33	25	PB12		EIRQ12			VCOUT1	TIM4_2_OVL	TIM6_TRIGB	TIMA_1_PWM8	TIMA_5_TRIG	EMB_IN2	QSPI_IO1	USART5_CTS			EXMC_DA TA5		EVNTP212	EVENTOUT		PLU3_IND	PLU3_OUT		FG2

LQFP 80	LQFP 64	LQFP 48	PinName	Analog	EIRQ /WKUP	TRACE /JTAG	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func 9~10	Func11	Func12	Func13	Func14	Func15	Func 16~20	Func21	Func22	Func 23~31	Func Group
							GPO	other	TIM4, VCOUT	TIM4, TIM6	TIMA	TIMA	EMB, TIMA	USART,SPI, QSPI	KEY, USART	-	TIM4, TIMA	EXMC, TIMA	TIM6, TIMA	EVNTPT	EVENTOUT	-	PLUIN	PLUOUT		
42	34	26	PB13		EIRQ13			VCOUT2	TIM4_1_OUL	TIM6_1_PWMB	TIMA_1_PWM5	TIMA_4_PWM1/CLKA	TIMA_3_PWM1/CLKA	QSPI_IO0	USART5_RTS					EVNTP213	EVENTOUT		PLU0_INA	PLU0_OUT		FG2
43	35	27	PB14		EIRQ14			VCOUT3	TIM4_1_OVL	TIM6_2_PWMB	TIMA_1_PWM6	TIMA_4_PWM2/CLKB	TIMA_3_PWM2/CLKB	QSPI_SCK	USART6_CTS					EVNTP214	EVENTOUT		PLU0_INB	PLU1_OUT		FG2
44	36	28	PB15		EIRQ15			RTC_OUT	TIM4_1_OWL		TIMA_1_PWM7		EMB_IN4	USART3_CK	USART6_RTS		TIMA_1_PWM2/CLKB	TIMA_2_PWM2/CLKB	TIM6_2_PWMA	EVNTP215	EVENTOUT		PLU0_INC	PLU2_OUT		FG2
45	-	-	PD8		EIRQ8				TIM4_3_OUL	TIM4_2_OWL				QSPI_IO0	KEYOUT7		TIM4_1_OXH			EVNTP408	EVENTOUT		PLU0_IND	PLU3_OUT		FG2
46	-	-	PD9		EIRQ9				TIM4_3_OVL	TIM4_2_OVL				QSPI_IO1	KEYOUT6		TIM4_1_OXL			EVNTP409	EVENTOUT		PLU1_INA	PLU0_OUT		FG2
47	-	-	PD10		EIRQ10				TIM4_3_OWL					QSPI_IO2	KEYOUT5		TIM4_2_OXH			EVNTP410	EVENTOUT		PLU1_INB	PLU1_OUT		FG2
48	-	-	PD11		EIRQ11				TIM4_3_CLK					QSPI_IO3	KEYOUT4		TIM4_2_OXL			EVNTP411	EVENTOUT		PLU1_INC	PLU2_OUT		FG2
49	37	-	PC6		EIRQ6			CTCREF	TIM4_2_ADSM	TIM4_1_CLK	TIMA_3_PWM1/CLKA	TIMA_5_PWM8		QSPI_SCK	KEYOUT3					EVNTP306	EVENTOUT		PLU1_IND	PLU3_OUT		FG2
50	38	-	PC7		EIRQ7				TIM4_2_CLK	TIM4_3_OVH	TIMA_3_PWM2/CLKB	TIMA_5_PWM7		QSPI_NSS	KEYOUT2					EVNTP307	EVENTOUT		PLU2_INA	PLU0_OUT		FG2
51	39	-	PC8		EIRQ8				TIM4_2_OWH	TIM4_3_OVL	TIMA_3_PWM3	TIMA_5_PWM6		USART3_CK	KEYOUT1			EXMC_DATA14		EVNTP308	EVENTOUT		PLU2_INB	PLU1_OUT		FG2
52	40	-	PC9		EIRQ9			MCO_2	TIM4_2_OWL	TIM4_3_OUL	TIMA_3_PWM4	TIMA_5_PWM5			KEYOUT0			EXMC_DATA15		EVNTP309	EVENTOUT		PLU2_INC	PLU2_OUT		FG1
53	41	29	PA8	CMP4_INM2	EIRQ8+WKUP2_0			MCO_1	TIM4_1_OUH	TIM6_1_PWMA	TIMA_1_PWM1/CLKA	TIMA_2_PWM1/CLKA		USART1_CK						EVNTP108	EVENTOUT		PLU2_IND	PLU3_OUT		FG1
54	42	30	PA9	CMP4_INP1	EIRQ9+WKUP2_1			CTCREF	TIM4_1_OVH	TIM6_2_PWMA	TIMA_1_PWM2/CLKB									EVNTP109	EVENTOUT		PLU3_INA	PLU0_OUT		FG1
55	43	31	PA10	CMP4_INP4	EIRQ10+WKUP2_2			CTCREF	TIM4_1_OWH	TIM4_3_CLK	TIMA_1_PWM3	TIMA_5_TRIG		USART6_CK						EVNTP110	EVENTOUT		PLU3_INB	PLU1_OUT		FG1
56	44	32	PA11		EIRQ11+WKUP2_3			TIM4_1_OXL	TIM4_1_CLK	TIM6_TRIGA	TIMA_1_PWM4	TIMA_5_PWM1/CLKA	EMB_IN1	USART5_CK	USART3_RTS					EVNTP111	EVENTOUT		PLU3_INC	PLU2_OUT		FG1
57	45	33	PA12		EIRQ12+WKUP3_0			TIM4_1_ADSM	TIM4_3_OWL	TIM6_TRIGA	TIMA_1_TRIG		TIMA_2_TRIG	USART6_CK	USART3_CTS		TIM4_2_PCT	EXMC_DATA6	TIMA_3_PWM1/CLKA	EVNTP112	EVENTOUT		PLU3_IND	PLU3_OUT		FG1
58	46	34	PA13		EIRQ13+WKUP3_1	JTMS_SWDIO			TIM4_3_ADSM		TIMA_2_PWM5			SPI2_NSS1			TIMA_5_TRIG	EXMC_DATA7		EVNTP113	EVENTOUT		PLU0_INA	PLU0_OUT		FG1
59	47	35	VSS																							
60	48	36	VCC																							
61	49	37	PA14		EIRQ14+WKUP3_2	JTCK_SWCLK			TIM4_3_PCT		TIMA_2_PWM6		TIMA_4_TRIG	SPI2_NSS2				EXMC_CE0		EVNTP114	EVENTOUT		PLU0_INB	PLU1_OUT		FG1
62	50	38	PA15		EIRQ15+WKUP3_3	JTDI			TIM4_3_OXH		TIMA_2_PWM1/CLKA		TIMA_2_TRIG	SPI2_NSS3						EVNTP115	EVENTOUT		PLU0_INC	PLU2_OUT		FG1
63	51	-	PC10		EIRQ10				TIM4_3_OUH		TIMA_2_PWM7	TIMA_5_PWM1/CLKA					TIM4_2_OXL			EVNTP310	EVENTOUT		PLU0_IND	PLU3_OUT		FG1

LQFP 80	LQFP 64	LQFP 48	PinName	Analog	EIRQ /WKUP	TRACE /JTAG	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func 9~10	Func11	Func12	Func13	Func14	Func15	Func 16~20	Func21	Func22	Func 23~31	Func Group
							GPO	other	TIM4, VCOUT	TIM4, TIM6	TIMA	TIMA	EMB, TIMA	USART,SPI, QSPI	KEY, USART	-	TIM4, TIMA	EXMC, TIMA	TIM6, TIMA	EVNTPT	EVENTOUT	-	PLUIN	PLUOUT		
64	52	-	PC11		EIRQ11				TIM4_3_OVH		TIMA_2_PWM8	TIMA_5_PWM2/CLKB					TIM4_2_OXH			EVNTP311	EVENTOUT		PLU1_INA	PLU0_OUT		FG1
65	53	-	PC12		EIRQ12				TIM4_3_OWH	TIM4_2_PCT	TIMA_4_TRIG	TIMA_5_PWM3					TIM4_1_OXL			EVNTP312	EVENTOUT		PLU1_INB	PLU1_OUT		FG1
66	-	-	PD0		EIRQ0			VCOUT	TIM4_2_OUL	TIM4_3_OUH		TIMA_5_PWM4								EVNTP400	EVENTOUT		PLU1_INC	PLU2_OUT		FG1
67	-	-	PD1		EIRQ1				TIM4_2_OWH	TIM4_3_OWH	TIMA_3_TRIG									EVNTP401	EVENTOUT		PLU1_IND	PLU3_OUT		FG1
68	54	-	PD2		EIRQ2				TIM4_1_OXH	TIM4_2_OVH	TIMA_2_PWM4									EVNTP402	EVENTOUT		PLU2_INA	PLU0_OUT		FG1
69	55	39	PB3		EIRQ3+WKUP0_3	JTDO_TRACESWO		FCMREF	TIM4_3_CLK		TIMA_2_PWM2/CLKB									EVNTP203	EVENTOUT		PLU2_INB	PLU1_OUT		FG2
70	56	40	PB4		EIRQ4+WKUP1_0	NJTRST			TIM4_3_OWL		TIMA_3_PWM1/CLKA									EVNTP204	EVENTOUT		PLU2_INC	PLU2_OUT		FG2
71	57	41	PB5		EIRQ5+WKUP1_1			ADTRG3	TIM4_3_OWH	TIM6_1_PWMA	TIMA_3_PWM2/CLKB	TIMA_3_TRIG	TIMA_4_TRIG	USART4_CK			TIM4_1_OXH		TIMA_1_PWM2/CLKB	EVNTP205	EVENTOUT		PLU2_IND	PLU3_OUT		FG2
72	58	42	PB6		EIRQ6+WKUP1_2			ADTRG2	TIM4_3_OVL		TIMA_4_PWM1/CLKA						TIM4_1_OXL			EVNTP206	EVENTOUT		PLU3_INA	PLU0_OUT		FG2
73	59	43	PB7		EIRQ7+WKUP1_3			ADTRG1	TIM4_3_OVH		TIMA_4_PWM2/CLKB						TIM4_2_OXH	EXMC_ADV		EVNTP207	EVENTOUT		PLU3_INB	PLU1_OUT		FG2
74	60	44	PB11/MD																	EVNTP211			PLU3_INC	PLU2_OUT		
75	61	45	PB8		EIRQ8				TIM4_3_OUL		TIMA_4_PWM3			USART5_CK	KEYOUT7		TIM4_2_OXL	EXMC_WE		EVNTP208	EVENTOUT		PLU3_IND	PLU3_OUT		FG2
76	62	46	PB9		EIRQ9				TIM4_3_OUH		TIMA_4_PWM4		EMB_IN4	SPI2_NSS1	KEYOUT6		TIM4_1_ADSM	EXMC_OE		EVNTP209	EVENTOUT		PLU0_INA	PLU0_OUT		FG2
77	-	-	PE0		EIRQ0			MCO_1	TIM4_1_ADSM		TIMA_4_TRIG			SPI2_NSS2							EVENTOUT		PLU0_INB	PLU1_OUT		FG2
78	-	-	PE1		EIRQ1			MCO_2	TIM4_3_CLK					SPI2_NSS3			TIM4_2_OUH				EVENTOUT		PLU0_INC	PLU2_OUT		FG2
79	63	47	VSS																							
80	64	48	VCC																							

Note:

– *In the above table, Func32~63 are mainly serial communication functions (including USART, SPI, I2C, and MCAN), which are divided into two groups of FunctionGroups, referred to as FG1 and FG2. Please refer to Table 2-2 for details.*

Table 2-2 Func32~63 table

	Func32	Func33	Func34	Func35	Func36	Func37	Func38	Func39	Func40	Func41	Func42	Func43	Func44	Func45	Func46	Func47
FG1	USART1_TX	USART1_RX	USART1_RTS	USART1_CTS	USART2_TX	USART2_RX	USART2_RTS	USART2_CTS	SPI1_MOSI	SPI1_MISO	SPI1_NSS0	SPI1_SCK	SPI2_MOSI	SPI2_MISO	SPI2_NSS0	SPI2_SCK
FG2	USART3_TX	USART3_RX	USART3_RTS	USART3_CTS	USART4_TX	USART4_RX	USART4_RTS	USART4_CTS	SPI3_MOSI	SPI3_MISO	SPI3_NSS0	SPI3_SCK	SPI1_MOSI	SPI1_MISO	SPI1_NSS0	SPI1_SCK

	Func48	Func49	Func50	Func51	Func52	Func53	Func54	Func55	Func56	Func57	Func58	Func59	Func60	Func61	Func62	Func63
FG1	I2C1_SDA	I2C1_SCL	I2C2_SDA	I2C2_SCL	USART3_TX	USART3_RX	USART6_TX	USART6_RX	MCAN1_TX	MCAN1_RX	-	-	-	-	-	-
FG2	I2C1_SDA	I2C1_SCL	MCAN1_TX	MCAN1_RX	USART5_TX	USART5_RX	USART6_TX	USART6_RX	MCAN2_TX	MCAN2_RX	-	-	-	-	-	-

Table 2-3 Port Configuration

Package	Port Group	Bits																Pin Count Total	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
LQFP80	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	67
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	-	-	-	-	o	o	o	o	-	-	-	-	-	o	o	o	7	
	PortE	o	o	o	o	-	-	-	-	-	-	-	o	o	o	o	o	9	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	3	
LQFP64	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	52
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	-	-	-	-	-	-	-	-	-	-	-	-	-	o	-	-	1	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	3	
LQFP48	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	38
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	-	-	-	-	-	-	-	-	-	-	-	-	-	3	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	3	
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	-	-	-	-	-	-	-	-	-	-	-	-	-	3	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	3	
	PortB	o	o	o	o	o	o	-	-	-	-	o	o	o	o	o	-	11	
	PortC	o	o	o	-	-	-	-	-	-	-	-	-	-	-	-	-	3	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	3	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		

Table 2-4 Common Functional Specifications

Port		Pull-up/ Pull-down	Open-Drain Output	Driving Capacity	5V Withstand Voltage
PortA	PA0~PA6, PA9~PA15	Support	Support	Low, Medium, High	Support
	PA7, PA8	Support	Support	Low, Medium, High	not support
PortB	PB0~PB15	Support	Support	Low, Medium, High	Support
PortC	PC0~PC2, PC6~PC15	Support	Support	Low, Medium, High	Support
	PC3~PC5	Support	Support	Low, Medium, High	not support
PortD	PD0~PD2, PD8~11	Support	Support	Low, Medium, High	Support
PortE	PE0~PE5, PE12~15	Support	Support	Low, Medium, High	Support
PortH	PH0~PH2	Support	Support	Low, Medium, High	Support

Note:

– *When used as an analog function, the input voltage must not be higher than AVCC/ VREFH.*

2.3 Pin Function Description

Table 2-5 Pin Function Description

Categories	Functional name	I/O	Note
Power System	VCC	I	Power supply
	VSS	I	Source ground
	VCAP_1	IO	Core voltage
	AVCC/VREFH	I	Analog Power Supply/Analog Reference Voltage
	AVSS/VREFL	I	Analog Power Ground/Analog Reference Voltage
	NRST	I	Reset terminal, low effective
	MD	I	Mode terminal
PVD	PVD2EXINP	I	PVD2 external input comparison voltage
Clock	XTAL_IN	I	External master clock oscillator interface
	XTAL_EXT/XTAL_OUT	O	XTAL_EXT external clock input
	XTAL32_IN	I	External sub clock (32KHz) oscillator interface
	XTAL32_OUT	O	
	MCO_x (x=1~2)	O	Internal clock output
GPIO	GPIOxy (x=A~E, H y=0~15)	IO	General input/output
EVENTOUT	EVENTOUT	O	Cortex-M4 CPU event output
EIRQ	EIRQx (x=0~15)	I	Shielded external interrupt
	WKUPx_y (x=0~3 y=0~3)	I	Power Down mode external wake-up input
Event Port	EVNTPxy (x=1~4 y=0~15)	IO	Event port input and output functions
Key	KEYOUTx (x=0~7)	O	KEYSCAN scan output signal
JTAG/ SWD	JTCK_SWCLK	I	Online debugging interface
	JTMS_SWDIO	IO	
	JTDO_TRACESWO	O	
	JTDI	I	
	NJTRST	I	
TRACE	TRACECLK	O	Trace debug sync clock output
	TRACEDx (x=0~3)	O	Trace debug data output
FCM	FCMREF	I	The external pin input reference clock of clock frequency measurement function
RTC	RTC_OUT	O	1Hz clock output
Timer4 (<t>=1~3)	TIM4_<t>_CLK	I	Counting clock port input
	TIM4_<t>_OUH	IO	PWM port U-phase output
	TIM4_<t>_OUL	IO	PWM port U-phase output
	TIM4_<t>_OVH	IO	PWM port V-phase output
	TIM4_<t>_OVL	IO	PWM port V-phase output
	TIM4_<t>_OWH	IO	PWM port W-phase output
	TIM4_<t>_OWL	IO	PWM port W-phase output

Categories	Functional name	I/O	Note
Timer4 (<t>=1~3)	TIM4_<t>_OXH	IO	PWM port X-phase output
	TIM4_<t>_OXL	IO	PWM port X-phase output
	TIM4_<t>_ADSM	O	Dedicated event output monitoring
	TIM4_<t>_PCT	O	PWM period output monitoring
Timer6 (<t>=1~2)	TIM6_TRIGA	I	External event trigger A input
	TIM6_TRIGB	I	External event trigger B input
	TIM6_<t>_PWMA	IO	External Event Trigger Input or PWM Port Output
	TIM6_<t>_PWMB	IO	External Event Trigger Input or PWM Port Output
TimerA (<t>=1~5)	TIMA_<t>_TRIG	I	External event trigger input
	TIMA_<t>_PWM1/CLKA	IO	External event trigger input or PWM port output or count clock port input
	TIMA_<t>_PWM2/CLKB	IO	External event trigger input or PWM port output or count clock port input
	TIMA_<t>_PWMy (y=3~8)	IO	External Event Trigger Input or PWM Port Output
EMB	EMB_INx (x=1~4)	I	Port input control signal
USARTx (x=1~6)	USARTx_TX	IO	Send data
	USARTx_RX	IO	Receiving data
	USARTx_CK	IO	Communication clock
	USARTx_RTS	O	Request to send a signal
	USARTx_CTS	I	Clear Send Signal
SPIx (x=1~3)	SPIx_MISO	IO	Primary input/secondary output data transfer pin
	SPIx_MOSI	IO	Primary output/slave input data transfer pin
	SPIx_SCK	IO	Transmission clock
	SPIx_NSS0	IO	Select input/output pin from machine
	SPIx_NSSy (y=1~3)	O	Slave select output pin
QSPI	QSPI_IOx (x=0~3)	IO	Data line
	QSPI_SCK	O	clock output
	QSPI_NSS	O	Slave selection
I2Cx (x=1~2)	I2Cx_SCL	IO	Clock line
	I2Cx_SDA	IO	Data line
MCANx (x=1~2)	MCANx_TX	O	Send data
	MCANx_RX	I	Receiving data
CMP	VCOUT1	O	CMP1 result output
	VCOUT2	O	CMP2 result output
	VCOUT3	O	CMP3 result output
	VCOUT4	O	CMP4 result output
	VCOUT	O	CMP1~4 result logic or output
	CMPx_INPy (x=1~4 y=1~4)	I	CMPx positive analog input
	CMPx_INM2 (x=1~4)	I	CMPx negative analog input
	CMP1234_INM1	I	CMP1~4 negative terminal analog input

Categories	Functional name	I/O	Note
ADC	ADTRG1	I	ADC1 AD conversion external start source
	ADTRG2	I	ADC2 AD conversion external start source
ADC	ADTRG3	I	ADC3 AD conversion external start source
	ADC123_INx (x=6~9)	I	ADC1/2/3 share external analog input port
	ADC12_INx (x=4~5, 10~11)	I	ADC1/2 share external analog input port
	ADC1_INx (x=0~3, 12~15)	I	ADC1 external analog input port
	ADC3_INx (x=0~5, 10, 11)	I	ADC3 external analog input port
DAC	DAC_OUTy (y=1, 2)	O	DAC analog output
EXMC	EXMC_CLK	IO	For details, refer to Table 30-4 in Chapter EXMC of the reference manual.
	EXMC_OE	O	
	EXMC_WE	O	
	EXMC_ALE	O	
	EXMC_BAA	O	
	EXMC_ADV	O	
	EXMC_CEx (x=0, 4~5)	O	
	EXMC_RB0	I	
	EXMC_ADDx (x=16~20)	O	
	EXMC_DATAx (x=0~15)	IO	
PLU	PLUx_INy (x=0~3 y=A~D)	I	Input of logic operation unit PLU
	PLUx_OUT (x=0~3)	O	The output of the logical operation unit PLU

2.4 Pin Usage Instructions

Table 2-6 Pin Usage Description

Pin Name	Usage Notes
VCC	Power supply, connected to a voltage of 1.8V~3.6V, and a decoupling capacitor connected to the VSS pin nearby (refer to [Electrical Characteristics (ECs)])
VSS	Source ground, connected to 0V
VCAP_1	For the core voltage, connect a capacitor to the VSS pin nearby to stabilize the core voltage (refer to [Electrical Characteristics (ECs)])
AVCC	Analog power supply, supplying power to analog modules, connected to the same voltage as VCC (refer to [Electrical Characteristics (ECs)]) When not using the analog module, please short it with VCC
AVSS	Analog power ground, which supplies power to the analog modules and connects to the same voltage as VSS (refer to [Electrical Characteristics (ECs)]) When not using the analog module, please short it with VSS
PB11/ MD	Analog input. When the reset pin (NRST) is released (from low level to high level), this pin must be fixed at low level. It is recommended to connect a resistor (4.7KΩ) to VSS (pull-down)
NRST	Reset pin, low effective. Resistance to VCC when not in use (pull-up)
Pxy (x=A~E, H y=0~15)	General pin. When used as an input function, the input voltage of pins that support 5V tolerance should not exceed 5V, internal pull-up/pull-down is prohibited when the input voltage exceeds VCC, and the input voltage of pins that do not support 5V tolerance should not exceed VCC. When used as an analog input, the analog voltage should not exceed VREFH/AVCC Hang out when not in use or connect to VCC (pull-up)/VSS (pull-down)

3 Electrical Characteristics (ECs)

3.1 Parameter Conditions

All voltages are referenced to VSS unless otherwise noted.

3.1.1 Minimum and Maximum

Unless otherwise specified, the minimum and maximum values of all devices are comprehensively evaluated by sample testing at the worst ambient temperature, supply voltage and clock frequency.

3.1.2 Typical Value

Unless otherwise specified, typical data are obtained by comprehensive evaluation of sample tests under the conditions of T_A=25°C and V_{CC}=3.3V.

3.1.3 Typical Curve

Unless otherwise specified, all typical curves are not tested for design reference only.

3.1.4 Load Capacitance

The load conditions used to measure the pin parameters are shown in Figure 3-1 (left).

3.1.5 Pin Input Voltage

Figure 3-1 (right) shows how to measure the input voltage at the pins of the device.

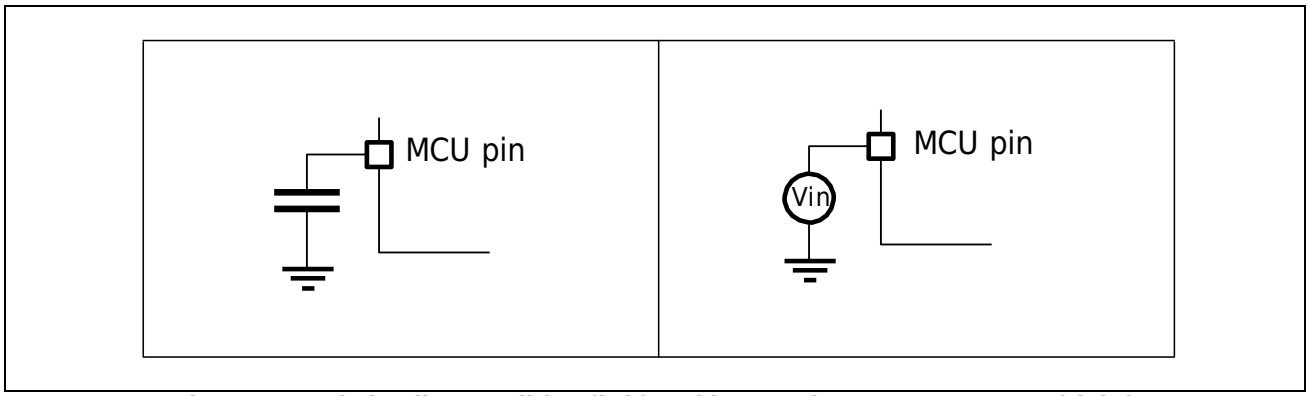


Figure 3-1 Pin loading condition (left) and input voltage measurement (right)

3.1.6 Power Supply Scheme

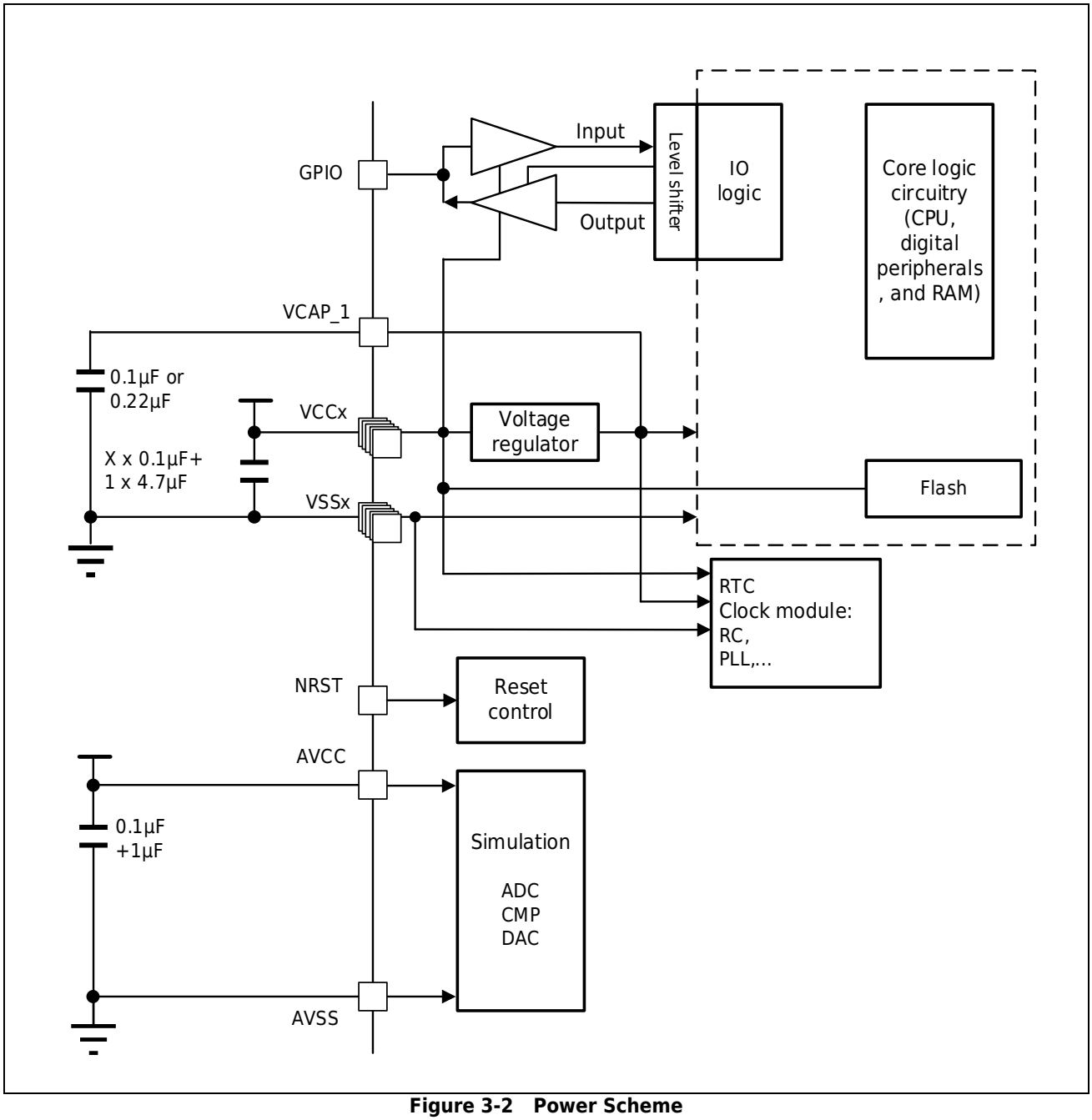


Figure 3-2 Power Scheme

1. A 4.7µF ceramic capacitor must be connected to one of the VCC pins.
2. AVSS=VSS.
3. Each supply pair (e.g. VCC/VSS, AVCC/AVSS...) must be decoupled with filter ceramic capacitors as mentioned above. These capacitors must be placed as close as possible to or under the power pair pins on the underside of the PCB to ensure proper device operation. It is not recommended to remove the filter capacitor to reduce PCB size or cost, it may cause the device not to work properly.

3.1.7 Current Consumption Measurement

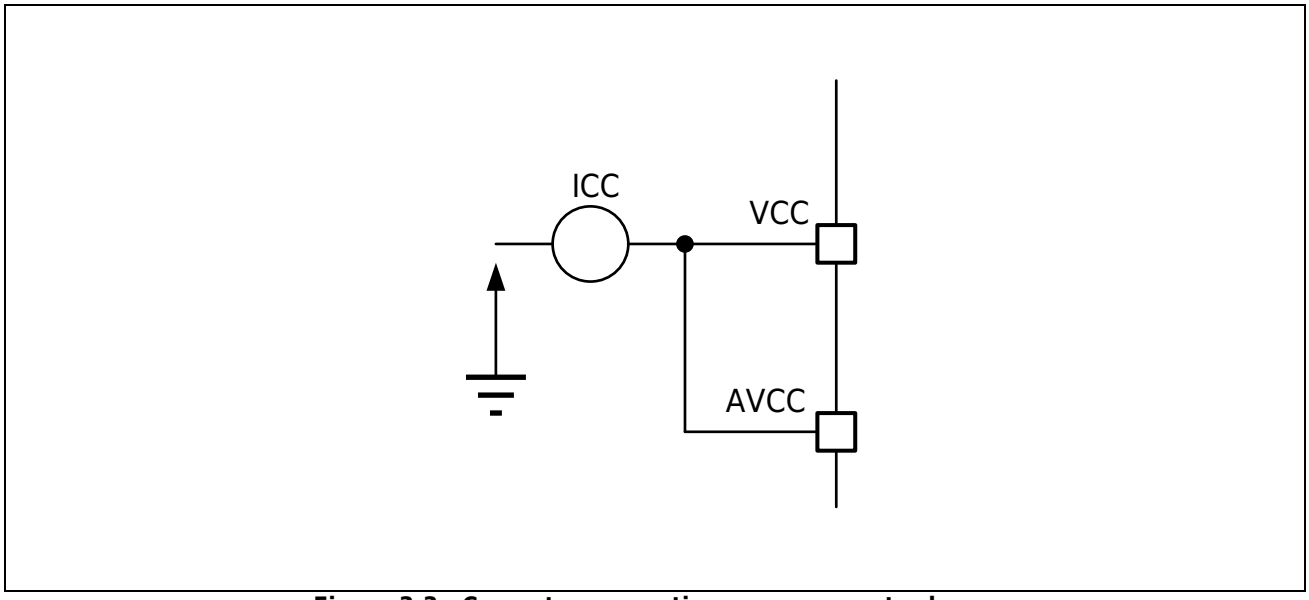


Figure 3-3 Current consumption measurement scheme

3.2 Absolute Maximum Ratings

Permanent damage to the device may result if loads exceeding the Absolute Maximum Ratings listed in Table 3-1, Table 3-2, and Table 3-3 are applied to the device. These values are just rated stresses and do not mean that the device works properly under these conditions. Long-term operation may affect the reliability.

Table 3-1 Voltage Characteristics

Symbol	Item	Minimum Value	Maximum Value	Unit
V_{CC}-V_{SS}	External main supply voltage (including AVCC, VCC) (1)	-0.3	4.0	V
V_{IN}	Input voltage on pins other than PA7,PA8,PC3~PC5(2)	V_{SS}–0.3	V_{CC}+4.0 (Maximum 5.8V)	
	Input voltage on pins PA7,PA8,PC3~PC5(2)	V_{SS}–0.3	V_{CC}+0.7 (Maximum 4.0V)	
|VSSx-VSS|	Voltage difference between different ground pins	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage	Please refer to [Electrical Sensitivity]		-

1. All main power (VCC, AVCC) and ground (VSS, AVSS) pins must always be connected to an external power supply, within the limits allowed.
2. The maximum value of V_{IN} must always be followed. For information on the maximum allowable injected current values, See Table 3-2.

Table 3-2 Current Characteristics

Symbol	Item	Maximum Value	Unit
∑IVCC	Total current flowing into all VCCX power lines (source current) (1)	240	mA
∑IVSS	Total current flowing (sinking) out of all VSSX ground wires(1)	-240	
IVCC	Maximum current into each VCCX supply line (source current)(1)	100	
IVSS	Maximum Current Out of Each VSSX Ground Line (Sink)(1)	-100	
IIO	Output current sink for any I/O and control pin	20	
	Output current source for any I/O and control pin	-20	
∑IIO	Total output sink current on all I/O and control pins (2)	120	
	Total output source current on all I/O and control pins (2)	-120	

1. All main power (VCC, AVCC) and ground (VSS, AVSS) pins must always be connected to an external power supply, within the limits allowed.
2. This total output current must be properly distributed in all power domains; this total output current applies to 64 PINs and above packages, for 48 PINs packages, the maximum total output current is ±80mA.

Table 3-3 Thermal Characteristics

Symbol	Item	Numerical Value	Unit
T_{STG}	Storage temperature range	–65~150	°C
T_J	Junction Temperature Range	-40~125	°C

3.3 Operating Conditions

3.3.1 General Working Conditions

Table 3-4 General Operating Conditions

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
f_{HCLK}	Internal AHB clock frequency	High Speed Mode (1) PWRC2.DVS=0b11 PWRC3.DDAS=0xF	-	-	200	MHz
		Super low speed mode PWRC2.DVS=0b10 PWRC3.DDAS=0x0	-	-	8	
V_{CC}	Standard operating voltage	-	1.8	-	3.6	V
V_{AVCC}	Analog working voltage	-	1.8	-	3.6	V
V_{IN}	Input voltage on 5V tolerant pin (2)(3)(4)	2V≤V_{CC}≤3.6V 2V≤V_{AVCC}≤3.6V	–0.3	-	5.5	
		V_{CC}<2V V_{AVCC}<2V	–0.3	-	5.2	
	Input voltage on non-5V tolerant pin (PA7, PA8, PC3~PC5)	-	-0.3	-	Vcc+0.3	
T_J	Junction temperature range	-	-40	-	125	°C
T_A	Operating temperature range	-	-40	-	105	°C

1. Guarantee of mass production test.
2. To keep the voltage above V_{CC}+0.3V, the internal pull-up/pull-down resistors must be disabled.
3. After the power supply (VCC, AVCC) of the device is stable, the voltage is then added to the 5V voltage pin of the device.
4. Do not connect the input voltage directly to an external power supply. It is recommended to connect the external power supply through a resistor above 100Ω.

3.3.2 Operating Conditions During Power Up/ Down

Table 3-5 Operating conditions at power-up/power-down

Symbol	Parameter	Minimum Value	Maximum Value	Unit
t_{VCC}	VCC rise time rate	20	20000	μs/V
	VCC down time rate	20	20000	

3.3.3 Reset and Power Control Block Features

Table 3-6 Reset and Power Control Module Characteristics

Symbol	Parameter	Conditions		Minimum Value	Typical Value	Maximum Value	Unit
V_{BOR}	Monitoring Voltage of BOR	High speed mode Super low speed mode	ICG1.BOR_LEV[1:0]=0b00(1)	1.70	1.90	2.10	V
			ICG1.BOR_LEV[1:0]=0b01	1.80	2.00	2.20	V
			ICG1.BOR_LEV[1:0]=0b10	1.90	2.10	2.30	V
			ICG1.BOR_LEV[1:0]=0b11(1)	2.10	2.30	2.50	V
V_{PVD1}	PVD1 Monitoring Voltage (3)	High speed mode Super low speed mode	PVD1LVL[2:0]=0b000(1)	1.80	2.00	2.20	V
			PVD1LVL[2:0]=0b001	1.90	2.10	2.30	V
			PVD1LVL[2:0]=0b010	2.10	2.30	2.50	V
			PVD1LVL[2:0]=0b011	2.33	2.55	2.77	V
			PVD1LVL[2:0]=0b100	2.43	2.65	2.87	V
			PVD1LVL[2:0]=0b101	2.53	2.75	2.97	V
			PVD1LVL[2:0]=0b110	2.63	2.85	3.07	V
			PVD1LVL[2:0]=0b111(1)	2.73	2.95	3.17	V
V_{PVD2}	PVD2 Monitoring Voltage(3)	High speed mode Super low speed mode	PVD2LVL[2:0]=0b000(1)	1.90	2.10	2.30	V
			PVD2LVL[2:0]=0b001	2.10	2.30	2.50	V
			PVD2LVL[2:0]=0b010	2.33	2.55	2.77	V
			PVD2LVL[2:0]=0b011	2.43	2.65	2.87	V
			PVD2LVL[2:0]=0b100	2.53	2.75	2.97	V
			PVD2LVL[2:0]=0b101	2.63	2.85	3.07	V
			PVD2LVL[2:0]=0b110(1)	2.73	2.95	3.17	V
			PVD2LVL[2:0]=0b111(1)(5)	0.90	1.10	1.30	V
V_{pvd}hyst	Hysteresis for PVD1/2(4)	-		-	100	-	mV
V_{POR}	Power-on/power-off reset threshold(1)	Rising edge VPOR		1.56	1.68	1.80	V
		Falling edge VPDR		1.52	1.64	1.76	V
V_{POR}hyst	POR Hysteresis	-		-	40	-	mV
I_{RUSH}	Inrush current at regulator power-up (POR or wake-up from standby)	-		-	100	150	mA
T_{NRST}	NRST reset minimum width	-		10	-	-	μs
T_{IPVD1}	PVD1 reset release time(2)	-		300	380	460	μs
T_{IPVD2}	PVD2 reset release time(2)	-		300	380	460	μs
T_{INRST}	NRST reset release time(2)	-		25	35	50	μs
T_{RIPT}	Internal reset time(2)	-		140	160	200	μs
T_{RSTBOR}	BOR reset	-		440	520	610	μs

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
	release time(2)					
T_{RSTPOR}	Power-on reset release time(2)	-	-	2500	3000	μs

1. Guarantee of mass production test.
2. Guarantee of design.
3. The PVD1 monitoring voltage is the monitoring voltage when the VCC voltage drops; when PVD2LVL[2:0] is set to 0b111, the PVD2 monitoring voltage is the monitoring voltage when the PVDEXINP voltage drops, and when PVD2LVL[2:0] is set to a value other than 0b111, PVD2 The monitor voltage is a monitor voltage when the VCC voltage drops.
4. The hysteresis of PVD1/2 is the difference between the monitoring voltage during rising and falling VCC or PVDEXINP.
   PVD1 monitoring voltage when VCC rises = V_{pvd1}+V_{pvd}hyst.
   PVD2 monitoring voltage when VCC or PVDEXINP rises = V_{pvd2}+V_{pvd}hyst.
5. When PVD2LVL[2:0]=0b111, the comparison voltage is the external input comparison voltage of the PVD2EXINP pin.

3.3.4 Supply Current Characteristics

The current consumption is affected by several parameters and factors, including operating voltage, ambient temperature, I/O pin load, device software configuration, operating frequency, I/O pin switch rate, program position in memory and running code.

The method for measuring the current consumption is described in Figure 3-3. The measured values of current consumption in various modes described in this section are obtained under laboratory conditions through a set of test codes running on FLASH.

The specific conditions are as follows:

1) All I/O pins are in high-impedance mode (no load).
2) Clock frequency selection high-speed mode f_{HCLK}=200MHz/ 100MHz/ 24MHz and ultra-low-speed mode f_{HCLK}=8MHz/ 1MHz.
3) The power consumption mode is divided into: normal working mode ICC_RUN, sleep mode ICC_SLEEP, stop mode ICC_STP, power down mode ICC_PD, Dhrystone working mode ICC_DHRYSTONE.
4) For peripheral clock ON/OFF, please refer to the description of specific current conditions.
5) In high-speed mode f_{HCLK}=200MHz/ 100MHz, the PLL is on.

Table 3-7 High Speed Mode Current Consumption 1

Pattern	Parameter	Symbol	Conditions	T_A(°C)	Product Specifications			Unit
					Minimum Value	Typical value (1)	Max (2)	
High speed mode	f_{HCLK}= 200MHz	ICC_RUN	while(1), all module clock OFF(3)	-40	-	23	-	mA
			while(1), all module clock ON(3)	-40	-	37	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	24	-	mA
			CACHE ON	-40	-	24	-	mA
		ICC_SLEEP	All module clock OFF(3)	-40	-	14	-	mA
			All module clock ON(3)	-40	-	28	-	mA
		ICC_RUN	while(1), all module clock OFF(3)	25	-	23	-	mA
			while(1), all module clock ON(3)	25	-	37	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	24	-	mA
			CACHE ON	25	-	24	-	mA
		ICC_SLEEP	All module clock OFF(3)	25	-	14	-	mA
			All module clock ON(3)	25	-	28	-	mA
		ICC_RUN	While (1), full-module clock OFF	85	-	-	29	mA
			While (1), full module clock ON	85	-	-	43	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	30	mA
			CACHE ON	85	-	-	30	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	20	mA
			Full module clock ON	85	-	-	34	mA
		ICC_RUN	while(1), all module clock OFF(3)	105	-	-	33	mA
			while(1), all module clock ON(3)	105	-	-	48	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	34	mA
			CACHE ON	105	-	-	34	mA
		ICC_SLEEP	All module clock OFF(3)	105	-	-	24	mA
			All module clock ON(3)	105	-	-	39	mA

1. Typical voltage condition V_{CC}=3.3V.
2. Maximum voltage condition V_{CC}=1.8~3.6V.
3. Guarantee of mass production test.

Table 3-8 High Speed Mode Current Consumption 2

Pattern	Parameter	Symbol	Conditions	T_A(°C)	Product Specifications			Unit
					Minimum Value	Typical value (1)	Max (2)	
High speed mode	f_{HCLK}= 100MHz	ICC_RUN	While (1), full-module clock OFF	-40	-	12	-	mA
			While (1), full module clock ON	-40	-	20	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	13	-	mA
			CACHE ON	-40	-	13	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	8	-	mA
			Full module clock ON	-40	-	15	-	mA
		ICC_RUN	While (1), full-module clock OFF	25	-	13	-	mA
			While (1), full module clock ON	25	-	20	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	14	-	mA
			CACHE ON	25	-	14	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	8	-	mA
			Full module clock ON	25	-	16	-	mA
		ICC_RUN	While (1), full-module clock OFF	85	-	-	19	mA
			While (1), full module clock ON	85	-	-	27	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	20	mA
			CACHE ON	85	-	-	20	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	14	mA
			Full module clock ON	85	-	-	22	mA
		ICC_RUN	While (1), full-module clock OFF	105	-	-	23	mA
			While (1), full module clock ON	105	-	-	31	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	24	mA
			CACHE ON	105	-	-	24	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	18	mA
			Full module clock ON	105	-	-	27	mA

1. Typical voltage condition V_{CC}=3.3V.
2. Maximum voltage condition V_{CC}=1.8~3.6V.

Table 3-9 High Speed Mode Current Consumption 3

Pattern	Parameter	Symbol	Conditions	T_A(°C)	Product Specifications			Unit
					Minimum Value	Typical value (1)	Max (2)	
High speed mode	f_{HCLK}= 24MHz	ICC_RUN	While (1), full-module clock OFF	-40	-	4	-	mA
			While (1), full module clock ON	-40	-	8	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	5	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	3	-	mA
			Full module clock ON	-40	-	6	-	mA
		ICC_RUN	While (1), full-module clock OFF	25	-	4	-	mA
			While (1), full module clock ON	25	-	8	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	5	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	3	-	mA
			Full module clock ON	25	-	7	-	mA
		ICC_RUN	While (1), full-module clock OFF	85	-	-	10	mA
			While (1), full module clock ON	85	-	-	14	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	12	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	9	mA
			Full module clock ON	85	-	-	13	mA
		ICC_RUN	While (1), full-module clock OFF	105	-	-	15	mA
			While (1), full module clock ON	105	-	-	19	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	17	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	14	mA
			Full module clock ON	105	-	-	18	mA

1. Typical voltage condition V_{CC}=3.3V.
2. Maximum voltage condition V_{CC}=1.8~3.6V.

Table 3-10 Ultra Low Speed Mode Current Consumption 1

Pattern	Parameter	Symbol	Conditions	T_A(°C)	Product Specifications			Unit
					Minimum Value	Typical value (1)	Max (2)	
Ultra low speed Pattern	f_{HCLK}= 8MHz	ICC_RUN	While (1), full-module clock OFF(3)	-40	-	2	-	mA
			While (1), full module clock ON(3)	-40	-	4	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	2.2	-	mA
		ICC_SLEEP	Full module clock OFF(3)	-40	-	1	-	mA
			Full module clock ON(3)	-40	-	3	-	mA
		ICC_RUN	While (1), full-module clock OFF(3)	25	-	2	-	mA
			While (1), full module clock ON(3)	25	-	4	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	2.3	-	mA
		ICC_SLEEP	Full module clock OFF(3)	25	-	1	-	mA
			Full module clock ON(3)	25	-	3	-	mA
		ICC_RUN	While (1), full-module clock OFF	85	-	-	5	mA
			While (1), full module clock ON	85	-	-	7	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	5.5	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	4.6	mA
			Full module clock ON	85	-	-	6.7	mA
		ICC_RUN	While (1), full-module clock OFF(3)	105	-	-	8	mA
			While (1), full module clock ON(3)	105	-	-	10	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	9	mA
		ICC_SLEEP	Full module clock OFF(3)	105	-	-	7.5	mA
			Full module clock ON(3)	105	-	-	9.5	mA

1. Typical voltage condition V_{CC}=3.3V.
2. Maximum voltage condition V_{CC}=1.8~3.6V.
3. Guarantee of mass production test.

Table 3-11 Ultra Low Speed Mode Current Consumption 2

Pattern	Parameter	Symbol	Conditions	T_A(°C)	Product Specifications			Unit
					Minimum Value	Typical value (1)	Max (2)	
Super low speed mode	f_{HCLK}= 1MHz	ICC_RUN	While (1), full-module clock OFF	-40	-	1	-	mA
			While (1), full module clock ON	-40	-	2.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	1	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	0.5	-	mA
			Full module clock ON	-40	-	2	-	mA
		ICC_RUN	While (1), full-module clock OFF	25	-	1	-	mA
			While (1), full module clock ON	25	-	2.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	1	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	0.7	-	mA
			Full module clock ON	25	-	2.2	-	mA
		ICC_RUN	While (1), full-module clock OFF	85	-	-	4.5	mA
			While (1), full module clock ON	85	-	-	6	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	4.7	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	4.3	mA
			Full module clock ON	85	-	-	5.9	mA
		ICC_RUN	While (1), full-module clock OFF	105	-	-	7.5	mA
			While (1), full module clock ON	105	-	-	9	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	8	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	7	mA
			Full module clock ON	105	-	-	8.8	mA

1. Typical voltage condition V_{CC}=3.3V.
2. Maximum voltage condition V_{CC}=1.8~3.6V.

Table 3-12 Low Power Mode Current Consumption

Pattern	Parameter	Symbol	Conditions	T_A(°C)	Product Specifications			Unit
					Minimum Value	Typical value (1)	Max (2)	
Stop mode	-	ICC_STP	PWC_PWRC1.STPDAS=00(3)	-40	-	188	-	μA
			PWC_PWRC1.STPDAS=11(3)	-40	-	45	-	μA
			PWC_PWRC1.STPDAS=00(3)	25	-	455	-	μA
			PWC_PWRC1.STPDAS=11(3)	25	-	304	-	μA
			PWC_PWRC1.STPDAS=00	85	-	-	3.9	mA
			PWC_PWRC1.STPDAS=11	85	-	-	3.6	mA
			PWC_PWRC1.STPDAS=00(3)	105	-	-	6.5	mA
			PWC_PWRC1.STPDAS=11(3)	105	-	-	6.2	mA
Power Down Mode	-	ICC_PD	Power Down Mode 1(3)	-40	-	10	-	μA
			Power Down Mode 2(3)	-40	-	4	-	μA
			Power Down Mode 3(3)	-40	-	1.7	-	μA
			Power Down Mode 4(3)	-40	-	1.7	-	μA
			Power-down mode 2+ XTAL32+ RTC	-40	-	6	-	μA
			Power-down mode 2+ LRC+ RTC	-40	-	9	-	μA
			Power Down Mode 1(3)	25	-	11	-	μA
			Power Down Mode 2(3)	25	-	4.5	-	μA
			Power Down Mode 3(3)	25	-	2.1	-	μA
			Power Down Mode 4(3)	25	-	2.1	-	μA
			Power-down mode 2+ XTAL32+ RTC	25	-	7	-	μA
			Power-down mode 2+ LRC+ RTC	25	-	9	-	μA
			Power down mode 1	85	-	-	20	μA
			Power down mode 2	85	-	-	18	μA
			Power down mode 3	85	-	-	11	μA
			Power down mode 4	85	-	-	11	μA
			Power-down mode 2+ XTAL32+ RTC	85	-	-	20	μA
			Power down mode 2+ LRC+ RTC	85	-	-	20	μA
			Power Down Mode 1(3)	105	-	-	31	μA
			Power Down Mode 2(3)	105	-	-	29	μA
			Power Down Mode 3(3)	105	-	-	21	μA
			Power Down Mode 4(3)	105	-	-	21	μA
			Power-down mode 2+ XTAL32+ RTC	105	-	-	31	μA

Pattern	Parameter	Symbol	Conditions	T_A(°C)	Product Specifications			Unit
					Minimum Value	Typical value (1)	Max (2)	
			Power-down mode 2+ LRC+ RTC	105	-	-	31	μA

1. Typical voltage condition V_{CC}=3.3V.
2. Maximum voltage condition V_{CC}=1.8~3.6V.
3. Guarantee of mass production test.

Table 3-13 Analog Module Current Consumption

Item	Parameter	Symbol	Conditions (VCC=AVCC=3.3V)		T_A(°C)	Product Specifications			Unit
						Minimum Value	Typical Value	Maximum Value	
Module current	-	ICC_MODULE	XTAL Oscillation Mode high Drive 24MHz		25	-	1.8	-	mA
			Drive 16 MHz in Oscillation Mode		25	-	1.0	-	mA
			Oscillating mode low drive 10 MHz		25	-	0.8	-	mA
			Oscillating mode ultra-low drive 8 MHz		25	-	0.6	-	mA
			XTAL 32.768KHz		25	-	1.1	-	μA
			HRC		25	-	0.3	-	mA
			PLLH (VCO=1200MHz)		25	-	3.5	-	mA
			PLLH (VCO=600MHz)		25	-	1.8	-	mA
			ADC		25	-	1.3	-	mA
			DAC	Amplifier allows	25	-	0.8	-	mA
				Amplifier prohibited	25	-	0.2	-	mA
			CMP		25	-	0.3	-	mA

3.3.5 Low Power Mode Wake-Up Timing

The wake-up time is measured from the wake-up event trigger to the first instruction executed by the CPU:

- For stop or sleep mode: Wakeup event is WFE.
- WKUP pins are used to wake up from standby, stop, and sleep modes. All the timings are measured at ambient temperature and V_{CC}=3.3V.

Table 3-14 Low power mode wake-up time

Symbol	Parameter	Conditions	Typical Value	Maximum Value	Unit
T_{STOP}	Wakeup from stop mode	System clock is MRC	8	15	μs
T_{PD1}(1)	Wake up from power-down mode 1	The total capacitance of VCAP_1 is 0.094μF or 0.1μF	25	35	
		The total capacitance of VCAP_1 is 0.2μF or 0.22μF	30	40	
T_{PD2}(1)	Wake up from power-down mode 2	The total capacitance of VCAP_1 is 0.094μF or 0.1μF	70	80	
		The total capacitance of VCAP_1 is 0.2μF or 0.22μF	75	85	
T_{PD3}(1)	Wake up from power-down mode 3	The total capacitance of VCAP_1 is 0.094μF or 0.1μF	2500	3000	
		The total capacitance of VCAP_1 is 0.2μF or 0.22μF	2500	3000	
T_{PD4}(1)	Wake up from power-down mode 4	The total capacitance of VCAP_1 is 0.094μF or 0.1μF	130	140	
		The total capacitance of VCAP_1 is 0.2μF or 0.22μF	140	150	

1. The total VCAP_1 capacity of the chip must match the assignment of the PWC_PWRC1.PDTS bits. When the total capacity of VCAP_1 is 0.2μF or 0.22μF, it is necessary to ensure that the PWC_PWRC1.PDTS bit is cleared before entering power-down mode. When the total capacity of VCAP_1 is 0.094μF or 0.1μF, it is necessary to ensure that the PWC_PWRC1.PDTS bit is set before entering power-down mode.

3.3.6 External Timer Characteristic

3.3.6.1 High-speed External Subscriber Clock Generated By External Source

In bypass mode, the XTAL oscillator is turned off and the input pins are standard I/Os. The external clock signal must consider the requirements for external input clock characteristics in Table 3-15.

Table 3-15 High-Speed External User Clock Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
f_{XTAL_EXT}	User external timer frequency	-	1	-	25(1)	MHz
V_{IH_XTAL}	XTAL_EXT input pin high level voltage		$0.8\times V_{CC}$	-	V_{CC}	V
V_{IL_XTAL}	XTAL_EXT input pin low level voltage		V_{SS}	-	$0.2\times V_{CC}$	
$t_{r(XTAL)}$ $t_{f(XTAL)}$	XTAL_EXT rise or fall time		-	-	5	ns
$Duty_{(XTAL)}$	Duty ratio	-	40	-	60	%

1. Guarantee of mass production test.

3.3.6.2 High-Speed External Clock from Crystal/Ceramic Resonator

The high-speed external (XTAL) clock can be generated using a 4 to 25MHz crystal/ceramic resonator. In applications, the resonator and load capacitance must be as close to the oscillator pin as possible to minimize output distortion and vibration stabilization time. For more information on the resonator characteristics (frequency, encapsulation, accuracy, etc.), please consult the crystal resonator manufacturer.

Table 3-16 XTAL 4-25MHz Oscillator Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
f_{XTAL_IN}	Oscillator frequency	-	4	-	25	MHz
R_F	Feedback resistance(1)	-	-	300	-	KΩ
A_{XTAL}	XTAL accuracy(2)(3)	-	-500	-	500	ppm
G_{mmax}	Oscillator Gm(2)	Wake up	4	-	-	mA/V
$t_{SU(XTAL)}$	Start time(4)	VCC is stable, crystal oscillator=8MHz	-	2.0	-	ms
		VCC is stable, crystal oscillator=4MHz	-	4.0	-	ms

1. Guarantee of mass production test.
2. Guarantee of design.
3. This parameter depends on the resonator used in the application system.
4. $t_{SU(XTAL)}$ is the start-up time, that is, the time from when XTAL is enabled by software until a stable oscillation frequency is obtained. This value is measured based on the standard crystal resonator and may vary significantly with the crystal resonator manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors designed for high-frequency applications to meet the crystal or resonator requirements (see figure below). C_{L1} and C_{L2} are usually the same size, $C_{L1}=C_{L2}=2*(C_L-Cs)$. Cs is the total parasitic capacitance between the PCB and MCU pins (XTAL_IN, XTAL_OUT). C_L is a load capacitor for crystal or ceramic resonators, please consult the crystal resonator manufacturer.

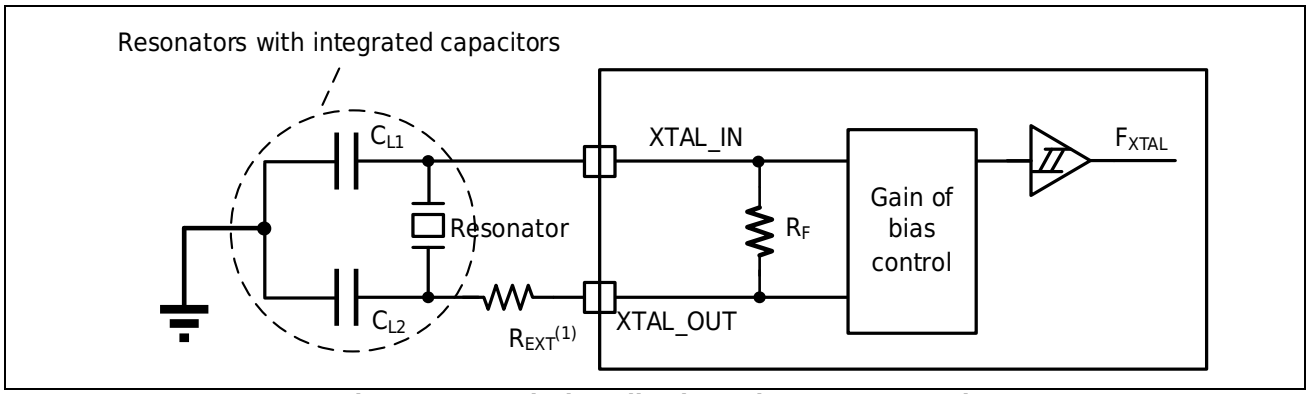


Figure 3-4 Typical Application Using 8 MHz Crystal

1. The value of R_{EXT} depends on the crystal oscillator characteristics.

3.3.6.3 Low-speed external clock generated by crystal oscillator/ceramic resonator

Low-speed external clocks can be produced using a oscillator composed of 32.768 KHz crystal oscillator/ceramic resonator. In applications, the resonator and load capacitance must be as close to the oscillator pin as possible to minimize output distortion and vibration stabilization time. For more information on the resonator characteristics (frequency, encapsulation, accuracy, etc.), please consult the crystal resonator manufacturer.

Table 3-17 XTAL32 Oscillator Features

Symbol	Parameter	Conditions	Specifications			Unit
			Minimum Value	Typical Value	Maximum Value	
F_{XTAL32}	Frequency	-	-	32.768	-	KHz
R_F	Feedback resistance(1)	-	-	15	-	MΩ
I_{DD_XTAL32}	Power consumption	XTAL32DRV[2:0]=0b000	-	0.8	-	μA
A_{XTAL32}(2)	XTAL32 precision(3)	-	-500	-	500	ppm
G_{mmax}	Oscillator Gm(2)	XTAL32DRV[2:0]=0b000	5.6	-	-	μA/V
$T_{SUXTAL32}$	Start time(4)	VCC Stabilization	-	2	-	s

1. Mass production test guarantee.
2. Guarantee of design.
3. This parameter depends on the resonator used in the application system.
4. $T_{SUXTAL32}$ is the start-up time, which starts with the software enabling XTAL 32 to measure until a stable oscillation frequency of 32.768 KHz is obtained. This value is measured based on the standard crystal resonator and may vary significantly with the crystal resonator manufacturer.

For C_{L1} and C_{L2}, high quality external ceramic capacitors are recommended (see figure below). C_{L1} and C_{L2} are usually the same size, C_{L1}=C_{L2}=2*(C_L-Cs). Cs is the total parasitic capacitance between the PCB and MCU pins (XTAL32_IN, XTAL32_OUT). If C_{L1} or C_{L2} is greater than 18 pF, it is recommended to set XTAL32DRV[2:0]=0b001 (high drive, typical power consumption increased by 0.2 μA). C_L is a load capacitor for crystal or ceramic resonators, please consult the crystal resonator manufacturer.

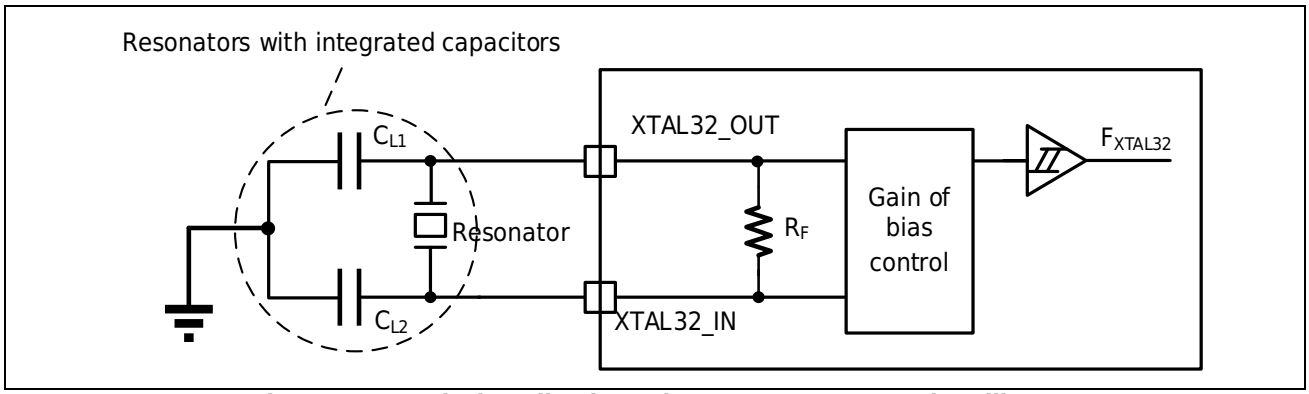


Figure 3-5 Typical application using 32.768 KHz crystal oscillator

3.3.7 Internal Timer Characteristics

3.3.7.1 Internal High Speed (HRC) Oscillator

Table 3-18 HRC Oscillator Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
f_{HRC}	Frequency(1)	Pattern 1	-	16	-	MHz
		Pattern 2	-	20	-	
	User Adjustment Scale	-	-	-	0.2	%
	Frequency Accuracy	T_A=-40 to 105℃(1)	-2	-	2	%
		T_A=-20 to 105℃	-1.5	-	1.5	%
$t_{st(HRC)}$	HRC oscillator oscillation stabilization time(1)	-	-	-	15	μs

1. Guarantee of mass production test.

3.3.7.2 Internal Medium Speed (MRC) Oscillator

Table 3-19 MRC Oscillator Characteristics

Symbol	Parameter	Minimum Value	Typical Value	Maximum Value	Unit
f_{MRC}	Frequency(1)	7.2	8	8.8	MHz
$t_{st(MRC)}$	MRC Oscillator Settling Time(1)	-	-	3	μs

1. Guarantee of mass production test.

3.3.7.3 Internal Low Speed (LRC) Oscillator

Table 3-20 LRC Oscillator Characteristics

Symbol	Parameter	Minimum Value	Typical Value	Maximum Value	Unit
f_{LRC}	Frequency(1)	27.853	32.768	37.683	KHz
$t_{st(LRC)}$	LRC Oscillator Settling Time(1)	-	-	36	μs

1. Guarantee of mass production test.

3.3.7.4 SWDT Dedicated Internal Low-Speed (SWDTLRC) Oscillator

Table 3-21 SWDTLRC Oscillator Characteristics

Symbol	Parameter	Minimum Value	Typical Value	Maximum Value	Unit
$f_{SWDTLRC}$	Frequency(1)	9	10	11	KHz
$t_{st(SWDTLRC)}$	SWDTLRC oscillator stabilization time(1)	-	-	57.1	μs

1. Guarantee of mass production test.

3.3.8 PLL Characteristic

Table 3-22 PLLH Main Performance Indicators

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
f_{PLL_IN}	Input clock for PLL phase frequency detector (PFD)(1)(2)	-	4	-	25	MHz
f_{PLL_OUT}	The output clock of the PLL multiplier	-	37.5	-	600	MHz
f_{VCO_OUT}	The output of the PLL voltage-controlled oscillator (VCO)(1)	-	600	-	1200	MHz
$Jitter_{PLL}$	Period jitter	PLL PFD input clock is 8MHz, system clock is 120MHz, peak-to-peak	-	±70	-	ps
	Jitter between adjacent cycles	PLL PFD input clock is 8MHz, system clock is 120MHz, peak-to-peak	-	±100	-	
t_{LOCK}	PLL lock time	-	-	80	120	μs

1. Guarantee of mass production test.
2. A higher input clock is recommended for good jitter characteristics.

3.3.9 Memory (Flash) Characteristics

Flash memory was erased when the device was delivered to the customer.

Table 3-23 Flash Features

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
I_{VCC}	Supply current(1)	Read mode, V_{CC}=1.8V~3.6V	-	-	5	mA
		Programming mode, V_{CC}=1.8V~3.6V	-	-	10	
		Block erase mode, V_{CC}=1.8V~3.6V	-	-	10	
		Full erase mode, V_{CC}=1.8V~3.6V	-	-	10	

1. Guarantee of design.

Table 3-24 Flash Program Erase Time

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
T_{prog}	Word programming time(1)	Single programming mode	$43+2\times T_{hclk}$(2)	$48+4\times T_{hclk}$(2)	$53+6\times T_{hclk}$(2)	μs
	Word programming time(1)	Continuous programming mode	$12+2\times T_{hclk}$(2)	$14+4\times T_{hclk}$(2)	$16+6\times T_{hclk}$(2)	μs
T_{erase}	Block erase time(1)	-	$16+2\times T_{hclk}$(2)	$18+4\times T_{hclk}$(2)	$20+6\times T_{hclk}$(2)	ms
T_{mas}	Full erase time(1)	-	$16+2\times T_{hclk}$(2)	$18+4\times T_{hclk}$(2)	$20+6\times T_{hclk}$(2)	ms

1. Guarantee of mass production test.
2. T_{hclk} is one cycle of CPU clock.

Table 3-25 Flash Memory Erasability and Data Retention Period

Symbol	Parameter	Conditions	Numerical Value	Unit
			Minimum Value	
N_{end}	Programming, number of block erases	T_A=85℃	10	Thousands of times
N_{end}	Number of whole erases	T_A=85℃	10	Thousands of times
T_{ret}	Data retention period	T_A=85℃, after 10 kcycles	10	Year

3.3.10 Electrical Sensitivity

The chip is tested differently (ESD, LU) using specific measurement methods to determine its performance in terms of electrical susceptibility.

3.3.10.1 Electrostatic Discharge (ESD)

Electrostatic discharge is applied to the pins of each sample according to each pin combination. This test complies with the ANSI/ESDA/JEDEC JS-001, ANSI/ESDA/JEDEC JS-002 standard.

Table 3-26 ESD Characteristics

Symbol	Parameter	Conditions	Maximum Value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A=+25°C, complies with ANSI/ESDA/JEDEC JS-001 standard	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging equipment model)	T_A=+25°C, complies with ANSI/ESDA/JEDEC JS-002 standard	1000	

3.3.10.2 Static Latch-up

To assess static Latch-up performance, two complementary static Latch-up tests are required on the chip:

- Over-voltage applied to each power supply and analog input pin
- Apply current injection to other input, output, and configurable I/O pins

These tests comply with the EIA/JESD 78A IC Latch-up standard.

Table 3-27 Static Latch-up Features

Symbol	Parameter	Conditions	Maximum Value	Unit
LU	Static Latch-up	T_A=+105°C, complies with JESD78A standard	200	mA

3.3.11 I/O Port Characteristics

General input/ output characteristics

Table 3-28 I/O Static Characteristics

Symbol	Parameter		Conditions	Minimum Value	Typical Value	Max.	Unit
V_{IL}	Schmitt input low level(1)		1.8≤V_{CC}≤3.6	-	-	0.3V_{CC}	V
V_{IH}	Schmitt input high level(1)		1.8≤V_{CC}≤3.6	0.7V_{CC}	-	-	V
V_{HYS}	Schmitt input hysteresis		1.8≤V_{CC}≤3.6	0.1	0.2	-	V
V_{IL}	CMOS Input Low Level(1)		1.8≤V_{CC}≤3.6	-	-	0.3V_{CC}	V
V_{IH}	CMOS input high level(1)		1.8≤V_{CC}≤3.6	0.7V_{CC}	-	-	V
TTL_V_{IL}	CMOS/Schmitt compatible TTL Input low level(1)		2.7≤V_{CC}≤3.6	-	-	0.8	V
TTL_V_{IH}	CMOS/Schmitt compatible TTL Input high level(1)		2.7≤V_{CC}≤3.6	2.2	-	-	V
$F_{max(in)}$	Schmitt input maximum frequency		2.7≤V_{CC}≤3.6	-	-	40	MHz
			1.8≤V_{CC}≤2.7	-	-	20	MHz
	CMOS input maximum frequency		2.7≤V_{CC}≤3.6	-	-	80	MHz
			1.8≤V_{CC}≤2.7	-	-	40	MHz
I_{LKG}	I/O input leakage current(1)		V_{SS}≤V_{IN}≤V_{CC}	-	-	1	μA
			V_{IN}=5.5V(2)	-	-	10	μA
R_{PU}	Weak pull-up Equivalent resistance(1)(3)		V_{IN}=V_{SS} 1.8≤V_{CC}≤3.6	10	30	150	KΩ
R_{PD}	Weak pull-down Equivalent resistance(1)(3)		V_{IN}=V_{cc} 1.8≤V_{CC}≤3.6	5	20	50	KΩ
C_{IO}	I/O pin capacitance(2)	PB11/MD	-	-	10	-	pF
		Input pins other than the above	-	-	5	-	pF

1. Guarantee of mass production test.
2. Guarantee of design.
3. To keep the voltage above V_{CC}+0.3V, the internal pull-up/ pull-down resistors must be disabled.

Output current

GPIO (General Purpose Input/ Output) can source or sink current up to ±20mA.

The output voltage

Table 3-29 Output Voltage Characteristics

Driver Settings	Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Low drive	V_{OL}	Low level output(1)(2)	I_{IO}=±1.5mA, 1.8≤V_{CC}<2.7	-	-	0.6	V
	V_{OH}	High level output(1)(3)		V_{CC}-0.6	-	-	
	V_{OL}	Low level output(1)(2)	I_{IO}=±3mA, 2.7≤V_{CC}≤3.6	-	-	0.6	
	V_{OH}	High level output(1)(3)		V_{CC}-0.6	-	-	
	V_{OL}	Low level output(1)(2)	I_{IO}=±6mA, 2.7≤V_{CC}≤3.6	-	-	1.3	
	V_{OH}	High level output(1)(3)		V_{CC}-1.3	-	-	
medium drive	V_{OL}	Low level output(1)(2)	I_{IO}=±3mA, 1.8≤V_{CC}<2.7	-	-	0.4	
	V_{OH}	High level output(1)(3)		V_{CC}-0.4	-	-	
	V_{OL}	Low level output(1)(2)	I_{IO}=±5mA, 2.7≤V_{CC}≤3.6	-	-	0.4	
	V_{OH}	High level output(1)(3)		V_{CC}-0.4	-	-	
	V_{OL}	Low level output(1)(2)	I_{IO}=±12mA, 2.7≤V_{CC}≤3.6	-	-	1.3	
	V_{OH}	High level output(1)(3)		V_{CC}-1.3	-	-	
High drive	V_{OL}	Low level output(1)(2)	I_{IO}=±6mA, 1.8≤V_{CC}<2.7	-	-	0.4	
	V_{OH}	High level output(1)(3)		V_{CC}-0.4	-	-	
	V_{OL}	Low level output(1)(2)	I_{IO}=±8mA, 2.7≤V_{CC}≤3.6	-	-	0.4	
	V_{OH}	High level output(1)(3)		V_{CC}-0.4	-	-	
	V_{OL}	Low level output(1)(2)	I_{IO}=±20mA, 2.7 ≤V_{CC}≤3.6	-	-	1.3	
	V_{OH}	High level output(1)(3)		V_{CC}-1.3	-	-	
	V_{OL}	Low level output(1)(2)	I_{IO}=±20mA, 3.0 ≤V_{CC}≤3.6	-	-	0.88	
	V_{OH}	High level output(1)(3)		V_{CC}-0.88	-	-	

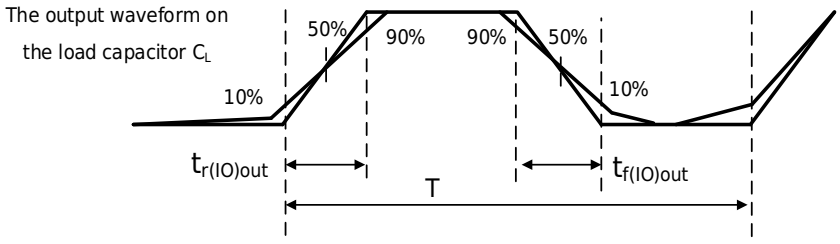
1. Guarantee of mass production test.
2. The I_{IO} sink current of the device must always take into account the absolute maximum ratings specified in Table 3-2. The sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
3. The device's I_{IO} source current must always adhere to the absolute maximum ratings listed in Table 3-2, and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VCC}.

Input/ output AC Characteristics

Table 3-30 I/O AC Characteristics

Driver Settings	Symbol	Parameter	Condition(3)	Minimum Value	Typical Value	Maximum Value	Unit
Low drive	f_{max}(IO)out	Maximum frequency(1)	C_L=30pF, V_{CC}≥2.7V	-	-	20	MHz
			C_L=30pF, V_{CC}≥1.8V	-	-	10	
			C_L=10pF, V_{CC}≥2.7V	-	-	40	
			C_L=10pF, V_{CC}≥1.8V	-	-	20	
	t_f(IO)out t_r(IO)out	Output high to low level drop time and output low to high level rise time	C_L=30pF, V_{CC}≥2.7V	-	-	15	ns
			C_L=30pF, V_{CC}≥1.8V	-	-	25	
			C_L=10pF, V_{CC}≥2.7V	-	-	7.5	
			C_L=10pF, V_{CC}≥1.8V	-	-	15	
medium drive	f_{max}(IO)out	Maximum frequency(1)	C_L=30pF, V_{CC}≥2.7V	-	-	45	MHz
			C_L=30pF, V_{CC}≥1.8V	-	-	22.5	
			C_L=10pF, V_{CC}≥2.7V	-	-	90	
			C_L=10pF, V_{CC}≥1.8V	-	-	45	
	t_f(IO)out t_r(IO)out	Output high to low level drop time and output low to high level rise time	C_L=30pF, V_{CC}≥2.7V	-	-	6	ns
			C_L=30pF, V_{CC}≥1.8V	-	-	10	
			C_L=10pF, V_{CC}≥2.7V	-	-	4	
			C_L=10pF, V_{CC}≥1.8V	-	-	6	
High drive	f_{max}(IO)out	Maximum frequency(1)	C_L=30pF, V_{CC}≥2.7V	-	-	100	MHz
			C_L=30pF, V_{CC}≥1.8V	-	-	50	
			C_L=10pF, V_{CC}≥1.8V	-	-	100	
	t_f(IO)out t_r(IO)out	Output high to low level drop time and output low to high level rise time	C_L=30pF, V_{CC}≥2.7V	-	-	4	ns
			C_L=30pF, V_{CC}≥1.8V	-	-	6	
			C_L=10pF, V_{CC}≥2.7V	-	-	2.5	
			C_L=10pF, V_{CC}≥1.8V	-	-	3.5	

1. The maximum frequency is defined in Figure 3-6.
2. The load capacitance C_L must take into account the capacitance of the PCB and MCU pins (the capacitance between the MD pin PB11 and the circuit board can be roughly estimated as 15pF; the capacitance between other pins and the circuit board can be roughly estimated as 10pF).



Maximum frequency condition: (t_r + t_f) ≤ (2/3)T and Duty cycle= 50%±5% (the load capacitance C_L is indicated in the "Condition" column of the "Input/Output AC Characteristics" table)

Figure 3-6 Definition of I/O AC Characteristics

3.3.12 I2C Interface Characteristics

Table 3-31 I2C Electrical Characteristics

Symbol	Parameter	Standard Mode (SM)		Fast Mode (FM)		Unit
		Minimum Value	Maximum Value	Minimum Value	Maximum Value	
f_{SCL}	SCL frequency	0	100	0	400	KHz
$t_{HD;STA}$	Start condition/restart condition Hold	4.0	-	0.6	-	μs
t_{LOW}	SCL Low Level	4.7	-	1.3	-	μs
t_{HIGH}	SCL High Level	4	-	0.6	-	μs
$t_{SU;STA}$	Restarting Condition Setup	4.7	-	0.6	-	μs
$t_{HD;DAT}$	Data Hold(1)	0	-	0	-	μs
$t_{SU;DAT}$	Data Setup(1)	30+ $t_{I2Creference\ clock\ period}$(2)	-	30+ $t_{I2Creference\ clock\ period}$(2)	-	ns
t_R	Ascending time of SCL/ SDA	-	1000	-	300	ns
t_F	Falling time of SCL/ SDA	-	300	-	300	ns
$t_{SU;STO}$	Stop Condition Setup	4	-	0.6	-	μs
t_{BUF}	BUS Idle Time Between Stop Condition and Start Condition	4.7	-	1.3	-	μs
C_b	Load capacitance	-	400	-	400	pF

1. Guarantee of mass production test.
2. $t_{I2Creference\ clock\ period}$ is the I2C reference clock cycle, set by the I2C_CCR.FREQ[2:0] bits.

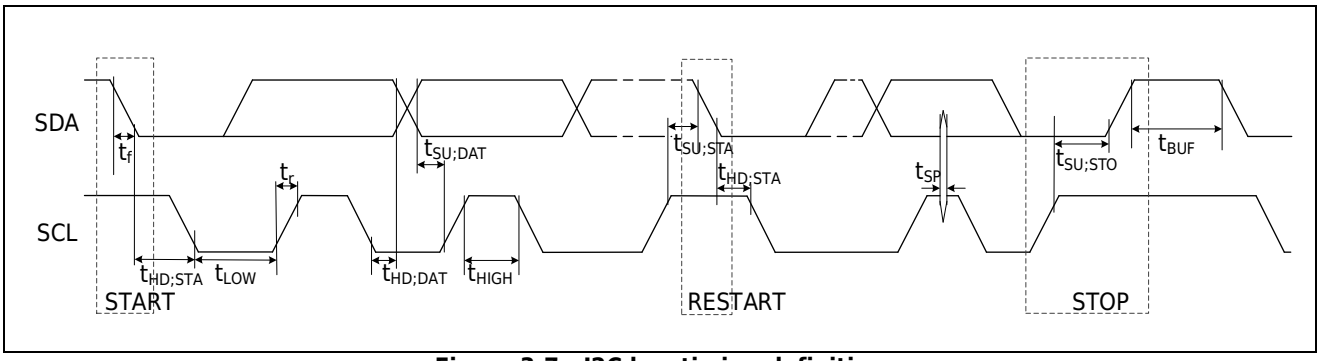


Figure 3-7 I2C bus timing definition

3.3.13 SPI Interface Characteristics

Table 3-32 SPI Electrical Characteristics

Symbol	Parameter	Conditions	Minimum Value	Max.	Unit
t_w(SCKH)	SCK high level time	Host mode(4), 1.8V≤Vcc≤3.6V	T_{pclk1}-1(5)	T_{pclk1}+1(5)	ns
		Slave mode(4), 1.8V≤Vcc≤3.6V	3xT_{pclk1}-1(5)	3×T_{pclk1}+1(5)	ns
t_w(SCKL)	SCK low level time	Host mode(4), 1.8V≤Vcc＜3.6V	T_{pclk1}-1(5)	T_{pclk1}+1(5)	ns
		Slave mode(4), 1.8V≤Vcc＜3.6V	3×T_{pclk1}-1(5)	3×T_{pclk1}+1(5)	ns
t_{su}(SI)	Data input setup time	Slave mode, 1.8V≤Vcc≤3.6V(1)	4	-	ns
t_h(SI)	Data input hold time	Slave mode, 1.8V≤Vcc≤3.6V(1)	3	-	ns
t_v(SO)	Data output effective time	Slave mode, 2.7V≤Vcc≤3.6V(1)	-	15	ns
		Slave mode, 1.8V≤Vcc＜2.7V(1)	-	26	ns
t_{su}(MI)	Data input setup time	Host mode, 2.7V≤Vcc≤3.6V(1)	5	-	ns
		Host mode, 1.8V≤Vcc＜2.7V(1)	9	-	ns
t_h(MI)	Data input hold time	Host mode, 2.7V≤Vcc≤3.6V(1)	5	-	ns
		Host mode, 1.8V≤Vcc＜2.7V(1)	15	-	ns
t_{su}(SS)	SS establishment time	Slave mode, 1.8V≤Vcc≤3.6V	6×T_{pclk1} (5)	-	ns
		Host mode, 2.7V≤Vcc≤3.6V	-5+N×T_{sck} (2)(5)	-	ns
		Host mode, 1.8V≤Vcc＜2.7V	-10+N×T_{sck} (2)(5)	-	ns
t_h(SS)	SS hold time	Slave mode, 1.8V≤Vcc≤3.6V	6×T_{pclk1} (5)	-	ns
		Host mode, 2.7V≤Vcc≤3.6V	-5+N×T_{sck} (3)(5)	-	ns
		Host mode, 1.8V≤Vcc＜2.7V	-10+N×T_{sck} (3)(5)	-	ns
t_v(MO)	Data output effective time	Host mode, 2.7V≤Vcc≤3.6V(1)	-	4	ns
		Host mode, 1.8V≤Vcc≤2.7V(1)	-	9	ns

1. Guarantee of mass production test.
2. N=1~8, determined by register SPI_CFG1.MSSI[2:0].
3. N=1~8, determined by register SPI_CFG1.MSSDL[2:0].
4. The values of t_w(SCKH) and t_w(SCKL) are determined by SPI_CFG2.MBR, and the values listed in the table are the values of SPI_CFG2.MBR=0.
5. T_{pclk1} refers to one cycle of the clock PCLK1, and T_{sck} refers to one cycle of the SPI communication clock.

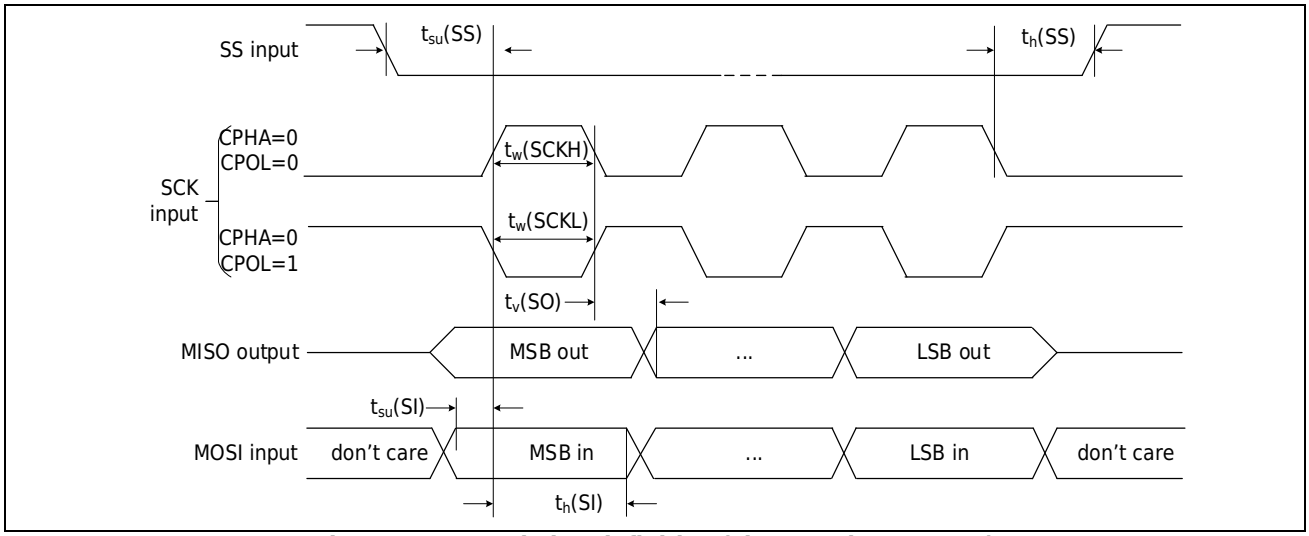


Figure 3-8 SPI timing definition (slave mode, CPHA=0)

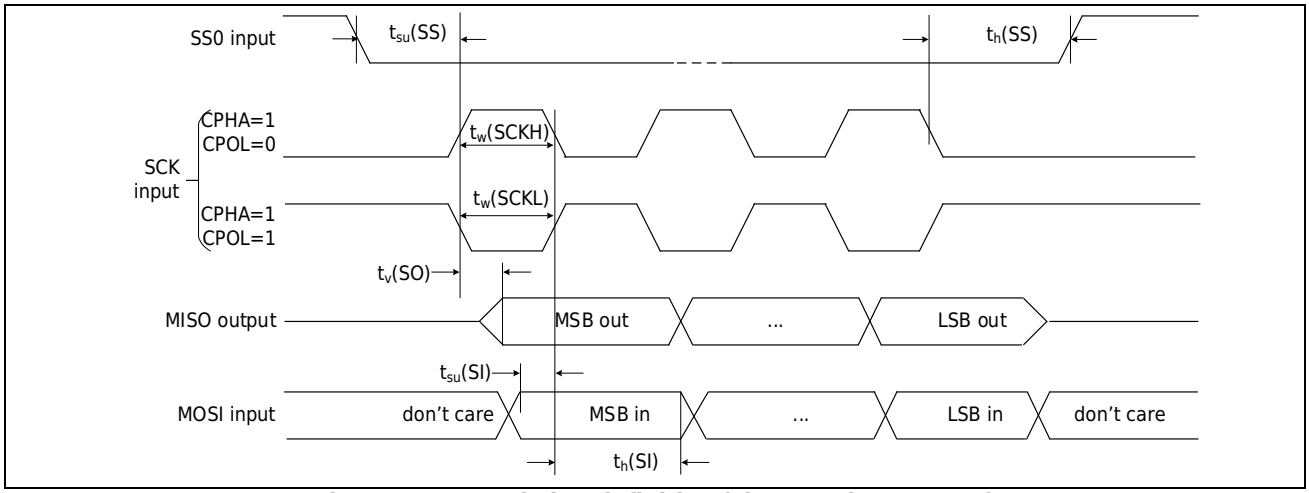


Figure 3-9 SPI timing definition (slave mode, CPHA=1)

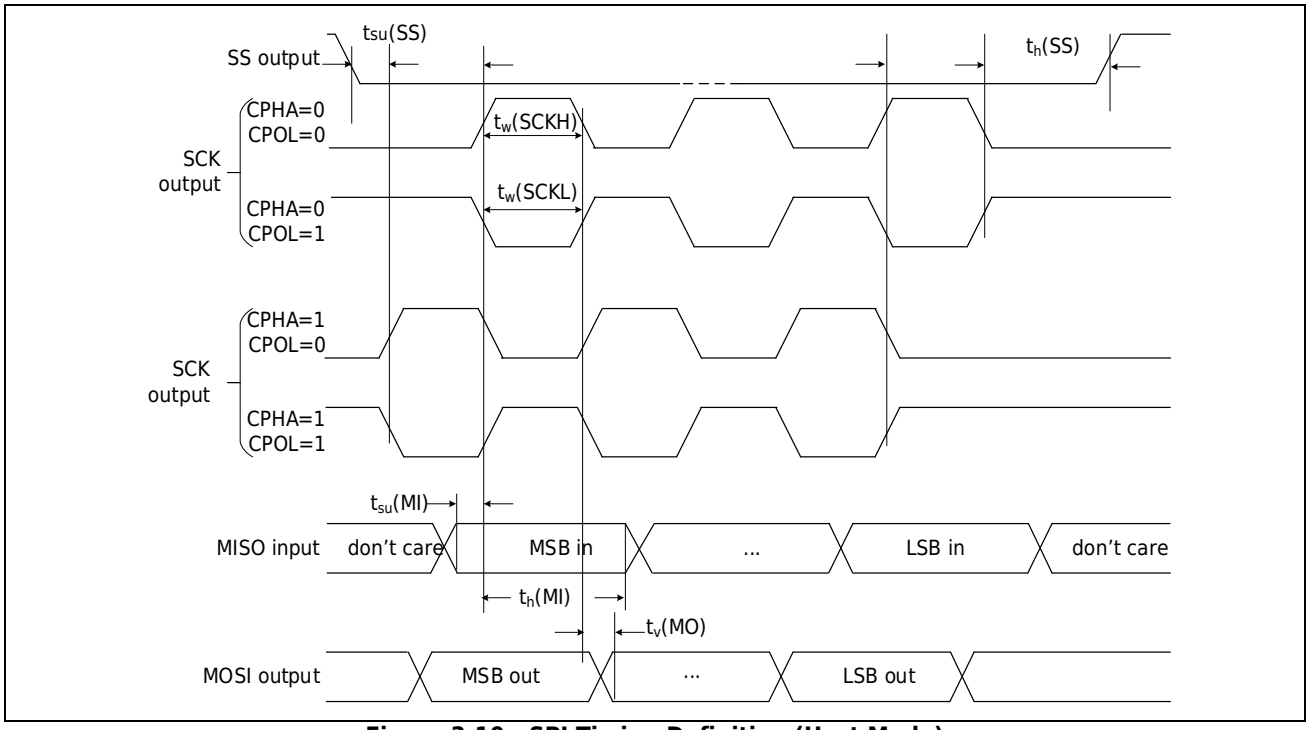


Figure 3-10 SPI Timing Definition (Host Mode)

3.3.14 QSPI Interface Characteristics

Table 3-33 QSPI Electrical Characteristics

Symbol	Parameter	Minimum Value	Max.	Unit
t_{Qscyc}	SCK clock cycles	2	48	t_{hclk}
t_{QSWH}	SCK High Level	t_{Qscyc}×0.4	-	ns
t_{QSWL}	SCK Low Level	t_{Qscyc}×0.4	-	ns
t_{SU}	Data input setup time (1.8V~3.6V)(1)	5	-	ns
t_{IH}	Data input hold time (2.7V~3.6V)(1)	5	-	ns
	Data input hold time (1.8V~2.7V)(1)	15	-	ns
t_{OD}	Data output delay(1)	-	4	ns
t_{OH}	Data output hold time	0	-	ns

1. Guarantee of mass production test.

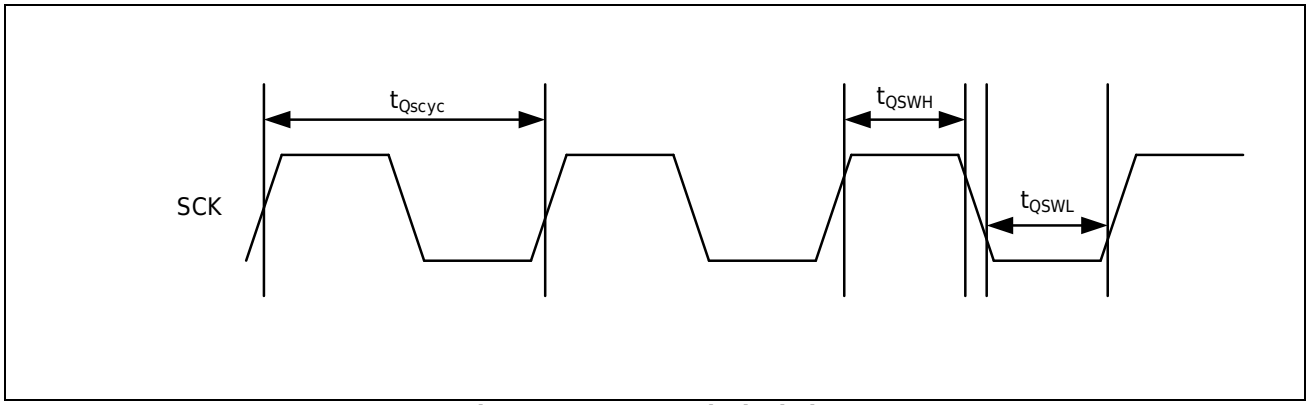


Figure 3-11 QSPI Clock Timing

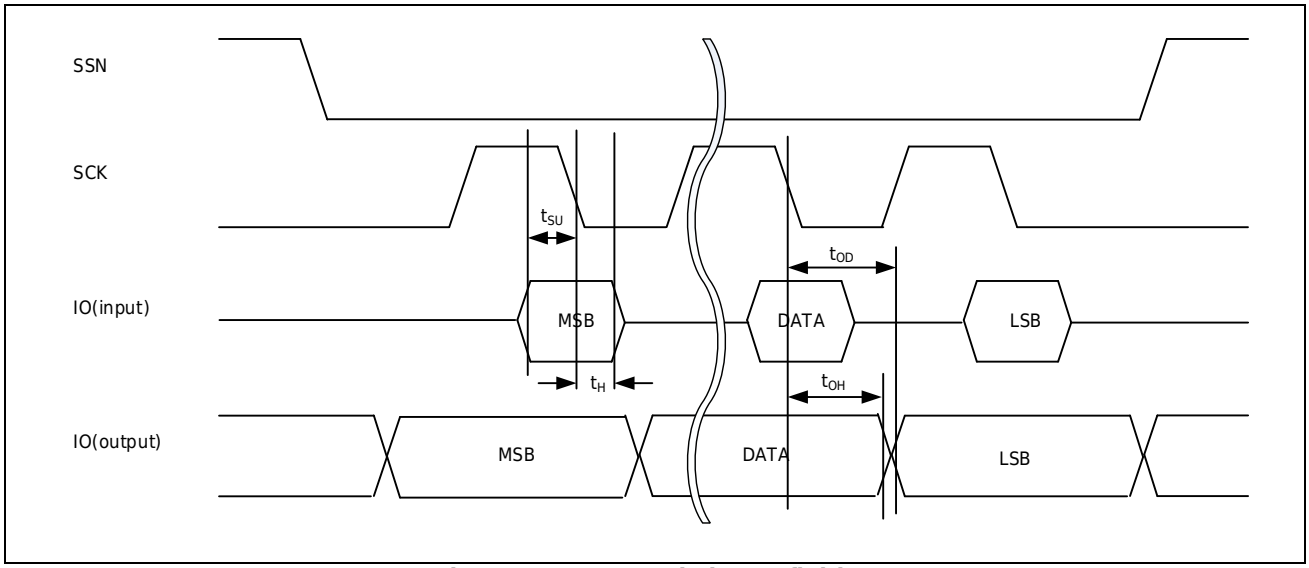


Figure 3-12 QSPI Timing Definition

3.3.15 USART Interface Characteristics

Table 3-34 USART AC Timing

Symbol	Parameter		Minimum Value	Maximum Value	Unit
t_{cyc}	Input clock cycles	UART	4	-	t_{PCLK1}
		Clock synchronization mode	6	-	
t_{CKw}	Input Clock Width		0.4	0.6	t_{cyc}
t_{CKr}	Input Clock Rise Time		-	5	ns
t_{CKf}	Input Clock Fall Time		-	5	ns
t_{TD}	Send delay time 2.7V≤Vcc≤3.6V(1)	Clock synchronization mode	-	23	ns
	Send delay time 1.8V≤Vcc<2.7V	Clock synchronization mode	-	30	ns
t_{RDS}	Receive data setup time 2.7V≤Vcc≤3.6V(1)	Clock synchronization mode	17	-	ns
	Receive data setup time 1.8V≤Vcc<2.7V	Clock synchronization mode	23	-	ns
t_{RDH}	Receive data hold time	Clock synchronization mode	5	-	ns

1. Guarantee of mass production test.

Table 3-35 USART Maximum Baud Rates

Pattern		Highest baud rate
UART	Internal timer	PCLK1/8
	External timer	PCLK1/32
Clock synchronous mode 2.7V≤Vcc≤3.6V		12.0Mbps
Clock synchronous mode 1.8V≤Vcc<2.7V		8.0Mbps

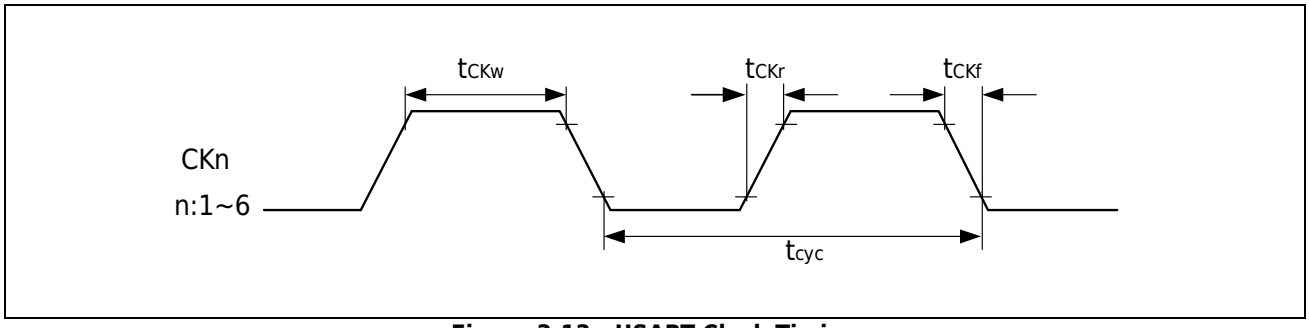


Figure 3-13 USART Clock Timing

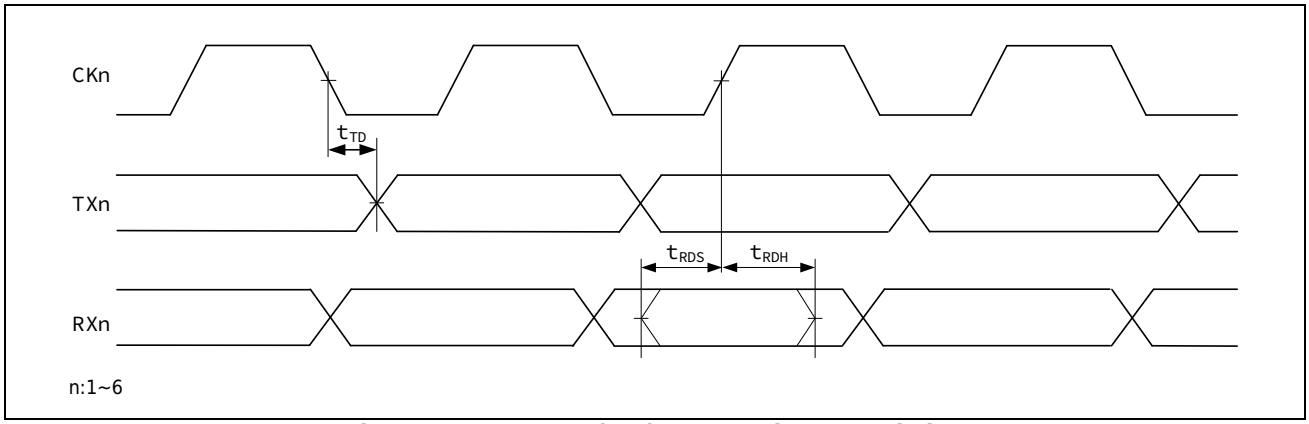


Figure 3-14 USART (CSI) Input and Output Timing

3.3.16 JTAG Interface Features

Table 3-36 JTAG Interface Features

Symbol	Parameter	Minimum Value	Typical Value	Max.	Unit
t_{TCKcyc}	JTCK clock cycle	50	-	-	ns
t_{TCKH}	JTCK clock high level	15	-	-	ns
t_{TCKL}	JTCK clock low level	15	-	-	ns
t_{TCKr}	JTCK clock rise time	-	-	5	ns
t_{TCKf}	JTCK clock fall time	-	-	5	ns
t_{TMSs}	JTMS establishment time(1)	10	-	-	ns
t_{TMSh}	JTMS hold time(1)	10	-	-	ns
t_{TDIs}	JTDI build time(1)	10	-	-	ns
t_{TDIh}	JTDI hold time(1)	10	-	-	ns
t_{TDOd}	JTDO data latency(1)	-	-	25	ns

1. Guarantee of mass production test.

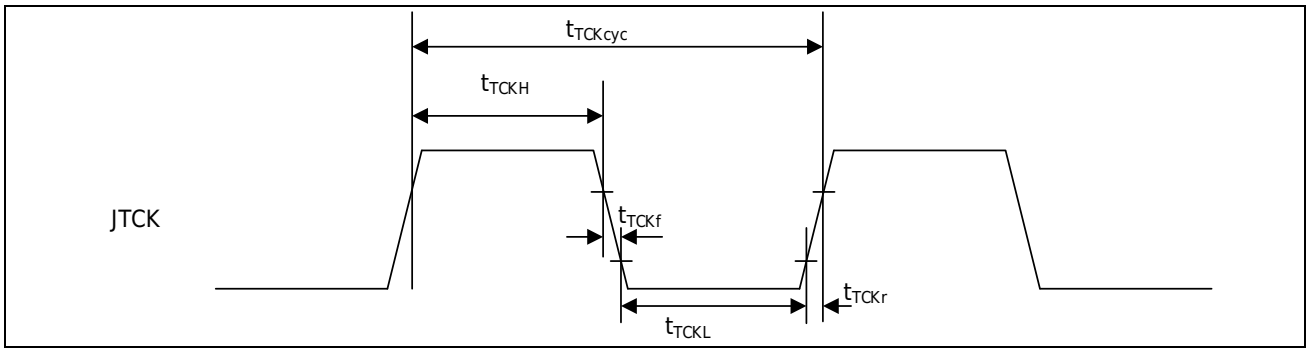


Figure 3-15 JTAG TCK clock

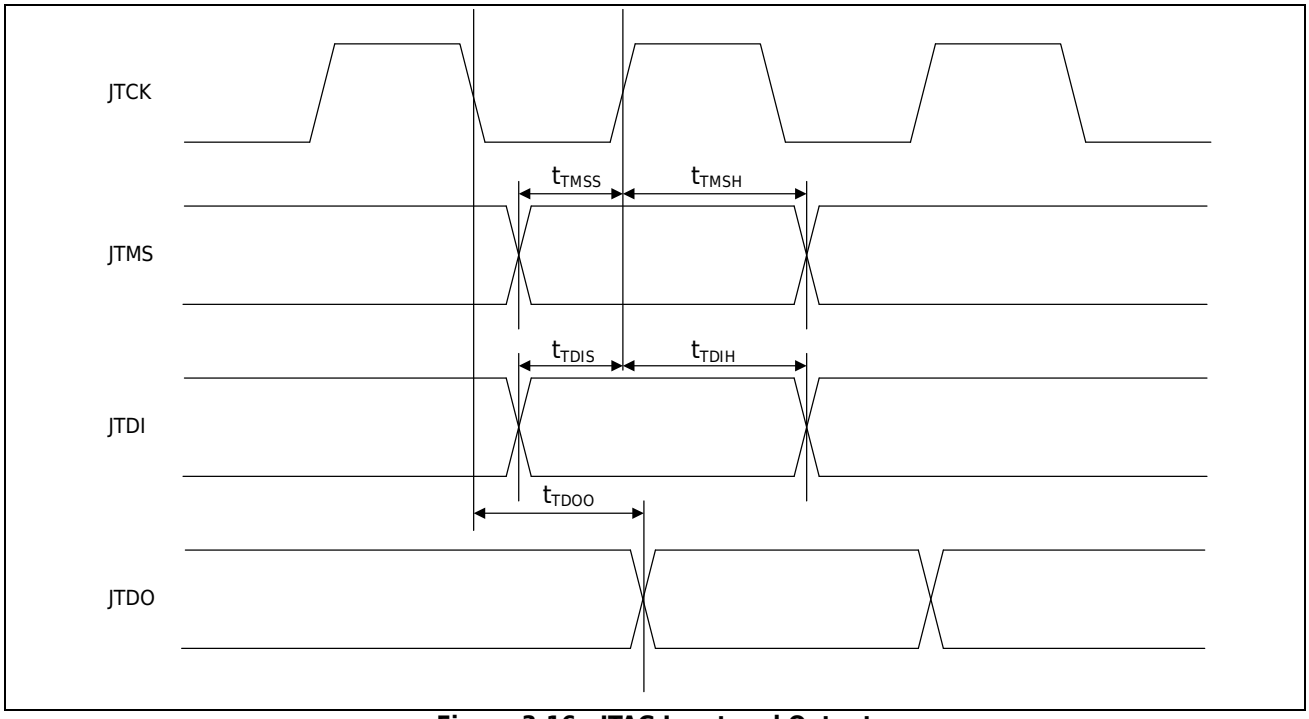


Figure 3-16 JTAG Input and Output

3.3.17 SWD Interface Characteristics

Table 3-37 SWD Interface Features

Symbol	Parameter	Minimum Value	Typical Value	Max.	Unit
$t_{SWCLKcyc}$	SWCLK clock period	50	-	-	ns
t_{SWCLKH}	SWCLK clock high level	15	-	-	ns
t_{SWCLKL}	SWCLK clock low level	15	-	-	ns
t_{SWCLKr}	SWCLK clock rise time	-	-	5	ns
t_{SWCLKf}	SWLCK clock fall time	-	-	5	ns
t_{SWDIs}	SWDI establishment time(1)	10	-	-	ns
t_{SWDIh}	SWDI hold time(1)	10	-	-	ns
t_{SWDOd}	SWDO data latency(1)	2	-	25	ns

1. Guarantee of mass production test.

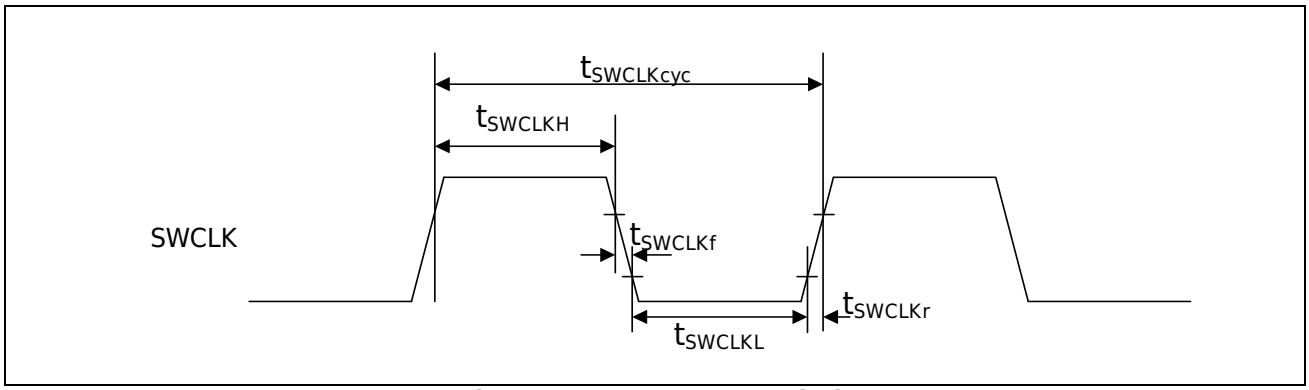


Figure 3-17 SWD SWCLK Clock

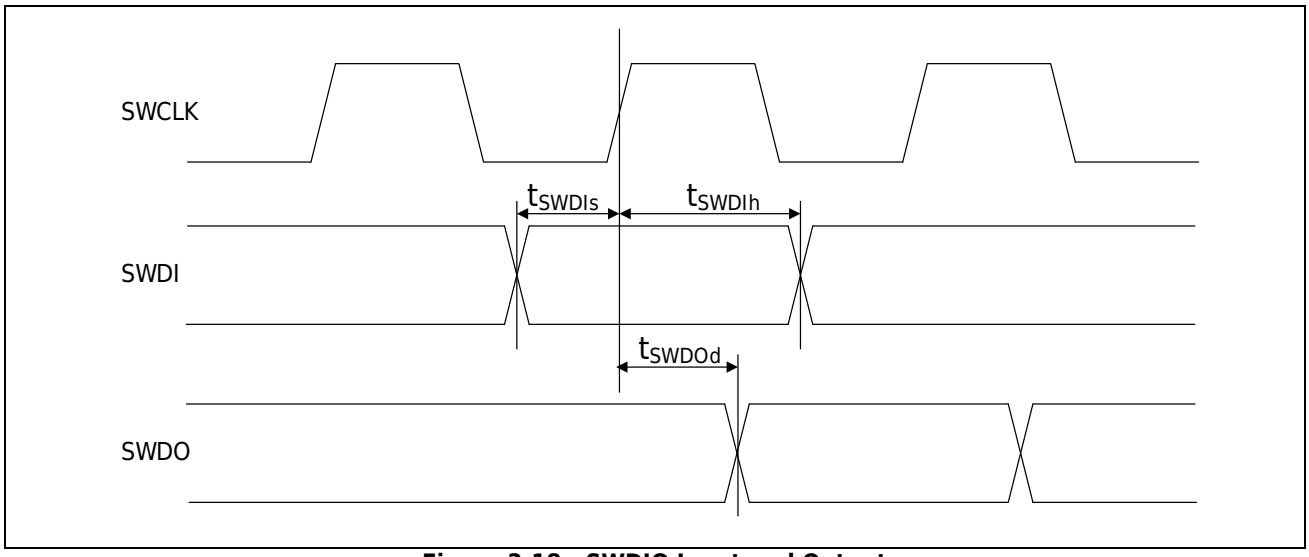


Figure 3-18 SWDIO Input and Output

3.3.18 TRACE Interface Features

Table 3-38 TRACE Interface Features

Symbol	Parameter	Minimum Value	Typical Value	Maximum Value	Unit
$t_{TRCLKcyc}$	TRACECK clock period	20	-	-	ns
t_{TRCKH}	TRACECK clock high level	7	-	-	ns
t_{TRCKL}	TRACECK clock low level	7	-	-	ns
t_{TRCKr}	TRACECK clock rise time	-	-	2.5	ns
t_{TRCKf}	TRACECK clock fall time	-	-	2.5	ns
t_{TRDd}	TRACED0~3 data latency(1)	1.6	-	8.4	ns

1. Guarantee of mass production test.

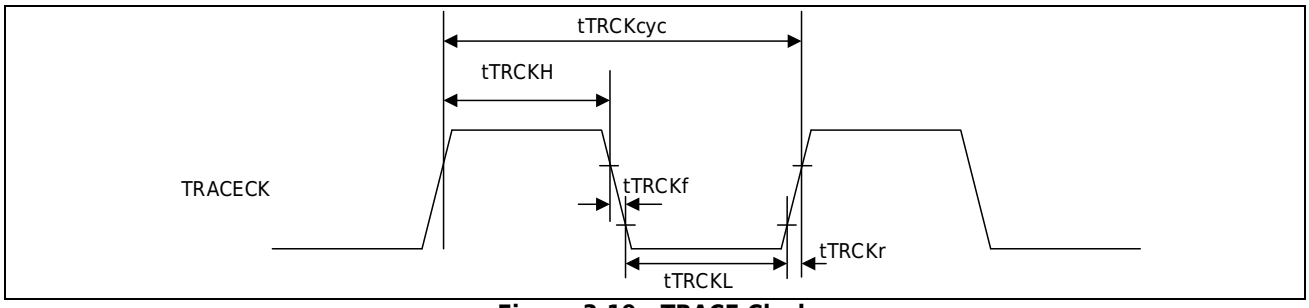


Figure 3-19 TRACE Clock

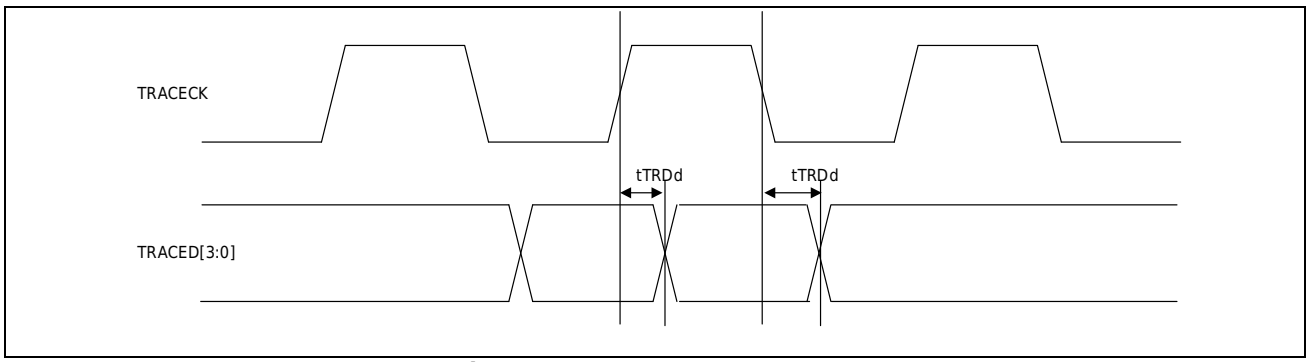


Figure 3-20 TRACE Data Output

3.3.19 12-bit ADC Characteristic

Table 3-39 ADC Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
$V_{AVCC/REFH}$	Power supply	-	1.8	-	3.6	V
f_{ADC}	ADC conversion clock frequency	In high-speed working mode V_{AVCC}=2.4~3.6V	1	-	60	MHz
		In low speed mode V_{AVCC}=1.8~2.4V	1	-	30	
		Ultra low speed working mode	1	-	8	
V_{AIN}	Conversion voltage range	-	V_{AVSS}	-	$V_{AVCC/VREFH}$	V
R_{AIN}	External input impedance(1)	Refer to Formula 1 for details	-	-	50	kΩ
R_{ADC}	Sampling switch resistance(1)	-	-	3	6	kΩ
C_{ADC}	Internal sampling and retention capacitance(1)	-	-	4	7	PF
t_D	Trigger conversion delay(1)	f_{ADC}=60MHz	-	-	0.3	μs
t_S	Sampling time(1)	f_{ADC}=60MHz	0.183	-	4.266	μs
			11	-	255	$1/f_{ADC}$
t_{CONV}	Single-channel total conversion time(1) (including sampling time)	f_{ADC}=60MHz 12-bit resolution	0.4	-	-	μs
		f_{ADC}=60MHz 10-bit resolution	0.37	-	-	μs
		f_{ADC}=60MHz 8 bit resolution	0.34	-	-	μs
		20 to 268 (sampling time Ts + successively approaching n-bit resolution + 1)				$1/f_{ADC}$
f_S	Sampling rate(1) f_{ADC}=60MHz	12-bit resolution single ADC	-	-	2.5	Msps
t_{ST}	Start time(1)	-	-	1	2	μs

1. Guarantee of design.

Formula 1: RAIN maximum formula

$$R_{AIN}=\frac{k}{f_{ADC}\times C_{ADC}\times \ln(2^{N+2})}-R_{ADC}$$

The above equation (Equation 1) is used to determine the maximum external impedance that keeps the error below 1/4LSB. Where N=12 (12-bit resolution), k is the number of sampling periods defined in the ADC_SSTR register.

Table 3-40 Input Channel Static Accuracy @ f_{ADC}=60MHz

Symbol	Parameter	Conditions	Typical Value	Maximum Value	Unit
E_T	Total unadjusted error	f_{ADC}=60MHz Input source impedance<1KΩ V_{AVCC}=2.4V/ 3.6V T_A=-40℃/ 105℃	±5.5	±7	LSB
E_O	Offset error		±4.5	±7	LSB
E_G	Gain error		±4.5	±7	LSB
E_D	Differential nonlinear error		±1.5	±3	LSB
E_L	Integral nonlinear error		±2.0	±4	LSB

Table 3-41 Input Channel Static Accuracy @ f_{ADC}=8MHz/ 30MHz

Symbol	Parameter	Conditions	Typical Value	Maximum Value	Unit
E_T	Total unadjusted error	f_{ADC}=8MHz/ 30MHz Input source impedance<1KΩ V_{AVCC}=1.8V T_A=-40℃/ 105℃	±5.5	±7	LSB
E_O	Offset error		±4.5	±7	LSB
E_G	Gain error		±4.5	±7	LSB
E_D	Differential nonlinear error		±1.5	±3	LSB
E_L	Integral nonlinear error		±2.0	±4	LSB

Table 3-42 Input Channel Dynamic Accuracy @ f_{ADC}=60MHz

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
ENOB	Significant digits	f_{ADC}=60MHz Input signal frequency = 2KHz Input source impedance=0Ω V_{AVCC}=2.4V/ 3.6V T_A=-40℃/ 105℃	10.5	-	Bits
SINAD	Signal noise harmonic ratio		65.0	-	dB
SNR	Signal noise ratio		65.1	-	dB
THD	Total Harmonic Distortion		-	-78.1	dB

Table 3-43 Input Channel Dynamic Accuracy @ f_{ADC}=8MHz/ 30MHz

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
ENOB	Significant digits	f_{ADC}=8MHz/ 30MHz Input signal frequency = 2KHz Input source impedance=0Ω V_{AVCC}=1.8V T_A=-40℃/ 105℃	10.5	-	Bits
SINAD	Signal noise harmonic ratio		65.0	-	dB
SNR	Signal noise ratio		65.1	-	dB
THD	Total Harmonic Distortion		-	-78.1	dB

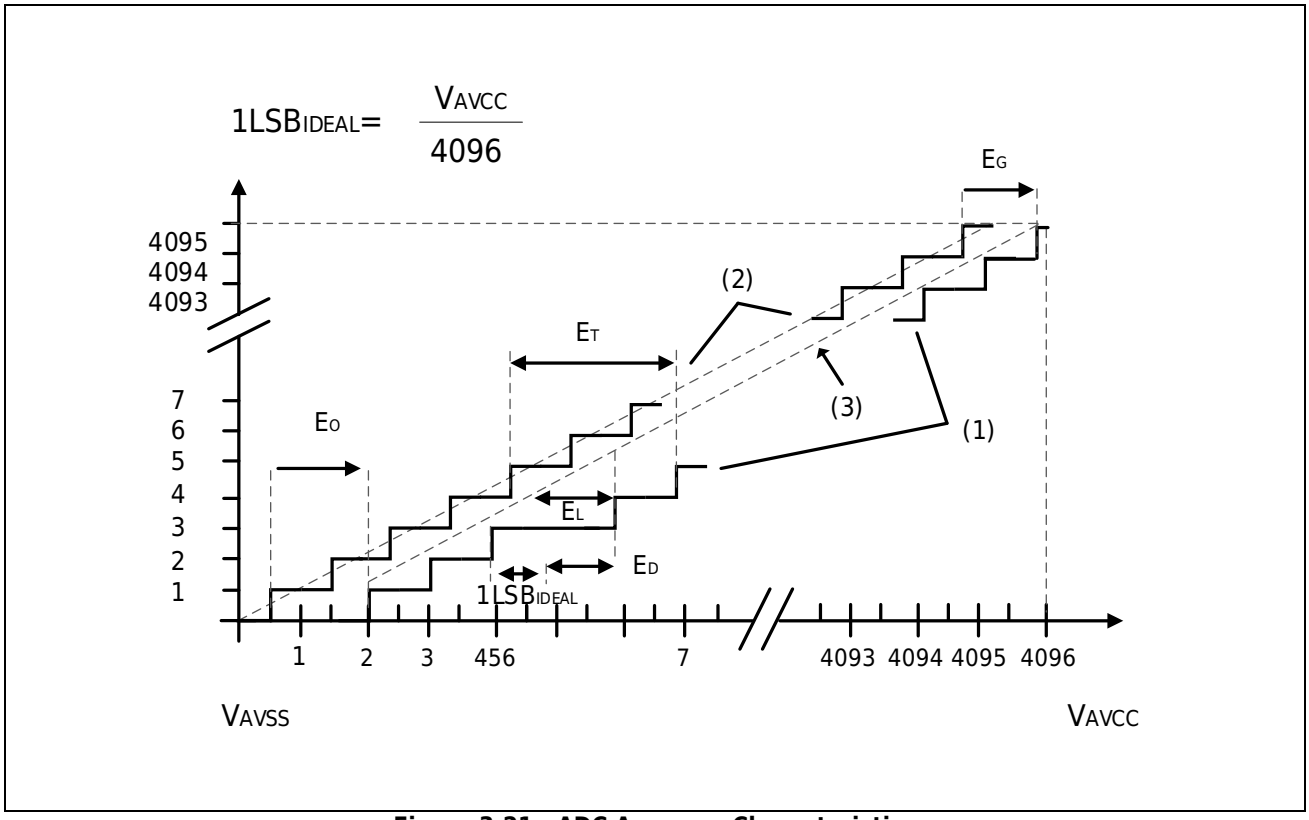


Figure 3-21 ADC Accuracy Characteristics

1. Refer to also table above.
2. Examples of actual transmission curves.
3. Ideal transfer curve.
4. End point correlation line.
5. E_T = Total Unadjusted Error: The maximum deviation between the actual and ideal transfer curve.

   E_O = Offset Error: The deviation between the first actual transition and the first ideal transition.

   E_G = Gain Error: The deviation between the last ideal transition and the last actual transition.

   E_D = Differential Nonlinearity Error: The maximum deviation between the actual step and the ideal value.

   E_L = Integral Nonlinearity Error: The maximum deviation between any actual transition and the line associated with the endpoints.

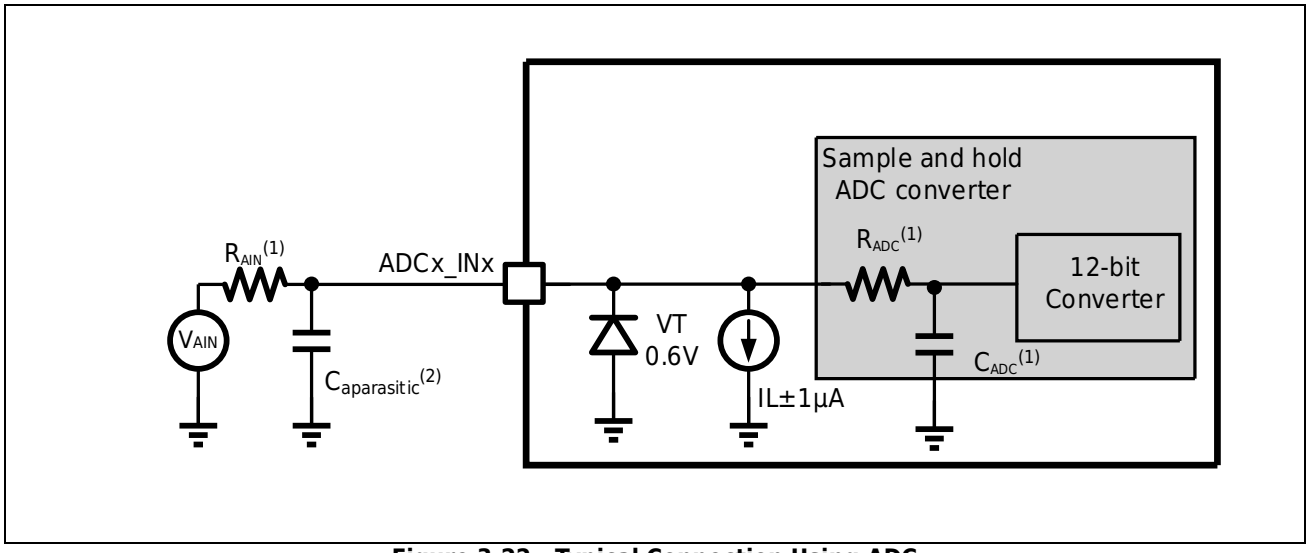


Figure 3-22 Typical Connection Using ADC

1. See Table 3-39 for R_{AIN}, R_{ADC}, and C_{ADC} values.
2. $C_{parasitic}$ means PCB capacitance (depending on soldering and PCB routing quality) as well as pad capacitance (about 5pF). Higher values of $C_{parasitic}$ result in less accurate conversions. To solve this problem, f_{ADC} should be reduced.

General PCB Design Guidelines

The power supply should be decoupled as shown in the figure below. The 0.1μF capacitor should be a (good quality) ceramic capacitor. These capacitors should be placed as close to the chip as possible.

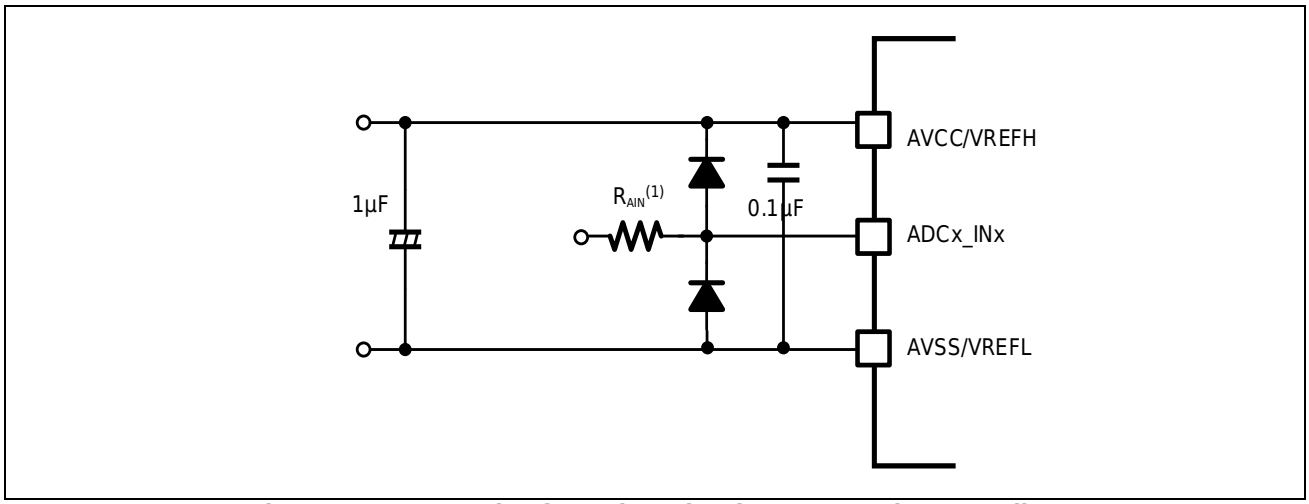


Figure 3-23 Example of Supply and Reference Supply Decoupling

1. See Table 3-39 for R_{AIN} values.

3.3.20 12-bit DAC Characteristic

Table 3-44 Characteristics when 12bit DAC port output is enabled and the output amplifier is enabled

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{AVCC}	Analog supply voltage	-	1.8	3.3	3.6	V
AO	Output voltage range(1)	-	0.2	-	V_{AVCC}-0.2	-
RL	Load Resistance	-	40	-	-	KΩ
CL	Load capacitance	-	-	-	50	pF
DNL	Differential nonlinearity error (deviation between two consecutive codes -1LSB)(1)	RL=40KΩ	-	-	±3	LSB
INL	Integral nonlinearity error (difference between the value measured at code I and the value at code I on the line between code 0 and the last code 4095)(1)	RL=40KΩ	-	-	±5	LSB
OE	Offset error (difference between measured value at code 2048 and ideal value VREF+/2)	-	-	-	±15	LSB
GE	Gain error	-	-	-	±1	%
T_{st}	Settling Time (Full Scale: Applies to 12-bit input code transition between lowest input code and highest input code until DAC output reaches ±4LSB of final value)(2)	-	-	2	3	μs

1. Guarantee of mass production test.
2. Guarantee of design.

Table 3-45 Characteristics when 12bit DAC port output is enabled and output amplifier is disabled

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{AVCC}	Analog supply voltage	-	1.8	3.3	3.6	V
AO	Output voltage range	-	0	-	V_{AVCC}-1LSB	V
CL	Load capacitance	-	-	-	20	pF
RO	Output resistance	-	-	8.6	12	KΩ
DNL	Differential nonlinearity error (deviation between two consecutive codes -1LSB)(1)	-	-	-	±2	LSB
TUE	Total Unadjustable Error	-	-	-	±24	LSB
T_{st}	Settling time (applicable to 12-bit input code transition between lowest input code and highest input code until DAC output reaches ±4LSB of final value, CL=10pF)(2)	-	-	1.5	2.5	μs

1. Guarantee of mass production test.
2. Guarantee of design.

Table 3-46 Characteristics when 12bit DAC port output is disabled and output amplifier is disabled

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{AVCC}	Analog supply voltage	-	1.8	3.3	3.6	V
AO	Output voltage range(1)	-	0	-	V_{AVCC}-1LSB	-
DNL	Differential nonlinearity error (deviation between two consecutive codes -1LSB)(1)	-	-	-	±2	LSB
TUE	Total Unadjustable Error(1)	-	-	-	±5	LSB
T_{st}	Settling time (applicable to 12-bit input code transition between the lowest input code and the highest input code until the DAC output reaches the final value ±1LSB, Vavcc≥2.7)(1)	-	-	95.5	117.3	ns
	Settling time (applicable to 12-bit input code transition between the lowest input code and the highest input code until the DAC output reaches the final value ±32LSB, Vavcc≥2.7)(1)	-	-	57.2	70.5	ns
	Settling time (applies to 12-bit input code transition between lowest input code and highest input code until DAC output reaches final value ±1LSB, Vavcc<2.7) (1)	-	-	-	121.6	ns
	Settling time (applies to 12-bit input code transition between lowest input code and highest input code until DAC output reaches final value ±32LSB, Vavcc<2.7) (1)	-	-	-	79.1	ns

1. Guarantee of design.

3.3.21 Comparator Characteristics

Table 3-47 Comparator Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{AVCC}	Analog supply voltage	-	1.8	3.3	3.6	V
V_I	Input voltage range	-	0	-	V_{AVCC}	V
T_{cmp}	Response time(1)	Comparator resolution voltage = 100 mV	-	30	50	ns
T_{set}	Input channel switching stabilization time	-	-	100	200	ns

1. Guarantee of design.

3.3.22 EXMC Characteristic

Table 3-48 EXMC features of internal EXCLK mode

Symbol	Parameter	Minimum Value	Typical Value	Maximum Value	Unit
t_add_d	Address line output delay time (2.7V~3.6V)(1)	-	-	12	ns
	Address line output delay time (1.8V~2.7V)(1)	-	-	18	ns
t_data_d	Data line output delay time (2.7V~3.6V)(1)	-	-	12	ns
	Data line output delay time (1.8V~2.7V)(1)	-	-	18	ns
t_ce_d	CE output delay time (2.7V~3.6V)(1)	-	-	9	ns
	CE output delay time (1.8V~2.7V)(1)	-	-	12	ns
t_we_d	WE output delay time (2.7V~3.6V)(1)	-	-	9	ns
	WE output delay time (1.8V~2.7V)(1)	-	-	12	ns
t_oe_d	OE output delay time (2.7V~3.6V)(1)	-	-	9	ns
	OE output delay time (1.8V~2.7V)(1)	-	-	12	ns
t_baa_d	BAA output delay time (2.7V~3.6V)(1)	-	-	9	ns
	BAA output delay time (1.8V~2.7V)(1)	-	-	12	ns
t_adv_d	ADV output delay time (2.7V~3.6V)(1)	-	-	9	ns
	ADV output delay time (1.8V~2.7V)(1)	-	-	12	ns
t_ale_d	ALE output delay time (2.7V~3.6V)(1)	-	-	9	ns
	ALE output delay time (1.8V~2.7V)(1)	-	-	12	ns
t_data_s	Data line input Setup time (2.7V~3.6V)(1)	24	-	-	ns
	Data line input Setup time (1.8V~2.7V)(1)	28	-	-	ns
t_data_h	Data line input Hold time(1)	0	-	-	ns
t_rb_s	RB input Setup time (2.7V~3.6V)(1)	24	-	-	ns
	RB input Setup time (1.8V~2.7V)(1)	28	-	-	ns
t_rb_h	RB input Hold time(1)	0	-	-	ns

1. Guarantee of mass production test.

Table 3-49 EXMC features of feedback EXCLK mode

Symbol	Parameter	Minimum Value	Typical Value	Maximum Value	Unit
t_add_d	Address line output delay time (2.7V~3.6V)(1)	-	-	12	ns
	Address line output delay time (1.8V~2.7V)(1)	-	-	18	ns
t_data_d	Data line output delay time (2.7V~3.6V)(1)	-	-	12	ns
	Data line output delay time (1.8V~2.7V)(1)	-	-	18	ns
t_ce_d	CE Output delay time (2.7V~3.6V)(1)	-	-	9	ns
	CE Output delay time (1.8V~2.7V)(1)	-	-	12	ns
t_we_d	WE Output delay time (2.7V~3.6V)(1)	-	-	9	ns
	WE Output delay time (1.8V~2.7V)(1)	-	-	12	ns
t_oe_d	OE Output delay time (2.7V~3.6V)(1)	-	-	9	ns
	OE Output delay time (1.8V~2.7V)(1)	-	-	12	ns
t_baa_d	BAA output delay time (2.7V~3.6V)(1)	-	-	9	ns
	BAA output delay time (1.8V~2.7V)(1)	-	-	12	ns
t_adv_d	ADV Output delay time (2.7V~3.6V)(1)	-	-	9	ns
	ADV Output delay time (1.8V~2.7V)(1)	-	-	12	ns
t_ale_d	ALE output delay time (2.7V~3.6V)(1)	-	-	9	ns
	ALE output delay time (1.8V~2.7V)(1)	-	-	12	ns
t_data_s	Data line input Setup time (1.8V~3.6V)(1)	7	-	-	ns
t_data_h	Data line input Hold time (2.7V~3.6V)(1)	5	-	-	ns
	Data line input Hold time (1.8V~2.7V)(1)	14	-	-	ns
t_rb_s	RB Input Setup time (1.8V~3.6V)(1)	7	-	-	ns
t_rb_h	RB Input Hold time (2.7V~3.6V)(1)	5	-	-	ns
	RB Input Hold time (1.8V~2.7V)(1)	14	-	-	ns

1. Guarantee of mass production test.

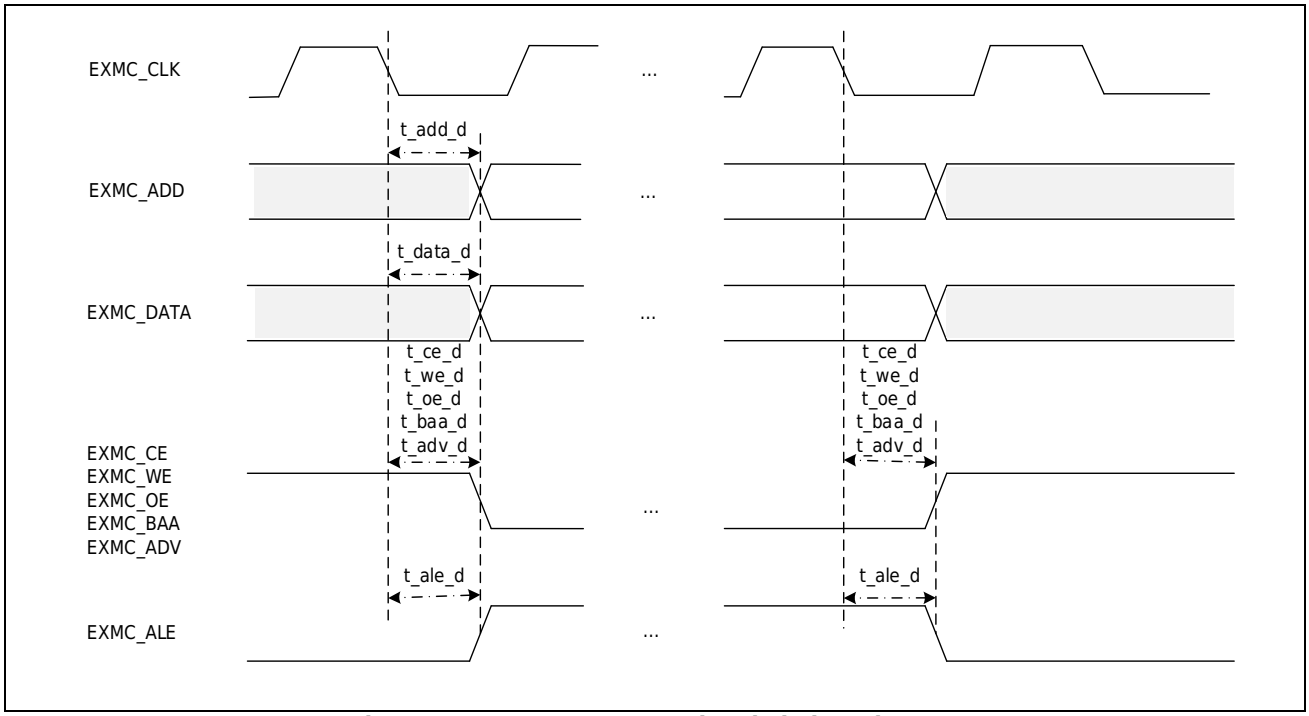


Figure 3-24 EXMC Output Signal Timing Diagram

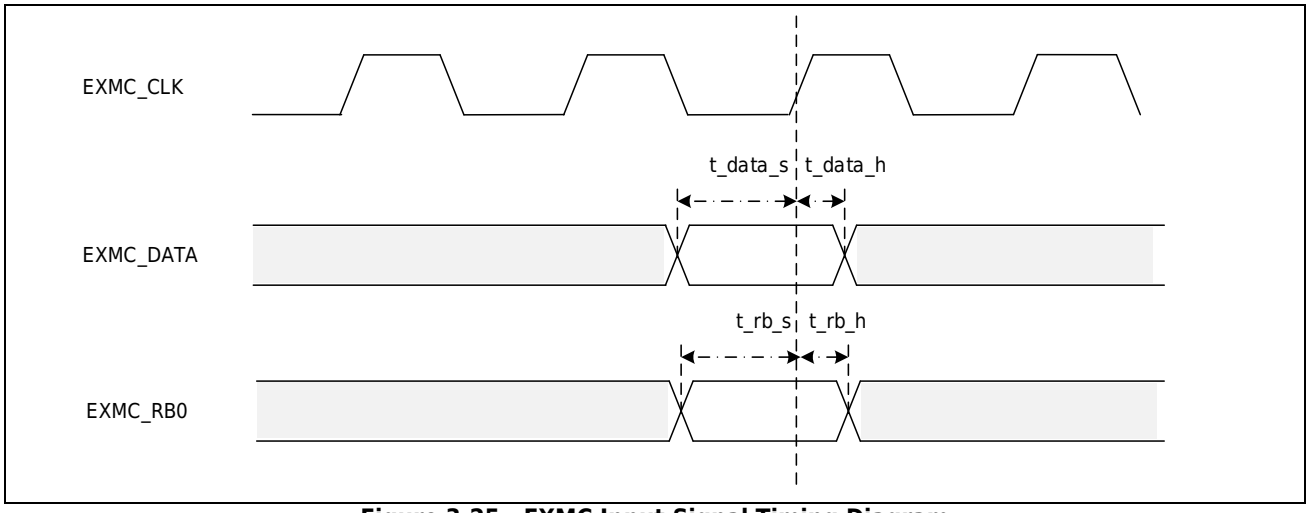


Figure 3-25 EXMC Input Signal Timing Diagram

3.3.23 EIRQ Filter Characteristics

Table 3-50 EIRQ Filter Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
W_{F_EIRQ}	EIRQ input filter width	INTC_EIRQCR.NOCSEL[1:0] = 0b00	0.6	-	1.0	μs
		INTC_EIRQCR.NOCSEL[1:0] = 0b01	1.3	-	2.0	μs
		INTC_EIRQCR.NOCSEL[1:0] = 0b10	2.6	-	4.0	μs
		INTC_EIRQCR.NOCSEL[1:0] = 0b11	5.2	-	8.0	μs

3.3.24 RX filter characteristics in USART1 Stop mode

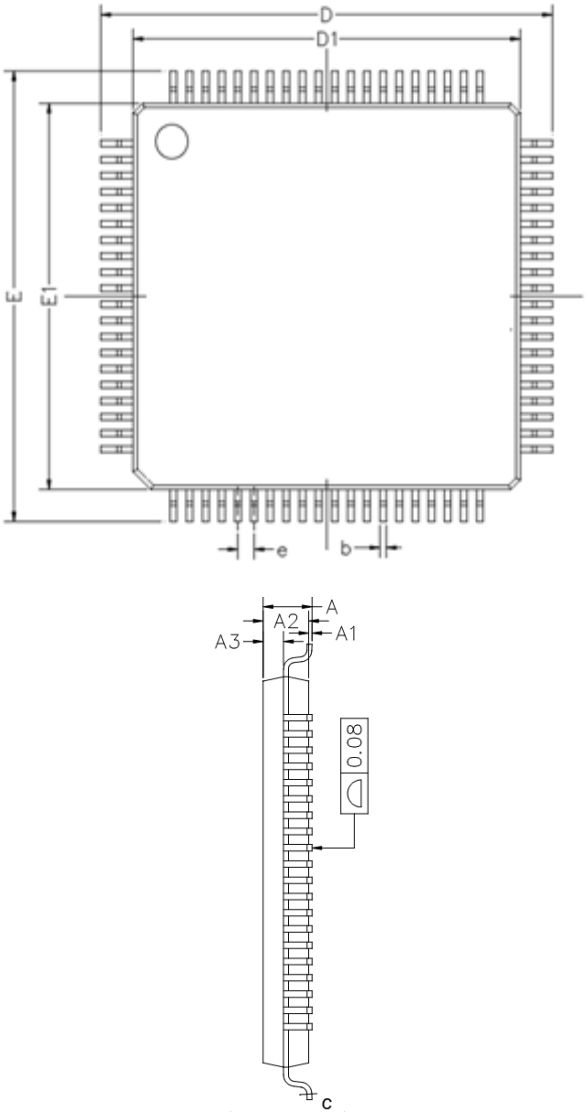
Table 3-51 RX Filter Characteristics in USART1 STOP Mode

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
W_{F_USART1}	USART1 input filter width	USART1_NFC.USART1_NFS[1:0] = 0b00	0.6	-	1.0	μs
		USART1_NFC.USART1_NFS[1:0] = 0b01	1.3	-	2.0	μs
		USART1_NFC.USART1_NFS[1:0] = 0b10	2.6	-	4.0	μs
		USART1_NFC.USART1_NFS[1:0] = 0b11	5.2	-	8.0	μs

4 Package Information

4.1 Packaging Size

LQFP80 package

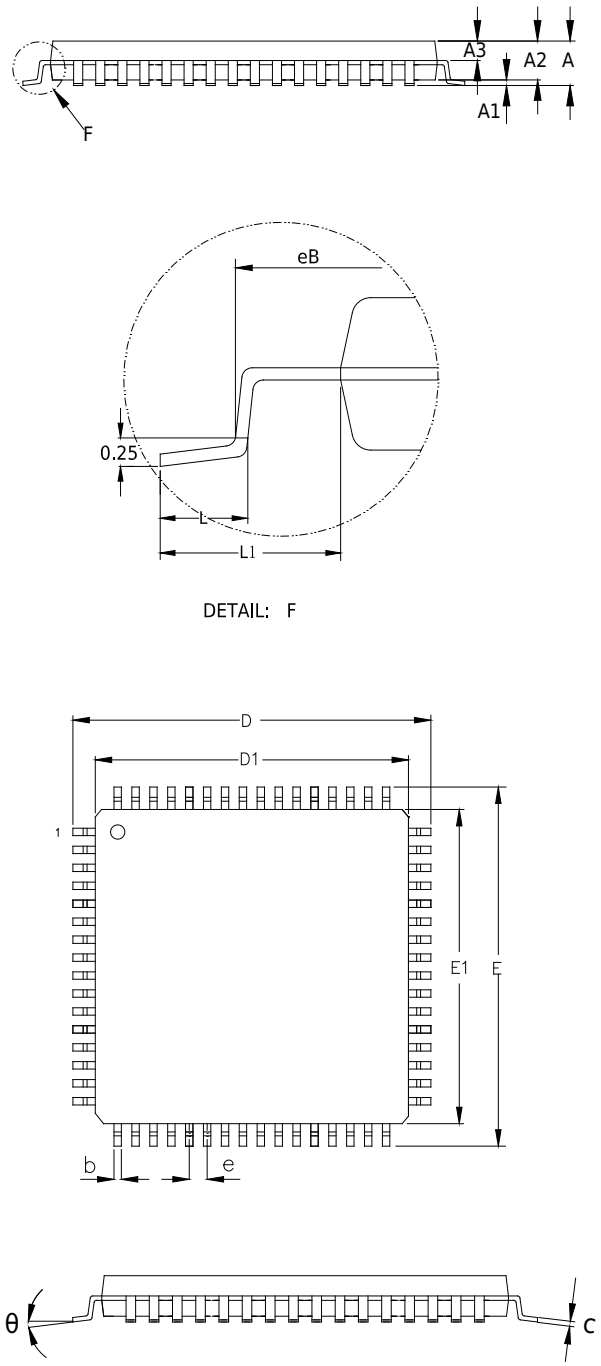


Symbol	12x12 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	0.22	0.27
c	0.09	--	0.20
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0°	3.5°	7°

NOTE:

- Dimensions “D1” and “E1” do not include mold flash.

LQFP64 package

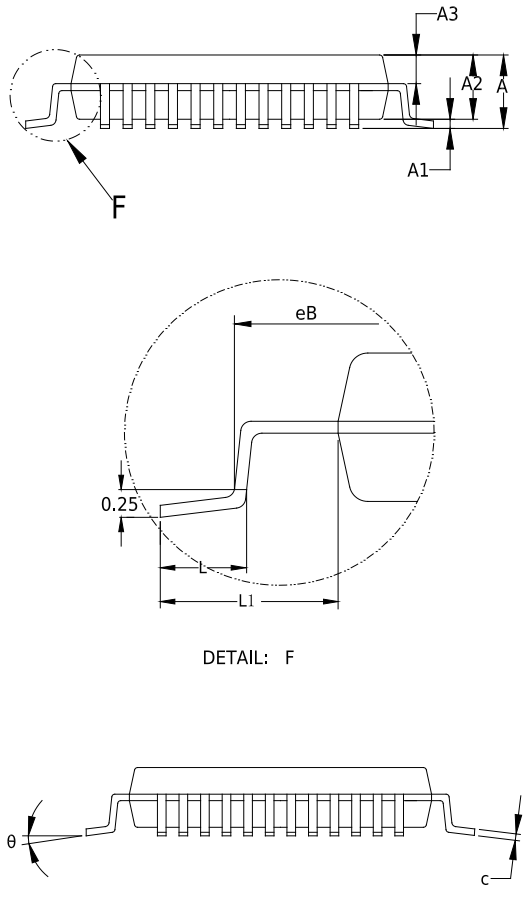


Symbol	10x10 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	0.22	0.27
c	0.09	--	0.20
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0°	--	7°

NOTE:

- Dimensions “D1” and “E1” do not include mold flash.

LQFP48 package



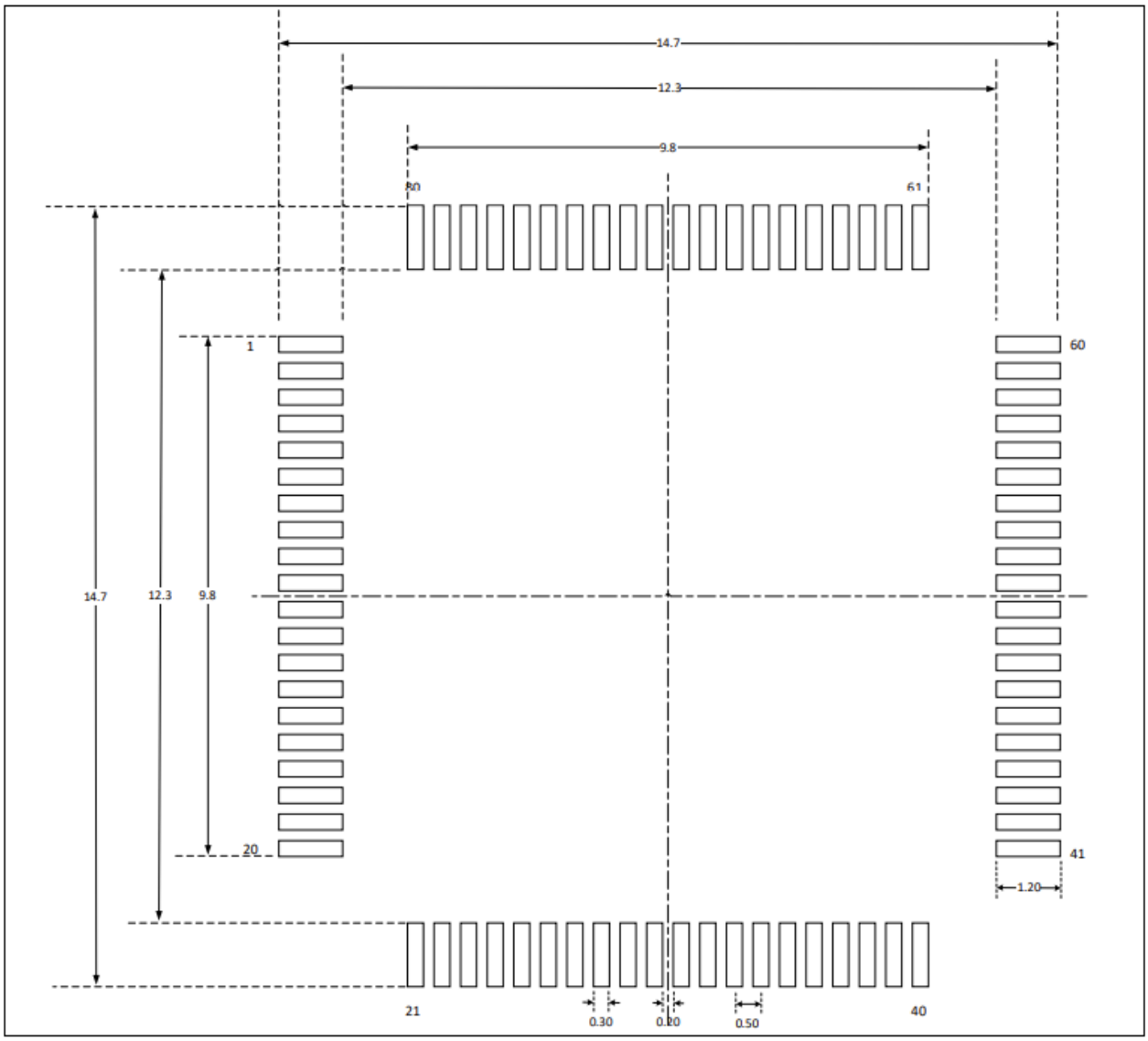
Symbol	7x7 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	0.22	0.27
c	0.09	--	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	--	7°

NOTE:

- Dimensions “D1” and “E1” do not include mold flash.

4.2 Schematic Diagram of Pad

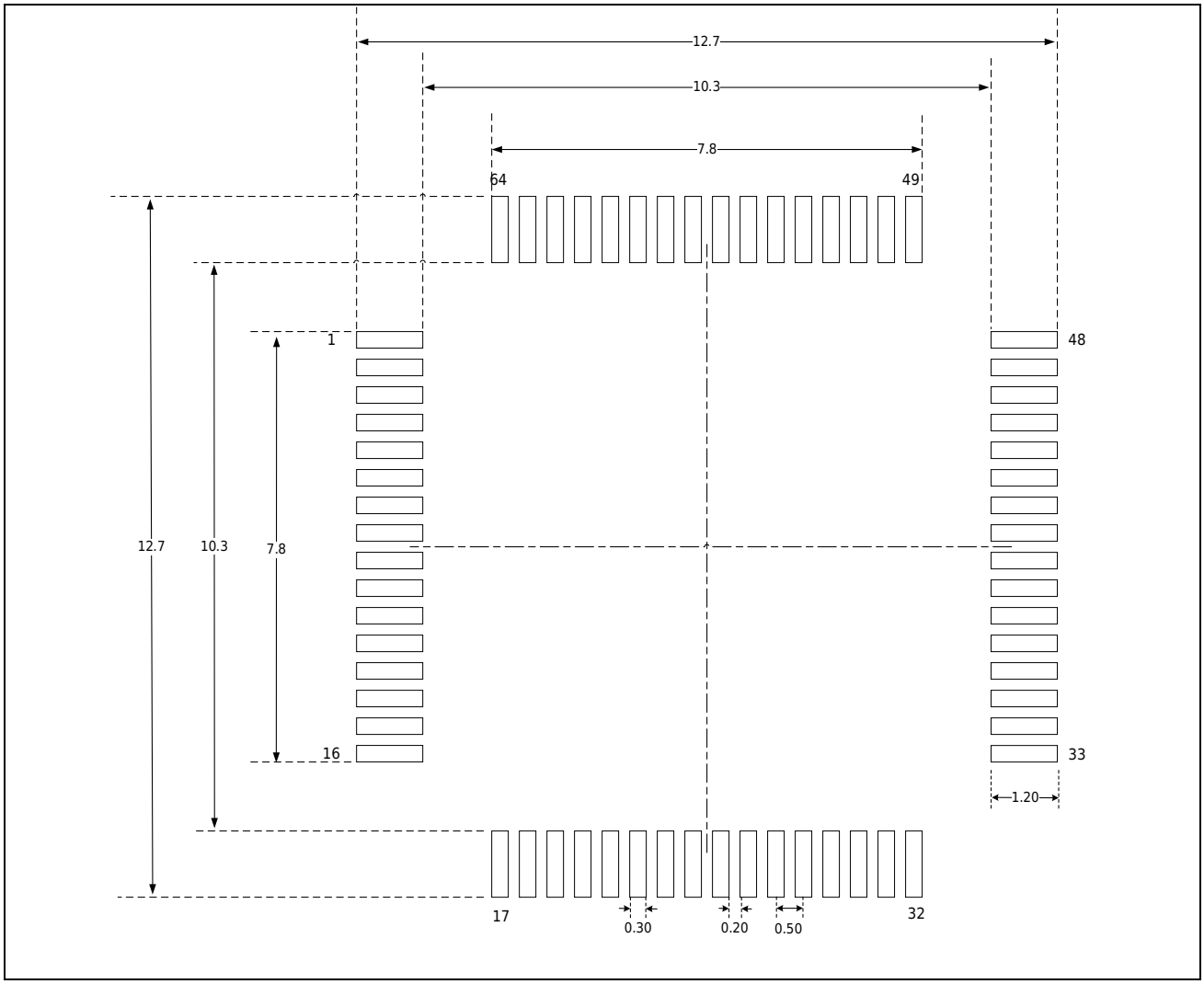
LQFP80 package (12mm x 12mm)



Note:

- *Dimensions are in millimeters.*
- *Dimensions are for reference only.*

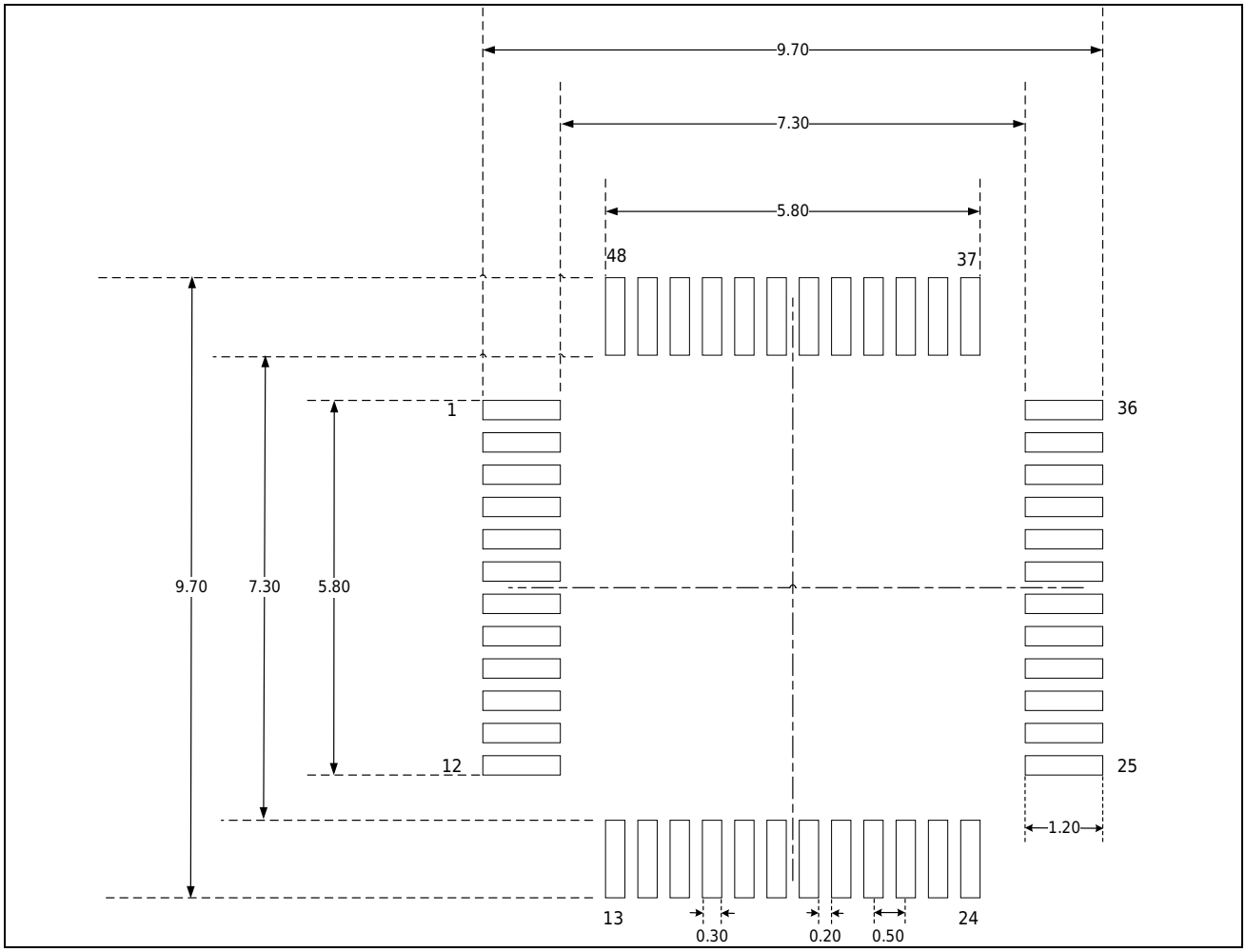
LQFP64 package (10mm x 10mm)



Note:

- *Dimensions are in millimeters.*
- *Dimensions are for reference only.*

LQFP48 package (7mm x 7mm)



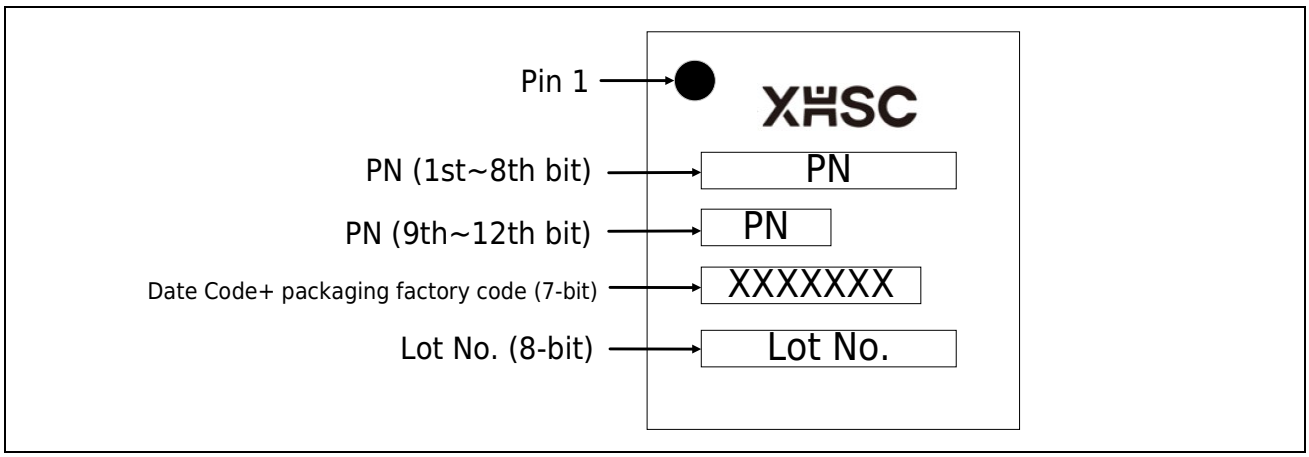
Note:

- *Dimensions are in millimeters.*
- *Dimensions are for reference only.*

4.3 Silkscreen instructions

The position and information of Pin 1 printed on the front of each package are given below.

LQFP80 package (12mm x 12mm) / LQFP64 package (10mm x 10mm) / LQFP48 package (7mm x 7mm)



Note:

– *The blank boxes in the above figure indicate optional marks related to production, which are not explained in this section.*

4.4 Packaging Thermal Resistance Coefficient

When the packaged chip works at the specified working environment temperature, the junction temperature Tj (°C) on the chip surface can be calculated according to the following formula:

$$T_j = T_A + (P_D \times \theta_{JA})$$

- T_A refers to the working environment temperature when the packaged chip is working, the unit is ℃;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is ℃/W;
- P_D is equal to the sum of the internal power consumption (P_{INT}) of the chip and the power consumption ($P_{I/O}$) generated by the I/O pin when the chip is working, and the unit is W.

  $P_{INT} = I_{CC} \times V_{CC}$

  $P_{I/O} = \sum(V_{OL} \times I_{OL}) + \sum((V_{CC} - V_{OH}) \times I_{OH})$

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable junction temperature T_J of the chip.

Table 4-1 Thermal resistance coefficient table for each package

Package Type and Size	Thermal Resistance Junction-ambient Value (θ_{JA})	Unit
LQFP80 12*12*1.4 e=0.5	55+/-10%	℃/W
LQFP64 10*10*1.4 e=0.5	65+/-10%	℃/W
LQFP48 7*7*1.4 e=0.5	75+/-10%	℃/W

5 Ordering Information

Function		Product Model		
		HC32A448 JCTI-LQ48	HC32A448 KCTI-LQFP64	HC32A448 MCTI-LQFP80
Main frequency (MHz)		200		
Kernel		M4		
Number of GPIOs		38	52	67
Power supply voltage range (V)		1.8~3.6		
Flash (KB)		256	256	256
SRAM (KB)		68		
DMA		2unit * 6ch		
Communication Interface	USART	6ch		
	SPI	3ch		
	I2C	2ch		
	CAN FD	2ch		
	QSPI	1ch		
	EXMC	not support	✓	✓
Timing and counting	Timer0	2unit		
	TimerA	5unit		
	Timer4	3unit		
	Timer6	2unit		
	WDT	1ch		
	SWDT	1ch		
	RTC	1ch		
Simulation	12bit ADC	3unit, 11ch	3unit, 17ch	3unit, 24ch

Function		Product Model		
		HC32A448 JCTI-LQ48	**HC32A448 KCTI-LQFP64**	**HC32A448 MCTI-LQFP80**
	12bit DAC	2ch	2ch	2ch
	CMP	4ch		
Simulation	PVD	✓		
Safety	TRNG	✓		
	AES256	✓		
	HASH (SHA256)	✓		
Co-processing	DCU	✓		
Operating temperature		-40~105℃		
Packaging (mm)	Encapsulation Form:	LQFP48 (7*7)	LQFP64 (10*10)	LQFP80 (12*12)
	Thickness	1.6	1.6	1.6
	Package style	Tray	Tray	Tray

Before ordering, please contact the sales window for the latest mass production information.

Version Revision History

Version Number	Revision Date	Modify the content
Rev1.00	2024/05/31	First edition release.