XIAOHUA SEMICONDUCTOR

HC32A052 Series

32-bit ARM® Cortex®-M0+ Microcontroller

Datasheet

Rev1.01

February 2026

Feature List

Support Features

- 64MHz Cortex-M0+ 32-bit CPU platform
- HC32A052 Series has a flexible power management system:
  - 20μA@3V DeepSleep mode: all clocks off, power-on reset active, IO state retention, IO interrupt active, all registers, RAM and CPU data save state power consumption
  - 40μA/MHz@3V@64MHz operating mode: CPU running, program running from Flash
  - 9μs wake-up time makes mode switching more flexible and efficient, and the system reacts more quickly
- 128KB Flash memory, with erase and write protection function
- 16KB RAM memory with parity check to enhance system stability
- GPIO: 40IO/48pin, 26IO/32pin
- Clock, Crystal
  - XTH: 8-24MHz
  - XTL: 32.768kHz
  - RCH: 12MHz
  - RCL: 32.768/38.4kHz
  - PLL: up to 64MHz
  - Hardware supports internal and external clock calibration and monitoring
- Timer/Counter
  - 2 composite 16-bit timers/counters
  - 4 high-performance 16-bit timers/counters
  - 1 low-power 16-bit timers/counters
  - 1 independent WDT, using 32k oscillator to provide WDT counting
  - 1 window WDT, counting using system clock
- Communication interface
  - 2-channel USART standard communication interface
  - Up to 2-channel LPUART low power communication interface, can work in DeepSleep mode
  - Up to 2-channel SPI standard communication interface
  - 2-channel I2C standard communication interface
  - 1-channel I2C Slave communication interface
  - 1-channel CAN communication interface
- Timer as buzzer frequency generator
- Hardware perpetual calendar RTC
- Hardware CRC-16/CRC-32 module
- Hardware 32-bit square divider
- Globally unique 10-byte ID number
- Integrate a 12-bit 1Msps sampling high-speed and high-precision SAR ADC with built-in follower to measure weak external signals
- Integrate a high-precision temperature sensor
- 2-way VC with integrated 64-level voltage programmable reference input
- Integrate LVD, configurable 16-level comparison level, can monitor port voltage and power supply voltage
- Integrate 2 OPAs
- SWD debugging solution provides a full-featured debugger
- Working conditions: -40-105℃, 2.0-5.5V
- Meets AEC-Q100 G2
- Package: LQFP48, QFN32

Support Model

HC32A052JATI-LQ48	HC32A052FAUI-QFN32TR

Statement

Precautions

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Preface

Number Format

- 0x prefix is used for hexadecimal numbers
- 0b prefix is used for binary numbers
- Numbers without prefix are in decimal representation

Security Statement

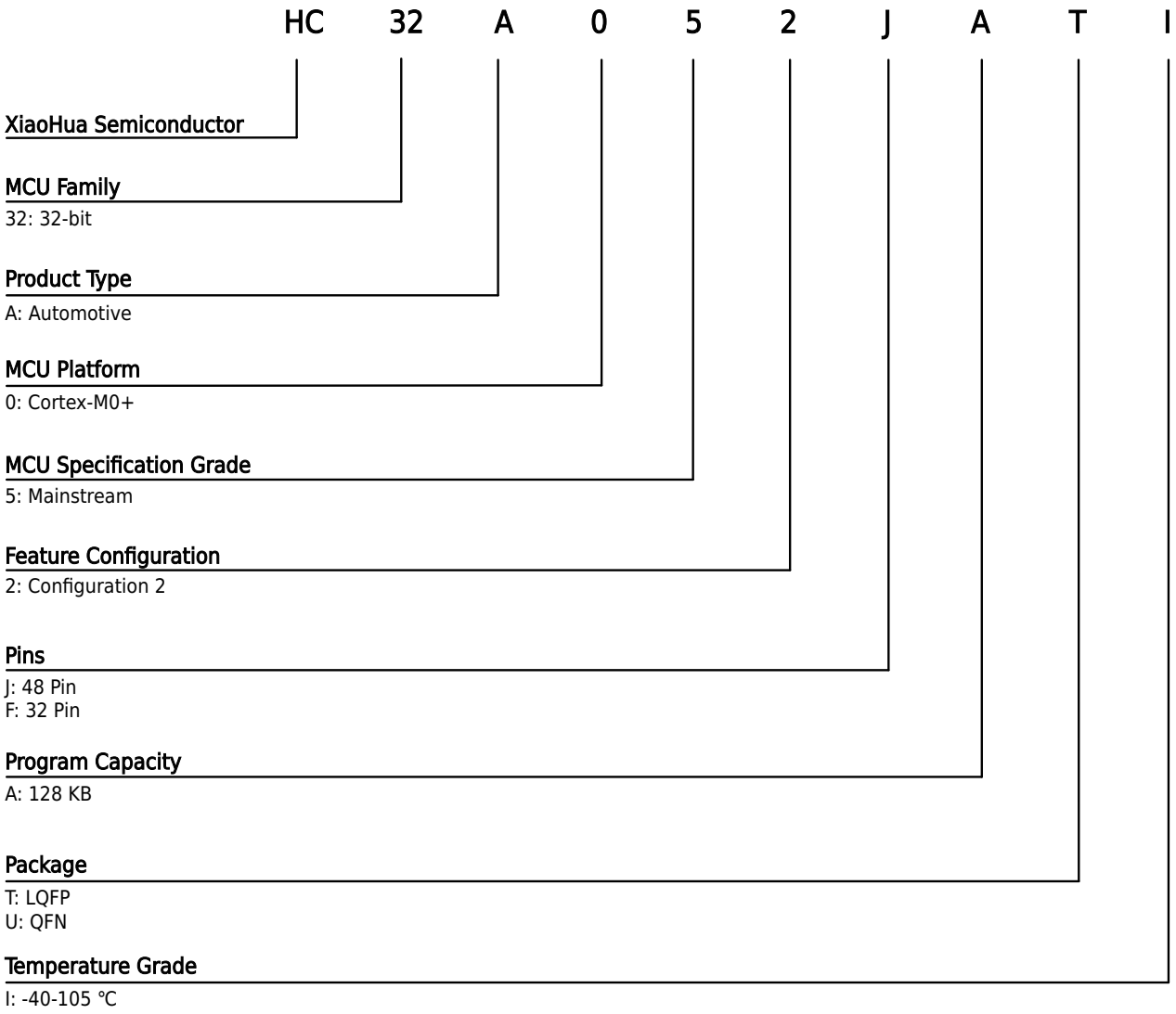
There may be potential security problems due to the use of a certain function or protocol, which need to be declared to remind users and avoid security risks.

Contents

1 Product Overview

1.1 Product Lineup

Product Name

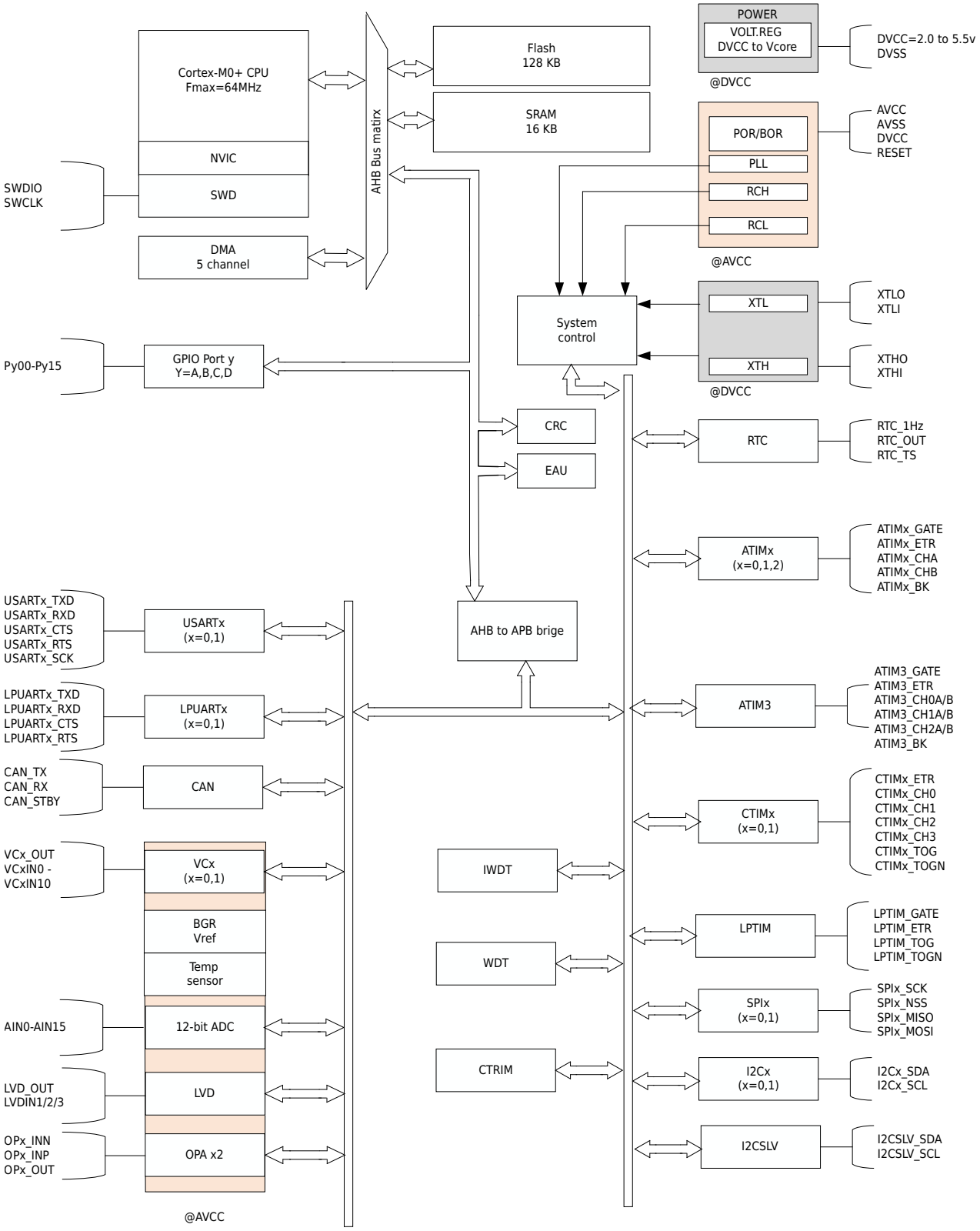


Model Function Comparison Table

Product Name		HC32A052JATI	HC32A052FAUI
Pins		48	32
GPIOs		40	26
CPU	Core	Cortex-M0+	
	Frequency	64MHz	
Memory	Flash	128KB	
	RAM	16KB	
Clock	RCH	12MHz	
	RCL	32.768/38.4kHz	
	PLL	Maximum 64MHz	
	XTH	8-24MHz	
	XTL	32.768kHz	
Power Voltage Range		2.0-5.5V	
Temperature Range		-40-105℃	
DMA Controller		1*5ch	
Timer		Advanced Timer ATIM0/1/2/3 Basic Timers (Multiplexed) BTIM0/1/2/3/4/5 General Timer GTIM0/1 Low Power Timer LPTIM	
RTC		1	
Watchdog Timer		IWDT *1 WWDT *1	
Connectivity	LPUART	LPUART0/1	LPUART1
	USART	USART0/1	USART0/1
	LIN	Support	Support
	ISO7816	Support	Support
	Infrared	Support	Support
	CAN	CAN 1 Unit	CAN 1 Unit
	I2C	I2C0/1	I2C0/1
	I2C SLV	I2C SLV 1Unit	I2C SLV 1Unit
	SPI	SPI0/1	SPI0
ADC, 12-bit		1*16ch	1*10ch
OPA		OPA0/1	-
VC		VC0/1	
LVD		Support	

Product Name	HC32A052JATI	HC32A052FAUI
Buzzer	Support	
Flash Security Protection	Support	
RAM Parity	Support	
CRC	Support	
EAU	Support	
CTRIM	Support	
Debug Function	SWD debug interface	
Package (mm*mm)	LQFP48 (7*7)	QFN32 (4*4)

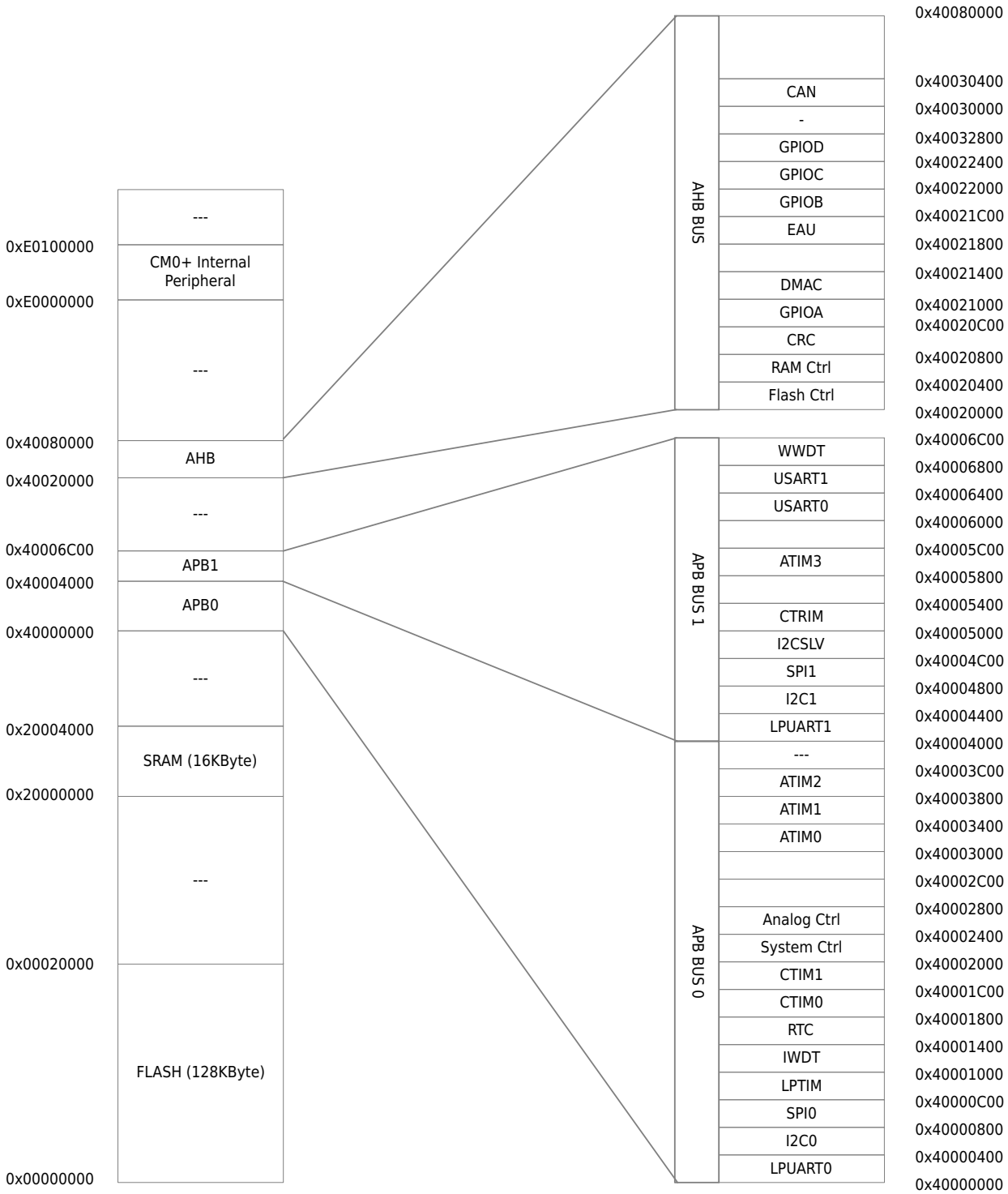
1.2 Functional Block Diagram



Note

Products in different packages support varying resources. For detailed specifications, please refer to Model Function Comparison Table.

1.3 Memory Map



Note

GPIOA and GPIOB/C/D modules use two separate address spaces.

Products in different packages support varying FLASH and SRAM sizes. Pay attention to the address space ranges during use. For details, refer to the Model Function Comparison Table.

2 Functional Description

2.1 32-bit Cortex-M0+ Core

The ARM Cortex-M0+ processor is based on the Cortex-M0 and integrates a 32-bit RISC processor with a computing performance of 0.95 Dhrystone MIPS/MHz. It also incorporates multiple new designs, including improved debugging and tracing capabilities, reduced instructions per cycle (IPC) count, an enhanced two-stage pipeline for Flash access, and integrates energy-saving technologies. The Cortex-M0+ processor fully supports Keil & IAR debuggers.

The Cortex-M0+ includes a hardware debug circuit supporting the 2-pin SWD debug interface.

ARM Cortex-M0+ support features:

Instruction set	Thumb/Thumb-2
Assembly line	2-stage assembly line
Performance efficiency	2.46 CoreMark/MHz
Performance efficiency	0.95 DMIPS/MHz in Dhrystone
Interrupt	32 fast interrupts
Interrupt priority	Configurable 4-level interrupt priority
Enhanced instruction	Single-cycle 32-bit multiplier
Debugging	Serial-wire debug port, supports four break points and two watch points.

2.2 128KB FLASH

Built-in fully integrated FLASH controller, no need for external high voltage input, high voltage generated by the fully built-in circuit for programming. Supports ISP, IAP, ICP functions.

2.3 16KB RAM

According to different ultra-low power modes selected by customers, RAM data will be retained. With hardware parity bit, in case the data is accidentally damaged, when the data is read, the hardware circuit will immediately generate an interrupt to ensure the reliability of the system.

2.4 Clock System

- A high-precision internal RCH clock with a frequency of 12MHz. Calibration values are preset at the factory.
- An internal RCL clock with frequencies of 32.768/38.4kHz.
- An external crystal oscillator XTH with a frequency range of 8-24MHz.
- An external 32.768kHz crystal oscillator XTL, primarily providing the RTC real-time clock.
- A PLL with an output frequency range of 12-64MHz.

2.5 Operating Mode

1. Active Mode: CPU running, on-chip peripherals running.
2. Sleep mode: CPU halted, on-chip peripherals running.
3. DeepSleep mode: CPU halted, low-power on-chip peripherals running.

2.6 RTC

The RTC (Real-Time Clock) is a functional module supporting BCD data format, typically using a 32.768kHz crystal as its clock. It enables perpetual calendar functionality with configurable interrupt periods: month/day/hour/minute/second. 24/12 hour time mode, the hardware automatically corrects leap years. It features precision compensation, with maximum accuracy of 0.96ppm. Precision compensation can be performed using either the internal or external temperature sensor. Software adjustments of +1/-1 are available for year/month/day/hour/minute/second, with a minimum adjustable precision of one second.

The RTC calendar recorder used to indicate time and date does not reset the register when the MCU is reset by external factors.

2.7 GPIO

It can provide up to 40 GPIO ports, some of which are multiplexed with analog ports. Each port is controlled by independent control register bits and supports FAST IO. Supports edge-triggered interrupts and level-triggered interrupts, and can wake up the MCU to working mode from various ultra-low power consumption modes. Supports bit set, bit clear, and bit set clear operations. Supports CMOS Push-Pull output, Open-Drain output. Built-in pull-up resistor, pull-down resistor, with Schmitt trigger input filter function. The output drive capability is configurable, and the maximum current drive capability is 18mA. All general-purpose IOs can support external asynchronous interrupts.

2.8 NVIC

The Cortex-M0+ processor integrates a Nested Vectored Interrupt Controller (NVIC) supporting up to 32 interrupt request (IRQ) inputs. With 4 interrupt priority levels, it can handle complex logic for real-time control and interrupt processing.

2.9 RESET

This product features 7 reset signal sources. Each reset signal can restart the CPU, reset most registers, and point the program counter (PC) to the starting address.

- Digital area power-on and power-off reset POR
- External Reset PAD, low level is reset signal
- WWDT reset
- IWDT reset
- LVD low voltage reset
- Cortex-M0+ SYSRESETREQ software reset
- Cortex-M0+ LOCKUP hardware reset

2.10 DMAC

The DMAC (Direct Memory Access Controller) function block can transmit data at high speed without passing through the CPU. Using DMAC can improve system performance.

2.11 Timer

Name	Width	Prescaler	Count Direction	PWM	Capture	Complementary Output
ATIM0/1/2	16/32	1/2/4/8/16/32/64/256	Up count/ Count down/ Up and down count	2	2	1
ATIM3	16/32	1/2/4/8/16/32/64/256	Up count/ Count down/ Up and down count	6	6	3
CTIM0/1	16	1-32768	Up count	4	4	-

The composite timer CTIM can be configured as a timer that supports 4-channel comparison capture function, or it can be configured as 3 basic timers. The basic timer is a timer with only timing and counting functions.

Adcanced timer includes four timers: ATIM0/1/2/3, supporting the following functions:

- PWM independent output, complementary output
- Capture input
- Pulse width measurement
- Quadrature encoder counting function
- Single pulse mode
- External counting function
- Dead-time control
- Braking control
- Cycle-by-cycle current limiting
- Edge alignment, symmetric center alignment and asymmetric center alignment PWM output

ATIM0/1/2 is a synchronous timer/counter, which can be used as a 16-bit timer/counter with automatic reloading function, or as a 32-bit timer/counter without reloading function. Each timer of ATIM0/1/2 has 2 channels of capture and comparison function, which can generate 2 channels of independent PWM output or 1 group of complementary PWM outputs. With dead zone control function.

ATIM3 is a multi-channel general-purpose timer with all functions of ATIM0, capable of generating 3 sets of complementary PWM outputs or 6 independent PWM channels, with up to 6 input capture channels. With dead zone control function.

The low-power timer LPTIM is an asynchronous 16-bit timer/counter that can continue timing/counting via the internal low-speed RC oscillator or external low-speed crystal oscillator even when the system clock is disabled. Wake up the system in low-power mode through interrupts.

2.12 WDT

The IWDT is a configurable 12-bit timer that provides a reset in case of MCU malfunction, with a built-in RCL (32.768kHz/38.4kHz) clock input as the counter clock. In debug mode, it can be configured to pause or continue running; the IWDT can only be restarted by writing a specific sequence.

WWDT is a 7-bit timer. When external interference or unforeseen logic conditions cause the application program to deviate from the normal running sequence, WWDT can detect such software failures and generate interrupts or resets.

2.13 USART

2-channel Universal Synchronous Asynchronous Receiver/Transmitter.

Basic functions of USART:

- Support full-duplex asynchronous communication and full-duplex clock synchronous communication
- Support multi-machine communication
- Support smart card 7816 interface communication
- Supports 2 infrared modes: 3/16 and 38K modulation
- Support LIN
- Built-in dual buffers enable full-duplex communication
- 2 frame lengths: 8 bits, 9 bits
- 2 stop lengths: 1 bit, 2 bits
- 2 data sequence orders: MSB first, LSB first
- Supports frame error, check error, overflow error, receiving data full, sending data empty, sending completed, timeout interrupt
- Support decimal frequency division
- Support configurable 8x or 16x oversampling, providing the possibility for flexible configuration of speed tolerance and clock tolerance
- Support single-wire half-duplex communication
- Support DMA
- Support TX/RX pin configuration exchangeable
- Support modem hardware flow control
- Support timeout function

2.14 LPUART

2-channel Low-Power Universal Asynchronous Receiver/Transmitter (LPUART) that can operate in low-power mode.

Basic functions of LPUART:

- Configuration clock PCLK
- Transmission clock SCLK (SCLK can select XTL, RCL and PCLK)
- Support synchronous half-duplex, asynchronous full-duplex and single-wire half-duplex transmission.
- Programmable serial communication function
  - 2 character lengths: 8 bits, 9 bits
  - 3 check methods: no check, odd check, even check
  - 3 stop lengths: 1 bit, 1.5 bits, 2 bits
- Supports transmitting and receiving data in low power mode
- 16-bit baud rate counter
- Support hardware flow control (RTS, CTS)
- Support multi-machine communication and automatic address recognition
- Support data transfer via DMA

2.15 CAN

CAN (Controller Area Network) bus is a bus standard that can realize mutual communication between microprocessors or devices without host device.

- Fully supports CAN2.0A/CAN2.0B protocols
- Upward compatible with CAN-FD
- Supports a maximum communication baud rate of 1Mbit/s
- Supports baud rate prescaler of 1 to 1/256 for flexible baud rate configuration
- 10 receive buffers
  - FIFO mode
  - Messages stored will not be overwritten by erroneous or unreceived data
- 1 high-priority PTB
- 4 STB
  - FIFO Mode
  - Priority arbitration method
- 8 independent filter groups
  - Support 11-bit standard ID and 29-bit extended ID
  - Programmable ID CODE bits and MASK bits
- Both PTB and STB support single send mode
- Supports silent mode
- Supports loopback mode
- Supports capturing transmission error types and locating bit arbitration lost bits
- Programmable error warning value
- Supports ISO11898-4 defined time-trigger CAN and receive timestamps

2.16 SPI

2-channel Serial Peripheral Interface(SPI).

Basic features of SPI:

- Can be configured as master or slave, support multi-machine mode
- The maximum division factor in master mode is PCLK/2
- The maximum division factor in slave mode is PCLK/4
- Multiple communication modes: full-duplex, single-wire half-duplex, simplex
- 2 transmission orders: MSB first or LSB first
- Various data frame lengths: 4bits-16bits
- 2 NSS methods: hardware control, software control
- Configurable serial clock polarity and phase
- Support DMA

2.17 I2C

2-channel I2C, using serial synchronous clock, can realize data transmission between devices at different rates.

Basic features of I2C:

- Support 4 working modes of master sending/receiving and slave sending/receiving

- Support 3 operating rates: Standard (100kbps)/Fast (400kbps)/High-speed (1Mbps)
- Support 7-bit addressing function
- Support noise filtering function
- Support 3 slave addresses
- Support broadcast address
- Support interrupt status query function

2.18 I2CSLV

The I2C Slave Module (I2CSLV) is a 2-wire bidirectional serial bus compatible with the I2C 3.0 bus specification. It achieves a transmission rate of 3.4 Mbps in high-speed mode.

- Transmission rate: standard (about 100kbps), fast (400kbps), ultra-fast (1Mbps), and high speed (3.4Mbps, the module working clock PCLK must be no less than 24MHz)
- Only supports slave mode
- Supports clock low-level extension function to interface with faster masters
- Supports 7-bit slave address and 10-bit slave address
- Support 4 slave addresses
- Support SCL low level timeout
- Support Device ID reading

2.19 CTRIM

The clock calibration timer can adjust and calibrate the RC clock frequency and the clock frequencies of other RC oscillations. It can also be used as a general timer or an automatic wake-up timer. When RCH real-time calibration is enabled and a precise reference clock exists in the system, the RCH's full working range accuracy can reach 1%.

2.20 Electronic Signature

Each chip has a unique 10-byte device identification number before leaving the factory, including wafer lot information, chip coordinate information, and so on.

2.21 CRC

CRC16 conforms to the polynomial given in ISO/IEC13239: $x^{16}+ x^{12}+ x^{5}+ 1$.

CRC32 conforms to the polynomial given in ISO/IEC13239: $x^{32}+ x^{26}+ x^{23}+ x^{22}+ x^{16}+ x^{12}+ x^{11}+ x^{10}+ x^{8}+ x^{7}+ x^{5}+ x^{4}+ x^{2}+ x + 1$.

2.22 EAU

The Extended Arithmetical Unit (EAU) is a coprocessor designed specifically for arithmetic operations. It efficiently performs signed integer division, unsigned integer division, and integer square root operations, Cortex-M0+ providing effective supplement and extension to the arithmetic commands of the core.

- Supports the square root operation of 32-bit unsigned integers, and can obtain the square root and remainder.
- Supports 32-bit by 32-bit signed and unsigned integer division, and can obtain the quotient and remainder.
- Supports an unsigned division by zero flag.
- Supports a signed division by zero flag and an overflow flag.

2.23 ADC

A monotonic no missing code 12-bit successive approximation register analog-to-digital converter achieves a sampling rate of 1 Msps when operating with a 16MHz ADC clock. The reference voltage can be selected from the on-chip precision voltage (1.5V or 2.5V) or from an external input or power supply voltage.

- 12-bit conversion accuracy
- 1Msps conversion speed
- Up to 18 input channels are supported, including 16 external pin inputs, 1 internal temperature sensor voltage channel, and 1 channel of 1/3 AVCC voltage
- 4 reference sources: AVCC voltage, EXVREF pins, internal 1.5V reference voltage, internal 2.5V reference voltage
- ADC voltage input range: 0-Vref
- Built-in signal follower, which can convert high-impedance signals
- Multiple conversion modes: single conversion, SQR scan single sequence conversion, SQR scan continuous conversion, SQR scan discontinuous conversion, JQR scan conversion, continuous conversion accumulation
- Software can configure ADC conversion rate
- Support on-chip peripherals to automatically trigger ADC conversion, effectively reducing chip power consumption and improving real-time conversion
- Input channel voltage threshold monitoring

2.24 VC

Chip pin voltage monitoring/comparison circuit. 11 configurable positive external input channels, 11 configurable negative external input channels; 4 internal negative input channels including 1-channel internal temperature sensor voltage, 1-channel ADC module reference voltage, and 1-channel 64-step resistor divider voltage. Can generate asynchronous interrupts based on rising/falling edges to wake up the MCU from low-power modes. Configurable software anti-shake function.

2.25 LVD

Detects chip supply voltage or pin voltage, supporting the following functions:

- 4 monitoring sources: AVCC, PC13, PB08, PB07
- 16-stage threshold voltage, optional
- 8 trigger conditions, combinations of high level, rising edge and falling edge
- 2 trigger results: reset and interrupt
- 8-stage filter configuration to prevent false triggering
- With hysteresis function, strong anti-interference

2.26 OPA

Operational Amplifier (OPA) can be flexibly configured and is suitable for simple amplifier and Buffer applications.

2.27 Embedded Debugging System

Embedded debugging solution, providing a full-featured real-time debugger, with standard mature Keil/IAR and other debugging and development softwares. Support four hard breakpoints and multiple soft breakpoints.

2.28 Programming Mode

Support programming modes: online programming and offline programming.

Support programming protocols: ISP protocol, SWD protocol.

Support programming interface: ISP protocol and SWD protocol share SWD port.

When reset, the BOOT0 (PD03) pin is high level, the chip works in ISP programming mode, and Flash can be programmed through ISP protocol.

When reset, the BOOT0 (PD03) pin is low level, the chip works in user mode, the chip executes the program code in the Flash, and the Flash can be programmed through the SWD protocol.

2.29 High Security

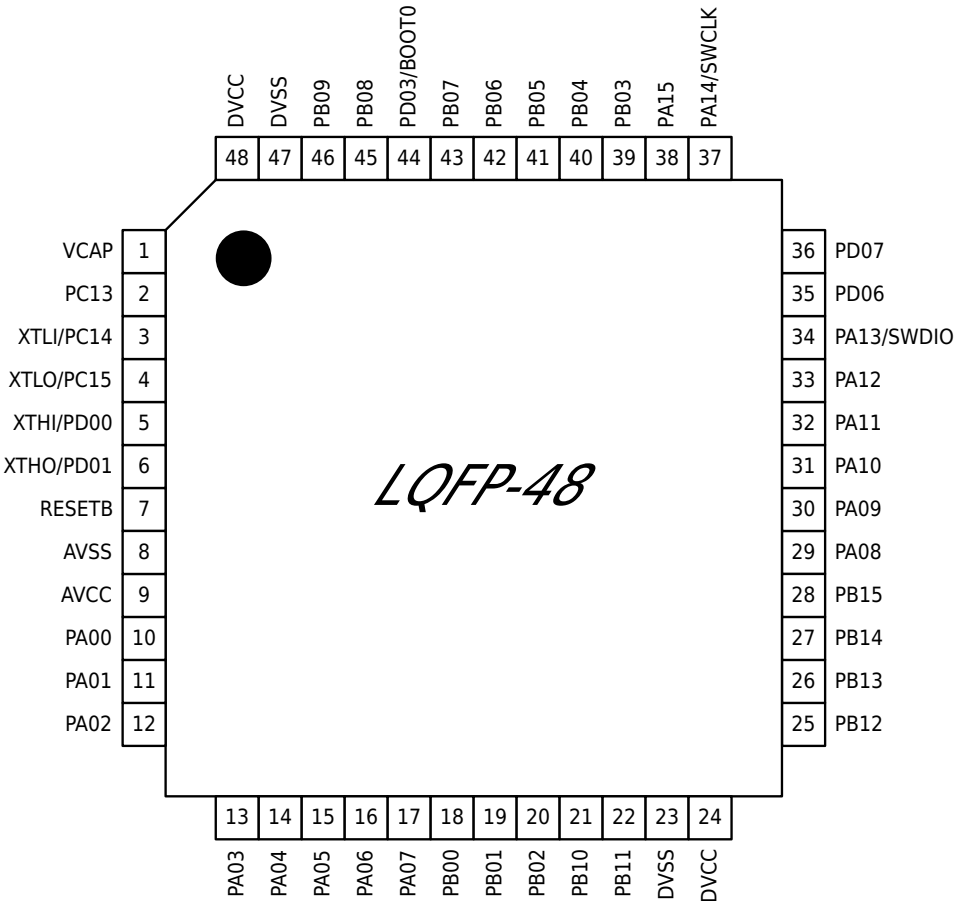
Encrypted embedded debugging solution, providing a full-featured real-time debugger.

3 Pin Definitions

3.1 Pinout

3.1.1 LQFP48 Package

HC32A052JATI-LQ48

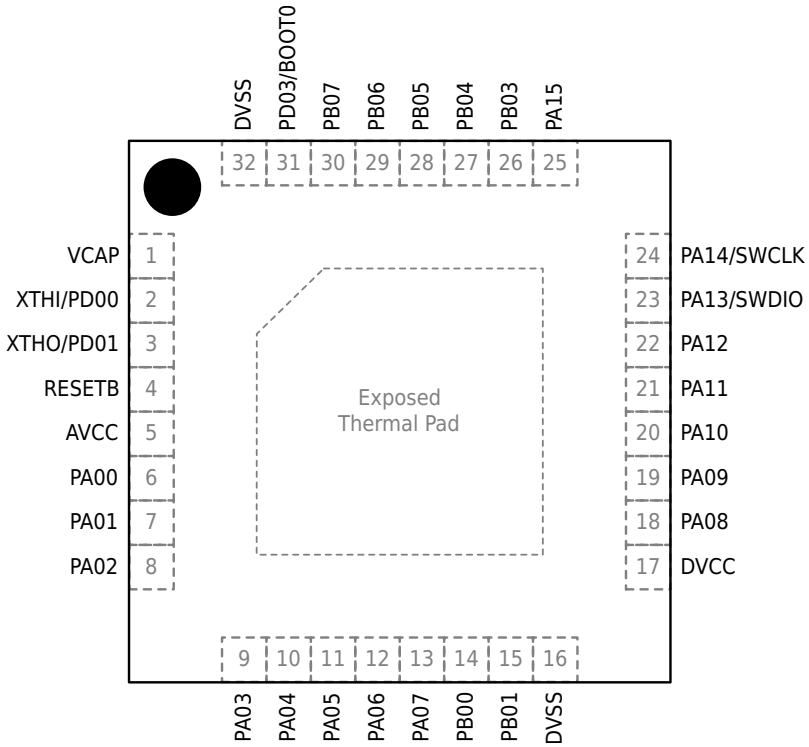


Note

- BOOT0 pin is used to control FLASH programming, see Module Signal Description.

3.1.2 QFN32 Package

HC32A052FAUI-QFN32TR



Note

- Exposed Thermal Pad needs to be connected to DVSS.
- For details on the IOs not brought out by this package, please refer to Pin Function Description.
- BOOT0 pin is used to control FLASH programming, see Module Signal Description.

3.2 Pin Function Description

LQFP48	QFN32	Name	Digital	Analog
1	1	VCAP	-	-
2	-	PC13	CTIM1_ETR RTC_1HZ ATIM3_CH1B CTIM0_TOG	LVD_IN1
3	-	PC14	CTIM1_CH0 CTIM0_TOGN LVD_OUT	XTLI
4	-	PC15	CTIM1_CH0	XTLO
5	2	PD00	I2C0_SDA CTRIM_ETRTOG USART1_TXD CTIM1_CH2 I2CSLV_SCL	XTHI
6	3	PD01	I2C0_SCL ATIM3_CH0B USART1_RXD CTIM1_CH3 I2CSLV_SDA	XTHO
7	4	RESETB	-	-
8	-	AVSS	-	-
9	5	AVCC	-	-
10	6	PA00	USART1_CTS LPUART1_TXD ATIM0_ETR VC0_OUT ATIM1_CHA ATIM3_ETR ATIM0_CHA	AIN0 VCx_INN0 VCx_INP0
11	7	PA01	USART1_RTS LPUART1_RXD ATIM0_CHB ATIM1_ETR ATIM1_CHB HCLK_OUT SPI1_MOSI	AIN1 VCx_INN1 VCx_INP1
12	8	PA02	USART1_TXD ATIM0_CHA VC1_OUT ATIM1_CHA ATIM2_CHA ATIM3_CH0A SPI1_MISO	AIN2 VCx_INN2 VCx_INP2
13	9	PA03	USART1_RXD ATIM0_GATE ATIM1_CHB ATIM2_CHB SPI1_NSS ATIM3_CH0B PCLK_OUT	AIN3 VCx_INN3 VCx_INP3

LQFP48	QFN32	Name	Digital	Analog
14	10	PA04	SPI0_NSS USART1_SCK CTIM1_CH0 ATIM2_ETR ATIM3_CH1A USART1_TXD I2CSLV_SCL	AIN4 VCx_INN4 VCx_INP4
15	11	PA05	SPI0_SCK ATIM0_ETR CTIM0_ETR ATIM0_CHA ATIM3_CH1B XTL_OUT XTH_OUT	AIN5 VCx_INN5 VCx_INP5
16	12	PA06	SPI0_MISO CTIM0_CH0 ATIM3_BK ATIM1_CHA VC0_OUT ATIM3_GATE LPUART0_CTS	AIN6
17	13	PA07	SPI0_MOSI CTIM0_CH1 HCLK_OUT ATIM3_CH2A ATIM2_CHA VC1_OUT CTIM1_TOG	AIN7
18	14	PB00	CTIM0_CH2 CTIM1_TOGN LPUART0_TXD ATIM3_CH2B RCH_OUT RCL_OUT PLL_OUT	AIN8 VCx_INN6 VCx_INP6
19	15	PB01	CTIM0_CH3 PCLK_OUT I2CSLV_SDA ATIM3_CH1B LPUART0_RTS LPTIM_TOGN USART0_SCK	AIN9/EXVREF VCx_INN7 VCx_INP7
20	-	PB02	LPTIM_TOG CTIM0_ETR LPUART1_TXD ATIM3_CH0B ATIM1_BK ATIM0_BK ATIM2_BK	AIN10 OP2_INN
21	-	PB10	I2C1_SCL SPI1_SCK ATIM1_CHA LPUART0_TXD ATIM3_CH2A LPUART1_RTS USART1_RTS	AIN11 OP2_INP

LQFP48	QFN32	Name	Digital	Analog
22	-	PB11	I2C1_SDA ATIM1_CHB LPUART0_RXD ATIM2_GATE ATIM3_CH1A LPUART1_CTS USART1_CTS	AIN12 OP2_OUT
23	16	DVSS	-	-
24	17	DVCC	-	-
25	-	PB12	SPI1_NSS ATIM3_BK LPUART0_TXD ATIM0_BK LPUART0_RTS ATIM3_CH0A	AIN13 VCx_INN8 VCx_INP8 OP1_INN
26	-	PB13	SPI1_SCK I2C1_SCL ATIM3_CH0B LPUART0_CTS ATIM1_CHA ATIM1_GATE	AIN14 OP1_INP
27	-	PB14	SPI1_MISO I2C1_SDA ATIM3_CH1B ATIM0_CHA ATIM3_CH2A LPUART0_RTS ATIM1_BK	AIN15 OP1_OUT
28	-	PB15	SPI1_MOSI ATIM3_CH2B ATIM0_CHB ATIM0_GATE RTC_1HZ CTIM0_TOG LPUART1_RXD	-
29	18	PA08	USART0_SCK ATIM3_CH0A USART0_TXD CAN_STBY ATIM1_GATE CTIM0_TOGN ATIM3_BK	-
30	19	PA09	USART0_TXD ATIM3_CH1A ATIM0_BK I2C0_SCL MCO_OUT HCLK_OUT I2CSLV_SCL	-
31	20	PA10	USART0_RXD ATIM3_CH2A ATIM2_BK I2C0_SDA ATIM2_GATE PCLK_OUT I2CSLV_SDA	-

LQFP48	QFN32	Name	Digital	Analog
32	21	PA11	USART0_CTS ATIM3_GATE I2C1_SCL CAN_TX VC0_OUT SPI0_MISO ATIM3_CH1B	-
33	22	PA12	USART0_RTS ATIM3_ETR I2C1_SDA CAN_RX VC1_OUT SPI0_MOSI CTIM1_ETR	-
34	23	PA13/SWDIO	USART1_SCK USART0_RXD LVD_OUT ATIM3_ETR RTC_1HZ CTIM1_CH1 CTRIM_ETRTOG	-
35	-	PD06	I2C1_SCL LPUART1_CTS USART0_CTS RTC_OUT ATIM3_BK CTIM1_CH2	-
36	-	PD07	I2C1_SDA LPUART1_RTS USART0_RTS RTC_TS ATIM3_ETR CTIM1_CH3	-
37	24	PA14/SWCLK	USART1_TXD USART0_TXD ATIM3_CH2A LVD_OUT RCH_OUT RCL_OUT PLL_OUT	-
38	25	PA15	SPI0_NSS USART1_RXD LPUART1_RTS ATIM0_ETR ATIM0_CHA ATIM3_CH1A CAN_STBY	-
39	26	PB03	SPI0_SCK ATIM0_CHB ATIM1_GATE ATIM3_CH0A LPTIM_GATE XTL_OUT XTH_OUT	-

LQFP48	QFN32	Name	Digital	Analog
40	27	PB04	SPI0_MISO CTIM0_CH0 ATIM2_BK USART0_CTS ATIM2_GATE ATIM3_CH0B LPTIM_ETR	VCx_INN9 VCx_INP9
41	28	PB05	SPI0_MOSI ATIM3_BK ATIM1_BK CTIM0_CH1 LPTIM_GATE CTRIM_ETRTOG USART0_RTS	VCx_INN10 VCx_INP10
42	29	PB06	I2C0_SCL USART0_TXD ATIM1_CHB ATIM0_CHA LPTIM_ETR ATIM3_CH0A LPTIM_TOG	-
43	30	PB07	I2C0_SDA USART0_RXD ATIM2_CHB LPUART1_CTS ATIM0_CHB LPTIM_TOGN ATIM3_ETR	LVD_IN3
44	31	PD03/BOOT0	-	-
45	-	PB08	I2C0_SCL ATIM1_CHA CAN_RX ATIM2_CHA ATIM0_GATE ATIM3_CH2A USART0_TXD	LVD_IN2
46	-	PB09	I2C0_SDA USART0_SCK SPI1_NSS ATIM2_CHA CAN_TX ATIM2_CHB USART0_RXD	-
47	32	DVSS	-	-
48	-	DVCC	-	-

The digital function of each pin is controlled by the PSEL bit field, as detailed in the following table.

Table 3-2 Port Digital Multiplexed Function

Name	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC13	CTIM1_ETR	RTC_1HZ	ATIM3_CH1B	CTIM0_TOG	-	-	-
PC14	CTIM1_CH0	CTIM0_TOGN	LVD_OUT	-	-	-	-
PC15	CTIM1_CH0	-	-	-	-	-	-
PD00	I2C0_SDA	CTRIM_ETRTOG	USART1_TXD	CTIM1_CH2	I2CSLV_SCL	-	-
PD01	I2C0_SCL	ATIM3_CH0B	USART1_RXD	CTIM1_CH3	I2CSLV_SDA	-	-
PA00	USART1_CTS	LPUART1_TXD	ATIM0_ETR	VC0_OUT	ATIM1_CHA	ATIM3_ETR	ATIM0_CHA
PA01	USART1_RTS	LPUART1_RXD	ATIM0_CHB	ATIM1_ETR	ATIM1_CHB	HCLK_OUT	SPI1_MOSI

Name	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA02	USART1_TXD	ATIM0_CHA	VC1_OUT	ATIM1_CHA	ATIM2_CHA	ATIM3_CH0A	SPI1_MISO
PA03	USART1_RXD	ATIM0_GATE	ATIM1_CHB	ATIM2_CHB	SPI1_NSS	ATIM3_CH0B	PCLK_OUT
PA04	SPI0_NSS	USART1_SCK	CTIM1_CH0	ATIM2_ETR	ATIM3_CH1A	USART1_TXD	I2CSLV_SCL
PA05	SPI0_SCK	ATIM0_ETR	CTIM0_ETR	ATIM0_CHA	ATIM3_CH1B	XTL_OUT	XTH_OUT
PA06	SPI0_MISO	CTIM0_CH0	ATIM3_BK	ATIM1_CHA	VC0_OUT	ATIM3_GATE	LPUART0_CTS
PA07	SPI0_MOSI	CTIM0_CH1	HCLK_OUT	ATIM3_CH2A	ATIM2_CHA	VC1_OUT	CTIM1_TOG
PB00	CTIM0_CH2	CTIM1_TOGN	LPUART0_TXD	ATIM3_CH2B	RCH_OUT	RCL_OUT	PLL_OUT
PB01	CTIM0_CH3	PCLK_OUT	I2CSLV_SDA	ATIM3_CH1B	LPUART0_RTS	LPTIM_TOGN	USART0_SCK
PB02	LPTIM_TOG	CTIM0_ETR	LPUART1_TXD	ATIM3_CH0B	ATIM1_BK	ATIM0_BK	ATIM2_BK
PB10	I2C1_SCL	SPI1_SCK	ATIM1_CHA	LPUART0_TXD	ATIM3_CH2A	LPUART1_RTS	USART1_RTS
PB11	I2C1_SDA	ATIM1_CHB	LPUART0_RXD	ATIM2_GATE	ATIM3_CH1A	LPUART1_CTS	USART1_CTS
PB12	SPI1_NSS	ATIM3_BK	LPUART0_TXD	ATIM0_BK	-	LPUART0_RTS	ATIM3_CH0A
PB13	SPI1_SCK	I2C1_SCL	ATIM3_CH0B	LPUART0_CTS	ATIM1_CHA	ATIM1_GATE	-
PB14	SPI1_MISO	I2C1_SDA	ATIM3_CH1B	ATIM0_CHA	ATIM3_CH2A	LPUART0_RTS	ATIM1_BK
PB15	SPI1_MOSI	ATIM3_CH2B	ATIM0_CHB	ATIM0_GATE	RTC_1HZ	CTIM0_TOG	LPUART1_RXD
PA08	USART0_SCK	ATIM3_CH0A	USART0_TXD	CAN_STBY	ATIM1_GATE	CTIM0_TOGN	ATIM3_BK
PA09	USART0_TXD	ATIM3_CH1A	ATIM0_BK	I2C0_SCL	MCO_OUT	HCLK_OUT	I2CSLV_SCL
PA10	USART0_RXD	ATIM3_CH2A	ATIM2_BK	I2C0_SDA	ATIM2_GATE	PCLK_OUT	I2CSLV_SDA
PA11	USART0_CTS	ATIM3_GATE	I2C1_SCL	CAN_TX	VC0_OUT	SPI0_MISO	ATIM3_CH1B
PA12	USART0_RTS	ATIM3_ETR	I2C1_SDA	CAN_RX	VC1_OUT	SPI0_MOSI	CTIM1_ETR
PA13	USART1_SCK	USART0_RXD	LVD_OUT	ATIM3_ETR	RTC_1HZ	CTIM1_CH1	CTRIM_ETRTOG
PD06	I2C1_SCL	LPUART1_CTS	USART0_CTS	RTC_OUT	ATIM3_BK	CTIM1_CH2	-
PD07	I2C1_SDA	LPUART1_RTS	USART0_RTS	RTC_TS	ATIM3_ETR	CTIM1_CH3	-
PA14	USART1_TXD	USART0_TXD	ATIM3_CH2A	LVD_OUT	RCH_OUT	RCL_OUT	PLL_OUT
PA15	SPI0_NSS	USART1_RXD	LPUART1_RTS	ATIM0_ETR	ATIM0_CHA	ATIM3_CH1A	CAN_STBY
PB03	SPI0_SCK	ATIM0_CHB	ATIM1_GATE	ATIM3_CH0A	LPTIM_GATE	XTL_OUT	XTH_OUT
PB04	SPI0_MISO	CTIM0_CH0	ATIM2_BK	USART0_CTS	ATIM2_GATE	ATIM3_CH0B	LPTIM_ETR
PB05	SPI0_MOSI	ATIM3_BK	ATIM1_BK	CTIM0_CH1	LPTIM_GATE	CTRIM_ETRTOG	USART0_RTS
PB06	I2C0_SCL	USART0_TXD	ATIM1_CHB	ATIM0_CHA	LPTIM_ETR	ATIM3_CH0A	LPTIM_TOG
PB07	I2C0_SDA	USART0_RXD	ATIM2_CHB	LPUART1_CTS	ATIM0_CHB	LPTIM_TOGN	ATIM3_ETR
PD03	-	-	-	-	-	-	-
PB08	I2C0_SCL	ATIM1_CHA	CAN_RX	ATIM2_CHA	ATIM0_GATE	ATIM3_CH2A	USART0_TXD
PB09	I2C0_SDA	USART0_SCK	SPI1_NSS	ATIM2_CHA	CAN_TX	ATIM2_CHB	USART0_RXD

3.3 Module Signal Description

Table 3-3 Module Signal Description

Modules	Pin Name	Description
Power supply	DVCC	Digital power supply
	AVCC	Analog power
	DVSS	Digital ground
	AVSS	Analog ground
	VCAP	LDO core power supply output (only for internal circuit use, external voltage stabilization capacitor is required)
ISP	BOOT0	When reset, the BOOT0 (PD03) pin is high level, the chip works in ISP programming mode, and Flash can be programmed through ISP protocol When reset, the BOOT0 (PD03) pin is low level, the chip works in user mode, the chip executes the program code in the Flash, and the Flash can be programmed through the SWD protocol

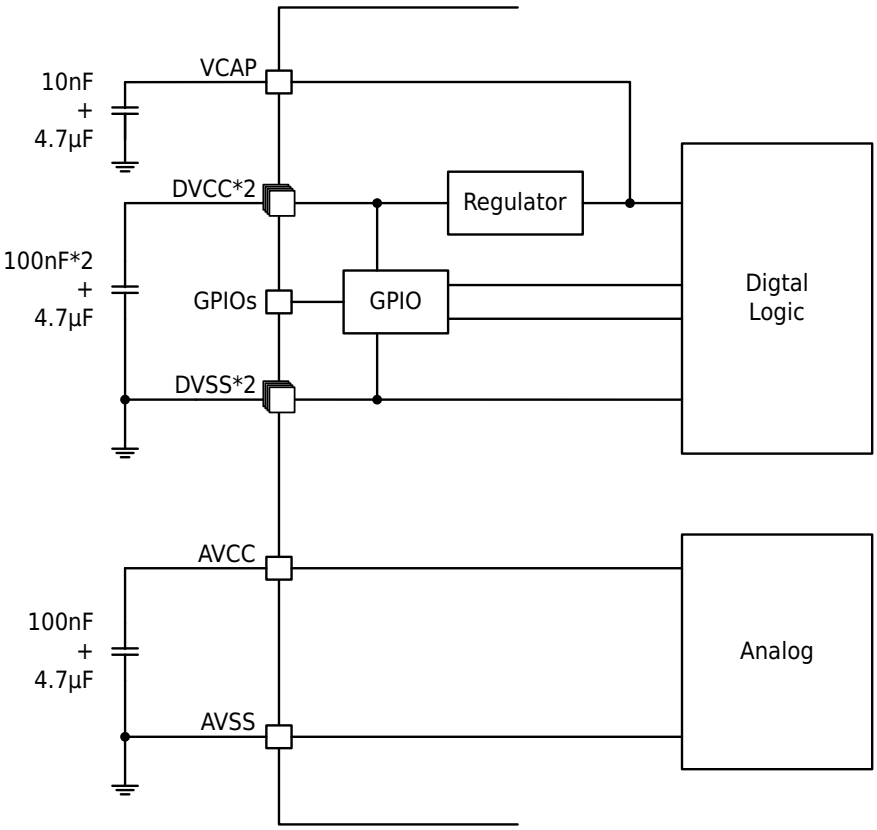
Modules	Pin Name	Description
ADC	AINx (x=0-15)	ADC input channel
	EXVREF	ADC external reference voltage
VC	VCx_INNy (x=0-1 y=0-10)	VCx negative terminal input
	VCx_INPy (x=0-1 y=0-10)	VCx positive terminal input
	VCx_OUT (x=0-1)	VCx compare output
LVD	LVD_INx (x=1-3)	Voltage detection input
	LVD_OUT	Voltage detection output
OPA	OPAx_INNx (x=0-1)	OPA negative terminal input
	OPAx_INPx (x=0-1)	OPA positive terminal input
	OPAx_OUTx (x=0-1)	OPA output
USART	USARTx_TXD (x=0-1)	USART data transmitter
	USARTx_RXD (x=0-1)	USART data receiver
	USARTx_CTS (x=0-1)	USART transmit hardware flow control
	USARTx_RTS (x=0-1)	USART receive hardware flow control
	USARTx_SCK	USART clock input and output
LPUART	LPUARTx_TXD (x=0-1)	LPUART data transmitter
	LPUARTx_RXD (x=0-1)	LPUART data receiver
	LPUARTx_CTS (x=0-1)	LPUART transmit hardware flow control
	LPUARTx_RTS (x=0-1)	LPUART receive hardware flow control
CTRIM	CTRIM_ETR/TOG	CTRIM external sync signal/inverted output signal
SPI	SPIx_MISO (x=0-1)	SPI master input and slave output data signal
	SPIx_MOSI (x=0-1)	SPI master output and slave input data signal
	SPIx_SCK (x=0-1)	SPI clock signal
	SPIx_NSS (x=0-1)	SPI chip selection
I2C	I2Cx_SDA (x=0-1)	I2C data signal
	I2Cx_SCL (x=0-1)	I2C clock signal
I2CSLV	I2CSLV_SDA	I2CSLV data signal
	I2CSLV_SCL	I2CSLV clock signal
CAN	CAN_TX	CAN transmit pin
	CAN_RX	CAN receive pin
	CAN_STBY	CAN transceiver standby control pin
RTC	RTC_1HZ	RTC 1Hz output
	RTC_OUT	RTC interrupt flag output
	RTC_TS	RTC timestamp input

Modules	Pin Name	Description
CTIM	CTIMx_CHy (x=0-1 y=0-3)	GTIM capture input comparison output/BTIM inverted output signal
	CTIMx_ETR (x=0-1)	External counting input signal of GTIM
	CTIMx_TOG/TOGN (x=0-1)	Inverted output signal of GTIM/BTIM
ATIM0-2	ATIMx_CHA (x=0-2)	Capture input and compare output A of ATIM
	ATIMx_CHB (x=0-2)	Capture input and compare output B of ATIM
	ATIMx_ETR (x=0-2)	External counting input signal of ATIM
	ATIMx_BK (x=0-2)	External brake input signal of ATIM
	ATIMx_GATE (x=0-2)	Gating signal of ATIM
ATIM3	ATIM3_CHyA (y=0-2)	Capture input and compare output A of ATIM3
	ATIM3_CHyB (y=0-2)	Capture input and compare output B of ATIM3
	ATIM3_ETR	External counting input signal of ATIM3
	ATIM3_BK	External brake input signal of ATIM3
	ATIM3_GATE	Gating signal of ATIM3
LPTIM	LPTIM_TOG	Inverted output signal of LPTimer
	LPTIM_TOGN	Toggle output inverted signal of LPTimer
	LPTIM_ETR	External count input signal of LPTimer
	LPTIM_GATE	Gating signal of LPTimer

Note

Most I/O ports are reset to analog input state, while the port states are maintained in Sleep/DeepSleep mode.

4 Typical Application Circuit Diagram



Notice

- AVCC and DVCC voltage must be the same.
- Each power supply requires a decoupling capacitor placed as close as possible to the respective power supply pin.

5 Electrical Specifications

5.1 Parameter Conditions

Unless otherwise specified, all voltages are based on VSS.

5.1.1 Minimum and Maximum Values

All Minimum Values and Maximum Values are measured under the worst conditions.

Data resulted from comprehensive evaluation, and/or guaranteed by design are indicated in the table footnotes, and they will not be tested on the production line.

5.1.2 Typical Values

Unless otherwise specified, typical data are given based on T_A=25℃ and VCC=3.3V. These data are only used for design guidance and have not been tested.

5.2 Absolute Maximum Ratings

If the load applied to the device exceeds the value given in the list of "Absolute Maximum Ratings", it may cause permanent damage to the device. The maximum load given here is for reference, which does not mean that the functional operation of the device is correct under this condition. Operation of the device under the condition of maximum value for a long time will affect the reliability of the device.

Table 5-1 Voltage Characteristics

Symbol	Parameters	Min	Max	Unit
VCC-VSS	External main supply voltage (including AVCC and DVCC)(1)	-0.3	5.5	V
V_{IN}	Input voltage on other pins(2)	VSS-0.3	VCC+0.3	V
|ΔVCCx|	Voltage difference between different power supply pins	-	50	mV
|VSSx-VSS|	Voltage difference between different grounding pins	-	50	mV
V_{ESD}(HBM)	Electrostatic discharge voltage (Human model)	Refer to absolute maximum electrical parameters		V

Note

1. All powers (DVCC, AVCC) and grounding (DVSS, AVSS) pins should always be connected to the power supply system within the external allowable range.
2. $I_{INJ(PIN)}$ should not exceed its limit, that is, ensure that V_{IN} does not exceed its maximum value. If V_{IN} cannot be guaranteed not to exceed its maximum value, it is also necessary to ensure that $I_{INJ(PIN)}$ does not exceed its maximum value externally. When V_{IN}>VCC, there is a forward injection current; When V_{IN}<VSS, there is a reverse injection current.

Table 5-2 Current Characteristics

Symbol	Parameters	Max(1)	Unit
I_{VCC}	Total current through DVCC/AVCC power line (supply current)(1)	100	mA
I_{VSS}	Total current through VSS ground wire (outflow current)(1)	100	mA

Symbol	Parameters	Max(1)	Unit
I_{IO}	Output sink current on any I/O and control pins	18	mA
	Output current on any I/O and control pins	-18	mA
$I_{INJ(PIN)}$(2)(3)	Injection current of RESETB pin	±5	mA
	Injection current of XTHI pin of XTH and XTLI pin of XTL	±5	mA
	Injection current of other pins(4)	±5	mA
$\sum I_{INJ(PIN)}$(2)	Total injection current on all I/O and control pin(4)	±25	mA

Note

1. All power supply (DVCC, AVCC) and grounding (DVSS, AVSS) pins should always be connected to the power supply system within the external allowable range.
2. $I_{INJ(PIN)}$ should not exceed its limit, that is, ensure that V_{IN} does not exceed its maximum value. If V_{IN} cannot be guaranteed not to exceed its maximum value, it is also necessary to ensure that $I_{INJ(PIN)}$ does not exceed its maximum value externally. When V_{IN}>VCC, there is a forward injection current; When V_{IN}<VSS, there is a reverse injection current.
3. The reverse injection current will interfere with the simulation performance of the device.
4. When several I/O ports have injection currents at the same time, the maximum value of $\sum I_{INJ(PIN)}$ is the sum of the instantaneous absolute values of the forward injection current and the reverse injection current. This result is based on the features of the maximum value of $\sum I_{INJ(PIN)}$ at four I/O ports of the device.

Table 5-3 Temperature Characteristics

Symbol	Parameters	Value	Unit
T_{STG}	Storage temperature range	-65-+150	℃
T_{Jmax}	Maximum Junction Temperature	125	℃

5.3 Operating Conditions

5.3.1 General Operating Conditions

Table 5-4 General Operating Conditions

Symbol	Parameters	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	64	MHz
f_{PCLK0}	Internal APB0 clock frequency	-	0	64	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	64	MHz
DVCC	Digital Operating Voltage	-	2.0	5.5	V
AVCC(1)	Analog Operating Voltage	Must be the same as DVCC(2)	2.0	5.5	V
T_A	Ambient temperature	Maximum power consumption	-40	105	℃
		Low power consumption	-40	125	℃
T_J	Junction Temperature Range	-	-40	125	℃

Note

1. When using an ADC, see ADC Electrical Specifications.
2. It is recommended to use the same power supply for DVCC and AVCC, allowing a maximum of 300mV difference between DVCC and AVCC during power-up and normal operation.

5.3.2 Working Conditions at Power-On and Power-Down

Table 5-5 Working Conditions at Power-On and Power-Down

Symbol	Parameters	Conditions	Min	Max	Unit
t_{Vcc}	VCC Rise Rate	-	1	∞	μs/V
t_{Vcc}	VCC Fall Rate	-	10	∞	μs/V

5.3.3 Embedded Reset and LVD Module Characteristics

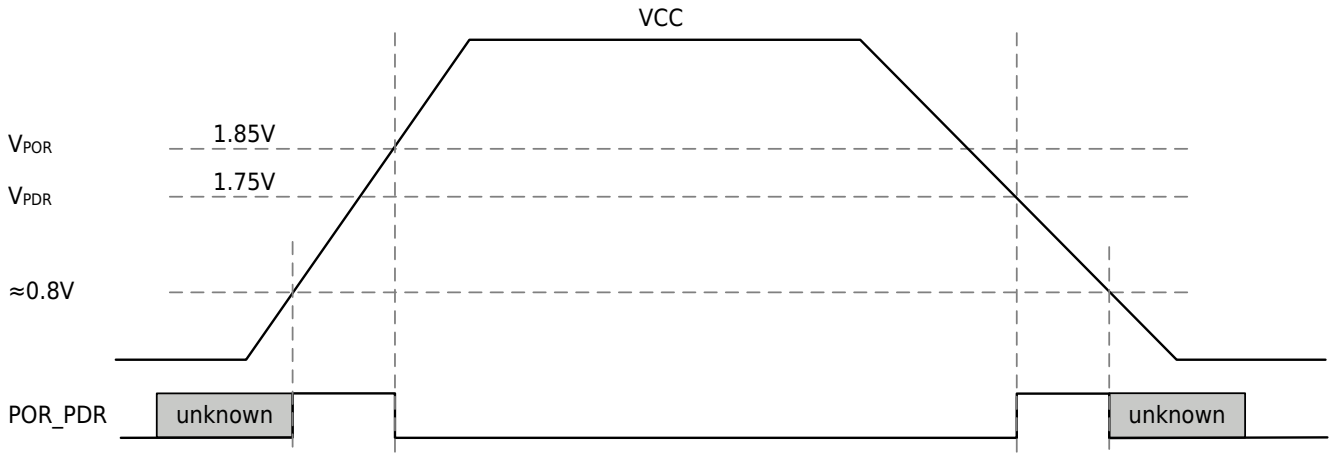


Figure 5-1 POR/Brown Out Schematic Diagram

Table 5-6 POR/Brown Out

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{POR}	POR release voltage (power on process)	-	-	1.85	-	V
V_{PDR}	PDR detection voltage (power down process)	-	-	1.75	-	V

Table 5-7 LVD module features

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{ex}	External input voltage range	-	0	-	VCC	V
V_{level}	Detection threshold	LVD_CR.VTDS=0b0000 LVD_CR.VTDS=0b0001 LVD_CR.VTDS=0b0010 LVD_CR.VTDS=0b0011 LVD_CR.VTDS=0b0100 LVD_CR.VTDS=0b0101 LVD_CR.VTDS=0b0110 LVD_CR.VTDS=0b0111	1.70 1.80 1.90 2.00 2.10 2.20 2.30 2.35	1.80 1.90 2.00 2.10 2.20 2.30 2.40 2.50	1.90 2.00 2.10 2.20 2.30 2.40 2.55 2.65	V

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{level}	Detection threshold	LVD_CR.VTDS=0b1000 LVD_CR.VTDS=0b1001 LVD_CR.VTDS=0b1010 LVD_CR.VTDS=0b1011 LVD_CR.VTDS=0b1100 LVD_CR.VTDS=0b1101 LVD_CR.VTDS=0b1110 LVD_CR.VTDS=0b1111	2.45 2.55 2.65 2.75 2.85 2.95 3.05 3.15	2.60 2.70 2.80 2.90 3.00 3.10 3.20 3.30	2.75 2.85 2.95 3.05 3.15 3.25 3.35 3.45	V
$T_{response}$	Response time	Choose to detect the GPIO pin voltage, VCC=3.3V, LVD_CR.VTDS= 0b1000, the detection voltage changes from (V_{level}+100mV) to (V_{level}-100mV), and the change slope is $2 \times 10^5 V/\mu s$	-	28	-	µs
T_{setup}	Settling time	Choose to detect the GPIO pin voltage, VCC=3.3V, LVD_CR.VTDS= 0b1000, the detection voltage is lower than V_{level} 100mV	-	50	-	µs
V_{hyste}	Hysteresis voltage	-	-	40	-	mV
T_{filter}	Filter time	LVD_CR.DEBOUNCETIME=0b000 LVD_CR.DEBOUNCETIME=0b001 LVD_CR.DEBOUNCETIME=0b010 LVD_CR.DEBOUNCETIME=0b011 LVD_CR.DEBOUNCETIME=0b100 LVD_CR.DEBOUNCETIME=0b101 LVD_CR.DEBOUNCETIME=0b110 LVD_CR.DEBOUNCETIME=0b111	-	7 14 28 112 450 1800 7200 28800	-	µs

5.3.4 Built-In Reference Voltage

Table 5-8 Built-In Reference Voltage Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{REF25}(2)	Internal 2.5V Reference Voltage	V_{CC}=3.3V T_A=25℃	2.475	2.5	2.525	V
V_{REF25}(1)(2)	Internal 2.5V Reference Voltage	V_{CC}=2.8-5.5V T_A=-40-105℃	2.45	2.5	2.55	V
V_{REF15}	Internal 1.5V reference voltage	V_{CC}=3.3V T_A=25℃	1.485	1.5	1.515	V
V_{REF15}(1)	Internal 1.5V reference voltage	V_{CC}=2.0-5.5V T_A=-40-105℃	1.47	1.5	1.53	V
T_{Coeff}(3)	Internal 2.5V 1.5V temperature coefficient	T_A=-40-105℃	-	-	120	ppm /℃

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$T_{stable(BGR)}$ (3)	BGR stable time	V_{CC}=3.3V T_A=25℃	-	60	-	us

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. The 2.5V range can only be selected when the power supply voltage exceeds 2.8V, otherwise it will cause system malfunction.
3. Guaranteed by design, not tested in production.

5.3.5 Supply Current Characteristics

Current consumption is a comprehensive index of multiple parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin flip rate, and the location of the program in memory and the executed code, etc.

The MCU is in the following conditions:

- All I/O pins are in input mode and connected to a static level-VCC or VSS (no load).
- All peripherals are turned off, unless otherwise specified.
- The access time of the flash memory is adjusted to the frequency f_{HCLK} (0 wait cycle for 0-24MHz, 1 wait cycle for 24-48MHz)
- When periphrals is used: f_{PCLK0}=f_{HCLK}, f_{PCLK1}=f_{HCLK}.

Table 5-9 Operating Current Characteristics

Symbol	Parameters	Conditions			Typ(1)(3)	Max(2)(3)	Unit
I_{DD} (Run in RAM)	All peripherals clock ON, Run while(1) in RAM	V_{CAP}=1.2V V_{CC}=3.3V T_A=2x℃	RCH clock source	3M	520	-	μA
				4M	590	-	
				6M	730	-	
				12M	1150	-	
			PLL RCH12M to xxM clock source	16M	2000	-	
				24M	2600	-	
				32M	3280	-	
				64M	5830	-	
	All peripherals clock OFF, Run while(1) in RAM	V_{CAP}=1.2V V_{CC}=3.3V T_A=2x℃	RCH clock source	3M	380	-	μA
				4M	400	-	
				6M	460	-	
				12M	610	-	
			PLL RCH12M to xxM clock source	16M	1280	-	
				24M	1520	-	
				32M	1820	-	
				64M	2920	-	
I_{DD} (Run CoreMark)	All peripherals clock OFF, Run CoreMark in Flash	V_{CAP}=1.2V V_{CC}=3.3V T_A=2x℃	RCH clock source	3M	763	-	μA
				4M	903	-	
				6M	1175	-	
				12M	1775	-	

Symbol	Parameters	Conditions			Typ(1)(3)	Max(2)(3)	Unit
			PLL RCH12M to xxM clock source	16M	2338	-	
				24M Flash Wait=1	2549	-	
				32M Flash Wait=1	2835	-	
				64M Flash Wait=2	4310	-	
I_{DD} (Run mode)	All peripherals clock ON, Run while(1) in Flash	V_{CAP}=1.2V V_{CC}=2.0-5.5 V T_A=-40-105 ℃	RCH clock source	3M	492	-	μA
				4M	557	-	
				6M	685	-	
				12M	1071	3600	
			PLL RCH12M to xxM clock source	16M	1894	-	
				24M Flash Wait=1	2445	5000	
				32M Flash Wait=1	3070	6400	
				64M Flash Wait=2	5425	9000	
	All peripherals clock OFF, Run while(1) in Flash	V_{CAP}=1.2V V_{CC}=2.0-5.5 V T_A=-40-105 ℃	RCH clock source	3M	356	-	μA
				4M	375	-	
				6M	414	-	
				12M	528	2900	
			PLL RCH12M to xxM clock source	16M	1171	-	
				24M Flash Wait=1	1366	4200	
				32M Flash Wait=1	1615	4800	
				64M Flash Wait=2	2518	5800	
I_{DD} (Sleep mode)	All peripherals clock ON	V_{CAP}=1.2V V_{CC}=2.0-5.5 V T_A=-40-105 ℃	RCH clock source	3M	460	-	μA
				4M	514	-	
				6M	621	-	
				12M	944	1600	
			PLL RCH12M to xxM clock source	16M	1725	-	
				24M Flash Wait=1	2191	3000	
				32M Flash Wait=1	2727	3600	
				64M Flash Wait=2	4741	6000	
	All peripherals clock OFF	V_{CAP}=1.2V V_{CC}=2.0-5.5 V T_A=-40-105 ℃	RCH clock source	3M	323	-	μA
				4M	332	-	
				6M	348	-	
				12M	398	1000	
			PLL RCH12M to xxM clock source	16M	998	-	
				24M Flash Wait=1	1106	1800	
				32M Flash Wait=1	1267	2000	
				64M Flash Wait=2	1824	2600	

Symbol	Parameters	Conditions			Typ(1)(3)	Max(2)(3)	Unit
I_{DD} (LP Run)	All peripherals clock ON, Run while(1) in Flash	V_{CAP}=1.2V V_{CC}=2.0-5.5 V T_A=-40-105 ℃	RCL clock source(4)	-	113	600	μA
			XTL clock source(4)	Driver=2	112	600	
	All peripherals clock OFF, Run while(1) in Flash		RCL clock source(4)	-	112	590	
			XTL clock source(4)	Driver=2	111	590	
I_{DD} (LP Sleep)	All peripherals clock ON,	V_{CAP}=1.2V V_{CC}=2.0-5.5 V T_A=-40-105 ℃	RCL clock source(4)	-	113	580	μA
			XTL clock source(4)	Driver=2	113	580	
	All peripherals clock OFF,		RCL clock source(4)	-	111	570	
			XTL clock source(4)	Driver=2	111	570	
I_{DD} (Deep-Sleep)	All peripherals clock OFF	V_{CAP}=1.2V V_{CC}=2.0-5.5 V T_A=-40-105 ℃	NO CLK	-	21	410	μA
	All peripherals clock OFF		RCL(4)	-	22	420	
	All peripherals clock OFF		XTL(4)	-	21	405	
	Other peripherals clock OFF		RCL(4)	WDT	22	430	
	Other peripherals clock OFF		RCL(4)	LVD	22	430	
	Other peripherals clock OFF		RCL(4)	WDT+LVD	22	430	

Note

1. If there are no other specified conditions, the value of the Typ is 25℃ & V_{CC}=3.3V measured.
2. If there are no other specified conditions, the value of Max is the maximum value in the range of V_{CC}=2.0-5.5V & Temperature=-40-105℃.
3. Resulted from comprehensive evaluation, not tested in production.
4. RCL and XTL clock testing uses a frequency of 32.768kHz.

5.3.6 Time to Wake-Up from Low-Power Mode

The wake-up time is measured during the wake-up phase of the RCH oscillator. The clock source used when waking up depends on the current operating mode:

- Sleep mode: clock source is RCH oscillator
- DeepSleep mode: clock source is RCH oscillator

Table 5-10 Low-Power Mode Wake-Up Time(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
T_{wu}	Sleep mode wake-up time	-	-	1.8	-	μs
	DeepSleep mode wake-up time	F_{RCH}=4MHz	-	13	-	μs
		F_{RCH}=6MHz	-	11	-	μs
		F_{RCH}=12MHz	-	9	-	μs

Note

1. Guaranteed by design, not tested in production.
2. The wake-up time is measured from the start of the wake-up event to the user program reading the first instruction.

5.3.7 External Clock Source Characteristics

5.3.7.1 External Input High-Speed Clock

Table 5-11 External Input High-Speed Clock Characteristics(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{XTH_ext}	User external clock frequency	-	8	-	24	MHz
V_{XTHH}	Input pin high level voltage	-	0.7VCC	-	VCC	V
V_{XTHL}	Input pin low level voltage	-	VSS	-	0.3VCC	V
$T_{r(XTH)}$	Risign time	-	-	-	20	ns
$T_{f(XTH)}$	Falling time	-	-	-	20	ns
$T_{w(XTH)}$	Enter high or low time	-	16	-	-	ns
$C_{in(XTH)}$	Input capacitance	-	-	5	-	pF
Duty	Duty cycle	-	40	-	60	%
I_L	Input leakage current	-	-	-	±1	μA

Note

1. Guaranteed by design, not tested in production.

5.3.7.2 External Input Low-Speed Clock

Table 5-12 External Input Low-Speed Clock Characteristics(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{XTL_ext}	User external clock frequency	-	0	32.768	1000	kHz
V_{XTLH}	Input pin high level voltage	-	0.7VCC	-	VCC	V

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{XTLL}	Input pin low level voltage	-	VSS	-	0.3VCC	V
$T_{r(XTL)}$	Rising time	-	-	-	50	ns
$T_{f(XTL)}$	Falling time	-	-	-	50	ns
$T_{w(XTL)}$	Enter high or low time	-	450	-	-	ns
$C_{in(XTL)}$	Input capacitance	-	-	5	-	pF
Duty	Duty cycle	-	30	-	70	%
I_L	Input leakage current	-	-	-	±1	μA

Note

1. Guaranteed by design, not tested in production.

5.3.7.3 External High-Speed Crystal XTH

The external high-speed crystal (XTH) can be generated using a 8-24MHz crystal/ceramic resonator oscillator. The information given in this section is based on the results obtained through comprehensive characteristic evaluation using the typical external components listed in the table below. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and settling time at startup. For detailed parameters (frequency, package, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Table 5-13 High-Speed External Clock XTH(1)(2)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
F_{CLK}	Oscillator frequency	-	8	-	24	MHz
ESR_{CLK}	Supported crystal oscillator ESR range	24MHz	-	-	60	Ω
		16MHz	-	-	80	
		8MHz	-	-	120	
C_{LX}(3)	Matching Capacitance	Configure as required by the crystal manufacturer.	4	12	20	pF
g_m	Transconductance	SYSCTRL_XTHCR[3:0]=0b1111	-	11	-	mS
		SYSCTRL_XTHCR[3:0]=0b1110	-	6.286	-	
		SYSCTRL_XTHCR[3:0]=0b1101	-	4.411	-	
		SYSCTRL_XTHCR[3:0]=0b1100	-	3.42	-	
		SYSCTRL_XTHCR[3:0]=0b1011	-	6.963	-	
		SYSCTRL_XTHCR[3:0]=0b1010	-	3.98	-	
		SYSCTRL_XTHCR[3:0]=0b1001	-	2.794	-	
		SYSCTRL_XTHCR[3:0]=0b1000	-	2.167	-	
		SYSCTRL_XTHCR[3:0]=0b0111	-	2.42	-	

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
g_m	Transcon-ductance	SYSCTRL_XTHCR[3:0]=0b0110	-	1.369	-	mS
		SYSCTRL_XTHCR[3:0]=0b0101	-	0.955	-	
		SYSCTRL_XTHCR[3:0]=0b0100	-	0.738	-	
		SYSCTRL_XTHCR[3:0]=0b0011	-	1.177	-	
		SYSCTRL_XTHCR[3:0]=0b0010	-	0.670	-	
		SYSCTRL_XTHCR[3:0]=0b0001	-	0.469	-	
		SYSCTRL_XTHCR[3:0]=0b0000	-	0.363	-	
Duty	Duty cycle	-	40	50	60	%
Idd(4)	Electro-rheograph	SYSCTRL_XTHCR[3:0]=0b1111	-	1200	-	μA
		SYSCTRL_XTHCR[3:0]=1110, Freq=24M, VCC=3.3V, Temp=25℃	-	750	-	μA
		SYSCTRL_XTHCR[3:0]=0b0000	-	150	-	μA
T_{start}(5)	Start time	24M, CL=16pF@ SYSCTRL_XTHCR[3:0]=0b1110	-	300	-	μs
		16 MHz, CL=16pF@ SYSCTRL_XTHCR[3:0]=0b1010	-	400	-	μs
		8MHz, CL=16pF@ SYSCTRL_XTHCR[3:0]=0b0110	-	1	-	ms

Note

1. The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.
2. Resulted from comprehensive evaluation, not tested in production.
3. C_{Lx} refers to the two pin matching capacitors C_{L1} and C_{L2} of the crystal. It is recommended to use high-quality ceramic capacitors, and select a crystal or resonator that meets the requirements. Usually C_{L1} and C_{L2} have the same parameters. When selecting C_{Lx}, one should take into account parameters such as the crystal oscillator's frequency and ESR, as well as the total parasitic capacitance to ground (C_P) from the PCB and MCU pins.

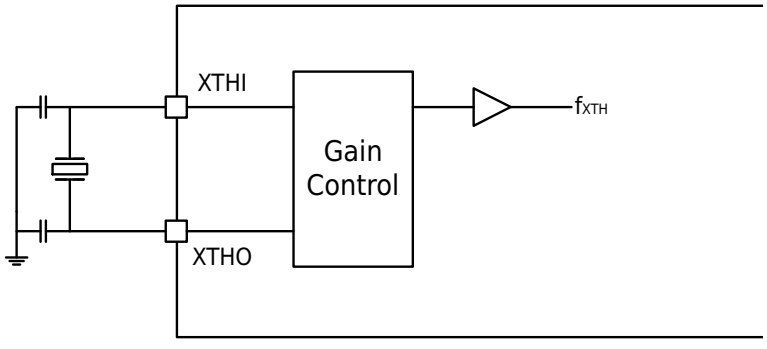
   The C_{Lx} is recommended to be configured in accordance with the requirements of the crystal manufacturer's technical manual.

   - If the crystal manufacturer gives *the value of the load capacitance* (C_L), the matching capacitance C_{Lx} = 2 * C_L - C_P.
   - If the crystal manufacturer gives *the value of the matching capacitance*, the matching capacitance C_{Lx} = matching capacitance value - C_P.

   In practical applications, if a larger C_{Lx} is selected, it is recommended to choose an appropriate current level setting.

   Example:

   - When the crystal manufacturer gives the load capacitance of the crystal as 8pF, considering the distributed capacitance between the PCB and MCU pins, it is recommended to choose a matching capacitor with a capacitance of 12pF.
   - When the crystal manufacturer gives the matching capacitance of the crystal as 12pF, considering the distributed capacitance between the PCB and MCU pins, it is recommended to choose a matching capacitor with a capacitance of 10pF or 8pF.
4. Current varies with frequency and drive capability selection.
5. T_{start} is the start-up time, which is the period of time from when the software enables XTH until a stable frequency output is obtained. This value is measured using a standard crystal resonator with the *SYSCTRL_XTHCR[5:4]= 0b10* setting. It may vary greatly depending on the crystal manufacturer and model.



5.3.7.4 External Low-Speed Crystal XTL

The external low-speed crystal (XTL) can be generated using a 32.768kHz crystal/ceramic resonator oscillator. The information given in this section is based on typical external components and the results obtained through comprehensive characteristic evaluation. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and settling time

at startup. For detailed parameters (frequency, package, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Table 5-14 External Low-Speed Crystal XTL Characteristics(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
F_{CLK}	Oscillator frequency	-	-	32.768	-	kHz
ESR_{CLK}	Supported crystal oscillator ESR range	-	-	-	60	kΩ
C_{Lx}(2)	Matching capacitance	Configure as required by the crystal manufacturer.	4	12	20	pF
DC_{ACLK}	Duty Cycle	-	30	50	70	%
I_{dd}(3)	electrorheograph	SYSCTRL_XTLCR[3:0]=0b1111	-	2000	-	nA
		SYSCTRL_XTLCR[3:0]=0b0010	-	400	-	
g_m	Transconductance	SYSCTRL_XTLCR[3:0]=0b1111	-	20.1	-	μS
		SYSCTRL_XTLCR[3:0]=0b1110	-	10.1	-	
		SYSCTRL_XTLCR[3:0]=0b1101	-	6.6	-	
		SYSCTRL_XTLCR[3:0]=0b1100	-	4.9	-	
		SYSCTRL_XTLCR[3:0]=0b1011	-	18.1	-	
		SYSCTRL_XTLCR[3:0]=0b1010	-	9.1	-	
		SYSCTRL_XTLCR[3:0]=0b1001	-	5.9	-	
		SYSCTRL_XTLCR[3:0]=0b1000	-	4.4	-	
		SYSCTRL_XTLCR[3:0]=0b0111	-	16.2	-	
		SYSCTRL_XTLCR[3:0]=0b0110	-	8.1	-	
		SYSCTRL_XTLCR[3:0]=0b0101	-	5.2	-	
		SYSCTRL_XTLCR[3:0]=0b0100	-	3.9	-	
		SYSCTRL_XTLCR[3:0]=0b0011	-	14.1	-	
		SYSCTRL_XTLCR[3:0]=0b0010	-	7.0	-	
		SYSCTRL_XTLCR[3:0]=0b0001	-	4.6	-	
		SYSCTRL_XTLCR[3:0]=0b0000	-	3.4	-	
T_{start}(4)	Start time	ESR=30kΩ C_L=12pF 40%-60% duty cycle has been reached	-	1000	-	ms

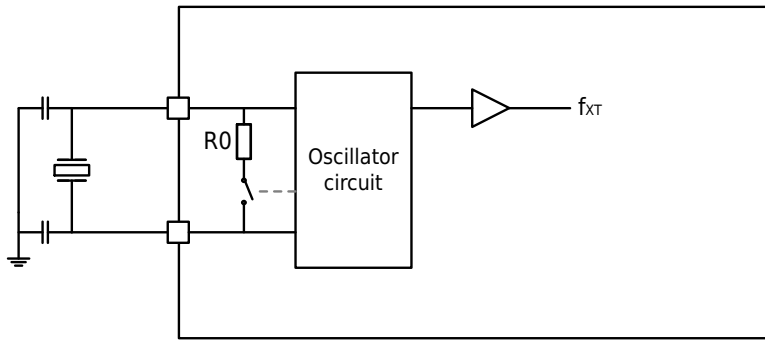
Note

1. Resulted from comprehensive evaluation, not tested in production.
2. C_{Lx} refers to the two pin matching capacitors C_{L1} and C_{L2} of the crystal. It is recommended to use high-quality ceramic capacitors, and select a crystal or resonator that meets the requirements. Usually C_{L1} and C_{L2} have the same parameters. When selecting C_{Lx}, one should take into account parameters such as the crystal oscillator's frequency and ESR, as well as the total parasitic capacitance to ground (C_P) from the PCB and MCU pins.

   The C_{Lx} is recommended to be configured in accordance with the requirements of the crystal manufacturer's technical manual.

   - If the crystal manufacturer gives *the value of the load capacitance* (C_L), the matching capacitance C_{Lx} = 2 * C_L - C_P.
   - If the crystal manufacturer gives *the value of the matching capacitance*, the matching capacitance C_{Lx} = matching capacitance value - C_P.

   In practical applications, if a larger C_{Lx} is selected, it is recommended to choose an appropriate current level setting.
3. Choose a high-quality oscillator with a small ESR value, and you can optimize the current consumption by adjusting the SYSCTRL_XTLCR[3:0] setting value. Current consumption is proportional to the transconductance (g_m) provided by the circuit.
4. T_{start} is the start-up time, which is the time from the software enabling XTL to start measuring until a stable 32768Hz oscillation is obtained. This value is measured using a standard crystal resonator with the settings *SYSCTRL_XTLCR[3:0]= 0b1001* and *SYSCTRL_XTLCR[5:4]=0b10*. It may vary greatly depending on the crystal manufacturer and model.



Note

- The feedback resistance R0 has been integrated in the chip.

5.3.8 Internal Clock Source Characteristics

5.3.8.1 RCH

Table 5-15 Internal High-Speed Clock RCH Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Dev(1)	RCH oscillator accuracy	User trimming step for given VCC and T_A conditions	-	0.25	-	%
		VCC=2.0-5.5V, T_A=-40-105℃	-1.5	0.25	1.5	%
F_{CLK}	Oscillator frequency	VCC=3.3V, T_A=25℃	11.94	12	12.06	MHz
Tsu(2)	Start time	-	-	5	-	us
I_{CLK}(2)	Electro-rheograph	F_{MCLK}=12MHz	-	120	-	μA
DC_{CLK}(1)	Duty cycle	-	45	50	55	%

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.

5.3.8.2 RCL

Table 5-16 Internal Low-Speed Clock RCL Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Dev(1)	RCL oscillator accuracy	User trimming step for given VCC and T_A conditions	-	0.5	-	%
		VCC=2.0-5.5V, T_A=-40-105℃	-2	-	2	%
		VCC=2.0-5.5V, T_A=-20-50℃	-1.5	-	1.5	%
F_{CLK}	Oscillator frequency	VCC=3.3V T_A=25℃	38.09	38.4	38.71	kHz
			32.50	32.768	33.03	kHz
T_{CLK}(2)	Start time	-	-	150	-	μs
DC_{CLK}(1)	Duty cycle	-	25	50	75	%
I_{CLK}(2)	Power consumption	-	-	0.9	-	μA

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.

5.3.9 PLL Characteristics

Table 5-17 PLL Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
F_{in}(1)	Input Clock	-	4	4	24(2)	MHz
$Duty_{in}$	Input clock duty cycle	-	40	-	60	%
F_{out}	Output frequency	-	12	-	64	MHz
T_{lock}(1)	Lock time	F_{in}=8M	-	40	80	μs
$Duty_{out}$(1)	Output duty cycle	-	48%	-	52%	-

Note

1. Guaranteed by design, not tested in production.
2. When the input frequency exceeds 12M, prescaler division must be configured. For detailed settings, refer to the corresponding "Reference Manual".

5.3.10 Flash Memory Characteristics

Table 5-18 Flash Memory Characteristics

Symbol	Parameters	Conditions		Min	Typ	Max	Unit
EC_{FLASH}	Program, Sector Erase times	T_A=-40 ℃-105℃	Data Storage Period (RET_{FLASH}): 10 years, T_A=85℃	-	100000	-	times
			Data Storage Period (RET_{FLASH}): 20 years, T_A=85℃	20000	-	-	times
T_{b_prog}	Programming time (bytes)	-		22	-	30	μs
T_{w_prog}	Programming time (words)	-		40	-	52	μs
T_{p_erase}	Page erase time	-		2	-	3	ms
T_{m_erase}	Full chip erase time	-		30	-	40	ms

5.3.11 ESD Characteristics

Using specific measurement methods, the chip is subjected to strength testing to determine its electrical sensitivity performance.

Table 5-19 ESD Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$VESD_{HBM}$(1)	ESD @ Human Body Mode	T_A=25℃, in line with ANSI/ESDA/JEDEC JS-001	-4	-	4	kV

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$VESD_{CDM}$(1)	ESD @ Charge Device Mode	T_A=25℃, in line with ANSI/ESDA/JEDEC JS-002	-1	-	1	kV
$I_{latchup}$(1)	Latch up current	T_A=105℃, in line with JESD78	-200	-	200	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

5.3.12 I/O Port Characteristics

5.3.12.1 Output Characteristics-Port

Table 5-20 Port Output Characteristics(1)

Symbol	Parameters	Conditions	Min	Max	Unit
V_{OH}	IO pin output high level (weak driver)	I_{IO}=4mA, VCC=3.3V	VCC-0.25	-	V
		I_{IO}=8mA, VCC=3.3V	VCC-0.60	-	V
V_{OL}	IO pin output low level (weak driver)	I_{IO}=4mA, VCC=3.3V	-	VSS+0.25	V
		I_{IO}=8mA, VCC=3.3V	-	VSS+0.70	V
V_{OHD}	IO pin output high level (strong driver)	I_{IO}=8mA, VCC=3.3V	VCC-0.25	-	V
		I_{IO}=18mA, VCC=3.3V	VCC-0.60	-	V
V_{OLD}	IO pin output low level (strong driver)	I_{IO}=8mA, VCC=3.3V	-	VSS+0.25	V
		I_{IO}=18mA, VCC=3.3V	-	VSS+0.60	V

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. The device's I_{IO} current must always comply with the absolute maximum ratings specified in Current Characteristics, and the sum of I_{IO} (I_{OH} and I_{OL} of I/O ports) must not exceed I_{Vcc}.

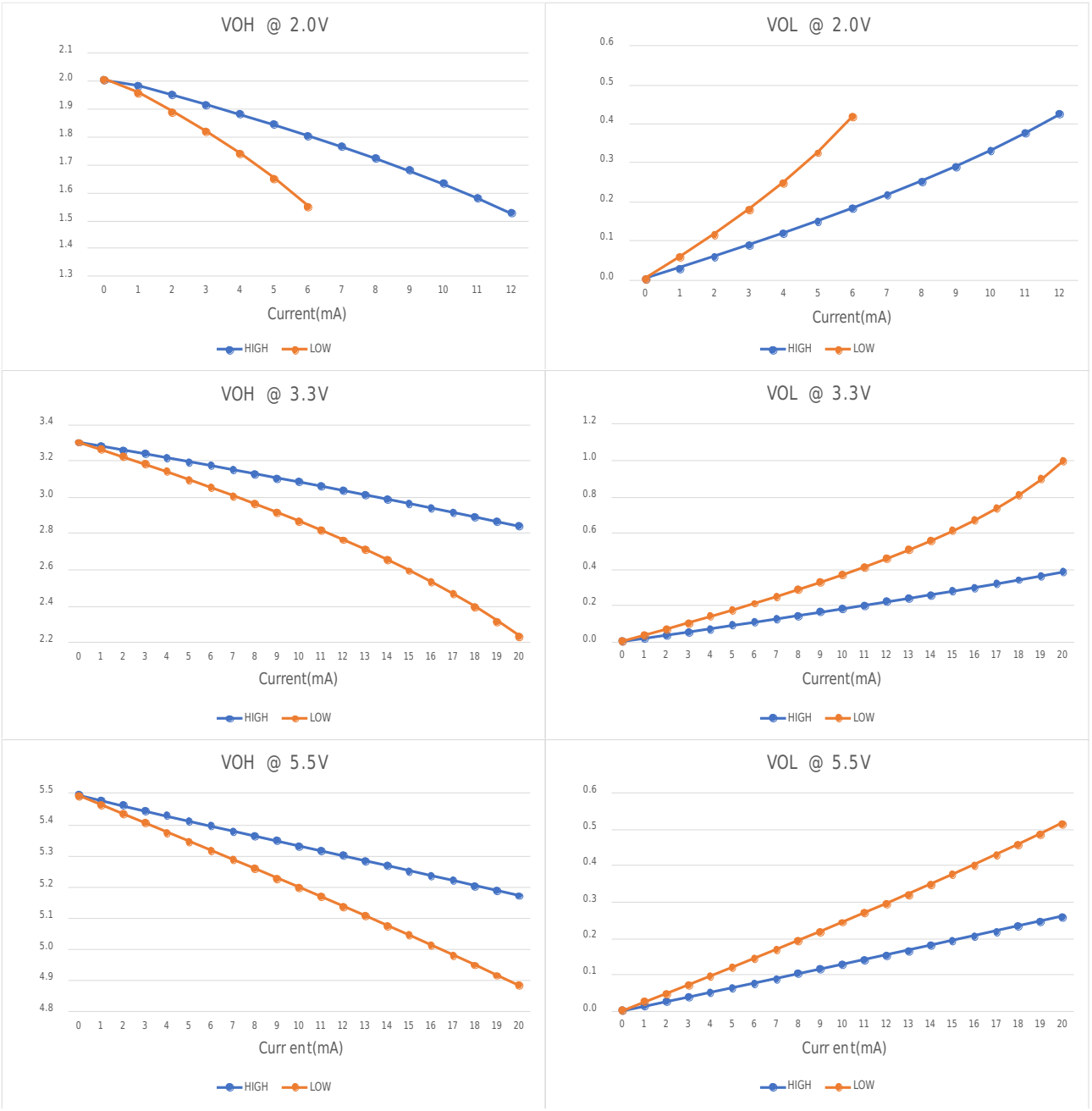


Figure 5-4 Output Port VOH/VOL Measured Curve (Typical Value)

5.3.12.2 Input Characteristics-PA/PB/PC/PD Port

Table 5-21 PA/PB/PC/PD Port Input Characteristics(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high-level voltage	VCC=2.0V	0.7VCC	-	-	V
		VCC=3.3V	0.7VCC	-	-	V
		VCC=5.5V	0.7VCC	-	-	V
V_{IL}	Input low-level voltage	VCC=2.0V	-	-	0.3VCC	V
		VCC=3.3V	-	-	0.3VCC	V
		VCC=5.5V	-	-	0.3VCC	V

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{hys}	Schmitt trigger input voltage hysteresis(V_{IH}-V_{IL})	VCC=2.0V	-	0.14	-	V
		VCC=3.3V	-	0.22	-	V
		VCC=5.5V	-	0.34	-	V
$R_{pullhigh}$	Weak pull-up equivalent resistance	Weak pull-up enable VCC=3.3V	-	55	-	kΩ
$R_{pulllow}$	Weak pull-down equivalent resistance	Weak pull-down enable VCC=3.3V	-	55	-	kΩ
C_{input}	Input equivalent capacitance	-	-	5	10	pF

Note

1. Resulted from comprehensive evaluation, not tested in production.

5.3.12.3 Port External Input Sampling Requirements-Timer Gate/Timer Clock

Table 5-22 Timer Gate/Timer Clock External Input Sampling Requirements(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$t_{(cap)}$	Timer capture timing	Timer capture pulse width	-	0.5	-	μs
$t_{(clk)}$	Timer clock frequency applied to pin	Timer external clock input f_{HCLK}=4MHz	-	-	PCLK/2	MHz

Note

1. Resulted from comprehensive evaluation, not tested in production.

5.3.12.4 Port Leakage Characteristics- PA/PB/PC/PD Port

Table 5-23 PA/PB/PC/PD Port Leakage Characteristics(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$I_{lkg(Px.y)}$	Leakage current	$V_{(Px.y)}$(2)(3)	-	±50	-	nA

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. The port leakage is based on the corresponding port being connected to VSS or VCC.
3. The port must be configured as an input port.

5.3.13 RESETB Pin Characteristics

The RESETB pin input driver uses CMOS technology, which is connected with a pull-up resistor that cannot be disconnected.

Table 5-24 RESETB Pin Characteristics(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{IL(RESETB)}$	Input low-level voltage	-	-0.3	-	0.3VCC	V
$V_{IH(RESETB)}$	Input high-level voltage	-	0.7VCC	-	VCC+0.3	V
$V_{hys(RESETB)}$	Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistance	$V_{IN}=V_{SS}$	-	55	-	kΩ
$T_{F(RESETB)}$	Filtered input pulse	-	-	-	2	μs
$T_{NF(RESETB)}$	Non-filtered input pulse	-	10	-	-	μs

Note

1. Guaranteed by design, not tested in production.

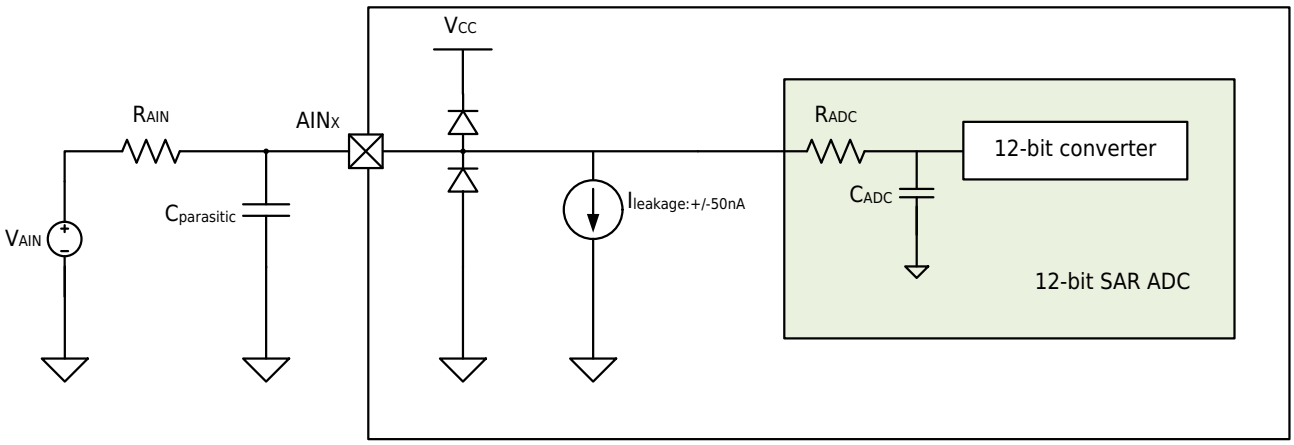
5.3.14 ADC Characteristics

Table 5-25 ADC Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{ADCIN}	Input voltage range	-	0	-	V_{REF+}	V
V_{REF+}(1)	Positive reference voltage	-	1.5	-	AVCC	V
V_{REF-}	Negative reference voltage	-	-	AVSS	-	V
$DEV_{AVCC/3}$	Accuracy of AVCC/3		-	±3	-	%
V_{INBUF}(1)	Input voltage range of the input buffer within which the accuracy is guaranteed	(AVCC-0.1V)<V_{REF+}	0.1	-	AVCC-0.1	V
		(AVCC-0.1V)≥V_{REF+}	0.1	-	V_{REF+}	
I_{ADC1}	Active current including reference generator and buffer	200ksps	-	2.0	-	mA
I_{ADC2}	Active current including reference generator and buffer	1Msps	-	1.0	-	
C_{ADCIN}(1)	ADC input capacitance	-	-	19	-	pF
R_{ADC}(1)	ADC sampling switch impedance	-	-	1.2	-	kΩ
R_{AIN}(1)(2)	ADC external input resistor	-	-	-	100	kΩ
f_{ADCCLK}	ADC clock Frequency	-	-	-	16	MHz

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$T_{ADCSTART}$(1)	Startup time of reference generator and ADC core	-	-	20	-	μs
T_S	Sampling time	-	4	-	10	1/f_{ADCCLK}
$T_{ADCCONV}$	Total conversion time (including sampling time)	-	-	T_S+12	-	
ENOB(1)	Effective bits	1Msps@VCC≥2.7V 500ksps@VCC≥2.4V 200ksps@VCC≥2.0V REF=EXVREF	-	10.7	-	bits
		1Msps@VCC≥2.7V 500ksps@VCC≥2.4V 200ksps@VCC≥2.0V REF=VCC	-	10.8	-	bits
		200ksps@VCC≥2.0V REF=internal 1.5V	-	10.0	-	bits
		200ksps@VCC≥2.8V REF=internal 2.5V	-	10.2	-	bits
SNR(1)	Signal to noise ratio	1Msps@VCC≥2.7V 500ksps@VCC≥2.4V 200ksps@VCC≥2.0V REF=EXVREF	-	70.0	-	dB
		1Msps@VCC≥2.7V 500ksps@VCC≥2.4V 200ksps@VCC≥2.0V REF=VCC	-	70.3	-	dB
		200ksps@VCC≥2.0V REF=internal 1.5V	-	61.8	-	dB
		200ksps@VCC≥2.8V REF=internal 2.5V	-	64.5	-	dB
DNL(1)	Differential non-linearity	200ksps, VREF=EXVREF/AVCC	-1	-0.9/+1.2	+2.5	LSB
INL(1)	Integral non-linearity	200ksps, VREF=EXVREF/AVCC	-4.5	-2.1/+1.6	+3	LSB
E_o(1)	Offset error	VREF=EXVREF/AVCC	-	-3/+3	-	LSB
E_g(1)	Gain error	VREF=EXVREF/AVCC	-	-3/+3	-	LSB
E_T(1)	Total unadjusted error	VREF=EXVREF/AVCC	-	-5/+5	-	LSB

1. Guaranteed by design, not tested in production.
2. The typical application of ADC is shown in the figure below:



Under the condition of 0.5LSB sampling error accuracy requirement, the calculation formula of external input impedance is as follows:

$$R_{AIN} \leq \frac{T_S}{C_{ADC} *(N+1) * \ln (2)} - R_{ADC} = \frac{M}{f_{ADCCLK} * C_{ADC} *(N+1) * \ln (2)} - R_{ADC}$$

Where T_s is the sampling time, N is the ADC bit number 12, f_{ADCCLK} is the ADC clock frequency, and M is the number of sampling cycles (the sampling time occupies M ADC clock cycles).

Register ADC_CR0[3:1] can set the relationship between f_{ADCCLK} and PCLK frequency, as shown in the following table:

Table 5-26 ADC Clock Frequency f_{ADCCLK} and PCLK Frequency Division Ratio Relationship

ADC_CR0[3:1]	f_{PCLK}/f_{ADCCLK}
0b000	2
0b001	4
0b010	6
0b011	8
0b100	10
0b101	12
0b110	14
0b111	1

Register ADC_CR0[13:12] can set the number of sampling periods M, as shown in the following table:

Table 5-27 ADC Sampling Period Number M

ADC_CR0[13:12]	M
0b00	4
0b01	6
0b10	9
0b11	10

The table below shows the relationship between ADC minimum sampling time T_S and external resistor R_{AIN} under typical operating conditions (with 0.5LSB sampling error). For other special external input impedance values, the corresponding minimum sampling time requirements can also be calculated through the external input impedance calculation formula given above.

Table 5-28 Relationship Between ADC Minimum Sampling Time and External Resistance R_{AIN}

R_{AIN} (Ω)	Minimum Sampling Time T_S (ns)
10	218
47	224
68	228
100	234
150	243
220	255
330	275
470	301
680	338
1000	396
1500	486
2200	612
3300	811
4700	1063
6800	1441
10000	2018
15000	2919

For the above typical applications, you should pay attention to:

- Minimize parasitic capacitance $C_{parasitic}$ at the ADC input port AIN.
- In addition to consider R_{AIN} value, if the internal resistance of signal source V_{AIN} is large, it also needs to be considered.

5.3.15 Temperature Sensor Characteristics

When the measurement channel of the ADC selects the output voltage of the temperature sensor, the current chip temperature can be calculated through the output result of the ADC and the calibration value stored in the Flash memory.

Table 5-29 Temperature Sensor Parameters

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Temp	Temp Sensor working environment	-	-40	-	105	℃
Offset	Calculated Temp offset	-	-	±5	-	℃

5.3.16 VC Characteristics

Table 5-30 VC Characteristics

Symbol	Parameters	Conditions		Min	Typ	Max	Unit
V_{in}	Input voltage range	-		0	-	5.5	V
V_{incom}	Input common mode range	-		0.2	-	VCC-0.2	V
V_{offset}	Input offset	Room temperature 25℃, 3.3V	VCx_CR0.BIAS=0b00	-	±20	-	mV
			VCx_CR0.BIAS=0b01	-	±20	-	
			VCx_CR0.BIAS=0b10	-	±15	-	
			VCx_CR0.BIAS=0b11	-	±10	-	
I_{comp}	Comparator's current	VCx_CR0.BIAS=0b00 VCx_CR0.BIAS=0b01 VCx_CR0.BIAS=0b10 VCx_CR0.BIAS=0b11		-	1 4 18 36	-	μA
$T_{response}$	Comparator's response time when one input cross another	VCx_CR0.BIAS=0b00 VCx_CR0.BIAS=0b01 VCx_CR0.BIAS=0b10 VCx_CR0.BIAS=0b11		-	20 5 1 0.2	-	μs
T_{setup}	Comparator's setup time when ENABLE. Input signals unchanged.	-		-	1	-	μs
$V_{hysteresis}$	Comparator's hysteresis voltage	VCx_CR0.HYS=0b00 VCx_CR0.HYS=0b01 VCx_CR0.HYS=0b10 VCx_CR0.HYS=0b11		-	0 10 20 30	-	mV
R_{in}	Equivalent input resistance of signal at positive input	-		-	-	350	Ω
V_{off_DAC}	Comparator's inner DAC's offset	VCx_CR1.NSEL=0b1011		-	±40	-	mV
T_{warmup}	From main bandgap enable to 1.2V BGR reference, Temp sensor voltage, ADC internal 1.5V/2.5V reference stable	-		-	60	-	μs
T_{filter}	Digital filter time (When filter clock is RC150K)	VCx_CR1.FLTTIME=0b000		-	7	-	μs

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
T_{filter}	Digital filter time (When filter clock is RC150K)	VCx_CR1.FLTTIME=0b001	-	14	-	μs
		VCx_CR1.FLTTIME=0b010	-	28	-	μs
		VCx_CR1.FLTTIME=0b011	-	112	-	μs
		VCx_CR1.FLTTIME=0b100	-	450	-	μs
		VCx_CR1.FLTTIME=0b101	-	1800	-	μs
		VCx_CR1.FLTTIME=0b110	-	7200	-	μs
		VCx_CR1.FLTTIME=0b111	-	28800	-	μs

5.3.17 OPA Characteristics

Table 5-31 OPA Characteristics(3)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{in}	Input voltage	-	0.2	-	AVCC-0.2	V
V_o(1)	The output voltage	-	0.2	-	AVCC-0.2	V
I_o(1)	Output current	-	-	-	0.3	mA
RL(1)	Load resistance	-	5	-	-	kΩ
T_{start}(1)(2)	Initialization time	-	-	3	-	μs
V_{os}	Input offset voltage	V_{in}=AVCC/2, V_o=AVCC/2, RL=5kΩ, Rs=50Ω, AutoZero function off	-	±3.5	-	mV
		V_{in}=AVCC/2, V_o=AVCC/2, RL=5kΩ, Rs=50Ω, AutoZero function on, after calibration	-	±1.5	-	mV
UGBW(1)	Unity gain bandwidth	RL=5kΩ	-	10	-	MHz
SR(1)	Slew rate	RL=5kΩ	-	5.5	-	V/μs

Note

1. Guaranteed by design, not tested in production.
2. Need to set ADC_BGR[0]=0b1 at the same time.
3. AVCC=2.0V-5.5V, AVSS=0V, T_A=-40℃-105℃.

5.3.18 TIM Timer Characteristics

For details on the features of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), see the table below.

Table 5-32 Advanced Timer (ATIM) Characteristics(1)

Symbol	Parameters	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	-	1	-	t_{TIMCLK}
		f_{TIMCLK}=64MHz	15.6	-	ns
f_{ext}	External clock frequency	f_{TIMCLK}=64MHz	0	32	MHz
Res_{Tim}	Timer resolution	Mode 0 free counting	-	32	Bit
		-	-	16	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter	-	1	65536	t_{TIMCLK}
	When the internal clock is selected, the 32-bit counter	-	1	4294967296	t_{TIMCLK}

Note

1. Guaranteed by design, not tested in production.

Table 5-33 Composite Timer (CTIM) Characteristics(1)

Symbol	Parameters	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	-	1	-	t_{TIMCLK}
		f_{TIMCLK}=64MHz	15.6	-	ns
f_{ext}	External clock frequency	f_{TIMCLK}=64MHz	0	32	MHz
Res_{Tim}	Timer resolution	-	-	16	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter	-	1	65536	t_{TIMCLK}

Note

1. Guaranteed by design, not tested in production.

Table 5-34 Low-Power Timer Characteristics(1)

Symbol	Parameters	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	-	1	-	t_{TIMCLK}
		f_{TIMCLK}=64MHz	15.6	-	ns
f_{ext}	External clock frequency	f_{TIMCLK}=64MHz	0	32	MHz
Res_{Tim}	Timer resolution	-	-	16	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter	-	1	65536	t_{TIMCLK}

Note

1. Guaranteed by design, not tested in production.

Table 5-35 IWDT Characteristics(1)

Symbol	Parameters	Conditions	Min	Max	Unit
t_{res}	IWDT overflow time	f_{WDTCLK}=32kHz	0.125	65000	ms

Note

1. Guaranteed by design, not tested in production.

5.3.19 Communication Interface

5.3.19.1 I2C Characteristics

I2C interface features are as follows:

Table 5-36 I2C Interface Characteristics(1)

Symbol	Parameters	Standard Mode (100k)		Fast Mode (400k)		High-Speed Mode (1M)		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCLL}	SCL clock low time	4.7	-	1.25	-	0.5	-	µs
t_{SCLH}	SCL clock high time	4.0	-	0.6	-	0.26	-	µs
$t_{SU.SDA}$	SDA establishment time	250	-	100	-	50	-	ns
$t_{HD.SDA}$	SDA hold time	0	-	0	-	0	-	µs
$t_{HD.STA}$	Start condition hold time	2.5	-	0.625	-	0.25	-	µs
$t_{SU.STA}$	Repeated start condition establishment time	2.5	-	0.6	-	0.25	-	µs
$t_{SU.STO}$	Stop condition setup time	0.25	-	0.25	-	0.25	-	µs
t_{BUF}	Bus idle (stop condition to start condition)	4.7	-	1.3	-	0.5	-	µs

Note

1. Guaranteed by design, not tested in production.

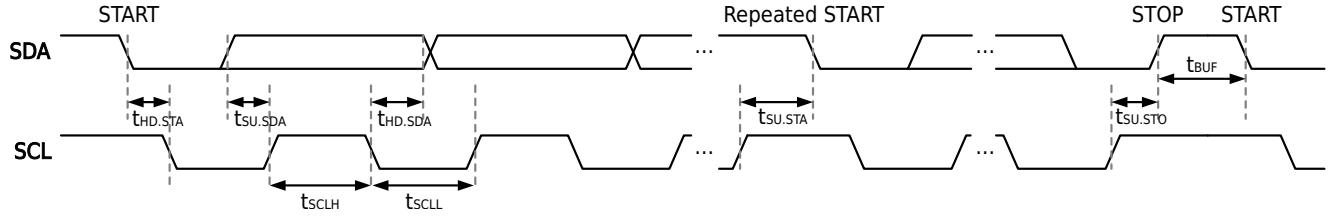


Figure 5-6 I2C Interface Timing

5.3.19.2 SPI Characteristics

Table 5-37 SPI Interface Characteristics[1][2]

Symbol	Parameters	Conditions	Min	Max	Unit
$t_{c(SCK)}$	Serial clock period[3]	Master transmit mode f_{PCLK}=60MHz	33.3	-	ns
		Master receiving mode (Master delayed sampling disabled) f_{PCLK}=60MHz	133	-	ns
		Master receiving mode (Master delayed sampling enabled) f_{PCLK}=60MHz	66.6	-	ns
		Slave transmit mode (Master delayed sampling disabled) f_{PCLK}=60MHz	133	-	ns
		Slave transmit mode (Master delayed sampling enabled) f_{PCLK}=60MHz	66.6	-	ns
		Slave receiving mode f_{PCLK}=60MHz	66.6	-	ns
$t_{w(SCKH)}$	High level time of serial clock	Master mode	$0.45\times t_{c(SCK)}$	-	ns
		Slave mode	$0.45\times t_{c(SCK)}$	-	ns
$t_{w(SCKL)}$	Low level time of serial clock	Master mode	$0.45\times t_{c(SCK)}$	-	ns
		Slave mode	$0.45\times t_{c(SCK)}$	-	ns
$t_{su(SSN)}$	Setup time selected by slave	Slave Mode	$0.45\times t_{c(SCK)}$	-	ns
$t_{h(SSN)}$	Hold time selected by slave	Slave Mode	$0.45\times t_{c(SCK)}$	-	ns
$t_{v(MO)}$	Effective time of master data output	-	-	3	ns
$t_{h(MO)}$	Hold time of master data output	-	0	-	ns
$t_{v(SO)}$	Effective time of slave data output	-	-	$20+1.5\times T_{PCLK}$	ns
$t_{h(SO)}$	Hold time of slave data output	-	$14+0.5\times T_{PCLK}$	-	ns
$t_{su(MI)}$	Setup time of master data input	-	20	-	ns
$t_{h(MI)}$	Hold time of master data input	-	2	-	ns

Symbol	Parameters	Conditions	Min	Max	Unit
$t_{su(SI)}$	Setup time of slave data input	-	0	-	ns
$t_{h(SI)}$	Hold time of slave data input	-	$2+1.5\times T_{PCLK}$	-	ns

Note

1. Guaranteed by design, not tested in production.
2. The data is provided under the condition of V_{CC}=3.0V.
3. The maximum frequency division factor of the master mode is PCLK/2, and the The maximum frequency division factor of slave mode is PCLK/4.

The waveform and timing parameters of the SPI interface signal are as follows:

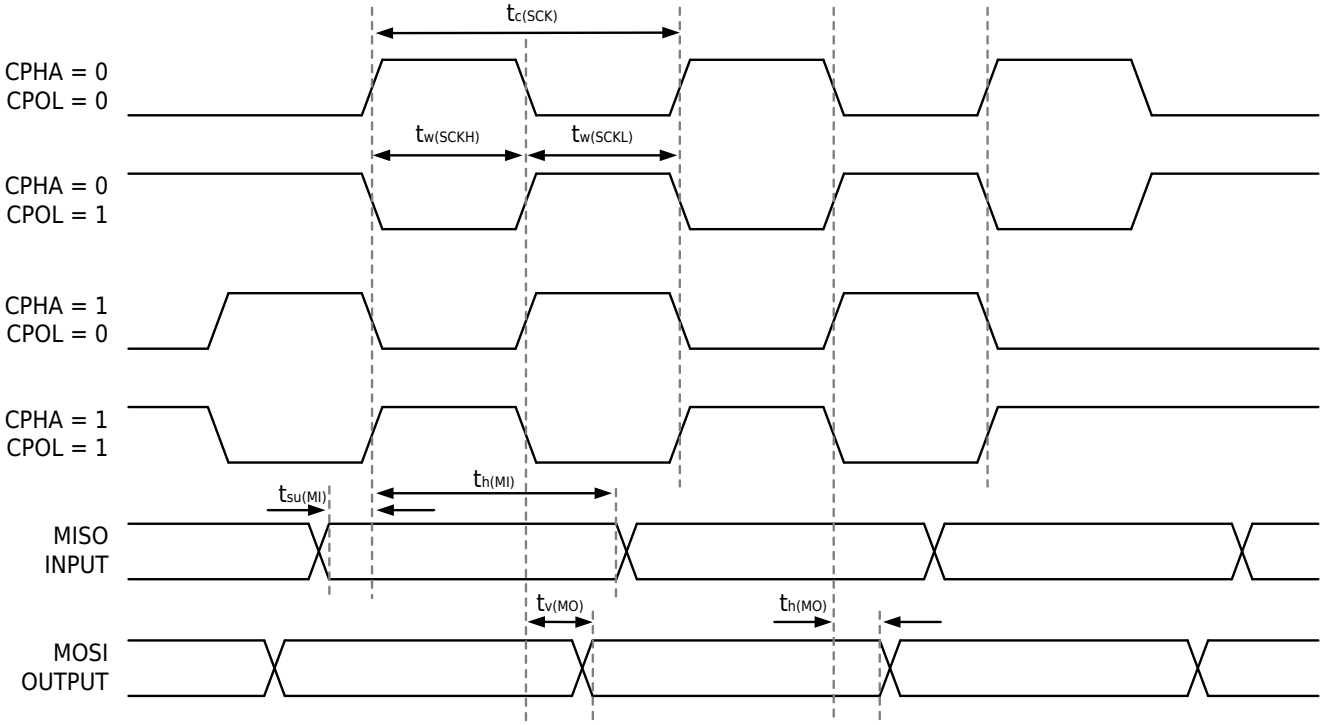


Figure 5-7 SPI Timing Diagram (Master Mode)

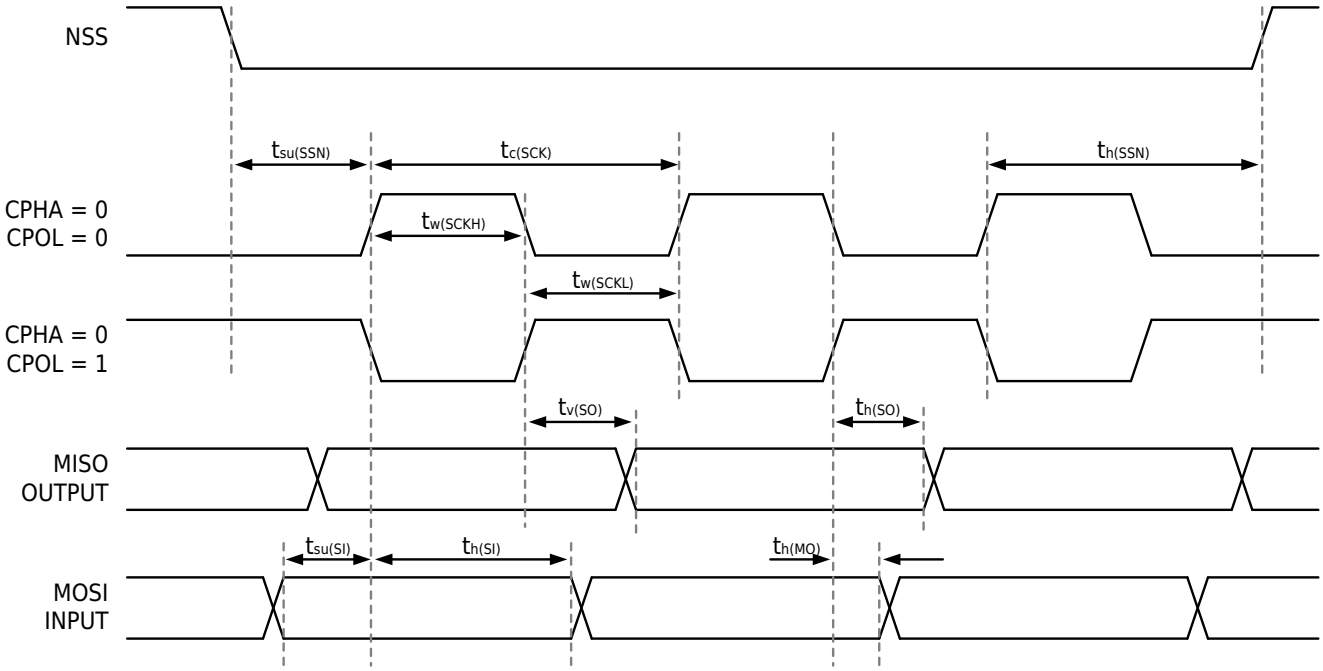


Figure 5-8 SPI Timing Diagram (Slave Mode CPHA=0)

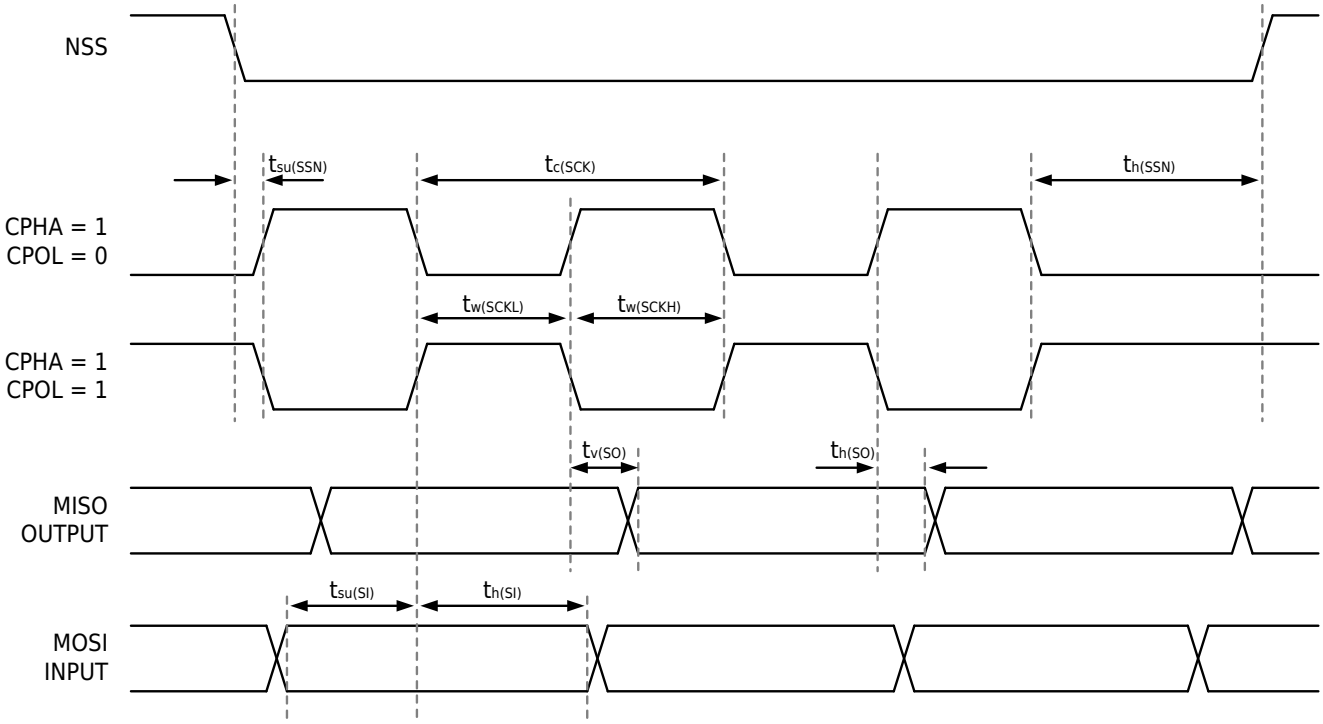
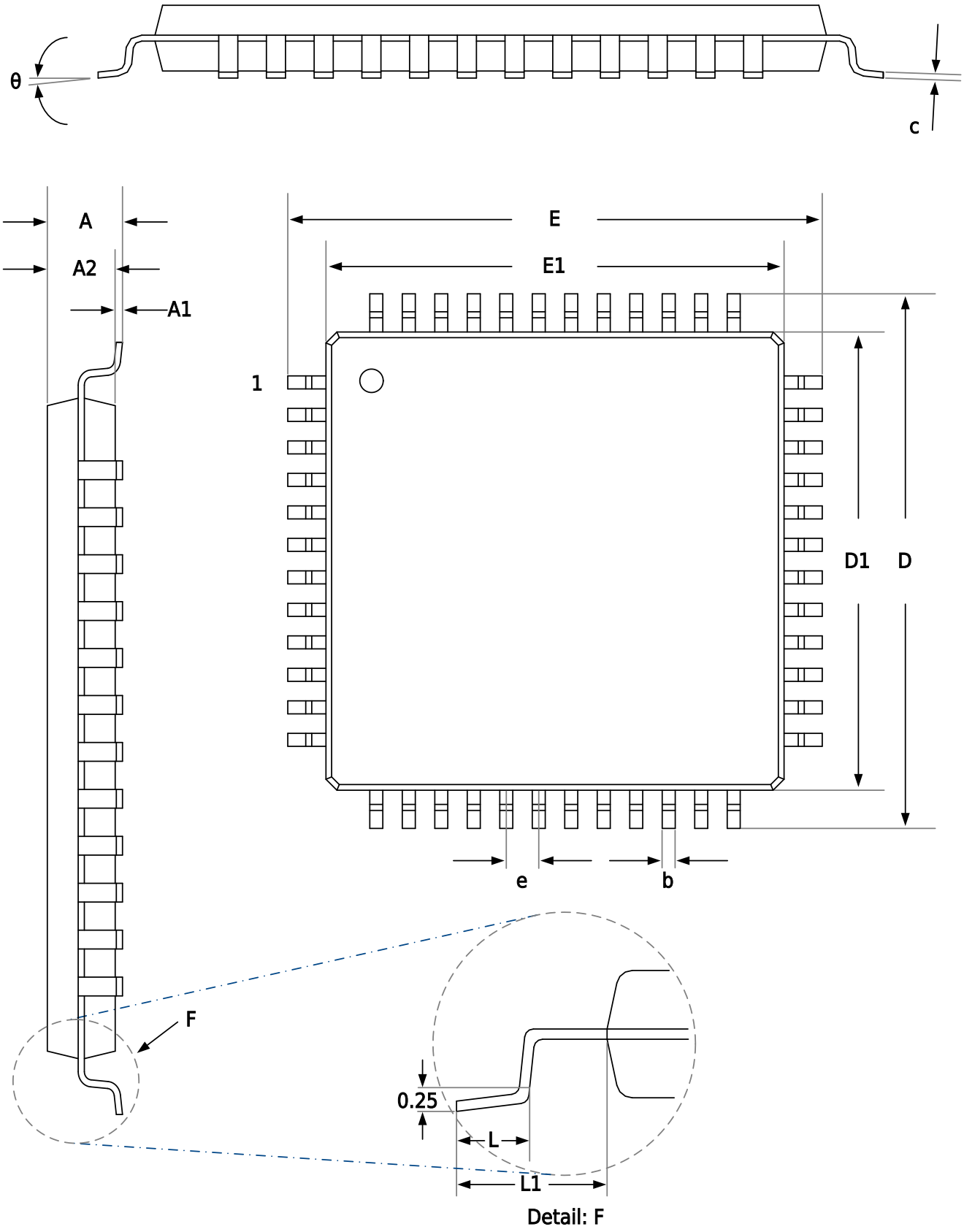


Figure 5-9 SPI Timing Diagram (Slave Mode CPHA=1)

6 Package Specifications

6.1 Package Dimensions

6.1.1 LQFP48 Package

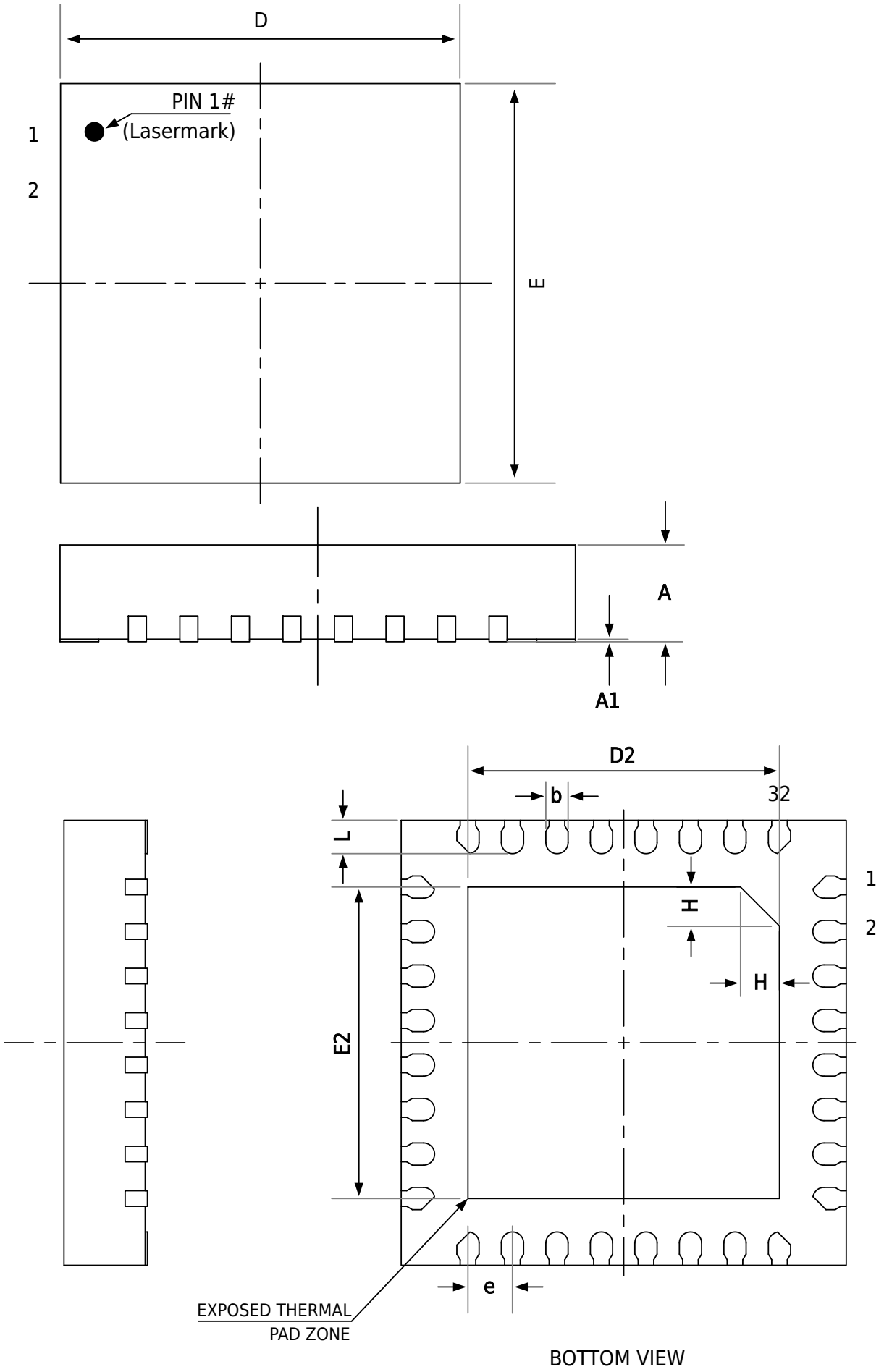


Symbol	7*7 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0	--	7°

Note

Dimensions "D1" and "E1" do not include mold flash.

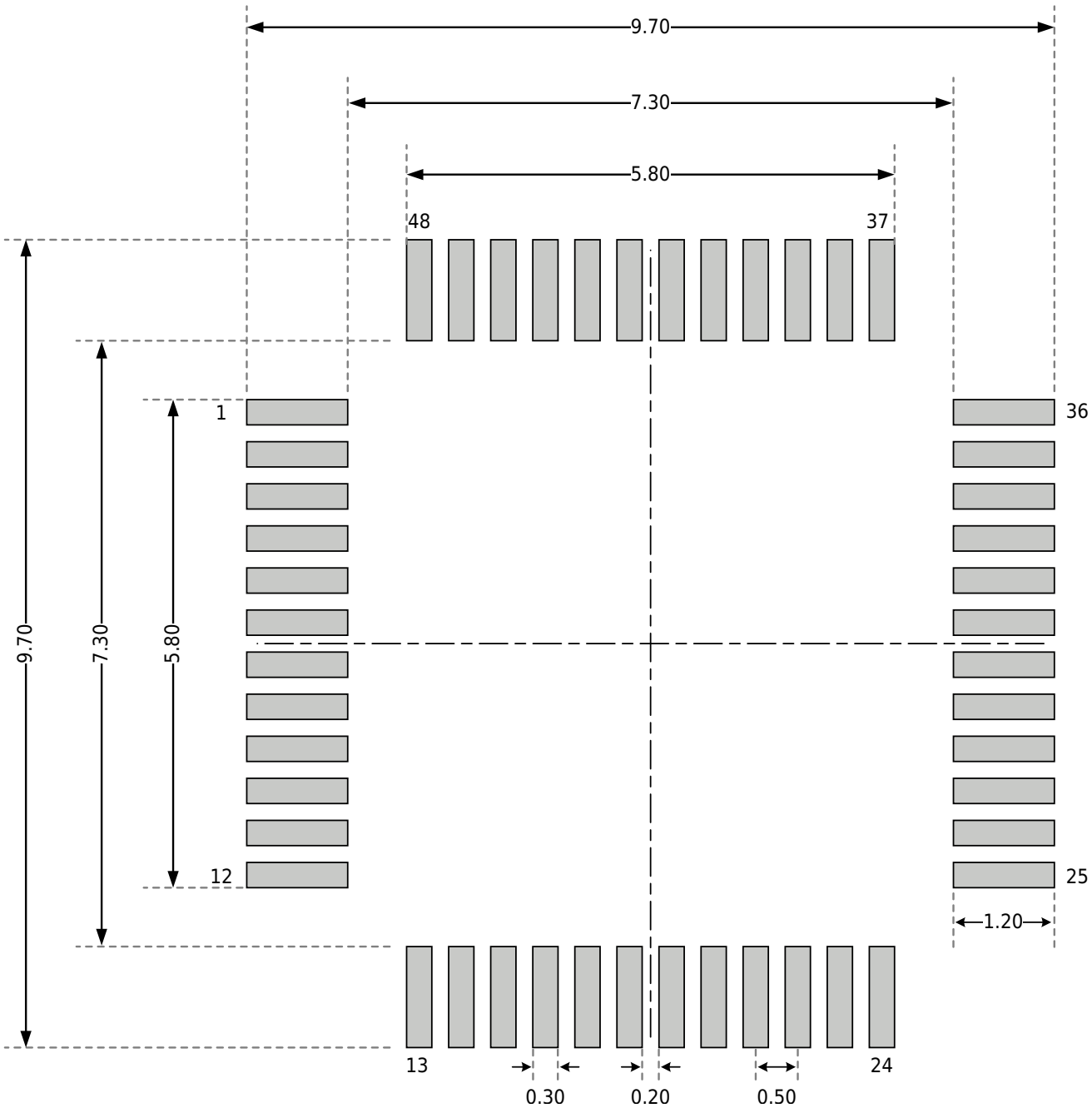
6.1.2 QFN32 Package



Symbol	4*4 Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
e	0.40BSC		
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
L	0.30	0.40	0.50
H	0.30REF		

6.2 PCB Land Pattern

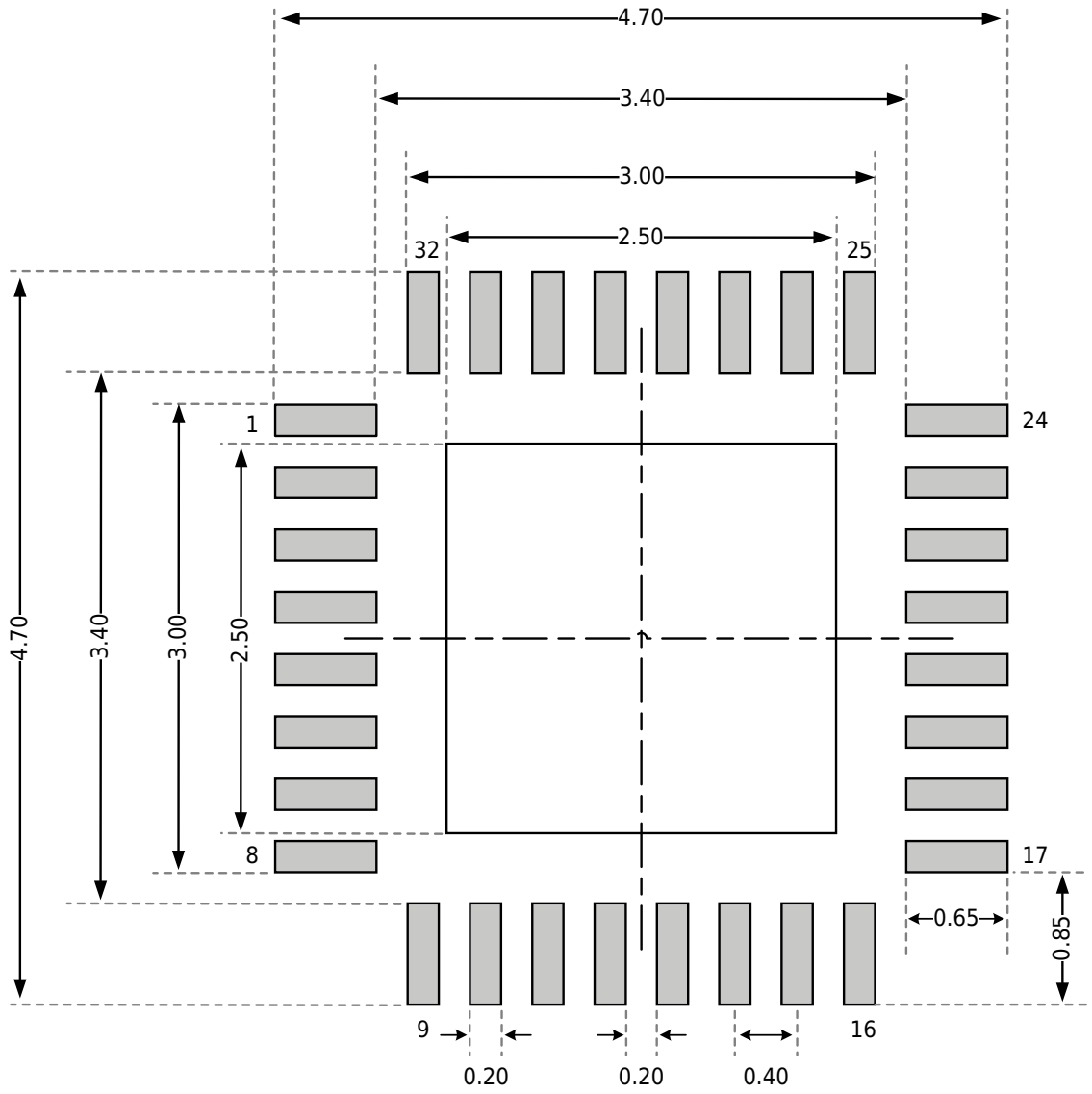
6.2.1 LQFP48 Package (7mm*7mm)



Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

6.2.2 QFN32 Package (4mm*4mm)



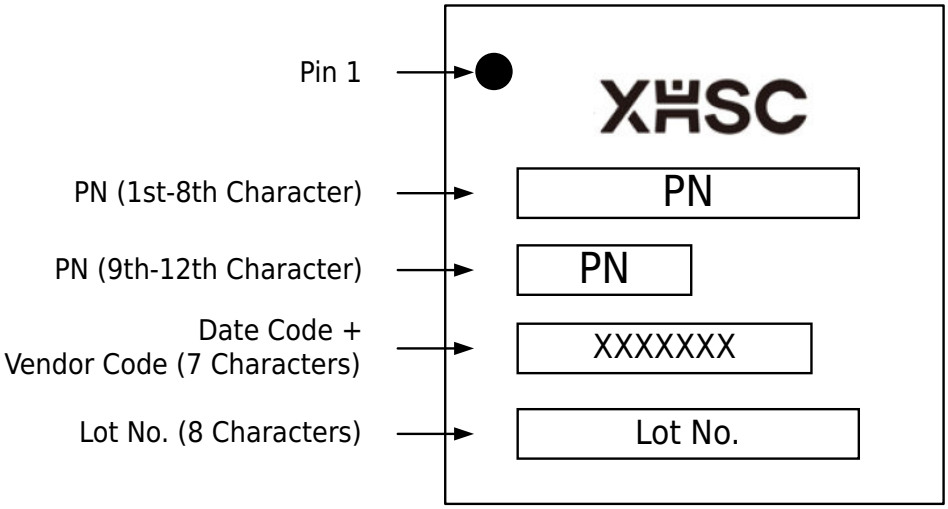
Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

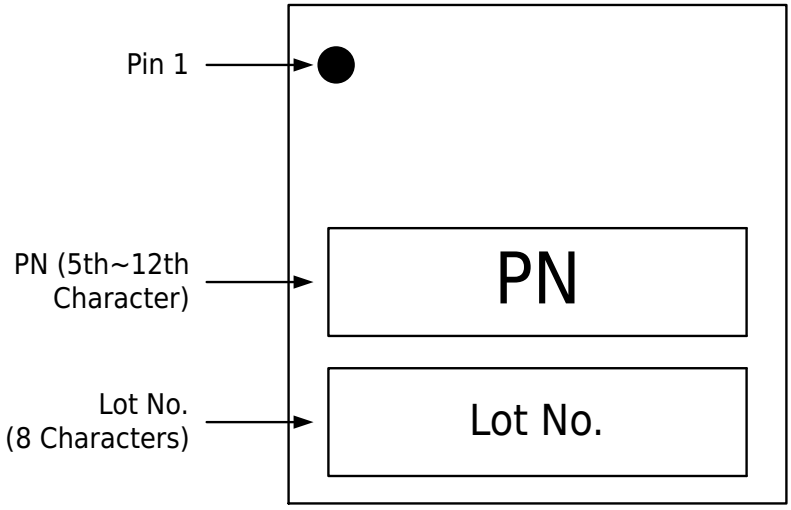
6.3 Package Marking

The location and information description of Pin1 on the front of each package are given below.

LQFP48 package (7mm*7mm)



QFN32 package (4mm*4mm)



Note

The blank boxes in the above figure indicate optional marks related to production, which are not explained in this section.

6.4 Packaging Thermal Resistance Coefficient

When the packaged chip is working at the specified working environment temperature, the junction temperature T_j(℃) of the chip surface can be calculated according to the following formula:

$T_j = T_A + (P_D * \theta_{JA})$

- T_A refers to the working environment temperature when the packaged chip is working, the unit is ℃;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is ℃/W;

- P_D refers to total power dissipation, which is the sum of internal power consumption (P_{INT}) and I/O pin power consumption (P_{IO}), the unit is W.

  $P_D = P_{INT} + P_{IO}$

  - P_{INT}: Internal power consumption, calculated as the product of Icc and Vcc.
  - P_{IO}: I/O pin power consumption, calculated as: $P_{IO} = \Sigma(V_{OL} * I_{OL}) + \Sigma((V_{CC} - V_{OH}) * I_{OH})$

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable junction temperature T_{Jmax} of the chip.

Table 6-3 Thermal Resistance Coefficient Table For Each Package

Package Type and Dimensions	Thermal Resistance Parameters (θ_{JA})	Unit
LQFP48 7mm*7mm/0.5mm pitch	75±10%	℃/W
QFN32 4mm*4mm/0.4mm pitch	53±10%	℃/W

7 Ordering Information

Part Number	HC32A052JATI-LQ48	HC32A052FAUI-QFN32TR
GPIO	40	26
Core	Cortex-M0+	Cortex-M0+
Frequency	64MHz	64MHz
Code Flash	128KB	128KB
RAM	16KB	16KB
Power Supply Voltages	2.0-5.5V	2.0-5.5V
Temp Range	-40-105℃	-40-105℃
DMA	1*5ch	1*5ch
LPTimer	1	1
Basic Timer	[6](1)	[6](1)
General Timer	2	2
Advanced Timer	4	4
RTC	1	1
IWDT	1	1
WWDT	1	1
PWM Channel	20ch	19ch
LPUART	2	1
USART	2	2
LIN	√	√
ISO7816	√	√
CAN	1	1
I2C	2	2
I2CSLV	1	1
SPI	2	1
12-bit ADC	1*16ch	1*10ch
OPA	2	-
VC	2	2
LVD	√	√
CRC	√	√
EAU	1	1
Package (mm*mm)	LQFP48(7*7)	QFN32(4*4)
Packing	Tray	Tape & Reel
Pitch	0.5mm	0.4mm
Thickness	1.4mm	0.75mm

Note

1. This module is time-division multiplexed with the General Timer.

Please contact the sales window for the latest mass production information before ordering.

Revision History

Revision/Date	Changes
Rev1.01 Feb. 12, 2026	1. Electrical Specifications: In the "Absolute Maximum Ratings" chapter, the symbol "T_J" representing temperature characteristics is revised to "T_{Jmax}"; In the "General Operating Conditions" chapter, the descriptions related to power dissipation have been removed; In the "External High-Speed Crystal XTH" chapter, the description of C_{Lx} is changed to "Matching capacitance". Meanwhile, optimize the annotation description; In the "External Low-Speed Crystal XTL" chapter, the description of C_{Lx} is changed to "Matching capacitance", and change the minimum value to "4pF". Meanwhile, optimize the annotation description; In the "RCH" chapter, the accuracy of the RCH Oscillator is revised to "1.5%" under the condition of T_A= -40-105 ℃; In the "Flash Memory Characteristics" chapter, the data of EC_{FLASH} parameters have been optimized and updated based on new conditions. 2. Package Specifications: In the "Package Dimensions" chapter, the A3, R, c of QFN package have been removed; In the "QFN48 Package" chapter, the max value of D2/E2 is modified to "5.40"; In the "QFN32 Package" chapter, the min value of L is modified to "0.30", the max and min value of D2/E2 is modified to "2.80, 2.60", the value of H (original "h") is modified to "0.30REF".
Rev1.00 May 12, 2025	First official release.