XIAOHUA SEMICONDUCTOR

HC32A448 Series

32-bit ARM® Cortex®-M4 Microcontroller

Datasheet

Rev1.31

February 2026

Feature List

ARM Cortex-M4 32-bit MCU+FPU, 250DMIPS, 256KB Flash, 68KB SRAM, 2CAN FD, EXMC, 15Timers, 3ADCs, 2DACs, 4CMPs, 6UARTs, 3SPIs, 2I2Cs, QSPI, AES, HASH (SHA256)

- ARMv7-M Architecture 32-bit Cortex-M4 CPU, FPU, MPU, DSP with SIMD instructions, and CoreSight standard debug unit. The highest operating frequency 200MHz can reach 250DMIPS or 680Coremarks computing performance
- Built-in memory
  - Maximum 256KB Flash memory
  - Maximum 68KB single-period access high-speed SRAM
- Power, clock, reset management
  - System power (V_{CC}) : 1.8-3.6V
  - 7 independent clock sources: XTAL (4-25MHz); XTAL32 (32.768kHz); HRC (16/20MHz); MRC (8MHz); LRC (32kHz); PLL; SWDTLRC (10kHz)
  - 15 reset sources: including POR, PVD1R/ PVD2R, NRST, etc. Each with an independent flag bit
- Low power operation
  - Peripheral functions can be independently enabled or disabled
  - 3 low power consumption modes: Sleep mode, Stop mode, Power-down mode
- Peripheral operation support system significantly reduces CPU processing load
  - 12-channel dual-host DMAC
  - 4 data computing units (DCU)
  - Supports peripheral event mutual triggering (AOS)
- High-performance simulation
  - 3 independent 12-bit 2.5Msps ADC
  - 2 independent 12-bit DAC
  - 4 independent voltage comparator (CMP)
- Timer
  - 2 multifunctional 16-bit PWM Timer (Timer6)
  - 3 16-bit motor PWM Timer (Timer4)
  - 1 32-bit general Timer (TimerA)
  - 4 16-bit general Timer (TimerA)
  - 2 16-bit basic Timer (Timer0)
  - Real-time Clock Timer (RTC)
  - 2 WDTs supporting internal dedicated clock
- Maximum 67 GPIOs
  - Maximum 62 5V-tolerant IOs
- Maximum 14 communication interfaces
  - 6 USART, supporting ISO7816-3 protocol
  - 3 SPI
  - 2 I2C, support SMBus protocol
  - 1 QSPI supporting 100Mbps high-speed access (XIP)
  - 2 CAN FD controllers (MCAN), compatible with CAN2.0A/B
- External Memory Controller EXMC
  - Supports static memory controller
  - Supports LCD parallel interface, compatible with 8080/6800 modes
- Data encryption function
  - AES/HASH (SHA256)/TRNG
- Package Form: LQFP80/64/48

Support model

HC32A448JCTI-LQ48	HC32A448KCTI-LQFP64
HC32A448MCTI-LQFP80	-

Statement

Precautions

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Xiaohua Semiconductor Co., Ltd.

Address:	F4, Block A, No.1867 Zhongke Road, Pudong New Area, Shanghai, China
URL:	https://www.xhsc.com.cn
E-mail:	XHSC_MCU@xhsc.com.cn (Business Consulting) XHSC_FAE@xhsc.com.cn (Technical Consulting)

Preface

Number Format

- 0x prefix is used for hexadecimal numbers
- 0b prefix is used for binary numbers
- Numbers without prefix are in decimal representation

Security Statement

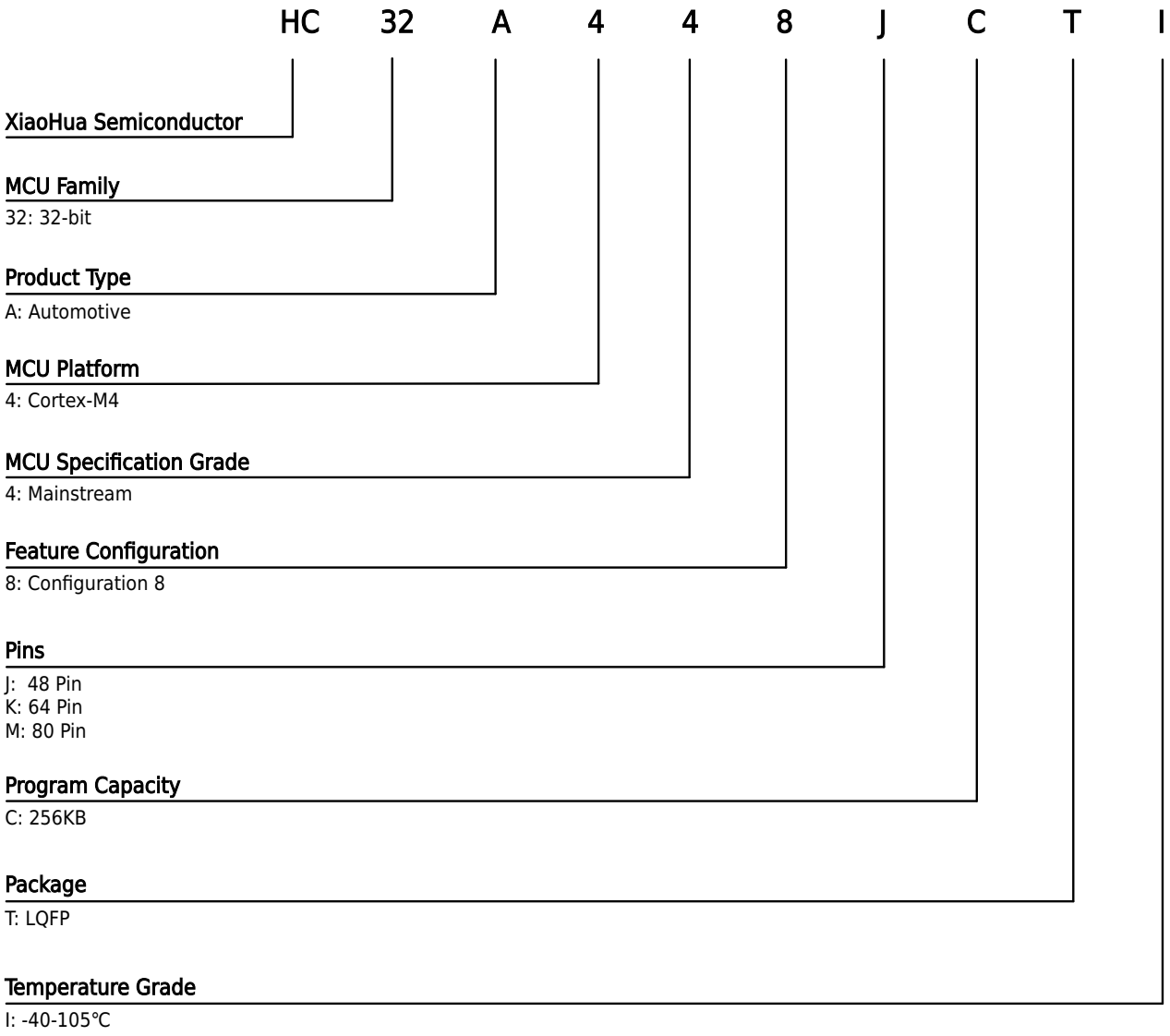
There may be potential security problems due to the use of a certain function or protocol, which need to be declared to remind users and avoid security risks.

Contents

1 Product Overview

1.1 Product Lineup

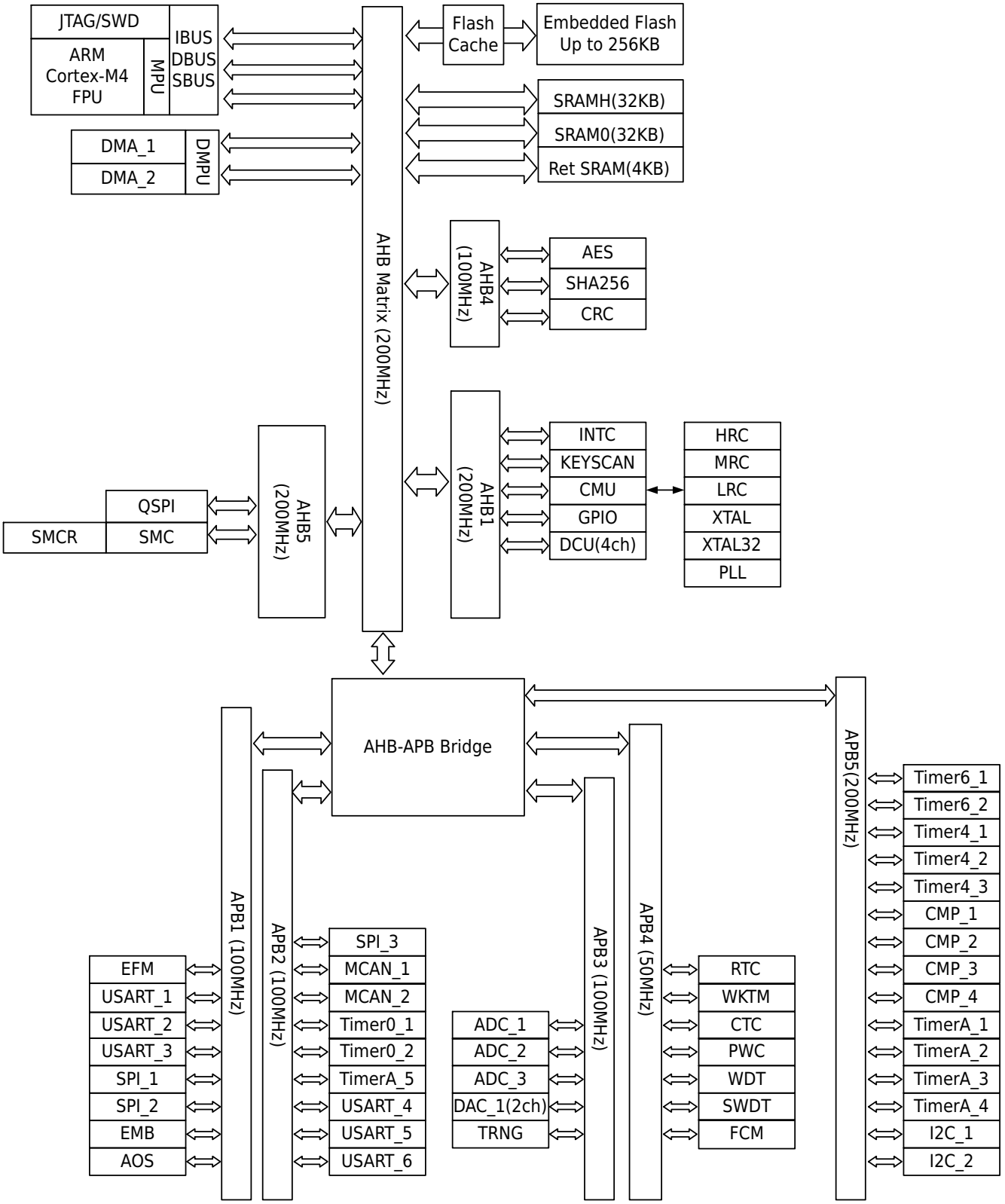
Product Name



Model Function Comparison Table

Product Name		HC32A448JCTI	HC32A448KCTI	HC32A448MCTI
Pins		48	64	80
GPIOs		38	52	67
5V Tolerant GPIOs		36	47	62
CPU	Core	Cortex-M4		
	Frequency	200MHz		
Storage Space	Flash	256KB		
	OTP	9KB		
	SRAM	68KB		
Clock	HRC	16/20MHz		
	MRC	8MHz		
	LRC	32.768kHz		
	XTAL	4-25MHz		
	XTAL32	32.768kHz		
	SWDTLRC	10kHZ		
Power Voltage Range		1.8-3.6V		
Temperature Range		-40-105℃		
External Port Interrupt		EIRQ * 16		
DMA Controller		2unit * 6ch		
Timer and Counter	Timer0	2unit		
	TimerA	5unit		
	Timer4	3unit		
	Timer6	2unit		
	RTC	1ch		
	WDT	1ch		
	SWDT	1ch		
Connectivity	USART	6ch		
	I2C	2ch		
	SPI	3ch		
	QSPI	1ch		
	CAN FD	2ch		
	EXMC	Not Supported	√	√
Analog	12-bit ADC	3unit, 11ch	3unit, 17ch	3unit, 24ch
	12-bit DAC	2ch	2ch	2ch
	CMP	4ch		
	PVD	√		
Safety	AES256	√		
	TRNG	√		
	HASH	SHA256		
Co-processing	DCU	√		
FCM		√		
Debugging Interface	SWD	√		
	JTAG	√		
Package		LQFP	LQFP	LQFP

1.2 Functional Block Diagram



Note

Products in different packages support varying resources. For detailed specifications, please refer to Model Function Comparison Table.

2 Functional Description

2.1 CPU

HC32A448 Series integrates embedded ARM® Cortex-M4 with FPU 32-bit simplified command CPU, which realizes less pins and low power consumption, and provides excellent computing performance and rapid interrupt response capability. The on-chip integrated storage capacity can give full play to the excellent command efficiency of ARM® Cortex-M4. The CPU supports DSP command, which can realize efficient signal processing operations and complex algorithms. Single-point precision FPU (Floating Point Unit) can avoid command saturation and speed up software development.

2.2 BUS

The main system consists of a 32-bit multi-layer AHB bus matrix, enabling the interconnection of the following host buses and slave buses:

- Host bus
  - Cortex-M4 core CPU-I bus, CPU-D bus, CPU-S bus
  - System DMA_1 bus, System DMA_2 bus
- Slave bus
  - Flash ICODE bus
  - Flash DCODE bus
  - Flash MCODE bus (The bus for accessing Flash by components other than the CPU on the host)
  - High-speed SRAMH (SRAMH 32KB) bus
  - System SRAM (SRAM0 32KB) bus
  - System SRAM (Ret SRAM 4KB) bus
  - APB1 peripheral bus (AOS/EFM/EMB/SPI/USART)
  - APB2 peripheral bus (TimerA/Timer0/SPI/USART/MCAN)
  - APB3 peripheral bus (ADC/DAC/TRNG)
  - APB4 peripheral bus (FCM/WDT/SWDT/PWC/CTC/RTC/WKTM)
  - APB5 peripheral bus (Timer4/TimerA/Timer6/CMP/I2C)
  - AHB1 peripheral bus (DCU/CMU/GPIO/DMA/INTC/KEYSCAN/MPU)
  - AHB4 peripheral bus (AES/HASH/CRC)
  - AHB5 peripheral bus (SMC/SMCR/QSPI)

With the bus matrix, efficient concurrent access from host buses to slave buses can be achieved.

2.3 RMU

The chip is configured with 15 reset modes:

- Power-on Reset (POR)
- NRST Pin Reset (NRST)
- Brown-out Reset (BOR)
- Programmable Voltage Detect 1 Reset (PVD1R)
- Programmable Voltage Detect 2 Reset (PVD2R)
- Watchdog Reset (WDTR)

- Special Watchdog Reset (SWDTR)
- Power-down Wake-up Reset (PDRST)
- Software Reset (SRST)
- MPU Error Reset (MPUR)
- RAM Parity Reset (RAMPR)
- RAMECC Reset (RAMECCR)
- Clock Frequency Error Reset (CKFER)
- XTAL Error Reset (XTALER)
- Cortex-M4 Lockup Reset (LKUPR)

2.4 CMU

The clock control unit provides a series of clock functions with different frequencies, including: an external high-speed oscillator, an external low-speed oscillator, one PLL clock, an internal high-speed oscillator, an internal medium-speed oscillator, an internal low-speed oscillator, a dedicated internal low-speed oscillator for SWDT, a clock prescaler, clock multiplexing, and clock gating circuit.

The clock control unit also provides a clock frequency measurement function. The clock frequency measurement circuit (FCM) monitors and measures the measurement target clock using the measurement reference clock. An interrupt or reset occurs when the setting range is exceeded.

AHB, APB, and Cortex-M4 clocks are derived from the System Clock. The maximum operating clock frequency of the System Clock can reach 200MHz, with 6 selectable clock sources:

1. External High-speed Oscillator (XTAL)
2. External Low-speed Oscillator (XTAL32)
3. PLLH Clock (PLLH)
4. Internal High-speed Oscillator (HRC)
5. Internal Medium-speed Oscillator (MRC)
6. Internal Low-speed Oscillator (LRC)

For each clock source, it can be individually turned on and off when not in use to reduce power consumption.

SWDT has an independent clock source: the dedicated internal low-speed oscillator for SWDT (SWDTLRC). The Real Time Clock (RTC) uses the external low-speed oscillator, internal low-speed oscillator, or the XTAL fractional frequency division clock as the clock source.

2.5 PWC

Power controller is used to control the supply, switching and detection of multiple power domains in multiple run modes and low power modes. The power controller consists of a power consumption control logic (PWCL), a power supply voltage detection unit (PVD).

The operating voltage (VCC) of the chip is 1.8V to 3.6V. The voltage regulator (LDO) supplies power to the VDD and VDDR domains, and the VDDR voltage regulator (RLDO) supplies power to the VDDR domain in Power-down mode. The chip provides two operating modes: high-speed and ultra-low-speed, and three low-power modes: sleep, stop and power-off through the power consumption control logic (PWCL).

The power voltage detection unit (PVD) provides functions such as power on reset (POR), power down reset (PDR), brown out reset (BOR), programmable voltage detection 1 (PVD1), programmable voltage detection 2 (PVD2). Among them, POR, PDR, and BOR control the chip reset action by detecting the

VCC voltage. PVD1 detects the VCC voltage and resets or interrupts the chip according to the register settings. PVD2 detects VCC voltage or external input detection voltage, and generates reset or interrupt according to register selection.

The VDDR area maintains power through RLDO when the chip enters Power-down mode, retaining the data of the 4KB Ret SRAM.

The analog blocks are equipped with dedicated supply pins for improved analog performance.

2.6 ICG

After the chip's reset is released, the hardware circuit reads data from FLASH addresses 0x00000400-0x0000045F and loads it into the Initialization Configuration (ICG) register. Addresses 0x00000408-0x0000040B, 0x00000410-0x0000041F, and 0x00000438-0x0000045F are reserved; please write all 1s to ensure normal chip action. When FLASH boot swap is disabled, this region is located in FLASH block 0, sector 0; when FLASH boot swap is enabled and the OTP in FLASH block 0, sector 0 is not latched (data at 0x03000A80-0x03000A83 is all 1s), this region is located in FLASH block 0, sector 1; Otherwise, this region is in FLASH block 0, sector 0. Users can modify the ICG register by programming or erasing sector 0. Addresses 0x00000420-0x00000437 are the data security protection enable region. The register reset value is determined by FLASH data.

2.7 EFM

The Flash interface accesses Flash through the ICODE, DCODE, and MCODE buses. The interface can perform programming, erasing and full erasing operations on Flash. Besides, it can accelerate code execution through command prefetching and caching mechanisms.

Main Features:

- Maximum 9KBytes OTP space
- ICODE Bus 16Bytes prefetching
- Two independent cache areas: ICODE bus cache space 1KBytes; DCODE bus cache space 128Bytes
- Supports boot swap function
- Support data security protection

2.8 SRAM

This product has 64KB system SRAM (SRAMH/SRAM0) and 4KB Power-down mode retention SRAM (Ret SRAM).

Each SRAM can be accessed as a byte, half-word (16 bits), or full-word (32 bits). All SRAM read and write operations can be performed at the fastest CPU speed (200MHz).

Ret SRAM can provide 4KB of data retention space in Power-down mode.

SRAM0 and Ret SRAM have ECC check. The ECC check is a one-correction-two-check code, which can correct one-bit error and check 2-bit errors. SRAMH has a parity check, with one check bit for each byte of data.

2.9 GPIO

Main features of GPIO:

- Each port group has 16 I/O pins, which may be less than 16 depending on actual configuration
- Support pull-up and pull-down input
- Support push-pull, open-drain output mode

- Support high, medium and low drive modes
- Supports free switching between CMOS/Schmitt input modes
- Support for external interrupt input
- Support I/O pin peripheral function multiplexing, one I/O pin can have up to 41 optional multiplexing functions
- Individual I/O pins can be programmed independently
- Each I/O pin can select 2 functions to be enable at the same time (does not support 2 output functions to be enable at the same time)

2.10 INTC

The interrupt controller (INTC) selects an interrupt event as an interrupt request and sends it to NVIC to wake up WFI; selects interrupt event as event input (RXEV) to wake up WFE; select low power consumption mode (Sleep mode and Stop mode) of interrupt event wake-up system ; control external interrupts and software interrupts.

The main features of INTC are as follows:

1. Maskable interrupts: INTC is equipped with 257 interrupt events, which are processed and sent to NVIC as interrupt requests (IRQ). It supports 130 IRQs, each IRQ corresponds to one or more interrupt events.

   Note

   For more instructions on exception and NVIC programming, please refer to the "Arm Cortex-M4 Processor Technical Reference Manual".

2. Programmable priority of NVIC: 16 programmable priorities (4-bit interrupt priority register is used).
3. Non-maskable interrupts: Multiple system interrupt event requests can be independently selected as non-maskable interrupts, and each interrupt event is equipped with independent enable, flag and flag clear registers.
4. Equipped with 16 external pin interrupt events.
5. Equipped with multiple interrupt events, please refer to the "Interrupt Event List" in the "Interrupt Controller (INTC)" chapter of "Reference Manual" for the specific number.
6. Equipped with 32 software interrupt events.
7. Interrupt wakes up system Sleep mode and Stop mode.

2.11 AOS

The Automatic Operation System (AOS) is used to achieve coordination between peripherals without the assistance of the CPU. It utilizes events generated by peripherals as AOS sources, such as timer comparison matches, timer counting overflow, RTC periodic signals, various states of the sending and receiving data of the communication module (idle, receive data full, transmit data end, transmit data empty), ADC conversion end events, etc., to trigger actions of other peripherals. The triggered peripheral actions are referred to as AOS targets.

The AOS also equips 4 programmable logical units (PLUs) for logical operations between PORT and AOS sources. Users can select one or more AOS sources to trigger the same AOS target based on their needs.

2.12 MPU

The MPU can provide protection to the memory, and can improve the security of the system by preventing unauthorized access.

This chip has built-in 1 MPU unit for CPU, 1 MPU unit for CPU main stack pointer, 1 MPU unit for CPU thread stack pointer, 2 MPU units for DMA and 1 MPU unit for IP.

Among them, the ARM MPU provides the access control of the CPU to the entire 4G address space.

MSPMPU/PSPMPU provide protection for the CPU's main stack pointer/thread stack pointer respectively. When the pointer exceeds the set range, the MPU action can be set to non-maskable interrupt/reset.

DMPU includes SMPU1/SMPU2, which respectively provide read and write access rights control of system DMA_1/system DMA_2 to the entire 4G address space. When accessing the prohibited space, the MPU action can be set to ignore/bus error/non-maskable interrupt/reset.

The IPMPU provides access control to system IP and security-related IP in non-privileged mode.

2.13 KEYSCAN

This product is equipped with a keyboard scan control module (KEYSCAN) 1 unit. The KEYSCAN module supports keyboard array (row and column) scanning, the column is driven by an independent scan output KEYOUTm (m=0-7), and the row KEYINn (n=0-15) is input as EIRQn (n=0-15) is detected. This module realizes the key recognition function through the line scan query method.

2.14 CTC

Clock Trimming Controller (CTC) can automatically calibrate internal high-speed oscillator (HRC). Due to the influence of the working environment, the frequency of HRC may deviate. Based on the external high-precision reference clock, CTC is used to automatically adjust the frequency of HRC by hardware to get an accurate HRC clock.

The CTC main features are as follows:

- Three external reference clock sources: XTAL, XTAL32, CTCREF
- 16-bit calibration counter for frequency measurement with reload function
- 8-bit calibration deviation value and 6-bit calibration value for frequency calibration
- Error interrupt for indicating calibration failure

2.15 DMA

DMA is used to transfer data between memory and peripheral function modules, enabling data exchange between memories, between memory and peripheral function modules, and between peripheral function modules without CPU involvement.

Main features of DMA:

- The DMA bus is independent of the CPU bus and transmits data according to the AMBA AHB-Lite bus protocol
- With 2 DMA control units, a total of 12 independent channels, which can independently operate different DMA transfer functions
- The start source of each channel is configured through an independent trigger source selection register
- 1 block per request
- The data block is a minimum of one data and can be up to 1024 data
- The width of each data item can be configured as 8-bit, 16-bit, or 32-bit
- It can be configured for 1-65535 transfers or infinite transfers
- The source address and destination address can be independently configured as fixed, incrementing, decrementing, repeated jump, or specified offset jump

- 3 types of interrupts can be generated: block transfer completed interrupt, transfer completed interrupt, and transfer error interrupt. Each interrupt can be configured to be masked or unmasked. Among them, block transfer completed and transfer completed can be used as event outputs, serving as trigger sources for other peripheral modules
- Support chain transfer function, enabling the transfer of multiple data blocks in a single request
- Support channel reset triggered by external events
- Support software-triggered start of transfer and software-triggered channel reset
- When not in use, it can be set to stop state to reduce power consumption
- The HPROT value in the AHB bus during DMA access can be set through a register

2.16 CMP

Voltage Comparator (hereinafter referred to as CMP) is a peripheral module that compares two analog voltages and outputs the comparison result. This product is equipped with two groups of 4 comparison channels: CMP1 and CMP2, CMP3 and CMP4.

CMP Main features:

- 4 comparison channels can independently perform normal comparison
- 2 comparison channels in the same group can be combined to achieve up to 2 window comparisons
- Each comparison channel's positive and negative voltage inputs have multiple input sources (IO, DAC) to choose from
- A noise filter can filter the comparator output, with 7 sampling clocks to choose from
- Timer PWM can be used for comparator blanking window control
- Interrupts can be generated at the edges of comparison result changes, other peripherals can be triggered, and STOP mode can be woken up
- Compare results can be monitored through registers and output to the external pin VCOUT
- Compare results can be used for EMB control events

2.17 ADC

The 12-bit ADC is an analog-to-digital converter that adopts the successive approximation method. This MCU is equipped with 3 ADC units, unit 1 supports a maximum of 16 channels, unit 2 supports a maximum of 8 channels, unit 3 supports a maximum of 12 channels, which can convert analog signals from external pins and inside the chip. Analog input channels can be arbitrarily combined into a sequence for single scan or continuous scan conversion. It supports continuous multiple conversions on any specified channel and averaging of the conversion results. The ADC block also includes an analog watchdog function that monitors the conversion results of any specified channel to detect if they exceed user-set ranges.

The main features of the ADC are as follows:

- High Performance
  - Configurable 12-bit, 10-bit and 8-bit resolution
  - The frequency ratio of the ADC digital interface clock (PCLK4) and conversion clock (PCLK2, also known as ADCLK) can be set to 1:1, 2:1, 4:1, 8:1, 1:2, or 1:4

    PCLK2 can optionally use a PLL clock source asynchronous to the system clock (HCLK), with a frequency ratio of PCLK4:PCLK2=1:1

    PCLK2 frequency supports up to 60MHz
  - Sampling Rate: 2.5Msps (PCLK2=60MHz, 12-bit, 11 sample periods, 13 conversion periods)

  - Independent programming of channel sampling time is supported
  - Each channel has an independent data register
  - Data registers can be configured for left/right alignment
  - Continuous multiple conversion averaging function
  - Oversampling function
  - Analog watchdog to monitor conversion results
  - The ADC module can be set to stop when not in use
- Analog Input Channel
  - Up to 24 external analog inputs
  - 1 internal analog signal: internal reference voltage
- Conversion Start Conditions
  - Software setup conversion started
  - Peripheral synchronously trigger the conversion to start
  - External pin trigger the conversion to start
- Conversion Mode
  - 2 scan sequences A, B, optionally specifying a single or multiple channels
  - Sequence A single scan
  - Sequence A continuous scan
  - Sequence A multiple data buffer mode
  - Dual sequence scan, with sequences A and B independently selecting trigger sources, and sequence B having higher priority than A
  - Cooperative operating mode (applicable to devices with two or three ADCs)
- Interrupt and Event Signal Output
  - Sequence A scan end interrupt and event ADC_EOCA
  - Sequence B scan end interrupt and event ADC_EOCB
  - Analog watchdog 0 compare interrupt and event ADC_CMP0
  - Analog watchdog 1 compare interrupt and event ADC_CMP1
  - All the event outputs mentioned above can start DMA

2.18 DAC

This MCU is equipped with 1 12-bit digital-to-analog converter (DAC) unit. DAC unit includes two DAC conversion channels that can operate independently or synchronously. The analog voltage output range has two selectable settings. Each conversion channel has an output amplifier to drive external loads directly without an external operational amplifier.

DAC Main features:

- 2 DAC conversion channels.
- 12-bit conversion data can be configured as left- or right-aligned.
- Both conversion channels module can perform synchronous conversion.
- The data computing unit (DCU) can output triangular and sawtooth waves.
- The output can be used as the negative-end voltage for the voltage comparator (CMP).
- The output has amplification function and can drive external loads directly.
- The ADC conversion priority mode reduces interference during ADC conversion.

2.19 Timer6

Advanced Control Timer 6 (Timer6) is a high-performance timer with 16-bit counting width, offering a rich and flexible combination of configurations suitable for various complex application scenarios. It supports multiple interrupts, events, and PWM outputs. This timer supports both sawtooth and triangular waveform modes and can generate various types of PWM signals (edge-aligned independent PWM, center-aligned independent PWM, center-aligned complementary PWM, and center-aligned asymmetric PWM, etc.). It enables both software and hardware synchronization between units (synchronized start, stop, clear, refresh, etc.). All reference registers support buffering (single-level and double-level buffering). Timer6 also supports pulse width and period measurement, 2-phase and 3-phase quadrature encoding count, and EMB control. This series of products is equipped with 2 units of Timer6.

2.20 Timer4

The General Control Timer 4 is a timer module designed for three-phase motor control, offering a variety of solutions for different three-phase motor control applications. It supports both triangular and sawtooth waveform modes, enabling the generation of various PWM waveforms. It also features buffer functionality and supports EMB control. 3 unit of Timer4 is carried in this product family.

2.21 EMB

The emergency brake module is a function module that generates contorl events output to the timer when certain conditions are met to stop the timer or change the PWM signal output to the external motor. The following factors are used to generate control events:

- External port input level change
- Level of PWM output port occurs in phase (same high or same low)
- Voltage comparator comparison results
- System error occurred
- Write register software control

2.22 TimerA

The General Timer A (TimerA) is a timer with a 16/32-bit counting width and 8-channel PWM output. This timer supports two waveform modes, triangular wave and sawtooth wave, capable of generating various PWM waveforms (single-side aligned PWM, double-side symmetrical PWM); supports synchronized counter startup; the compare reference value register supports the buffer function; supports cascading between units; supports 2-phase quadrature encoding count and 3-phase quadrature encoding count. This product series is equipped with 5 TimerA units, where Unit 1 (TimerA1) is a 32-bit timer; Units 2 (TimerA2) to 5 (TimerA5) are 16-bit timers; the 5 units can support up to 40 channels of PWM output.

2.23 Timer0

General Timer 0 (Timer0) is a basic timer that can realize synchronous counting and asynchronous counting. The timer contains two channels (CH-A and CH-B) that can generate compare match events and count overflow events during counting. This event can trigger an interrupt and can be used to trigger other module actions. This series of products is equipped with 2 units of Timer0.

2.24 RTC

A real time clock (RTC) is a counter that stores time information in BCD format. Record the specific calendar time from 00 to 99. Support 12/24 hour time system, automatically calculate the number of days 28, 29 (leap year), 30 and 31 according to the month and year.

2.25 WDT/SWDT

This product has two watchdog timers: one is a specialized watchdog timer (SWDT) with a dedicated internal RC (SWDTLRC: 10kHz) as the counting clock source, and the other is a universal watchdog timer (WDT) with a PCLK3 as the counting clock source. SWDT and WDT are 16-bit down-counters designed to detect software faults caused by applications deviating from normal operation due to external interference or unforeseen logical conditions.

Both watchdogs support the window function. The window interval can be preset before the count starts, and when the count value is within the window interval, the counter can be refreshed and the count restarted.

2.26 USART

This product is equipped with 6 units of Universal Synchronous Asynchronous Receiver/Transmitter (USART) modules, which can flexibly exchange full-duplex data with external devices; the USART equipped in this product supports universal asynchronous serial communication interface (UART) , clock synchronous communication interface, smart card interface (ISO/IEC7816-3) and LIN communication interface. Support modem operation (CTS/RTS operation), multiprocessor operation. UART receive timeout function is supported by cooperating with the Timer0 module. USART1 supports the STOP mode wake-up function via the RX line.

The specific function allocation is as follows:

Function	Support Module					
	USART1	USART2	USART3	USART4	USART5	USART6
UART	✓	✓	✓	✓	✓	✓
Multiprocessor Communication	✓	✓	✓	✓	✓	✓
Clock Synchronization Communication	✓	✓	✓	✓	✓	✓
Wake-up from STOP Mode via RX Line	✓	-	-	-	-	-
Fractional Baud Rate	✓	✓	✓	✓	✓	✓
LIN	-	-	✓	-	-	✓
Smart Card	✓	✓	-	✓	✓	-
UART Reception Timeout Function	✓	✓	-	✓	✓	-

2.27 I2C

I2C (Inter-Integrated Circuit) used as an interface between the microcontroller and the I2C serial bus. Provide multi-master mode function, which can control the protocol and arbitration of all I2C buses. Standard mode and fast mode are supported. SMBus is also supported.

Main Features of I2C:

- I2C bus mode and SMBUS bus mode are optional. Master mode and slave mode are optional. Automatically ensure various preparation times, hold times, and bus idle times corresponding to the transfer rate

- Standard mode up to 100kbps, fast mode up to 400kbps
- The start condition, restart condition, and stop condition are automatically generated, and the start condition, restart condition, and stop condition of the bus can be detected
- Supports up to 128 slave mode addresses. Supports 7-bit address format and 10-bit address format. Broadcast call address, SMBus host address, SMBus device default address, SMBus alarm address can be detected
- Answer bits can be automatically determined when sent. Answer bits can be automatically sent when reception
- Handshake function
- Arbitration function
- Timeout function, can detect SCL clock stop for a long time
- SCL input and SDA input have built-in digital filters that are programmable to filter
- Communication error, receive data full, send data empty, one frame send end, address match unanimously interrupt
- 2-stage transmit FIFO and 2-stage receive FIFO

2.28 SPI

This product is equipped with 3-channel serial peripheral interface SPI, supports high-speed full-duplex serial synchronous transmission, and facilitates data exchange with peripheral devices. Users can set the range of 3/4-wire, master/slave and baud rate as as required.

Table 2-2 SPI Main Features

Essentials	Description
Serial Communication Function	● Supporting 4-wire SPI mode and 3-wire clock synchronization mode ● Supports full-duplex synchronous communication mode and transmit-only communication mode ● Polarity and phase of adjustable communication clock SCK
Data Format	● Selectable data shift order: MSB start/LSB start ● Selectable data width: 4/5/6/7/8/9/10/11/12/13/14/15/16/20/24/32 bits ● A maximum of 4 frames width of 32-bit data can be transmitted or received at a single time
Baud Rate	● The baud rate can be adjusted by the built-in special baud rate generator in master mode. The baud rate ranges from 2 to 256 frequency division of PCLK1. ● Maximum baud rate allowed in slave mode is 6 frequency division of PCLK1
Data Buffer	● With 16-byte data buffer ● Supports double buffering
Error Monitoring	● Mode fault error monitoring ● Data overload error monitoring ● Data underload error monitoring ● Parity error monitoring

Essentials	Description
Chip Selection Signal Control	● Each channel is configured with 4 chip-selected signal line ● The relative timing relationship between the chip select signal and the communication clock can be adjusted ● The inactive time of the chip select signal between two consecutive communications can be adjusted ● Polarity adjustable
Transmission Control in Master Mode	● Start transmission by writing data to the data register ● Communication auto suspend function
Interrupt	● Receive buffer is full ● Transmit buffer is empty ● SPI error (mode/overload/underload/parity) ● SPI vacant ● Transmit complete (event source only)
Low Power Control	● Configurable module stop
Other Functions	● SPI initialization function

2.29 QSPI

The Quad Serial Peripheral Interface (QSPI) is a memory control module designed to communicate with serial ROMs with an SPI-compatible interface. Its objects mainly include serial flash memory, serial EEPROM and serial FeRAM.

2.30 EXMC

The External Memory Controller (EXMC) is an independent block used to access various off-chip storage and achieve data exchange. Through configuration, EXMC can convert the internal AMBA protocol interface into various types of dedicated off-chip memory communication protocol interfaces, including SRAM, PSRAM, NOR Flash.

2.31 MCAN

This product is equipped with two units of MCAN communication interface modules (MCAN1 and MCAN2), and two MCAN controllers are equipped with 2KB RAM.

Both CAN modules (MCAN1 and MCAN2) comply with ISO 11898-1:2015 (CAN Protocol Specification Version 2.0 Parts A, B) and CAN with Flexible Data-Rate Specification Version 1.0.

The 2KB message RAM memory can realize the filter (Rx Filter), receive FIFO (Rx FIFO), receive buffer (Rx Buffer), transmit event FIFO (Tx Event FIFO), and transmit buffer (Tx Buffer) functions. The message RAM is shared between MCAN1 and MCAN2 modules.

2.32 CPM

The Cryptographic Coprocessing Module (CPM) includes three sub-modules: AES Encryption and Decryption Algorithm Processor, HASH Secure Hash Algorithm, and TRNG True Random Number Generator.

- AES complies with the new Data Encryption Standard officially announced by the National Institute Of Standards and Technology (NIST) on October 2, 2000, with a fixed block length of 128 bits and key lengths supporting 128/192/256 bits.
- HASH is the SHA-2 version of SHA-256 (Secure Hash Algorithm), which complies with the national standard "FIPS PUB 180-3" issued by the US National Institute of Standards and Technology, and can generate a 256-bit message digest output for messages with a length of up to 2^{64} bits.
- TRNG is a random number generator based on continuous analog noise, providing 64-bit random numbers.

2.33 DCU

The Data Computing Unit (DCU) is a simple data processing block that does not rely on the CPU. Each DCU unit has three data registers capable of performing addition, subtraction, comparison, and window comparison functions on two data values. It can also provide continuously varying digital values to the DAC module through timer triggers to generate triangular and sawtooth wave outputs. This product is equipped with 4 DCU units.

2.34 CRC

The CRC algorithm of this module follows the definition of ISO/IEC13239, and adopts 32-bit CRC and 16-bit CRC respectively. The CRC32 generating polynomial is $X^{32}+ X^{26}+ X^{23}+ X^{22}+ X^{16}+ X^{12}+ X^{11}+ X^{10}+ X^{8}+ X^{7}+ X^{5}+ X^{4}+ X^{2}+ X+ 1$, and the initial value of 32 bits is 0xFFFFFFFF. The generating polynomial of CRC16 is $X^{16}+ X^{12}+ X^{5}+ 1$, and the initial value of 16 bits is 0xFFFF.

2.35 DBGC

This MCU's core is Cortex-M4, which includes hardware for advanced debugging functions. Using these debugging functions, the core can be stopped when fetching instructions (instruction breakpoint) or accessing data (data breakpoint). When the core is stopped, the internal state of the core and the external state of the system can be queried. After the query completes, the kernel and system are restored and program execution is restored.

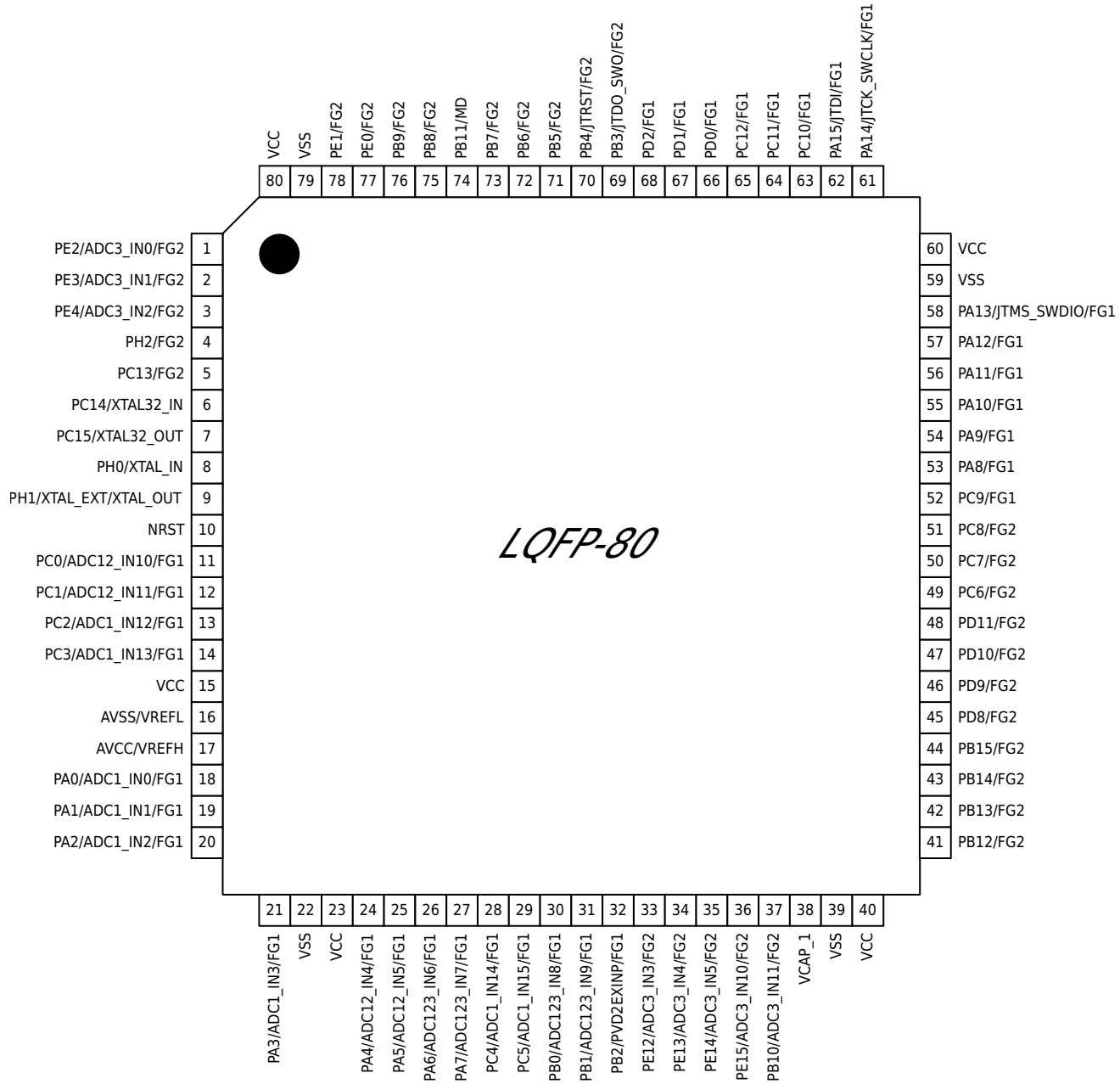
Debugging interface supported:

- Serial debug trace interface SWD
- Parallel debug trace interface JTAG

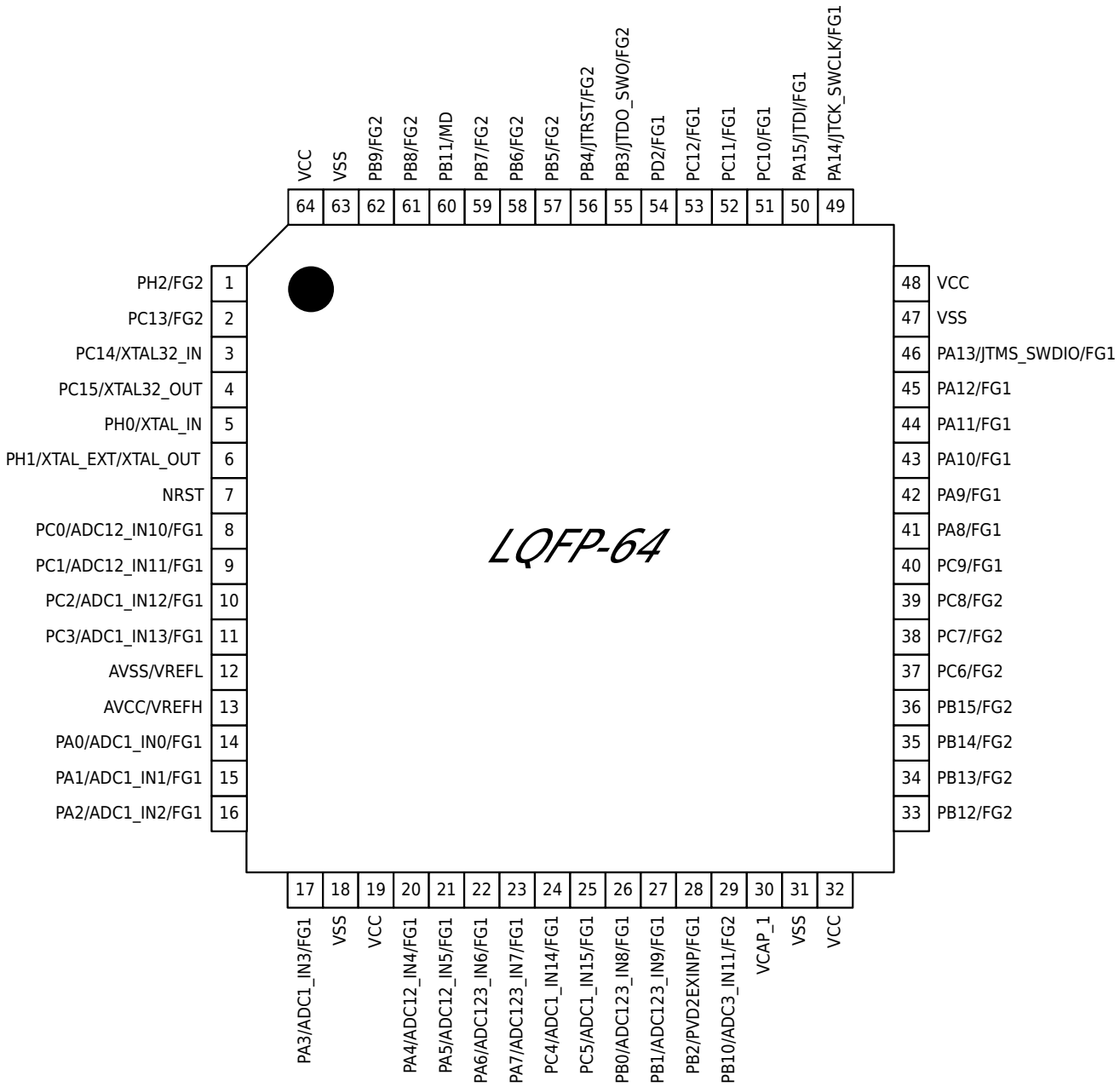
3 Pin Definitions

3.1 Pinout

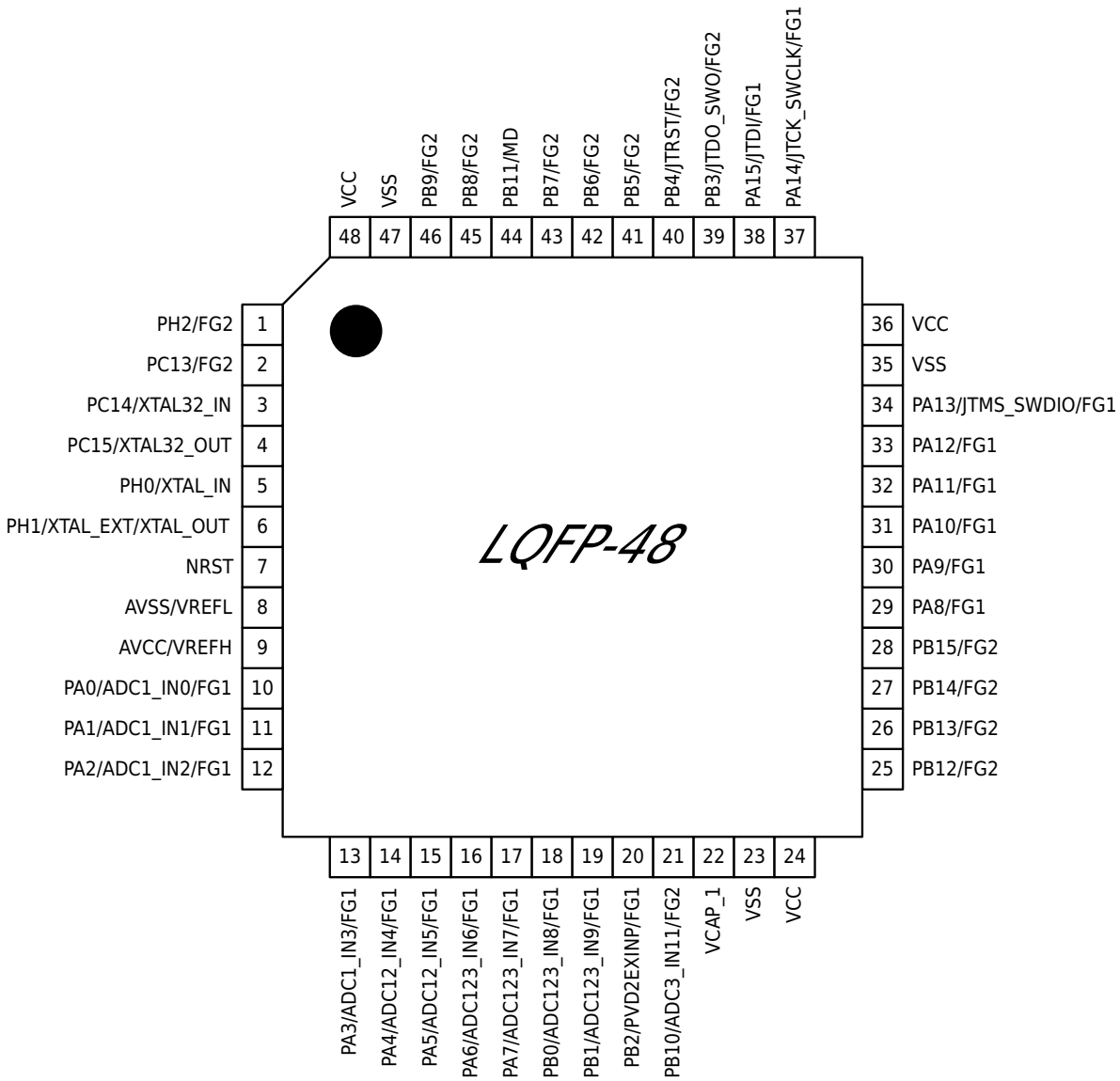
3.1.1 LQFP80 Package



3.1.2 LQFP64 Package



3.1.3 LQFP48 Package



3.2 Pin Function Table

LQFP80	LQFP64	LQFP48	Pin Name	Analog	EIRQ/ WKUP	TRACE/ JTAG	Func0 GPO	Func1 other	Func2 TMR4, VCOUT	Func3 TMR4, TMR6	Func4 TMRA	Func5 TMRA	Func6 EMB, TMRA	Func7 USART, SPI, QSPI	Func8 KEY, USART	Func9~10	Func11 TMR4, TMRA	Func12 EXMC, TMRA	Func13 TMR6, TMRA	Func14 EVNTPT	Func15 EVENTOUT	Func16~20	Func21 PLUIN	Func22 PLUOUT	Func23~31	Func Group
1	-	-	PE2	ADC3_IN0	EIRQ2	TRACECLK			TMR4_2_PCT		TMRA_3_PWM5			USART3_CK	USART6_RTS						EVENTOUT		PLU0_INA	PLU0_OUT		FG2
2	-	-	PE3	ADC3_IN1	EIRQ3	TRACED0			TMR4_2_ADSM		TMRA_3_PWM6			USART4_CK	USART5_RTS						EVENTOUT		PLU0_INB	PLU1_OUT		FG2
3	-	-	PE4	ADC3_IN2	EIRQ4	TRACED1		CTCREF	TMR4_1_PCT	TMR4_2_OWL	TMRA_3_PWM7			USART6_CK							EVENTOUT		PLU0_INC	PLU2_OUT		FG2
4	1	1	PH2		EIRQ2	TRACED2		FCMREF	TMR4_2_CLK		TMRA_4_PWM7	TMRA_3_TRIG	EMB_IN4	USART4_CK	USART6_CTS		TMRA_4_TRIG				EVENTOUT		PLU0_IND	PLU3_OUT		FG2
5	2	2	PC13		EIRQ13	TRACED3		RTC_OUT	VCOUT4	TMR4_1_OXL	TMRA_4_PWM8	TMRA_2_PWM2/ TMRA_2_CLKB		USART5_CK	USART6_RTS		TMR4_1_ADSM	EXMC_ADD16		EVNTP313			PLU1_INA	PLU0_OUT		FG2
6	3	3	PC14	XTAL32_IN	EIRQ14			CTCREF	TMR4_1_OVH	TMR4_3_OXH	TMRA_4_PWM5				USART5_CTS		TMR4_1_OXH	EXMC_BAA		EVNTP314			PLU1_INB	PLU1_OUT		
7	4	4	PC15	XTAL32_OUT	EIRQ15				TMR4_1_OWH	TMR4_3_OXL	TMRA_4_PWM6				USART5_RTS		TMR4_1_CLK	EXMC_ALE		EVNTP315			PLU1_INC	PLU2_OUT		
8	5	5	PH0	XTAL_IN	EIRQ0				TMR4_3_OXL			TMRA_5_PWM3											PLU1_IND	PLU3_OUT		
9	6	6	PH1	XTAL_EXT/ XTAL_OUT	EIRQ1				TMR4_3_CLK			TMRA_5_PWM4											PLU2_INA	PLU0_OUT		
10	7	7	NRST																							
11	8	-	PC0	ADC12_IN10+ CMP3_INP3+ CMP4_INP3	EIRQ0				TMR4_3_PCT		TMRA_2_PWM5							EXMC_RB0		EVNTP300	EVENTOUT		PLU2_INB	PLU1_OUT		FG1
12	9	-	PC1	ADC12_IN11	EIRQ1				TMR4_3_ADSM		TMRA_2_PWM6							EXMC_CLK		EVNTP301	EVENTOUT		PLU2_INC	PLU2_OUT		FG1
13	10	-	PC2	ADC1_IN12	EIRQ2				TMR4_3_OXH		TMRA_2_PWM7		EMB_IN3					EXMC_CE4		EVNTP302	EVENTOUT		PLU2_IND	PLU3_OUT		FG1
14	11	-	PC3	ADC1_IN13+ CMP1_INM2	EIRQ3			MCO_2	TMR4_3_OXL		TMRA_2_PWM8							EXMC_CE5		EVNTP303	EVENTOUT		PLU3_INA	PLU0_OUT		FG1
15	-	-	VCC																							
16	12	8	AVSS/VREFL																							
17	13	9	AVCC/VREFH																							
18	14	10	PA0	ADC1_IN0+ CMP1_INP1	EIRQ0+ WKUP0_0			TMR4_1_OVH	TMR4_2_OUH		TMRA_2_PWM1/ TMRA_2_CLKA	TMRA_1_PWM1/ TMRA_1_CLKA	TMRA_2_TRIG	SPI1_NSS1	USART3_CTS			EXMC_ADD17		EVNTP100	EVENTOUT		PLU3_INB	PLU1_OUT		FG1
19	15	11	PA1	ADC1_IN1+ CMP1_INP2	EIRQ1				TMR4_2_OUL		TMRA_2_PWM2/ TMRA_2_CLKB	TMRA_3_TRIG		SPI1_NSS2	USART5_CTS			EXMC_ADD18		EVNTP101	EVENTOUT		PLU3_INC	PLU2_OUT		FG1
20	16	12	PA2	ADC1_IN2+ CMP1_INP3	EIRQ2				TMR4_2_OVH		TMRA_2_PWM3	TMRA_5_PWM1/ TMRA_5_CLKA		SPI1_NSS3	USART6_CTS			EXMC_ADD19		EVNTP102	EVENTOUT		PLU3_IND	PLU3_OUT		FG1
21	17	13	PA3	ADC1_IN3+ CMP1_INP4+ CMP2_INP4	EIRQ3				TMR4_2_OVL		TMRA_2_PWM4	TMRA_5_PWM2/ TMRA_5_CLKB		USART5_CK	USART3_RTS			EXMC_ADD20		EVNTP103	EVENTOUT		PLU0_INA	PLU0_OUT		FG1
22	18	-	VSS																							
23	19	-	VCC																							
24	20	14	PA4	ADC12_IN4+ CMP2_INP1+ CMP3_INP4+ DAC_OUT1	EIRQ4			TMR4_1_OWH	TMR4_2_OWH			TMRA_3_PWM5		USART2_CK	KEYOUT0			EXMC_CE0		EVNTP104	EVENTOUT		PLU0_INB	PLU1_OUT		FG1
25	21	15	PA5	ADC12_IN5+ CMP2_INP2+ DAC_OUT2	EIRQ5				TMR4_2_OWL		TMRA_2_PWM1/ TMRA_2_CLKA	TMRA_3_PWM6	TMRA_2_TRIG	SPI3_NSS1	KEYOUT1			EXMC_DATA7		EVNTP105	EVENTOUT		PLU0_INC	PLU2_OUT		FG1
26	22	16	PA6	ADC123_IN6+ CMP2_INP3	EIRQ6				TMR4_2_ADSM	TMR4_1_PCT		TMRA_3_PWM1/ TMRA_3_CLKA	EMB_IN2	SPI3_NSS2	KEYOUT2			EXMC_DATA0		EVNTP106	EVENTOUT		PLU0_IND	PLU3_OUT		FG1
27	23	17	PA7	ADC123_IN7+ CMP1234_INM1	EIRQ7				TMR4_1_OUL	TMR6_1_PWMB	TMRA_1_PWM5	TMRA_3_PWM2/ TMRA_3_CLKB	EMB_IN3	SPI3_NSS3	KEYOUT3			EXMC_DATA1		EVNTP107	EVENTOUT		PLU1_INA	PLU0_OUT		FG1
28	24	-	PC4	ADC1_IN14+ CMP2_INM2	EIRQ4				TMR4_2_OUH			TMRA_3_PWM7		USART1_CK				EXMC_DATA8		EVNTP304	EVENTOUT		PLU1_INB	PLU1_OUT		FG1
29	25	-	PC5	ADC1_IN15+ CMP3_INM2	EIRQ5				TMR4_2_OUL			TMRA_3_PWM8						EXMC_DATA9		EVNTP305	EVENTOUT		PLU1_INC	PLU2_OUT		FG1
30	26	18	PB0	ADC123_IN8+ CMP3_INP1	EIRQ0				TMR4_1_OVL	TMR6_2_PWMB	TMRA_1_PWM6	TMRA_3_PWM3		USART4_CK	KEYOUT4			EXMC_DATA2		EVNTP200	EVENTOUT		PLU1_IND	PLU3_OUT		FG1
31	27	19	PB1	ADC123_IN9+ CMP3_INP2+ CMP4_INP2	EIRQ1+ WKUP0_1			CTCREF	TMR4_1_OWL		TMRA_1_PWM7	TMRA_3_PWM4	TMRA_4_PWM4	QSPI_NSS	KEYOUT5			EXMC_DATA3		EVNTP201	EVENTOUT		PLU2_INA	PLU0_OUT		FG1
32	28	20	PB2	PVD2EXINP	EIRQ2+ WKUP0_2			VCOUT	TMR4_1_PCT	TMR6_TRIGB	TMRA_1_PWM8	TMRA_5_PWM2/ TMRA_5_CLKB	EMB_IN1	QSPI_IO3						EVNTP202	EVENTOUT		PLU2_INB	PLU1_OUT		FG1
33	-	-	PE12	ADC3_IN3	EIRQ12				TMR4_1_OWL		TMRA_1_PWM7			SPI1_NSS1				EXMC_DATA10			EVENTOUT		PLU2_INC	PLU2_OUT		FG2
34	-	-	PE13	ADC3_IN4	EIRQ13				TMR4_1_OWH		TMRA_1_PWM3			SPI1_NSS2				EXMC_DATA11			EVENTOUT		PLU2_IND	PLU3_OUT		FG2
35	-	-	PE14	ADC3_IN5	EIRQ14			ADTRG1	TMR4_1_CLK		TMRA_1_PWM4			SPI1_NSS3				EXMC_DATA12			EVENTOUT		PLU3_INA	PLU0_OUT		FG2
36	-	-	PE15	ADC3_IN10	EIRQ15			ADTRG3			TMRA_1_PWM8	TMRA_5_TRIG	EMB_IN2	USART4_CK				EXMC_DATA13			EVENTOUT		PLU3_INB	PLU1_OUT		FG2
37	29	21	PB10	ADC3_IN11	EIRQ10			ADTRG2	TMR4_2_OVH	TMR4_1_OXL	TMRA_2_PWM3	TMRA_5_PWM8	TMRA_1_PWM3	QSPI_IO2				EXMC_DATA4		EVNTP210	EVENTOUT		PLU3_INC	PLU2_OUT		FG2
38	30	22	VCAP_1																							
39	31	23	VSS																							
40	32	24	VCC																							
41	33	25	PB12		EIRQ12			VCOUT1	TMR4_2_OVL	TMR6_TRIGB	TMRA_1_PWM8	TMRA_5_TRIG	EMB_IN2	QSPI_IO1	USART5_CTS			EXMC_DATA5		EVNTP212	EVENTOUT		PLU3_IND	PLU3_OUT		FG2

LQFP80	LQFP64	LQFP48	Pin Name	Analog	EIRQ/ WKUP	TRACE/ JTAG	Func0 GPO	Func1 other	Func2 TMR4, VCOUT	Func3 TMR4, TMR6	Func4 TMRA	Func5 TMRA	Func6 EMB, TMRA	Func7 USART, SPI, QSPI	Func8 KEY, USART	Func9~10	Func11 TMR4, TMRA	Func12 EXMC, TMRA	Func13 TMR6, TMRA	Func14 EVNTPT	Func15 EVENTOUT	Func16~20	Func21 PLUIN	Func22 PLUOUT	Func23~31	Func Group
42	34	26	PB13		EIRQ13			VCOUT2	TMR4_1_OUL	TMR6_1_PWMB	TMRA_1_PWM5	TMRA_4_PWM1/ TMRA_4_CLKA	TMRA_3_PWM1/ TMRA_3_CLKA	QSPI_IO0	USART5_RTS					EVNTP213	EVENTOUT		PLU0_INA	PLU0_OUT		FG2
43	35	27	PB14		EIRQ14			VCOUT3	TMR4_1_OVL	TMR6_2_PWMB	TMRA_1_PWM6	TMRA_4_PWM2/ TMRA_4_CLKB	TMRA_3_PWM2/ TMRA_3_CLKB	QSPI_SCK	USART6_CTS					EVNTP214	EVENTOUT		PLU0_INB	PLU1_OUT		FG2
44	36	28	PB15		EIRQ15			RTC_OUT	TMR4_1_OWL		TMRA_1_PWM7		EMB_IN4	USART3_CK	USART6_RTS		TMRA_1_PWM2/ CLKB	TMRA_2_PWM2/ CLKB	TMR6_2_PWMA	EVNTP215	EVENTOUT		PLU0_INC	PLU2_OUT		FG2
45	-	-	PD8		EIRQ8				TMR4_3_OUL	TMR4_2_OWL				QSPI_IO0	KEYOUT7		TMR4_1_OXH			EVNTP408	EVENTOUT		PLU0_IND	PLU3_OUT		FG2
46	-	-	PD9		EIRQ9				TMR4_3_OVL	TMR4_2_OVL				QSPI_IO1	KEYOUT6		TMR4_1_OXL			EVNTP409	EVENTOUT		PLU1_INA	PLU0_OUT		FG2
47	-	-	PD10		EIRQ10				TMR4_3_OWL					QSPI_IO2	KEYOUT5		TMR4_2_OXH			EVNTP410	EVENTOUT		PLU1_INB	PLU1_OUT		FG2
48	-	-	PD11		EIRQ11				TMR4_3_CLK					QSPI_IO3	KEYOUT4		TMR4_2_OXL			EVNTP411	EVENTOUT		PLU1_INC	PLU2_OUT		FG2
49	37	-	PC6		EIRQ6			CTCREF	TMR4_2_ADSM	TMR4_1_CLK	TMRA_3_PWM1/ TMRA_3_CLKA	TMRA_5_PWM8		QSPI_SCK	KEYOUT3					EVNTP306	EVENTOUT		PLU1_IND	PLU3_OUT		FG2
50	38	-	PC7		EIRQ7				TMR4_2_CLK	TMR4_3_OVH	TMRA_3_PWM2/ TMRA_3_CLKB	TMRA_5_PWM7		QSPI_NSS	KEYOUT2					EVNTP307	EVENTOUT		PLU2_INA	PLU0_OUT		FG2
51	39	-	PC8		EIRQ8				TMR4_2_OWH	TMR4_3_OVL	TMRA_3_PWM3	TMRA_5_PWM6		USART3_CK	KEYOUT1			EXMC_DATA14		EVNTP308	EVENTOUT		PLU2_INB	PLU1_OUT		FG2
52	40	-	PC9		EIRQ9			MCO_2	TMR4_2_OWL	TMR4_3_OUL	TMRA_3_PWM4	TMRA_5_PWM5			KEYOUT0			EXMC_DATA15		EVNTP309	EVENTOUT		PLU2_INC	PLU2_OUT		FG1
53	41	29	PA8	CMP4_INM2	EIRQ8+ WKUP2_0			MCO_1	TMR4_1_OUH	TMR6_1_PWMA	TMRA_1_PWM1/ TMRA_1_CLKA	TMRA_2_PWM1/ TMRA_2_CLKA		USART1_CK						EVNTP108	EVENTOUT		PLU2_IND	PLU3_OUT		FG1
54	42	30	PA9	CMP4_INP1	EIRQ9+ WKUP2_1			CTCREF	TMR4_1_OVH	TMR6_2_PWMA	TMRA_1_PWM2/ TMRA_1_CLKB									EVNTP109	EVENTOUT		PLU3_INA	PLU0_OUT		FG1
55	43	31	PA10	CMP4_INP4	EIRQ10+ WKUP2_2			CTCREF	TMR4_1_OWH	TMR4_3_CLK	TMRA_1_PWM3	TMRA_5_TRIG		USART6_CK						EVNTP110	EVENTOUT		PLU3_INB	PLU1_OUT		FG1
56	44	32	PA11		EIRQ11+ WKUP2_3			TMR4_1_OXL	TMR4_1_CLK	TMR6_TRIGA	TMRA_1_PWM4	TMRA_5_PWM1/ TMRA_5_CLKA	EMB_IN1	USART5_CK	USART3_RTS					EVNTP111	EVENTOUT		PLU3_INC	PLU2_OUT		FG1
57	45	33	PA12		EIRQ12+ WKUP3_0			TMR4_1_ADSM	TMR4_3_OWL	TMR6_TRIGA	TMRA_1_TRIG		TMRA_2_TRIG	USART6_CK	USART3_CTS		TMR4_2_PCT	EXMC_DATA6	TMRA_3_PWM1/ CLKA	EVNTP112	EVENTOUT		PLU3_IND	PLU3_OUT		FG1
58	46	34	PA13		EIRQ13+ WKUP3_1	JTMS_SWDIO			TMR4_3_ADSM		TMRA_2_PWM5			SPI2_NSS1			TMRA_5_TRIG	EXMC_DATA7		EVNTP113	EVENTOUT		PLU0_INA	PLU0_OUT		FG1
59	47	35	VSS																							
60	48	36	VCC																							
61	49	37	PA14		EIRQ14+ WKUP3_2	JTCK_SWCLK			TMR4_3_PCT		TMRA_2_PWM6		TMRA_4_TRIG	SPI2_NSS2				EXMC_CE0		EVNTP114	EVENTOUT		PLU0_INB	PLU1_OUT		FG1
62	50	38	PA15		EIRQ15+ WKUP3_3	JTDI			TMR4_3_OXH		TMRA_2_PWM1/ TMRA_2_CLKA		TMRA_2_TRIG	SPI2_NSS3						EVNTP115	EVENTOUT		PLU0_INC	PLU2_OUT		FG1
63	51	-	PC10		EIRQ10				TMR4_3_OUH		TMRA_2_PWM7	TMRA_5_PWM1/ TMRA_5_CLKA					TMR4_2_OXL			EVNTP310	EVENTOUT		PLU0_IND	PLU3_OUT		FG1
64	52	-	PC11		EIRQ11				TMR4_3_OVH		TMRA_2_PWM8	TMRA_5_PWM2/ TMRA_5_CLKB					TMR4_2_OXH			EVNTP311	EVENTOUT		PLU1_INA	PLU0_OUT		FG1
65	53	-	PC12		EIRQ12				TMR4_3_OWH	TMR4_2_PCT	TMRA_4_TRIG	TMRA_5_PWM3					TMR4_1_OXL			EVNTP312	EVENTOUT		PLU1_INB	PLU1_OUT		FG1
66	-	-	PD0		EIRQ0			VCOUT	TMR4_2_OUL	TMR4_3_OUH		TMRA_5_PWM4								EVNTP400	EVENTOUT		PLU1_INC	PLU2_OUT		FG1
67	-	-	PD1		EIRQ1				TMR4_2_OWH	TMR4_3_OWH	TMRA_3_TRIG									EVNTP401	EVENTOUT		PLU1_IND	PLU3_OUT		FG1
68	54	-	PD2		EIRQ2				TMR4_1_OXH	TMR4_2_OVH	TMRA_2_PWM4									EVNTP402	EVENTOUT		PLU2_INA	PLU0_OUT		FG1
69	55	39	PB3		EIRQ3+ WKUP0_3	JTDO_TRACE-SWO		FCMREF	TMR4_3_CLK		TMRA_2_PWM2/ TMRA_2_CLKB									EVNTP203	EVENTOUT		PLU2_INB	PLU1_OUT		FG2
70	56	40	PB4		EIRQ4+ WKUP1_0	NJTRST			TMR4_3_OWL		TMRA_3_PWM1/ TMRA_3_CLKA									EVNTP204	EVENTOUT		PLU2_INC	PLU2_OUT		FG2
71	57	41	PB5		EIRQ5+ WKUP1_1			ADTRG3	TMR4_3_OWH	TMR6_1_PWMA	TMRA_3_PWM2/ TMRA_3_CLKB	TMRA_3_TRIG	TMRA_4_TRIG	USART4_CK			TMR4_1_OXH		TMRA_1_PWM2/ CLKB	EVNTP205	EVENTOUT		PLU2_IND	PLU3_OUT		FG2
72	58	42	PB6		EIRQ6+ WKUP1_2			ADTRG2	TMR4_3_OVL		TMRA_4_PWM1/ TMRA_4_CLKA						TMR4_1_OXL			EVNTP206	EVENTOUT		PLU3_INA	PLU0_OUT		FG2
73	59	43	PB7		EIRQ7+ WKUP1_3			ADTRG1	TMR4_3_OVH		TMRA_4_PWM2/ TMRA_4_CLKB						TMR4_2_OXH	EXMC_ADV		EVNTP207	EVENTOUT		PLU3_INB	PLU1_OUT		FG2
74	60	44	PB11/MD																	EVNTP211			PLU3_INC	PLU2_OUT		
75	61	45	PB8		EIRQ8				TMR4_3_OUL		TMRA_4_PWM3			USART5_CK	KEYOUT7		TMR4_2_OXL	EXMC_WE		EVNTP208	EVENTOUT		PLU3_IND	PLU3_OUT		FG2
76	62	46	PB9		EIRQ9				TMR4_3_OUH		TMRA_4_PWM4		EMB_IN4	SPI2_NSS1	KEYOUT6		TMR4_1_ADSM	EXMC_OE		EVNTP209	EVENTOUT		PLU0_INA	PLU0_OUT		FG2
77	-	-	PE0		EIRQ0			MCO_1	TMR4_1_ADSM		TMRA_4_TRIG			SPI2_NSS2							EVENTOUT		PLU0_INB	PLU1_OUT		FG2
78	-	-	PE1		EIRQ1			MCO_2	TMR4_3_CLK					SPI2_NSS3			TMR4_2_OUH				EVENTOUT		PLU0_INC	PLU2_OUT		FG2
79	63	47	VSS																							
80	64	48	VCC																							

Func32-63 are primarily serial communication functions (including USART, SPI, I2C, MCAN), divided into 2 Function Groups (FG1, FG2). Detailed correspondence is shown in the following table.

Table 3-2 Func32-63 Table

	Func32	Func33	Func34	Func35	Func36	Func37	Func38	Func39	Func40	Func41	Func42	Func43	Func44	Func45	Func46	Func47
FG1	USART1_TX	USART1_RX	USART1_RTS	USART1_CTS	USART2_TX	USART2_RX	USART2_RTS	USART2_CTS	SPI1_MOSI	SPI1_MISO	SPI1_NSS0	SPI1_SCK	SPI2_MOSI	SPI2_MISO	SPI2_NSS0	SPI2_SCK
FG2	USART3_TX	USART3_RX	USART3_RTS	USART3_CTS	USART4_TX	USART4_RX	USART4_RTS	USART4_CTS	SPI3_MOSI	SPI3_MISO	SPI3_NSS0	SPI3_SCK	SPI1_MOSI	SPI1_MISO	SPI1_NSS0	SPI1_SCK

	Func48	Func49	Func50	Func51	Func52	Func53	Func54	Func55	Func56	Func57	Func58	Func59	Func60	Func61	Func62	Func63
FG1	I2C1_SDA	I2C1_SCL	I2C2_SDA	I2C2_SCL	USART3_TX	USART3_RX	USART6_TX	USART6_RX	MCAN1_TX	MCAN1_RX	-	-	-	-	-	-
FG2	I2C1_SDA	I2C1_SCL	MCAN1_TX	MCAN1_RX	USART5_TX	USART5_RX	USART6_TX	USART6_RX	MCAN2_TX	MCAN2_RX	-	-	-	-	-	-

Table 3-3 Port Configuration

Package	Port Group	Bits																Pin Count Total	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
LQFP80	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	67
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	-	-	-	-	o	o	o	o	-	-	-	-	-	o	o	o	7	
	PortE	o	o	o	o	-	-	-	-	-	-	-	o	o	o	o	o	9	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	3	
LQFP64	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	52
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	-	-	-	-	-	-	-	-	-	-	-	-	-	o	-	-	1	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	3	
LQFP48	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	38
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	-	-	-	-	-	-	-	-	-	-	-	-	-	3	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	3	

Table 3-4 General Functional Specifications

Port		Pull-Up/Pull-Down	Open-Drain Output	Driving Capacity	5V Tolerant
PortA	PA0-PA6, PA9-PA15	Support	Support	Low/Medium/High	Support
	PA7, PA8	Support	Support	Low/Medium/High	Not supported
PortB	PB0-PB15	Support	Support	Low/Medium/High	Support
PortC	PC0-PC2, PC6-PC15	Support	Support	Low/Medium/High	Support
	PC3-PC5	Support	Support	Low/Medium/High	Not supported
PortD	PD0-PD2, PD8-PD11	Support	Support	Low/Medium/High	Support
PortE	PE0-PE4, PE12-PE15	Support	Support	Low/Medium/High	Support
PortH	PH0-PH2	Support	Support	Low/Medium/High	Support

Note

Input voltage must not be higher than VREFH/AVCC when used as an analog function.

3.3 Pin Function Description

Table 3-5 Pin Function Description

Categories	Functional Name	I/O	Description
Power	VCC	I	Power supply
	VSS	I	Power ground
	VCAP_1	IO	Core voltage
	AVCC/VREFH	I	Analog power supply/analog reference voltage
	AVSS/VREFL	I	Analog power ground/analog reference voltage
System	NRST	I	Reset terminal, active low
	MD	I	Mode terminal
PVD	PVD2EXINP	I	PVD2 external input comparison voltage
Clock	XTAL_IN	I	External main clock oscillator interface
	XTAL_EXT/XTAL_OUT	IO	XTAL_EXT external clock input/external main clock oscillator interface
	XTAL32_IN	I	External sub clock (32.768kHz) oscillator interface
	XTAL32_OUT	O	
	MCO_x (x=1-2)	O	Internal clock output
GPIO	GPIOxy (x=A to E, H y=0-15)	IO	General input output
EVENTOUT	EVENTOUT	O	Cortex-M4 CPU event output
EIRQ	EIRQx (x=0-15)	I	Maskable external interrupt
	WKUPx_y (x=0-3 y=0-3)	I	PowerDown mode external wake-up input
Event Port	EVNTPxy (x=1-4 y=0-15)	IO	Event port input and output functions
KEYSCAN	KEYOUTx (x=0-7)	O	KEYSCAN scan output signal
JTAG/SWD	JTCK_SWCLK	I	Online debugging interface
	JTMS_SWDIO	IO	
	JTDO_TRACESWO	O	
	JTDI	I	
	NJTRST	I	
TRACE	TRACECLK	O	Trace debug synchronous clock output
	TRACEDx (x=0-3)	O	Trace debug data output

Categories	Functional Name	I/O	Description
FCM	FCMREF	I	External reference clock input for clock frequency measurement
RTC	RTC_OUT	O	1Hz clock output
Timer4	TMR4_x_CLK (x=1-3)	I	Counting clock port input
	TMR4_x_OUH (x=1-3)	IO	PWM port U-phase output
	TMR4_x_OUL (x=1-3)	IO	PWM port U-phase output
	TMR4_x_OVH (x=1-3)	IO	PWM port V-phase output
	TMR4_x_OVL (x=1-3)	IO	PWM port V-phase output
	TMR4_x_OWH (x=1-3)	IO	PWM port W-phase output
	TMR4_x_OWL (x=1-3)	IO	PWM port W-phase output
	TMR4_x_OXH (x=1-3)	IO	PWM port X-phase output
	TMR4_x_OXL (x=1-3)	IO	PWM port X-phase output
	TMR4_x_ADSM (x=1-3)	O	Special event output monitoring
	TMR4_x_PCT (x=1-3)	O	PWM periodic output monitoring
Timer6	TMR6_TRIGA	I	External event trigger A input
	TMR6_TRIGB	I	External event trigger B input
	TMR6_x_PWMA (x=1-2)	IO	External Event Trigger Input or PWM Port Output
	TMR6_x_PWMB (x=1-2)	IO	External Event Trigger Input or PWM Port Output
TimerA	TMRA_x_TRIG (x=1-5)	I	External event trigger input
	TMRA_x_PWM1/CLKA (x=1-5)	IO	External event trigger input or PWM port output or count clock port input
	TMRA_x_PWM2/CLKB (x=1-5)	IO	External event trigger input or PWM port output or count clock port input
	TMRA_x_PWMy (x=1-5 y=3-8)	IO	External Event Trigger Input or PWM Port Output
EMB	EMB_INx (x=1-4)	I	Port input control signal
USART	USARTx_TX (x=1-6)	IO	Transmit data
	USARTx_RX (x=1-6)	IO	Receiving data
	USARTx_CK (x=1-6)	IO	Communication clock
	USARTx_RTS (x=1-6)	O	Request transmiting signal
	USARTx_CTS (x=1-6)	I	Clear transmiting signal

Categories	Functional Name	I/O	Description
SPI	SPIx_MISO (x=1-3)	IO	Master input/slave output data transfer pin
	SPIx_MOSI (x=1-3)	IO	Master output/slave input data transfer pin
	SPIx_SCK (x=1-3)	IO	Transmission clock
	SPIx_NSS0 (x=1-3)	IO	Slave selection input/output pin
	SPIx_NSSy (x=1-3 y=1-3)	O	Slave selection output pin
QSPI	QSPI_IOx (x=0-3)	IO	Data line
	QSPI_SCK	O	Clock output
	QSPI_NSS	O	Slave selection
I2C	I2Cx_SCL (x=1-2)	IO	Clock line
	I2Cx_SDA (x=1-2)	IO	Data line
MCAN	MCANx_TX (x=1-2)	O	Transmit data
	MCANx_RX (x=1-2)	I	Receiving data
CMP	VCOUT1	O	CMP1 result output
	VCOUT2	O	CMP2 result output
	VCOUT3	O	CMP3 result output
	VCOUT4	O	CMP4 result output
	VCOUT	O	CMP1-4 result OR output
	CMPx_INPy (x=1-4 y=1-4)	I	CMPx positive analog input
	CMPx_INM2 (x=1-4)	I	CMPx negative analog input
	CMP1234_INM1	I	CMP1,2,3,4 negative analog input
ADC	ADTRG1	I	ADC1 AD conversion external start source
	ADTRG2	I	ADC2 AD conversion external start source
	ADTRG3	I	ADC3 AD conversion external start source
	ADC123_INx (x=6-9)	I	ADC1,2,3 shared external analog input port
	ADC12_INx (x=4-5, 10, 11)	I	ADC1,2 shared external analog input port
	ADC1_INx (x=0-3, 12-15)	I	ADC1 external analog input port
	ADC3_INx (x=0-5, 10, 11)	I	ADC3 external analog input port
DAC	DAC_OUTx (x=1-2)	O	DAC analog output
EXMC	EXMC_CLK	IO	For detailed information, refer to the "Reference Manual" chap-

Categories	Functional Name	I/O	Description
EXMC	EXMC_OE	O	ter titled "External Memory Controller (EXMC) - Functional Description - Protocol Interface" for EXMC port configuration.
	EXMC_WE	O	
	EXMC_ALE	O	
	EXMC_BAA	O	
	EXMC_ADV	O	
	EXMC_CEx (x=0, 4-5)	O	
	EXMC_RB0	I	
	EXMC_ADDx (x=16-20)	O	
	EXMC_DATAx (x=0-15)	IO	
PLU	PLUx_INy (x=0-3 y=A-D)	I	Logic Processing Unit Input
	PLUx_OUT (x=0-3)	O	Logic Processing Unit Output

3.4 Pin Instructions

Table 3-6 Pin Instruction

Pin Name	Usage Notes
VCC	Power Supply. Connect to 1.8V-3.6V and place a decoupling capacitor near the VSS pin (refer to "Electrical Specifications").
VSS	Source ground, connected to 0V.
VCAP_1	Core Voltage. Place a capacitor near the VSS pin to stabilize the core voltage (refer to "Electrical Specifications").
AVCC	Analog Power Supply. Supply power to analog modules; connect to the same voltage as VCC (refer to "Electrical Specifications"). When not using an independent analog power supply, connect the pin to VCC and ensure it is not left floating.
AVSS	Analog Power Ground. Supply ground to analog modules; connect to the same voltage as VSS (refer to "Electrical Specifications"). When not using an independent analog power supply, connect the pin to VSS and ensure it is not left floating.
PB11/MD	Mode input. When NRST is released (changing from low level to high level), this pin must be fixed at low level. Recommended to connect a resistor (4.7kΩ) to VSS (pull-down).
NRST	Reset pin (NRST), active low. Resistance to VCC when not in use (pull-up).
Pxy (x=A to E, H y=0-15)	General pin. When used as an input function, for 5V-tolerant pins, the input voltage should not exceed 5V; for non-5V-tolerant pins, it should not exceed VCC. When used as an analog input, the analog voltage should not exceed VREFH/AVCC. When not in use, leave floating or connect a resistor to VCC (pull-up) or VSS (pull-down).

4 Electrical Specifications

4.1 Parameter Conditions

Unless otherwise specified, all voltages are based on VSS.

4.1.1 Minimum and Maximum Values

All Minimum Values and Maximum Values are measured under the worst conditions.

Data resulted from comprehensive evaluation, and/or guaranteed by design are indicated in the table footnotes, and they will not be tested on the production line.

4.1.2 Typical Values

Unless otherwise specified, typical data are given based on T_A=25℃ and VCC=3.3V. These data are only used for design guidance and have not been tested.

4.1.3 Typical Curve

Unless otherwise specified, all typical curves are untested and are for design reference only.

4.1.4 Load Capacitance

The left of Figure 4-1 : Pin Load Condition (Left) and Input Voltage Measurement (Right) displays the load conditions used to measure the pin parameters.

4.1.5 Pin Input Voltage

The right of Figure 4-1 : Pin Load Condition (Left) and Input Voltage Measurement (Right) displays the measurement method of the input voltage on the device pin.

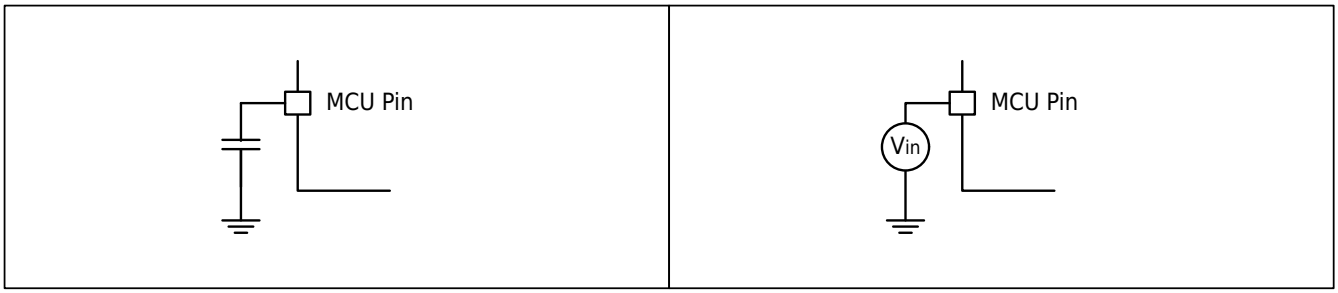


Figure 4-1 Pin Load Condition (Left) and Input Voltage Measurement (Right)

4.1.6 Power Scheme

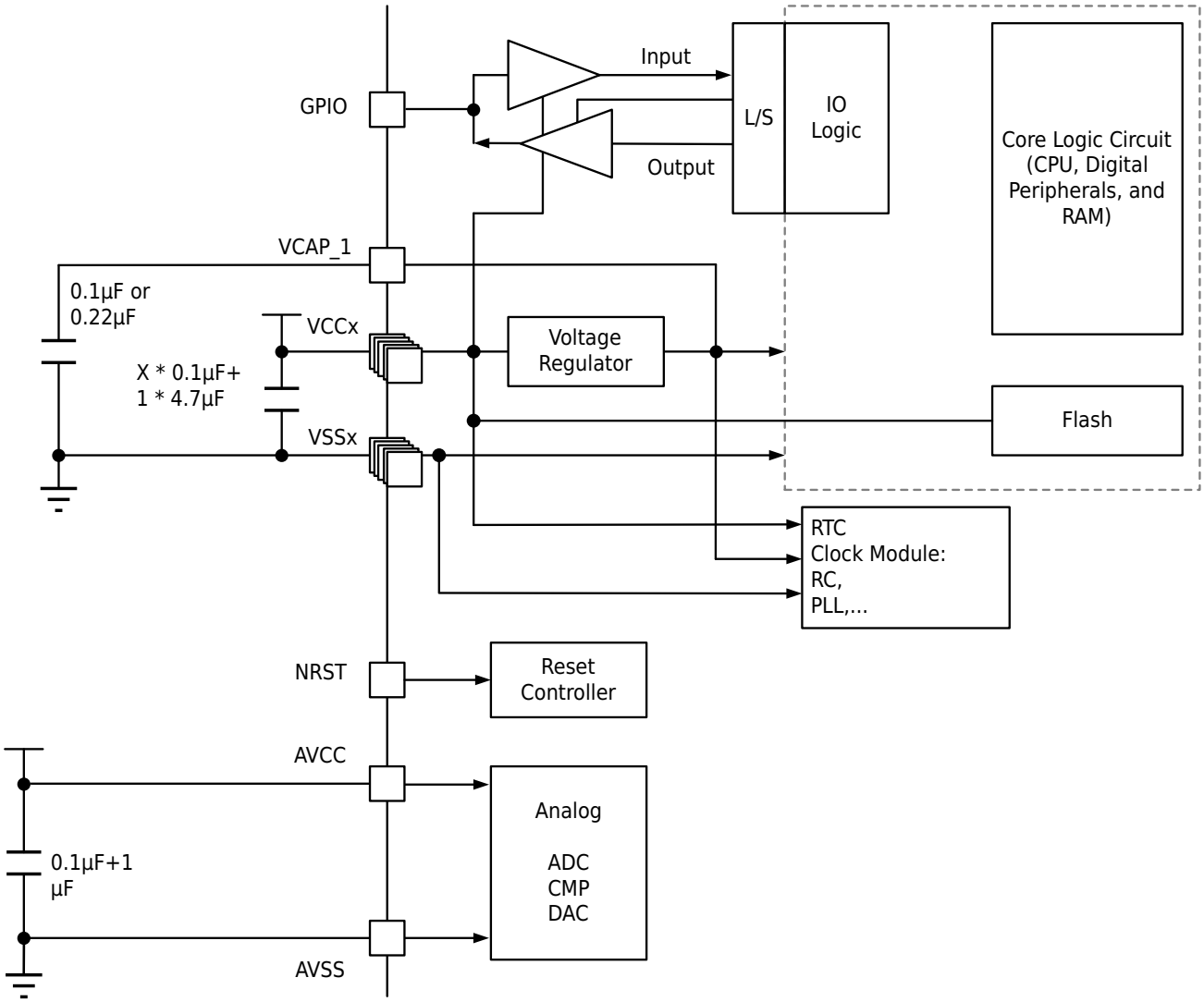


Figure 4-2 Power Scheme

Note

1. 4.7μF ceramic capacitor must be connected to one of VCC pins.
2. AVSS=VSS.
3. Each power supply pair (e.g. VCC/VSS, AVCC/AVSS...) must be decoupled with the above-mentioned filter ceramic capacitors. These capacitors must be as close as possible to or below that of the appropriate pins under the PCB to ensure the normal operation of the device. It is not recommended to remove the filter capacitor to reduce the size or cost of PCB, which may lead to abnormal operation of the device.

4.1.7 Current Consumption Measurement

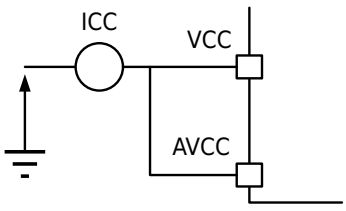


Figure 4-3 Current Consumption Measurement Solution

4.2 Absolute Maximum Ratings

If the load applied to the device exceeds the value given in the list of "Absolute Maximum Ratings", it may cause permanent damage to the device. These values are only rated stresses, and do not mean that the device functions normally under these conditions. Long-term operation at the maximum rating may affect the reliability of the device.

Table 4-1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{CC}-V_{SS}	External main supply voltage (including AVCC, VCC)(1)	-0.3	4.0	V
V_{IN}	Input voltage on pins other than PA7, PA8 and PC3-PC5(2)	V_{SS}-0.3	V_{CC}+4.0 (Max. 5.8V)	V
	Input voltage on PA7, PA8, PC3-PC5(2)	V_{SS}-0.3	V_{CC}+0.7 (Max. 4.0V)	
|VSSx-VSS|	Voltage difference between different grounding pins	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human model)	Please refer to "Electrical Sensitivity"		-

Note

1. Within the allowable range, all main power supply (VCC, AVCC) and grounding (VSS, AVSS) pins must always be connected to external power supply.
2. The maximum value of V_{IN} must always be followed. For information on the maximum allowable injected current values, refer to Table 4-2 : Current Characteristics.

Table 4-2 Current Characteristics

Symbol	Description	Max	Unit
ΣI_{VCC}	Total current flowing into all VCC_X power wires (pull current)(1)	240	mA
ΣI_{VSS}	Total current flowing out all VSS_X ground wires (sink current)(1)	-240	mA
I_{VCC}	Maximum current flowing into each VCC_X power wire (pull current)(1)	100	mA
I_{VSS}	Maximum current flowing out each VSS_X ground wire (sink current)(1)	-100	mA
I_{IO}	Output sink current on any I/O and control pins	20	mA
	Output pull current on any I/O and control pins	-20	mA
ΣI_{IO}	Total output sink current on all I/O and control pins(2)	120	mA
	Total output pull current on all I/O and control pins(2)	-120	mA

Note

1. Within the allowable range, all main power supply (VCC, AVCC) and grounding (VSS, AVSS) pins must always be connected to external power supply.
2. The total output current must be correctly distributed in all power domains. This total output current is suitable for packages of 64PINs and above; for 48PINs package, the maximum total output current is ±80mA.

Table 4-3 Temperature Characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage Temperature Range	-65-+150	℃
T_{Jmax}	Maximum Junction Temperature	125	℃

4.3 Operating Conditions

4.3.1 General Operating Conditions

Table 4-4 General Operating Conditions

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{HCLK}	Internal AHB Clock Frequency	High speed mode PWRC2.DVS=0b11 PWRC3.DDAS=0b1111	-	-	200	MHz
		Ultra-low speed mode(1) PWRC2.DVS=0b10 PWRC3.DDAS=0b0000	-	-	8	
V_{CC}(1)	Standard Operating Voltage	-	1.8	-	3.6	V
V_{AVCC}(1)	Analog Operating Voltage	-	1.8	-	3.6	V
V_{IN}(1)	Input Voltage on 5V Tolerant Pin(2)(3)(4)	$2V \le V_{CC} \le 3.6V$ $2V \le V_{AVCC} \le 3.6V$	-0.3	-	5.5	V
		$V_{CC}<2V$ $V_{AVCC}<2V$	-0.3	-	5.2	V
	Input Voltage on non-5V Tolerant Pin (PA7/PA8/PC3-5)	-	-0.3	-	V_{CC}+0.3	V
T_J(1)	Junction Temperature Range	-	-40	-	125	℃
T_A(1)	Working Temperature Range	-	-40	-	105	℃

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. To keep the voltage above V_{CC}+0.3, the internal pull-up/pull-down resistors must be disabled.
3. Ensure that the power supply (VCC, AVCC) of the device is stabilized before this voltage is added to the 5V voltage-tolerant pin of the device.
4. It is forbidden to directly connect this input voltage to external power supply. It is suggested that external power supply and grounding should be connected in series through a resistor above 1kΩ.

4.3.2 Working Conditions at Power On and Power Down

Table 4-5 Working Conditions at Power On and Power Down

Symbol	Parameters	Min	Max	Unit
t_{VCC}(1)	VCC Rise Time Rate	20	20000	μs/V
	VCC Fall Time Rate	20	20000	

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.3 Reset and Power Control Module Characteristics

Table 4-6 Reset and Power Control Module Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{BOR}	BOR Monitoring Voltage	ICG1.BOR_LEV=0b00	1.70	1.90	2.10	V
		ICG1.BOR_LEV=0b01(1)	1.80	2.00	2.20	V
		ICG1.BOR_LEV=0b10(1)	1.90	2.10	2.30	V
		ICG1.BOR_LEV=0b11	2.10	2.30	2.50	V
V_{PVD1}	PVD1 Monitoring Voltage(3)	PVD1LVL[2:0]=0b000	1.80	2.00	2.20	V
		PVD1LVL[2:0]=0b001(1)	1.90	2.10	2.30	V
		PVD1LVL[2:0]=0b010(1)	2.10	2.30	2.50	V
		PVD1LVL[2:0]=0b011(1)	2.33	2.55	2.77	V
		PVD1LVL[2:0]=0b100(1)	2.43	2.65	2.87	V
		PVD1LVL[2:0]=0b101(1)	2.53	2.75	2.97	V
		PVD1LVL[2:0]=0b110(1)	2.63	2.85	3.07	V
		PVD1LVL[2:0]=0b111	2.73	2.95	3.17	V
V_{PVD2}	PVD2 Monitoring Voltage(3)	PVD2LVL[2:0]=0b000	1.90	2.10	2.30	V
		PVD2LVL[2:0]=0b001(1)	2.10	2.30	2.50	V
		PVD2LVL[2:0]=0b010(1)	2.33	2.55	2.77	V
		PVD2LVL[2:0]=0b011(1)	2.43	2.65	2.87	V
		PVD2LVL[2:0]=0b100(1)	2.53	2.75	2.97	V
		PVD2LVL[2:0]=0b101(1)	2.63	2.85	3.07	V
		PVD2LVL[2:0]=0b110	2.73	2.95	3.17	V
		PVD2LVL[2:0]=0b111(5)	0.90	1.10	1.30	V
V_{PVD}hyst(1)	Hysteresis of PVD1/2(4)	-	-	100	-	mV
V_{POR}	Power On/Power Down Reset Threshold	Rising Edge VPOR	1.56	1.68	1.80	V
		Falling Edge VPDR	1.52	1.64	1.76	V
V_{POR}hyst(1)	Hysteresis of POR	-	-	40	-	mV

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
I_{RUSH}(1)	Surge Current When Voltage Regulator Powered On (POR or wake-up from Power-down)	-	-	100	150	mA
T_{NRST}(1)	NRST Reset Minimum Width	-	10	-	-	µs
T_{IPVD1}(2)	PVD1 Reset Release Time	-	300	380	460	µs
T_{IPVD2}(2)	PVD2 Reset Release Time	-	300	380	460	µs
T_{INRST}(2)	NRST Reset Release Time	-	25	35	50	µs
T_{RIPT}(2)	Internal Reset Time	-	140	160	200	µs
T_{RSTBOR}(2)	BOR Reset Release Time	-	440	520	610	µs
T_{RSTPOR}(2)	Power On Reset Release Time	-	-	2500	3000	µs

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. The monitoring voltage of PVD1 is the monitoring voltage when VCC voltage drops; when PVD2LVL[2:0] is set to 0b111, the PVD2 monitoring voltage is the monitoring voltage when the PVD2EXINP voltage drops, and when PVD2LVD[2:0] is set to a value other than 0b111, the PVD2 monitoring voltage is the monitoring voltage when the VCC voltage drops.
4. The hysteresis of PVD1/2 is the difference between the monitoring voltages when VCC or PVD2EXINP rises and falls.

   PVD1 monitoring voltage when VCC rises $=V_{PVD1}+V_{pvd}hyst$;

   PVD2 monitoring voltage when VCC or PVD2EXINP rises $=V_{PVD2}+V_{pvd}hyst$.
5. When PVD2LVDL[2:0]=0b111, the comparison voltage is the external input comparison voltage of PVD2EXINP pin.

4.3.4 Supply Current Characteristics

Current consumption is affected by many parameters and factors, including operating voltage, ambient temperature, I/O pin load, device software configuration, operating frequency, I/O pin switching rate, program location in memory and running code.

Figure 4-3 : Current Consumption Measurement Solution describes the measurement method of current consumption. The measured values of current consumption in various modes described in this section are obtained by a set of test codes running in FLASH under laboratory conditions.

The specific conditions are as follows:

1. All I/O pins are in high impedance mode (no load).
2. Clock frequency selects high-speed mode f_{HCLK}=200MHz/100MHz/24MHz and ultra-low-speed mode f_{HCLK}=8MHz/1MHz.

3. The power consumption modes are divided into: normal operating mode ICC_RUN, Sleep mode ICC_SLEEP, Stop mode ICC_STP, Power-down mode ICC_PD, Dhrystone operating mode ICC_DHRY-STONE.
4. Please refer to the specific current condition description for peripheral clock ON/OFF.
5. In high-speed mode f_{HCLK}=200MHz/100MHz, the PLL is in the enabled state.

Table 4-7 High Speed Mode Current Consumption 1

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=200MHz T_A=-40℃ V_{CC}=3.3V	-	23	-	mA
	While (1), all peripherals clock ON		-	37	-	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	24	-	mA
	CACHE ON		-	24	-	mA
ICC_SLEEP	All peripherals clock OFF		-	14	-	mA
	All peripherals clock ON		-	28	-	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=200MHz T_A=25℃ V_{CC}=3.3V	-	23	-	mA
	While (1), all peripherals clock ON		-	37	-	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	24	-	mA
	CACHE ON		-	24	-	mA
ICC_SLEEP	All peripherals clock OFF		-	14	-	mA
	All peripherals clock ON		-	28	-	mA
ICC_RUN(1)	While (1), all peripherals clock OFF	f_{HCLK}=200MHz T_A=85℃ V_{CC}=1.8-3.6V	-	-	29	mA
	While (1), all peripherals clock ON		-	-	43	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	-	30	mA
	CACHE ON		-	-	30	mA
ICC_SLEEP(1)	All peripherals clock OFF		-	-	20	mA
	All peripherals clock ON		-	-	34	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=200MHz T_A=105℃ V_{CC}=1.8-3.6V	-	-	33	mA
	While (1), all peripherals clock ON		-	-	48	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	-	34	mA
	CACHE ON		-	-	34	mA
ICC_SLEEP	All peripherals clock OFF		-	-	24	mA
	All peripherals clock ON		-	-	39	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-8 High Speed Mode Current Consumption 2(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=100MHz T_A=-40℃ V_{CC}=3.3V	-	12	-	mA
	While (1), all peripherals clock ON		-	20	-	mA
ICC_DHRYSTONE	CACHE OFF		-	13	-	mA
	CACHE ON		-	13	-	mA
ICC_SLEEP	All peripherals clock OFF		-	8	-	mA
	All peripherals clock ON		-	15	-	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=100MHz T_A=25℃ V_{CC}=3.3V	-	13	-	mA
	While (1), all peripherals clock ON		-	20	-	mA
ICC_DHRYSTONE	CACHE OFF		-	14	-	mA
	CACHE ON		-	14	-	mA
ICC_SLEEP	All peripherals clock OFF		-	8	-	mA
	All peripherals clock ON		-	16	-	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=100MHz T_A=85℃ V_{CC}=1.8-3.6V	-	-	19	mA
	While (1), all peripherals clock ON		-	-	27	mA
ICC_DHRYSTONE	CACHE OFF		-	-	20	mA
	CACHE ON		-	-	20	mA
ICC_SLEEP	All peripherals clock OFF		-	-	14	mA
	All peripherals clock ON		-	-	22	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=100MHz T_A=105℃ V_{CC}=1.8-3.6V	-	-	23	mA
	While (1), all peripherals clock ON		-	-	31	mA
ICC_DHRYSTONE	CACHE OFF		-	-	24	mA
	CACHE ON		-	-	24	mA
ICC_SLEEP	All peripherals clock OFF		-	-	18	mA
	All peripherals clock ON		-	-	27	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-9 High Speed Mode Current Consumption 3(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=24MHz T_A=-40℃ V_{CC}=3.3V	-	4	-	mA
	While (1), all peripherals clock ON		-	8	-	mA
ICC_DHRYSTONE	CACHE OFF		-	5	-	mA
ICC_SLEEP	All peripherals clock OFF		-	3	-	mA
	All peripherals clock ON		-	6	-	mA

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=24MHz T_A=25℃ V_{CC}=3.3V	-	4	-	mA
	While (1), all peripherals clock ON		-	8	-	mA
ICC_DHRYSTONE	CACHE OFF		-	5	-	mA
ICC_SLEEP	All peripherals clock OFF		-	3	-	mA
	All peripherals clock ON		-	7	-	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=24MHz T_A=85℃ V_{CC}=1.8-3.6V	-	-	10	mA
	While (1), all peripherals clock ON		-	-	14	mA
ICC_DHRYSTONE	CACHE OFF		-	-	12	mA
ICC_SLEEP	All peripherals clock OFF		-	-	9	mA
	All peripherals clock ON		-	-	13	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=24MHz T_A=105℃ V_{CC}=1.8-3.6V	-	-	15	mA
	While (1), all peripherals clock ON		-	-	19	mA
ICC_DHRYSTONE	CACHE OFF		-	-	17	mA
ICC_SLEEP	All peripherals clock OFF		-	-	14	mA
	All peripherals clock ON		-	-	18	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-10 Ultra-low Speed Mode Current Consumption 1

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=8MHz T_A=-40℃ V_{CC}=3.3V	-	2	-	mA
	While (1), all peripherals clock ON		-	4	-	mA
ICC_DHRYSTONE	CACHE OFF(1)		-	2.2	-	mA
ICC_SLEEP	All peripherals clock OFF		-	1	-	mA
	All peripherals clock ON		-	3	-	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=8MHz T_A=25℃ V_{CC}=3.3V	-	2	-	mA
	While (1), all peripherals clock ON		-	4	-	mA
ICC_DHRYSTONE	CACHE OFF(1)		-	2.3	-	mA
ICC_SLEEP	All peripherals clock OFF		-	1	-	mA
	All peripherals clock ON		-	3	-	mA
ICC_RUN(1)	While (1), all peripherals clock OFF	f_{HCLK}=8MHz T_A=85℃ V_{CC}=1.8-3.6V	-	-	5	mA
	While (1), all peripherals clock ON		-	-	7	mA
ICC_DHRYSTONE	CACHE OFF(1)		-	-	5.5	mA
ICC_SLEEP(1)	All peripherals clock OFF		-	-	4.6	mA
	All peripherals clock ON		-	-	6.7	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=8MHz T_A=105℃	-	-	8	mA

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
	While (1), all peripherals clock ON	V_{CC}=1.8-3.6V	-	-	10	mA
ICC_DHRYSTONE	CACHE OFF(1)		-	-	9	mA
ICC_SLEEP	All peripherals clock OFF		-	-	7.5	mA
	All peripherals clock ON		-	-	9.5	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-11 Ultra-low Speed Mode Current Consumption 2(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=1MHz T_A=-40℃ V_{CC}=3.3V	-	1	-	mA
	While (1), all peripherals clock ON		-	2.5	-	mA
ICC_DHRYSTONE	CACHE OFF		-	1	-	mA
ICC_SLEEP	All peripherals clock OFF		-	0.5	-	mA
	All peripherals clock ON		-	2	-	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=1MHz T_A=25℃ V_{CC}=3.3V	-	1	-	mA
	While (1), all peripherals clock ON		-	2.5	-	mA
ICC_DHRYSTONE	CACHE OFF		-	1	-	mA
ICC_SLEEP	All peripherals clock OFF		-	0.7	-	mA
	All peripherals clock ON		-	2.2	-	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=1MHz T_A=85℃ V_{CC}=1.8-3.6V	-	-	4.5	mA
	While (1), all peripherals clock ON		-	-	6	mA
ICC_DHRYSTONE	CACHE OFF		-	-	4.7	mA
ICC_SLEEP	All peripherals clock OFF		-	-	4.3	mA
	All peripherals clock ON		-	-	5.9	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=1MHz T_A=105℃ V_{CC}=1.8-3.6V	-	-	7.5	mA
	While (1), all peripherals clock ON		-	-	9	mA
ICC_DHRYSTONE	CACHE OFF		-	-	8	mA
ICC_SLEEP	All peripherals clock OFF		-	-	7	mA
	All peripherals clock ON		-	-	8.8	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-12 Low Power Mode Current Consumption

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_STP (Stop mode)	PWC_PWRC1.STPDAS=0b00	T_A=-40℃ V_{CC}=3.3V	-	188	-	μA
	PWC_PWRC1.STPDAS=0b11		-	45	-	μA
	PWC_PWRC1.STPDAS=0b00	T_A=25℃ V_{CC}=3.3V	-	455	-	μA
	PWC_PWRC1.STPDAS=0b11		-	304	-	μA

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_STP (Stop mode)	PWC_PWRC1.STPDAS=0b00(1)	T_A=85℃ V_{CC}=1.8-3.6V	-	-	3.9	mA
	PWC_PWRC1.STPDAS=0b11(1)		-	-	3.6	mA
	PWC_PWRC1.STPDAS=0b00	T_A=105℃ V_{CC}=1.8-3.6V	-	-	6.5	mA
	PWC_PWRC1.STPDAS=0b11		-	-	6.2	mA
ICC_PD Power-down mode 1	Power-down mode 1	T_A=-40℃ V_{CC}=3.3V	-	10	-	μA
	Power-down mode 2		-	4	-	μA
	Power-down mode 3		-	1.7	-	μA
	Power-down mode 4		-	1.7	-	μA
	Power-down mode 2+XTAL32+RTC(1)		-	6	-	μA
	Power-down mode 2+LRC+RTC(1)		-	9	-	μA
	Power-down mode 2+XTAL32+RTC+Ret RAM(1)		-	6	-	μA
	Power-down mode 1	T_A=25℃ V_{CC}=3.3V	-	11	-	μA
	Power-down mode 2		-	4.5	-	μA
	Power-down mode 3		-	2.1	-	μA
	Power-down mode 4		-	2.1	-	μA
	Power-down mode 2+XTAL32+RTC(1)		-	7	-	μA
	Power-down mode 2+LRC+RTC(1)		-	9	-	μA
	Power-down mode 2+XTAL32+RTC+Ret RAM(1)		-	7	-	μA
	Power-down mode 1(1)	T_A=85℃ V_{CC}=1.8-3.6V	-	-	20	μA
	Power-down mode 2(1)		-	-	18	μA
	Power-down mode 3(1)		-	-	11	μA
	Power-down mode 4(1)		-	-	11	μA
	Power-down mode 2+XTAL32+RTC(1)		-	-	20	μA
	Power-down mode 2+LRC+RTC(1)		-	-	20	μA
	Power-down mode 2+XTAL32+RTC+Ret RAM(1)		-	-	21	μA
	Power-down mode 1	T_A=105℃ V_{CC}=1.8-3.6V	-	-	31	μA
	Power-down mode 2		-	-	29	μA
	Power-down mode 3		-	-	21	μA
	Power-down mode 4		-	-	21	μA
	Power-down mode 2+XTAL32+RTC(1)		-	-	31	μA
	Power-down mode 2+LRC+RTC(1)		-	-	31	μA
	Power-down mode 2+XTAL32+RTC+Ret RAM(1)		-	-	32	μA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-13 Analog Module Current Consumption(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_MODULE	XTAL oscillation mode high drive 24MHz	T_A=25℃ V_{CC}=V_{AVCC}=3.3V	-	1.8	-	mA
	Oscillation mode medium drive 16MHz		-	1.0	-	mA
	Oscillation mode low drive 10MHz		-	0.8	-	mA
	Oscillation mode ultra-low drive 8MHz		-	0.6	-	mA
	XTAL 32.768kHz		-	1.1	-	μA
	HRC		-	0.3	-	mA
	PLLH (VCO=1200MHz)		-	3.5	-	mA
	PLLH (VCO=600MHz)		-	1.8	-	mA
	ADC		-	1.3	-	mA
	DAC (Amplifier Enabled)		-	0.8	-	mA
	DAC (Amplifier Disabled)		-	0.2	-	mA
	CMP		-	0.3	-	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.5 Low Power Mode Wake-up Timing

Wake-up time is measured from the trigger of wake-up event to the first command executed by CPU:

- For Stop or Sleep mode: the wake-up event is WFE.
- The WKUP pin is used to wake up from Power-down, Stop and Sleep modes. All time series are measured at ambient temperature V_{CC}=3.3V.

Table 4-14 Low Power Mode Wake-up Time(2)

Symbol	Parameters	Conditions	Typ	Max	Unit
T_{STOP}	Wake up from Stop mode	The system clock is MRC	8	15	μs
T_{PD1}(1)	Wake up from Power-down mode 1	The total capacity of VCAP_1 is 0.094μF or 0.1μF	25	35	μs
		The total capacity of VCAP_1 is 0.2μF or 0.22μF	30	40	μs
T_{PD2}(1)	Wake up from Power-down mode 2	The total capacity of VCAP_1 is 0.094μF or 0.1μF	70	80	μs
		The total capacity of VCAP_1 is 0.2μF or 0.22μF	75	85	μs
T_{PD3}(1)	Wake up from Power-down mode 3	The total capacity of VCAP_1 is 0.094μF or 0.1μF	2500	3000	μs
		The total capacity of VCAP_1 is 0.2μF or 0.22μF	2500	3000	μs

Symbol	Parameters	Conditions	Typ	Max	Unit
T_{PD4}(1)	Wake up from Power-down mode 4	The total capacity of VCAP_1 is 0.094μF or 0.1μF	130	140	μs
		The total capacity of VCAP_1 is 0.2μF or 0.22μF	140	150	μs

Note

1. The total capacity of VCAP_1 of the chip must match the assignment of PWC_PWRC1.PDTS bit. When the total capacity of VCAP_1 is 0.2μF or 0.22μF, it is necessary to ensure that the PWC_PWRC1.PDTS bit is cleared before entering Power-down mode. When the total capacity of VCAP_1 is 0.094μF or 0.1μF, ensure that PWC_PWRC1.PDTS position bit is set before entering the Power-down mode.
2. Resulted from comprehensive evaluation, not tested in production.

4.3.6 External Clock Source Characteristics

4.3.6.1 High-Speed External Clock Generated by External Source

In bypass mode, XTAL oscillator is disabled and the input pin is standard I/O. The external clock signal must comply with the external input clock characteristics specified in the table below.

Table 4-15 High-Speed External Clock Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{XTAL_EXT}	User external clock source frequency	-	1(1)	-	25	MHz
V_{IH_XTAL}(1)	XTAL_EXT input pin high level voltage	-	0.8*V_{CC}	-	V_{CC}	V
V_{IL_XTAL}(1)	XTAL_EXT input pin low level voltage	-	V_{SS}	-	0.2*V_{CC}	V
$t_{r(XTAL)}$(1) $t_{f(XTAL)}$(1)	XTAL_EXT rise or fall time	-	-	-	5	ns
$Duty_{(XTAL)}$(1)	Duty Cycle	-	40	-	60	%

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.6.2 High-Speed External Clock Generated by Crystal Oscillator/Ceramic Resonator

The high-speed external (XTAL) clock can be generated by a crystal oscillator/ceramic resonant oscillator with a frequency of 4-25MHz. In application, the resonator and load capacitor must be as close as possible to the pin of oscillator, so as to minimize the output distortion and the stabilization time. For detailed information about resonator characteristics (frequency, package, accuracy, etc.), please consult the crystal resonator manufacturer.

Table 4-16 XTAL 4-25MHz Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{XTAL_IN}(1)	Oscillator Frequency	-	4	-	25	MHz
R_F	Feedback Resistance	-	-	300	-	kΩ

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
A_{XTAL} (2)(3)	XTAL Precision	-	-500	-	500	ppm
G_{mmax} (2)	Oscillator Gm	Oscillator start	4	-	-	mA/V
$t_{SU(XTAL)}$ (1)(4)	Startup Time	V_{CC} stable, crystal oscillator =8MHz.	-	2.0	-	ms
		V_{CC} stable, crystal oscillator =4MHz.	-	4.0	-	ms

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. This parameter depends on the resonator used in the application system.
4. $t_{SU(XTAL)}$ is the oscillation starting time, that is, the time from the software enabling XTAL to the stable 8MHz oscillation frequency. This value is measured based on a standard crystal resonator, and may vary significantly depending on the crystal oscillator manufacturer.

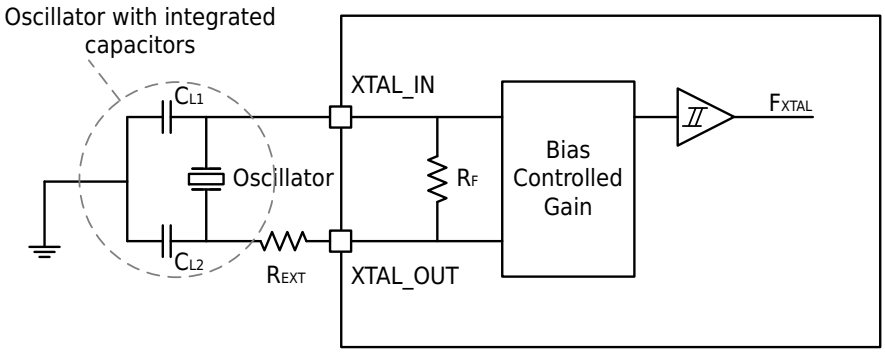


Figure 4-4 Typical application of 8MHz crystal oscillator

Note

- For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors designed for high-frequency applications, which can meet the requirements of crystal oscillator or resonator (see the figure above). C_{L1} and C_{L2} usually have the same size. C_{L1}=C_{L2}=2*(C_L-C_S). C_S represents the total parasitic capacitance between the PCB and MCU pins (XTAL_IN, XTAL_OUT). C_L denotes the load capacitance of the crystal oscillator or ceramic resonator, please consult the crystal oscillator manufacturer for details.
- The value of R_{EXT} depends on the crystal oscillation characteristics.

4.3.6.3 Low-Speed External Clock Generated by Crystal Oscillator/Ceramic Resonator

The low-speed external (XTAL32) clock can be generated by an oscillator composed of a crystal oscillator/ceramic resonator with a frequency of 32.768kHz. In application, the resonator and load capacitor must be as close as possible to the pin of oscillator, so as to minimize the output distortion and the stabilization time. For detailed information about resonator characteristics (frequency, package, accuracy, etc.), please consult the crystal resonator manufacturer.

Table 4-17 XTAL32 Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
F_{XTAL32} (1)	Frequency	-	-	32.768	-	kHz
R_F	Feedback resistance	-	-	15	-	MΩ
I_{DD_XTAL32} (1)	Power consumption	XTAL32DRV[2:0]=0b000	-	0.8	-	μA
A_{XTAL32} (2)(3)	XTAL32 accuracy	-	-500	-	500	ppm
G_{mmax} (2)	Oscillator G_m	XTAL32DRV[2:0]=0b000	5.6	-	-	μA/V
$T_{SUXTAL32}$ (1) (4)	Startup time	Under V_{CC} steady state	-	2	-	s

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. This parameter depends on the resonator used in the application system.
4. $T_{SUXTAL32}$ is the oscillation starting time, that is, the time from the software enabling XTAL32 to the stable 32.768kHz oscillation frequency. This value is measured based on a standard crystal resonator, and may vary significantly depending on the crystal oscillator manufacturer.

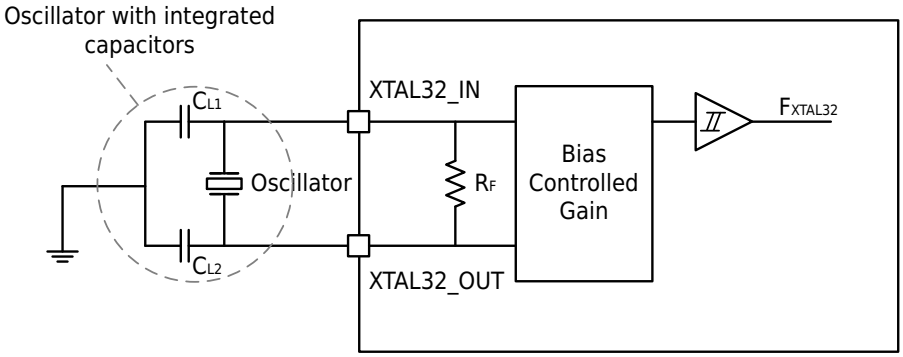


Figure 4-5 Typical application of 32.768kHz crystal oscillator

Note

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors (see the figure above). C_{L1} and C_{L2} usually have the same size, $C_{L1}=C_{L2}=2*(C_L-C_S)$. C_S represents the total parasitic capacitance between PCB and MCU pins (XTAL32_IN, XTAL32_OUT). If C_{L1} or C_{L2} is greater than 18pF, it is recommended to set XTAL32DRV=0b001 (high drive, typical power consumption increases by 0.2μA). C_L denotes the load capacitance of crystal resonator or ceramic resonator, please consult the crystal resonator manufacturer for details.

4.3.7 Internal Clock Source Characteristics

4.3.7.1 HRC

Table 4-18 HRC Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{HRC}	Frequency	Mode 1	-	16	-	MHz
		Mode 2	-	20	-	
	The user adjusts the scale(1)	-	-	-	0.2	%
	Frequency Accuracy	T_A=-40-105℃	-2	-	2	%
		T_A=-20-105℃(1)	-1.5	-	1.5	%
$t_{st(HRC)}$	HRC oscillation stabilization time	-	-	-	15	μs

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.7.2 MRC

Table 4-19 MRC Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{MRC}	Frequency	-	7.2	8	8.8	MHz
$t_{st(MRC)}$	MRC oscillator stabilization time	-	-	-	3	μs

4.3.7.3 LRC

Table 4-20 LRC Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{LRC}	Frequency	-	27.853	32.768	37.683	kHz
$t_{st(LRC)}$	LRC oscillator stabilization time	-	-	-	36	μs

4.3.7.4 SWDTLRC

Table 4-21 SWDTLRC Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$f_{SWDTLRC}$	Frequency	-	9	10	11	kHz
$t_{st(SWDTLRC)}$	SWDTLRC oscillator stabilization time	-	-	-	57.1	μs

4.3.8 PLL Characteristics

Table 4-22 System PLL (PLLH) Main Performance Indicators

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}(2)	Input clock of PLL phase detector (PFD)	-	4	-	25	MHz
f_{PLL_OUT}(1)	Output clock of PLL multiplier	-	37.5	-	600	MHz
f_{VCO_OUT}	PLL voltage controlled oscillator (VCO) output	-	600	-	1200	MHz
$Jitter_{PLL}$(1)	Periodic jitter	The input clock of PLL PFD is 8MHz, and the system clock is 120MHz, peak to peak.	-	±70	-	ps
	Jitter during adjacent periods	The input clock of PLL PFD is 8MHz, and the system clock is 120MHz, peak to peak.	-	±100	-	ps
t_{LOCK}(1)	PLL lock time	-	-	80	120	μs

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. It is recommended to use a higher input clock to obtain jittering characteristics.

4.3.9 Memory (Flash) Characteristics

When the device is delivered to the customer, the flash memory has been erased.

Table 4-23 Flash Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
I_{VCC}(1)	Supply current	Read mode, V_{CC}=1.8-3.6V	-	-	5	mA
		Programming mode, V_{CC}=1.8-3.6V	-	-	10	mA
		Block erase mode, V_{CC}=1.8-3.6V	-	-	10	mA
		Full erase mode, V_{CC}=1.8-3.6V	-	-	10	mA

Note

1. Guaranteed by design, not tested in production.

Table 4-24 Flash Programming Erase Time(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
T_{prog}	Word programming time	Single programming mode	$43+2*t_{HCLK}$	$48+4*t_{HCLK}$	$53+6*t_{HCLK}$	μs
	Word programming time	Continuous programming mode	$12+2*t_{HCLK}$	$14+4*t_{HCLK}$	$16+6*t_{HCLK}$	μs
T_{erase}	Block erase time	-	$16+2*t_{HCLK}$	$18+4*t_{HCLK}$	$20+6*t_{HCLK}$	ms
T_{mas}	Full erase time	-	$16+2*t_{HCLK}$	$18+4*t_{HCLK}$	$20+6*t_{HCLK}$	ms

Note

1. Guaranteed by design, not tested in production.
2. t_{HCLK} is 1 period of CPU clock.

Table 4-25 Flash Erase Write Times and Data Storage Period(1)

Symbol	Parameters	Conditions		Min	Typ	Unit
N_{end}	Program, Block Erase times	T_A=-40℃ -105℃	Data Storage Period (T_{ret}): 10 years, T_A=85℃	-	100000	times
			Data Storage Period (T_{ret}): 20 years, T_A=85℃	10000	-	times

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.10 Electrical Sensitivity

Different tests (ESD, LU) are carried out on the chip by using specific measurement methods to determine its electrical sensitivity.

4.3.10.1 ESD Characteristics

According to each pin combination, electrostatic discharge is applied to the pin of each sample. This test conforms to ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 standards.

Table 4-26 ESD Characteristics(1)

Symbol	Parameters	Conditions	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human model)	T_A=+25℃, compliant with ANSI/ESDA/JEDEC JS-001	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charging device model)	T_A=+25℃, compliant with ANSI/ESDA/JEDEC JS-002	1000	V

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.10.2 Static Latch-up Characteristics

To evaluate the static Latch-up performance, two complementary static Latch-up tests are needed to be performed on the chip:

- Apply overvoltage to each power supply and analog input pin.
- Apply current injection to other inputs, outputs and configurable I/O pins.

These tests conform to EIA/JESD 78A IC Latch-up standard.

Table 4-27 Static Latch-up Characteristics(1)

Symbol	Parameters	Conditions	Max	Unit
LU	Static Latch-up	T_A=+105℃, compliant with JESD78A standard	200	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.11 I/O Port Characteristics

General-Purpose Input/Output Characteristics

Table 4-28 I/O Static Characteristics

Symbol	Parameters		Conditions	Min	Typ	Max	Unit
V_{IL}	Schmitt input low level		1.8≤V_{CC}≤3.6	-	-	0.3V_{CC}	V
V_{IH}	Schmitt input high level		1.8≤V_{CC}≤3.6	0.7V_{CC}	-	-	V
V_{HYS}(1)	Schmitt input hysteresis		1.8≤V_{CC}≤3.6	0.1	0.2	-	V
V_{IL}	CMOS input low level		1.8≤V_{CC}≤3.6	-	-	0.3V_{CC}	V
V_{IH}	CMOS input high level		1.8≤V_{CC}≤3.6	0.7V_{CC}	-	-	V
TTL_V_{IL}	CMOS/Schmitt compatible with TTL Input low level		2.7≤V_{CC}≤3.6	-	-	0.8	V
TTL_V_{IH}	CMOS/Schmitt compatible with TTL Input high level		2.7≤V_{CC}≤3.6	2.2	-	-	V
$F_{max(in)}$(1)	Maximum input frequency for Schmitt		2.7≤V_{CC}≤3.6	-	-	40	MHz
			1.8≤V_{CC}<2.7	-	-	20	MHz
	Maximum input frequency for CMOS		2.7≤V_{CC}≤3.6	-	-	80	MHz
			1.8≤V_{CC}<2.7	-	-	40	MHz
I_{LKG}	I/O input leakage current		V_{SS}≤V_{IN}≤V_{CC}	-	-	1	μA
			V_{IN}=5.5V(2)	-	-	10	μA
R_{PU}(3)	Weak pull up Equivalent resistance		V_{IN}=V_{SS} 1.8≤V_{CC}≤3.6	10	30	150	kΩ
R_{PD}(3)	Weak pull down Equivalent resistance		V_{IN}=V_{CC} 1.8≤V_{CC}≤3.6	5	20	50	kΩ
C_{IO}(2)	I/O pin capacitance	PB11/MD	-	-	10	-	pF
		Input pins other than above	-	-	5	-	pF

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. To keep the voltage above V_{CC}+0.3V, the internal pull-up/pull-down resistors must be disabled.

Output Current

GPIO can provide the maximum pull current or sink current of ±20mA.

Output Voltage

Table 4-29 Output Voltage Characteristics

Driver	Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Low drive	V_{OL}(1)	Low level output	I_{IO}=±1.5mA 1.8≤V_{CC}<2.7	-	-	0.6	V
	V_{OH}(2)	High level output		V_{CC}-0.6	-	-	V
	V_{OL}(1)	Low level output	I_{IO}=±3mA 2.7≤V_{CC}≤3.6	-	-	0.6	V
	V_{OH}(2)	High level output		V_{CC}-0.6	-	-	V
	V_{OL}(1)	Low level output	I_{IO}=±6mA 2.7≤V_{CC}≤3.6	-	-	1.3	V
	V_{OH}(2)	High level output		V_{CC}-1.3	-	-	V
Medium drive	V_{OL}(1)	Low level output	I_{IO}=±3mA 1.8≤V_{CC}<2.7	-	-	0.4	V
	V_{OH}(2)	High level output		V_{CC}-0.4	-	-	V
	V_{OL}(1)	Low level output	I_{IO}=±5mA 2.7≤V_{CC}≤3.6	-	-	0.4	V
	V_{OH}(2)	High level output		V_{CC}-0.4	-	-	V
	V_{OL}(1)	Low level output	I_{IO}=±12mA 2.7≤V_{CC}≤3.6	-	-	1.3	V
	V_{OH}(2)	High level output		V_{CC}-1.3	-	-	V
High drive	V_{OL}(1)	Low level output	I_{IO}=±6mA 1.8≤V_{CC}<2.7	-	-	0.4	V
	V_{OH}(2)	High level output		V_{CC}-0.4	-	-	V
	V_{OL}(1)	Low level output	I_{IO}=±8mA 2.7≤V_{CC}≤3.6	-	-	0.4	V
	V_{OH}(2)	High level output		V_{CC}-0.4	-	-	V
	V_{OL}(1)	Low level output	I_{IO}=±20mA 2.7≤V_{CC}≤3.6	-	-	1.3	V
	V_{OH}(2)	High level output		V_{CC}-1.3	-	-	V
	V_{OL}(1)	Low level output	I_{IO}=±20mA 3.0≤V_{CC}≤3.6	-	-	0.88	V
	V_{OH}(2)	High level output		V_{CC}-0.88	-	-	V

Note

1. The device's I_{IO} sinking current must always take into account the absolute maximum ratings specified in Table 4-2 : Current Characteristics. The sum of I_{IO} (I/O port and control pin) must not exceed I_{VSS}.
2. The device's I_{IO} pull current must always conform to the absolute maximum ratings specified in Table 4-2 : Current Characteristics. The sum of I_{IO} (I/O port and control pin) must not exceed I_{VCC}.

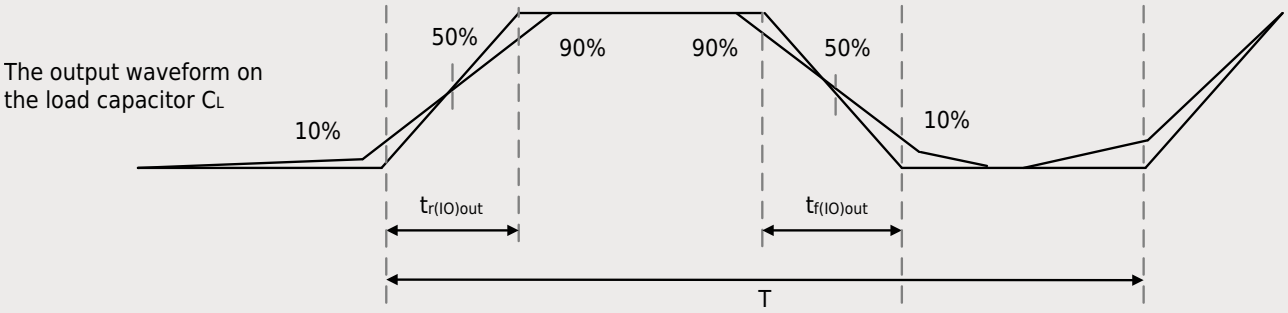
Input/Output AC Characteristics

Table 4-30 I/O AC Characteristics(1)

Driver	Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Low drive	$f_{max(IO)out}$(2)	Maximum frequency	C_L=30pF, V_{CC}≥2.7V	-	-	20	MHz
			C_L=30pF, V_{CC}≥1.8V	-	-	10	
			C_L=10pF, V_{CC}≥2.7V	-	-	40	
			C_L=10pF, V_{CC}≥1.8V	-	-	20	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Rise/Fall Time	C_L=30pF, V_{CC}≥2.7V	-	-	15	ns
			C_L=30pF, V_{CC}≥1.8V	-	-	25	
			C_L=10pF, V_{CC}≥2.7V	-	-	7.5	
			C_L=10pF, V_{CC}≥1.8V	-	-	15	
Medium drive	$f_{max(IO)out}$(2)	Maximum frequency	C_L=30pF, V_{CC}≥2.7V	-	-	45	MHz
			C_L=30pF, V_{CC}≥1.8V	-	-	22.5	
			C_L=10pF, V_{CC}≥2.7V	-	-	90	
			C_L=10pF, V_{CC}≥1.8V	-	-	45	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Rise/Fall Time	C_L=30pF, V_{CC}≥2.7V	-	-	6	ns
			C_L=30pF, V_{CC}≥1.8V	-	-	10	
			C_L=10pF, V_{CC}≥2.7V	-	-	4	
			C_L=10pF, V_{CC}≥1.8V	-	-	6	
High drive	$f_{max(IO)out}$(2)	Maximum frequency	C_L=30pF, V_{CC}≥2.7V	-	-	100	MHz
			C_L=30pF, V_{CC}≥1.8V	-	-	50	
			C_L=10pF, V_{CC}≥1.8V	-	-	100	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Rise/Fall Time	C_L=30pF, V_{CC}≥2.7V	-	-	4	ns
			C_L=30pF, V_{CC}≥1.8V	-	-	6	
			C_L=10pF, V_{CC}≥2.7V	-	-	2.5	
			C_L=10pF, V_{CC}≥1.8V	-	-	3.5	

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. The maximum frequency is defined in the figure below.
3. The load capacitance C_L must take into account the capacitance of both the PCB and the MCU pins. The capacitance between the MD pin (PB11) and the PCB can be roughly estimated as 15 pF, while that of other pins can be estimated as approximately 10 pF.



Maximum frequency condition ($t_r + t_f$) ≤ (2/3)T and Duty cycle= 50% ± 5%
C_L is indicated in the "Conditions" column of the "I/O AC Characteristics" table)

Figure 4-6 I/O AC Characteristics Definition

4.3.12 I2C Interface Characteristics

Table 4-31 I2C Characteristics

Symbol	Parameters	Standard mode (SM)		Fast mode (FM)		Unit
		Min	Max	Min	Max	
f_{SCL} (1)	SCL frequency	0	100	0	400	kHz
$t_{HD;STA}$ (1)	Start condition/restart condition hold time	4.0	-	0.6	-	μs
t_{LOW} (1)	SCL low level	4.7	-	1.3	-	μs
t_{HIGH} (1)	SCL high level	4	-	0.6	-	μs
$t_{SU;STA}$ (1)	Restart condition setup time	4.7	-	0.6	-	μs
$t_{HD;DAT}$	Data hold time	0	-	0	-	μs
$t_{SU;DAT}$	Data setup time	30+t_{I2C_REFCLK} (2)	-	30+t_{I2C_REFCLK} (2)	-	ns
t_R (1)	SCL/SDA rise time	-	1000	-	300	ns
t_F (1)	SCL/SDA fall time	-	300	-	300	ns
$t_{SU;STO}$ (1)	Stop condition setup time	4	-	0.6	-	μs
t_{BUF} (1)	BUS idle time from stop condition to start condition	4.7	-	1.3	-	μs
C_b (1)	Load capacitance	-	400	-	400	pF

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. The t_{I2C_REFCLK}, i.e., the I2C reference clock period, is determined by the I2C_CCR.FREQ bit.

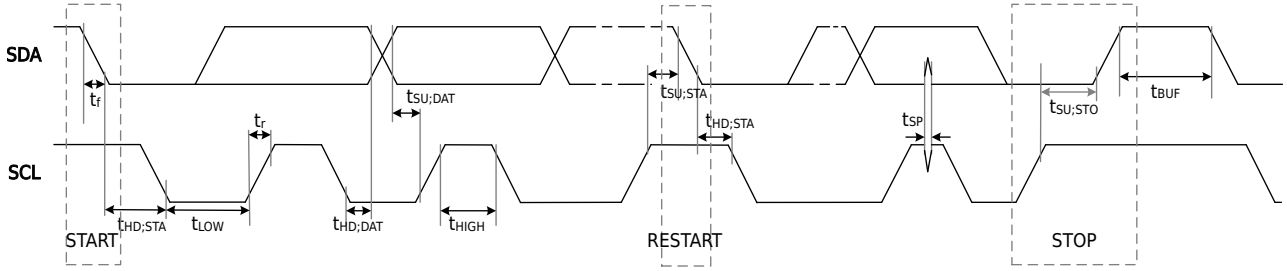


Figure 4-7 I2C Bus Timing Definition

4.3.13 SPI Interface Characteristics

Table 4-32 SPI Characteristics

Symbol	Parameters	Conditions	Min	Max	Unit
t_w(SCKH)(1)	SCK high level time	Master mode(4) 1.8V≤V_{CC}≤3.6V	T_{PCLK1}-1(5)	T_{PCLK1}+1(5)	ns
		Slave mode(4) 1.8V≤V_{CC}≤3.6V	3*T_{PCLK1}-1(5)	3*T_{PCLK1}+1(5)	ns
t_w(SCKL)(1)	SCK low level time	Master mode(4) 1.8V≤V_{CC}≤3.6V	T_{PCLK1}-1(5)	T_{PCLK1}+1(5)	ns
		Slave mode(4) 1.8V≤V_{CC}≤3.6V	3*T_{PCLK1}-1(5)	3*T_{PCLK1}+1(5)	ns
t_{su}(SI)	Data input setup time	Slave mode 1.8V≤V_{CC}≤3.6V	4	-	ns
t_h(SI)	Data input hold time	Slave mode 1.8V≤V_{CC}≤3.6V	3	-	ns
t_v(SO)	Data output active time	Slave mode 2.7V≤V_{CC}≤3.6V	-	15	ns
		Slave mode 1.8V≤V_{CC}<2.7V	-	26	ns
t_{su}(MI)	Data input setup time	Master mode 2.7V≤V_{CC}≤3.6V	5	-	ns
		Master mode 1.8V≤V_{CC}<2.7V	9	-	ns
t_h(MI)	Data input hold time	Master mode 2.7V≤V_{CC}≤3.6V	5	-	ns
		Master mode 1.8V≤V_{CC}<2.7V	15	-	ns

Symbol	Parameters	Conditions	Min	Max	Unit
$t_{su}(SS)^{(1)}$	SS setup time	Slave mode 1.8V≤V_{CC}≤3.6V	$6*T_{PCLK1}^{(5)}$	-	ns
		Master mode 2.7V≤V_{CC}≤3.6V	$-5+N*T_{SCK}^{(2)(5)}$	-	ns
		Master mode 1.8V≤V_{CC}<2.7V	$-10+N*T_{SCK}^{(2)(5)}$	-	ns
$t_h(SS)^{(1)}$	SS hold time	Slave mode 1.8V≤V_{CC}≤3.6V	$6*T_{PCLK1}^{(5)}$	-	ns
		Master mode 2.7V≤V_{CC}≤3.6V	$-5+N*T_{SCK}^{(3)(5)}$	-	ns
		Master mode 1.8V≤V_{CC}<2.7V	$-10+N*T_{SCK}^{(3)(5)}$	-	ns
t_v(MO)	Data output active time	Master mode 2.7V≤V_{CC}≤3.6V	-	4	ns
		Master mode 1.8V≤V_{CC}≤2.7V	-	9	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. N=1-8, determined by register SPI_CFG1.MSSI.
3. N=1-8, determined by register SPI_CFG1.MSSDL.
4. The values of t_w(SCKH) and t_w(SCKL) are determined by SPI_CFG2.MBR, and the values listed in the table are the values of SPI_CFG2.MBR=0.
5. T_{PCLK1} refers to 1 period of clock PCLK1, and T_{SCK} refers to 1 period of SPI communication clock.

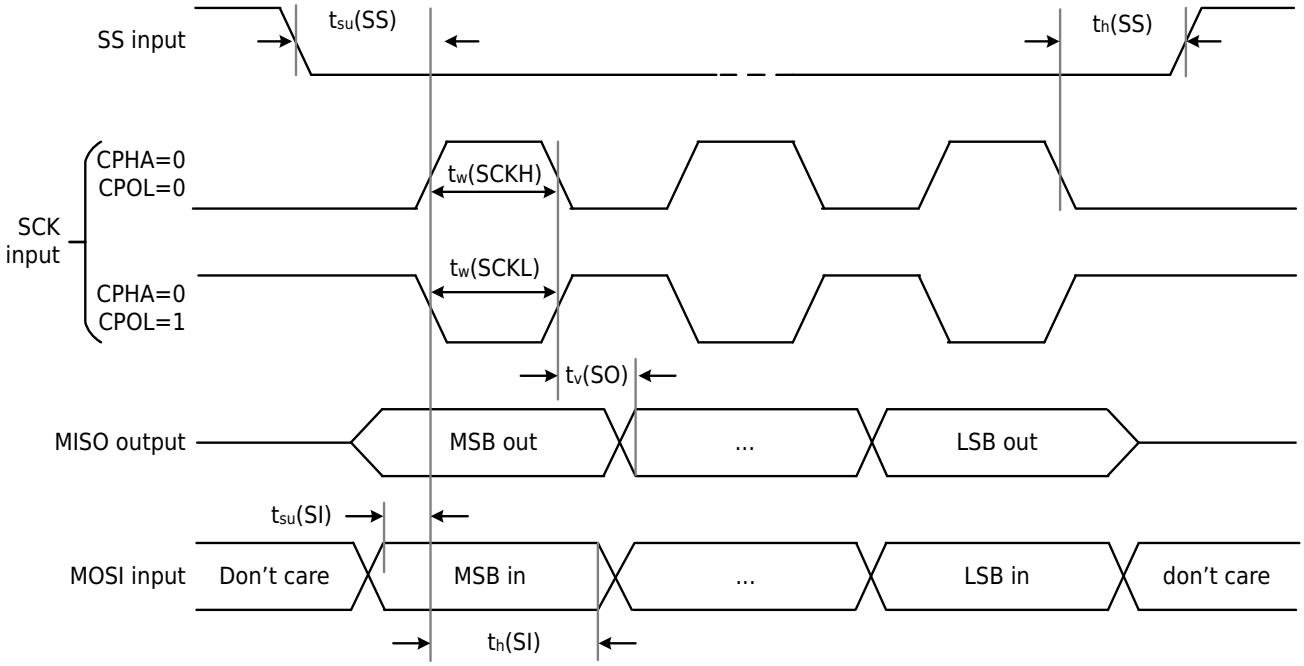


Figure 4-8 SPI Timing Definition (Slave mode, CPHA=0)

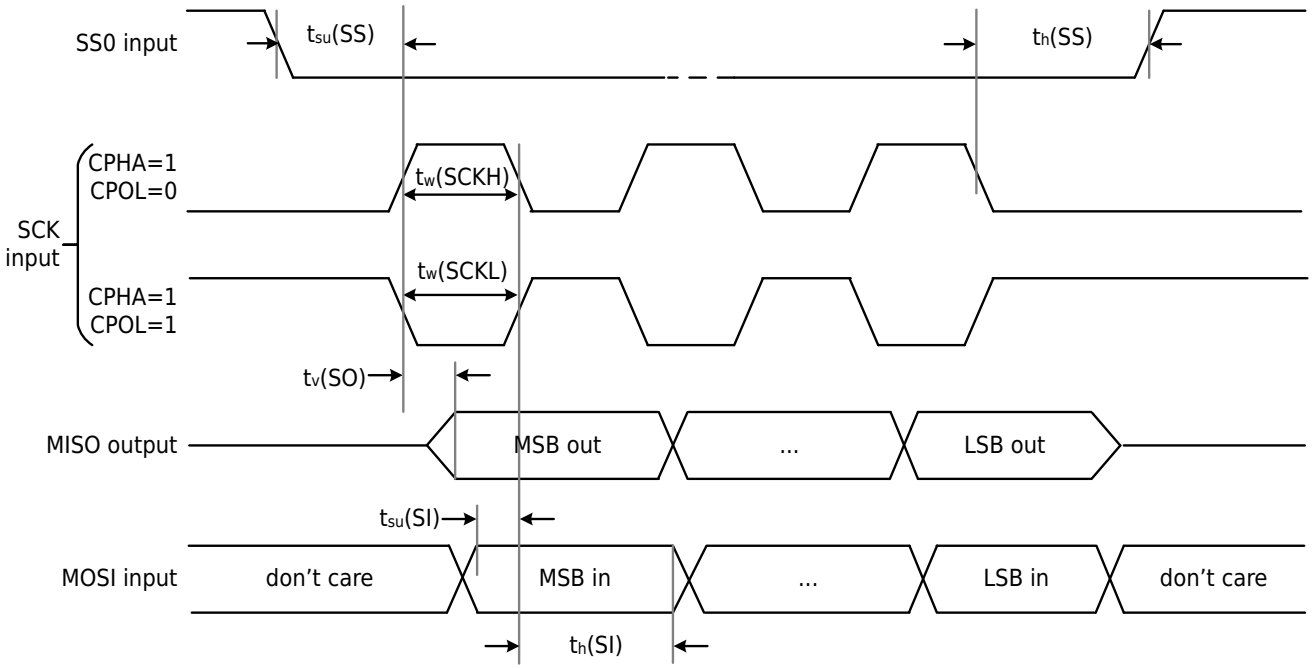


Figure 4-9 SPI Timing Definition (Slave mode, CPHA=1)

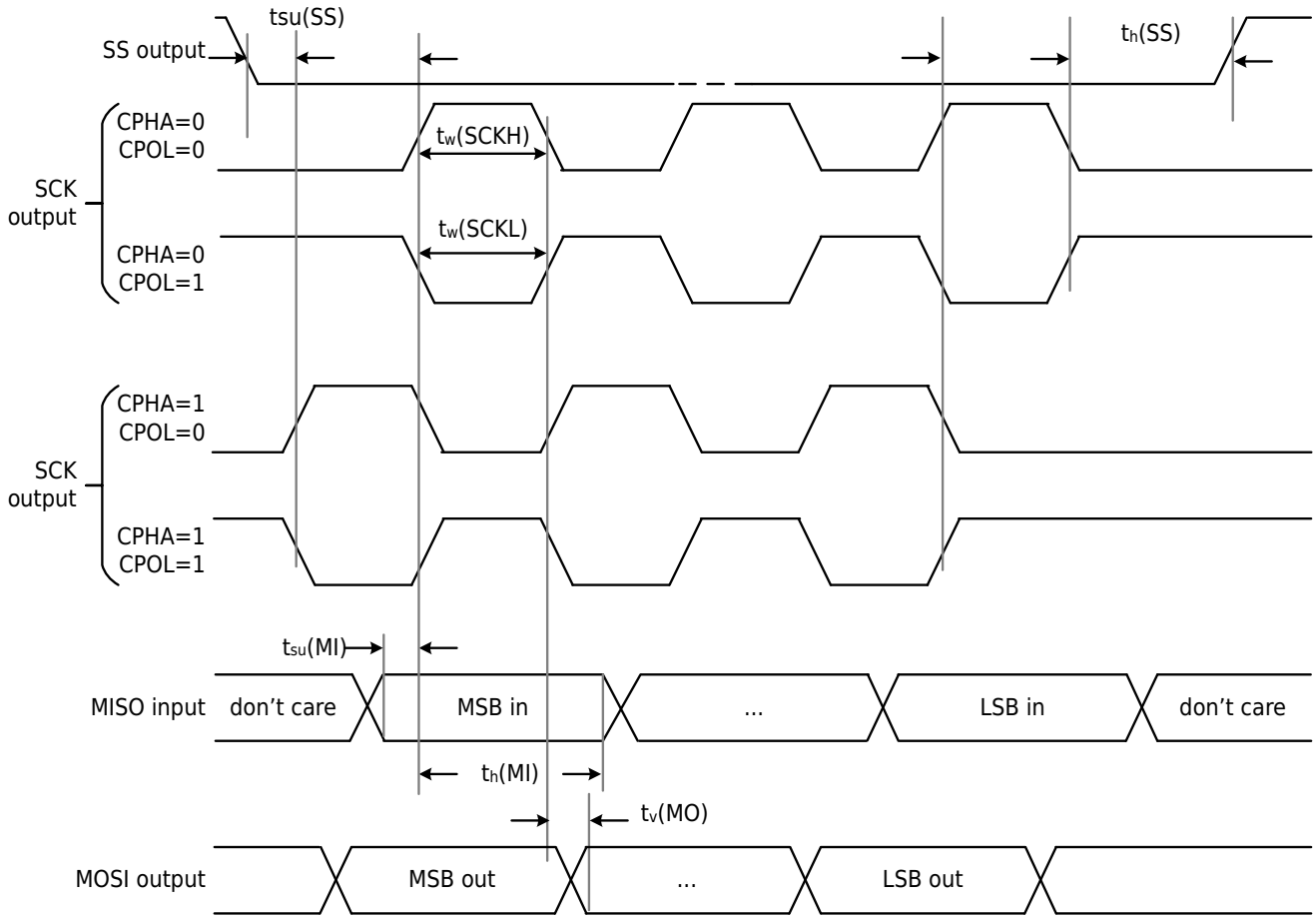


Figure 4-10 SPI Timing Definition (Master mode)

4.3.14 QSPI Interface Characteristics

Table 4-33 QSPI Characteristics

Symbol	Parameters	Conditions	Min	Max	Unit
t_{QSCYC}(1)	SCK clock periods	-	2	48	t_{HCLK}
t_{QSWH}(1)	SCK high level	-	t_{QSCYC}*0.4	-	ns
t_{QSWL}(1)	SCK low level	-	t_{QSCYC}*0.4	-	ns
t_{SU}	Data input setup time	1.8V≤V_{CC}≤3.6V	5	-	ns
t_{IH}	Data input hold time	2.7V≤V_{CC}≤3.6V	5	-	ns
		1.8V≤V_{CC}<2.7V	15	-	ns
t_{OD}	Data output delay	-	-	4	ns
t_{OH}(1)	Data output hold time	-	0	-	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.

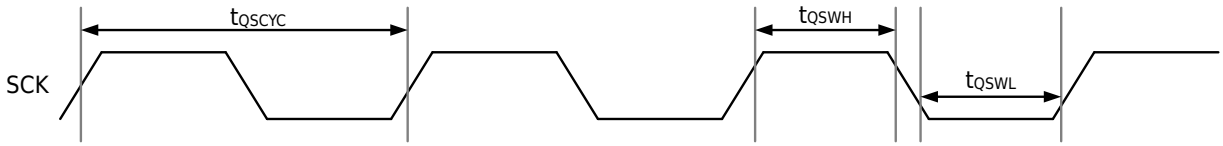


Figure 4-11 QSPI clock timing

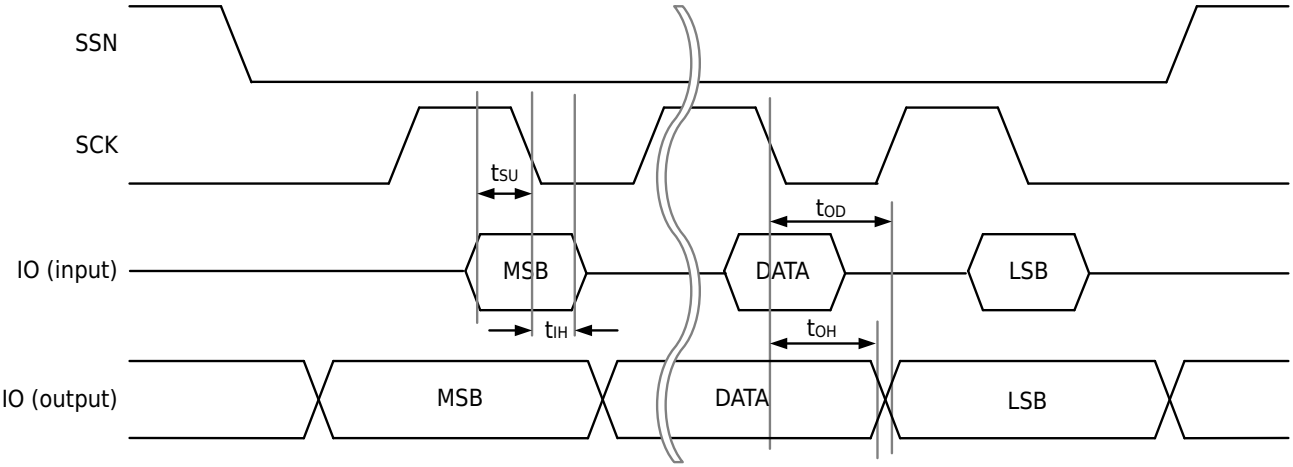


Figure 4-12 QSPI timing definition

4.3.15 MCAN Interface Characteristics

For the port characteristics of MCANx_TX/RX, please refer to "I/O Port Characteristics".

4.3.16 USART Interface Characteristics

Table 4-34 USART AC Timing

Symbol	Parameters	Conditions	Min	Max	Unit
t_{cyc} (1)	Input clock cycles	UART	4	-	t_{PCLK1}
		Clock Synchronization Mode	6	-	
t_{CKw} (1)	Input clock width	-	0.4	0.6	t_{cyc}
t_{CKr} (1)	Input clock rise time	-	-	5	ns
t_{CKf} (1)	Input clock fall time	-	-	5	ns
t_{TD}	Transmit delay time	Clock Synchronization Mode, $2.7V \le V_{CC} \le 3.6V$	-	23	ns
		Clock Synchronization Mode, $1.8V \le V_{CC} < 2.7V$ (1)	-	30	ns
t_{RDS}	Receive data setup time	Clock Synchronization Mode, $2.7V \le V_{CC} \le 3.6V$	17	-	ns
		Clock Synchronization Mode, $1.8V \le V_{CC} < 2.7V$ (1)	23	-	ns
t_{RDH} (1)	Receive data hold time	Clock Synchronization Mode	5	-	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-35 USART Maximum Baud Rate

Mode		Max Baud Rate
UART	Internal clock source	PCLK1/8
	External clock source	PCLK1/32
Clock synchronization mode 2.7V≤V_{CC}≤3.6V		12.0Mbps
Clock synchronization mode 1.8V≤V_{CC}<2.7V		8.0Mbps

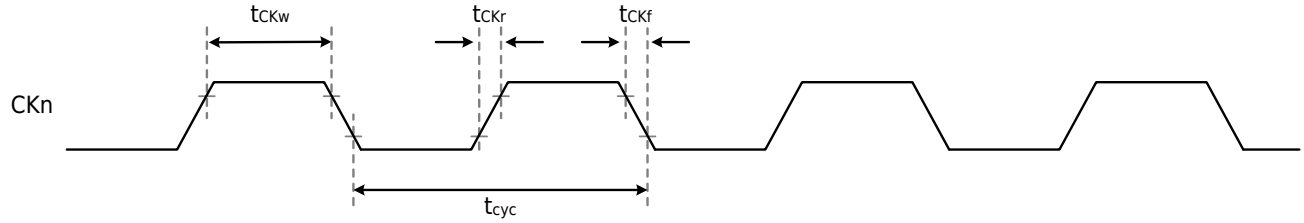


Figure 4-13 USART Clock Timing

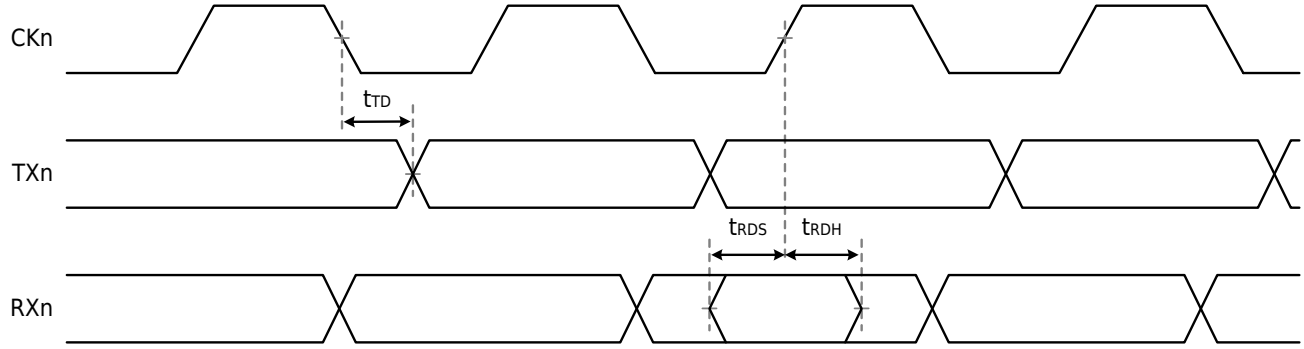


Figure 4-14 USART(CSI) Input and Output Timing

Note

The value of n in the diagram ranges from 1 to 6.

4.3.17 JTAG Interface Characteristics

Table 4-36 JTAG Interface Characteristics

Symbol	Parameters	Min	Typ	Max	Unit
t_{TCKcyc}(1)	JTCK clock period	50	-	-	ns
t_{TCKH}(1)	JTCK clock high level	15	-	-	ns
t_{TCKL}(1)	JTCK clock low level	15	-	-	ns
t_{TCKr}(1)	JTCK clock rise time	-	-	5	ns
t_{TCKf}(1)	JTCK clock fall time	-	-	5	ns
t_{TMSs}	JTMS setup time	10	-	-	ns
t_{TMSh}	JTMS hold time	10	-	-	ns
t_{TDIs}	JTDI setup time	10	-	-	ns
t_{TDIh}	JTDI hold time	10	-	-	ns
t_{TDOd}	JTDO data delay	-	-	25	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.

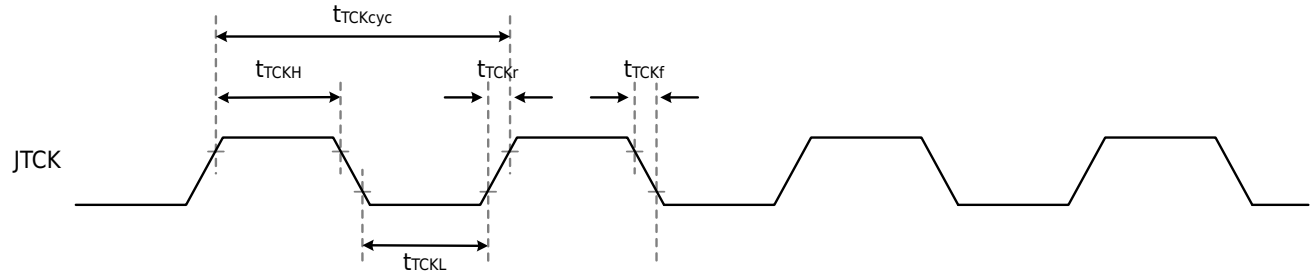


Figure 4-15 JTAG TCK Clock

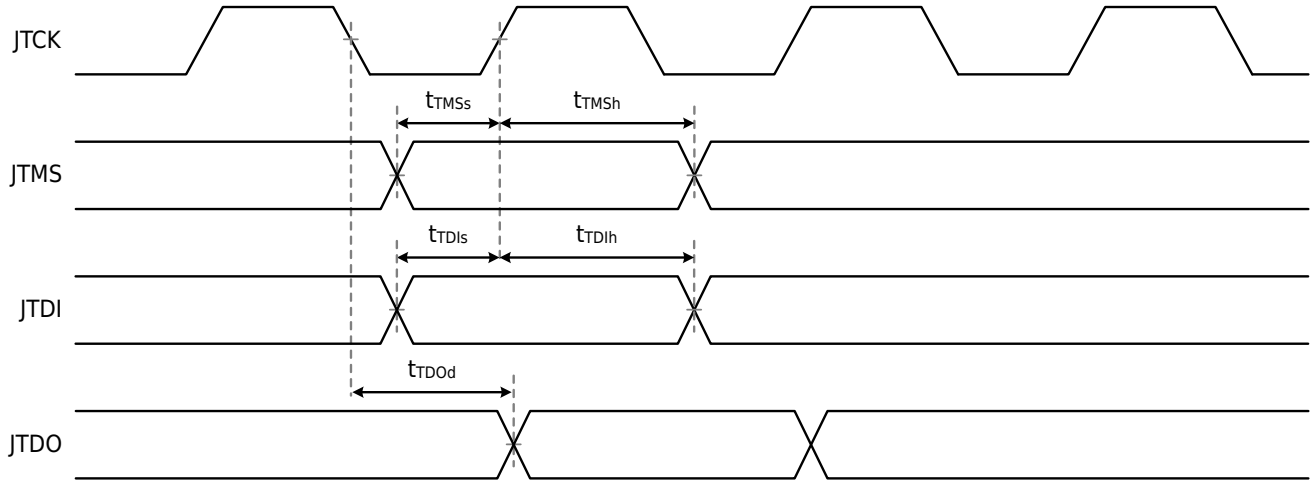


Figure 4-16 JTAG input and Output

4.3.18 SWD Interface Characteristics

Table 4-37 SWD Interface Characteristics

Symbol	Parameters	Min	Typ	Max	Unit
$t_{SWCLKcyc}$ (1)	SWCLK clock period	50	-	-	ns
t_{SWCLKH} (1)	SWCLK clock high level	15	-	-	ns
t_{SWCLKL} (1)	SWCLK clock low level	15	-	-	ns
t_{SWCLKr} (1)	SWCLK clock rise time	-	-	5	ns
t_{SWCLKf} (1)	SWLCK clock fall time	-	-	5	ns
t_{SWDIs}	SWDI setup time	10	-	-	ns
t_{SWDIh}	SWDI hold time	10	-	-	ns
t_{SWDOd}	SWDO data delay	2	-	25	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.

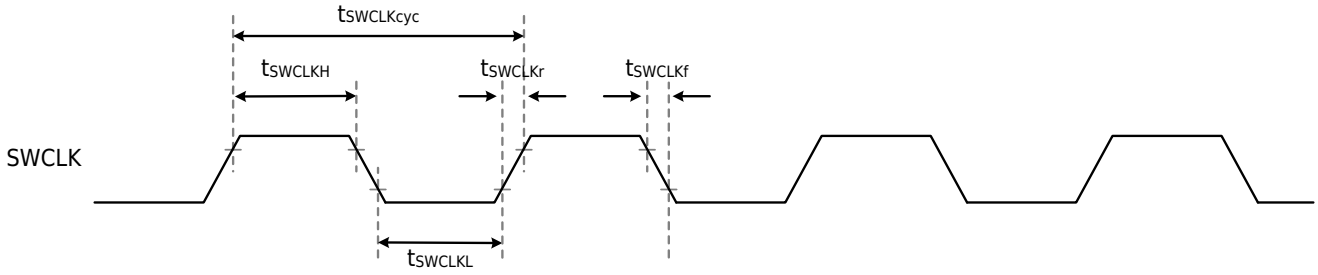


Figure 4-17 SWCLK Clock

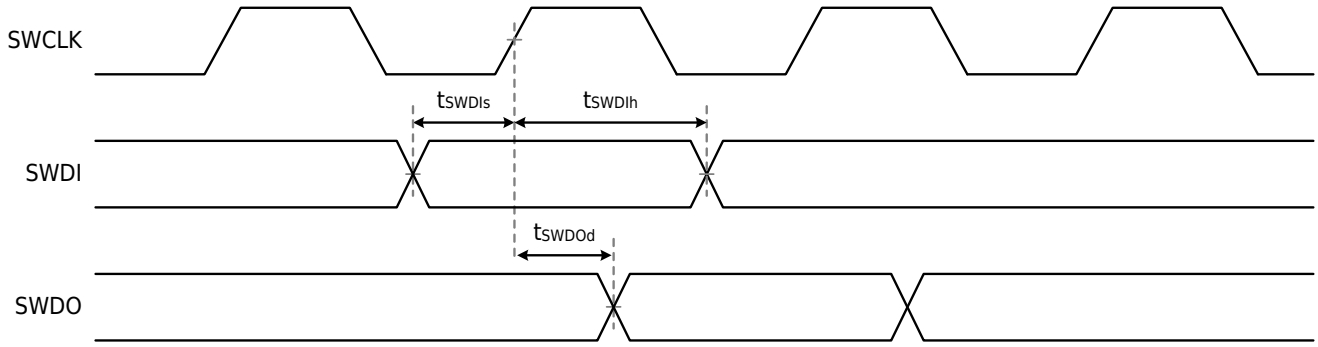


Figure 4-18 SWDIO Input and Output

4.3.19 TRACE Interface Characteristics

Table 4-38 ETM Interface Characteristics

Symbol	Parameters	Min	Typ	Max	Unit
$t_{TRCLKcyc}$ (1)	TRACECK clock period	20	-	-	ns
t_{TRCKH} (1)	TRACECK clock high level	7	-	-	ns
t_{TRCKL} (1)	TRACECK clock low level	7	-	-	ns
t_{TRCKr} (1)	TRACECK clock rise time	-	-	2.5	ns
t_{TRCKf} (1)	TRACECK clock fall time	-	-	2.5	ns
t_{TRDd}	TRACED 0-3 data delay	1.6	-	8.4	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.

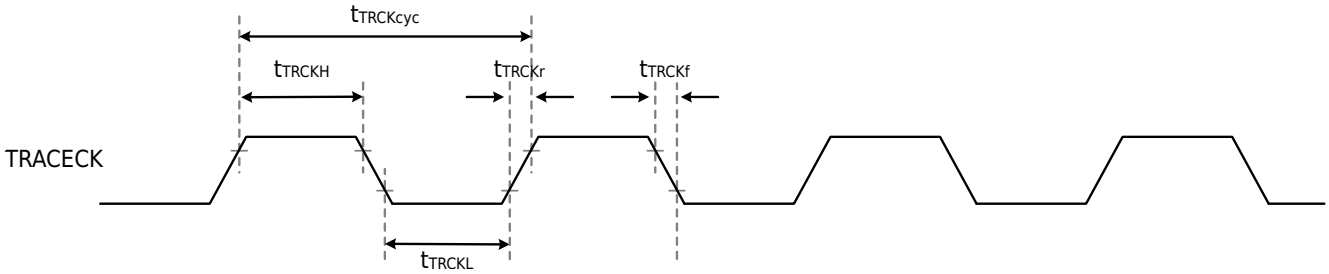


Figure 4-19 TRACE clock

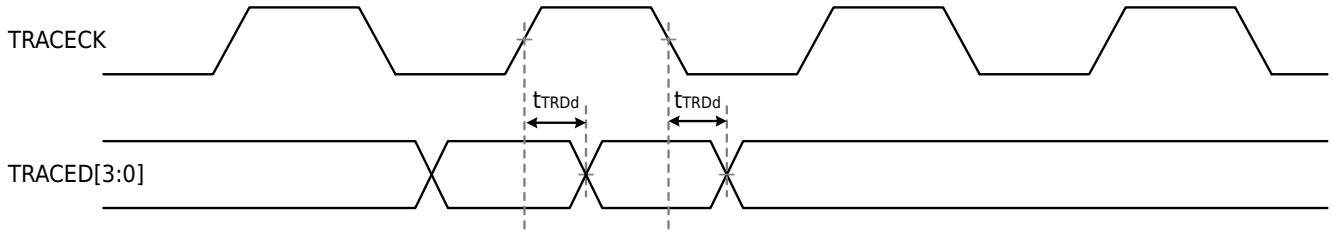


Figure 4-20 TRACE data output

4.3.20 12-bit ADC Characteristics

Table 4-39 ADC Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{AVCC/REFH}$(2)	Power Supply	-	1.8	-	3.6	V
f_{ADC}(2)	ADC Conversion Clock Frequency	High-speed working mode 2.4V≤V_{AVCC}≤3.6V	1	-	60	MHz
		Low-speed working mode 1.8V≤V_{AVCC}<2.4V	1	-	30	
		Ultra-low speed working mode	1	-	8	
V_{AIN}(2)	Conversion Voltage Range	-	V_{AVSS}	-	$V_{AVCC/VREFH}$	V
R_{AIN}(1)	External Input Impedance	See formula 1 for details.	-	-	50	kΩ
R_{ADC}(1)	Sample Switch Resistance	-	-	3	6	kΩ
C_{ADC}(1)	Internal Sampling and Holding Capacitor	-	-	4	7	pF
t_D(1)	Trigger Conversion Delay	f_{ADC}=60MHz	-	-	0.3	μs
t_S(1)	Sample Time	f_{ADC}=60MHz	0.183	-	4.266	μs
			11	-	255	1/f_{ADC}
t_{CONV}(1)	Single Channel Total Conversion Time (Including sampling time, calculated as: sampling time Ts+ gradually approaching n-bit resolution +1)	f_{ADC}=60MHz 12-bit resolution	0.4	-	-	μs
			24	-	268	1/f_{ADC}
		f_{ADC}=60MHz 10-bit resolution	0.37	-	-	μs
			22	-	266	1/f_{ADC}
		f_{ADC}=60MHz 8-bit resolution	0.34	-	-	μs
			20	-	264	1/f_{ADC}
f_S(1)	Sample Rate f_{ADC}=60MHz	12-bit resolution single ADC	-	-	2.5	Msps
t_{ST}(1)	Startup Time	-	-	1	2	μs

Note

1. Guaranteed by design, not tested in production.
2. Resulted from comprehensive evaluation, not tested in production.

Formula 1: RAIN Maximum Formula

$$R_{AIN} = \frac{k}{f_{ADC} \times C_{ADC} \times \ln\left(2^{N+2}\right)} - R_{ADC}$$

The above formula (Formula 1) is used to determine the maximum external impedance that makes the error less than 1/4LSB. Where N=12 (12-bit resolution) and k is the number of sampling periods defined in ADC_SSTR register.

Table 4-40 Input Channel Static Accuracy @f_{ADC}=60MHz(1)

Symbol	Parameters	Conditions	Min	Max	Unit
E_T	Total Unadjusted Error	f_{ADC}=60MHz Input Source Impedance<1kΩ V_{AVCC}=2.4V/3.6V T_A=-40℃/105℃	±5.5	±7	LSB
E_O	Offset Error		±4.5	±7	LSB
E_G	Gain Error		±4.5	±7	LSB
E_D	Differential Nonlinearity Error		±1.5	±3	LSB
E_L	Integral Nonlinearity Error		±2.0	±4	LSB

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-41 Input Channel Static Accuracy @f_{ADC}=8MHz/30MHz(1)

Symbol	Parameters	Conditions	Min	Max	Unit
E_T	Total Unadjusted Error	f_{ADC}=8MHz/30MHz Input Source Impedance<1kΩ V_{AVCC}=1.8V T_A=-40℃/105℃	±5.5	±7	LSB
E_O	Offset Error		±4.5	±7	LSB
E_G	Gain Error		±4.5	±7	LSB
E_D	Differential Nonlinearity Error		±1.5	±3	LSB
E_L	Integral Nonlinearity Error		±2.0	±4	LSB

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-42 Input Channel Dynamic Accuracy @f_{ADC}=60MHz(1)

Symbol	Parameters	Conditions	Min	Max	Unit
ENOB	Effective Number of Bits	f_{ADC}=60MHz Input Signal Frequency=2kHz Input Source Impedanc=0Ω V_{AVCC}=2.4V/3.6V T_A=-40℃/105℃	10.5	-	Bits
SINAD	Signal-to-Noise and Distortion Ratio		65.0	-	dB
SNR	Signal-to-Noise Ratio		65.1	-	dB
THD	Total Harmonic Distortion		-	-78.1	dB

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-43 Input Channel Dynamic Accuracy @f_{ADC}=8MHz/30MHz(1)

Symbol	Parameters	Conditions	Min	Max	Unit
ENOB	Effective Number of Bits	f_{ADC}=8MHz/30MHz Input Signal Frequency=2kHz Input Source Impedanc=0Ω V_{AVCC}=1.8V T_A=-40℃/105℃	10.5	-	Bits
SINAD	Signal-to-Noise and Distortion Ratio		65.0	-	dB
SNR	Signal-to-Noise Ratio		65.1	-	dB
THD	Total Harmonic Distortion		-	-78.1	dB

Note

1. Resulted from comprehensive evaluation, not tested in production.

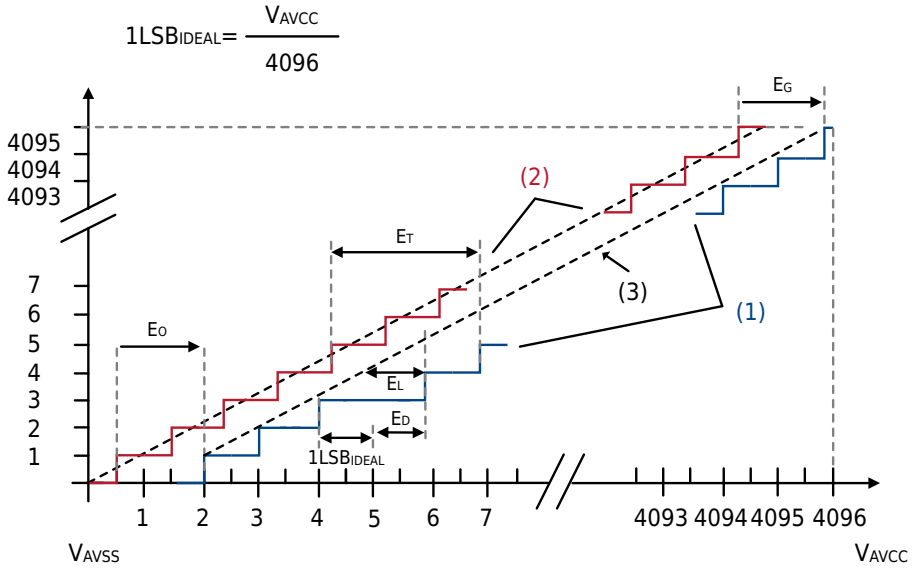


Figure 4-21 ADC Presision Characteristics

1. Examples of actual transmission curves.
2. Ideal transfer curve.
3. Endpoint correlation line.
4. E_T = Total Unadjusted Error: Maximum deviation between actual and ideal transfer curves.
   E_O = Offset Error: Deviation between the first actual conversion and the first ideal conversion.
   E_G = Gain Error: Deviation between the last ideal conversion and the last actual conversion.
   E_D = Differential Nonlinearity Error: Maximum deviation between actual step and ideal value.
   E_L = Integral Nonlinearity Error: Maximum deviation between any actual conversion and the endpoint correlation line.

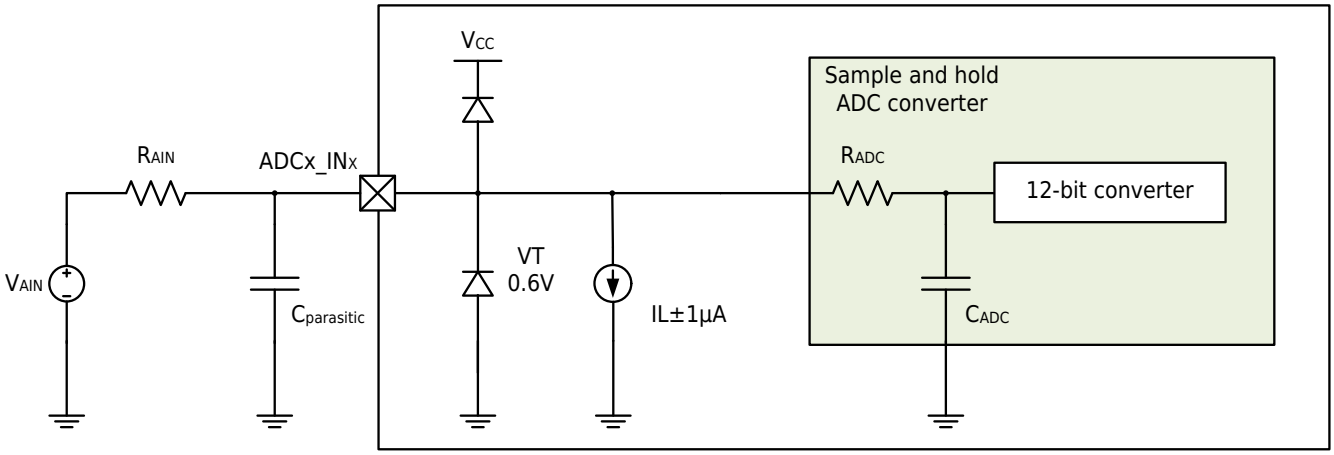


Figure 4-22 Typical connection using ADC

1. For information about R_{AIN}, R_{ADC}, and C_{ADC} values, refer to Table 4-39 : ADC Characteristics.
2. $C_{parasitic}$ indicates PCB capacitance (depending on the quality of soldering and PCB wiring) and bonding pad capacitance (about 5pF). Higher values of $C_{parasitic}$ result in less accurate conversions. To solve this problem, f_{ADC} should be reduced.

General PCB Design Guidelines

The power supply should be decoupled as shown in the following figure. 0.1μF capacitor should be (high quality) ceramic capacitor. These capacitors should be as close to the chip as possible.

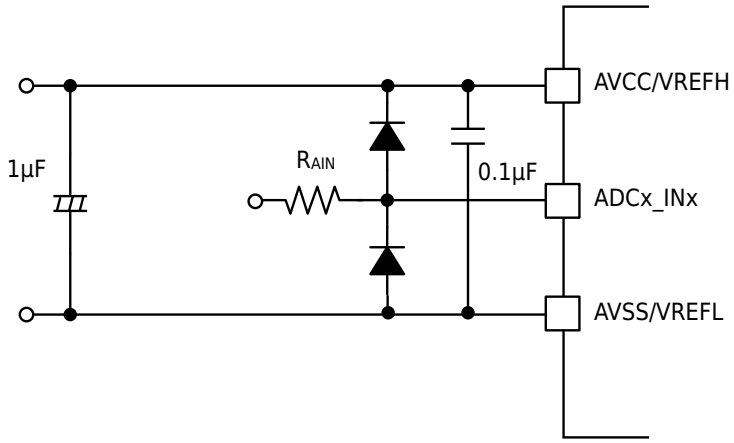


Figure 4-23 Example of Power Supply and Reference Supply Decoupling

1. For information about R_{AIN} values, refer to Table 4-39 : ADC Characteristics.

4.3.21 12-bit DAC Characteristics

Table 4-44 12-bit DAC Port Output Enabled and Output Amplifier Enabled Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{AVCC}(1)	Analog power voltage	-	1.8	3.3	3.6	V
AO	Output voltage range	-	0.2	-	V_{AVCC}-0.2	-
RL(1)	Load resistance	-	40	-	-	kΩ
CL(1)	Load capacitance	-	-	-	50	pF
DNL	Differential nonlinear error (deviation between two consecutive codes -1LSB)	RL=40kΩ	-	-	±3	LSB

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
INL	Integral nonlinear error (the difference between the value measured at code I and the value at code I on the line between code 0 and the last code 4095)	RL=40kΩ	-	-	±5	LSB
OE(1)	Offset error (the difference between measured value at code 2048 and ideal value VREF+/2)	-	-	-	±15	LSB
GE(1)	Gain error	-	-	-	±1	%
T_{st}(2)	Settling time (full scale: suitable for 12-bit input code conversion between the lowest input code and the highest input code when the DAC output reaches the final value of ±4LSB)	-	-	2	3	μs

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.

Table 4-45 12-bit DAC Port Output Enabled and Output Amplifier Disabled Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{AVCC}(1)	Analog Power Voltage	-	1.8	3.3	3.6	V
AO(1)	Output Voltage Range	-	0	-	V_{AVCC}-1LSB	V
CL(1)	Load Capacitance	-	-	-	20	pF
RO(1)	Output Resistance	-	-	8.6	12	kΩ
DNL	Differential nonlinear error (deviation between two consecutive codes -1LSB)	-	-	-	±2	LSB
TUE(1)	Total Unadjustable Error	-	-	-	±24	LSB
T_{st}(2)	Settling time (applicable to 12-bit input code conversion between the lowest input code and the highest input code when the DAC output reaches the final value of ±4LSB, CL=10pF)	-	-	1.5	2.5	μs

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.

Table 4-46 12-bit DAC Port Output Disabled and Output Amplifier Disabled Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{AVCC}(2)	Analog Power Voltage	-	1.8	3.3	3.6	V
AO(1)	Output Voltage Range	-	0	-	V_{AVCC}-1LSB	V

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
DNL(1)	Differential nonlinear error (deviation between two consecutive codes -1LSB)	-	-	-	±2	LSB
TUE(1)	Total Unadjustable Error	-	-	-	±5	LSB
T_{st}(1)	Settling time (applicable to 12-bit input code conversion between the lowest input code and the highest input code when the DAC output reaches the final value of ±1LSB)	V_{AVCC}≥2.7	-	95.5	117.3	ns
	Settling time (applicable to 12-bit input code conversion between the lowest input code and the highest input code when the DAC output reaches the final value of ±32LSB)	V_{AVCC}≥2.7	-	57.2	70.5	ns
	Settling time (applicable to 12-bit input code conversion between the lowest input code and the highest input code when the DAC output reaches the final value of ±1LSB)	V_{AVCC}<2.7	-	-	121.6	ns
	Settling time (applicable to 12-bit input code conversion between the lowest input code and the highest input code when the DAC output reaches the final value of ±32LSB)	V_{AVCC}<2.7	-	-	79.1	ns

Note

1. Guaranteed by design, not tested in production.
2. Resulted from comprehensive evaluation, not tested in production.

4.3.22 Comparator Characteristics

Table 4-47 Comparator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{AVCC}(2)	Analog Power Voltage	-	1.8	3.3	3.6	V
V_I(2)	Input Voltage Range	-	0	-	V_{AVCC}	V
T_{cmp}(1)	Compare Time	Comparator resolution voltage =100mV	-	30	50	ns
T_{set}(2)	Input Channel Switching Stabilization Time	-	-	100	200	ns

Note

1. Guaranteed by design, not tested in production.
2. Resulted from comprehensive evaluation, not tested in production.

4.3.23 EXMC Characteristics

Table 4-48 EXMC Characteristics in Internal EXCLK Mode

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
t_add_d	Address line output delay time	2.7V≤V_{CC}≤3.6V	-	-	12	ns
		1.8V≤V_{CC}<2.7V	-	-	18	ns
t_data_d	Data line output delay time	2.7V≤V_{CC}≤3.6V	-	-	12	ns
		1.8V≤V_{CC}<2.7V	-	-	18	ns
t_ce_d	CE output delay time	2.7V≤V_{CC}≤3.6V	-	-	9	ns
		1.8V≤V_{CC}<2.7V	-	-	12	ns
t_we_d	WE output delay time	2.7V≤V_{CC}≤3.6V	-	-	9	ns
		1.8V≤V_{CC}<2.7V	-	-	12	ns
t_oe_d	OE output delay time	2.7V≤V_{CC}≤3.6V	-	-	9	ns
		1.8V≤V_{CC}<2.7V	-	-	12	ns
t_baa_d	BAA output delay time	2.7V≤V_{CC}≤3.6V	-	-	9	ns
		1.8V≤V_{CC}<2.7V	-	-	12	ns
t_adv_d	ADV output delay time	2.7V≤V_{CC}≤3.6V	-	-	9	ns
		1.8V≤V_{CC}<2.7V	-	-	12	ns
t_ale_d	ALE output delay time	2.7V≤V_{CC}≤3.6V	-	-	9	ns
		1.8V≤V_{CC}<2.7V	-	-	12	ns
t_data_s	Data line input setup time	2.7V≤V_{CC}≤3.6V	24	-	-	ns
		1.8V≤V_{CC}<2.7V	28	-	-	ns
t_data_h	Data line input Hold time	-	0	-	-	ns
t_rb_s	RB input Setup time	2.7V≤V_{CC}≤3.6V	24	-	-	ns
		1.8V≤V_{CC}<2.7V	28	-	-	ns
t_rb_h	RB input Hold time	-	0	-	-	ns

Table 4-49 EXMC Characteristics in Feedback EXCLK Mode

Symbol	Parameters		Min	Typ	Max	Unit
t_add_d	Address line output delay time	2.7V≤V_{CC}≤3.6V	-	-	12	ns
		1.8V≤V_{CC}<2.7V	-	-	18	ns
t_data_d	Data line output delay time	2.7V≤V_{CC}≤3.6V	-	-	12	ns
		1.8V≤V_{CC}<2.7V	-	-	18	ns
t_ce_d	CE output delay time	2.7V≤V_{CC}≤3.6V	-	-	9	ns
		1.8V≤V_{CC}<2.7V	-	-	12	ns

Symbol	Parameters		Min	Typ	Max	Unit
t_we_d	WE output delay time	2.7V≤V_{CC}≤3.6V	-	-	9	ns
		1.8V≤V_{CC}<2.7V	-	-	12	ns
t_oe_d	OE output delay time	2.7V≤V_{CC}≤3.6V	-	-	9	ns
		1.8V≤V_{CC}<2.7V	-	-	12	ns
t_baa_d	BAA output delay time	2.7V≤V_{CC}≤3.6V	-	-	9	ns
		1.8V≤V_{CC}<2.7V	-	-	12	ns
t_adv_d	ADV output delay time	2.7V≤V_{CC}≤3.6V	-	-	9	ns
		1.8V≤V_{CC}<2.7V	-	-	12	ns
t_ale_d	ALE output delay time	2.7V≤V_{CC}≤3.6V	-	-	9	ns
		1.8V≤V_{CC}<2.7V	-	-	12	ns
t_data_s	Data line input setup time	1.8V≤V_{CC}≤3.6V	7	-	-	ns
t_data_h	Data line input Hold time	2.7V≤V_{CC}≤3.6V	5	-	-	ns
		1.8V≤V_{CC}<2.7V	14	-	-	ns
t_rb_s	RB input Setup time	1.8V≤V_{CC}≤3.6V	7	-	-	ns
t_rb_h	RB input Hold time	2.7V≤V_{CC}≤3.6V	5	-	-	ns
		1.8V≤V_{CC}<2.7V	14	-	-	ns

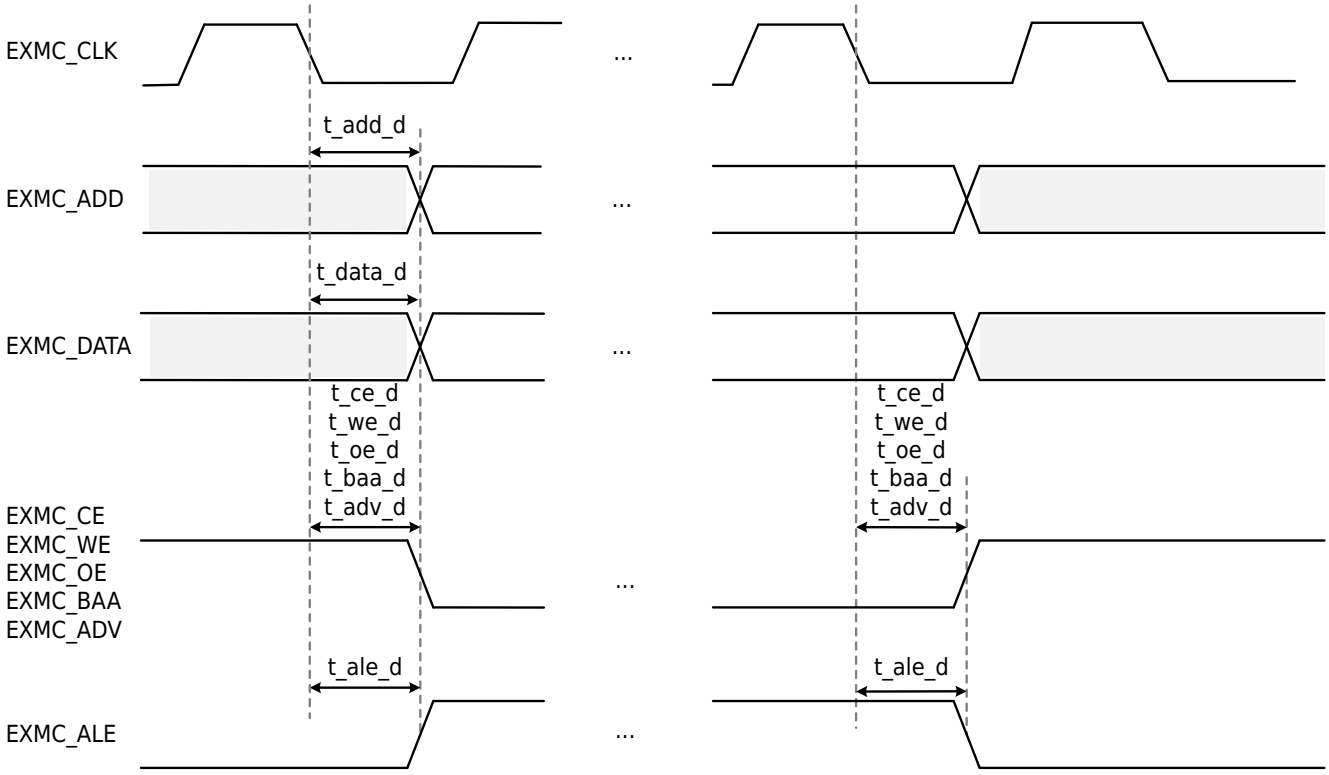


Figure 4-24 EXMC Output Signal Timing Diagram

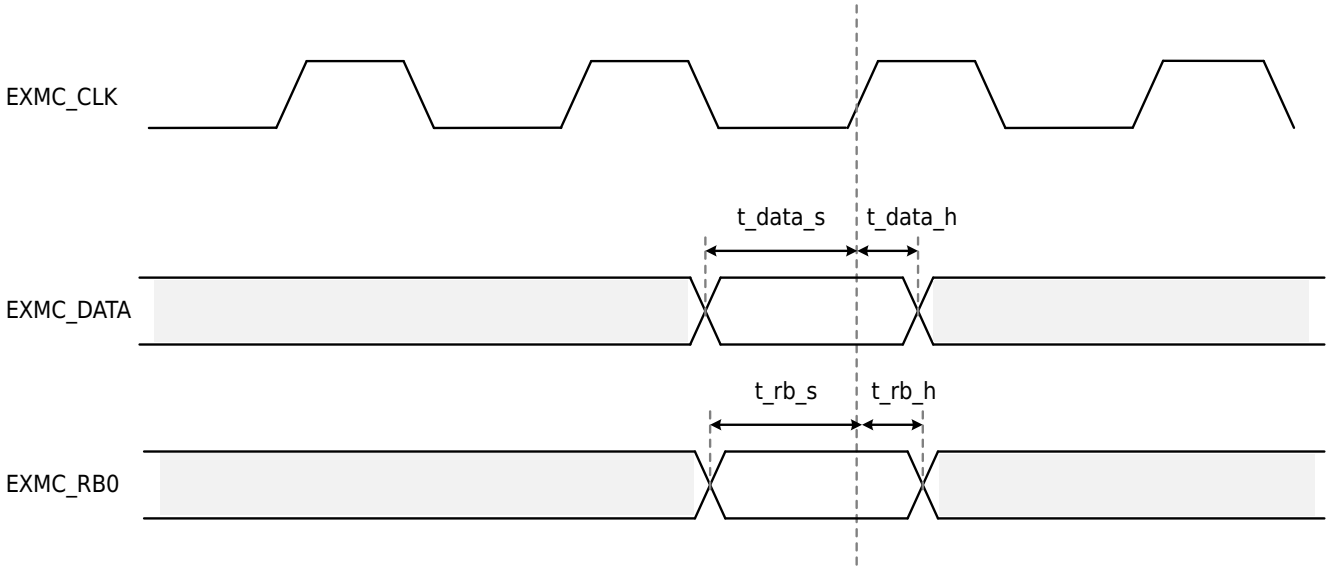


Figure 4-25 EXMC Input Signal Timing Diagram

4.3.24 EIRQ Filter Characteristics

Table 4-50 EIRQ Filter Characteristics(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
W_{F_EIRQ}	EIRQ input filter width	INTC_NOCCR.NOCSEL=0b00	0.6	-	1.0	μs
		INTC_NOCCR.NOCSEL=0b01	1.3	-	2.0	μs
		INTC_NOCCR.NOCSEL=0b10	2.6	-	4.0	μs
		INTC_NOCCR.NOCSEL=0b11	5.2	-	8.0	μs

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.25 RX Filter Characteristics in USART1 STOP Mode

Table 4-51 RX Filter Characteristics in USART1 STOP Mode(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
W_{F_USART1}	USART1 input filter width	USART1_NFC.USART1_NFS=0b00	0.6	-	1.0	μs
		USART1_NFC.USART1_NFS=0b01	1.3	-	2.0	μs
		USART1_NFC.USART1_NFS=0b10	2.6	-	4.0	μs
		USART1_NFC.USART1_NFS=0b11	5.2	-	8.0	μs

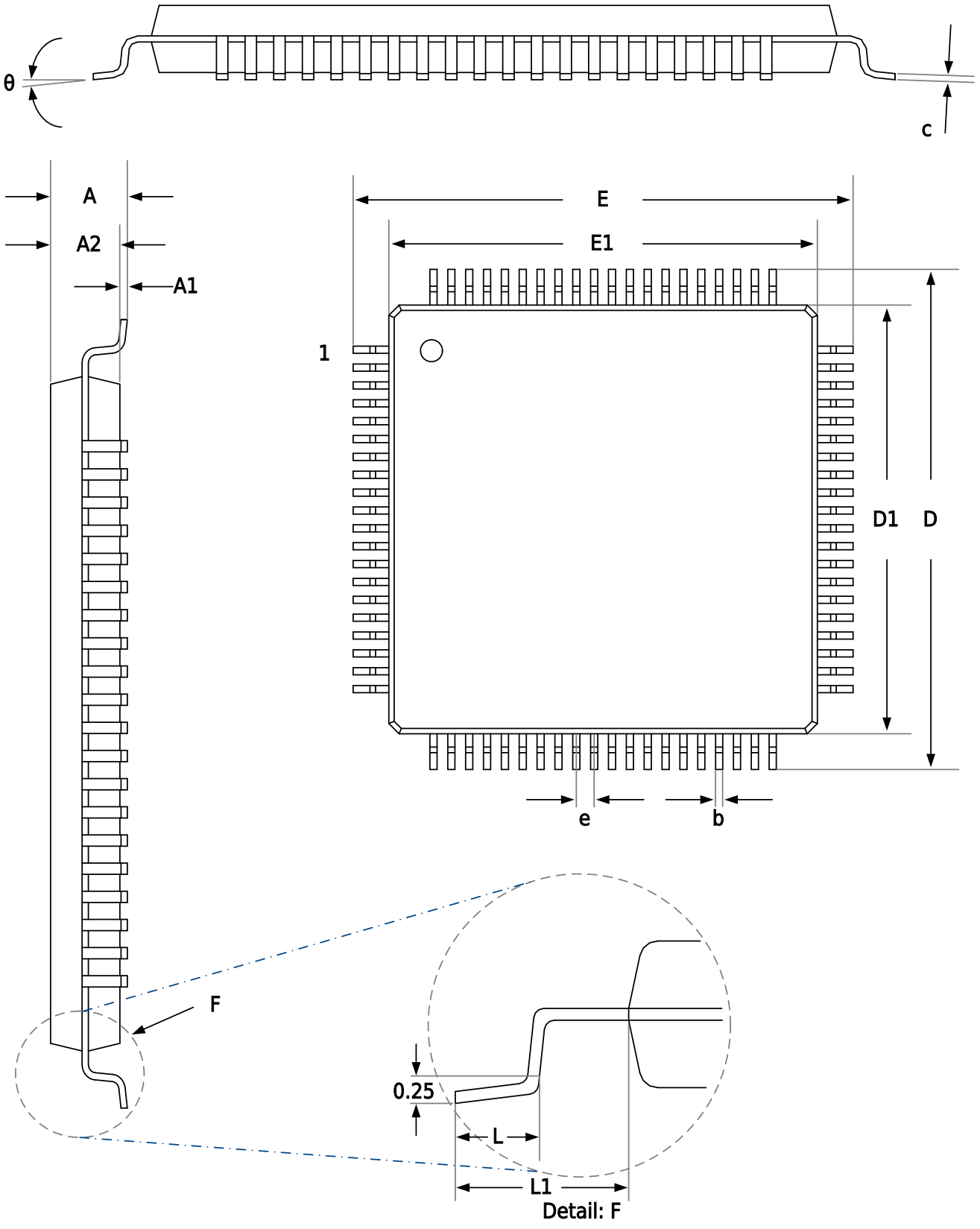
Note

1. Resulted from comprehensive evaluation, not tested in production.

5 Package Specifications

5.1 Package Dimensions

5.1.1 LQFP80 Package

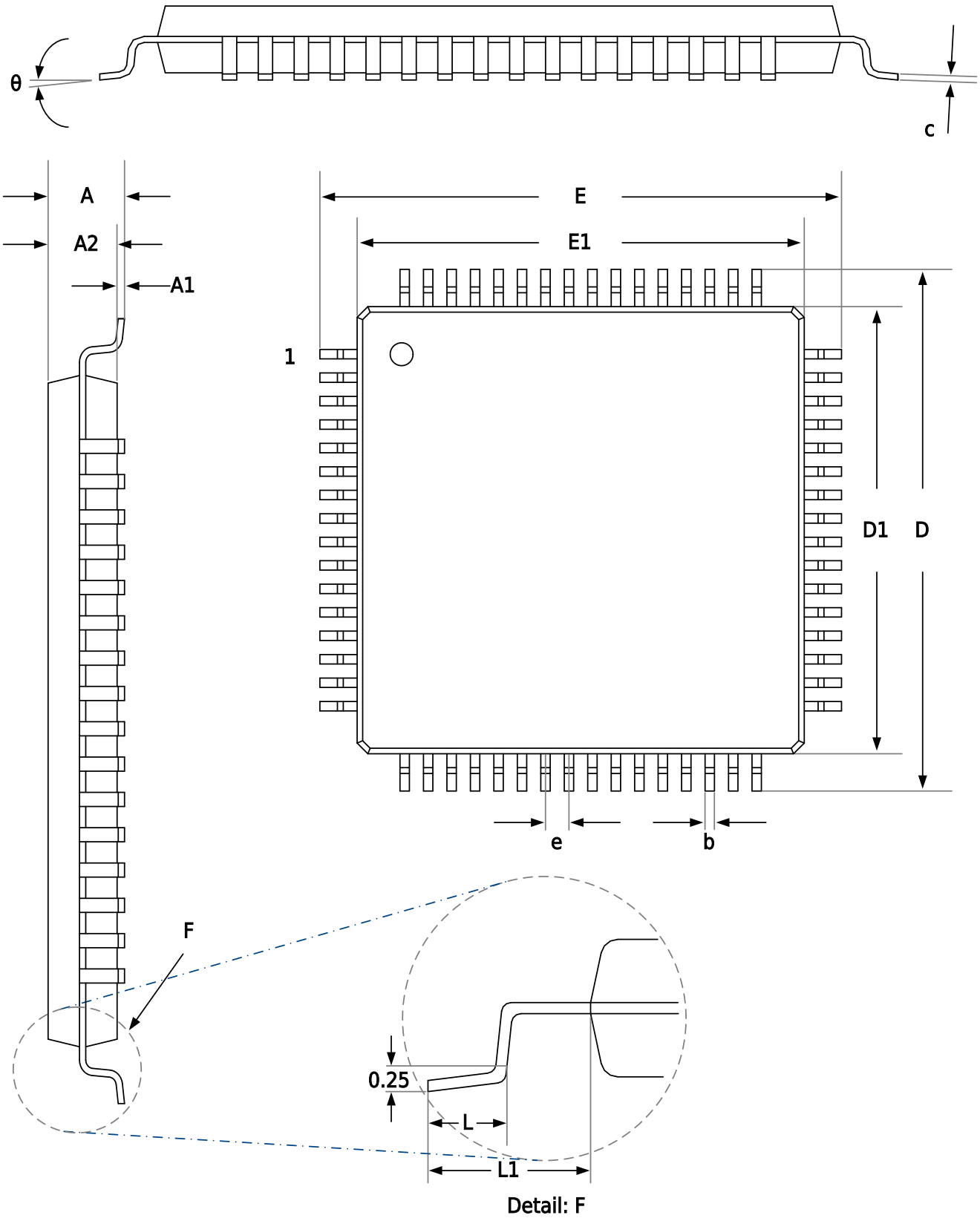


Symbol	12*12 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	--	7°

Note

Dimensions "D1" and "E1" do not include mold flash.

5.1.2 LQFP64 Package

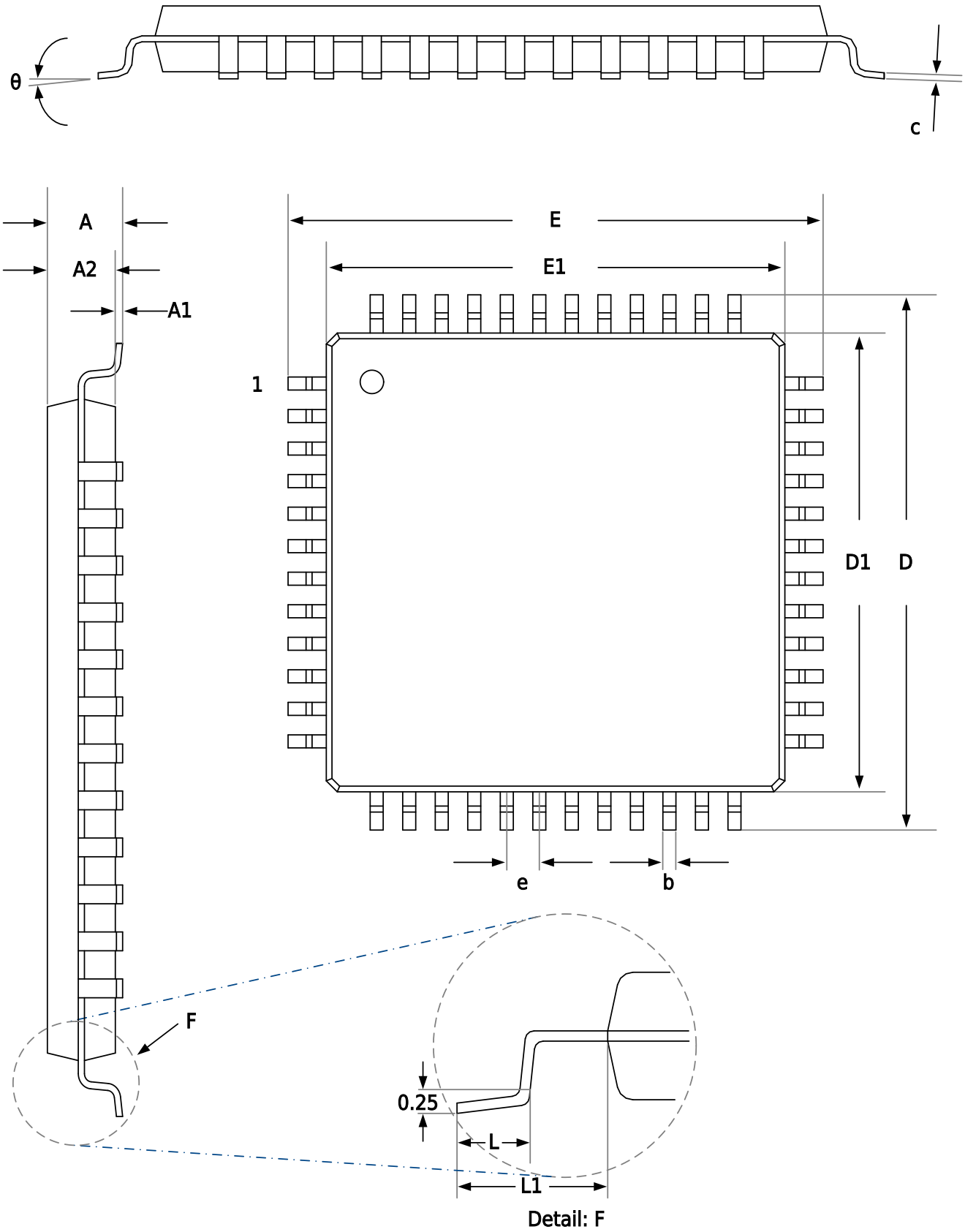


Symbol	10*10 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0°	--	7°

Note

Dimensions "D1" and "E1" do not include mold flash.

5.1.3 LQFP48 Package



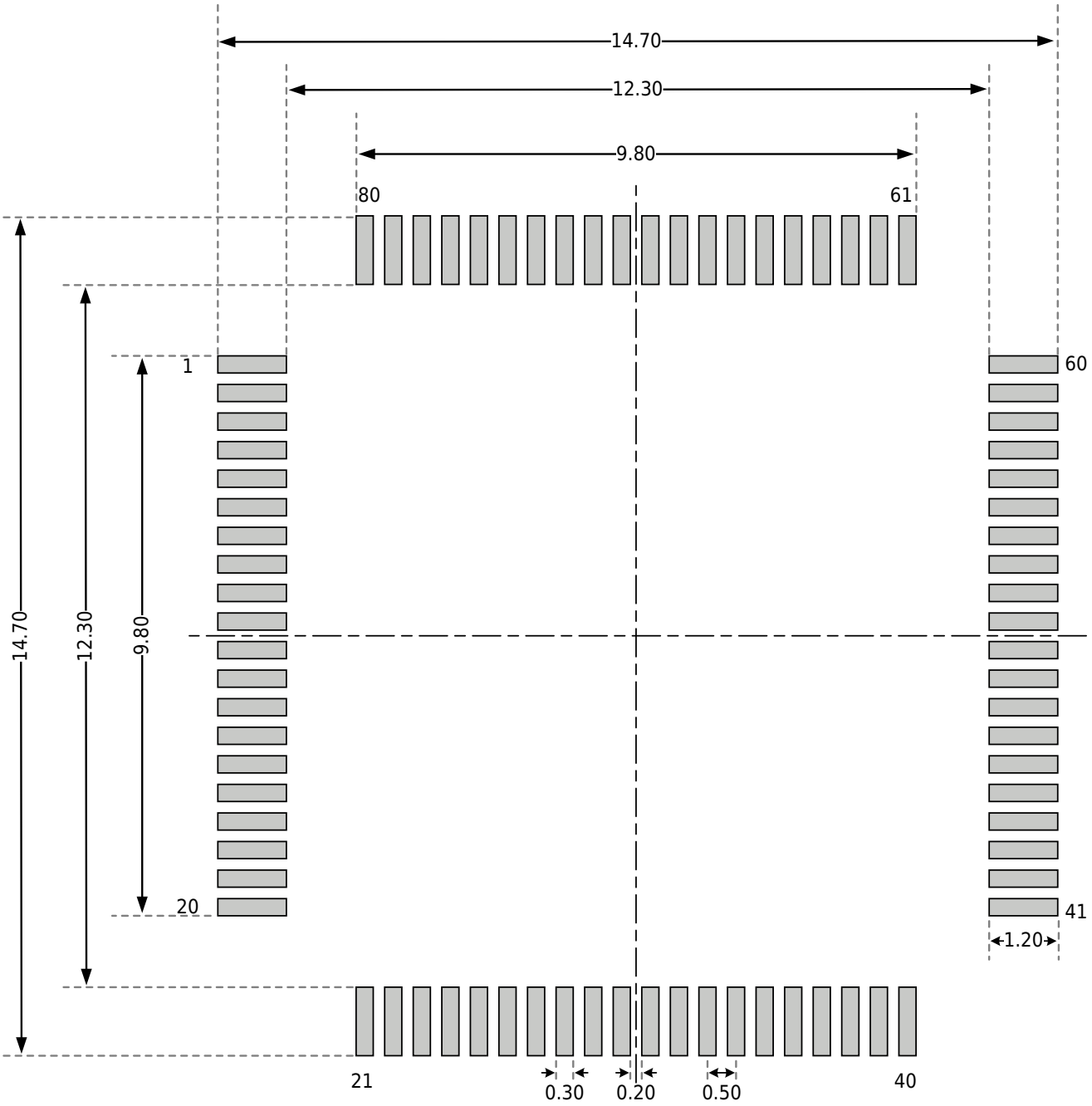
Symbol	7*7 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0	--	7°

Note

Dimensions "D1" and "E1" do not include mold flash.

5.2 PCB Land Pattern

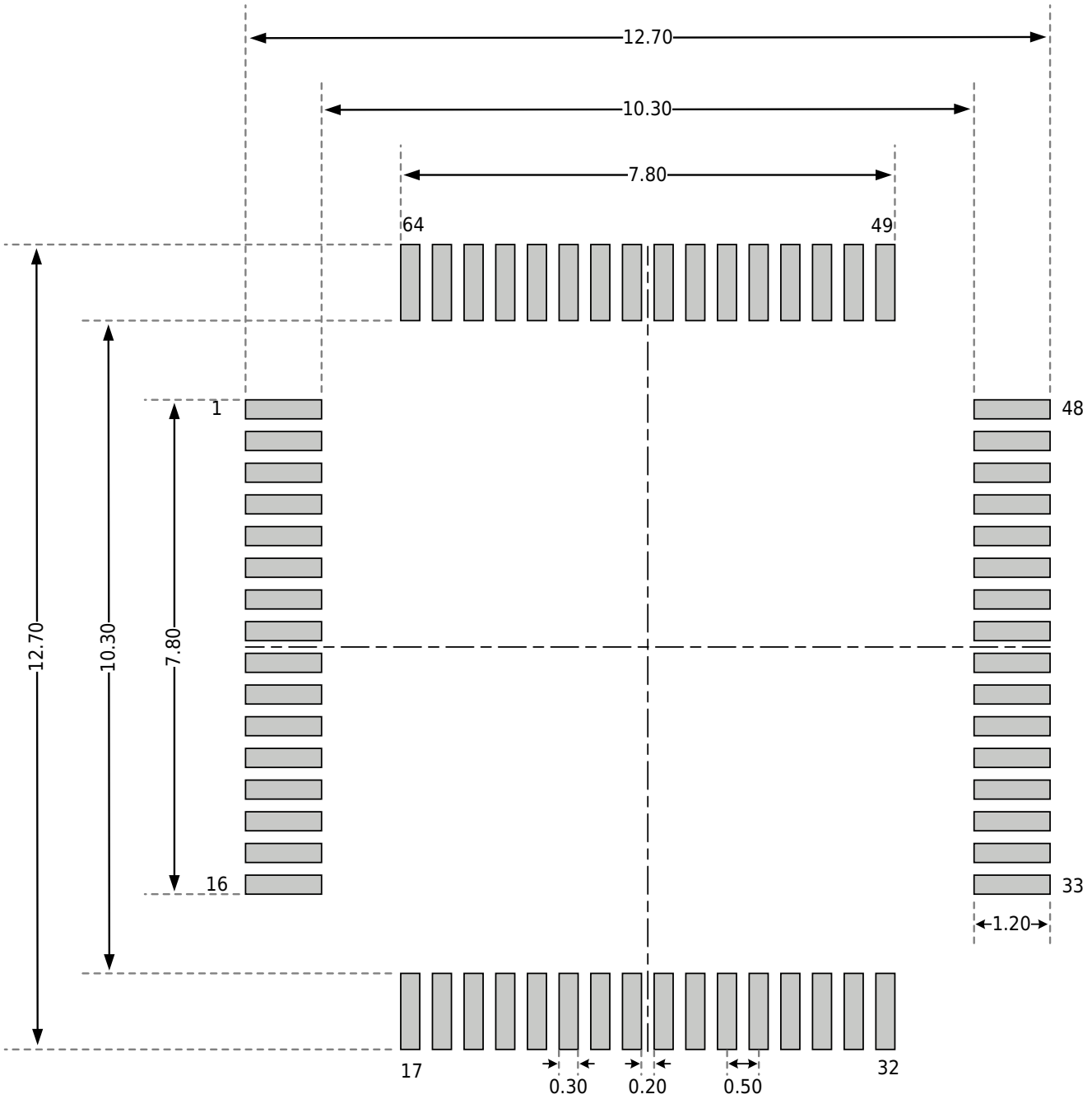
5.2.1 LQFP80 Package (12mm*12mm)



Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

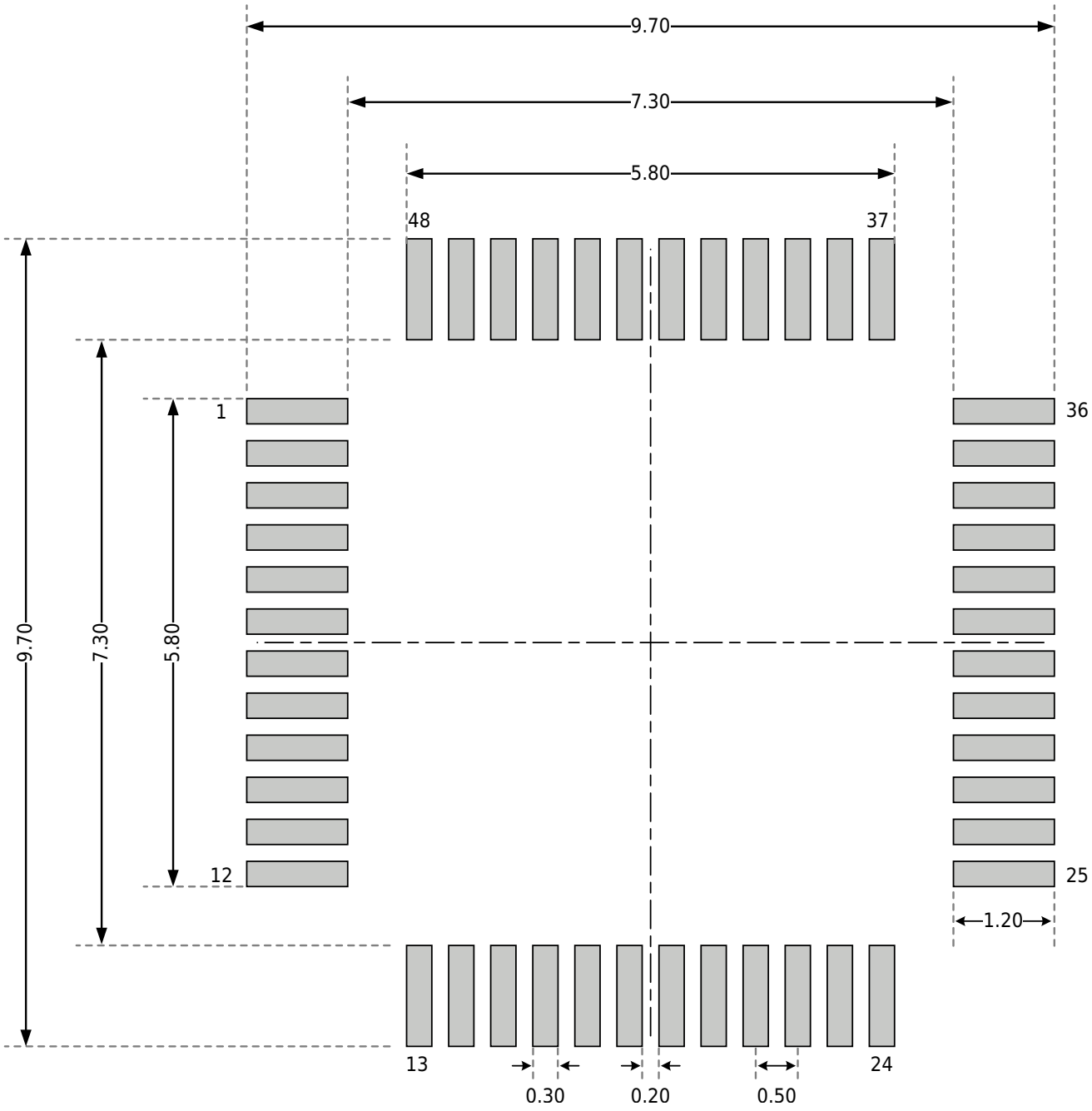
5.2.2 LQFP64 Package (10mm*10mm)



Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

5.2.3 LQFP48 Package (7mm*7mm)



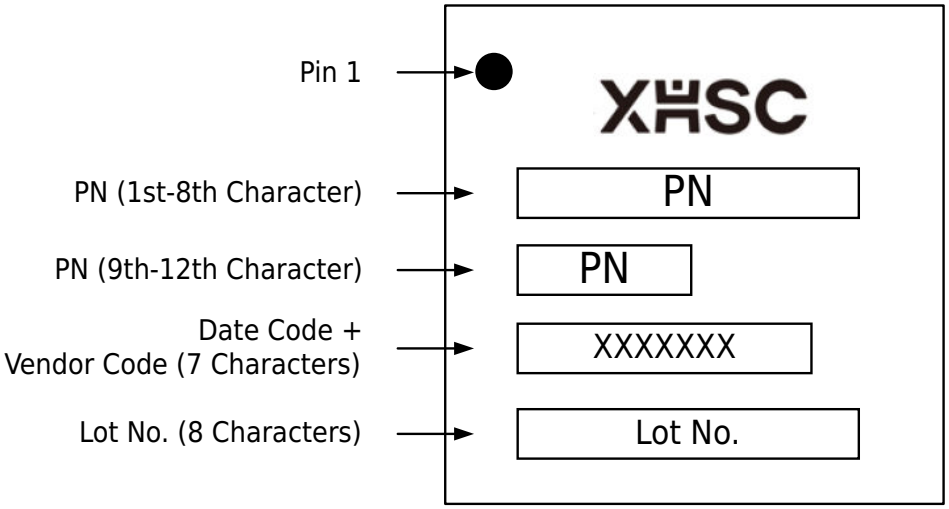
Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

5.3 Package Marking

The location and information description of Pin1 on the front of each package are given below.

LQFP80 package (12mm*12mm)/LQFP64 package (10mm*10mm)/LQFP48 package (7mm*7mm)



5.4 Packaging Thermal Resistance Coefficient

When the packaged chip is working at the specified working environment temperature, the junction temperature T_j(℃) of the chip surface can be calculated according to the following formula:

$T_j = T_A + (P_D * \theta_{JA})$

- T_A refers to the working environment temperature when the packaged chip is working, the unit is ℃;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is ℃/W;
- P_D refers to total power dissipation, which is the sum of internal power consumption (P_{INT}) and I/O pin power consumption (P_{IO}), the unit is W.

  $P_D = P_{INT} + P_{IO}$

  - P_{INT}: Internal power consumption, calculated as the product of Icc and Vcc.
  - P_{IO}: I/O pin power consumption, calculated as: $P_{IO} = \Sigma(V_{OL} * I_{OL}) + \Sigma((V_{CC} - V_{OH}) * I_{OH})$

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable junction temperature T_{Jmax} of the chip.

Table 5-4 Thermal Resistance Coefficient Table For Each Package

Package Type and Dimensions	Thermal Resistance Parameters (θ_{JA})	Unit
LQFP80 12mm*12mm/0.5mm pitch	55±10%	℃/W
LQFP64 10mm*10mm/0.5mm pitch	65±10%	℃/W
LQFP48 7mm*7mm/0.5mm pitch	75±10%	℃/W

6 Ordering Information

Part Number		HC32A448JCTI-LQ48	HC32A448KCTI-LQFP64	HC32A448MCTI-LQFP80
GPIO		38	52	67
CPU	Core	Cortex-M4	Cortex-M4	Cortex-M4
	Frequency	200MHz	200MHz	200MHz
Memory	Flash	256KB	256KB	256KB
	SRAM	68KB	68KB	68KB
Power supply voltages		1.8~3.6V	1.8~3.6V	1.8~3.6V
Temp Range		-40~105℃	-40~105℃	-40~105℃
DMA		2unit*6ch	2unit*6ch	2unit*6ch
TIMER	Timer0	2unit	2unit	2unit
	TimerA	5unit	5unit	5unit
	Timer4	3unit	3unit	3unit
	Timer6	2unit	2unit	2unit
RTC		1ch	1ch	1ch
WDT		1ch	1ch	1ch
SWDT		1ch	1ch	1ch
Connectivity	USART	6ch	6ch	6ch
	I2C	2ch	2ch	2ch
	SPI	3ch	3ch	3ch
	QSPI	1ch	1ch	1ch
	CAN FD	2ch	2ch	2ch
	EXMC	×	√	√
Analog	12-bit ADC	3unit, 11ch	3unit, 17ch	3unit, 24ch
	12-bit DAC	2ch	2ch	2ch
	CMP	4ch	4ch	4ch
	PVD	√	√	√
Security	AES256	√	√	√
	TRNG	√	√	√
	HASH	SHA256	SHA256	SHA256
Co-processing	DCU	√	√	√
Package (mm*mm)		LQFP48(7*7)	LQFP64(10*10)	LQFP80(12*12)
Packing		Tray	Tray	Tray
Pitch		0.5mm	0.5mm	0.5mm
Thickness		1.4mm	1.4mm	1.4mm

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Revision History

Revision/Date	Changes
Rev1.31 Feb. 12, 2026	1. Electrical Specifications: In the "Memory (Flash) Characteristics" chapter, the data of N_{end} parameters have been optimized and updated based on new conditions, the subscript of table "Flash Programming Erase Time" is added; 2. Ordering Information: The thickness of LQFP package is modified to "1.4mm".
Rev1.30 Nov. 27, 2025	1. Electrical Specifications: in the "General Operating Conditions" chapter, the 4th description of Note is changed from "It is suggested that external power supply should be connected in series through a resistor above 100Ω"to "It is suggested that external power supply and grounding should be connected in series through a resistor above 1kΩ"; in the "Supply Current Characteristics" chapter, the table of **Low Power Mode Current Consumption** has newly added data for "Power-down mode 2+XTAL32+RTC+Ret RAM".
Rev1.20 Mar. 28, 2025	1. The manual style is refreshed according to the structured development process. Content unified adjustment: ● Product Lineup (original "model naming rules" and "model function comparison table") and functional block diagram chapters are integrated into the "Product Overview" chapter. ● The directory level of "Function Introduction" is raised to the first-level title, and it is modified as the section of "Functional Description". Deleted the description of the introduction chapter. 2. Feature List: EXMC added the description "Support LCD interface, compatible with 8080/6800 mode". 3. Product Overview: in the "Product lineup" chapter, the description of product name diagram is changed from "Configuration 9" to "Configuration 8", and the content and form of model function comparison table are adjusted, added CPU and clock information, adjusted EXMC to communication interface, and adjusted PVD to analog; the chapter of "Functional Block Diagram" added the description of differences. 4. Pin Definitions: in the "Pin Function Table" chapter, LQFP48 is updated in the port configuration table, and the PortE description in the general function specification table is changed from "PE0-PE5" to "PE0-PE4"; in "Pin Function Description" chapter, IO attribute of XTAL_EXT/XTAL_OUT is changed from "O" to "IO", and "External Master Clock Oscillator Interface" is added. 5. Electrical Specification: in the "parameter conditions" chapter, the definition of maximum and minimum values and typical parameter values are optimized; the data sources of the whole chapter are adjusted according to the latest specifications; in the "Supply current characteristics" chapter, the data conditions are summarized and the condition information with instructions are refreshed; in "SPI interface characteristics" chapter, the condition of section t_w(SCKL) is changed from "1.8V≤Vcc<3.6V" to "1.8V≤Vcc≤3.6V"; in the "QSPI interface characteristics" chapter, the "t_H" in QSPI timing definition diagram is changed to "t_{IH}"; added "MCAN interface characteristics" chapter; in the "12-bit ADC Char-

Revision/Date	Changes
Rev1.20 Mar. 28, 2025	acteristics" chapter, figure "Typical connection using ADC" added a diode that pulls up V_{CC}; 6. Package Specifications: The graphic information in the section "Package Dimensions-LQFP80 Package" is optimized, which is consistent with the table; in the "Packaging Thermal Resistance Coefficient" chapter, the description of P_D is adjusted to make it more practical. 7. Ordering Information: adjusted the ordering of some information.
Rev1.00 Apr. 16, 2024	First official release.