XHSC 小华半导体 XIAOHUA SEMICONDUCTOR

HC32A472 Series

32-bit ARM® Cortex®-M4 Microcontroller

Datasheet

Rev1.01 December 2025

Features

ARM Cortex-M4 32bit MCU+FPU, 150 DMIPS, 512 KB Flash, 68 KB SRAM, USBFS, 3 CANs (FD/ 2.0B), EXMC, 25 Timers, 3 ADCs, DAC, 2 PGAs, 2 CMPs, 6 UARTs, 4 SPIs, 3 I2Cs, QSPI, AES, HASH (SHA256/ HMAC), FMAC (FIR), MAU

- **ARMv7-M architecture 32bit Cortex-M4 CPU, integrated FPU, MPU, DSP supporting SIMD instructions, and CoreSight standard debugging unit. The highest operating frequency is 120 MHz, reaching a computing performance of 150 DMIPS or 410 Coremarks**
- **Built-in memory**
  - Maximum 512 KByte dual bank Flash memory
  - Maximum 64 KByte of single-cycle access high-speed SRAM and 4 KByte of power-off retention SRAM.
- **Power, Clock, Reset Management**
  - System power supply (Vcc): 1.8-3.6V
  - 7 independent clock sources: external main clock crystal oscillator (4-25MHz), external secondary crystal oscillator (32.768kHz), internal high-speed RC (16/20MHz), internal medium-speed RC (8MHz), internal low-speed RC (32.768kHz), internal WDT Dedicated RC (10kHz)
  - 15 reset sources including power-on reset (POR), low voltage detection reset (PVD1R/PVD2R), port reset (NRST), each reset source has an independent flag bit
- **Low power operation**
  - Peripherals can be turned off or on independently
  - Three low power modes: Sleep, Stop, Power down mode
- **Peripheral operation support system significantly reduces CPU processing load**
  - 16-channel dual-host DMAC
  - DMAC for USBFS
  - 3 Data computing units (DCU)
  - Math coprocessing unit (MAU), supports Sin/Sqrt
  - Support 16th order FIR digital filter (FMAC)
  - Support mutual triggering of peripheral events (AOS)
- **High Performance Simulation**
  - 3 independent 12bit 2.5 MSPS ADCs
  - 1 independent 12-bit DAC
  - 2 programmable gain amplifier (PGA)
  - 2 independent voltage comparators (CMP)
  - 1 on-chip temperature sensor (OTS)
- **Timer**
  - 10 multifunctional 16bit PWM Timers (Timer6)
  - 1 16bit motor PWM Timers (Timer4)
  - 2 32bit Universal Timers (TimerA)
  - 4 16bit Universal Timers (TimerA)
  - 4 16-bit Universal Timers (Timer2)
  - 2 16-bit Basic Timers (Timer0)
  - Real-time Clock Timer (RTC)
  - 2 WDTs, support internal dedicated clock
- **Up to 85 GPIOs**
  - Up to 59 5V-tolerant IOs
- **Up to 19 communication interfaces**
  - 6 USARTs, support ISO7816-3 protocol
  - 4 SPIs
  - 3 I2Cs, support SMBus protocol
  - 1 QSPI, supports 60 Mbps high-speed access (XIP)
  - 3 CANs, support CAN2.0B, CAN FD
  - 1 USB 2.0, built-in FS-PHY, support Device/Host
  - 1 MDIO
- **External Memory Controller EXMC**
  - Support static Memory controller
- **Data Encryption Function**
  - AES/ HASH(SHA256/ HMAC) / TRNG
- **Passed AEC-Q100 G2 Test**
- **Encapsulation Form:**
  - LQFP100(14×14 mm)
  - LQFP48(7×7 mm)

Support Model:

HC32A472PETI-LQFP100	HC32A472JETI-LQ48

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1 Overview

The HC32A472 product family is a high-performance MCU based on ARM® Cortex®-M4 32-bit RISC CPU with a maximum operating frequency of 120 MHz. The Cortex-M4 core integrates a floating-point arithmetic unit (FPU) and a DSP to implement single-precision floating-point arithmetic operations, supports all ARM single-precision data processing instructions and data types, and supports the complete DSP instruction set. The kernel integrates the MPU unit and superimposes the DMAC dedicated MPU unit at the same time to ensure the safety of system operation.

HC32A472 series integrates high-speed on-chip memory, including a maximum of 512 KB Flash, a maximum of 64 KB SRAM, and 4 KB of power-off retention SRAM . Integrated Flash access acceleration unit to achieve single cycle program execution of the CPU on Flash. The polled bus matrix supports multiple bus hosts to access memory and peripherals simultaneously, improving performance. The bus host includes CPU, DMA, and USB-dedicated DMA. In addition to the bus matrix, it supports data transfer between peripherals, basic arithmetic operations and mutual triggering of events, which can significantly reduce the transaction processing load of the CPU.

The HC32A472 series integrates rich peripheral functions Includes: 3 independent 12-bit 2.5 MSPS ADCs; 2 gain-adjustable PGAs; 1 12- bit DAC; 2 high - speed voltage comparators (CMP); 10 multi-function PWM Timers (Timer6) supporting 20 complementary PWM outputs; 1 motor PWM Timer (Timer4) supporting 3 complementary PWM outputs; 4 16-bit universal Timers (TimerA) and 2 32 -bit universal Timers (TimerA) supporting orthogonal encoding input and 24 -way duty independently settable PWM outputs; 13 serial communication interfaces (I2C /UART/SPI); 1 QSPI interface; 3 CANs; USBFS Controller with built - in USBFS PHY; 1 external expansion bus controller, including SMC controller; 1 mathematical operation unit (MAU) and 4 filter math accelerators (FMAC).

The HC32A472 product family supports wide voltage range (1.8-3.6V), wide temperature range (-40-105 °C) and each low power mode.

Typical Application

The HC32A472 series provides 100-pin and 48-pin LQFP packages and is mainly used in application scenarios such as automotive body, intelligent network connection, and infotainment.

1.1 Model Naming Rules

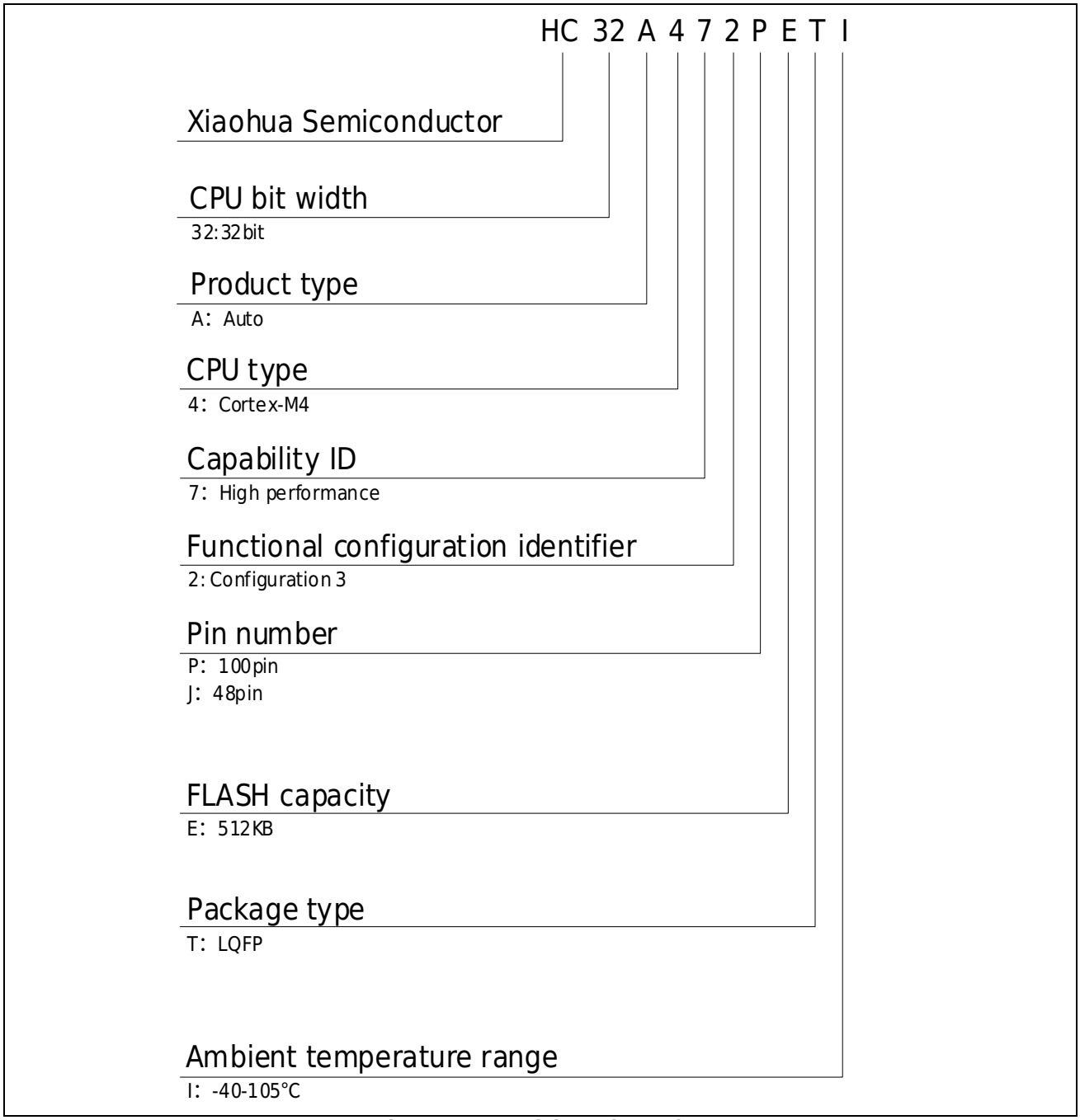


Figure 1-1 Model Naming Rules

1.2 Model Function Comparison Table

Table 1-1 Model Function Comparison Table

Function		Product Model	
		HC32A472JETI	HC32A472PETI
Pin number		48	100
Number of GPIOs		39	85
5V Tolerant Number of GPIOs		29	59
Encapsulation		LQFP	
Temperature range		-40~105 ℃	
Power voltage range		1.8~3.6 V	
Memory	Flash	512	
	OTP	134 KByte	
	SRAM	68 KB	
DMA		2unit * 8ch	
External port interrupt		EIRQ * 16vec	
Communcation Interfaces	UART	6ch	
	SPI	4ch	
	MDIO	1ch	
	I2C	3ch	
	CAN FD	3ch	
	QSPI	1ch	
	USB FS	1ch	
Timers	Timer0	2unit	
	Timer2	4unit	

Function		Product Model	
		HC32A472JETI	HC32A472PETI
Timers	TimerA	6unit	
	Timer4	1unit	
	Timer6	10unit	
	WDT	1ch	
	SWDT	1ch	
	RTC	1ch	
Analog	12bit ADC	3unit, 21ch	3unit, 27ch
	12bit DAC	2ch	
	PGA	2ch	
	CMP	2ch	
	OTS	✓	✓
DCU		✓	
FMAC		✓	
MAU		✓	
AES256		✓	
HASH(SHA256)		✓	
TRNG		✓	
EXMC		-	✓
PLA		✓	
Frequency monitoring module (FCM)		✓	
Programmable voltage detection function (PVD)		✓	
Debug Interface		SWD	
		JTAG	

1.3 Functional Block Diagram

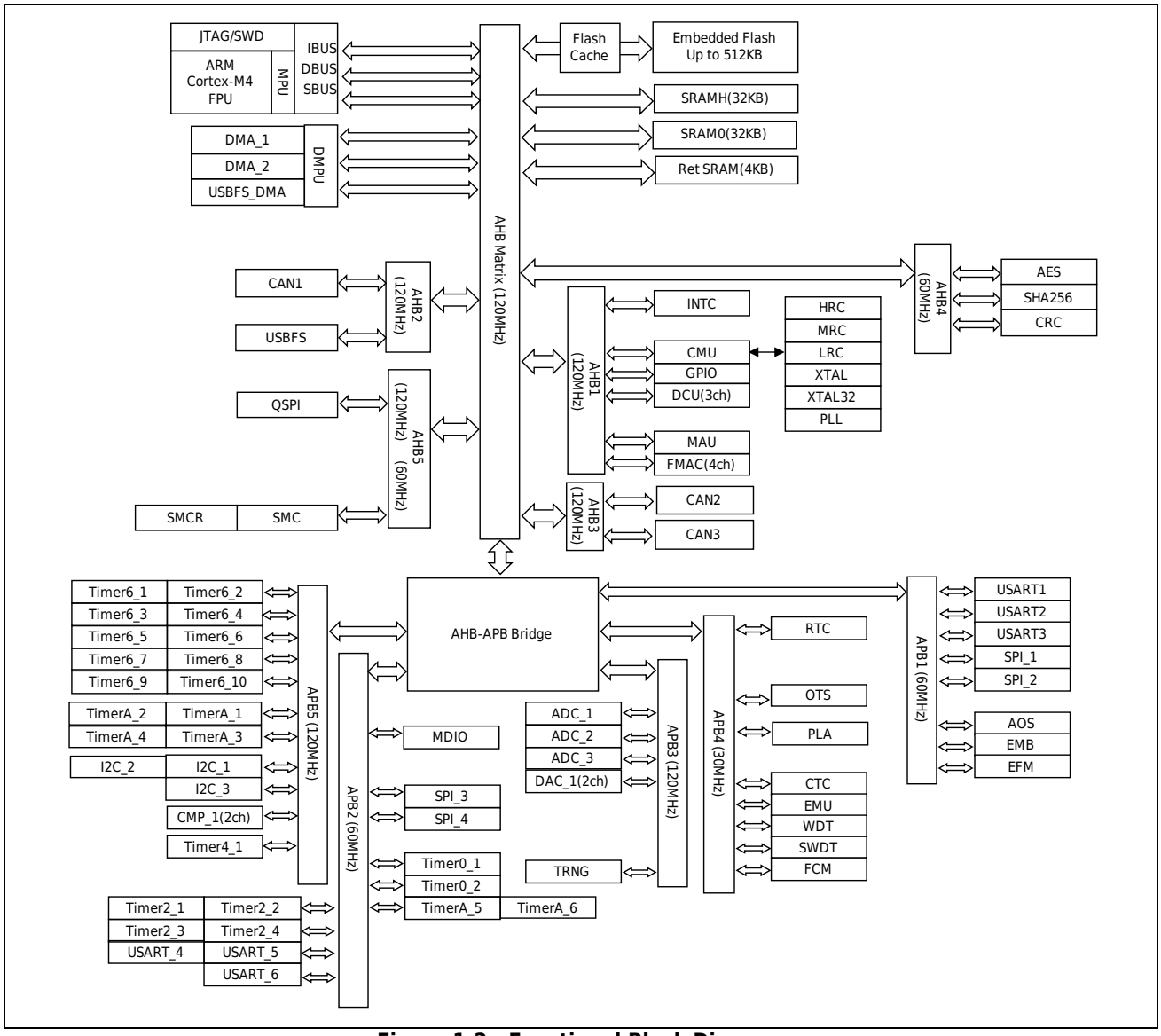


Figure 1-2 Functional Block Diagram

1.4 Function Introduction

1.4.1 CPU

The HC32A472 series integrates the latest generation of embedded ARM® Cortex®-M4 with FPU 32bit, which realizes fewer pins and lower power consumption while providing excellent computing performance and rapid interrupt response capability. The on-chip integrated memory capacity can fully utilize the excellent instruction efficiency of the ARM® Cortex®-M4 with FPU. The CPU supports DSP instructions, which can realize efficient signal processing operations and complex algorithms. The single-point precision FPU (Floating Point Unit) unit can avoid instruction saturation and speed up software development.

1.4.2 Bus Architecture (BUS)

The main system is composed of 32-bit multilayer AHB bus matrix, which can interconnect the following Host bus and slave bus.

- Host bus
  - Cortex-M4F core CPU-I bus, CPU-D bus, CPU-S bus
  - System DMA_1 bus, system DMA_2 bus
  - USBFS_DMA bus
- Slave bus
  - Flash ICODE bus
  - Flash DCODE bus
  - Flash MCODE bus (the bus used by masters other than the CPU to access Flash)
  - High-speed SRAMH (SRAMH 32 kB) bus
  - System SRAM (SRAM0 32 kB) bus
  - System SRAM (Ret SRAM 4KB) bus
  - APB2 Peripheral bus (EMB/ Timers/ SPI/ USART/ AOS/ EFM)
  - APB2 Peripheral bus (Timers/ SPI/ USART/ SPI/ MDIO)
  - APB3 peripheral bus (ADC/ DAC/TRNG)
  - APB4 peripheral bus (FCM/ WDT/ SWDT/ EMU/ CTC/ OTS/ RTC/ PLA)
  - APB5 peripheral bus (Timers/ CMP/ I2C)
  - AHB1 peripheral bus (DMPU/ KEYSCAN/ INTC/ DCU/ GPIO/ DMA/ CMU/ MAU/ FMAC)
  - AHB2 peripheral bus (CAN1/ USBFS)
  - AHB3 peripheral bus (CAN2/ CAN3)
  - AHB4 peripheral bus (AES/HASH/CRC)
  - AHB5 peripheral bus (SMC/ SMCR/ QSPI)

With the help of the bus matrix, high -efficiency concurrent access from the Host bus to the slave bus can be realized.

1.4.3 Reset Control (RMU)

The chip is configured with 15 reset modes:

- Power-on reset (POR)
- NRST pin reset (NRST)
- Brown-out Reset (BOR)
- Programmable voltage detect 1 reset (PVD1R)
- Programmable voltage detect 2 reset (PVD2R)
- Watchdog reset (WDTR)
- Special watchdog reset (SWDTR)
- Power-down wake-up reset (PDRST)
- Software reset (SRST)
- MPU error reset (MPUR)
- RAM odd-even check reset (RAMPR)
- RAMECC reset (RAMECCR)
- Clock exception reset (CKFER)
- External High Speed Oscillator Abnormal Shock Reset (XTALER)
- Cortex-M4 LOCKUP reset (LKUPR)

1.4.4 Clock Control (CMU)

The clock control unit provides a series of frequency clock functions, including an external high-speed oscillator, an external low-speed oscillator, a PLL clock, aninternal high-speed oscillator, an internal medium-speed oscillator, an internal low-speed oscillator, an SWDT dedicated internal low-speed oscillator, clock prescaler, clock multiplexing and clock gating circuits.

The clock control unit also provides a clock frequency measurement function. The clock frequency measurement circuit (FCM) monitors and measures the measurement target clock using the measurement reference clock. An interrupt or reset occurs when the set range is exceeded.

AHB, APB and Cortex-M4 clocks are all derived from the system clock. The system clock source can select 6 clock sources:

1. External high-speed oscillator (XTAL)
2. External low-speed oscillator (XTAL32)
3. PLLH clock (PLLH)
4. Internal high-speed oscillator (HRC)
5. Internal medium speed oscillator (MRC)
6. Internal low-speed oscillator (LRC)

The maximum operating clock frequency of the system clock can reach 120 MHz. SWDT has an independent clock source: SWDT dedicated internal low-speed oscillator (SWDTLRC). The real-time

clock (RTC) uses an external low-speed oscillator or an internal low-speed oscillator as a clock source. 48MHz clock of USB-FS can select the system clock PLLH as the clock source.

For each timer, you can turn it on and off separately when not in use to reduce power consumption.

1.4.5 Power Control (PWC)

Power controller is used to control the supply, switching and detection of multiple power domains in multiple operation modes and low power modes. The power controller is composed of power control logic (PWC) and power voltage detection unit (PVD).

The operating voltage (VCC) of the chip is 1.8 V to 3.6 V. A voltage regulator (LDO) supplies power to the VDD and VDDR domains, and a VDDR voltage regulator (RLDO) supplies power the VDDR domain in power-down mode. The chip provides two operating modes: high speed and ultra-low speed, and three low power modes: sleep, stop and power-off through the power consumption control logic (PWC).

The power voltage detection unit (PVD) provides functions such as power-on reset (POR), power-down reset (PDR), brown-out reset (BOR), programmable voltage detection 1 (PVD1), and programmable voltage detection 2 (PVD2). Among them, POR, PDR, and BOR control the reset action of the chip by detecting the VCC voltage. PVD1 detects the VCC voltage and resets or interrupts the chip according to the register settings. PVD2 detects VCC voltage or external input detection voltage, and generates reset or interrupt according to register selection.

After the chip enters power-down mode, the VDDR area can maintain power through RLDO to ensure that the real-time clock module (RTC) and wake-up timer (WKTM) can continue to operate, and keep the data of 4KB RetSRAM. The analog blocks are equipped with dedicated supply pins for improved analog performance.

1.4.6 Initialization Configuration (ICG)

After the chip reset is released, the hardware circuit will read the FLASH address 0x0000 0400H~0x000 0045FH and load the data into the initialization configuration register. Addresses 0x0000 0408~0x0000 040B, 0x0000 0414~0x0000 041F, and 0x0000 0438~0x0000 045F are reserved addresses. Please write all 1s to ensure normal operation of the chip. When FLASH boot swap is invalid, the area contains FLASH block 0 sector 0; when FLASH boot swap is valid, the area contains FLASH block 1 sector 0 . Users can modify the initial configuration (Initial ConfiG) register by programming or erasing sector 0. Address 0x0000 0420~0x0000 0437 is the data security protection enable area. The register reset value is determined by the FLASH address data.

1.4.7 Embedded FLASH Interface (EFM)

The FLASH interface accesses the FLASH through the ICODE, DCODE, and MCODE buses, and can perform programming, erasing, and full-erase operations on the FLASH; it accelerates code execution through instruction prefetching and caching mechanisms.

Main Features:

- Two independent FLASHs form a dual bank, which can realize the BGO (background operation) function
- Maximum 134 Kbytes of OTP space
- ICODE bus 16 Bytes prefetched instruction
- Two independent buffers: ICODE bus buffer space 2 Kbytes; DCODE bus buffer space 256 bytes
- Support boot swap function
- Support data security protection

1.4.8 Built-in SRAM (SRAM)

This product has 64KB system SRAM (SRAMH/SRAM0) and 4KB power-down mode retention SRAM (Ret SRAM).

Each SRAM can be accessed as a byte, half-word (16 bits), or full-word (32 bits). All SRAM (SRAMH/ SRAM0/ Ret SRAM) read and write operations can be performed at the fastest CPU speed (120 MHz).

Ret SRAM can provide 4KB of data retention space in Power Down mode.

SRAM0 and Ret SRAM have ECC (Error Checking and Correcting) check.The ECC check is a one-correction-two-check code, which can correct one-bit error and check two-bit error. SRAMH has an even -odd-even check.Each byte of data has a check bit.

1.4.9 Universal IO (GPIO)

Main Features of GPIO:

- Each port group has 16 I/O Pins, which may be less than 16 depending on actual configuration
- Support pull-up and pull-down
- Support push-pull, open-drain output mode
- Support high, medium and low drive modes
- Supports free switching between CMOS/Schmitt input modes
- Support for external interrupt input
- Supports I/O pin peripheral function multiplexing, each I/O pin has up to 64 selectable multiplexing functions
- Individual I/O pins can be programmed independently
- Each I/O pin can select 2 functions to be valid at the same time (does not support 2 output functions to be valid at the same time)

1.4.10 Interrupt Control (INTC)

The interrupt controller (INTC) selects interrupt events as interrupt requests to NVIC to wake up WFI; selects interrupt events as event inputs (RXEV) to wake up WFE; selects interrupt events to wake up the system in low power mode (sleep mode and stop mode); controls external interrupts and software interrupts.

The main specifications of INTC are as follows:

- NVIC interrupt request: The Cortex-M4 NVIC supports up to 240 interrupt requests (IRQ), each IRQ corresponds to one or more interrupt events
  For more instructions on exceptions and NVIC programming, please refer to Chapter 5: Exceptions and Chapter 8: Nested Vectored Interrupt Controller in the "ARM Cortex™-M4F Technical Reference Manual".
- Programmable priority: 16 programmable priorities (4-bit interrupt priority register is used).
- Non-maskable interrupts: Multiple system interrupt events can be independently selected as non-maskable interrupts, and each interrupt event is equipped with independent enable selection, flag, and flag clear registers.
- Equipped with 16 external pin interrupt events.
- Equipped with up to 512 interrupt events
- Equipped with 32 software interrupt events.
- Interrupt wakes up system sleep mode and stop mode.

1.4.11 Automatic Operation System (AOS)

The automatic operation system (Automatic Operation System) is used to realize the linkage between peripheral hardware circuits without the help of the CPU. Use the events generated by the peripheral circuit as the AOS source (AOS Source), such as the comparison and matching of the timer, timing overflow, the periodic signal of the RTC, and the various states of the communication module's sending and receiving data (idle, receiving data full, sending data end, Send data empty), ADC conversion end, etc., to trigger other peripheral circuit actions. The triggered peripheral circuit action is called AOS target (AOS Target).

1.4.12 Memory Protection Unit (MPU)

The MPU can provide protection to the memory, and can improve the security of the system by preventing unauthorized access.

his chip has built-in 1 MPU unit for CPU, 1 MPU unit for CPU main stack pointer, 1 MPU unit for CPU thread stack pointer, 3 MPU units for DMA and 1 MPU unit for IP.

Among them, the ARM MPU provides the access control of the CPU to the entire 4G address space.

MSPMPU/PSPMPU respectively provide protection for the CPU's main stack pointer/thread stack pointer. When the pointer exceeds the set range, the MPU action can be set to non-maskable interrupt/reset.

SMPU1/SMPU2/FMPU respectively provide system DMA_1/system DMA_2/USBFS-DMA to control the read and write access rights of the entire 4G address space. When accessing the prohibited space, the MPU action can be set to ignore/bus error/non-maskable interrupt/reset.

The IP MPU provides access control to system IP and security-related IP in non-privileged mode.

1.4.13 Keyboard Scanning (KEYSCAN)

This product is equipped with a keyboard control module (KEYSCAN) 1 unit. The KEYSCAN module supports keyboard array (row and column) scanning, the column is driven by an independent scan output KEYOUTm (m=0~7), and the row KEYINn (n=0~15) is input as EIRQn (n=0~15) is detected. This module realizes the key recognition function through the line scan query method.

1.4.14 Internal Clock Calibrator (CTC)

The Clock Trimming Controller (CTC) automatically calibrates the internal high-speed oscillator (HRC). Because the influence of working environment on HRC frequency may cause deviation, CTC can automatically adjust HRC frequency by hardware based on external high precision reference clock to obtain an accurate HRC clock.

The main features of CTC are as follows:

- Three external reference clock sources: XTAL, XTAL32, CTCREF
- 16-bit calibration counter for frequency measurement with heavy load function
- 8-bit calibration deviation and 6-bit calibration values for frequency calibration
- Error interrupt to prompt calibration failure

1.4.15 DMA Controller (DMA)

DMA is used to transfer data between memory and peripheral functional modules. It can exchange data between memory, between memory and peripheral functional modules and between peripheral functional modules without CPU involvement.

- DMA bus is independent of CPU bus and transmitted according to AMBA AHB-Lite bus protocol.
- With 2 DMA control units, a total of 16 independent channels, which can independently operate different DMA transfer functions
- For each channel, the source of the boot request is configured via a separate trigger source
- One block per request
- The data block is a minimum of one data and can be up to 1024 data
- The width of each data can be configured as 8 bit, 16 bit or 32 bit
- Up to 65535 transmissions can be configured

- The source address and target address can be independently configured as fixed, auto-increment, auto-decrement, loop or jump with a specified offset
- Three types of interrupts can be generated： block transport complete interrupt, transport complete interrupt and transport error interrupt. Each interrupt can be configured with a mask or not. Among them, the block transmission is completed, and the transmission completion can be used as an event output, which can be used as a trigger source for other peripheral modules
- Support for linked transmission to enable multiple blocks of data to be transmitted at a time
- Support channel reset triggered by external events
- You can set the module stop state to reduce power consumption when not in use

1.4.16 Voltage Comparator (CMP)

The voltage comparator (CMP) is a peripheral module that compares two analog voltages and outputs the comparison result. It provides 1 group of 2 comparison channels: CMP1/CMP2.

CMP has the following main features:

- 2 comparison channels can perform common comparison independently
- The combination of two comparison channels in the same group can realize up to one group of window comparison mode
- Each comparison channel has multiple input sources (IO/PGA/DAC) for selection of positive/negative voltage
- Noise filter can filter the comparator output, 7 sampling clocks are optional
- Timer PWM can be used to output the comparator blank window control
- Can generate interrupts at the changing edge of the comparison result, trigger other peripherals, and wake up STOP mode
- The comparison result can be monitored through the register and can also be output to the external pin VCOUT
- The comparison result can be used for emergency brake (EMB) and timer blank window control events
- The comparator output keeps on when software reset and watchdog reset occur.
- Hysteresis function

1.4.17 Analog-to-Digital Converter (ADC)

12-bit ADC is an analog-to-digital converter with successive approximation. This MCU is equipped with 3 ADC units, each unit supports up to 18 channels, and can convert analog signals from external pins and inside the chip. The analog input channels can be arbitrarily combined into a sequence, and a sequence can be converted in a single scan or in a continuous scan. It supports multiple consecutive conversions on any specified channel and averages the conversion results.

The ADC module is also equipped with an analog watchdog function to monitor the conversion result of any specified channel to detect whether it exceeds the range set by the user.

Main Features of ADC:

- High performance
  - Configurable 12-bit, 10-bit and 8-bit resolution
  - The frequency ratio of the ADC digital interface clock PCLK4 and the conversion clock PCLK2 (also called ADCLK) can be set to 1:1, 2:1, 4:1, 8:1, 1:2, 1:4
    PCLK2 can be a PLL clock asynchronous with the system clock HCLK. In this case, the frequency ratio of PCLK4: PCLK2=1:1
    PCLK2 frequency supports up to 60 MHz
  - Sampling rate: 2.5 MSPS (PCLK2 = 60 MHz, 12 bits, sampling 11 cycles, conversion 13 cycles)
  - The sampling time of each channel is independently programmed
  - Channel-independent data register
  - Data registers can be configured with left/right alignment
  - Consecutive multiple conversion average function
  - Simulation watchdog, monitoring conversion results
  - The ADC module can be set to stop when not in use
- Analog input channel
  - Maximum 27 external analog input channels
  - One internal analog input: internal reference voltage
- Conversion start condition
  - Software setup conversion started
  - Start of peripheral device synchronization trigger conversion
  - External pin triggering start
- Conversion mode
  - 2 scan sequences A and B, optionally specifying a single or multiple channels
  - Sequence A single scan
  - Sequence A continuous scanning
  - Double sequence scanning, sequence A and B independently select trigger source, sequence B has higher priority than A
  - Co-working mode (For devices with two or three ADCs)
- Interrupt and event signal output
  - Sequence A scan end interrupt and event ADC _ EOCA
  - Sequence B scan end Interrupt and event ADC _ EOCB
  - Analogwatchdog 0 compared interrupt and event ADC _ CMP0
  - Simulation watchdog 1 comparing interrupt and event ADC _ CMP1
  - All four of these event outputs can start the DMA

This MCU is equipped with 2 unit programmable gain amplifiers PGA, with a selectable gain range of x2~x32 . The analog input can be amplified by the PGA circuit first and then input to the ADC module for conversion.

1.4.18 Digital to Analog Converter (DAC)

This MCU is equipped with a 12 - bit conversion precision digital-to-analog converter unit DAC1, which includes two D/A conversion channels that can be converted independently or synchronously. The analog voltage output range can be set in two levels.

The main features of the DAC are as follows:

- 1 DAC unit, including two D/A conversion channels
- 12-bit conversion data can be configured as left-aligned or right-aligned format
- The two conversion channels of the same DAC unit can be converted synchronously
- Independent reference voltage VREFH is used to improve conversion accuracy
- The output can be used as the negative input of the voltage comparator (CMP)
- A/D conversion priority mode can reduce interference during ADC conversion
- Software reset / watchdog reset DAC output hold

1.4.19 Temperature Sensor (OTS)

OTS can obtain the temperature inside the chip to support the reliability operation of the system. After using software or hardware to trigger the temperature measurement, OTS provides a set of temperature-related digital quantities, and the temperature value can be calculated through the calculation formula.

1.4.20 Advanced Control Timer (Timer6)

Advanced Control Timer 6 (Timer6) is a high-performance timer with a 16-bit count width, which can provide rich and flexible combinations and various interrupts, events, and PWM outputs in various complex application scenarios. The timer supports two waveform modes, sawtooth wave and triangle wave, and can generate various PWM waveforms (single-side aligned independent PWM, bilateral symmetrical independent PWM, bilateral symmetrical complementary PWM, bilateral asymmetrical PWM, etc.); software synchronization and hardware synchronization (synchronous start, stop, clear, refresh, etc.) can be achieved between units; each reference value register supports cache function (single-level cache and double-level cache); supports pulse width measurement and period measurement; supports 2-phase orthogonal encoding and 3-phase orthogonal encoding; supports EMB control. This series of products is equipped with 10 units of Timer6 (U1~10 are 16-bit timers).

1.4.21 Universal Control Timer (Timer4)

Universal control timer 4 (Timer4) is a timer module for three-phase motor control. It provides three-phase motor control schemes for various applications. The timer supports triangular wave and sawtooth wave modes and generates various PWM waveforms. Supporting cache function; Support EMB control. 1 unit of Timer 4 is carried in this product family.

1.4.22 Emergency Brake Module (EMB)

The emergency brake module is a functional module that generates a control event and outputs it to the timer when certain conditions are met, so as to control the timer to stop outputting PWM signals to the external motor. The following factors are used to generate control events:

- Change of input level of external port
- Level of PWM output port occurs in phase (same high or same low)
- Voltage comparator comparison results
- System Error
- Write register software control

1.4.23 Universal Timer (TimerA)

Universal timer A (TimerA) is a timer with 16/32-bit count width and 4-channel PWM output. The timer supports two waveform modes, triangle wave and sawtooth wave, and can generate various PWM waveforms (single-side aligned PWM, double-side symmetrical PWM); supports synchronous start of counter; the Comparison Reference Value Register supports cache function; supports inter-unit cascade counting; supports 2-phase orthogonal encoding counting and 3-phase orthogonal encoding counting. This series of products is equipped with 6 units of TimerA (U1~U2 are 32-bit timers; U3~U6 are 16-bit timers), which can achieve a maximum of 24 PWM outputs .

1.4.24 Universal Timer (Timer2)

Universal timer 2 (Timer2) is a basic timer that can implement synchronous counting and asynchronous counting. This timer contains 2 channels (CH-A and CH-B). Each channel has an output port for basic square wave output; each channel has two input ports, one is the clock input port for asynchronous port counting; the other is the trigger input port for timer start, stop, reset, counting action and count value capture input; supports pulse width measurement and period measurement. 4 unit of Timer 2 is carried in this product family.

1.4.25 Universal Timer (Timer0)

Universal timer 0 (Timer0) is a basic timer that can implement synchronous counting and asynchronous counting. The timer contains 2 channels (CH-A and CH-B), which can generate compare match events during counting. The event can trigger interrupt, or can be output as an event to control other modules. This series of products is equipped with 2 units of Timer0.

1.4.26 Real Time Clock (RTC)

The real-time clock (RTC) is a counter that stores time information in BCD format. Record the specific calendar time from 00 to 99. Support 12/24 hour time system, automatically calculate the number of days 28, 29 (leap year), 30 and 31 Yes according to the month and year.

1.4.27 Watchdog Counter (WDT)

There are two watchdog timers, one is the special watchdog timer timerr (SWDT) whose counting clock source is dedicated internal RC (SWDTLRC: 10KHz), and the other is the universal watchdog timer (WDT) whose counting clock source is PCLK3 . The special watchdog and universal watchdog are 16-bit down counters used to monitor software failures due to external disturbances or unforeseen logic conditions that deviate from the normal operation of the application program.

Both watchdogs support window functions. The window interval can be preset before the count starts, and when the count value is within the window interval, the counter can be refreshed and the count restarted.

1.4.28 Serial Communication Interface (USART)

This product is equipped with 6 units of universal serial transceiver module (USART). The universal serial transceiver module (USART) can flexibly exchange full-duplex data with external devices; this USART supports the universal asynchronous serial communication interface (UART), clock synchronous communication interface, smart card interface (ISO/IEC7816-3) and LIN communication interface. Support modem operation (CTS/RTS operation), multiprocessor operation. Cooperate with Timer0 module to support UART receive TIMEOUT function. USART_1 supports the STOP mode wake-up function via the RX line.

The specific functions are allocated as follows:

- UART: Full channel support
- Multiprocessor communications: full channel support
- Clock synchronous communication: full channel support
- RX line wake-up STOP mode function: USART_1 support
- Fractional baud rate: all channels support
- LIN: USART_3, USART_6 supported
- Smart Card: USART_1, USART_2, USART_4, USART_5 support
- UART receive timeout function: supported by USART_1, USART_2, USART_4, USART_5

1.4.29 Integrated Circuit Bus (I2C)

I2C (Integrated Circuit Bus) is used as an interface between the microcontroller and the I2C serial bus. Provide multi-master mode function, which can control the protocol and arbitration of all I2C buses. Supports standard mode, fast mode, and SMBus bus.

I2C main features:

- I2C bus mode and SMBUS bus mode are optional. Host mode and slave mode are optional. Automatically ensure various preparation times, hold times, and bus idle times corresponding to the transfer rate
- Standard mode up to 100 Kbps, Fast mode up to 400 Kbps, FM+ mode up to 1 Mbps
- The start condition, restart condition, and stop condition are automatically generated, and the start condition, restart condition, and stop condition of the bus can be detected.
- Supports up to 128 slave addresses. Supports 7-bit address format and 10-bit address format. Broadcast call address, SMBus host address, SMBus device default address, SMBus alarm address can be detected
- Answer bits can be automatically determined when sent. Answer bits can be sent automatically upon reception
- Handshake function
- Arbitration function
- Timeout function, can detect SCL clock stop for a long time
- SCL input and SDA input have built-in digital filters that are programmable to filter
- Communication error, receive data full, send data empty, one frame send end, address match unanimously interrupt
- 2- level transmit/receive FIFO

1.4.30 Serial Peripheral Interface (SPI)

This product is equipped with 4-channel serial peripheral interface SPI, supports high-speed full-duplex serial synchronous transmission, and facilitates data exchange with peripheral devices. Users can set the range of 3/4-wire, host/slave and baud rate as needed.

Table 1-2 SPI Main Features

Essentials	Description
Serial communication function	• Supporting 4-wire SPI mode and 3-wire clock synchronization mode • Supports full-duplex and send-only communication modes • Polarity and phase of adjustable communication clock SCK
Data format	• Selectable data shift sequence: MSB first/LSB first • Selectable data width: 4/5/6/7/8/9/10/11/12/13/14/15/16/20/24/32 bit • Up to 4 frames of data with a width of 32 bits can be transmitted or received at a time
Baud rate	• The baud rate can be adjusted by the built-in special baud rate generator in host mode. The baud rate ranges from 2 to 256 frequency division of PCLK1. • The maximum baud rate allowed in slave mode is PCLK1 divided by 6
Data buffer	• Data buffer area with 16 bytes • Supports double buffering
Error monitoring	• Mode fault error monitoring • Data overload error monitoring • Data underload error monitoring • Odd-even error monitoring
Chip selection signal control	• Each channel is configured with excluding chip-selected signal line • The relative timing relationship between the chip select signal and the

Essentials	Description
	communication clock can be adjusted • The invalid time of the chip select signal between two consecutive communications can be adjusted • Polarity adjustable
Transmission control in host mode	• Start transmission by writing data to the data register • Communication auto suspend function
Interrupt	• Received data area full • Sending data area is empty • SPI error (mode/overload/underload/odd-even) • SPI idle • Transfer completed (event sources only)
Low power control	• Configurable module stop
Other functions	• SPI initialization function

1.4.31 Quad-wire Serial Peripheral Interface (QSPI)

The Quad Serial Peripheral Interface (QSPI) is a memory control module designed to communicate with serial ROMs with an SPI-compatible interface. Its objects mainly include serial flash memory, serial EEPROM and serial FeRAM.

1.4.32 USB2.0 Full Speed Module (USBFS)

The USB Full Speed (USBFS) controller provides a set of USB communication solutions for portable devices. The USBFS controller supports host mode and device mode, and a full-speed PHY is integrated inside the chip. In host mode, the USBFS controller supports full-speed (FS, 12Mb/s) and low-speed (LS, 1.5Mb/s) transceivers, while in device mode it only supports full-speed (FS, 12Mb/s) transceivers . The USBFS controller supports all four transmission methods defined by the USB2.0 protocol (control transmission, batch transmission, interrupt transmission and synchronous transmission).

1.4.33 Programmable Logic Array (PLA)

The Configurable Logic Array provides 256 programmable digital logic operations to external pins without CPU intervention. This module implements 16 independent PLA units.

1.4.34 CAN FD Controller (CAN FD)

CAN FD controller complies with the CAN bus CAN2.0 (2.0A, CAN2.0B) and CAN FD protocol.

The CAN bus controller can process the data transmission and reception on the bus. In this product, the CAN FD controller has 16 groups of acceptance filters. The acceptance filters are used to select messages for an application to receive.

The application program in the CAN FD bus controller sends the transmission data to the bus through a high-priority Primary Transmit Buffer (PTB) and 3 Secondary Transmit Buffers (STB). The sending scheduler determines the mailbox sending order. The bus data is obtained through 8 receive buffers (Receive Buffer, hereinafter referred to as RB). 3 STBs and 8 RBs can be understood as a 3-level FIFO and a 8-level FIFO, and the FIFO is completely controlled by hardware.

The CAN FD bus controller can also support time-triggered CAN communication (Time-trigger communication).

1.4.35 MDIO Serial Bus Interface (MDIO)

MDIO interface is included in the IEEE802.3 protocol and is a serial bus interface dedicated to the management of Ethernet PHY, using IEEE 802.3 Clause45 . The MDIO interface hardware can receive complete MDIO frames without software intervention. The MDIO interface hardware can also send complete MDIO frames without software intervention as long as the data to be sent is provided before the turnaround bit (TA) of a received read data frame or read post-increment address frame. To aid in the use and provision of relevant data, an interrupt is generated at the end of each complete frame. If the received PHYADR or DEVADD does not match the expected value, no action is taken on the frame. An interrupt can also be generated after each valid PHYADR and DEVADD to allow more complex control within the frame.

1.4.36 External Memory Controller EXMC

The external memory controller EXMC (External Memory Controller) is an independent module used to access various off-chip memories and realize data exchange. EXMC can convert the internal AMBA protocol interface into various types of dedicated off-chip memory communication protocol interfaces through configuration, including SRAM, PSRAM, NOR Flash, etc.

1.4.37 Cryptographic Coprocessing Module (CPM)

The encryption co-processing module (CPM) includes three sub-modules: AES encryption and decryption algorithm processor, HASH security hash algorithm, and TRNG true random number generator.

The AES encryption and decryption algorithm processor complies with the new data encryption standard officially announced by the National Institute of Standards and Technology (NIST) on October 2, 2000. The block length is fixed at 128 bits, while the key length supports 128/192/256 bits.

The HASH secure hash algorithm is the SHA-2 version of SHA-256 (Secure Hash Algorithm), which complies with the national standard "FIPS PUB 180-3" issued by the US National Institute of Standards and Technology, and can process messages with a length of no more than 2^64 bits. Produces a 256-bit message digest output.

TRNG is a random number generator based on continuous analog noise, providing 64-bit random numbers.

1.4.38 CRC Unit (CRC)

The CRC algorithm of this module complies with the definition of ISO/IEC 13239 and adopts 32-bit and 16-bit CRC respectively.

The generating polynomial of CRC32 is $X^{32}+ X^{26}+ X^{23}+ X^{22}+ X^{16}+ X^{12}+ X^{11}+ X^{10}+ X^{8}+ X^{7}+ X^{5}+ X^{4}+ X^{2}+ X+ 1$, and the 32-bit initial value is 0xFFFF FFFF.

The generating polynomial of CRC16 is $X^{16}+ X^{12}+ X^{5}+ 1$, and the 16-bit initial value is 0xFFFF.

1.4.39 Data Computing Unit (CRC)

The Data Computing Unit is a module that simply processes data without the help of a CPU. Each DCU unit has 3 data registers, which can add, subtract and compare the size of 2 data, as well as the window comparison function. This product is equipped with 3 DCU units, and each unit can independently complete its own functions.

1.4.40 Mathematical Arithmetic Unit (MAU)

The Mathematical Calculation Unit (MAU) is a hardware accelerated computing module that includes two types of operations: square root and sine operations. It supports square root and sine operations of fixed-point numbers. The sine function supports 360°/2^12 calculation accuracy.

1.4.41 Filter Math Accelerator (FMAC)

The Filter Math Accelerator (FMAC) is a hardware acceleration module for FIR filter calculations. This module can perform FIR digital filtering with a maximum order of 16 and configurable order . Built-in 16x16 bit multiplier and 32+5 bit adder, users can customize the output data precision. This series of products is equipped with 4 FMAC modules .

1.4.42 Debug Controller (DBGC)

The core of this MCU is Cortex™-M4F, which contains hardware for advanced debugging functions. With these debugging features, you can stop the kernel when fetching fingers (instruction breakpoints) or accessing data (data breakpoints). When the kernel stops, you can query the internal state of the kernel and the external state of the system. After the query completes, the kernel and system are restored and program execution is restored.

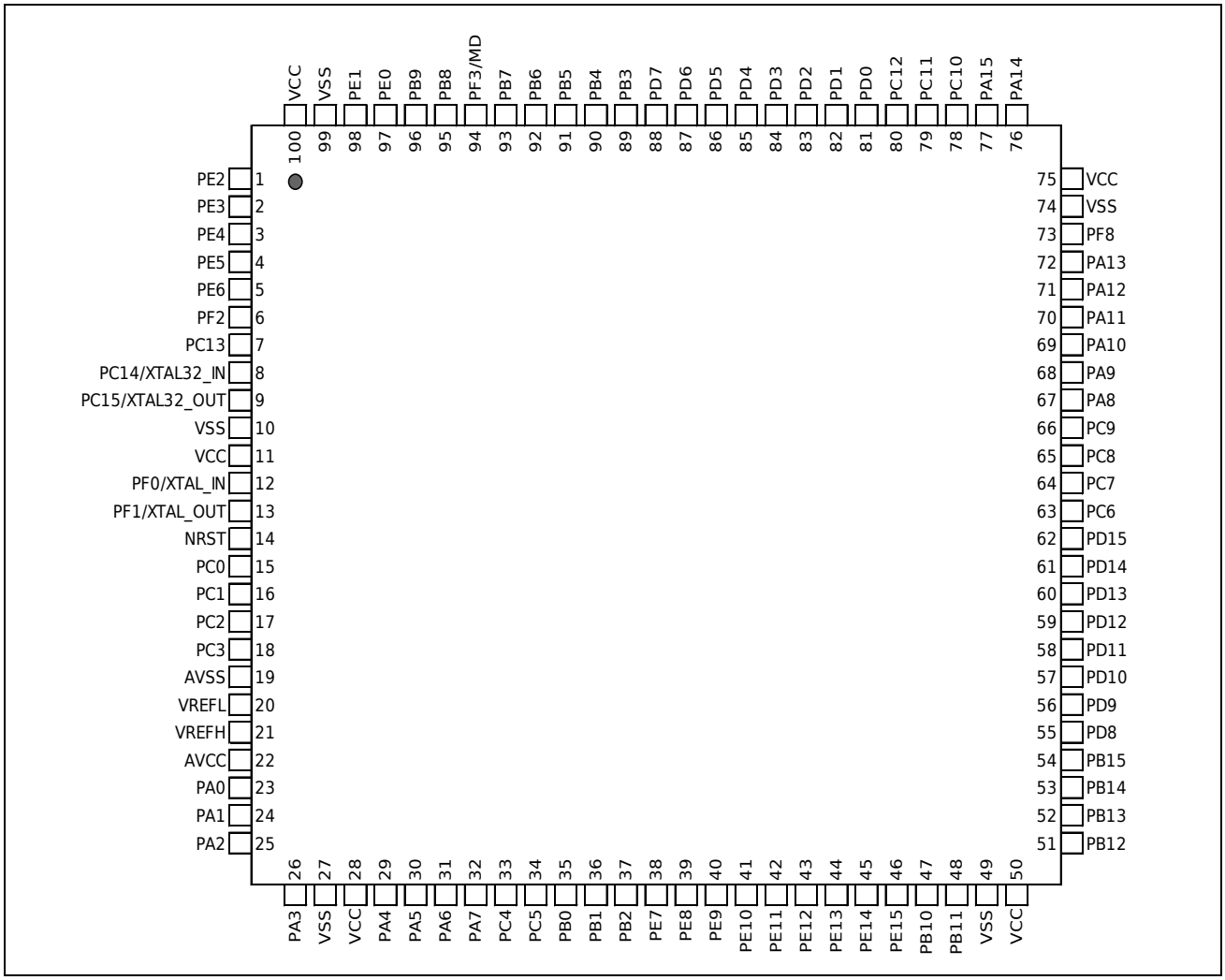
Two debugging interfaces are provided:

- Serial Debugging Tracking Interface SWD
- Parallel debug trace interface JTAG

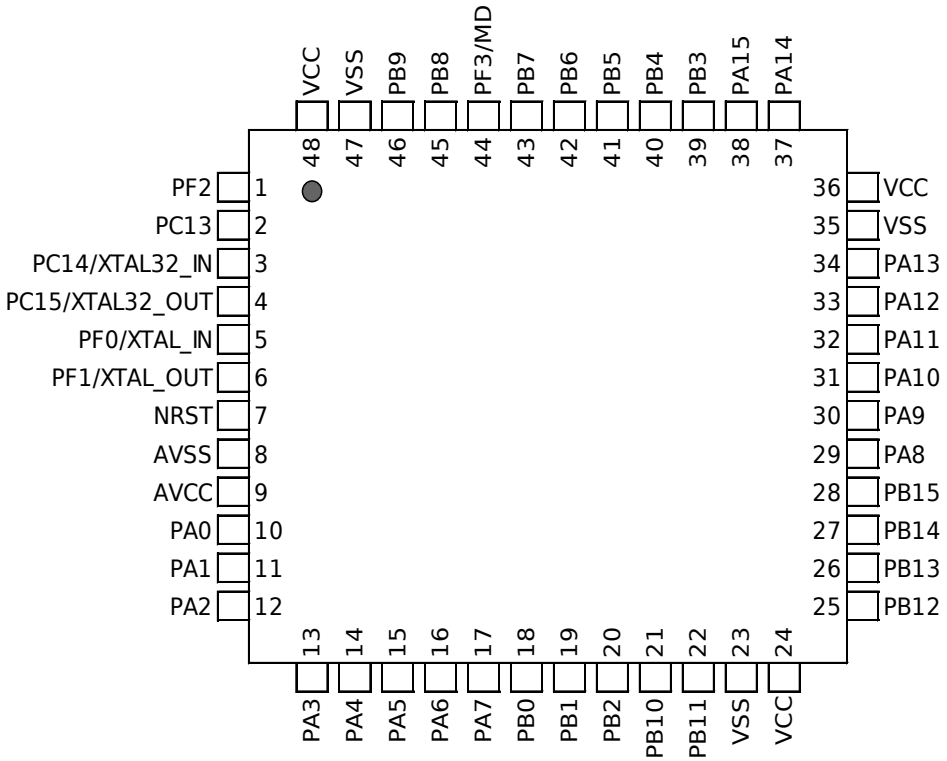
2 Pin Configuration and Functions (Pinouts)

2.1 Pin Configuration Diagram

LQFP100



LQPF48


VCC 48
VSS 47
PB9 46
PB8 45
PF3/MD 44
PB7 43
PB6 42
PB5 41
PB4 40
PB3 39
PA15 38
PA14 37
PF2 1
PC13 2
PC14/XTAL32_IN 3
PC15/XTAL32_OUT 4
PF0/XTAL_IN 5
PF1/XTAL_OUT 6
NRST 7
AVSS 8
AVCC 9
PA0 10
PA1 11
PA2 12
36 VCC
35 VSS
34 PA13
33 PA12
32 PA11
31 PA10
30 PA9
29 PA8
28 PB15
27 PB14
26 PB13
25 PB12
13 PA3
14 PA4
15 PA5
16 PA6
17 PA7
18 PB0
19 PB1
20 PB2
21 PB10
22 PB11
23 VSS
24 VCC

2.2 Pin Function Table

Table 2-1 Pin Function Table

LQFP48	LQFP100	Pin Name	Analog	EIRQ/WKUP	TRACE/ JTAG	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16	Func17	Func18	Func19	Func20	Func21	Func22	Func23	Func24	Func25	Func26	Func32~63
			-	-	-	GPO	I2C/ ADTRG	CMP/SPI/ KEY	EXMC/SPI	SPI/QSPI/ EXMC	QSPI/ KEY	SPI/KEY/ EMB	USART	USART	PLA	PLA/TIM6/ EMB	TIM6	TIM6/ EXMC	TIM6/ TIMA	TIM6/ TIMA	TIM6/ TIMA	TIM6/TIMA/ ADTRG	TIMA	TIMA/ TIM2	TIM2	TIM4/ CTC	TIM2/ EMB/CTC/ FCM	TIM2/ EMB/USB/ CMP	MDIO/ ADTRG	Other	EVENTOUT	EVENTPORT/ ADTRG	Communication Function Group
-	1	PE2	-	EIRQ2	TRACECLK	GPO	-	-	EXMC_ADD23	SPI4_NSS3	-	-	-	-	-	-	TIM6_4_PWMA	TIM6_4_PWMB	-	-	TIMA_5_PWM2/CLKB	TIMA_6_PWM1/CLKA	-	-	-	TIM4_1_OUH	-	-	-	-	-	-	FG1
-	2	PE3	-	EIRQ3	TRACED0	GPO	-	-	EXMC_ADD19	SPI4_NSS2	-	-	-	-	-	-	-	-	-	-	TIMA_5_PWM3	TIMA_6_PWM2/CLKB	-	-	-	TIM4_1_OUL	-	-	-	-	-	-	FG1
-	3	PE4	-	EIRQ4	TRACED1	GPO	-	-	EXMC_ADD20	SPI4_NSS1	-	-	-	-	-	-	-	-	-	-	TIMA_5_PWM4	TIMA_6_PWM3	-	-	-	TIM4_1_OVH	-	-	-	-	-	-	FG1
-	4	PE5	-	EIRQ5	TRACED2	GPO	-	-	EXMC_ADD21	SPI4_NSS0	-	-	-	-	-	-	-	-	-	TIMA_5_TRIG	TIMA_5_PWM1/CLKA	TIMA_6_PWM4	-	-	-	TIM4_1_OVL	-	-	-	-	-	-	FG1
-	5	PE6	-	EIRQ6	TRACED3	GPO	-	-	EXMC_ADD22	SPI4_SCK	-	-	-	-	-	-	-	-	-	TIMA_5_TRIG	TIMA_5_PWM2/CLKB	-	-	-	-	TIM4_1_CLK	-	-	-	-	-	-	FG1
1	6	PF2	-	EIRQ2	-	GPO	-	-	EXMC_ADD24	-	KEYOUT6	-	-	-	-	-	TIM6_10_PWMA	TIM6_10_PWMB	TIM6_TRIGB	-	TIMA_4_TRIG	-	-	-	-	TIM4_1_OWH	EMB_PORT4	-	-	-	-	-	FG2
2	7	PC13	-	EIRQ13+WKUP3_1	-	GPO	-	-	EXMC_ADD25	-	KEYOUT5	-	-	-	-	PLA3OUT	TIM6_7_PWMA	TIM6_7_PWMB	-	-	-	-	-	-	-	TIM4_1_OWL	-	-	-	RTC_OUT	-	EVNTP313	FG2
3	8	PC14	XTAL32_IN	EIRQ14	-	GPO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	TIM4_1_PCT	-	-	-	-	-	EVNTP314	-
4	9	PC15	XTAL32_OUT	EIRQ15	-	GPO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	TIM4_1_ADSM	-	-	-	-	-	EVNTP315	-
-	10	VSS	-	-	-		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	11	VCC	-	-	-		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
5	12	PF0	XTAL_IN/XTAL_EXT	EIRQ0	-	GPO	I2C1_SDA	-	EXMC_DATA27	-	-	-	-	-	PLAIN16	-	TIM6_9_PWMA	TIM6_9_PWMB	TIM6_TRIGC	-	-	-	-	-	-	TIM4_1_ADSM	-	-	-	-	-	-	-
6	13	PF1	XTAL_OUT	EIRQ1	-	GPO	I2C1_SCL	CMP1_OUT	EXMC_ADD29	-	-	-	-	-	PLAIN17	-	-	-	-	-	-	-	-	-	-	TIM4_1_PCT	-	-	-	-	-	-	-
7	14	NRST	-	-	-		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	15	PC0	ADC123_IN10	EIRQ0	-	GPO	-	-	EXMC_ADD0	SPI1_NSS3	KEYOUT4	-	-	-	-	PLA4OUT	TIM6_7_PWMB	TIM6_7_PWMA	-	TIMA_5_PWM1/CLKA	TIMA_6_PWM1/CLKA	-	-	-	-	-	-	-	-	-	EVENTOUT	EVNTP300	FG2
-	16	PC1	ADC123_IN11	EIRQ1	-	GPO	-	-	EXMC_ADD1	SPI1_NSS2	KEYOUT3	-	-	-	-	PLA5OUT	TIM6_8_PWMB	TIM6_8_PWMA	-	TIMA_5_PWM2/CLKB	TIMA_6_PWM2/CLKB	-	-	-	-	-	-	-	-	-	EVENTOUT	EVNTP301	FG2
-	17	PC2	ADC123_IN12	EIRQ2	-	GPO	-	SPI1_MISO	EXMC_ADD2	SPI1_NSS1	KEYOUT2	-	-	-	-	PLA6OUT	TIM6_9_PWMB	TIM6_9_PWMA	-	TIMA_5_PWM3	TIMA_6_PWM3	-	-	-	-	-	-	-	-	-	EVENTOUT	EVNTP302	FG2
-	18	PC3	ADC123_IN13	EIRQ3	-	GPO	-	SPI1_MOSI	EXMC_ADD3	-	KEYOUT1	-	-	-	-	PLA7OUT	TIM6_10_PWMB	TIM6_10_PWMA	-	TIMA_5_PWM4	TIMA_6_PWM4	-	-	-	-	-	EMB_PORT2	-	-	-	EVENTOUT	EVNTP303	FG2
8	19	AVSS	-	-	-		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	20	VREFL	-	-	-		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	21	VREFH	-	-	-		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
9	22	AVCC	-	-	-		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
10	23	PA0	ADC123_IN0+CMP1_INM1	EIRQ0+WKUP0_0	-	GPO	-	CMP1_OUT	EXMC_ADD10	SPI3_NSS1	KEYOUT4	-	USART1_CTS	USART2_CTS	PLAIN18	TIM6_TRIGD	TIM6_1_PWMA	TIM6_1_PWMB	TIM6_TRIGB	TIM6_TRIGA	TIMA_3_TRIG	TIMA_1_PWM1/CLKA	TIMA_1_TRIG	TIMA_3_PWM1/CLKA	TIM2_3_CLKB	TIM2_3_PWMB/TRIGB	-	EMB_PORT3	-	-	FCMREF	EVENTOUT	EVNTP100	FG1
11	24	PA1	ADC123_IN1+CMP1_INP1+CMP2_INP1+RTC_CLK1	EIRQ1	-	GPO	-	SPI2_NSS1	EXMC_ADD11	SPI3_NSS2	KEYOUT3	-	USART1_RTS	USART2_RTS	PLAIN19	-	TIM6_6_PWMB	TIM6_6_PWMA	TIM6_TRIGA	TIMA_4_PWM2/CLKB	TIMA_1_PWM2/CLKB	TIMA_6_TRIG	TIMA_3_PWM2/CLKB	TIM2_4_PWMB/TRIGB	TIM2_4_CLKB	TIM4_1_OUL	EMB_PORT4	-	-	-	EVENTOUT	EVNTP101	FG1
12	25	PA2	ADC123_IN2+CMP1_INM2+CMP2_INM1	EIRQ2	-	GPO	ADTRG1	CMP2_OUT	EXMC_ADD12	SPI3_NSS3	QSPI_IO2	KEYOUT7	-	-	-	PLA0OUT	-	-	TIMA_5_TRIG	TIMA_5_PWM1/CLKA	TIMA_1_PWM3	TIMA_4_PWM1/CLKA	TIMA_3_PWM3	TIM2_3_CLKA	TIM2_3_PWMA/TRIGA	TIM4_1_OUH	-	-	MDC	CAN2_TST_SAMPLE	EVENTOUT	EVNTP102	FG1
13	26	PA3	ADC123_IN3+CMP1_INP2+CMP2_INP2	EIRQ3	-	GPO	ADTRG2	SPI2_NSS2	EXMC_ADD13	SPI4_NSS1	QSPI_IO3	KEYOUT7	-	-	-	PLA4OUT	TIM6_1_PWMA	TIM6_1_PWMB	TIMA_4_PWM3	TIMA_5_PWM2/CLKB	TIMA_1_PWM4	TIMA_5_TRIG	TIMA_3_PWM4	TIM2_3_PWMB/TRIGB	TIM2_3_CLKB	TIM4_1_CLK	-	-	MDIO	-	EVENTOUT	EVNTP103	FG1
-	27	VSS	-	-	-		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	28	VCC	-	-	-		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
14	29	PA4	ADC12_IN4+DAC1_OUT1	EIRQ4	-	GPO	-	SPI3_NSS0	EXMC_ADD14	SPI2_NSS0	QSPI_NSS	SPI1_NSS0	USART1_CK	USART2_CK	-	PLA5OUT	-	-	-	-	TIMA_4_TRIG	TIMA_2_PWM2/CLKB		TIM2_1_PWMA/TRIGA	TIM2_1_CLKA	TIM4_1_OVL	-	-	-	CAN2_TST_CLOCK	EVENTOUT	EVNTP104	FG2
15	30	PA5	ADC12_IN5+DAC1_OUT2	EIRQ5	-	GPO	-	SPI2_NSS3	EXMC_ADD15	-	QSPI_SCK	SPI1_SCK	USART6_CTS	-	-	PLA6OUT	-	-	TIMA_5_PWM3	TIMA_1_PWM1/CLKA	TIMA_1_TRIG	TIMA_3_TRIG	TIMA_3_PWM1/CLKA	TIM2_1_PWMB/TRIGB	TIM2_1_CLKB	TIM4_1_PCT	-	-	-	CAN1_TST_SAMPLE	EVENTOUT	EVNTP105	FG2
16	31	PA6	ADC12_IN6	EIRQ6	-	GPO	CAN3_TST_SAMPLE	CMP1_OUT	EXMC_DATA24	-	QSPI_IO1	SPI1_MISO	USART6_RTS	-	-	PLA7OUT	-	-	TIMA_5_PWM4	-	-	TIMA_2_PWM1/CLKA	TIMA_5_PWM1/CLKA	TIM2_3_PWMA/TRIGA	TIM2_3_CLKA	TIM4_1_OVH	EMB_PORT2	EMB_PORT1	-	-	EVENTOUT	EVNTP106	FG2
17	32	PA7	ADC12_IN7 +PGA1	EIRQ7	-	GPO	ADTRG3	CMP2_OUT	EXMC_DATA25	-	QSPI_IO0	SPI1_MOSI	USART6_CK	-	-	PLA1OUT	TIM6_1_PWMA	TIM6_7_PWMA	TIM6_7_PWMB	TIM6_1_PWMB	TIMA_2_PWM2/CLKB	TIMA_6_PWM1/CLKA	TIMA_3_PWM4	TIM2_1_PWMA/TRIGA	TIM2_1_CLKA	TIM4_1_OWH	TIM2_4_PWMA/TRIGA	TIM2_4_CLKA	-	CAN1_TST_CLOCK	EVENTOUT	EVNTP107	FG2
-	33	PC4	ADC12_IN14+	EIRQ4	-	GPO	-	SPI4_MISO	EXMC_ADD4	-	KEYOUT0	-	-	-	-	PLA12OUT	-	-	TIM6_TRIGC	TIM6_TRIGA	-	-	-	-	-	-	-	-	-	EVENTOUT	EVNTP304	FG1

LQFP48	LQFP100	Pin Name	Analog	EIRQ/WKUP	TRACE/ JTAG	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16	Func17	Func18	Func19	Func20	Func21	Func22	Func23	Func24	Func25	Func26	Func32~63
-	-	-	-	-	-	GPO	I2C/ ADTRG	CMP/SPI/ KEY	EXMC/SPI	SPI/QSPI/ EXMC	QSPI/ KEY	SPI/KEY/ EMB	USART	USART	PLA	PLA/TIM6/ EMB	TIM6	TIM6/ EXMC	TIM6/ TIMA	TIM6/ TIMA	TIM6/ TIMA	TIM6/TIMA/ ADTRG	TIMA	TIMA/ TIM2	TIM2	TIM4/ CTC	TIM2/ EMB/CTC/ FCM	TIM2/ EMB/USB/ CMP	MDIO/ ADTRG	Other	EVENTOUT	EVENTPORT/ ADTRG	Communication Function Group
-	34	PC5	ADC12_IN15	EIRQ5	-	GPO	-	SPI4_MOSI	EXMC_ADD5	-	KEYOUT0	-	-	-	-	PLA13OUT	-	-	-	-	-	-	-	-	-	-	EMB_PORT3	-	-	-	EVENTOUT	EVNTP305	FG1
18	35	PB0	ADC12_IN8+PGA2	EIRQ0	-	GPO	ADTRG1	-	EXMC_DATA21	SPI3_NSS0	KEYOUT2	-	USART5_CTS	-	PLAIN8	PLA1OUT	TIM6_8_PWMA	TIM6_2_PWMA	TIM6_2_PWMB	TIM6_8_PWMB	TIMA_6_TRIG	TIMA_2_PWM3	TIMA_3_PWM1/CLKA	TIM2_3_PWMB/TRIGB	TIM2_3_CLKB	TIM4_1_ADSM	-	-	-	RTC_OUT	EVENTOUT	EVNTP200	FG1
19	36	PB1	ADC12_IN9	EIRQ1+WKUP0_1	-	GPO	ADTRG2	-	EXMC_DATA22	-	QSPI_SCK	-	USART5_RTS	-	PLAIN9	-	TIM6_3_PWMA	TIM6_9_PWMA	TIM6_9_PWMB	TIM6_3_PWMB	-	TIMA_2_PWM4	TIMA_3_PWM2/CLKB	TIM2_1_PWMA/TRIGA	TIM2_1_CLKA	TIM4_1_PCT	-	-	-	MCO_1	EVENTOUT	EVNTP201	FG1
20	37	PB2	ADC12_IN16	EIRQ2+WKUP0_2	-	GPO	ADTRG3	-	EXMC_DATA23	SPI4_NSS2	KEYOUT1	-	USART5_CK	-	PLAIN10	-	-	TIM6_TRIGB	TIM6_TRIGC	TIM6_TRIGD	TIMA_2_TRIG	-	TIMA_3_PWM3	TIM2_1_PWMB/TRIGB	TIM2_1_CLKB	TIM4_1_OWL	-	-	-	MCO_2	EVENTOUT	EVNTP202	FG1
-	38	PE7	-	EIRQ7	-	GPO	-	-	EXMC_DATA4	QSPI_IO2	QSPI_SCK	EMB_PORT3	-	-	-	-	TIM6_TRIGC	TIM6_TRIGA	TIM6_5_PWMA	TIM6_5_PWMB	TIMA_1_PWM3	TIMA_3_PWM3	-	-	-	-	-	-	-	-	EVENTOUT	-	FG2
-	39	PE8	-	EIRQ8	-	GPO	-	-	EXMC_DATA5	QSPI_IO3	-	EMB_PORT4	-	-	-	-	TIM6_7_PWMA	TIM6_7_PWMB	TIM6_4_PWMA	TIM6_4_PWMB	TIMA_1_PWM4	TIMA_3_PWM4	-	-	-	-	-	-	-	-	EVENTOUT	-	FG2
-	40	PE9	-	EIRQ9	-	GPO	-	-	EXMC_DATA6	-	-	-	-	-	-	-	TIM6_7_PWMB	TIM6_7_PWMA	-	-	-	-	-	-	-	-	-	-	-	-	-	-	FG2
-	41	PE10	-	EIRQ10	-	GPO	-	-	EXMC_DATA7	-	-	-	-	-	-	-	TIM6_8_PWMA	TIM6_8_PWMB	-	-	-	-	-	-	-	-	-	-	-	-	-	-	FG2
-	42	PE11	-	EIRQ11	-	GPO	-	-	EXMC_DATA8	-	-	-	-	-	-	-	TIM6_8_PWMB	TIM6_8_PWMA	-	-	-	-	-	-	-	-	-	-	-	-	-	-	FG2
-	43	PE12	-	EIRQ12	-	GPO	-	-	EXMC_DATA9	-	-	-	-	-	-	-	TIM6_9_PWMA	TIM6_9_PWMB	-	-	-	-	-	-	-	-	-	-	-	-	-	-	FG2
-	44	PE13	-	EIRQ13	-	GPO	-	-	EXMC_DATA10	-	-	-	-	-	-	-	TIM6_9_PWMB	TIM6_9_PWMA	-	-	-	-	-	-	-	-	-	-	-	-	-	-	FG2
-	45	PE14	-	EIRQ14	-	GPO	-	-	EXMC_DATA11	-	-	-	-	-	-	-	TIM6_10_PWMB	TIM6_10_PWMA	-	-	-	-	-	-	-	-	-	-	-	-	-	-	FG1
-	46	PE15	-	EIRQ15	-	GPO	-	-	EXMC_DATA12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EMB_PORT1	-	-	-	-	-	FG1
21	47	PB10	-	EIRQ10	-	GPO	-	-	EXMC_DATA30	QSPI_IO2	QSPI_SCK	-	-	-	-	EMB_PORT3	TIM6_5_PWMB	TIM6_5_PWMA	TIM6_TRIGC	-	TIMA_1_PWM3	TIMA_3_PWM3	-	-	-	-	-	-	-	-	EVENTOUT	EVNTP210	FG1
22	48	PB11	-	EIRQ11	-	GPO	-	-	EXMC_DATA31	QSPI_IO3	KEYOUT1	EMB_PORT4	-	-	-	-	TIM6_4_PWMA	TIM6_4_PWMB	-	-	TIMA_1_PWM4	TIMA_3_PWM4	-	-	-	-	-	-	-	-	EVENTOUT	EVNTP211	FG1
23	49	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
24	50	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
25	51	PB12	-	EIRQ12	-	GPO	-	-	EXMC_ALE	SPI2_NSS0	QSPI_NSS	SPI1_NSS0	-	USART3_CK	-	-	-	TIM6_3_PWMB	TIM6_TRIGB	TIM6_3_PWMA	-	-	-	-	-	-	EMB_PORT1	-	MDC	-	EVENTOUT	EVNTP212	FG2
26	52	PB13	-	EIRQ13	-	GPO	-	-	EXMC_CE1	-	QSPI_SCK	SPI1_SCK	-	USART3_CTS	-	-	TIM6_7_PWMA	TIM6_3_PWMA	TIM6_7_PWMB	TIM6_3_PWMB	-	-	-	-	-	-	-	-	MDIO	-	EVENTOUT	EVNTP213	FG2
27	53	PB14	-	EIRQ14	-	GPO	-	-	EXMC_CE2	-	QSPI_IO1	SPI1_MISO	-	USART3_RTS	-	-	TIM6_8_PWMA	TIM6_4_PWMB	TIM6_8_PWMB	TIM6_4_PWMA	TIMA_6_PWM1/CLKA	TIMA_6_TRIG	TIMA_4_PWM1/CLKA	-	-	TIM4_1_OUH	-	-	MDIO_A0	-	EVENTOUT	EVNTP214	FG2
28	54	PB15	ADC12_IN20+RTC_CLK2	EIRQ15	-	GPO	-	CMP1_OUT	EXMC_CE3	-	QSPI_IO0	SPI1_MOSI	-	USART4_CTS	-	-	TIM6_9_PWMA	TIM6_4_PWMA	TIM6_9_PWMB	TIM6_4_PWMB	TIMA_6_PWM2/CLKB	TIMA_4_PWM3	TIMA_4_PWM2/CLKB	TIMA_6_TRIG	-	TIM4_1_OUL	-	-	MDIO_A1	-	EVENTOUT	EVNTP215	FG2
-	55	PD8	-	EIRQ8	-	GPO	-	-	EXMC_DATA13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	TIM4_1_OVH	-	-	-	-	-	EVNTP408	FG1
-	56	PD9	-	EIRQ9	-	GPO	-	-	EXMC_DATA14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	TIM4_1_OVL	-	-	-	-	-	EVNTP409	FG1
-	57	PD10	-	EIRQ10	-	GPO	-	-	EXMC_DATA15	-	-	-	-	USART3_CK	-	-	-	-	-	-	-	-	-	-	-	TIM4_1_OWH	-	-	-	-	-	EVNTP410	FG1
-	58	PD11	-	EIRQ11	-	GPO	-	-	EXMC_ADD16	-	-	-	-	USART3_CTS	-	-	-	-	-	-	-	-	-	-	-	TIM4_1_OWL	-	-	-	-	-	EVNTP411	FG1
-	59	PD12	-	EIRQ12	-	GPO	-	-	EXMC_ADD17	-	-	-	-	USART3_RTS	-	-	-	-	-	-	-	TIMA_4_PWM1/CLKA	-	-	-	TIM4_1_PCT	-	-	-	-	-	EVNTP412	FG1
-	60	PD13	-	EIRQ13	-	GPO	-	-	EXMC_ADD18	-	-	-	-	-	-	-	-	-	-	-	-	TIMA_4_PWM2/CLKB	-	-	-	TIM4_1_ADSM	-	-	-	-	-	EVNTP413	FG1
-	61	PD14	-	EIRQ14	-	GPO	-	-	EXMC_DATA0	-	-	-	-	-	-	-	-	-	-	-	-	TIMA_4_PWM3	-	-	-	TIM4_1_CLK	-	-	-	-	-	EVNTP414	FG1
-	62	PD15	-	EIRQ15	-	GPO	-	-	EXMC_DATA1	-	-	-	-	USART4_CK	-	-	-	-	-	-	-	TIMA_4_PWM4	-	-	-	CTCREF	-	-	-	-	-	EVNTP415	FG1
-	63	PC6	-	EIRQ6	-	GPO	-	-	EXMC_ADD6	-	KEYOUT2	-	-	USART6_CTS	-	-	-	TIM6_1_PWMB	TIM6_TRIGD	TIM6_1_PWMA	-	TIMA_2_PWM1/CLKA	-	-	-	-	-	-	MDIO_A2	-	EVENTOUT	EVNTP306	FG2
-	64	PC7	-	EIRQ7	-	GPO	-	SPI2_NSS3	EXMC_ADD7	-	KEYOUT3	EMB_PORT5	-	USART6_RTS	-	-	-	TIM6_2_PWMB		TIM6_2_PWMA	-	TIMA_2_PWM2/CLKB	-	-	-	-	-	-	MDIO_A3	-	EVENTOUT	EVNTP307	FG2
-	65	PC8	-	EIRQ8	-	GPO	-	SPI2_NSS2	EXMC_ADD8	-	KEYOUT4	-	-	USART6_CK	PLAIN16	-	TIM6_5_PWMB	TIM6_3_PWMB	TIM6_5_PWMA	TIM6_3_PWMA	-	TIMA_2_PWM3	-	-	-	-	-	-	MDIO_A4	-	EVENTOUT	EVNTP308	FG2
-	66	PC9	-	EIRQ9	-	GPO	-	SPI2_NSS1	EXMC_ADD9	-	KEYOUT5	-	-	USART4_RTS	PLAIN17	-	TIM6_5_PWMA	TIM6_4_PWMB	TIM6_5_PWMB	TIM6_4_PWMA	-	TIMA_2_PWM4	-	-	-	-	-	-	-	-	EVENTOUT	EVNTP309	FG2
29	67	PA8	ADC3_IN4	EIRQ8+WKUP2_0	-	GPO	CAN3_TST_CLOCK	KEYOUT6	EXMC_DATA16	SPI4_NSS3	-	-	-	USART1_CK	PLAIN11	-	TIM6_1_PWMB	TIM6_7_PWMB	TIM6_1_PWMA	TIM6_7_PWMA	-	-	TIMA_2_PWM1/CLKA	TIM2_1_CLKB	TIM2_3_PWMB/TRIGB	CTCREF	-	USBFS_SOF	MDIO_A0	MCO_1	EVENTOUT	EVNTP108	FG1
30	68	PA9	ADC3_IN5	EIRQ9	-	GPO	-	KEYOUT5	EXMC_DATA17	-	-	-	USART4_CTS	-	PLAIN12	-	TIM6_1_PWMA	TIM6_8_PWMB	TIM6_1_PWMB	TIM6_8_PWMA	TIMA_1_PWM3	TIMA_3_PWM3	TIMA_2_PWM2/CLKB	TIM2_1_CLKA	TIM2_3_PWMA/TRIGA	TIM4_1_ADSM	EMB_PORT3	USBFS_VBUS	MDIO_A1	MCO_2	EVENTOUT	EVNTP109	FG1
31	69	PA10	ADC3_IN6	EIRQ10+WKUP2_2	-	GPO	-	-	EXMC_ADD26	-	-	-	USART4_RTS	-	PLAIN13	PLA2OUT	TIM6_2_PWMB	TIM6_9_PWMB	TIM6_2_PWMA	TIM6_9_PWMA	TIMA_1_PWM4	TIMA_3_PWM4	TIMA_2_PWM3	TIM2_3_CLKB	TIM2_1_PWMB/TRIGB	TIM4_1_CLK	EMB_PORT5	USBFS_ID	MDIO_A2	-	EVENTOUT	EVNTP110	FG1

LQFP48	LQFP100	Pin Name	Analog	EIRQ/WKUP	TRACE/ JTAG	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16	Func17	Func18	Func19	Func20	Func21	Func22	Func23	Func24	Func25	Func26	Func32~63
-	-	-	-	-	-	GPO	I2C/ ADTRG	CMP/SPI/ KEY	EXMC/SPI	SPI/QSPI/ EXMC	QSPI/ KEY	SPI/KEY/ EMB	USART	USART	PLA	PLA/TIM6/ EMB	TIM6	TIM6/ EXMC	TIM6/ TIMA	TIM6/ TIMA	TIM6/ TIMA	TIM6/TIMA/ ADTRG	TIMA	TIMA/ TIM2	TIM2	TIM4/ CTC	TIM2/ EMB/CTC/ FCM	TIM2/ EMB/USB/ CMP	MDIO/ ADTRG	Other	EVENTOUT	EVENTPORT/ ADTRG	Communication Function Group
32	70	PA11	ADC3_IN7+USBFS_DM	EIRQ11+WKUP2_3	-	GPO	-	CMP1_OUT	EXMC_ADD27	QSPI_IO2	-	-	-	USART1_CTS	PLAIN14	PLA3OUT	TIM6_7_PWMA	TIM6_10_PWMB	TIM6_7_PWMB	TIM6_10_PWMA	TIM6_2_PWMB	TIM6_2_PWMA	TIMA_2_PWM4	TIM2_3_CLKA	TIM2_1_PWMA/TRIGA	TIM4_1_OWL	EMB_PORT2	-	MDIO_A3	-	EVENTOUT	EVNTP111	FG1
33	71	PA12	ADC3_IN17+USBFS_DP	EIRQ12+WKUP3_0	-	GPO	-	CMP2_OUT	EXMC_ADD28	SPI1_NSS1	QSPI_IO3	EMB_PORT1	-	USART1_RTS	PLAIN15	-	TIM6_TRIGC	TIM6_8_PWMA	TIM6_TRIGA	TIM6_8_PWMB	TIMA_1_TRIG	TIMA_5_PWM1/CLKA	-	-	-	TIM4_1_OVH	-	-	MDIO_A4	FCMREF	EVENTOUT	EVNTP112	FG2
34	72	PA13	-	EIRQ13	JTMS_SWDIO	GPO	-	-	EXMC_ADD29	-	QSPI_IO1	-	USART4_CK	USART3_CTS	-	PLA8OUT	TIM6_6_PWMB	TIM6_6_PWMA	TIM6_TRIGD	-	-	TIMA_5_PWM2/CLKB	TIMA_6_PWM3	-	-	TIM4_1_OVL	-	-	ADTRG3	IFRP_OUT	EVENTOUT	EVNTP113	FG2
-	73	PF8	-	EIRQ8	-	GPO	-	-	EXMC_DATA26	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMA_5_PWM4	-	-	-	-	-	-	-	EVENTOUT	-	FG2
35	74	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
36	75	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
37	76	PA14	-	EIRQ14+WKUP3_2	JTCK_SWCLK	GPO	-	-	EXMC_DATA27	-	QSPI_IO0	-	-	-	-	-	TIM6_4_PWMB	TIM6_4_PWMA	TIM6_6_PWMA	TIM6_6_PWMB	-	-	TIMA_6_PWM4	-	-	TIM4_1_OUH	EMB_PORT1	-	ADTRG2	-	EVENTOUT	EVNTP114	FG2
38	77	PA15	ADC3_IN18	EIRQ15+WKUP3_3	JTDI	GPO	-	SPI3_NSS0	SPI1_NSS0	SPI2_NSS0	QSPI_NSS	EMB_PORT2	-	-	PLAIN0	PLA3OUT	TIM6_5_PWMB	TIM6_5_PWMA	TIM6_TRIGC	TIMA_1_PWM1/CLKA	TIMA_1_TRIG	TIMA_3_TRIG	TIMA_3_PWM1/CLKA	-	EXMC_RB7	TIM4_1_OUL	-	EMB_PORT1	-	-	EVENTOUT	EVNTP115	FG2
-	78	PC10	-	EIRQ10	-	GPO	-	-	EXMC_DATA18	SPI3_NSS3	-	-	-	-	-	PLA2OUT	TIM6_1_PWMA	TIM6_1_PWMB	TIM6_6_PWMB	TIM6_6_PWMA	-	-	-	-	-	-	-	-	MDC	-	EVENTOUT	EVNTP310	FG1
-	79	PC11	-	EIRQ11	-	GPO	-	-	EXMC_DATA19	SPI3_NSS2	KEYOUT6	-	-	-	-	PLA14OUT	-	-	-	-	-	-	-	-	-	-	-	-	MDIO	-	EVENTOUT	EVNTP311	FG1
-	80	PC12	-	EIRQ12	-	GPO	-	-	EXMC_DATA20	SPI3_NSS1	KEYOUT7	-	-	USART3_CK	-	PLA15OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT	EVNTP312	FG1
-	81	PD0	-	EIRQ0	-	GPO	-	-	EXMC_DATA2	-	-	-	-	USART5_CTS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVNTP400	FG1
-	82	PD1	-	EIRQ1	-	GPO	-	-	EXMC_DATA3	-	-	-	-	USART5_RTS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVNTP401	FG1
-	83	PD2	-	EIRQ2	-	GPO	-	-	EXMC_BAA	-	-	-	-	-	-	-	TIM6_3_PWMB	TIM6_3_PWMA	TIM6_TRIGD	-	-	-	TIMA_2_TRIG	-	-	-	EMB_PORT5	-	-	-	EVENTOUT	EVNTP402	FG1
-	84	PD3	-	EIRQ3	-	GPO	-	-	EXMC_CLK	-	-	-	USART5_CK	USART2_CTS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVNTP403	FG2
-	85	PD4	-	EIRQ4	-	GPO	-	-	EXMC_OE	-	-	-	-	USART2_RTS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVNTP404	FG2
-	86	PD5	-	EIRQ5	-	GPO	-	-	EXMC_WE	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVNTP405	FG2
-	87	PD6	-	EIRQ6	-	GPO	-	-	EXMC_RB0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVNTP406	FG2
-	88	PD7	-	EIRQ7	-	GPO	-	-	EXMC_CE0	-	-	-	-	USART2_CK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVNTP407	FG1
39	89	PB3	ADC3_IN19	EIRQ3+WKUP0_3	TDO_TRACESWO	GPO	-	-	-	-	QSPI_SCK	-	-	-	PLAIN1	PLA0OUT	TIM6_10_PWMA	TIM6_10_PWMB	TIM6_TRIGC	TIMA_1_PWM2/CLKB	TIMA_3_PWM2/CLKB	TIMA_2_TRIG	TIMA_4_PWM1/CLKA	TIM2_2_CLKB	TIM2_4_PWMB/TRIGB	TIM4_1_OWL	-	-	MDIO_A0	-	EVENTOUT	EVNTP203	FG1
40	90	PB4	ADC3_IN20	EIRQ4+WKUP1_0	NJTRST	GPO	-	-	EXMC_CE6	-	QSPI_IO1	-	-	-	PLAIN2	PLA1OUT	TIM6_2_PWMB	TIM6_2_PWMA	-	TIMA_5_PWM1/CLKA	-	TIMA_2_PWM1/CLKA	TIMA_4_PWM2/CLKB	TIM2_2_CLKA	TIM2_4_PWMA/TRIGA	TIM4_1_OVH	EMB_PORT5	-	MDIO_A1	MCO_2	EVENTOUT	EVNTP204	FG1
41	91	PB5	ADC3_IN21	EIRQ5+WKUP1_1	-	GPO	-	-	EXMC_CE7	-	QSPI_IO0	-	-	USART2_CK	PLAIN3	PLA2OUT	TIM6_4_PWMB	TIM6_4_PWMA	-	TIMA_6_PWM1/CLKA	-	TIMA_2_PWM2/CLKB	TIMA_4_PWM3	TIM2_4_CLKB	TIM2_2_PWMB/TRIGB	TIM4_1_OWH	EMB_PORT4	-	MDIO_A2	MCO_1	EVENTOUT	EVNTP205	FG1
42	92	PB6	-	EIRQ6+WKUP1_2	-	GPO	-	-	-	SPI1_NSS2	QSPI_IO2	-	-	-	PLAIN4	-	TIM6_TRIGA	EXMC_CE6	TIM6_TRIGC	TIMA_5_PWM2/CLKB	TIM6_TRIGD	TIMA_4_PWM1/CLKA	TIMA_4_PWM4	TIM2_4_CLKA	TIM2_2_PWMA/TRIGA	TIM4_1_OVL	CTCREF	CMP1_OUT	MDIO_A3	ADTRG1	EVENTOUT	EVNTP206	FG2
43	93	PB7	-	EIRQ7+WKUP1_3	-	GPO	-	-	-	EXMC_ADV	QSPI_IO3	-	-	-	PLAIN5	-	TIM6_6_PWMB	TIM6_6_PWMA	TIM6_TRIGD	TIMA_6_PWM2/CLKB	-	TIMA_4_PWM2/CLKB	TIMA_2_PWM4	TIM2_1_PWMB/TRIGB	TIM2_1_CLKB	TIM4_1_OWL	FCMREF	CMP2_OUT	MDIO_A4	ADTRG2	EVENTOUT	EVNTP207	FG2
44	94	PF3/MD	-	-	-	GPO	-	-	EXMC_CE7	SPI2_NSS0	QSPI_NSS	-	-	-	PLAIN7	-	-	-	-	-	-	TIMA_2_TRIG	TIMA_6_PWM1/CLKA	TIM2_2_PWMB/TRIGB	TIM2_2_CLKB	TIM4_1_OWH	-	-	-	IFRP_OUT	EVENTOUT	ADTRG3	FG2
45	95	PB8	PVD2EXINP	EIRQ8	-	GPO	-	-	EXMC_DATA28	SPI1_NSS3	KEYOUT0	-	-	-	PLAIN6	PLA3OUT	TIM6_5_PWMB	TIM6_5_PWMA	TIM6_TRIGB	-	TIMA_5_PWM1/CLKA	ADTRG1	TIMA_4_PWM3	TIM2_1_PWMA/TRIGA	TIM2_1_CLKA	TIM4_1_OVH	EMB_PORT1	USBFS_DRVVBUS	MDC	FCMREF	EVENTOUT	EVNTP208	FG2
46	96	PB9	-	EIRQ9+WKUP2_1	-	GPO	-	CMP2_OUT	EXMC_DATA29	SPI2_NSS0	QSPI_NSS	-	-	-	PLAIN7	-	TIM6_1_PWMA	TIM6_1_PWMB	-	TIMA_6_PWM1/CLKA	-	TIMA_4_TRIG	TIMA_4_PWM4	TIM2_2_PWMA/TRIGA	TIM2_2_CLKA	TIM4_1_OWH	-	-	MDIO	IFRP_OUT	EVENTOUT	EVNTP209	FG2
-	97	PE0	-	EIRQ0	-	GPO	-	-	EXMC_CE4	-	-	-	-	-	-	-	-	-	-	-	-	TIMA_4_TRIG	-	-	-	-	-	-	-	-	-	-	FG2
-	98	PE1	-	EIRQ1	-	GPO	-	-	EXMC_CE5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	FG2
47	99	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
48	100	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Note:

– *In the above table, Func32~63 are mainly serial communication functions (including USART, SPI, I2C, CAN), which are divided into two groups FunctionGroup, referred to as FG1 and FG2 .* Please refer to Table 22 *Table 2-2* for details.

Table 2-2 Func32~63 table

	Func32	Func33	Func34	Func35	Func36	Func37	Func38	Func39	Func40	Func41	Func42	Func43	Func44	Func45	Func46	Func47
FG1	USART1_TX	USART1_RX	USART2_TX	USART2_RX	USART3_TX	USART3_RX	USART4_TX	USART4_RX	USART5_TX	USART5_RX	USART6_TX	USART6_RX	SPI1_SCK	SPI1_MOSI	SPI1_MISO	SPI2_SCK
FG2	USART1_TX	USART1_RX	USART2_TX	USART2_RX	USART3_TX	USART3_RX	USART4_TX	USART4_RX	USART5_TX	USART5_RX	USART6_TX	USART6_RX	SPI2_SCK	SPI2_MOSI	SPI2_MISO	SPI3_SCK

	Func48	Func49	Func50	Func51	Func52	Func53	Func54	Func55	Func56	Func57	Func58	Func59	Func60	Func61	Func62	Func63
FG1	SPI2_MOSI	SPI2_MISO	SPI3_SCK	SPI3_MOSI	SPI3_MISO	SPI1_NSS0	I2C1_SDA	I2C1_SCL	I2C2_SDA	I2C2_SCL	I2C3_SDA	I2C3_SCL	CAN1_TX	CAN1_RX	CAN2_TX	CAN2_RX
FG2	SPI3_MOSI	SPI3_MISO	SPI4_SCK	SPI4_MOSI	SPI4_MISO	SPI4_NSS0	I2C1_SDA	I2C1_SCL	I2C2_SDA	I2C2_SCL	I2C3_SDA	I2C3_SCL	CAN2_TX	CAN2_RX	CAN3_TX	CAN3_RX

Table 2-3 Port Configuration

Package	Port Group	Bits																Pin Count	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Total	
LQFP100	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	85
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortE	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortF	-	-	-	-	-	-	-	o	-	-	-	-	o	o	o	o	5	
LQFP48	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	39
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	-	-	-	-	-	-	-	-	-	-	-	-	-	3	
	PortF	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	o	4	

Table 2-4 Universal Functional Specifications

Port		Pull-up / Pull-down	Open-Drain Output	Driving Capacity	5V Withstand Voltage
Port A	PA0~PA3 PA8~PA10 PA13~PA15	Support Support Support	Support Support Support	Low Medium High Low Medium High Low Medium High	Support Support Support
	PA4~PA7, PA11, PA12	Support	Support	Low Medium High	not support
Port B	PB0~PB11	Support	Support	Low Medium High	Support
	PB12~PB15	Support	Support	Low Medium High	not support
Port C	PC0~PC3 PC10~PC15	Support Support	Support Support	Low Medium High Low Medium High	Support Support
	PC4~PC9	Support	Support	Low Medium High	not support
Port D	PD0~PD7	Support	Support	Low Medium High	Support
	PD8~PD15	Support	Support	Low Medium High	not support
Port E	PE0~PE6 PE9~PE15	Support Support	Support Support	Low Medium High Low Medium High	Support Support
	PE7~PE8	Support	Support	Low Medium High	not support
Port F	PF0~PF8	Support	Support	Low Medium High	Support

Note:

– *Input voltage must not be higher than VREFH/AVCC when used as an analog function.*

2.3 Pin function description

Table 2-5 Pin Function Description

Categories	Functional name	I/O	Description
Power	VCC	I	Power supply
	VSS	I	Power ground
	AVCC	I	Analog power
	VREFH	I/O	Analog reference voltage
	AVSS	I	Analog power ground
	VREFL	I	Analog reference voltage
System	NRST	I	Reset terminal, low effective
	MD	I	Mode terminal
PVD	PVD2EXINP	I	PVD2 external input comparison voltage
Clock	XTAL_IN/ XTAL_EXT	I	External master clock oscillator interface
	XTAL_OUT	O	
	XTAL32_IN	I	External sub-clock (32.768K) oscillator interface
	XTAL32_OUT	O	
	MCO_x (x=1~2)	O	Internal clock output
GPIO	GPIOxy (x=A~F y=0~15)	IO	Universal input/output
EVENTOUT	EVENTOUT	O	Cortex-M4 CPU event output
EIRQ	EIRQx (x=0~15)	I	Maskable external interrupts
	WKUPx_y (x=0~3 y=0~3)	I	PowerDown mode external wake-up input
Event Port	EVNTPxy (x=1~4 y=0~15)	IO	Event port input and output functions
Key	KEYOUTx (x=0~7)	O	KEYSCAN scan output signal
JTAG/ SWD	JTCK_SWCLK	I	Online debugging interface
	JTMS_SWDIO	IO	
	JTDO_TRACESWO	O	
	JTDI	I	
	NJTRST	I	
TRACE	TRACECLK	O	Trace debug synchronous clock output
	TRACEDx (x=0~3)	O	Trace debug data output
FCM	FCMREF	I	External pin input reference clock for clock frequency measurement function
RTC	RTC_OUT	O	1Hz clock output
	RTC_CLK x (x=1~2)	I	External clock input
Timer2 (x=1~4)	TIM2_x_CLKA	I	Counting clock port input
	TIM2_x_CLKB	I	Counting clock port input
	TIM2_x_PWMA/ TRIGA	IO	External event trigger input or PWM port output
	TIM2_x_PWMB/ TRIGB	IO	External event trigger input or PWM port output
Timer4	TIM4_x_CLK	I	Counting clock port input

Categories	Functional name	I/O	Description
(x=1)	TIM4_x_OUH	IO	PWM port U-phase output
	TIM4_x_OUL	IO	PWM port U-phase output
	TIM4_x_OVH	IO	PWM port V-phase output
	TIM4_x_OVL	IO	PWM port V-phase output
	TIM4_x_OWH	IO	PWM port W-phase output
	TIM4_x_OWL	IO	PWM port W-phase output
	TIM4_x_ADSM	O	Dedicated event output monitoring
	TIM4_x_PCT	O	PWM cycle output monitoring
Timer6 (x=1~10)	TIM6_TRIGA	I	External event trigger A input
	TIM6_TRIGB	I	External event trigger B input
	TIM6_TRIGC	I	External event trigger C input
	TIM6_TRIGD	I	External event trigger D input
	TIM6_x_PWMA	IO	External event trigger input or PWM port output
	TIM6_x_PWMB	IO	External event trigger input or PWM port output
TimerA (x=1~6)	TIMA_x_TRIG	I	External event trigger input
	TIMA_x_PWM1/ CLKA	IO	External event trigger input or PWM port output or count clock port input
	TIMA_x_PWM2/ CLKB	IO	External event trigger input or PWM port output or count clock port input
	TIMA_x_PWMy (y=3~4)	IO	External event trigger input or PWM port output
EMB	EMB_PORTx (x=1~5)	I	Port input control signal
USARTx (x=1~6)	USARTx_TX	IO	Send data
	USARTx_RX	IO	Receiving data
	USARTx_CK	IO	Communication clock
	USARTx_RTS	O	Request ttransmiting signal
	USARTx_CTS	I	Clear transmit signal
SPIx (x=1~4)	SPIx_MISO	IO	Primary input/slave output data transmission pin
	SPIx_MOSI	IO	Primary output/slave input data transmission pin
	SPIx_SCK	IO	Transmission clock
	SPIx_NSS0	IO	Select input/output pin from machine
	SPIx_NSSy (y=1~3)	O	Slave selection output pin
QSPI	QSPI_IOx (x=0~3)	IO	Data line
	QSPI_SCK	O	Clock output
	QSPI_NSS	O	Slave selection
I2Cx (x=1~3)	I2Cx_SCL	IO	Clock line
	I2Cx_SDA	IO	Data line
CANx (x=1~3)	CANx_TX	O	Send data
	CANx_RX	I	Receiving data
	CANx_TST_SAMPLE	O	For observation only, sampling position (communication clock width of one cycle after the sampling point)

Categories	Functional name	I/O	Description
	CANx_TST_CLOCK	O	For observation only, baud rate (the width of the communication clock before a bit starts in one cycle)
USB_FS	USBFS_DM	IO	USBFS on-chip full-speed PHY D- signal
	USBFS_DP	IO	USBFS on-chip full-speed PHY D+ signal
	USBFS_VBUS	I	USBFS VBUS signal
	USBFS_ID	I	USBFS ID signal
	USBFS_SOF	O	USBFS SOF pulse output signal
	USBFS_DRVVBUS	O	USBFS VBUS driver permission signal
CMP	CMP1_OUT	O	CMP1 result output
	CMP2_OUT	O	CMP2 result output
	CMPx_INPy (x=1~2 y=1~4)	I	CMPx positive analog input
	CMPx_INMy (x=1~2 y=1~4)	I	CMPx negative analog input
ADC	ADTRG1	I	ADC1 AD conversion external start source
	ADTRG2	I	ADC2 AD conversion external start source
	ADTRG3	I	ADC3 AD conversion external start source
	ADC123_INx (x=0~3, 10~13)	I	ADC1, 2, 3 share external analog input port
	ADC12_INx (x=4~9, 14~16, 20)	I	ADC1, 2 share external analog input port
	ADC3_INx (x=4~7, 17~21)	I	ADC3 external analog input port
DAC	DACx_OUTy (x=1 y=1, 2)	O	DAC analog output
EXMC	EXMC_CLK	IO	EXMC section of the reference manual for details.
	EXMC_OE	O	
	EXMC_WE	O	
	EXMC_ALE	O	
	EXMC_BAA	O	
	EXMC_ADV	O	
	EXMC_CEx (x=0~7)	O	
	EXMC_RBx(x=0~7)	I	
	EXMC_ADDx (x=0~29)	O	
	EXMC_DATAx (x=0~31)	IO	

2.4 Pin Instruction

Table 2-6 Pin Use Instructions

Pin Name	Usage Notes
VCC	Power supply, connect 1.8V~3.6V voltage, and connect a decoupling capacitor to the VSS pin nearby (refer to [Electrical Characteristics (ECs)])
VSS	Source ground, connected to 0V
AVCC	Analog power supply, power the analog module, connect to the same voltage as VCC (refer to [Electrical Characteristics (ECs)]) When not using the analog module, please short it with VCC
AVSS	Analog power ground, powering the analog module, connected to the same voltage as VSS (refer to [Electrical Characteristics (ECs)]) When not using the analog module, please short it with VSS
VREFL	Analog reference voltage, connected to the same voltage as AVSS (reference [Electrical Characteristics (ECs)]) When not using the analog module, please short it with AVSS
VREFH	Analog reference voltage, Connect a voltage no higher than AVCC. When the analog module is not used, short it with AVCC.
PF3/ MD	Mode input. When the reset pin (NRST) is released (from low to low, the pin must be fixed at low level. It is recommended to connect a resistor (4.7 KΩ) to VSS (pull-down)
NRST	Reset pin, low effective. Resistance to VCC when not in use (pull-up)
Pxy (x=A~F y=0~15)	Universal pin. When used as input function, the input voltage of the pin that supports 5V voltage tolerance should not exceed 5V. When the input voltage exceeds VCC, the internal pull-up/pull-down is prohibited. The input voltage of the pin that does not support 5V voltage tolerance should not exceed VCC. When used as an analog input, the analog voltage should not exceed VREFH/AVCC Hang out when not in use or connect to VCC (Pull-up)/VSS (Pull-down)

3 Electrical Characteristics (ECs)

3.1 Parameter Conditions

All voltages are V_{SS}-based unless otherwise specified.

3.1.1 Minimum and Maximum

Unless otherwise stated, the minimum and maximum values of all devices are obtained through comprehensive evaluation through sample testing under the worst-case ambient temperature, supply voltage and clock frequency conditions.

3.1.2 Typical Value

Unless otherwise stated, typical data are obtained through comprehensive evaluation of sample tests at T_A = 25 °C, V_{CC} = 3.3 V.

3.1.3 Typical Curve

Unless otherwise specified, all typical curves are not tested for design reference only.

3.1.4 Load Capacitance

Figure 3-1 (Left) shows the load conditions used to measure the pin parameters.

3.1.5 Pin Input Voltage

Figure 3-1 (Right) shows how to measure the input voltage at the device pins.

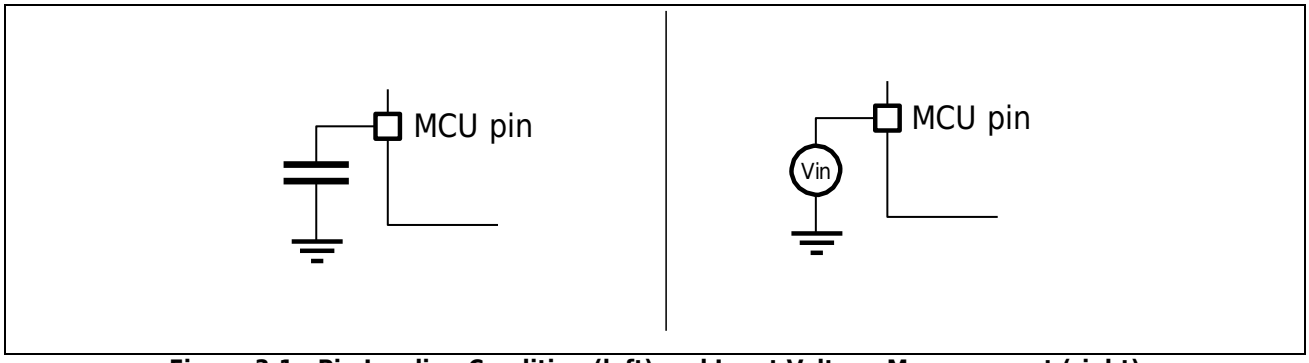


Figure 3-1 Pin Loading Condition (left) and Input Voltage Measurement (right)

3.1.6 Power Supply Scheme

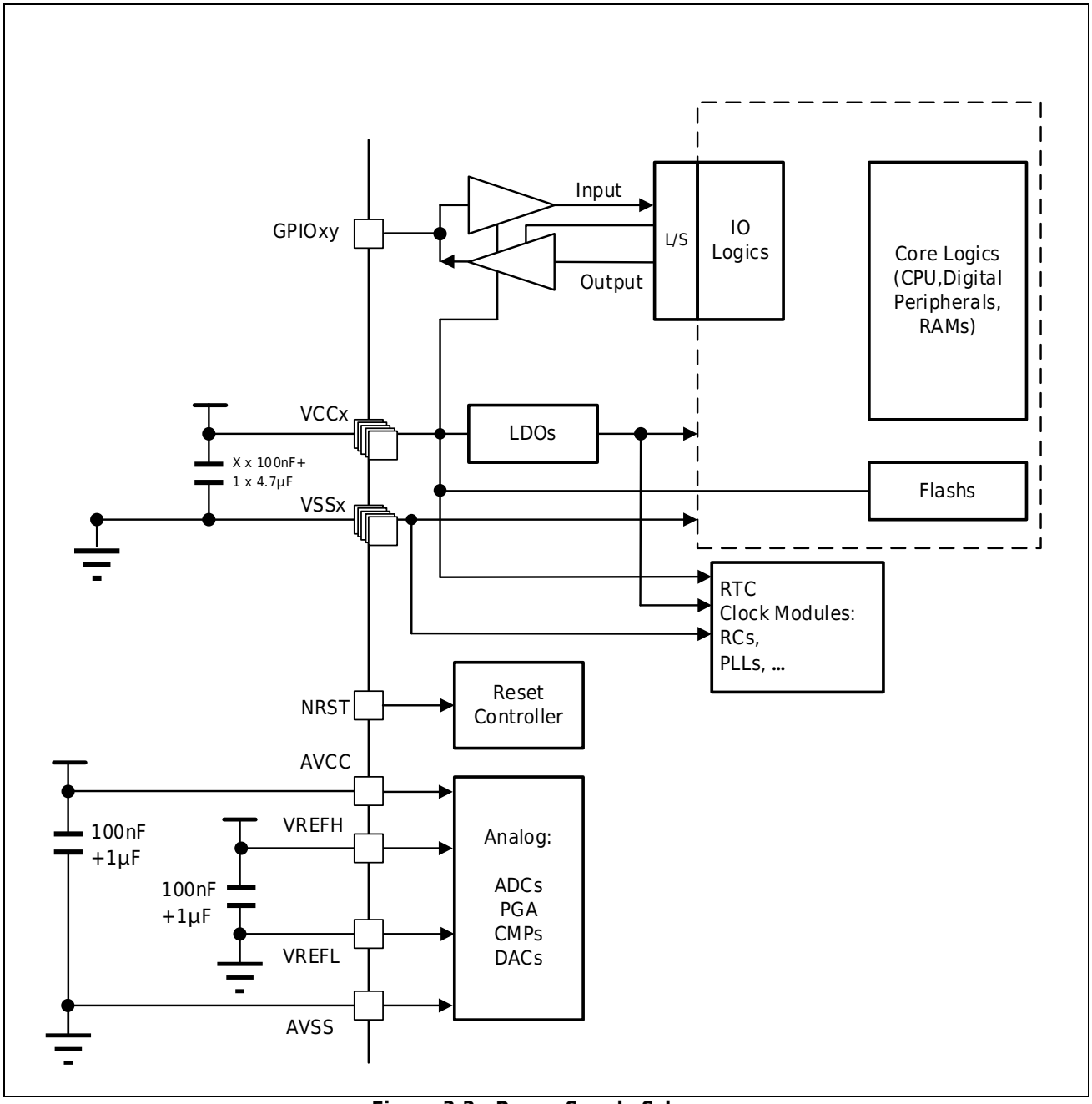


Figure 3-2 Power Supply Scheme

1. A 4.7 µF ceramic capacitor must be connected to one of the VCC pins.
2. AVSS=VSS=VREFL.
3. Each power supply pair (e.g. VREFH/ VREFL, VCC/ VSS, AVCC/ AVSS.....) must be decoupled using the filtering ceramic capacitors mentioned above. These capacitors must be placed as close as possible to or below the appropriate pins on the underside of the PCB to ensure proper device operation. Filtering capacitors are not recommended to reduce PCB size or cost. This may result in abnormal operation of the device.

3.1.7 Current Consumption Measurement

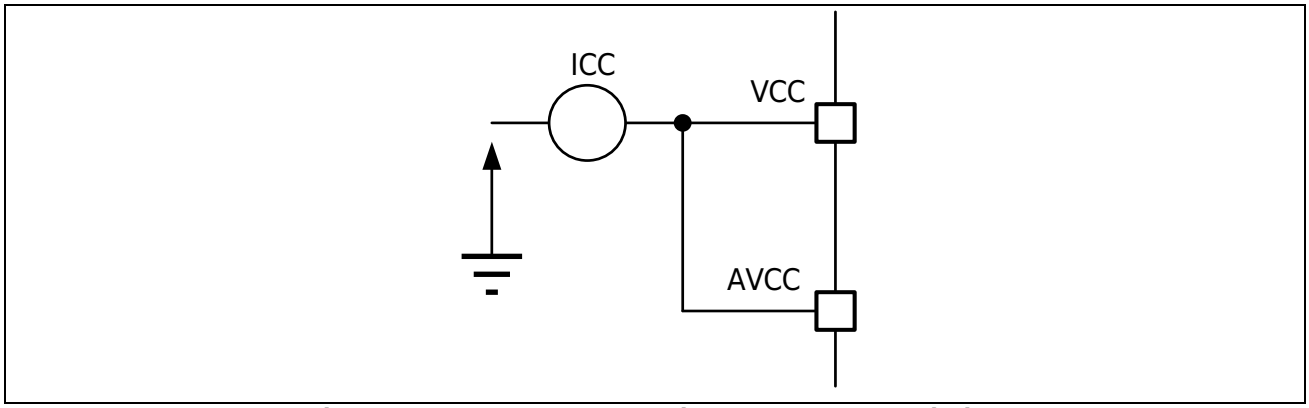


Figure 3-3 Current Consumption Measurement Solution

3.2 Absolute Maximum Rating

Permanent damage to the device may result if loads exceeding the absolute maximum ratings listed in Table 3-1, Table 3-2 and Table 3-3 are applied to the device. These values are just rated stresses and do not mean that the device works properly under these conditions. Long-term operation may affect the reliability.

Table 3-1 Voltage Characteristics

Symbol	Item	Min.	Max.	Unit
V_{CC}-V_{SS}	External main supply voltage (including AVCC, VCC)(1)	-0.3	4.0	V
V_{IN}	Except PA4~PA5(DAC), PA6~PA7, PC4~PC5, PE7~8 PB12~15, PC6~9, PD8~15 PA11/ USBFS_DM, PA12/ USBFS_DP Input voltage on pins other than(2)	V_{SS}–0.3	V_{CC}+4.0(Maximum 5.8 V)	
	PA4~PA5(DAC), PA6~PA7, PC4~PC5, PE7~8 PB12~15, PC6~9, PD8~15 PA11/ USBFS_DM, PA12/ USBFS_DP Input voltage on pin	V_{SS}–0.3	Vcc+0.7(Maximum 4.0 V)	
|VSSx-VSS|	Voltage difference between different ground pins (including VREFL)	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage	Please refer to [Electrical Sensitivity]		-

1. All main power (VCC, AVCC) and ground (VSS, AVSS) pins must always be connected to an external power supply, within the limits allowed.
2. The maximum value of VIN must always be followed.

Table 3-2 Voltage Characteristics

Symbol	Item	Max.	Unit
$\sum I_{VCC}$	Total current flowing into all VCC_X supply lines (source current)(1)	240	mA
$\sum I_{VSS}$	Total current flowing out of all VSS_X ground wires (sinking current) (1)	-240	
I_{VCC}	Maximum current flowing into each VCC_X power line (source current) (1)	100	
I_{VSS}	Maximum current out of each VCC_X ground wire (sinking current) (1)	-100	
I_{IO}	Output current sinking on any I/O and control pin	20	
	Output current sourced by any I/O and control pin	-20	
$\sum I_{IO}$	Total output sink current on all I/O and control pins (2)	120	
	Total output source current on all I/O and control pins(2)	-120	

1. All main power (VCC, AVCC) and ground (VSS, AVSS) pins must always be connected to an external power supply, within the limits allowed.
2. This total output current must be correctly distributed in all power domains; this total output current is applicable to packages of 64 PINs and above. For 48 PINs package, the maximum total output current is ±80 mA, and for 32 PINs package, the maximum total output current is ±40 mA.

Table 3-3 Thermal Characteristics

Symbol	Item	Numerical Value	Unit
T_{STG}	Storage temperature range	–65~150	°C
T_J	Junction temperature range	-40~125	°C

3.3 Operating Conditions

3.3.1 General Working Conditions

Table 3-4 Universal Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HCLK}	Internal AHB clock frequency(1)	-	-	-	120	MHz
V_{CC}	Standard operating voltage	-	1.8	-	3.6	V
V_{AVCC}	Analog operating voltage(2)	-	1.8	-	3.6	V
V_{IN}	Input voltage on 5V tolerant pin(3) (4) (5)	2 V ≤ VCC ≤ 3.6 V 2 V ≤ AVCC ≤ 3.6 V	–0.3	-	5.5	
		VCC < 2 V AVCC < 2 V	–0.3	-	5.2	
	PA4~PA5(DAC), PA6~PA7, PC4~PC5, PE7~8 PB12~15, PC6~9, PD8~15 PA11/ USBFS_DM、 PA12/ USBFS_DP Input voltage on pin(5)	-	–0.3	-	V_{CC}+0.3	
T_A	Ambient temperature range	-	-40	-	105	℃
T_J	Junction temperature range	-	-40	-	125	℃

1. Guarantee of mass production test.
2. VREFH pin exists, the following condition must be considered: 0 ≤ AVCC-VREFH ≤ 1.2 V.
3. To keep the voltage above VCC + +0.3V, the internal pull-up/pull-down resistors must be disabled.
4. It is necessary to ensure that the power supply (VCC, AVCC) of the device is stable before adding this voltage to the 5V withstand voltage pin of the device.
5. It is prohibited for such pins to be directly connected to power sources or ground other than those of this chip. It is recommended to pull it up to the power supply or down to the ground through a resistor of 1KΩ or above.

3.3.2 Operating Conditions During Power Up/Down

TA is subject to normal working conditions.

Table 3-5 Operating Conditions in Case of Power-on/Power-off

Symbol	Parameter	Min.	Max.	Unit
t_{VCC}	VCC Rise Time Rate	20	20000	μs/V
	VCC Fall Time Rate	20	20000	

3.3.3 Reset and Power Control Block Features

Table 3-6 Reset and Power Control Block Features

Symbol	Parameter	Conditions	Min.	Typical Value	Max.	Unit
V_{BOR}	BOR Monitoring Voltage	ICG1.BOR_LEV[1:0]=0b00(1)	1.78	1.99	2.19	V
		ICG1.BOR_LEV [1:0]=0b01	1.89	2.09	2.30	V
		ICG1.BOR_LEV [1:0]=0b10	1.99	2.20	2.40	V
		ICG1.BOR_LEV [1:0]=0b11(1)	2.20	2.40	2.60	V
V_{PVD1}	PVD1 Monitoring Voltage(3)	PVD1LVL[2:0]=0b000(1)	1.80	2.00	2.20	V
		PVD1LVL[2:0]=0b001	1.90	2.10	2.30	V
		PVD1LVL[2:0]=0b010	2.10	2.30	2.50	V
		PVD1LVL[2:0]=0b011	2.33	2.55	2.77	V
		PVD1LVL[2:0]=0b100	2.43	2.65	2.87	V
		PVD1LVL[2:0]=0b101	2.53	2.75	2.97	V
		PVD1LVL[2:0]=0b110	2.63	2.85	3.07	V
		PVD1LVL[2:0]=0b111(1)	2.73	2.95	3.17	V
V_{PVD2}	PVD2 Monitoring Voltage(3)	PVD2LVL[2:0]=0b000(1)	1.90	2.10	2.30	V
		PVD2LVL[2:0]=0b001	2.10	2.30	2.50	V
		PVD2LVL[2:0]=0b010	2.33	2.55	2.77	V
		PVD2LVL[2:0]=0b011	2.43	2.65	2.87	V
		PVD2LVL[2:0]=0b100	2.53	2.75	2.97	V
		PVD2LVL[2:0]=0b101	2.63	2.85	3.07	V
		PVD2LVL[2:0]=0b110 (1)	2.73	2.95	3.17	V
		PVD2LVL[2:0]=0b111(1) (5)	0.90	1.10	1.30	V
V_{pvd}hyst	Hysteresis of PVD1, 2 (4)	-	-	100	-	mV
V_{POR}	Power-on/power-off reset threshold(1)	Rising edge VPOR	1.56	1.68	1.80	V
		Falling edge VPDR	1.52	1.64	1.76	V
V_{POR}hyst	POR Hysteresis	-	-	40	-	mV
I_{RUSH}	Surge current when the voltage regulator is powered on (POR or awakens from standby)	-	-	100	150	mA
T_{NRST}	NRST reset minimum width	-	10	-	-	μs

Symbol	Parameter	Conditions	Min.	Typical Value	Max.	Unit
T_{IPVD1}	PVD1 reset release time(2)	-	300	380	460	μs
T_{IPVD2}	PVD2 reset release time(2)	-	300	380	460	μs
T_{INRST}	NRST reset release time(2)	-	25	35	50	μs
T_{RIPT}	NRST reset release time(2)	-	140	160	200	μs
T_{RSTBOR}	BOR reset release time(2)	-	440	520	610	μs
T_{RSTPOR}	Power-on reset release time(2)	-	-	2500	3000	μs

1. Guarantee of mass production test.
2. Design guaranteed.
3. The PVD1 monitoring voltage is the monitoring voltage when the VCC voltage drops; when PVD2LVL[2:0] is set to 0b111, the PVD2 monitoring voltage is the monitoring voltage when the PVDEXINP voltage drops; when PVD2LVD[2:0] is set to a value other than 0b111, the PVD2 monitoring voltage is the monitoring voltage when the VCC voltage drops.
4. The hysteresis of PVD1,2 is the difference between the monitored voltage when VCC is rising and the monitored voltage when VCC is falling.
   PVD1 monitoring voltage when VCC rises = Vpvd1+Vpvdhyst;
   PVD2 monitoring voltage when VCC rises = Vpvd2+Vpvdhyst.
5. PVD2LVDL[2:0] = 0b111, the comparison voltage is the external input comparison voltage of the PVD2EXINP pin.

3.3.4 Supply Current Features

The current consumption is affected by several parameters and factors, including operating voltage, ambient temperature, I/O pin load, device software configuration, operating frequency, I/O pin switch rate, program position in memory and running code.

The method for measuring the current consumption is described in Figure 3-3. The current consumption measurements in the various modes described in this section are obtained under laboratory conditions using a set of test codes running in FLASH.

The specific conditions are as follows:

1. All I/O pins are in high-impedance mode (no load).
2. Clock frequency selection f_{HCLK}=120MHz/ 60MHz/ 24MHz/ 8MHz/ 1MHz。
3. The power consumption modes are divided into: normal working mode ICC_RUN, sleep mode ICC_SLEEP, stop mode ICC_STP, power-down mode ICC_PD, and Dhrystone working mode ICC_DHRYSTONE.
4. Please refer to the specific current condition description for peripheral clock ON/OFF.
5. When f_{HCLK}=120 MHz/ 60 MHz, PLL is enabled.

Table 3-7 Run Mode Current Consumption 1

Mode	Parameter	Symbol	Conditions	T_A(°C)	Product Specifications			Unit
					Min	Typ(3)	Max(2)	
Operating Mode	f_{HCLK}= 120 MHz	ICC_RUN	while(1), all modules clock OFF(1)	-40	-	15.5	-	mA
			while(1), all modules clock ON(1)	-40	-	32	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	16	-	mA
			CACHE ON	-40	-	16	-	mA
		ICC_SLEEP	All module clocks OFF(1)	-40	-	10.5	-	mA
			All module clocks ON(1)	-40	-	27	-	mA
		ICC_RUN	while(1), all modules clock OFF(1)	25	-	16	-	mA
			while(1), all modules clock ON(1)	25	-	32	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	17	-	mA
			CACHE ON	25	-	17	-	mA
		ICC_SLEEP	All module clocks OFF(1)	25	-	11	-	mA
			All module clocks ON(1)	25	-	27	-	mA
		ICC_RUN	while(1), all module clocks are OFF	85	-	17	29	mA
			while(1), all module clocks are ON	85	-	34	49	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	30	mA
			CACHE ON	85	-	-	30	mA
		ICC_SLEEP	Full module clock OFF	85	-	12	23	mA

Mode	Parameter	Symbol	Conditions	T_A(°C)	Product Specifications			Unit
					Min	Typ(3)	Max(2)	
			Full module clock ON	85	-	29	43	mA
		ICC_RUN	while(1), all modules clock OFF(1)	105	-	19	36	mA
			while(1), all modules clock ON(1)	105	-	35	56	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	38	mA
			CACHE ON	105	-	-	38	mA
		ICC_SLEEP	All module clocks OFF(1)	105	-	14	30	mA
			All module clocks ON(1)	105	-	30	51	mA

1. Guarantee of mass production test.
2. Max voltage condition, VCC=1.8~3.6 V.
3. Typ voltage condition, VCC=3.3 V.

Table 3-8 Run Mode Current Consumption 2

Mode	Parameter	Symbol	Conditions	T_A(°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
Operating Mode	f_{HCLK}= 60 MHz	ICC_RUN	while(1), all module clocks are OFF	-40	-	9	-	mA
			while(1), all module clocks are ON	-40	-	18.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	8.7	-	mA
			CACHE ON	-40	-	8.7	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	6.5	-	mA
			Full module clock ON	-40	-	16	-	mA
		ICC_RUN	while(1), all module clocks are OFF	25	-	9.5	-	mA
			while(1), all module clocks are ON	25	-	19	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	9	-	mA
			CACHE ON	25	-	9	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	7	-	mA
			Full module clock ON	25	-	16.5	-	mA
		ICC_RUN	while(1), all module clocks are OFF	85	-	11	22	mA
			while(1), all module clocks are ON	85	-	20	33	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	22	mA
			CACHE ON	85	-	-	22	mA
		ICC_SLEEP	Full module clock OFF	85	-	8	19	mA
			Full module clock ON	85	-	18	31	mA
		ICC_RUN	while(1), all module clocks are OFF	105	-	12	29	mA
			while(1), all module clocks are ON	105	-	22	41	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	29	mA
			CACHE ON	105	-	-	29	mA
		ICC_SLEEP	Full module clock OFF	105	-	10	26	mA
			Full module clock ON	105	-	19	38	mA

1. Typ voltage condition VCC=3.3 V.
2. Max voltage condition VCC=1.8~3.6 V.

Table 3-9 Run Mode Current Consumption 3

Mode	Parameter	Symbol	Conditions	T_A(°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
Operating Mode	f_{HCLK}= 24 MHz	ICC_RUN	while(1), all module clocks are OFF	-40	-	5	-	mA
			while(1), all module clocks are ON	-40	-	10.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	10.5	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	4	-	mA
			Full module clock ON	-40	-	9.5	-	mA
		ICC_RUN	while(1), all module clocks are OFF	25	-	5	-	mA
			while(1), all module clocks are ON	25	-	10.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	10.5	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	4	-	mA
			Full module clock ON	25	-	9.5	-	mA
		ICC_RUN	while(1), all module clocks are OFF	85	-	-	17	mA
			while(1), all module clocks are ON	85	-	-	24	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	18	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	16	mA
			Full module clock ON	85	-	-	22	mA
		ICC_RUN	while(1), all module clocks are OFF	105	-	-	24	mA
			while(1), all module clocks are ON	105	-	-	31	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	25	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	23	mA
			Full module clock ON	105	-	-	30	mA

1. Typ voltage condition, VCC=3.3 V
2. Max voltage condition VCC=1.8~3.6 V.

Table 3-10 Run Mode Current Consumption4

Mode	Parameter	Symbol	Conditions	T_A(°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
Operating Mode	f_{HCLK}= 8 MHz	ICC_RUN	while(1), all module clocks are OFF	-40	-	3.2	-	mA
			while(1), all module clocks are ON	-40	-	6	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	3.3	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	2.8	-	mA
			Full module clock ON	-40	-	5.6	-	mA
		ICC_RUN	while(1), all module clocks are OFF	25	-	3.4	-	mA
			while(1), all module clocks are ON	25	-	6.2	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	3.5	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	3.0	-	mA
			Full module clock ON	25	-	5.8	-	mA
		ICC_RUN	while(1), all module clocks are OFF	85	-	-	12.8	mA
			while(1), all module clocks are ON	85	-	-	16.4	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	13.3	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	9.7	mA
			Full module clock ON	85	-	-	15.7	mA
		ICC_RUN	while(1), all module clocks are OFF	105	-	-	19	mA
			while(1), all module clocks are ON	105	-	-	22	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	20	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	15.4	mA
			Full module clock ON	105	-	-	22.5	mA

1. Typ voltage condition, VCC=3.3 V
2. Max voltage condition VCC=1.8~3.6 V.

Table 3-11 Run Mode Current Consumption 5

Mode	Parameter	Symbol	Conditions	T_A(°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
Operating Mode	f_{HCLK}= 1 MHz	ICC_RUN	while(1), all module clocks are OFF	-40	-	2.4	-	mA
			while(1), all module clocks are ON	-40	-	3.9	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	2.4	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	2.4	-	mA
			Full module clock ON	-40	-	3.8	-	mA
		ICC_RUN	while(1), all module clocks are OFF	25	-	2.6	-	mA
			while(1), all module clocks are ON	25	-	4.1	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	2.6	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	2.5	-	mA
			Full module clock ON	25	-	4	-	mA
		ICC_RUN	while(1), all module clocks are OFF	85	-	-	11	mA
			while(1), all module clocks are ON	85	-	-	12.5	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	11.3	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	8.8	mA
			Full module clock ON	85	-	-	12.5	mA
		ICC_RUN	while(1), all module clocks are OFF	105	-	-	17.5	mA
			while(1), all module clocks are ON	105	-	-	18	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	18.1	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	14.5	mA
			Full module clock ON	105	-	-	18.7	mA

1. Typ voltage condition, VCC=3.3 V
2. Max voltage condition VCC=1.8~3.6 V.

Table 3-12 Low Power Mode Current Consumption

Mode	Parameter	Symbol	Condition (VCC = 3.3 V)	T_A(°C)	Product Specifications			Unit
					Min	Typ(3)	Max(2)	
Stop mode	-	ICC_STP	Stop mode	-40(1)	-	55	-	μA
				25(1)	-	204	-	μA
				85	-	1.1	6.7	mA
				105(1)	-	2	11	mA
Power Down Mode	-	ICC_PD	Power down mode 1(1)	-40	-	10	-	μA
			Power down mode 2(1)	-40	-	5	-	μA
			Power down mode 3(1)	-40	-	3	-	μA
			Power down mode 4(1)	-40	-	3	-	μA
			Power down mode 2+XTAL32+RTC	-40	-	6	-	μA
			Power-down mode 2+LRC+RTC(1)	-40	-	10	-	μA
			Power down mode 1(1)	25	-	11.5	-	μA
			Power down mode 2(1)	25	-	5.5	-	μA
			Power down mode 3(1)	25	-	3	-	μA
			Power down mode 4(1)	25	-	3.5	-	μA
			Power down mode 2+XTAL32+RTC	25	-	7	-	μA
			Power-down mode 2+LRC+RTC(1)	25	-	10.5	-	μA
			Power down mode 1	85	-	22.7	36	μA
			Power down mode 2	85	-	15.7	29	μA
			Power down mode 3	85	-	13.0	26	μA
			Power down mode 4	85	-	13.2	26	μA
			Power down mode 2+XTAL32+RTC	85	-	-	27	μA
			Power down mode 2+LRC+RTC	85	-	20.6	35	μA
			Power down mode 1(1)	105	-	36.4	60	μA
			Power down mode 2(1)	105	-	29.2	52	μA
			Power down mode 3(1)	105	-	26.4	49	μA
			Power down mode 4(1)	105	-	26.7	49	μA
			Power down mode 2+XTAL32+RTC	105	-	-	51	μA
			Power-down mode 2+LRC+RTC(1)	105	-	34.0	59	μA

1. Guarantee of mass production test.
2. Max voltage condition VCC=1.8~3.6 V.
3. Typ voltage condition, VCC=3.3 V

Table 3-13 Analog Module Current Consumption

Item	Parameter	Symbol	Conditions (VCC=AVCC=3.3V)	T_A(°C)	Product Specifications			Unit
					Min	Typ	Max	
Module current	-	ICC_MODULE	XTAL Oscillation Mode Large Drive 24MHz	25	-	1.8	-	mA
			Drive 16 MHz in Oscillation Mode	25	-	1	-	mA
			Oscillating mode small drive 10 MHz	25	-	0.8	-	mA
			Oscillating mode ultra-small drive 8 MHz	25	-	0.6	-	mA
			XTAL 32.768 kHz	25	-	1.1	-	μA
			HRC	25	-	0.3	-	mA
			PLLH(VCO=480 MHz)	25	-	2	-	mA
			PLLH(VCO=240 MHz)	25	-	1.1	-	mA
			ADC	25	-	1.3	-	mA
			DAC	25	-	0.2	-	mA
			CMP	25	-	0.3	-	mA
			PGA	25	-	0.7	-	mA
			USBFS(1)	25	-	6.0	-	mA

1. Design guarantee, including the current when the control part communicates with USBPHY, the load is 50 pf.

3.3.5 Low Power Mode Wake-up Timing

The wake-up time measurement method is from the wake-up event triggering to the CPU execution of the first instruction:

- For stop or sleep mode: Wakeup event is WFE.
- WKUP pins are used to wake up from standby, stop, and sleep modes. All the timings are measured at ambient temperature and VCC=3.3V.

Table 3-14 Low Power Mode Wake Up Time

Symbol	Parameter	Conditions	Typical Value	Max. Value	Unit
T_{STOP}	Wakeup from stop mode	System clock is MRC	20.4	35	μs
T_{PD1}	Wake up from power-down mode 1	-	35	78	
T_{PD2}	Wake up from power-down mode 2	-	119	270	
T_{PD3}	Wake up from power-down mode 3	-	2220	3000	
T_{PD4}	Wake up from power-down mode 4	-	205	447	

3.3.6 External Clock Source Characteristics

3.3.6.1 High-speed External Subscriber Clock Generated by External Source

In bypass mode, the XTAL oscillator is turned off and the input pins are standard I/O. External clock signals must take into account I/O static characteristics.

Table 3-15 High-Speed External User Clock Features

Symbol	Parameter	Conditions	Min.	Typical Value	Max.	Unit
f_{XTAL_EXT}	User external timer frequency	-	1	-	25(1)	MHz
V_{IH_XTAL}	XTAL_EXT input pin high level voltage(1)		0.8*V_{CC}	-	V_{CC}	V
V_{IL_XTAL}	XTAL_EXT input pin low level voltage(1)		V_{SS}	-	0.2*V_{CC}	
$t_{r(XTAL\_EXT)}$ $t_{f(XTAL\_EXT)}$	XTAL_EXT rise or fall time		-	-	5	ns
$Duty_{(XTAL\_EXT)}$	Duty Ratio	-	40	-	60	%

1. Guarantee of mass production test.

3.3.6.2 High-speed External Clock Produced by Crystal Oscillator/ Ceramic Resonator

High-speed external (XTAL) clocks can be produced using a 4 to 25 MHz crystal oscillator/ceramic resonator oscillator. In applications, the resonator and load capacitance must be as close to the oscillator pin as possible to minimize output distortion and vibration stabilization time. For more information on the resonator characteristics (frequency, encapsulation, accuracy, etc.), please consult the crystal resonator manufacturer.

Table 3-16 XTAL 4-25 MHz Oscillator Features

Symbol	Parameter	Conditions	Min.	Typical Value	Max.	Unit
f_{XTAL_IN}	Oscillator frequency	-	4	-	25	MHz
R_F	Feedback Resistance(1)	-	-	300	-	kΩ
A_{XTAL}	XTAL Accuracy(2)(3)	-	-500	-	500	ppm
G_{mmax}	Oscillator Gm(2)	Wake up	4	-	-	mA/V
$t_{SU(XTAL)}$	Start time (4)	VCC is stable, crystal oscillator=8MHz	-	2.0	-	ms
		VCC is stable, crystal oscillator=4MHz	-	4.0	-	ms

1. Guarantee of mass production test.
2. Design guaranteed.
3. This parameter depends on the resonator used in the application system.
4. $t_{SU(XTAL)}$is the start-up time, which is measured from the time XTAL is enabled by software until a stable oscillation frequency is obtained. This value is measured based on the standard crystal resonator and may vary significantly with the crystal resonator manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors designed for high-frequency applications that meet crystal or resonator requirements (see figure below). C_{L1} and C_{L2} are usually the same size, C_{L1}=C_{L2}=2*(C_L-Cs). Cs is the PCB and MCU pins (XTAL_IN, XTAL_OUT) stray capacitance. C_L is the load capacitance of the crystal or ceramic resonator. Please consult the crystal resonator manufacturer.

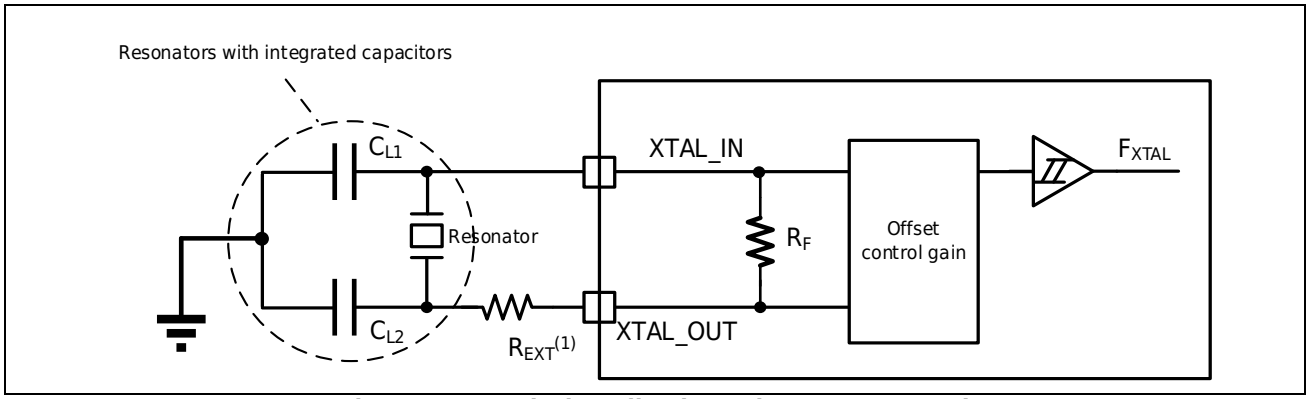


Figure 3-4 Typical Application Using 8 MHz Crystal

1. The value of R_{EXT} depends on the crystal oscillator characteristics.

3.3.6.3 Low-speed External Clock Generated by Crystal Oscillator/ Ceramic Resonator

Low-speed external clocks can be produced using a oscillator composed of 32.768 kHz crystal oscillator/ceramic resonator. In applications, the resonator and load capacitance must be as close to the oscillator pin as possible to minimize output distortion and vibration stabilization time. For more information on the resonator characteristics (frequency, encapsulation, accuracy, etc.), please consult the crystal resonator manufacturer.

Table 3-17 XTAL32 Oscillator Features

Symbol	Parameter	Conditions	Specifications			Unit
			Min	Typ	Max	
F_{XTAL32}	Frequency	-	-	32.768	-	kHz
R_F	Feedback Resistance(1)	-	-	15	-	MΩ
I_{DD_XTAL32}	Power consumption	XTAL32DRV[2:0]=0b000	-	0.8	-	μA
A_{XTAL32}	XTAL32 precision(3)	-	-500	-	500	ppm
G_{mmax}	Oscillator Gm((2)	XTAL32DRV[2:0]=0b000	5.6	-	-	μA/V
$T_{SUXTAL32}$	Start time (4)	VCC Stabilization	-	2	-	s

1. Guarantee of mass production test.
2. Design guaranteed.
3. This parameter depends on the resonator used in the application system.
4. $T_{SUXTAL32}$ is the start-up time, which is measured from the time when the software enables XTAL32 until a stable 32.768kHz oscillation frequency is obtained. This value is measured based on the standard crystal resonator and may vary significantly with the crystal resonator manufacturer.

For C_{L1} and C_{L2}, high quality external ceramic capacitors are recommended (see figure below). C_{L1} and C_{L2} are usually the same size, $C_{L1}=C_{L2}=2*(C_L-Cs)$. Cs is the PCB and MCU pins (XTAL32_IN, XTAL32_OUT) stray capacitance. If C_{L1} and C_{L2} are greater than 18 pF, it is recommended to set XTAL32DRV[2:0] = 0b001 (large drive, power consumption increases by 0.2 μA typically). C_L is the load capacitance of the crystal or ceramic resonator. Please consult the crystal resonator manufacturer.

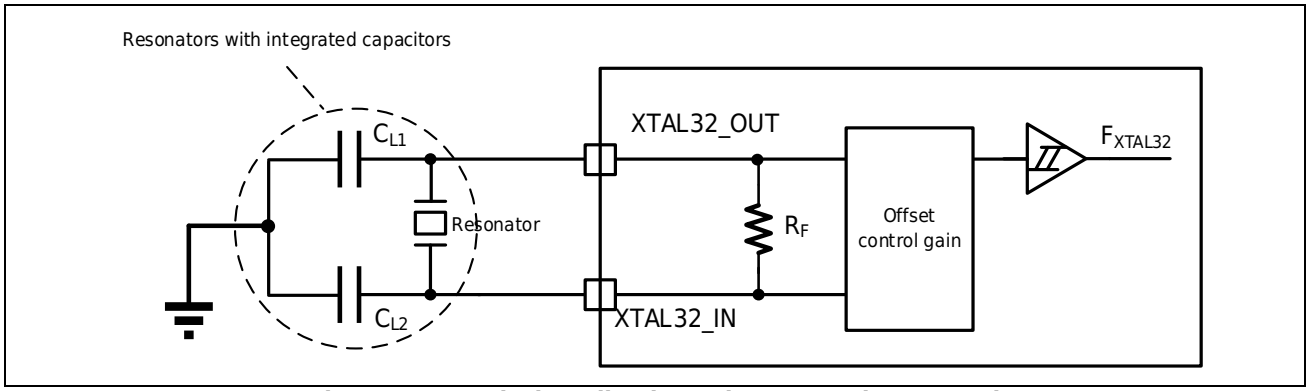


Figure 3-5 Typical Application Using 32.768 kHz Crystal

3.3.7 Internal Clock Source Characteristics

3.3.7.1 Internal High Speed (HRC) Oscillator

Table 3-18 HRC Oscillator Characteristics

Symbol	Parameter	Conditions	Min.	Typical Value	Max.	Unit
f_{HRC}	Frequency(1)	Pattern 1	-	16	-	MHz
		Pattern 2	-	20	-	
	User Adjustment Scale	-	-	-	0.2	%
	Speed Precision	T_A = -40 to 105 ℃(1)	-3	-	3	%
		T_A = -20 to 105 ℃	-2.5	-	2.5	%
		T_A = -20 to 85 ℃	-2	-	2	%
		T_A = 25 ℃(1)	-1.5	-	1.5	%
$t_{st(HRC)}$	HRC oscillator oscillation stabilization time(1)	-	-	-	15	μs

1. Guarantee of mass production test.

3.3.7.2 Internal Medium Speed (MRC) Oscillator

Table 3-19 MRC Oscillator Characteristics

Symbol	Parameter	Min.	Typical Value	Max.	Unit
f_{MRC}	Frequency(1)	7.2	8	8.8	MHz
$t_{st(MRC)}$	MRC oscillator stabilization time(1)	-	-	3	μs

1. Guarantee of mass production test.

3.3.7.3 Internal Low Speed (LRC) Oscillator

Table 3-20 LRC Oscillator Characteristics

Symbol	Parameter	Min.	Typical Value	Max.	Unit
f_{LRC}	Frequency(1)	27.853	32.768	37.683	kHz
$t_{st(LRC)}$	LRC oscillator stabilization time(1)	-	-	36	μs

1. Guarantee of mass production test.

3.3.7.4 SWDT dedicated internal low-speed (SWDTLRC) oscillator

Table 3-21 SWDTLRC Oscillator Characteristics

Symbol	Parameter	Min.	Typical Value	Max.	Unit
$f_{SWDTLRC}$	Frequency(1)	9	10	11	kHz
tst(SWDTLRC)	SWDTLRC oscillator stabilization time(1)	-	-	57.1	μs

1. Guarantee of mass production test.

3.3.8 PLL Characteristic

Table 3-22 PLLH Main Performance Indicators

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL PFD (Phase Frequency Detector) input clock(1) (2)	-	1	-	25	MHz
f_{PLL_OUT}	PLL multiplier output clock	-	15	-	120	MHz
f_{VCO_OUT}	PLL VCO output (1)	-	240	-	480	MHz
t_{LOCK}	PLL lock time(1)	-	-	80	120	μs
$Jitter_{PLL}$	Period Jitter	PLL PFD input clock=8 MHz, System clock=120 MHz, Peak-to-Peak	-	±100	-	ps
	Cycle-to-Cycle Jitter	PLL PFD input clock=8 MHz, System clock=120 MHz, Peak-to-Peak	-	±150	-	

1. Guarantee of mass production test.
2. It is recommended to use a higher input clock to obtain good Jitter characteristics.

3.3.9 Memory (Flash) Features

Flash memory was erased when the device was delivered to the customer.

Table 3-23 Flash Features

Symbol	Parameter	Conditions	Min.	Typical Value	Max.	Unit
I_{VCC}	Power supply current(1)	Read mode, V_{CC} = 1.8 V~3.6 V	-	-	5	mA
		Programming mode, V_{CC} = 1.8 V~3.6 V	-	-	10	
		Block erase mode, V_{CC} = 1.8 V~3.6 V	-	-	10	
		Full erase mode, V_{CC} = 1.8 V~3.6 V	-	-	10	

1. Design guaranteed.

Table 3-24 Flash Program Erase Time

Symbol	Parameter	Conditions	Min.	Typical Value	Max.	Unit
T_{prog}	Word programming time(1)	Single programming mode	43+2* T_{hclk}(2)	48+4* T_{hclk}(2)	53+6* T_{hclk}(2)	μs
	Word programming time(1)	Continuous programming mode	12+2* T_{hclk}(2)	14+4* T_{hclk}(2)	16+6* T_{hclk}(2)	μs
T_{erase}	Block erase time(1)	-	16+2* T_{hclk}(2)	18+4* T_{hclk}(2)	20+6* T_{hclk}(2)	ms
T_{mas}	Full erase time(1)	-	16+2* T_{hclk}(2)	18+4* T_{hclk}(2)	20+6* T_{hclk}(2)	ms

1. Guarantee of mass production test.
2. T_{hclk} is one cycle of CPU clock.

Table 3-25 Flash Memory Erasability and Data Retention Period

Symbol	Parameter	Conditions	Numerical Value	Unit
			Min.	
N_{end}	Programming, number of block erases	T_A = 85 ℃	10	Thousands of times
N_{end}	Number of whole erases	T_A = 85 ℃	10	Thousands of times
T_{ret}	Data retention period	T_A = 85 ℃	10	Year

3.3.10 Electrical Sensitivity

The chip is tested differently (ESD, LU) using specific measurement methods to determine its performance in terms of electrical susceptibility.

3.3.10.1 Electrostatic Discharge (ESD)

Electrostatic discharge is applied to the pins of each sample according to each pin combination. This test complies with JS001/JS002 standards.

Table 3-26 ESD Characteristics

Symbol	Parameter	Conditions	Max.	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage	T_A =+25°C, meet JS001 standard	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging equipment model)	T_A =+25°C, meet JS002 standard	1000	

3.3.10.2 Static Latch-up

To assess static Latch-up performance, two complementary static Latch-up tests are required on the chip:

- Over-voltage applied to each power supply and analog input pin
- Apply current injection to other input, output, and configurable I/O pins

These tests comply with the JESD 78 IC Latch-up standard.

Table 3-27 Static Latch-up Features

Symbol	Parameter	Conditions	Max.	Unit
LU	Static Latch-up	T_A =+105 °C, compliant with JESD78	200	mA

3.3.11 I/O Port Characteristics

Universal Input/output Characteristics

Table 3-28 I/O Static Characteristics

Symbol	Parameter		Conditions	Min.	Typical Value	Max.	Unit
V_{IL}	Schmitt input low level(1)		1.8≤V_{CC}≤3.6	-	-	0.3V_{CC}	V
V_{IH}	Schmitt input high level(1)		1.8≤V_{CC}≤3.6	0.7V_{CC}	-	-	V
V_{HYS}	Schmitt Input Hysteresis		1.8≤V_{CC}≤3.6	0.1	0.2	-	V
V_{IL}	CMOS Input Low Level(1)		1.8≤V_{CC}≤3.6	-	-	0.3V_{CC}	V
V_{IH}	CMOS input high level(1)		1.8≤V_{CC}≤3.6	0.7V_{CC}	-	-	V
TTL_V_{IL}	CMOS/ Schmitt compatible TTL input low level(1)		2.7≤V_{CC}≤3.6	-	-	0.8	V
TTL_V_{IH}	CMOS/ Schmitt compatible TTL input high level(1)		2.7≤V_{CC}≤3.6	2.2	-	-	V
TTL_V_{IH}	CMOS compatible TTL input high level(1)		2.7≤V_{CC}≤3.47	2.0	-	-	V
Fmax(in)	Schmitt input maximum frequency		2.7≤V_{CC}≤3.6	-	-	40	MHz
			1.8≤V_{CC}≤2.7	-	-	20	MHz
	CMOS input maximum frequency		2.7≤V_{CC}≤3.6	-	-	80	MHz
			1.8≤V_{CC}≤2.7	-	-	40	MHz
I_{LKG}	I/O input leakage current(1)		V_{SS}≤V_{IN}≤V_{CC}	-	-	1	μA
			V_{IN} = 5.5V(2)	-	-	10	μA
R_{PU}	Weak pull-up Equivalent resistance(1) (3) (5)	-	V_{IN} = V_{SS} 1.8≤V_{CC}≤3.6	10	30	150	KΩ
Rpd	Weak pull-down Equivalent resistance(1) (3) (5)	-	V_{IN} = Vcc 1.8≤V_{CC}≤3.6	5	20	50	KΩ
R_{PD}	Weak pull-down Equivalant resistance(4) (5)	PA11/ USBFS_DM PA12/ USBFS_DP	V_{IN} = V_{CC}	-	500	-	KΩ
C_{IO}	I/O Pin Capacitance(2)	PA11 (USBFS_DM) PA12 (USBFS_DP) PB6, PB7, PB10, PB11 (I2C) PF3 (MD)	-	-	10	-	pF
		Input pins other than those mentioned above	-	-	5	-	pF

1. Guarantee of mass production test.
2. Design guaranteed.
3. For PA11/USBFS_DM and PA12/USBFS_DP, it indicates the weak pull-up equivalent resistance value of GPIO when the USB function is disabled. For the pull-up/pull-down resistors for USB functions, please refer to the section [USB Interface Features] .
4. Only PA11/USBFS_DM and PA12/USBFS_DP have weak pull-down resistors, which are always valid.
5. To keep the voltage above V_{CC}+0.3 V, the internal pull-up/pull-down resistors must be disabled.

Output Current

The GPIO (universal Purpose Input/Output) can source or sink current up to ±20mA.

The output voltage

Table 3-29 Output Voltage Characteristics

Drive Setup	Symbol	Parameter	Conditions	Min.	Typical Value	Max.	Unit
Low drive	V_{OL}	Low level output(1)(2)	I_{IO}=±1.5 mA, 1.8≤V_{CC}<2.7	-	-	0.6	V
	V_{OH}	High level output(1)(3)		V_{CC}-0.6	-	-	
	V_{OL}	Low level output(1)(2)	I_{IO}=±3 mA, 2.7≤V_{CC}≤3.6	-	-	0.6	
	V_{OH}	High level output(1)(3)		V_{CC}-0.6	-	-	
	V_{OL}	Low level output(1)(2)	I_{IO}=±6 mA, 2.7≤V_{CC}≤3.6	-	-	1.3	
	V_{OH}	High level output(1)(3)		V_{CC}-1.3	-	-	
Medium drive	V_{OL}	Low level output(1)(2)	I_{IO}=±3 mA, 1.8≤V_{CC}<2.7	-	-	0.4	
	V_{OH}	High level output(1)(3)		V_{CC}-0.4	-	-	
	V_{OL}	Low level output(1)(2)	I_{IO}=±5 mA, 2.7≤V_{CC}≤3.6	-	-	0.4	
	V_{OH}	High level output(1)(3)		V_{CC}-0.4	-	-	
	V_{OL}	Low level output(1)(2)	I_{IO}=±12 mA, 2.7≤V_{CC}≤3.6	-	-	1.3	
	V_{OH}	High level output(1)(3)		V_{CC}-1.3	-	-	
High drive	V_{OL}	Low level output(1)(2)	I_{IO}=±6 mA, 1.8≤V_{CC}<2.7	-	-	0.4	
	V_{OH}	High level output(1)(3)		V_{CC}-0.4	-	-	
	V_{OL}	Low level output(1)(2)	I_{IO}=±8 mA, 2.7≤V_{CC}≤3.6	-	-	0.4	
	V_{OH}	High level output(1)(3)		V_{CC}-0.4	-	-	
	V_{OL}	Low level output(1)(2)	I_{IO}=±20 mA, 2.7 ≤V_{CC}≤3.6	-	-	1.3	
	V_{OH}	High level output(1)(3)		V_{CC}-1.3	-	-	
	V_{OL}	Low level output(1)(2)	I_{IO}=±20 mA, 2.97≤V_{CC}≤3.6	-	-	0.88	
	V_{OH}	High level output(1)(3)		V_{CC}-0.88	-	-	
IIC/FM+	VOLFM+	Low level output(1)(2)	I_{IO}=20 mA, 2.7≤V_{CC}≤3.6	-	-	0.4	

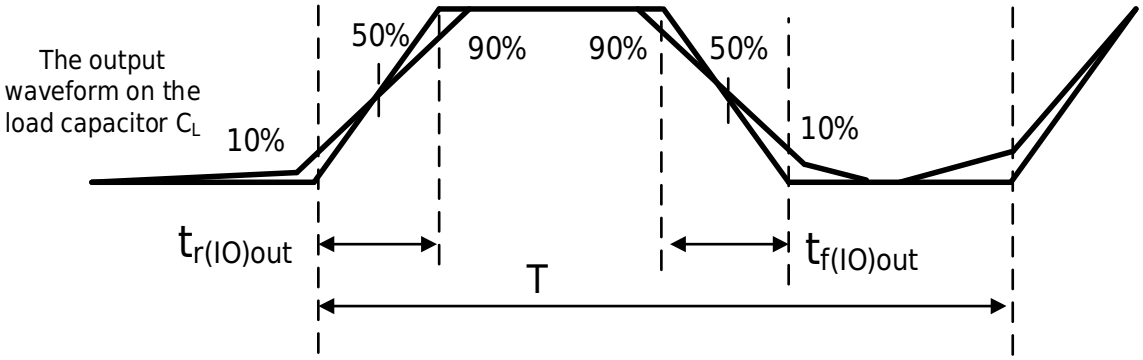
1. Guarantee of mass production test.
2. The I_{IO} current sunk by the device must always consider the absolute maximum ratings specified in the tableTable 3-2. The sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
3. The I_{IO} source current of the device must always adhere to the absolute maximum ratings listed in TableTable 3-2, and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VCC}.

Output AC Characteristics

Table 3-30 I/O AC Characteristics

Driver Settings	Symbol	Parameter	Condition(3)	Min.	Typical Value	Max.	Unit
Low drive	f_{max}(IO)out	Maximum frequency(1)	C_L=30 pF, V_{CC}≥ 2.7 V	-	-	20	MHz
			C_L=30 pF, V_{CC}≥1.8 V	-	-	10	
			C_L=10 pF, V_{CC}≥2.7 V	-	-	40	
			C_L=10 pF, V_{CC}≥1.8 V	-	-	20	
	t_f(IO)out t_r(IO)out	Output high to low level drop time and output low to high level rise time	C_L=30 pF, V_{CC}≥2.7 V	-	-	15	ns
			C_L=30 pF, V_{CC}≥1.8 V	-	-	25	
			C_L=10 pF, V_{CC}≥2.7 V	-	-	7.5	
			C_L=10 pF, V_{CC}≥1.8 V	-	-	15	
Medium drive	f_{max}(IO)out	Maximum frequency(1)	C_L=30 pF, V_{CC}≥ 2.7 V	-	-	45	MHz
			C_L=30 pF, V_{CC}≥1.8 V	-	-	22.5	
			C_L=10 pF, V_{CC}≥2.7 V	-	-	90	
			C_L=10 pF, V_{CC}≥1.8 V	-	-	45	
	t_f(IO)out t_r(IO)out	Output high to low level drop time and output low to high level rise time	C_L=30 pF, V_{CC}≥2.7 V	-	-	6	ns
			C_L=30 pF, V_{CC}≥1.8 V	-	-	10	
			C_L=10 pF, V_{CC}≥2.7 V	-	-	4	
			C_L=10 pF, V_{CC}≥1.8 V	-	-	6	
High drive	f_{max}(IO)out	Maximum frequency (1)	C_L=30 pF, V_{CC}≥2.7 V	-	-	100	MHz
			C_L=30 pF, V_{CC}≥1.8 V	-	-	50	
			C_L=10 pF, V_{CC}≥1.8 V	-	-	100	
	t_f(IO)out t_r(IO)out	Output high to low level drop time and output low to high level rise time	C_L=30 pF, V_{CC}≥2.7 V	-	-	4	ns
			C_L=30 pF, V_{CC}≥1.8 V	-	-	6	
			C_L=10 pF, V_{CC}≥2.7 V	-	-	2.5	
			C_L=10 pF, V_{CC}≥1.8 V	-	-	3.5	

1. The maximum frequency is defined in Figure Figure 3-6.
2. The load capacitance C_L must take into account the capacitance of the PCB and MCU pins (the capacitance between USB pins PA11, PA12 and I2C pins PB6, PB7, PB10, PB11 and MD pin PF3 and the circuit board can be roughly estimated as 15 pF respectively; the capacitance between other pins and the circuit board can be roughly estimated as 10 pF).



Maximum frequency condition: $(t_r+t_f)\leq(2/3)T$ and Duty cycle=50%±5% (Load capacitance CL is indicated in the "Conditions" column of the "Input/Output AC Features" table)

Figure 3-6 I/O AC Feature Definition

3.3.12 I2C Interface Characteristics

Table 3-31 I2C Electrical Characteristics

Symbol	Parameter	Standard Mode (SM)		Fast Mode (FM)		Fast Mode Plus(FM+) (3)		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL frequency	0	100	0	400	0	1000	kHz
$t_{HD;STA}$	Start condition/restart condition Hold	4.0	-	0.6	-	0.26	-	μs
t_{LOW}	SCL low level	4.7	-	1.3	-	0.5	-	μs
t_{HIGH}	SCL high level	4	-	0.6	-	0.26	-	μs
$t_{SU;STA}$	Restarting Condition Setup	4.7	-	0.6	-	0.26	-	μs
$t_{HD;DAT}$	Data Hold(1)	0	-	0	-	0	-	μs
$t_{SU;DAT}$	Data setup(1)	30+ $t_{I2C\ reference\ clock\ period}$ (2)	-	30+ $t_{I2C\ reference\ clock\ period}$ (2)	-	30+ $t_{I2C\ reference\ clock\ period}$ (2)	-	ns
t_R	Ascending time of SCL/SDA	-	1000	-	300	-	120	ns
t_F	Falling time of SCL/SDA	-	300	-	300	-	120	ns
$t_{SU;STO}$	Stop Condition Setup	4	-	0.6	-	0.26	-	μs
t_{BUF}	BUS Idle Time Between Stop Condition and Start Condition	4.7	-	1.3	-	0.5	-	μs
C_b	Load Capacitance	-	400	-	400	-	550	pF

1. Guarantee of mass production test.
2. $t_{I2C\ reference\ clock\ period}$ is the I2C reference clock period, which is set by the I2C_CCR.FREQ[2:0] bits.
3. FM+ mode, the I2C function needs to be configured on ports PB6, PB7, PB10, and PB11 .

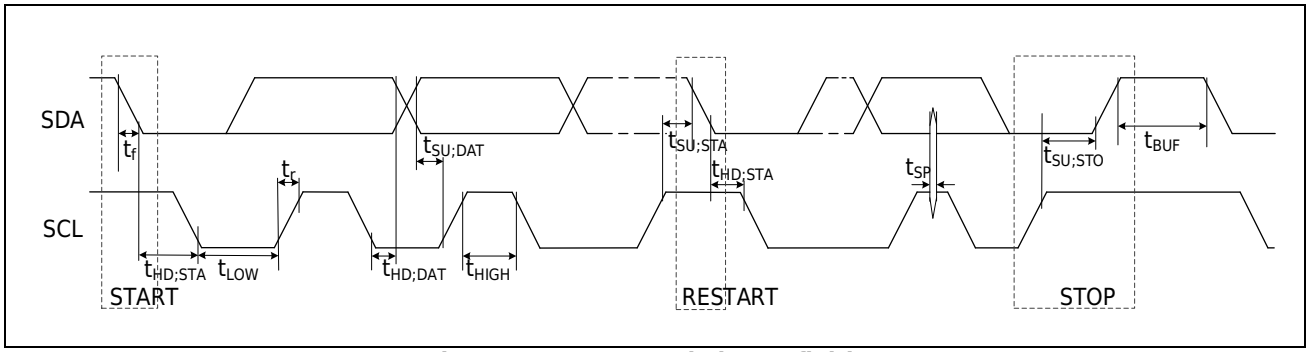


Figure 3-7 I2C Bus Timing Definition

3.3.13 MDIO Interface Features

Table 3-32 MDIO Electrical Characteristics

Symbol	Performance	Min	Typ	Max	Unit
f_{MDC}	MDC clock frequency	-	-	4	MHz
t_{setup}	MDIO setup time(1)	10	-	-	ns
t_{hold}	MDIO hold time(1)	10	-	-	ns
t_{delay}	MDIO output delay(1)	-	-	175	ns

1. Guarantee of mass production test.

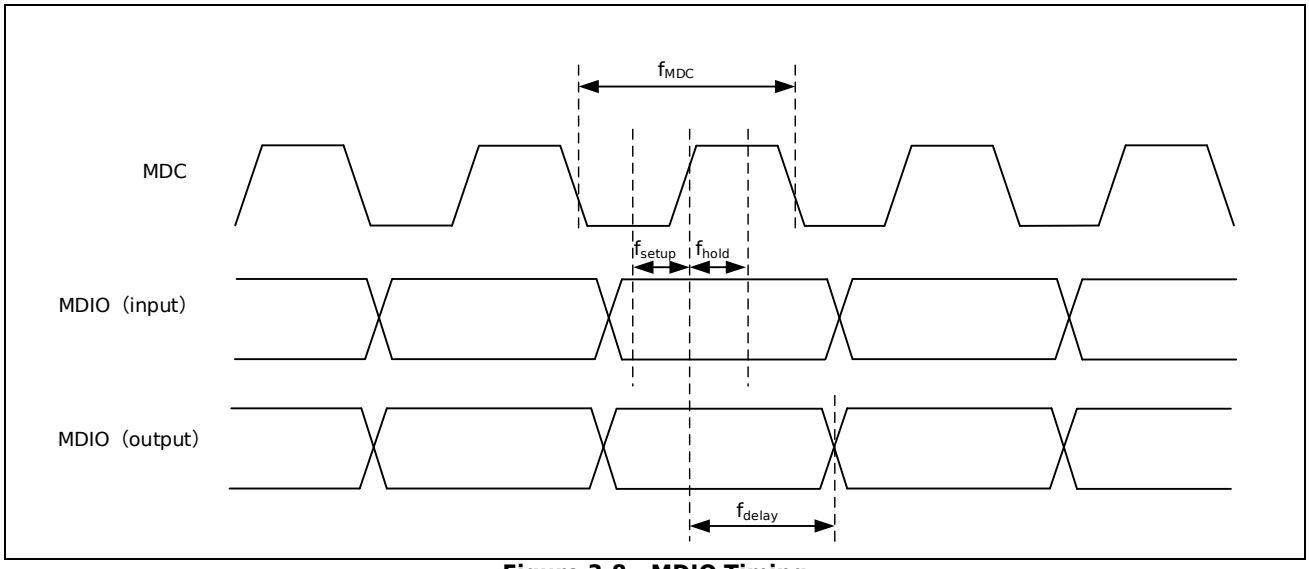


Figure 3-8 MDIO Timing

3.3.14 SPI Interface Features

Table 3-33 SPI Electrical Characteristics

Symbol	parameter	Conditions	min	max	Unit
t_w(SCKH)	SCK high level time	Master Mode(4), 1.8 V≤Vcc≤3.6 V	T_{pclk1}-1(5)	T_{pclk1}+1(5)	ns
		Slave Mode(4), 1.8 V≤Vcc≤3.6 V	3xT_{pclk1}-1(5)	3xT_{pclk1}+1(5)	ns
t_w(SCKL)	SCK low level time	Master Mode, 1.8V≤Vcc＜3.6V	T_{pclk1}-1(5)	$T_{pclk1*1}$+1(5)	ns
		Slave Mode, 1.8V≤Vcc≤3.6V	3xT_{pclk1}-1(5)	3xT_{pclk1}+1(5)	ns
t_{su}(SI)	Data input setup time	Slave Mode, 1.8V≤Vcc≤3.6V	4	-	ns
t_h(SI)	Data input hold time	Slave Mode, 1.8V≤Vcc≤3.6V	3	-	ns
t_v(SO)	Data output valid time	Slave Mode, 2.7V≤Vcc≤3.6V(1)	-	15	ns
		Slave Mode, 1.8V≤Vcc≤2.7V	-	26	ns
t_{su}(MI)	Data input setup time	Master Mode, 2.7V≤Vcc≤3.6V(1)	5	-	ns
		Master Mode, 1.8V≤Vcc＜2.7V	9	-	ns
t_h(MI)	Data input hold time	Master Mode, 2.7V≤Vcc≤3.6V(1)	5	-	ns
		Master Mode, 1.8V≤Vcc＜2.7V	15	-	ns
t_{su}(SS)	SS establishment time	Slave Mode, 1.8V≤Vcc≤3.6V	6×T_{pclk1} (5)	-	ns
		Master Mode, 2.7V≤Vcc≤3.6V	-5+N×T_{sck}(2) (5)	-	ns
		Master Mode, 1.8V≤Vcc＜2.7V	-10+N×T_{sck}(2) (5)	-	ns
t_h(SS)	SS hold time	Slave Mode, 1.8V≤Vcc≤3.6V	6×T_{pclk1}(5)	-	ns
		Master Mode, 2.7V≤Vcc≤3.6V	-5+N×T_{sck}(3) (5)	-	ns
		Master Mode, 1.8V≤Vcc＜2.7V	-10+N×T_{sck}(3) (5)	-	ns
t_v(MO)	Data output valid time	Master Mode, 2.7V≤Vcc≤3.6V(1)	-	4	ns
		Master Mode, 1.8V≤Vcc≤2.7V	-	9	ns

1: Guarantee of mass production test.

2: N=1~8, determined by register SPI_CFG1.MSSI[2:0].

3: N=1~8, determined by register SPI_CFG1.MSSDL[2:0].

4: The values of t_w(SCKH) and t_w(SCKL)) are determined by SPI_CFG2.MBR. The values listed in the table are those when SPI_CFG2.MBR=0.

5: T_{pclk1} refers to one cycle of the clock PCLK1, and T_{sck} refers to one cycle of the SPI communication clock.

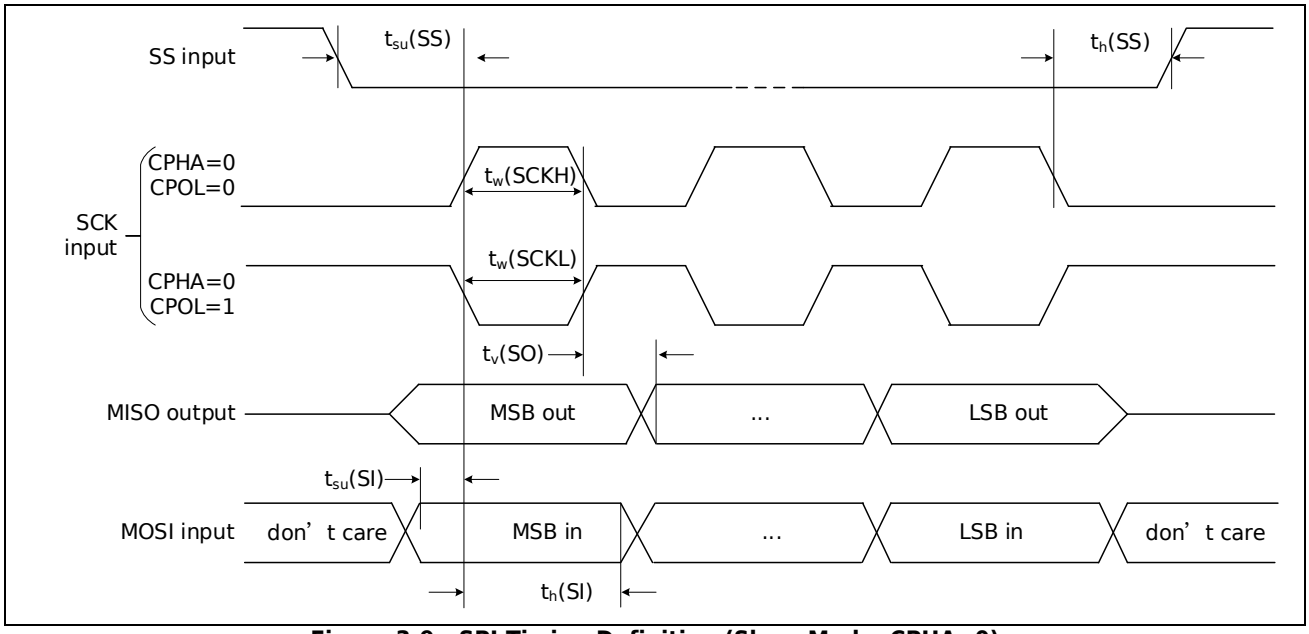


Figure 3-9 SPI Timing Definition (Slave Mode, CPHA=0)

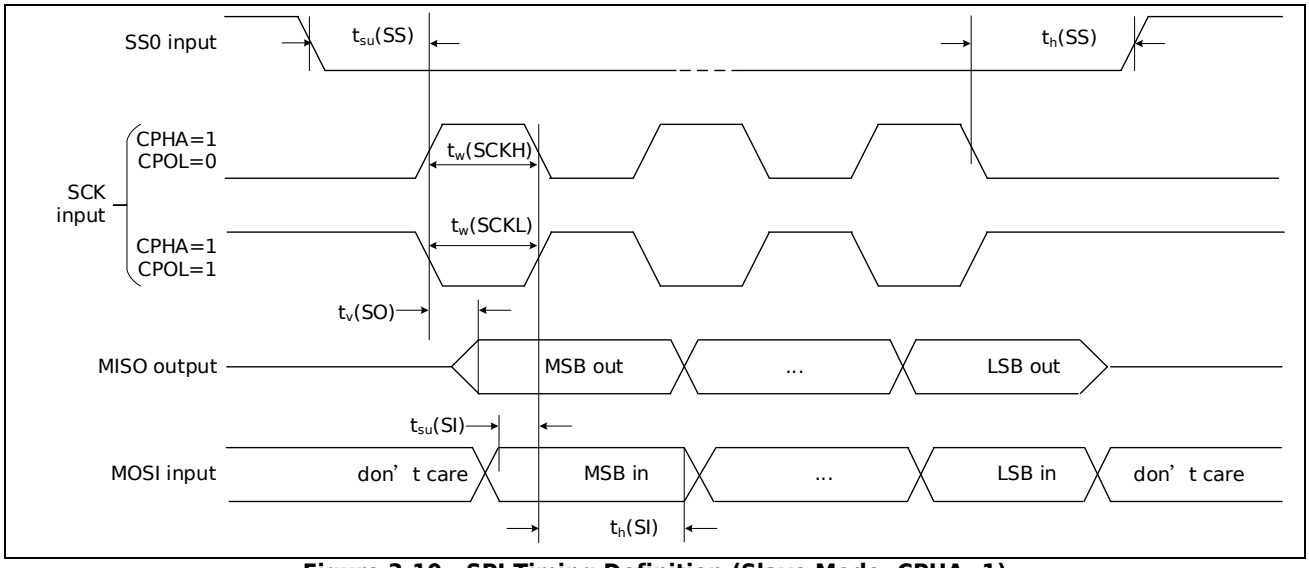


Figure 3-10 SPI Timing Definition (Slave Mode, CPHA=1)

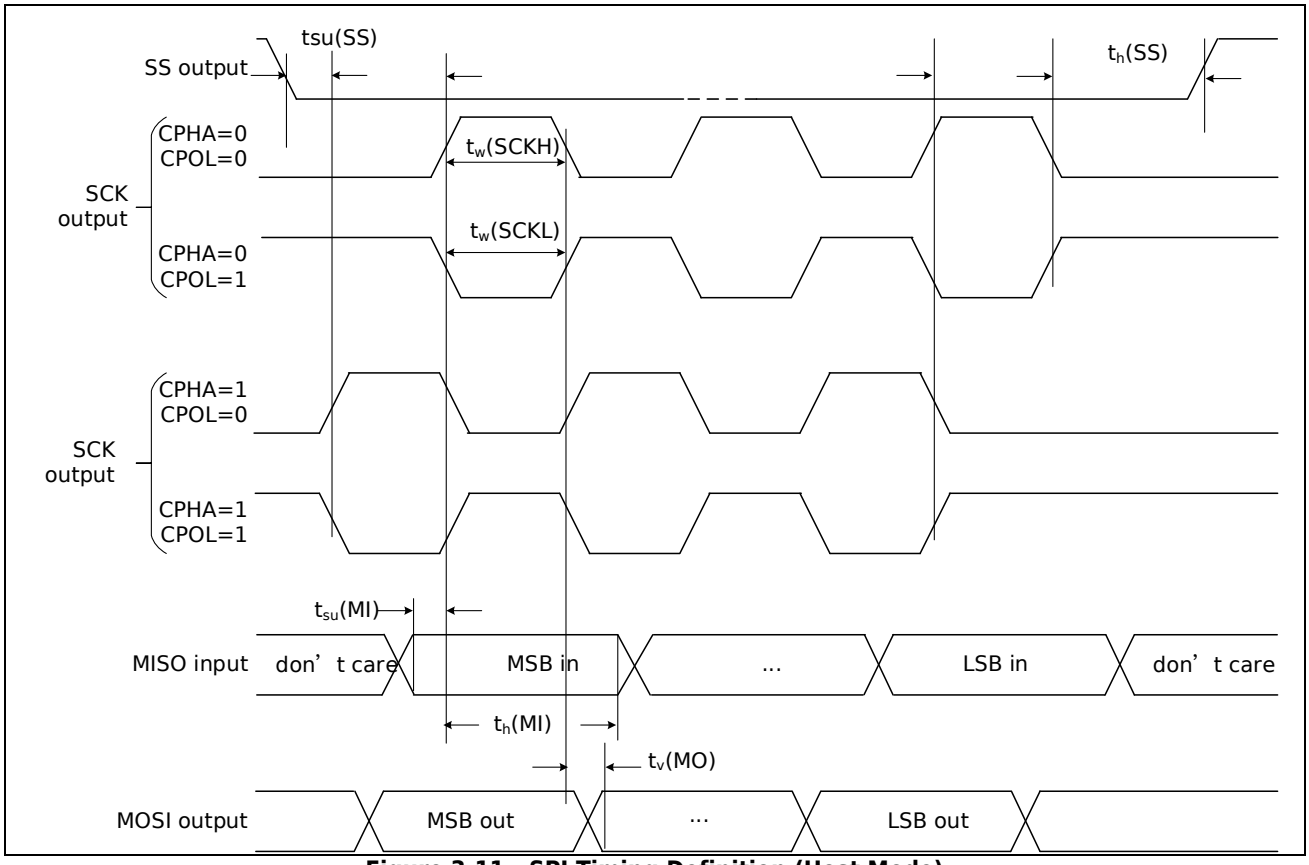


Figure 3-11 SPI Timing Definition (Host Mode)

3.3.15 QSPI Interface Features

Table 3-34 QSPI Electrical Characteristics

Symbol	parameter	Min	Max	Unit
t_{Qscyc}	SCK clock cycles	2	64	Thclk
t_{QSWH}	SCK High Level	t_{Qscyc}×0.4	-	ns
t_{QSWL}	SCK Low Level	t_{Qscyc}×0.4	-	ns
t_{SU}	Data input setup time (2.7 V~3.6 V)(1)	5	-	ns
	Data input setup time (1.8 V~2.7 V)	5	-	ns
t_{IH}	Data input setup time (2.7 V~3.6 V)(1)	5	-	ns
	Data input hold time (1.8 V~2.7 V)	15	-	ns
t_{OD}	Data output delay(1)	-	4	ns
t_{OH}	Data output hold time	0	-	ns

1. Guarantee of mass production test.

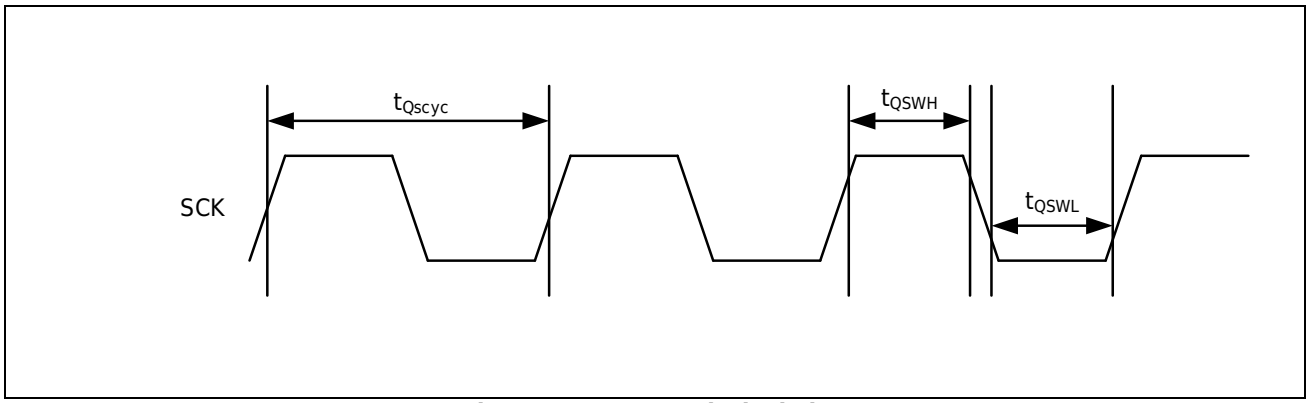


Figure 3-12 QSPI Clock Timing

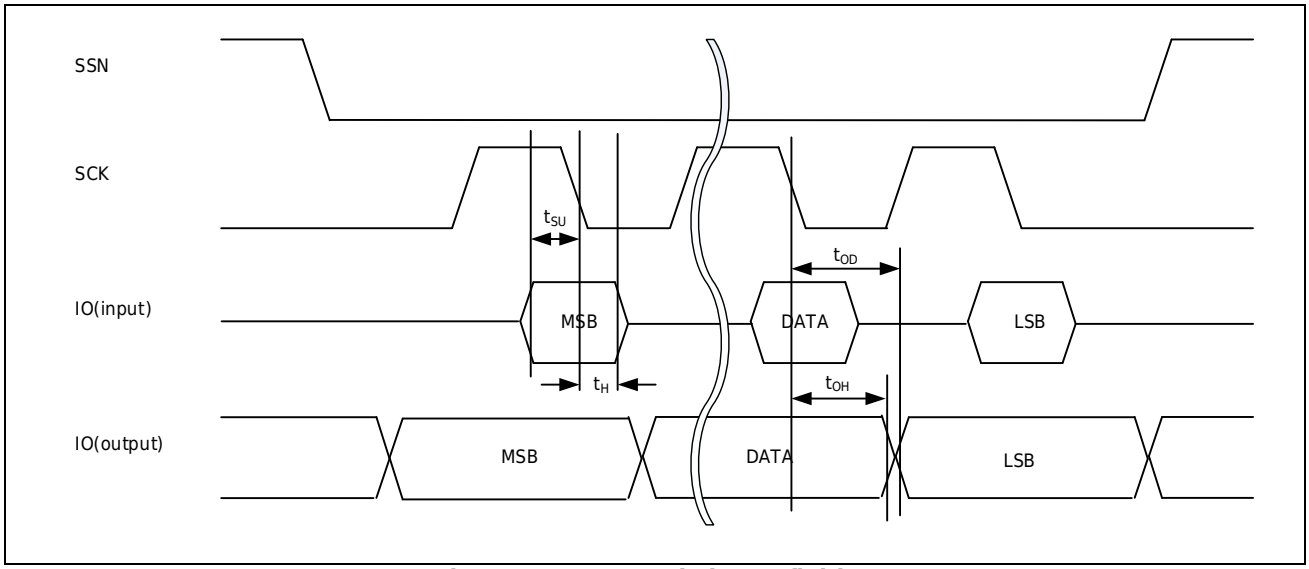


Figure 3-13 QSPI Timing Definition

3.3.16 USB Interface Features

Table 3-35 USB Full-Speed Electrical Characteristics

Symbol		Parameter	Conditions	Min.(3)	Typ.	Max.(3)	Unit
Input	V_{CC}	Operating voltage(2)	-	3.0	-	3.6	V
	V_{IL}	Input low level(1)	-	-	-	0.8	V
	V_{IH}	Input high level(1)	-	2.0	-	-	V
	V_{DI}	Differential input sensitivity(1)	-	0.2	-	-	V
	V_{CM}	Differential common mode voltage(1)	-	0.8	-	2.5	V
Output	V_{OL}	Static output low level (1) (4)	R_L=1.5 kΩ to 3.6 V	-	-	0.3	V
	V_{OH}	Static output high level (1) (4)	R_L=15 kΩ to VSS	2.8	-	3.6	V
	V_{CRS}	Cross-over voltage	C_L=50 pF	1.3	-	2.0	V
	t_R	Rise time	C_L=50 pF, 10%~90% of $\|V_{OH}-V_{OL}\|$	4	-	20	ns
	t_F	Fall time	C_L=50 pF, 10%~90% of $\|V_{OH}-V_{OL}\|$	4	-	20	ns
	t_{RFMA}	Rise and fall time ratio t_R/t_F	C_L=50 pF	90	-	111	%
R_{PD}		Pull-down resistor (1)	V_{IN} = V_{CC}, in host mode	-	15.0	-	kΩ
R_{PU}		Pull-up resistor(1)	V_{IN} = V_{SS}, idle state	0.900	1.2	1.575	kΩ
			V_{IN} = V_{SS}, in device mode	1.425	2.3	3.090	kΩ
Z_{DRV}		Output Impedance(5)	Driving high or low	28	36	44	Ω

1. Guarantee of mass production test.
2. The function of the USB full-speed transceiver is still guaranteed when the operating voltage is reduced to 2.7V, but the complete USB full-speed electrical characteristics are not guaranteed, which will be degraded in the V_{CC} voltage range of 2.7 to 3.0V.
3. All voltages are measured against local ground potential.
4. R_L is the load connected to the USB full speed drive.
5. The DP and DM ports do not require external series resistors for impedance matching. The Driver output already includes the matching resistor. This feature is guaranteed by design.
6. The DP and DM ports do not require external pull-up/pull-down resistors, as they are integrated inside the PHY.

Table 3-36 USB Low-Speed Electrical Characteristics

Symbol		Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
Input	V_{CC}	Operating voltage(2)	-	3.0	-	3.6	V
	V_{IL}	Input low level	-	-	-	0.8	V
	V_{IH}	Input high level	-	2.0	-	-	V
	V_{DI}	Differential Input Sensitivity	-	0.2	-	-	V
	V_{CM}	Differential Common Mode Voltage	-	0.8	-	2.5	V
Output	V_{OL}	Static output low level(3)	R_L=1.5 kΩ to 3.6 V	-	-	0.3	V
	V_{OH}	Static output high level(3)	R_L=15 kΩ to VSS	2.8	-	3.6	V
	V_{CRS}	Cross-over voltage	C_L=200 pF~600 pF	1.3	-	2.0	V
	t_R	Rise time	C_L=200 pF~600 pF, 10%~90% of $\|V_{OH}-V_{OL}\|$	75	-	300	ns
	t_F	Fall time	C_L=200 pF~600 pF, 10%~90% of $\|V_{OH}-V_{OL}\|$	75	-	300	ns
	t_{RFMA}	Rise and fall time ratio t_R/t_F	C_L=200 pF~600 pF	80	-	125	%
R_{PD}		Pull-down resistor	V_{IN} = V_{CC}, in host mode	-	15.0	-	kΩ
Z_{DRV}		Output Impedance(4)	Driving high or low	28	36	44	Ω

1. All voltages are measured against local ground potential.
2. When the operating voltage drops to 2.7V, the function of the USB low-speed transceiver can still be guaranteed, but the complete USB low-speed electrical characteristics cannot be guaranteed, and the latter will be degraded in the V_{CC} voltage range of 2.7 to 3.0V.
3. R_L is the load connected to the USB low-speed drive.
4. The DP and DM ports do not require external series resistors for impedance matching. The Driver output already includes the matching resistor. This feature is guaranteed by design.
5. The DP and DM ports do not require external pull-up/pull-down resistors, as they are integrated inside the PHY.

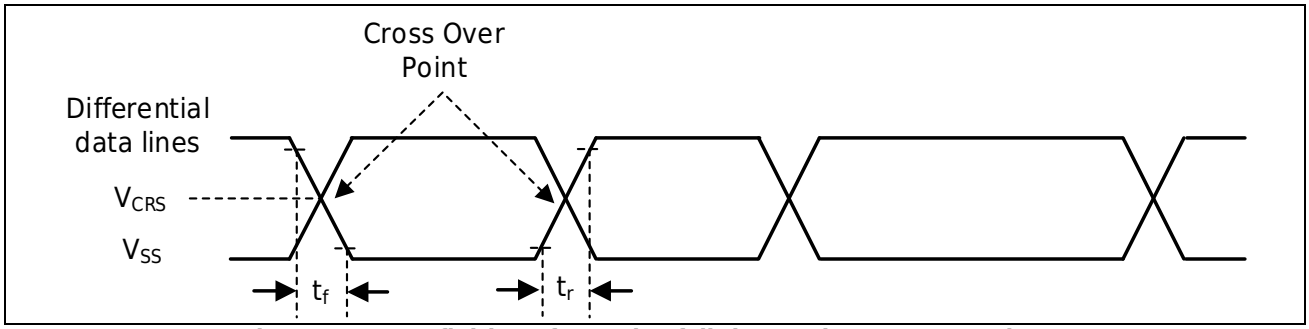


Figure 3-14 Definition of USB rise/fall time and Cross Over voltage

3.3.17 USART Interface Characteristics

Table 3-37 USART Electrical Characteristics

Symbol	Parameter		Min.	Max.	Unit
t_{cyc}	Input clock cycles	UART	4	-	t_{PCLK1}
		Clock synchronization mode	6	-	
t_{CKw}	Input clock width		0.4	0.6	t_{cyc}
t_{CKr}	Input clock rise time		-	5	ns
t_{CKf}	Input clock fall time		-	5	ns
t_{TD}	Transmit delay time 2.7 V≤Vcc≤3.6 V(1)	Clock synchronization mode	-	23	ns
	Transmit delay time 1.8 V≤Vcc<2.7 V	Clock synchronization mode	-	30	ns
t_{RDS}	Receiving data setup time 2.7 V≤Vcc≤3.6 V(1)	Clock synchronization mode	17	-	ns
	Receiving data setup time 1.8 V≤Vcc<2.7 V	Clock synchronization mode	23	-	ns
t_{RDH}	Receiving data hold time	Clock synchronization mode	5	-	ns

1. Guarantee of mass production test.

Table 3-38 USARTHighest Baud Rate

Mode		Maximum Baud Rate
UART	Internal clock source	PCLK1/8
	External clock source	PCLK1/32
Clock synchronization mode 2.7 V≤Vcc≤3.6 V		6.0 Mbps
Clock synchronization mode 1.8 V≤Vcc<2.7 V		4.0 Mbps

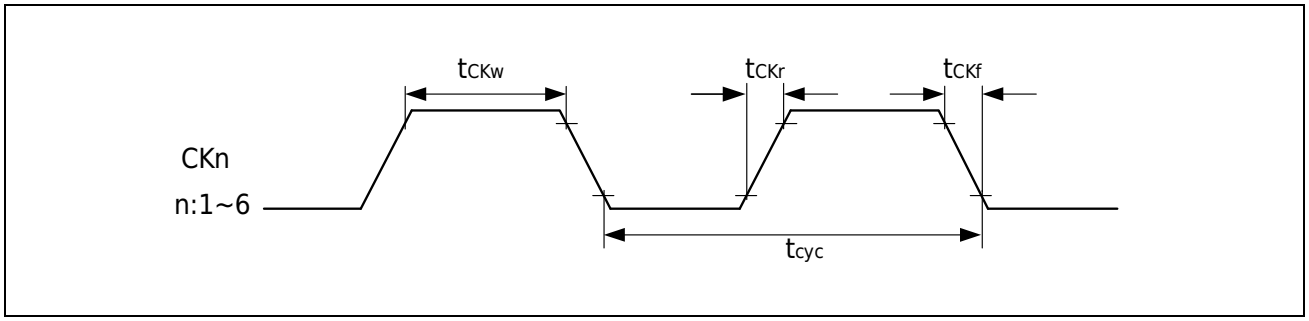


Figure 3-15 USART Clock Timing

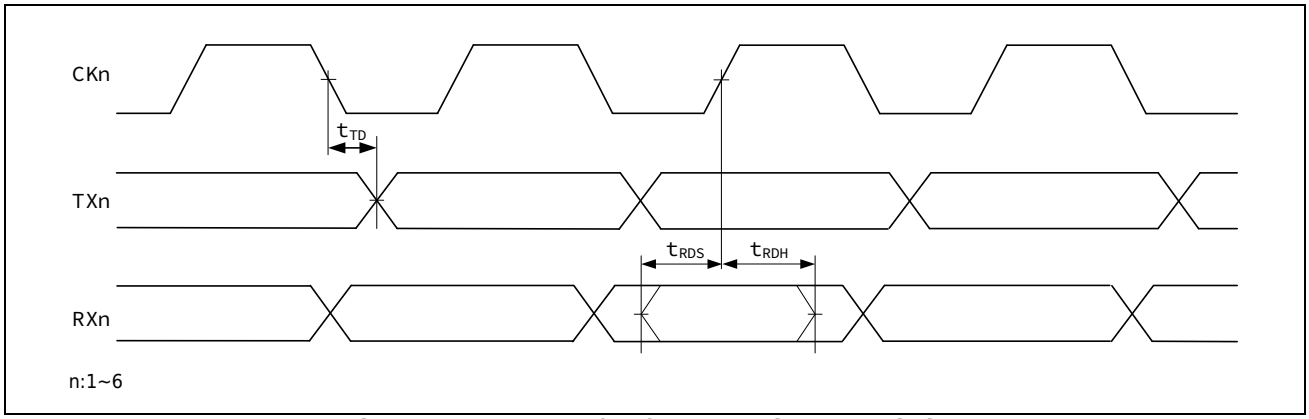


Figure 3-16 USART (CSI) Input and Output Timing

3.3.18 JTAG Interface Features

Table 3-39 JTAG Interface Features

Symbol	Item	Min	Typ	Max	Unit
t_{TCKcyc}	JTCK clock cycle time	50	-	-	ns
t_{TCKH}	JTCK clock high pulse width	15	-	-	ns
t_{TCKL}	JTCK clock low pulse width	15	-	-	ns
t_{TCKr}	JTCK clock rise time	-	-	5	ns
t_{TCKf}	JTCK clock fall time	-	-	5	ns
t_{TMSs}	JTMS setup time(1)	10	-	-	ns
t_{TMSh}	JTMS hold time(1)	10	-	-	ns
t_{TDIs}	JTDI setup time(1)	10	-	-	ns
t_{TDIh}	JTDI hold time(1)	10	-	-	ns
t_{TDOd}	JTDO data delay time(1)	10	-	25	ns

1. Guarantee of mass production test.

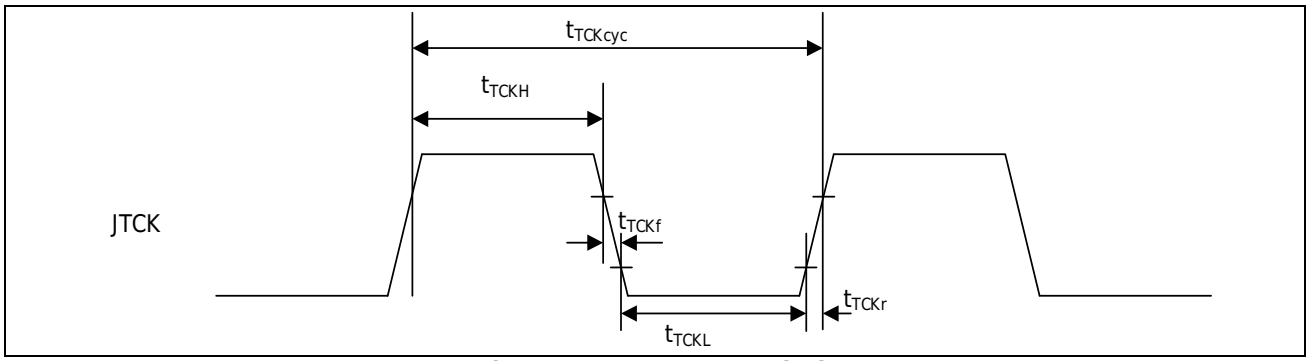


Figure 3-17 JTAG JTCK Clock

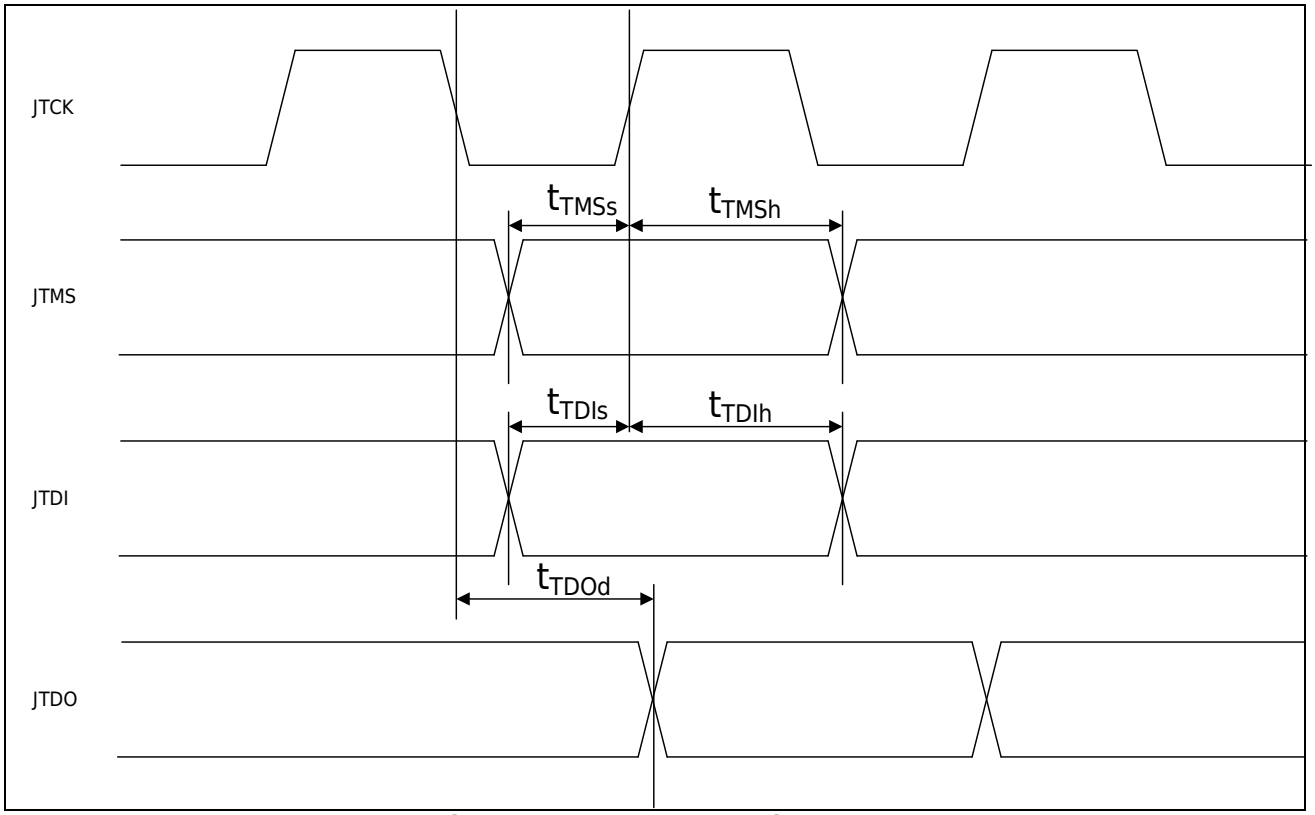


Figure 3-18 JTAG Input and Output

3.3.19 SWD Interface Features

Table 3-40 SWD Interface Features

Symbol	Item	Min	Typ	Max	Unit
$t_{SWCLKcyc}$	SWCLK clock cycle time	50	-	-	ns
t_{SWCLKH}	SWCLK clock high pulse width	15	-	-	ns
t_{SWCLKL}	SWCLK clock low pulse width	15	-	-	ns
t_{SWCLKr}	SWCLK clock rise time	-	-	5	ns
t_{SWCLKf}	SWLCK clock fall time	-	-	5	ns
t_{SWDIs}	SWDI setup time(1)	10	-	-	ns
t_{SWDIh}	SWDI hold time(1)	10	-	-	ns
t_{SWDOd}	SWDO data delay time(1)	2	-	25	ns

1. Guarantee of mass production test.

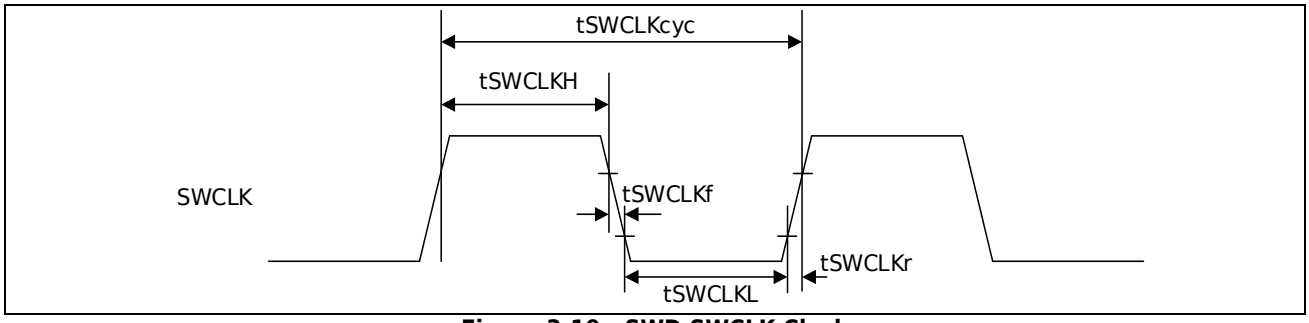


Figure 3-19 SWD SWCLK Clock

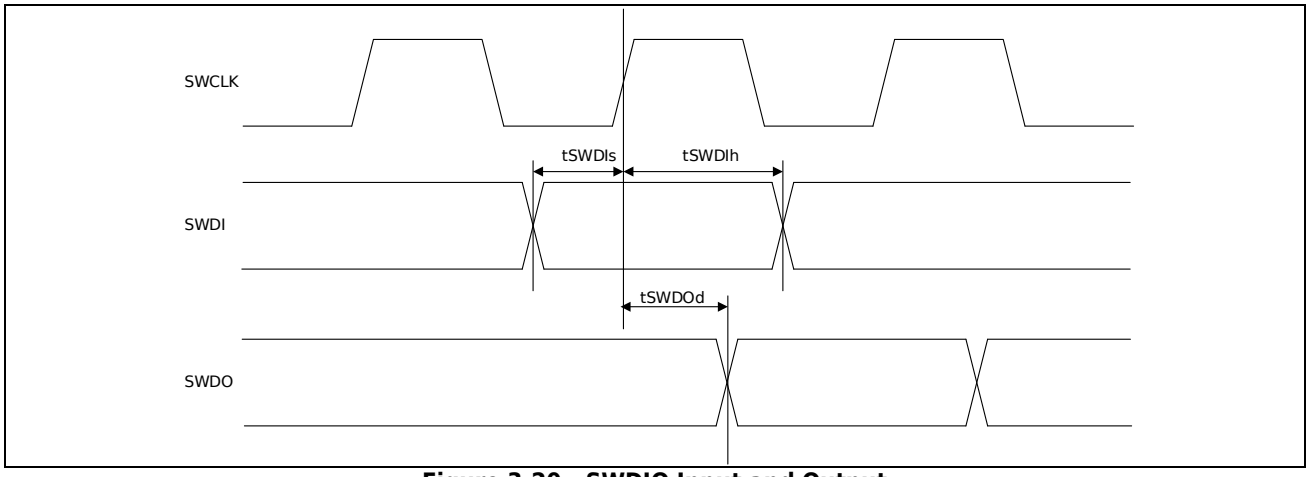


Figure 3-20 SWDIO Input and Output

3.3.20 TRACE Interface Features

Table 3-41 TRACE Interface Features

Symbol	Item	Min	Typ	Max	Unit
$t_{TRCLKcyc}$	TRACECK clock cycle time	20	-	-	ns
t_{TRCKH}	TRACECK clock high pulse width	7	-	-	ns
t_{TRCKL}	TRACECK clock low pulse width	7	-	-	ns
t_{TRCKr}	TRACECK clock rise time	-	-	2.5	ns
t_{TRCKf}	TRACECK clock fall time	-	-	2.5	ns
t_{TRDd}	TRACED[3:0] output delay time(1)	1.6	-	8.4	ns

1. Guarantee of mass production test.

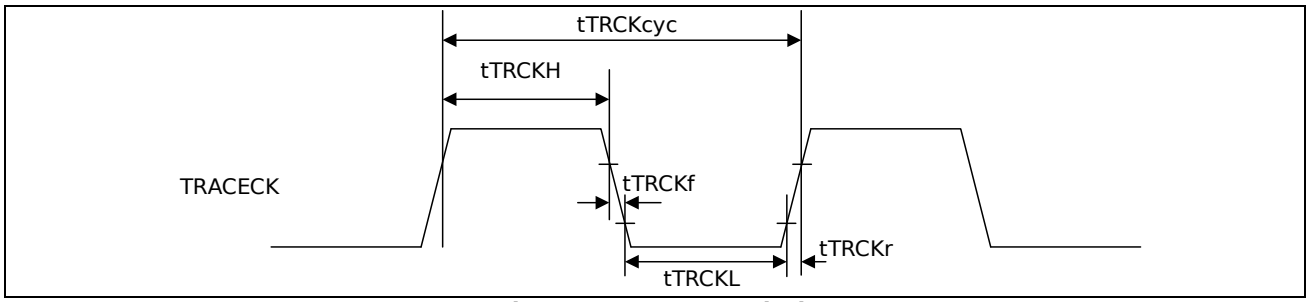


Figure 3-21 TRACE Clock

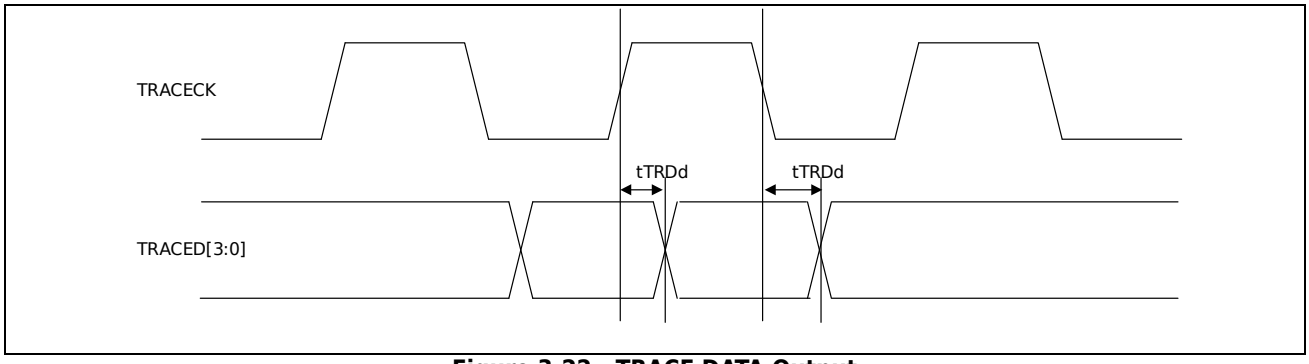


Figure 3-22 TRACE DATA Output

3.3.21 12-bit ADC Characteristic

Table 3-42 ADC Characteristics

Symbol	Parameter	Conditions	Min.	Typical Value	Max.	Unit
V_{AVCC}	Power supply	-	1.8	-	3.6	V
V_{REFH}	Positive reference voltage(1)	-	1.8	-	V_{AVCC}	V
V_{REFL}	Negative reference voltage	-	-	V_{AVSS}	-	V
f_{ADC}	ADC conversion clock speed	High-speed working mode V_{AVCC} = 2.4 ~ 3.6 V	1	-	60	MHz
		Low speed working mode V_{AVCC} = 1.8 ~ 2.4 V	1	-	30	
		Ultra-low speed working mode	1	-	8	
V_{AIN}	Conversion voltage range	-	V_{REFL}	-	V_{REFH}	V
R_{AIN}	External input impedance(2)	Refer to Formula 1 for details	-	-	50	kΩ
R_{ADC}	Sampling switch resistance(2)	-	-	3	6	kΩ
C_{ADC}	Internal sampling and retention capacitance(2)	-	-	4	7	pF
t_D	Trigger conversion delay(2)	f_{ADC} = 60 MHz	-	-	0.3	µs
t_S	Sampling time(2)	f_{ADC}=60 MHz	0.183	-	4.266	µs
			11	-	255	1/ f_{ADC}
t_{CONV}	Single channel total conversion time(2) (Including sampling time)	f_{ADC} = 60 MHz 12-bit resolution	0.4	-	-	µs
		f_{ADC} = 60 MHz 10-bit resolution	0.37	-	-	µs
		f_{ADC} = 60 MHz 8-bit resolution	0.34	-	-	µs
		20 to 268 (sampling time Ts + successive approximation n-bit resolution + 1)				1/ f_{ADC}
f_S	Sampling rate(2) f_{ADC} = 60 MHz	12-bit resolution single ADC	-	-	2.5	Msps
t_{ST}	Power-on time(2)	-	-	1	2	µs

1. $0 \le V_{AVCC} - V_{REFH} \le 1.2V$.
2. Design guaranteed.

Formula 1: RAIN Maximum Value Formula

$$R_{AIN} = \frac{k-1}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula (Formula 1) is used to determine the maximum external impedance to make the error lower than 1/4 LSB. Where N = 12 (12 bit resolution), k is the number of sampling cycles defined in the ADC _ SSTR register.

High-speed channel: PC0~3, PA0~3 .

Low-speed channel: channels other than high-speed channels.

Table 3-43 Input Channel Dynamic Accuracy@ f_{ADC}=60 MHz

Symbol	Parameter	Conditions	Typical Value	Max. Value	Unit
E_T	Total Unadjusted Error	f_{ADC}=60 MHz Input source impedance<1KΩ V_{REFH}=V_{AVCC}=2.4/ 3.6 V T_A =-40 ℃/ 105 ℃	±4.5	±6	LSB
E_O	Offset error		±3.5	±6	LSB
E_G	Gain error		±3.5	±6	LSB
E_D	Differential nonlinearity error		±1	±3	LSB
E_L	Integral nonlinearity error		±1.5	±4	LSB

Table 3-44 Input Channel Dynamic Accuracy@ f_{ADC}=30 MHz

Symbol	Parameter	Conditions	Typical Value	Max. Value	Unit
E_T	Total Unadjusted Error	f_{ADC}=30 MHz Input source impedance<1 KΩ V_{REFH}=V_{AVCC}=1.8 V T_A =-40 ℃/ 105 ℃	±4.5	±6	LSB
E_O	Offset error		±3.5	±6	LSB
E_G	Gain error		±3.5	±6	LSB
E_D	Differential nonlinearity error		±1	±3	LSB
E_L	Integral nonlinearity error		±1.5	±4	LSB

Table 3-45 Input Channel Dynamic Accuracy@ f_{ADC}=60 MHz

Symbol	Parameter	Conditions	Min.	Max.	Unit
ENOB	Effective Bits	f_{ADC}=60 MHz Input signal frequency = 2kHz Input source impedance = 0 Ω V_{REFH}=V_{AVCC}=2.4/ 3.6 V T_A =-40 ℃/ 105 ℃	10.5	-	Bits
SINAD	Signal-to-Noise Harmonic Ratio		64.3	-	dB
SNR	Signal-to-Noise Ratio		64.4	-	dB
THD	Total Harmonic Distortion		-	-78.1	dB

Table 3-46 Input Channel Dynamic Accuracy@ f_{ADC}=30 MHz

Symbol	Parameter	Conditions	Min.	Max.	Unit
ENOB	Effective Bits	f_{ADC}=30 MHz Input signal frequency = 2kHz Input source impedance = 0 Ω V_{REFH}=V_{AVCC}=1.8 V T_A =-40 ℃/ 105 ℃	10.6	-	Bits
SINAD	Signal-to-Noise Harmonic Ratio		67.0	-	dB
SNR	Signal-to-Noise Ratio		67.1	-	dB
THD	Total Harmonic Distortion		-	-75.1	dB

Table 3-47 Input Channel Dynamic Accuracy@ f_{ADC}=60 MHz

Symbol	Parameter	Conditions	Typical Value	Max. Value	Unit
E_T	Total Unadjusted Error	f_{ADC}=60 MHz Input source impedance<1 KΩ V_{REFH}=V_{AVCC}=2.4/ 3.6 V T_A =-40 ℃/ 105 ℃	±5.5	±7	LSB
E_O	Offset error		±4.5	±7	LSB
E_G	Gain error		±4.5	±7	LSB
E_D	Differential nonlinearity error		±1.5	±3	LSB
E_L	Integral nonlinearity error		±2.0	±4	LSB

Table 3-48 Input Channel Dynamic Accuracy @ f_{ADC}=30 MHz

Symbol	Parameter	Conditions	Typical Value	Max. Value	Unit
E_T	Total Unadjusted Error	f_{ADC}=30 MHz Input source impedance <1 KΩ V_{REFH}=V_{AVCC}=1.8 V T_A =-40 ℃/ 105 ℃	±5.5	±7	LSB
E_O	Offset error		±4.5	±7	LSB
E_G	Gain error		±4.5	±7	LSB
E_D	Differential nonlinearity error		±1.5	±3	LSB
E_L	Integral nonlinearity error		±2.0	±4	LSB

Table 3-49 Low Speed Input Channel Dynamic Accuracy@ f_{ADC}=60 MHz

Symbol	Parameter	Conditions	Min.	Max.	Unit
ENOB	Effective Bits	f_{ADC}=60 MHz Input signal frequency = 2kHz Input source impedance = 0 Ω V_{REFH}=V_{AVCC}=2.4/ 3.6 V T_A =-40 ℃/ 105 ℃	10.5	-	Bits
SINAD	Signal-to-Noise harmonic ratio		64.4	-	dB
SNR	Signal-to-Noise ratio		64.4	-	dB
THD	Total Harmonic Distortion		-	-80.3	dB

Table 3-50 Low Speed Input Channel Dynamic Accuracy@ f_{ADC}=30 MHz

Symbol	Parameter	Conditions	Min.	Max.	Unit
ENOB	Effective Bits	f_{ADC}=30 MHz Input signal frequency = 2kHz Input source impedance = 0 Ω V_{REFH}=V_{AVCC}=1.8 V T_A =-40 ℃/ 105 ℃	10.6	-	Bits
SINAD	Signal-to-noise harmonic ratio		66.6	-	dB
SNR	Signal-to-noise ratio		66.8	-	dB
THD	Total Harmonic Distortion		-	-79.4	dB

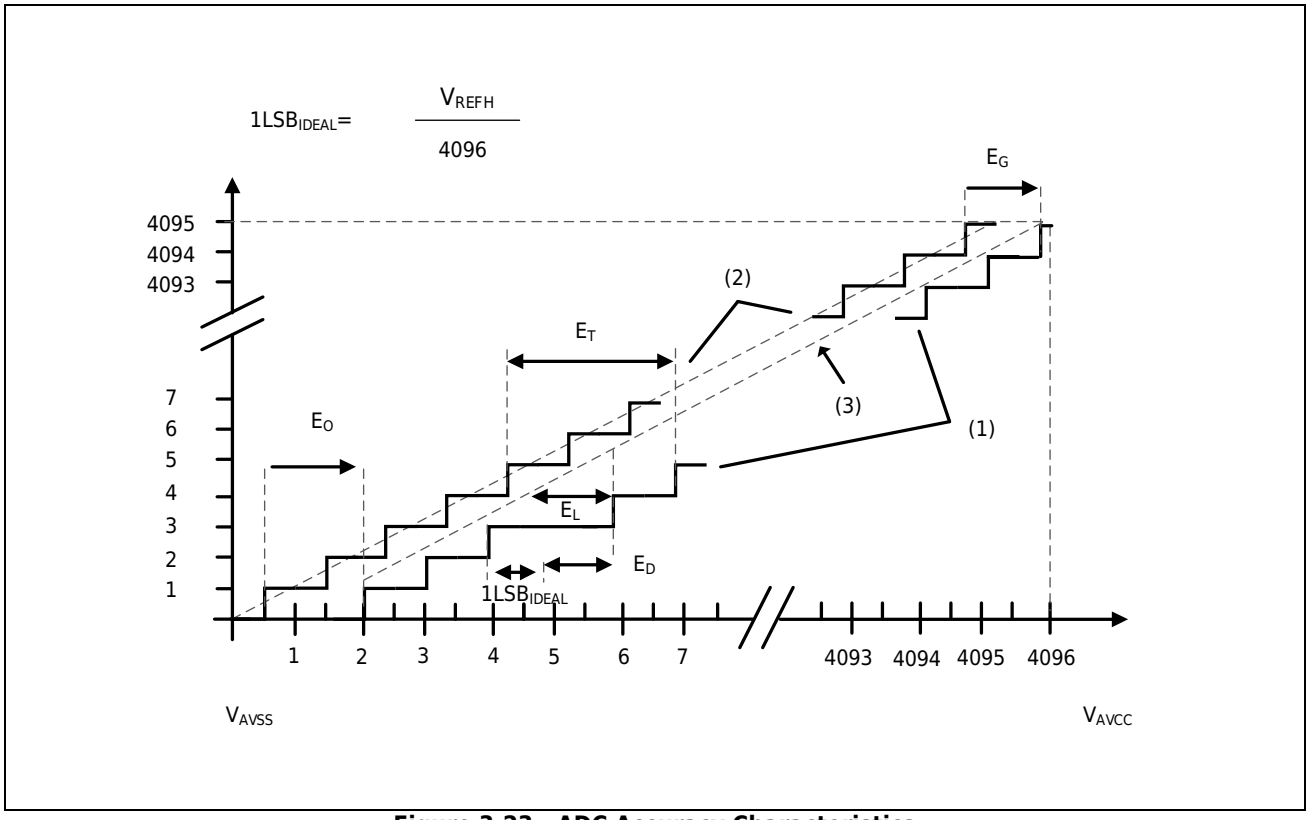


Figure 3-23 ADC Accuracy Characteristics

1. Examples of actual transmission curves.
2. Ideal transfer curve.
3. End point correlation line.

E_T = Total Unadjusted Error: The maximum deviation between the actual and ideal transfer curve.

E_O = Offset Error: The deviation between the first actual transition and the first ideal transition.

E_G = Gain Error: The deviation between the last ideal transition and the last actual transition.

E_D = Differential nonlinearity error: The maximum deviation between the actual step and the ideal value.

E_L = Integral Nonlinearity Error: The maximum deviation between any actual transition and the endpoint correlation line.

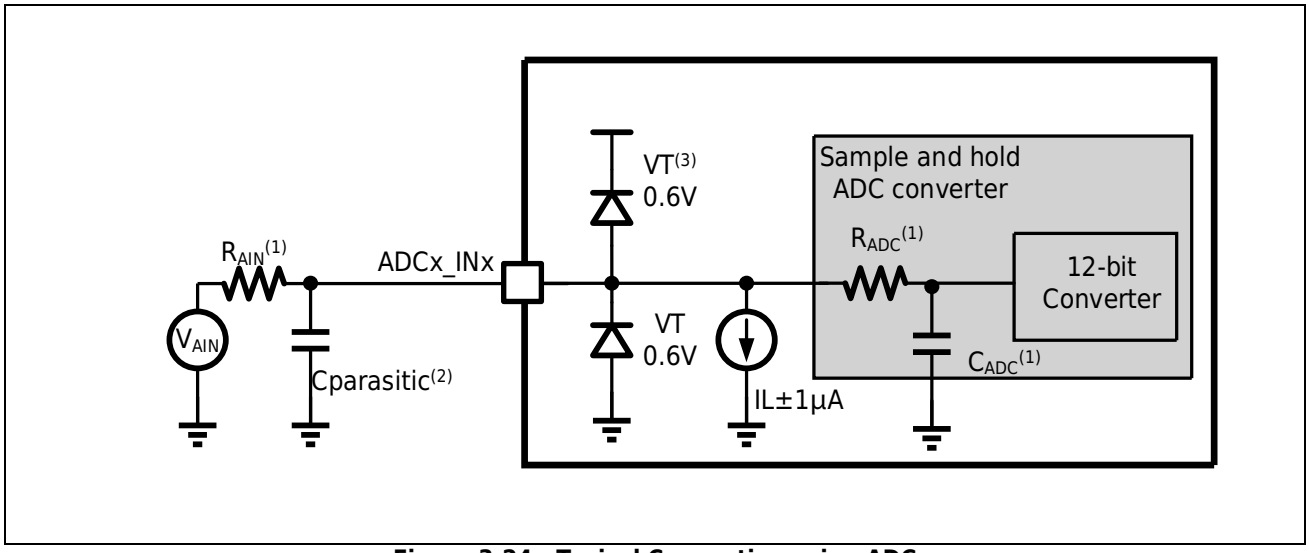


Figure 3-24 Typical Connection using ADC

1. For information on R_{AIN}, R_{ADC}, and C_{ADC} values, refer to Table 3-42.
2. Cparasitic represents PCB capacitance (depending on welding and PCB wiring quality) and pad capacitance (approximately 5 pF). Higher values of Cparasitic result in less accurate conversions. To solve this problem, f_{ADC} should be reduced.
3. The ADC channels of the PA4~PA7, PC4, PC5, and PB15 pins have this diode.

Universal PCB Design Guidelines

The power supply should be decoupled as shown in the following figure. The 0.1 μF capacitor should be a (good quality) ceramic capacitor. These capacitors should be placed as close to the chip as possible.

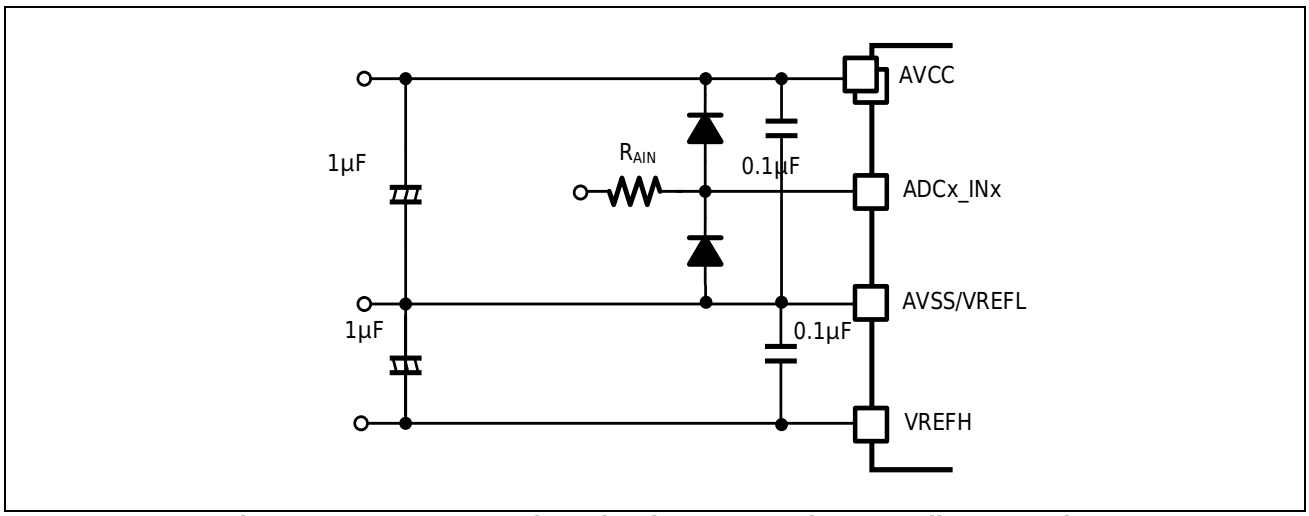


Figure 3-25 Power Supply and Reference Supply Decoupling Example

3.3.22 12-bit DAC Characteristic

Table 3-51 2-Bit DAC Port Output Enable Characteristics

Symbol	Parameter	Conditions	Min.	Typical Value	Max. Value	Unit
V_{AVCC}	Analog power voltage	-	1.8	3.3	3.6	V
V_{REFH}	Reference power supply voltage	-	1.8	3.3	V_{AVCC}	V
AO	Output voltage range(1)	-	0	-	V_{REFH} -1LSB	V
CL	Load Capacitance	-	-	-	20	pF
RO	Output resistance(2)	-	-	8	-	KΩ
DNL	Differential nonlinearity error (deviation between two consecutive codes -1LSB)(1)	-	-	-	±2	LSB
INL	Integral nonlinearity error (the difference between the value measured at code I and the value at code I on the line between code 0 and the last code 4095) (1)	-	-	-	±4	LSB
TUE	Total unadjusted error	-	-	-	±24	LSB
T_{st}	Settling Time (Applies to 12- bit input code transition between lowest input code and highest input code until DAC output reaches ±4LSB of final value, CL = 20 pF)	-	-	-	4	μs
Iavcc	Analog supply current (quiescent current)	-	-	-	2	μA
Irefh	Reference supply current (quiescent current)	-	-	-	250	μA

1. Guarantee of mass production test.
2. Design guaranteed.

Table 3-52 12-Bit DAC Port Output Disabled Characteristics

Symbol	Parameter	Conditions	Min.	Typical Value	Max.	Unit
V_{AVCC}	Analog power voltage	-	1.8	3.3	3.6	V
V_{REFH}	Reference power supply voltage	-	1.8	3.3	V_{AVCC}	V
AO	Output voltage range(1)	-	0	-	V_{REFH} -1LSB	-
DNL	Differential nonlinearity error (deviation between two consecutive codes -1LSB)(1)	-	-	-	±2	LSB
TUE	Total Unadjusted Error(1)	-	-	-	±5	LSB
T_{st}	Settling Time (Applies to 12 -bit input code transition between lowest input code and highest input code until DAC output reaches ±1 LSB of final value, V_{REFH}≥2.7) (DAC output to 2 comparators)(1)	-	-	-	230	ns
	Settling Time (Applies to 12 -bit input code transition between lowest input code and highest input code until DAC output reaches ±32 LSB of final value, V_{REFH}≥2.7) (DAC output to 2 comparators)(1)	-	-	-	135	ns
	Settling Time (Applies to 12 -bit input code transition between lowest input code and highest input code until DAC output reaches ±1 LSB of final value, V_{REFH} <2.7) (DAC output to 2 comparators)(1)	-	-	-	240	ns
	Settling Time (Applies to 12 -bit input code transition between lowest input code and highest input code until DAC output reaches ±32 LSB of final value, V_{REFH} <2.7) (DAC output to 2 comparators)(1)	-	-	-	145	ns
Iavcc	Analog supply current (quiescent current)	-	-	0.1	2	μA
Irefh	Reference supply current (quiescent current)	-	-	146	250	μA

1. Design guaranteed.

3.3.23 Temperature Sensor

Table 3-53 Temperature Sensor Characteristics

Symbol	Parameter	Conditions	Min.	Typical Value	Max.	Unit
T_L	Temperature linearity	-	-2	-	+2	℃
T_E	Absolute accuracy(1)	T_A 25 ℃, 105 ℃ Two-point calibration	-2	-	+2	℃

1. The actual characteristics are related to the accuracy of the calibration point temperature. If the chip preset data calibration is used, the characteristics are not guaranteed due to the temperature difference in the mass production test environment.

3.3.24 Comparator Characteristics

Table 3-54 Comparator Characteristics

Symbol	Parameter	Conditions	Min.	Typical Value	Max.	Unit
V_{AVCC}	Analog power voltage	-	1.8	3.3	3.6	V
V_I	Input voltage range	-	0	-	V_{AVCC}	V
T_{cmp}	Comparing Time(1)	Step=200 mV with overdrive 100 mV Input Slew Rate ≥ 4mV/ns	-	-	60	ns
T_{set}	Input channel switching settling time	-	-	100	200	ns
V_{hyst}	Hysteresis voltage	HYST[2:0]=0b000	-	0	-	mV
		HYST[2:0]=0b001	-	10	-	mV
		HYST[2:0]=0b010	-	20	-	mV
		HYST[2:0]=0b011	-	30	-	mV
		HYST[2:0]=0b100	-	40	-	mV
		HYST[2:0]=0b101	-	50	-	mV
		HYST[2:0]=0b110	-	60	-	mV
		HYST[2:0]=0b111	-	70	-	mV
V_{offset}	Comparator input offset voltage	-	-15	-	+15	mV

1. The performance test calculation method is to input voltage from the CMP input pin and output the comparison result from the CMP output pin.

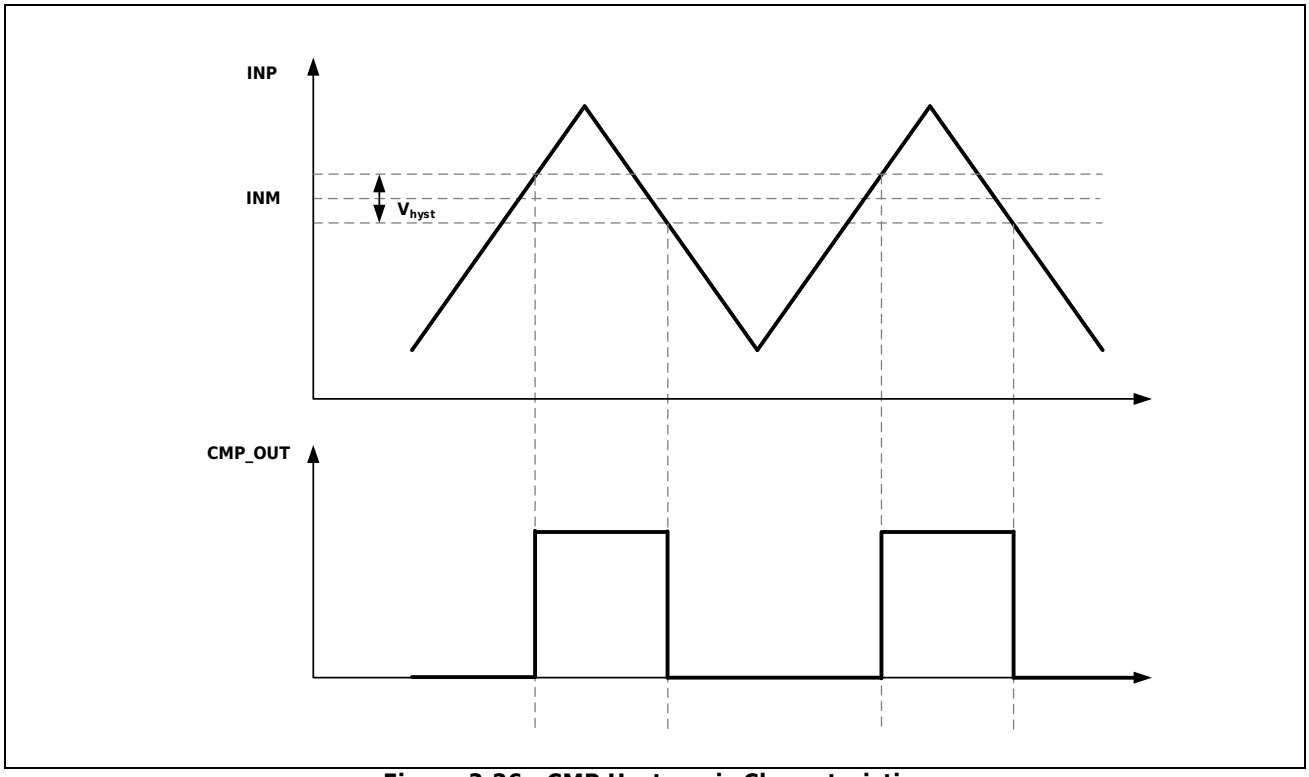


Figure 3-26 CMP Hysteresis Characteristics

3.3.25 EXMC Characteristic

Table 3-55 EXMC Characteristics In 55 Internal EXCLK Mode

Symbol	Parameter	Min	Typ	Max	Unit
t_add_d	Address line output delay time (2.7 V ~ 3.6 V)(1)	-	-	12	ns
	Address line output delay time (1.8 V~2.7 V)	-	-	18	ns
t_data_d	Data line output delay time (2.7 V~3.6 V)(1)	-	-	12	ns
	Data line output delay time (1.8 V~2.7 V)	-	-	18	ns
t_ce_d	CE output delay time (2.7 V~3.6 V) (1)	-	-	9	ns
	CE output delay time (1.8 V ~ 2.7 V)	-	-	12	ns
t_we_d	WE output delay time (2.7 V~3.6 V) (1)	-	-	9	ns
	WE output delay time (1.8 V ~ 2.7 V)	-	-	12	ns
t_oe_d	OE output delay time (2.7 V~3.6 V) (1)	-	-	9	ns
	OE output delay time (1.8 V ~ 2.7 V)	-	-	12	ns
t_baa_d	BAA output delay time (2.7 V~3.6 V) (1)	-	-	9	ns
	BAA output delay time (1.8 V ~ 2.7 V)	-	-	12	ns
t_adv_d	ADV output delay time (2.7 V~3.6 V) (1)	-	-	9	ns
	ADV output delay time (1.8 V ~ 2.7 V)	-	-	12	ns
t_ale_d	ALE output delay time (2.7 V~3.6 V) (1)	-	-	9	ns
	ALE output delay time (1.8 V ~ 2.7 V)	-	-	12	ns
t_data_s	Data line input Setup time (2.7 V~3.6 V)(1)	24	-	-	ns
	Data line input Setup time (1.8 V~2.7 V)	28	-	-	ns
t_data_h	Data line input hold time(1)	0	-	-	ns
t_rb_s	RB input setup time (2.7 V~3.6 V)(1)	24	-	-	ns
	RB input setup time (1.8 V~2.7 V)	28	-	-	ns
t_rb_h	RB input hold time(1)	0	-	-	ns

1. Guarantee of mass production test.

Table 3-56 EXMC Characteristics In 56- Feedback EXCLK Mode

Symbol	Parameter	Min	Typ	Max	Unit
t_add_d	Address line output delay time (2.7 V ~ 3.6 V)(1)	-	-	12	ns
	Address line output delay time (1.8 V~2.7 V)	-	-	18	ns
t_data_d	Data line output delay time (2.7 V~3.6 V)(1)	-	-	12	ns
	Data line output delay time (1.8 V~2.7 V)	-	-	18	ns
t_ce_d	CE output delay time (2.7 V~3.6 V) (1)	-	-	9	ns
	CE output delay time (1.8 V ~ 2.7 V)	-	-	12	ns
t_we_d	WE output delay time (2.7 V~3.6 V) (1)	-	-	9	ns
	WE output delay time (1.8 V ~ 2.7 V)	-	-	12	ns
t_oe_d	OE output delay time (2.7 V~3.6 V) (1)	-	-	9	ns
	OE output delay time (1.8 V ~ 2.7 V)	-	-	12	ns
t_baa_d	BAA output delay time (2.7 V~3.6 V) (1)	-	-	9	ns
	BAA output delay time (1.8 V ~ 2.7 V)	-	-	12	ns
t_adv_d	ADV output delay time (2.7 V~3.6 V) (1)	-	-	9	ns
	ADV output delay time (1.8 V ~ 2.7 V)	-	-	12	ns
t_ale_d	ALE output delay time (2.7 V~3.6 V) (1)	-	-	9	ns
	ALE output delay time (1.8 V ~ 2.7 V)	-	-	12	ns
t_data_s	Data line input Setup time (2.7 V~3.6 V)(1)	7	-	-	ns
	Data line input Setup time (1.8 V~2.7 V)	7	-	-	ns
t_data_h	Data line input Hold time (2.7 V~3.6 V)(1)	5	-	-	ns
	Data line input Hold time (1.8 V~2.7 V)	14	-	-	ns
t_rb_s	RB input setup time (2.7 V~3.6 V)(1)	7	-	-	ns
	RB input setup time (1.8 V~2.7 V)	7	-	-	ns
t_rb_h	Data line input Hold time (2.7 V~3.6 V)(1)	5	-	-	ns
	Data line input Hold time (1.8 V~2.7 V)	14	-	-	ns

1. Guarantee of mass production test.

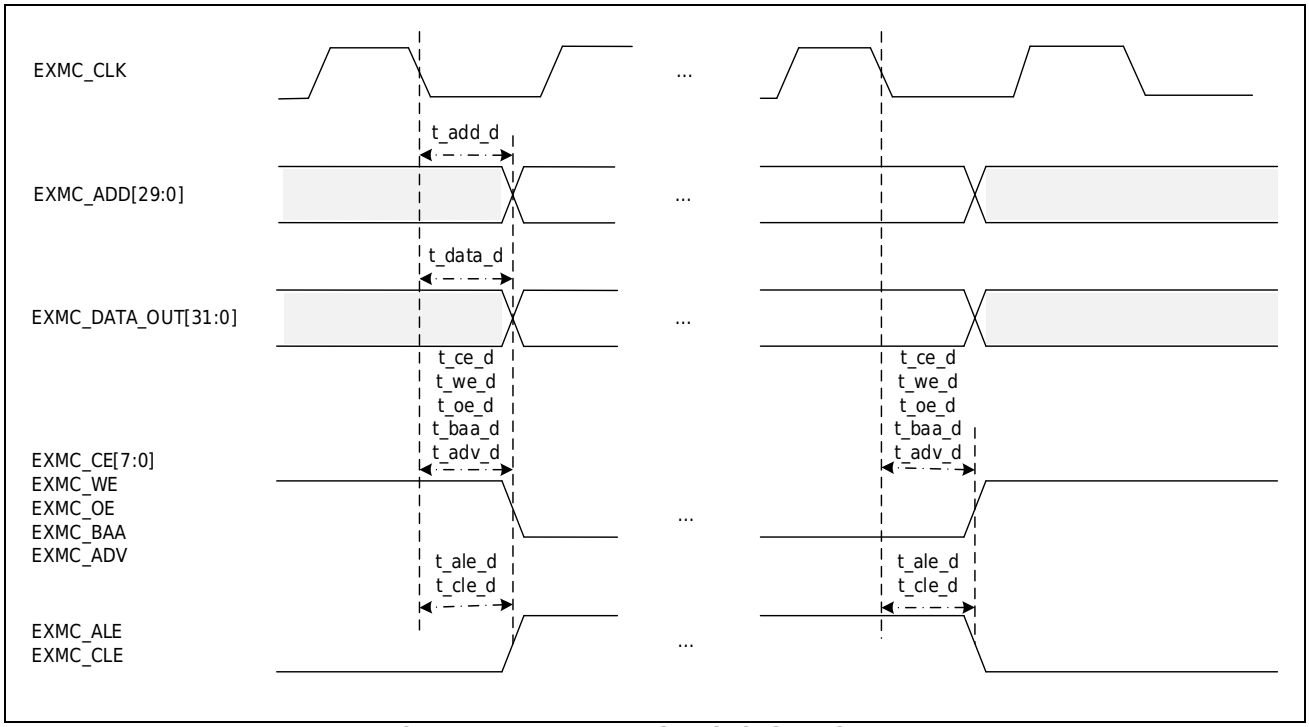


Figure 3-27 Output Signal Timing Diagram

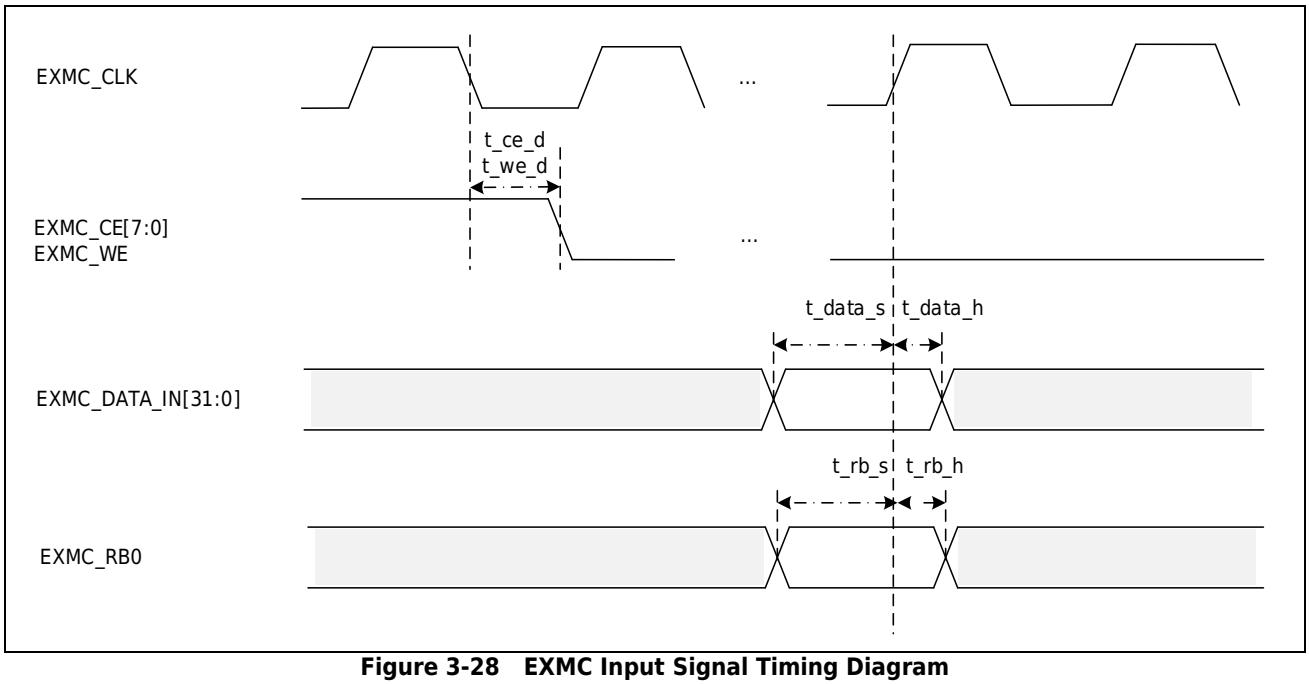


Figure 3-28 EXMC Input Signal Timing Diagram

3.3.26 Gain Adjustable Amplifier Characteristics

Table 3-57 Gain Adjustable Amplifier Characteristics

Symbol	Parameter		Conditions	Min.	Typical Value	Max.	Unit
V_{AVCC}	Analog power voltage		-	1.8	3.3	3.6	V
V_{OS}	Input offset voltage		-	-8	-	8	mV
V_I	Input voltage range		-	0.1*V_{AVCC}/ Gain	-	0.9*V_{AVCC}/ Gain	V
G_E	Gain error	Use the internal analog ground AVSS as the PGA negative input	Gain=2	-2	-	2	%
			Gain=2.133	-2	-	2	%
			Gain=2.286	-2	-	2	%
			Gain=2.667	-2	-	2	%
			Gain=2.909	-2	-	2	%
			Gain=3.2	-2.5	-	2.5	%
			Gain=3.556	-2.5	-	2.5	%
			Gain=4.0	-2.5	-	2.5	%
			Gain=4.571	-3.0	-	3.0	%
			Gain=5.333	-3.0	-	3.0	%
			Gain=6.4	-4.0	-	4.0	%
			Gain=8	-4.0	-	4.0	%
			Gain=10.667	-5.0	-	5.0	%
			Gain=16	-5.0	-	5.0	%
			Gain=32	-8.0	-	8.0	%

3.3.27 EIRQ Filter Characteristics

Table 3-58 EIRQ Filter Characteristics

Symbol	Parameter	Conditions	Min.	Typical Value	Max.	Unit
W_{F_EIRQ}	EIRQ Input Filter Width	INTC_NOCCR.NOCSEL = 0b00	0.4	-	1.2	μs
		INTC_NOCCR.NOCSEL = 0b01	0.8	-	2.3	μs
		INTC_NOCCR.NOCSEL = 0b10	1.7	-	4.5	μs
		INTC_NOCCR.NOCSEL = 0b11	3.4	-	8.9	μs

3.3.28 USART1 RX Filter Characteristics in STOP Mode

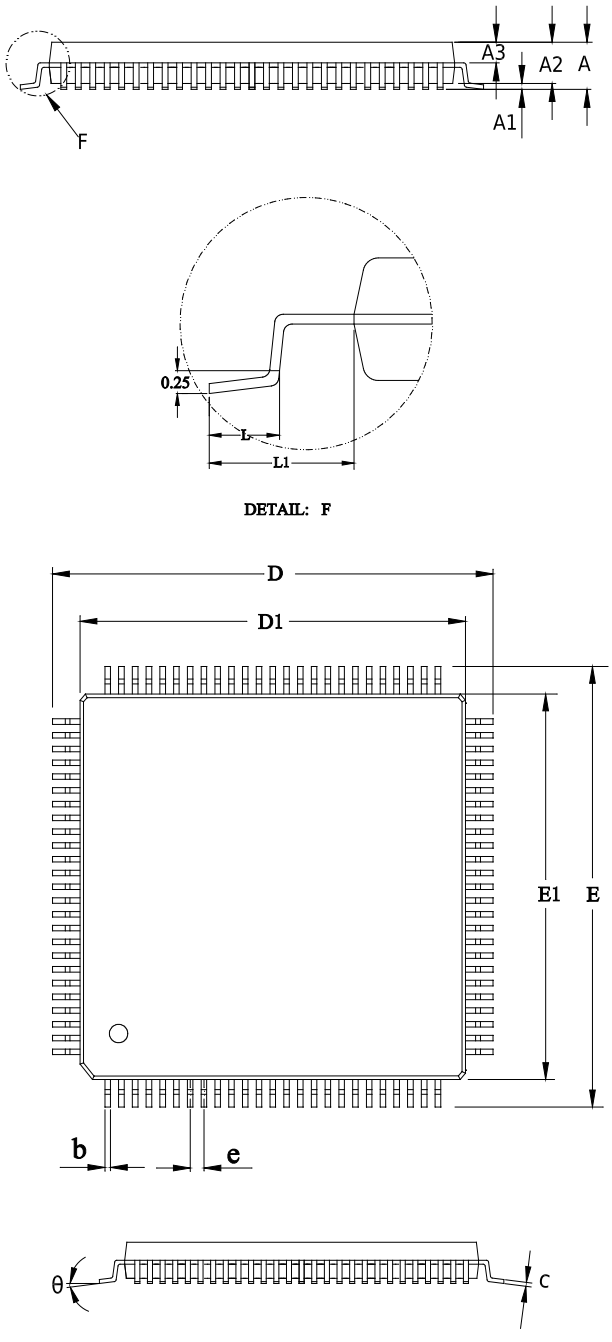
Table 3-59 USART1 RX Filter Characteristics In STOP Mode

Symbol	Parameter	Conditions	Min.	Typical Value	Max.	Unit
WF_USART1	USART1 input filter width	USART1_NFC.USART1_NFS = 0b00	0.4	-	1.2	μs
		USART1_NFC.USART1_NFS = 0b01	0.8	-	2.3	μs
		USART1_NFC.USART1_NFS = 0b10	1.7	-	4.5	μs
		USART1_NFC.USART1_NFS = 0b11	3.4	-	8.9	μs

4 Packaging Information

4.1 Packaging Size

LQFP100 package

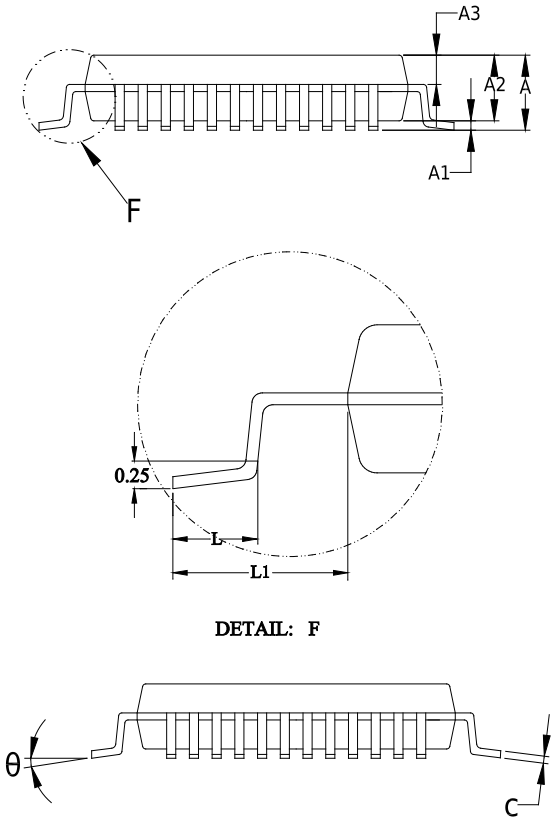


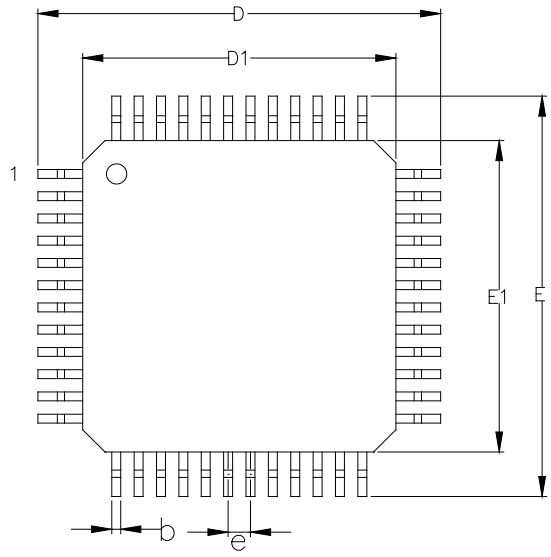
Symbol	14x14 Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	-	0.27
c	0.09	0.15	0.20
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	0.50BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	3.5°	7°

NOTE:

– *Dimensions “D1” and “E1” do not include mold flash.*

LQFP48 Package





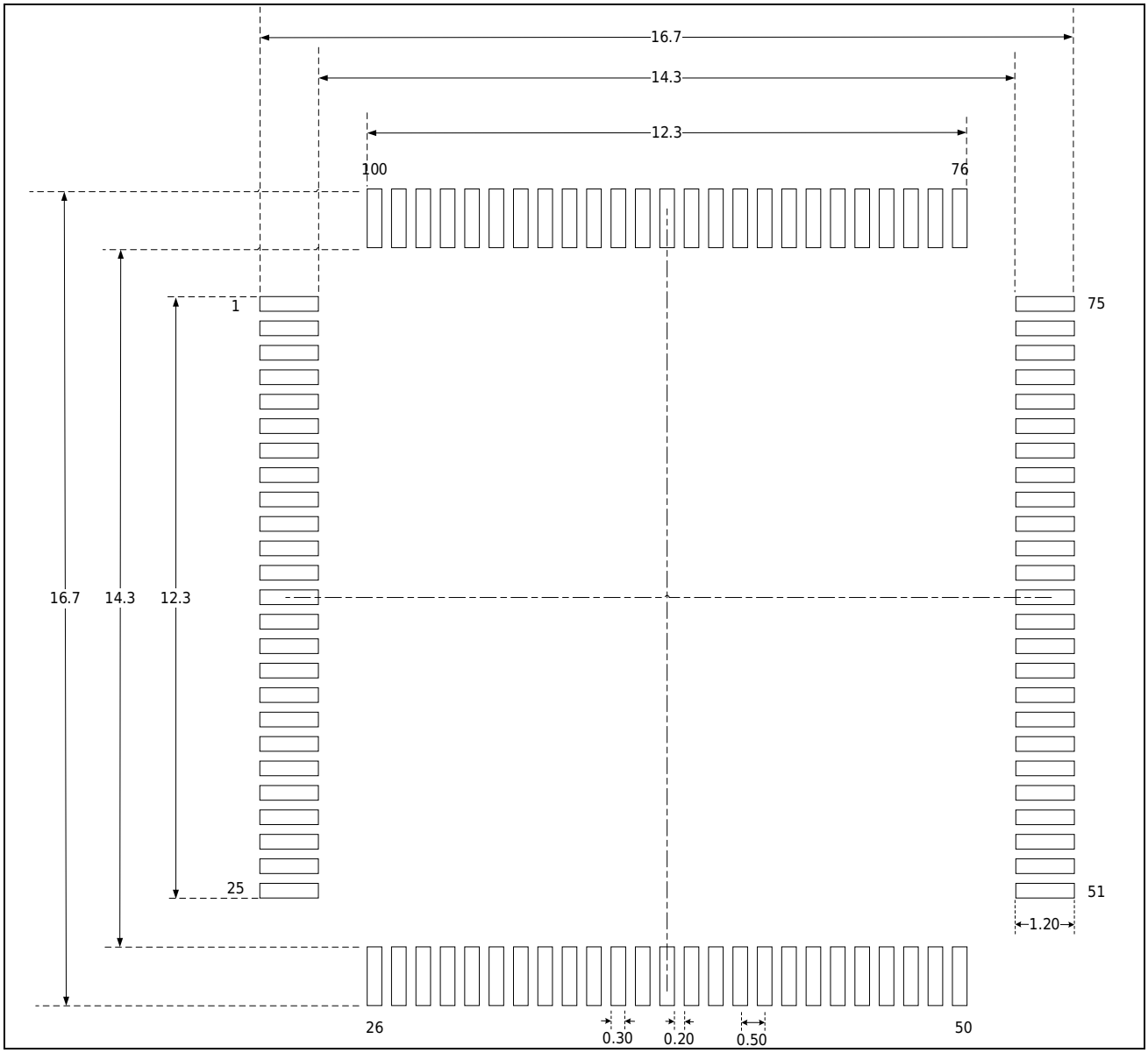
Symbol	7x7 Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	-	0.27
c	0.09	0.15	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	3.5°	7°

NOTE:

– *Dimensions "D1" and "E1" do not include mold flash.*

4.2 Schematic Diagram of Pad

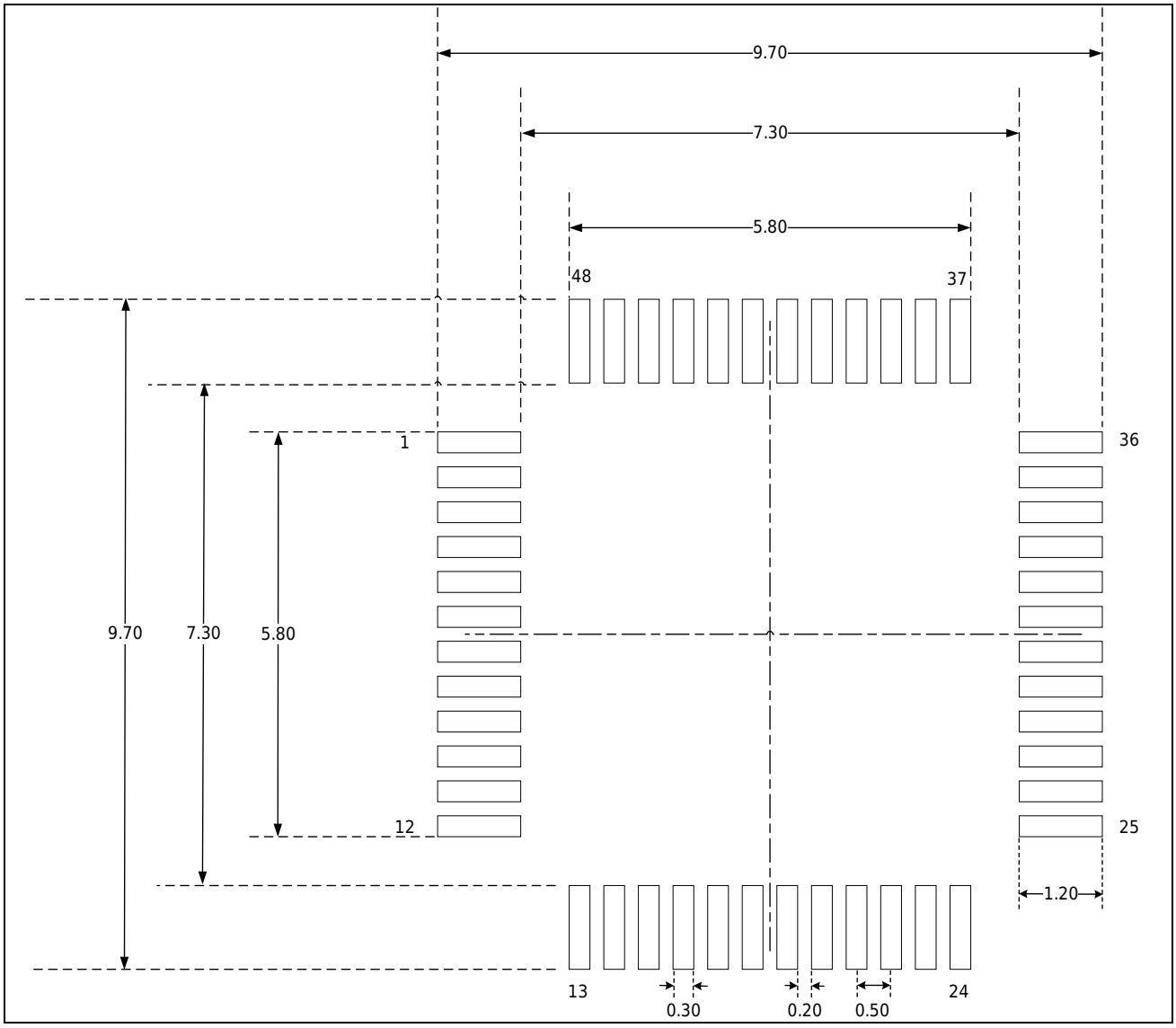
LQFP100 Packaging (14mm x 14mm)



NOTE:

– *Dimensions are expressed in millimeters.*

LQFP48 Packaging (7mm x 7mm)



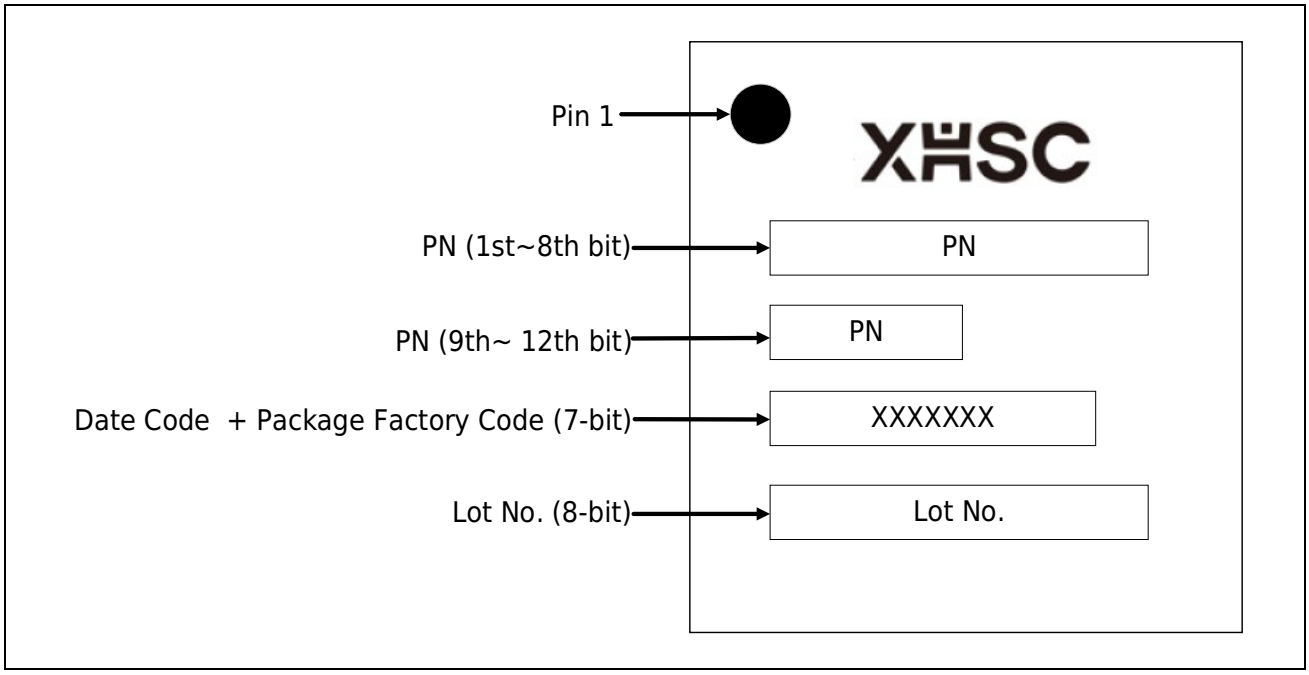
NOTE:

– *Dimensions are expressed in millimeters.*

4.3 Silkscreen Instructions

The position and information of Pin 1 printed on the front of each package are given below.

LQFP100 packaging (14mm x 14mm)/LQFP48 packaging (7mm x 7mm)



4.4 Packaging Thermal Resistance Coefficient

When the packaged chip is working at the specified working environment temperature, the junction temperature T_J (℃) of the chip surface can be calculated according to the following formula:

$$T_J = T_A + (P_D \times \theta_{JA})$$

- T_A refers to the working environment temperature when the packaged chip is working, the unit is ℃;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is ℃/W;
- P_D is equal to the sum of internal power consumption of the chip and I/O power consumption, and the unit is W. The internal power consumption of the chip is the product's I_{DD} x V_{DD}.I/O power consumption refers to the power consumption generated by the I/O pins when the chip is working. Usually this part of the value is very small and can be ignored.

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable junction temperature T_J of the chip.

Table 4-1 Thermal Resistance Coefficient Reference Value of Each Package

Package Type and Size	Thermal Resistance Junction-ambient Value (θ_{JA})	Unit
LQFP100 14 mm x 14 mm/ 0.5 mm pitch	56 +/- 10 %	℃/W
LQFP48 7 mm x 7 mm/ 0.5 mm pitch	57 +/- 10 %	℃/W

5 Ordering Information

Product Model		HC32A472JETI -LQ48	HC32A472PETI -LQFP100
Main Frequency (MHz)		120	
Core		M4	
Flash(KB)		512	
OTP(KB)		134	
RAM(KB)		68	
GPIO		39	85
Voltage (V)		1.8 ~ 3.6	
DMA		2unit * 8ch	
Timing and Counting	Timer	23	
	WDT	1ch	
	SWDT	1ch	
	RTC	1ch	
Communication Interface	UART	6	
	MDIO	1ch	
	I²C	3	
	SPI	4	
	QSPI	1	
	USB_FS	1ch	
	CAN-FD	3ch	
	EXMC	-	✓
Simulation	ADC 12bit	3unit, 21ch	3unit, 27ch
	DAC 12bit	2ch	
	PGA	2ch	
	OTS	✓	
	CMP	2ch	
	PVD	✓	
Co-processing	FMAC	✓	
	DCU	✓	
	MAU	✓	
Safety	AES	AES256	
	TRNG	1	
	Hash	SHA256	
Working Temperature (℃)		-40~105	-40~105
Encapsulation and Packaging	Encapsulation Form	LQFP48 (7*7)	LQFP100 (14*14)
	Packaging Form	TRAY	TRAY

Before ordering, please contact the sales window for the latest mass production information.

Version Revision History

Version Number	Revision Date	Modified Content
Rev1.00	2025/02/18	First edition release.
Rev1.01	2025/12/18	3.3.1 General Working Conditions: Note (5) was modified to " It is prohibited for such pins to be directly connected to power sources or ground other than those of this chip. It is recommended to pull it up to the power supply or down to the ground through a resistor of 1KΩ or above."