XIAOHUA SEMICONDUCTOR

HC32A4A8 Series

32-bit ARM® Cortex®-M4 Microcontroller

Datasheet

Rev1.00

July 2025

Feature List

ARM Cortex-M4 32-bit MCU+FPU, 300DMIPS, 2MB Flash, 516KB SRAM, 2USBs (HS/FS OTG), Ethernet MAC, 4CANs(FD/2.0B), 2SDIOs, DVP, EXMC, 35Timers, 3ADCs, 4DACs, 4PGAs, 4CMPs, 10USARTs, 6SPIs, 6I2Cs, 4I2Ss, QSPI, PKE, SKE, HASH(SHA256/HMAC), FMAC(FIR), MAU, ERMU, HSM

- ARMv7-M Architecture 32-bit Cortex-M4 CPU, integrated FPU, MPU, DSP with SIMD instructions, full instruction trace unit ETM, and CoreSight standard debug unit. Maximum operating frequency 240MHz (achieves 300 DMIPS or 825 Coremarks)
- Built-in memory
  - Maximum 2048KByte dual bank Flash memory with ECC checking
  - Maximum 516KByte SRAM, including 128KByte single-period access high-speed RAM with ECC checking
- Power, Clock, Reset management
  - System power (V_{CC}): 1.8-3.63V
  - 6 independent clock sources: XTAL (4-25MHz), XTAL32 (32.768kHz), HRC (16/20MHz), MRC (8MHz), LRC (32.768kHz), SWDTLRC (10kHz)
  - 16 reset sources including POR, PVD1R/PVD2R, and NRST, each with an independent flag bit
- Low power operation
  - Peripheral functions can be independently enabled or disabled
  - 3 low power consumption modes: Sleep mode, Stop mode, Power-down mode
  - VBAT independent power supply for ultra-low-power RTC, 128Byte backup register, 4KByte backup SRAM
- Peripheral operation support system significantly reduces CPU processing load
  - 16-channel dual-host DMAC
  - USBHS, USBFS, Ethernet MAC dedicated DMAC
  - 8 data computing units (DCU)
  - Math coprocessor unit (MAU), supports Sin/Sqrt
  - Support 16-order FIR digital filter (FMAC)
  - Supports peripheral event mutual triggering (AOS)
- High-performance simulation
  - 3 independent 12-bit 2.5Msps ADC
  - 3 simultaneous sample-and-hold circuits for 3-channel simultaneous sampling
  - 4 independent 12-bit 15Msps DAC
  - 4 programmable gain amplifier (PGA)
  - 4 independent voltage comparator (CMP)
  - 1 on-chip temperature sensor (OTS)
- Timer
  - 8 multifunctional 32/16-bit PWM Timer (Timer6)
  - 3 16-bit motor PWM Timer (Timer4)
  - 12 16-bit general Timer (TimerA)
  - 4 16-bit general-purpose Timer (Timer2)
  - 5 16-bit basic Timer (Timer0)
  - Real-time Clock Timer (RTC)
  - 2 WDTs supporting internal dedicated clock
- Maximum 142 GPIOs
  - Maximum 138 5V-tolerant IOs
- Maximum 36 communication interfaces
  - 10 USART, supporting ISO7816-3 protocol
  - 6 SPI
  - 6 I2C, support SMBus protocol
  - 4 I2S with built-in audio PLL
  - 2 SDIO, support SD/MMC/eMMC format
  - 1 QSPI supporting 240Mbps high-speed access (XIP)
  - 4 CAN FD controllers, compatible with CAN2.0A/B
  - 2 USB 2.0, supporting HS and FS, with built-in FS-PHY, Device/Host
  - 1 10/100M ETHMAC, supporting dedicated DMA, IEEE 1588-2018 PTP, MII/RMII interfaces
- External memory controller EXMC
  - Support Memory controllers: SRAM, PSRAM, NOR Flash, NAND Flash, SDRAM
  - Supports LCD parallel interface, compatible with 8080/6800 modes

- Hardware Security Module
  - HSM Light-Mid, including PKE/SKE/HASH (SHA256/HMAC) /TRNG
- Security mechanism
  - Error Management Unit (ERMU)
- Meets AEC-Q100
- Support ISO26262 ASIL-B
- Package Form: LQFP176/144/100

Support model

HC32A4A8PITJ-LQFP100	HC32A4A8PITI-LQFP100
HC32A4A8RITJ-LQFP144	HC32A4A8RITI-LQFP144
HC32A4A8SITJ-LQFP176	HC32A4A8SITI-LQFP176

Statement

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Preface

Number Format

- 0x prefix is used for hexadecimal numbers
- 0b prefix is used for binary numbers
- Numbers without prefix are in decimal representation

Security Statement

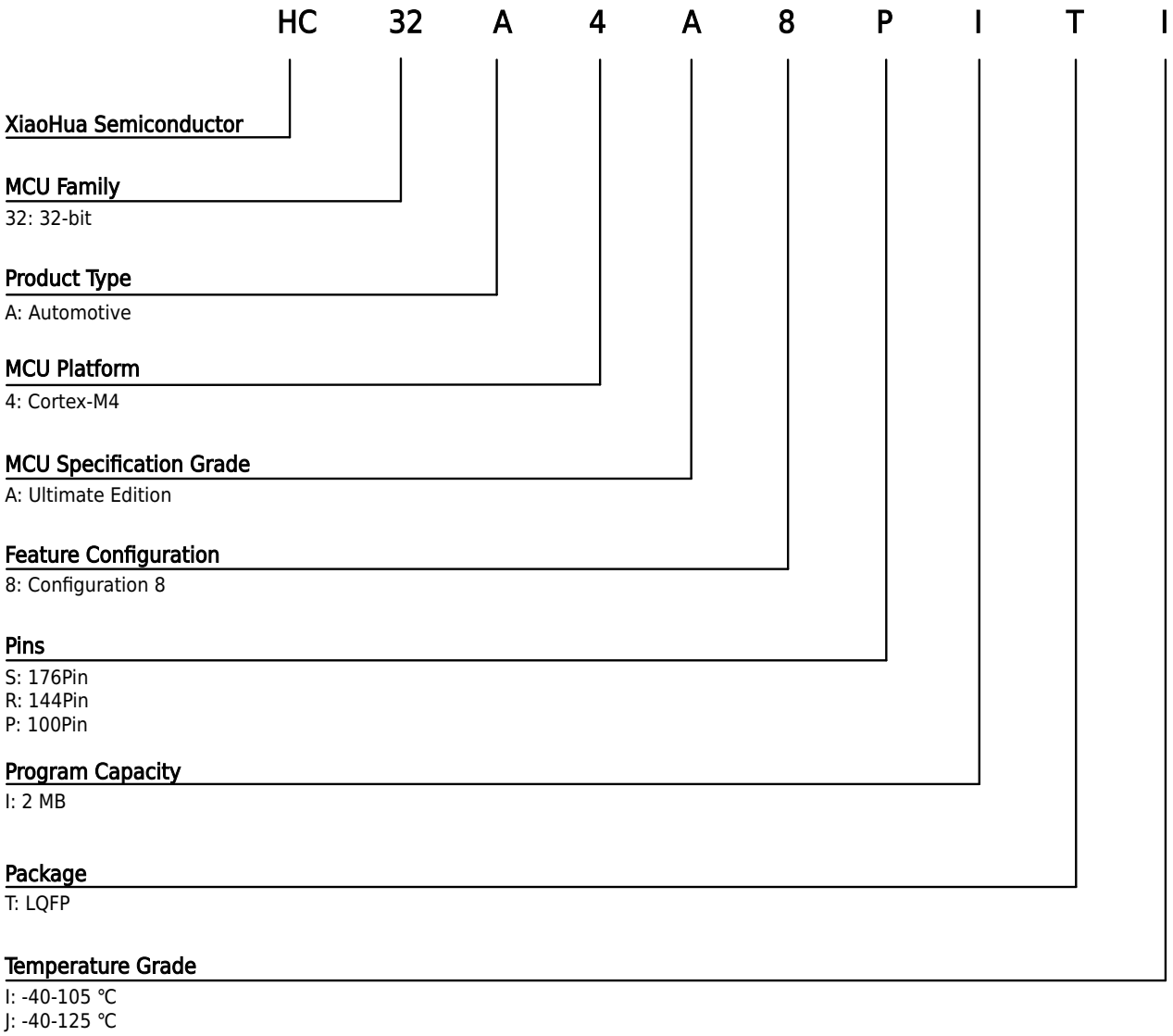
There may be potential security problems due to the use of a certain function or protocol, which need to be declared to remind users and avoid security risks.

Contents

1 Product Overview

1.1 Product Lineup

Product Name

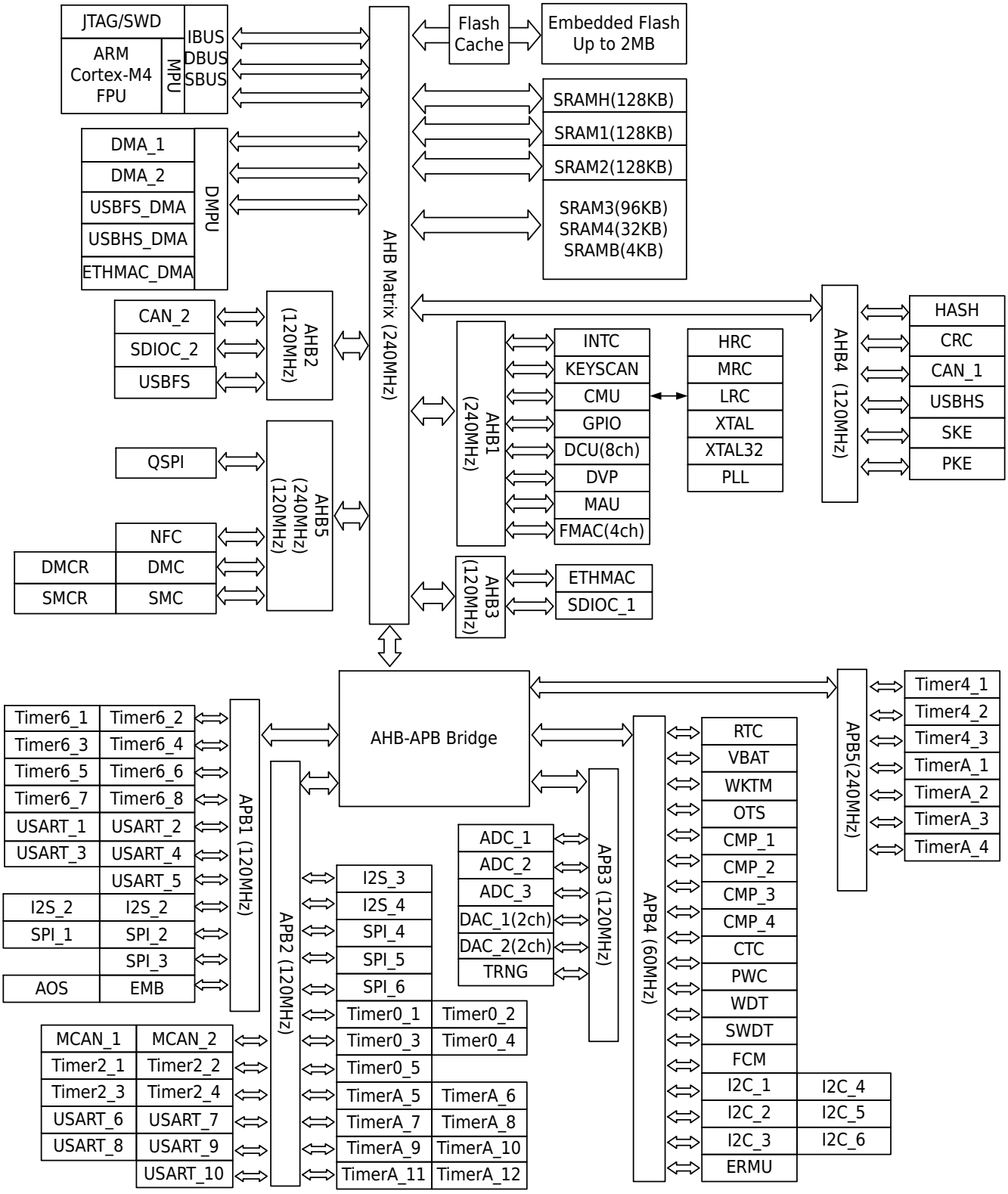


Model Function Comparison Table

Product Name		HC32A4A8SITI	HC32A4A8SITJ	HC32A4A8RITI	HC32A4A8RITJ	HC32A4A8PITI	HC32A4A8PITJ
Pins		176	176	144	144	100	100
GPIOs		142	142	116	116	83	83
5V Tolerant GPIOs		138	138	112	112	79	79
CPU	Core	Cortex-M4					
	Frequency	240MHz	200MHz	240MHz	200MHz	240MHz	200MHz
Storage Space	Flash	2MB					
	OTP	134KB					
	SRAM	512+4KB					
Clock	HRC	16/20MHz					
	MRC	8MHz					
	LRC	32.768kHz					
	XTAL	4-25MHz					
	XTAL32	32.768kHz					
	RTCLRC	32.768kHz					
	SWDTLRC	10kHZ					
Power Voltage Range		1.8-3.63V	2.7-3.63V	1.8-3.63V	2.7-3.63V	1.8-3.63V	2.7-3.63V
Temperature Range		-40-105℃	-40-125℃	-40-105℃	-40-125℃	-40-105℃	-40-125℃
External Port Interrupt		EIRQ * 16					
DMA Controller		2unit * 8ch					
Timer and Counter	Timer0	5unit					
	Timer2	4unit					
	TimerA	12unit					
	Timer4	3unit					
	Timer6	8unit					
	RTC	1ch					
	WDT	1ch					
	SWDT	1ch					

Product Name		HC32A4A8SITI	HC32A4A8SITJ	HC32A4A8RITI	HC32A4A8RITJ	HC32A4A8PITI	HC32A4A8PITJ
Connectivity	USART	10ch					
	I2C	6ch					
	SPI	6ch					
	QSPI	1ch					
	USB HS	1ch					
	USB FS	1ch					
	CAN FD	4ch					
	EXMC	√					
	ETHMAC	1ch					
	I2S	4ch					
	SDIO	2ch					
	DVP	√					
Analog	12-bit ADC	3unit, 28ch	3unit, 28ch	3unit, 24ch	3unit, 24ch	3unit, 16ch	3unit, 16ch
	12-bit DAC	4ch					
	PGA	4ch					
	OTS	√					
	CMP	4ch					
	PVD	√					
Security	HSM Light-Mid	√					
	SKE	√					
	PKE	√					
	TRNG	√					
	Hash	SHA256					
Co-processing	FMAC	√					
	MAU	√					
	DCU	√					
FCM		√					
ERMU		√					
Debugging Interface	SWD	√					
	JTAG	√					
Package		LQFP					

1.2 Functional Block Diagram



Note

Products in different packages support varying resources. For detailed specifications, please refer to Model Function Comparison Table.

2 Functional Description

2.1 CPU

HC32A4A8 Series integrates embedded ARM® Cortex-M4 with FPU 32-bit simplified command CPU, and provides excellent computing performance and rapid interrupt response capability. The on-chip integrated storage capacity can give full play to the excellent command efficiency of ARM® Cortex-M4. The CPU supports DSP command, which can realize efficient signal processing operations and complex algorithms. Single-point precision FPU (Floating Point Unit) can avoid command saturation and speed up software development.

Note

HC32A4A8SITI/HC32A4A8RITI/HC32A4A8PITI support a maximum operating main frequency of 240 MHz, achieving computational performance of up to 300 DMIPS or 825 Coremarks. HC32A4A8SITJ/HC32A4A8RITJ/HC32A4A8PITJ support a maximum operating main frequency of 200 MHz, achieving computational performance of up to 250 DMIPS or 680 Coremarks.

2.2 BUS

The main system consists of a 32-bit multi-layer AHB bus matrix, enabling the interconnection of the following host buses and slave buses:

- Host bus
  - Cortex-M4 core CPU-I bus, CPU-D bus, CPU-S bus
  - System DMA_1 bus, System DMA_2 bus
  - USBFS_DMA bus
  - USBHS_DMA bus
  - ETHMAC_DMA bus
- Slave bus
  - Flash ICODE bus
  - Flash DCODE bus
  - Flash MCODE bus (The bus through which non-CPU hosts access the Flash memory)
  - High-speed SRAMH (SRAMH 128KB) bus
  - System SRAM (SRAM1 128KB) bus
  - System SRAM (SRAM2 128KB) bus
  - System SRAM (SRAM3 96KB, SRAM4 32KB, Ret SRAM 4KB) bus
  - APB1 peripheral bus (AOS/EMB/Timer6/SPI/USART/I2S/EFM)
  - APB2 peripheral bus (Timer0/Timer2/TimerA/SPI/USART/I2S/CAN/MCAN)
  - APB3 peripheral bus (ADC/DAC/TRNG)
  - APB4 peripheral bus (FCG/CMU/FCM/ERMU/WDT/SWDT/CMP/PWC/CTC/OTS/RTC/VBAT/WKTM/I2C)
  - APB5 peripheral bus (Timer4/TimerA)
  - AHB1 peripheral bus (MPU/RAMIF/KEYSCAN/INTC/DCU/GPIO/DMA/CMU/DVP/MAU/FMAC)
  - AHB2 peripheral bus (CAN/SDIOC/USBFS)
  - AHB3 peripheral bus (SDIOC/ETHMAC)
  - AHB4 peripheral bus (HASH/CRC/CAN/USBHS/PKE/SKE)

- AHB5 peripheral bus (SMC/DMC/SMCR/DMCR/NFC/QSPI)

With the bus matrix, efficient concurrent access from host buses to slave buses can be achieved.

2.3 RMU

The chip is configured with 16 reset modes:

- Power-on Reset (POR)
- NRST pin Reset (NRST)
- Brown-out Reset (BOR)
- Programmable Voltage Detect 1 Reset (PVD1R)
- Programmable Voltage Detect 2 Reset (PVD2R)
- Watchdog Reset (WDTR)
- Special Watchdog Reset (SWDTR)
- Power-down Wake-up Reset (PDRST)
- Software Reset (SRST)
- MPU Error Reset (MPUR)
- RAMECC Reset (RAMECCR)
- FLASHECC Reset (FLASHECCR)
- ERMU Reset (ERMUR)
- Clock Frequency Error Reset (CKFER)
- XTAL Error Reset (XTALER)
- Cortex-M4 Lockup Reset (LKUPR)

2.4 CMU

The clock control unit provides a series of clock functions with different frequencies, including: an External High-speed Oscillator, an External Low-speed Oscillator, two PLL clocks, an Internal High-speed Oscillator, an Internal Medium-speed Oscillator, an Internal Low-speed Oscillator, a RTC Dedicated Internal Low-speed Oscillator, a dedicated Internal Low-speed Oscillator for SWDT, a Clock Prescaler, Clock Multiplexing, and Clock Gating Circuit.

The clock control unit also provides a clock frequency measurement function. The clock frequency measurement circuit (FCM) monitors and measures the measurement target clock using the measurement reference clock. An interrupt or reset occurs when the setting range is exceeded.

AHB, APB, and Cortex-M4 clocks are derived from the System Clock. The maximum operating clock frequency of the System Clock can reach 240MHz, with 6 selectable clock sources:

1. External High-speed Oscillator (XTAL)
2. External Low-speed Oscillator (XTAL32)
3. PLLH Clock (PLLH)
4. Internal High-speed Oscillator (HRC)
5. Internal Medium-speed Oscillator (MRC)
6. Internal Low-speed Oscillator (LRC)

For each clock source, it can be individually turned on and off when not in use to reduce power consumption.

SWDT has an independent clock source: the Dedicated Internal Low-speed Oscillator for SWDT (SWDTLRC). The Real Time Clock (RTC) uses the External Low-speed Oscillator, the RTC Dedicated

Internal Low-speed Oscillator, or the XTAL fractional frequency division clock as the clock source. The 48MHz clock for USBFS can select the System Clock, PLLH, or PLLA as the clock source.

2.5 PWC

Power controller is used to control the supply, switching and detection of multiple power domains in multiple run modes and low power modes. The power controller consists of a power consumption control logic (PWCL), a power supply voltage detection unit (PVD), and a battery backup control module (BATBKUP) that automatically switches between VCC and battery power.

The operating voltage (VCC) of the chip is 1.8V to 3.63V. The voltage regulator (LDO) supplies power to the VDD and VDDR domains, and the VDDR voltage regulator (RLDO) supplies power to the VDDR domain in Power-down mode or when VCC is powered off. The chip provides two operating modes: high-speed and ultra-low-speed, and three low-power modes: sleep, stop and power-off through the power consumption control logic (PWCL).

The power voltage detection unit (PVD) provides functions such as power on reset (POR), power down reset (PDR), brown out reset (BOR), programmable voltage detection 1 (PVD1), programmable voltage detection 2 (PVD2), reference voltage measurement path, VBAT voltage detection, and VBAT voltage measurement. Among them, POR, PDR, and BOR control the chip reset action by detecting the VCC voltage. PVD1 detects the VCC voltage and resets or interrupts the chip according to the register settings. PVD2 detects VCC voltage or external input detection voltage, and generates reset or interrupt according to register selection. The reference voltage measurement path is a function for measuring the reference voltage using ADC. VBAT voltage detection is a function that reads the register to obtain the VBAT voltage is higher or lower than the VBAT detection voltage. The VBAT detection voltage can be selected as 1.8V or 2.1V using the register. The VBAT voltage measurement function refers to the function of using ADC to measure the 1/2 voltage division of VBAT to obtain the VBAT voltage value.

The battery backup domain maintains power through VBAT when VCC is powered off, ensuring that the real-time clock module (RTC) and wake-up timer (WKTM) can continue to operate and provide power for RLDO. When the chip enters Power-down mode or VCC loses power, the VDDR area can maintain power through RLDO to keep the data of 4KB Ret SRAM.

The analog blocks are equipped with dedicated supply pins for improved analog performance.

2.6 ICG

After the chip's reset is released, the hardware circuit reads data from FLASH addresses 0x00000400-0x0000046F and loads it into the Initialization Configuration (ICG) register. Addresses 0x00000408-0x0000040B, 0x00000410-0x0000041F, and 0x00000438-0x0000045F are reserved; please write all 1s to ensure normal chip action. When FLASH boot swap is enabled and OTP is not enabled, this region is located in FLASH block 1, sector 0; Otherwise, this region is in FLASH block 0, sector 0. Users can modify the ICG register by programming or erasing sector 0. Addresses 0x00000420-0x00000437 are the data security protection enable region. The register reset value is determined by FLASH data.

2.7 EFM

The Flash interface accesses Flash through the ICODE, DCODE, and MCODE buses. The interface can perform programming, erasing and full erasing operations on Flash. Besides, it can accelerate code execution through command prefetching and caching mechanisms.

Main Features:

- Two independent Flash blocks form a dual bank, enabling BGO (BackGround Operation) functionality
- 134KBytes OTP space
- ICODE Bus 16Bytes prefetching
- Two independent cache areas: ICODE bus cache space 4KBytes (256x128); DCODE bus cache space 1KBytes (64x128)
- Supports boot swap function
- Support data security protection
- Features ECC (Error Checking and Correcting), which can correct one-bit errors in 128-bit data and 9-bit ECC, detect one-bit errors in 20-bit address-related information, and detect two-bit errors in 128-bit data with 9-bit ECC and 20-bit address-related information.

2.8 SRAM

This product has 512KB system SRAM (SRAMH/SRAM1/SRAM2/SRAM3/SRAM4) and 4KB backup SRAM (Ret SRAM).

Each SRAM can be accessed as a byte, half-word (16 bits), or full-word (32 bits). High-speed SRAM (SRAMH) read and write operations can be performed at the fastest CPU speed (240MHz) with 0 wait (i.e. 1 period), and wait periods can also be inserted. The wait period for read and write accesses to each SRAM is set by the SRAM Wait Control Register (SRAM_WTCR).

Ret SRAM can provide 4KB of data retention space in Power-down mode.

SRAM1, SRAM2, SRAM3, SRAM4, SRAMH and Ret SRAM have ECC check. The ECC check is a one-correction-two-check code, which can correct one-bit error in the read data and address, or check 2-bit errors.

2.9 GPIO

Main features of GPIO:

- Each port group has 16 I/O pins, which may be less than 16 depending on actual configuration
- Support pull-up input
- Support push-pull, open-drain output mode
- Support high, medium and low drive modes
- Supports free switching between CMOS/Schmitt input modes
- Support for external interrupt input
- Support I/O pin peripheral function multiplexing, one I/O pin can have up to 64 optional multiplexing functions
- Individual I/O pins can be programmed independently
- Each I/O pin can select 2 functions to be enable at the same time (does not support 2 output functions to be enable at the same time)

2.10 INTC

The interrupt controller (INTC) selects an interrupt event as an interrupt request and sends it to NVIC to wake up WFI; selects interrupt event as event input (RXEV) to wake up WFE; select low power consumption mode (Sleep mode and Stop mode) of interrupt event wake-up system ; control external interrupts and software interrupts.

The main features of INTC are as follows:

1. Maskable interrupts: INTC is equipped with 457 interrupt events, which are processed and sent to NVIC as interrupt requests (IRQ). It supports 144 IRQs, each IRQ corresponds to one or more interrupt events.

   Note

   For more instructions on exception and NVIC programming, please refer to the "Arm Cortex-M4 Processor Technical Reference Manual".

2. Programmable priority of NVIC: 16 programmable priorities (4-bit interrupt priority register is used).
3. Non-maskable interrupts: Multiple system interrupt event requests can be independently selected as non-maskable interrupts, and each interrupt event is equipped with independent enable, flag and flag clear registers.
4. Equipped with 16 external pin interrupt events.
5. Equipped with multiple interrupt events, please refer to the "Interrupt Event List" in the "Interrupt Controller (INTC)" chapter of "Reference Manual" for the specific number.
6. Equipped with 32 software interrupt events.
7. Interrupt wakes up system Sleep mode and Stop mode.

2.11 AOS

The Automatic Operation System (AOS) is used to achieve coordination between peripherals without the assistance of the CPU. It utilizes events generated by peripherals as AOS sources, such as timer comparison matches, timer counting overflow, RTC periodic signals, various states of the sending and receiving data of the communication module (idle, receive data full, transmit data end, transmit data empty), ADC conversion end events, etc., to trigger actions of other peripherals. The triggered peripheral actions are referred to as AOS targets.

The AOS also equips 4 programmable logical units (PLUs) for logical operations between PORT and AOS sources. Users can select one or more AOS sources to trigger the same AOS target based on their needs.

2.12 MPU

The MPU can provide protection to the memory, and can improve the security of the system by preventing unauthorized access.

This chip has built-in 1 MPU unit for CPU, 5 MPU units for host and 1 MPU unit for IP.

Among them, the ARM MPU provides the access control of the CPU to the entire 4G address space.

DMPU includes SMPU1/SMPU2/FMPU/HMPU/EMPU, which respectively provide read and write access rights control of system DMA_1/system DMA_2/USBFS-DMA/USBHS-DMA/ETH-DMA to the entire 4G address space. When accessing the prohibited space, the MPU action can be set to ignore/bus error/non-maskable interrupt/reset.

The IPMPU provides access control to system IP and security-related IP in non-privileged mode.

2.13 KEYSCAN

This product is equipped with a keyboard scan control module (KEYSCAN) 1 unit. The KEYSCAN module supports keyboard array (row and column) scanning, the column is driven by an independent scan output KEYOUTm (m=0-7), and the row KEYINn (n=0-15) is input as EIRQn (n=0-15) is detected. This module realizes the key recognition function through the line scan query method.

2.14 CTC

Clock Trimming Controller (CTC) can automatically calibrate internal high-speed oscillator (HRC). Due to the influence of the working environment, the frequency of HRC may deviate. Based on the external high-precision reference clock, CTC is used to automatically adjust the frequency of HRC by hardware to get an accurate HRC clock.

The CTC main features are as follows:

- Three external reference clock sources: XTAL, XTAL32, CTCREF
- 16-bit calibration counter for frequency measurement with reload function
- 8-bit calibration deviation value and 6-bit calibration value for frequency calibration
- Error interrupt for indicating calibration failure

2.15 DMA

DMA is used to transfer data between memory and peripheral function modules, enabling data exchange between memories, between memory and peripheral function modules, and between peripheral function modules without CPU involvement.

Main features of DMA:

- The DMA bus is independent of the CPU bus and transmits data according to the AMBA AHB-Lite bus protocol.
- With 2 DMA control units, a total of 16 independent channels, which can independently operate different DMA transfer functions.
- The start source of each channel is configured through an independent trigger source selection register.
- 1 block per request.
- The data block is a minimum of one data and can be up to 1024 data.
- The width of each data item can be configured as 8-bit, 16-bit, or 32-bit.
- It can be configured for 1-65535 transfers or infinite transfers.
- The source address and destination address can be independently configured as fixed, incrementing, decrementing, repeated jump, or specified offset jump.
- 3 types of interrupts can be generated: block transfer completed interrupt, transfer completed interrupt, and transfer error interrupt. Each interrupt can be configured to be masked or unmasked. Among them, block transfer completed and transfer completed can be used as event outputs, serving as trigger sources for other peripheral modules.
- Support chain transfer function, enabling the transfer of multiple data blocks in a single request.
- Support channel reset triggered by external events.
- Support software-triggered start of transfer and software-triggered channel reset.
- When not in use, it can be set to stop state to reduce power consumption.
- The HPROT value in the AHB bus during DMA access can be set through a register.

2.16 CMP

Voltage Comparator (hereinafter referred to as CMP) is a peripheral module that compares two analog voltages and outputs the comparison result. This product is equipped with two groups of 4 comparison channels: CMP1 and CMP2, CMP3 and CMP4.

CMP Main features:

- 4 comparison channels can independently perform normal comparison.
- Two comparison channels in the same group can be combined to achieve up to 2 window comparisons.
- Each comparison channel's positive and negative voltage inputs have multiple input sources (IO, PGA, DAC) to choose from.
- Hysteresis voltage is configurable.
- A noise filter can filter the comparator output, with 3 sampling clocks to choose from.
- Timer PWM can be used for comparator blanking window control.
- Interrupts can be generated at the edges of comparison result changes, other peripherals can be triggered, and STOP mode can be woken up.
- Compare results can be monitored through registers and output to the external pin VCOUT.
- Compare results can be used for EMB control events.

2.17 ADC

The 12-bit ADC is an analog-to-digital converter that adopts the successive approximation method. This MCU is equipped with 3 ADC units, units 1 and 2 support 16 channels, unit 3 supports 20 channels, which can convert analog signals from external pins and inside the chip. Analog input channels can be arbitrarily combined into a sequence for single scan or continuous scan conversion. It supports continuous multiple conversions on any specified channel and averaging of the conversion results. The ADC block also includes an analog watchdog function that monitors the conversion results of any specified channel to detect if they exceed user-set ranges.

The main features of the ADC are as follows:

- High Performance
  - Configurable 12-bit, 10-bit and 8-bit resolution
  - The frequency ratio of the ADC digital interface clock (PCLK4) and conversion clock (PCLK2, also known as ADCLK) can be set to 1:1, 2:1, 4:1, 8:1, 1:2, or 1:4

    PCLK2 can optionally use a PLL clock source asynchronous to the system clock (HCLK), with a frequency ratio of PCLK4:PCLK2=1:1

    PCLK2 frequency supports up to 60MHz
  - Sample Rate: 2.5Msps (PCLK2=60MHz, 12-bit, 11 sample periods, 13 conversion periods)
  - Independent programming of channel sampling time is supported
  - Each channel has an independent data register
  - Data registers can be configured for left/right alignment
  - Continuous multiple conversion averaging function
  - Oversampling function
  - Analog watchdog to monitor conversion results
  - The ADC module can be set to stop when not in use
- Analog Input Channel
  - Maximum of 28 external analog inputs, with a maximum of 20 channels supported by a single ADC unit
  - 2 internal analog signals: internal reference voltage, and VBAT divider
- Conversion Start Conditions
  - Software setup conversion started

  - Peripheral synchronously trigger the conversion to start
  - External pin trigger the conversion to start
- Conversion Mode
  - 2 scan sequences A, B, optionally specifying a single or multiple channels
  - Sequence A single scan
  - Sequence A continuous scan
  - Sequence A data buffer
  - Dual sequence scan, with sequences A and B independently selecting trigger sources, and sequence B having higher priority than A.
  - Cooperative operating mode (applicable to devices with two or three ADCs)
- Interrupt and Event Signal Output
  - Sequence A scan end interrupt and event ADC_EOCA
  - Sequence B scan end interrupt and event ADC_EOCB
  - Analog watchdog 0 compare interrupt and event ADC_CMP0
  - Analog watchdog 1 compare interrupt and event ADC_CMP1
  - All the event outputs mentioned above can start DMA

This MCU is equipped with four unit-programmable gain amplifiers PGA, and the gain range is selectable from x2 to x32. Analog input can be amplified by PGA circuit first, and then input to ADC module for conversion.

This MCU is equipped with three special sample-and-hold circuits (SH) for channels CH0-2 of ADC1. When the special sample hold circuit is active, every time the sequence is started, all the channels with active SH are sampled at the same time, and then the ADC is started to perform A/D conversion on each channel in the sequence in turn. In continuous scanning mode, the sampling time of SH will be inserted into the sequence at the start of the second and subsequent scanning.

2.18 DAC

This MCU is equipped with 2 12-bit digital-to-analog converter (DAC) unit, DAC1 and DAC2. Each DAC unit includes two DAC conversion channels that can operate independently or synchronously. The analog voltage output range has two selectable settings. Each conversion channel has an output amplifier to drive external loads directly without an external operational amplifier. Independent pin inputs for reference voltages VREFH and VREFL can improve conversion accuracy.

DAC Main features:

- 2 DAC units, each with 2 DAC conversion channels.
- 12-bit conversion data can be configured as left- or right-aligned.
- Both conversion channels in the same DAC module can perform synchronous conversion.
- The data computing unit (DCU) can output triangular and sawtooth waves.
- The output can be used as the negative-end voltage for the voltage comparator (CMP).
- The output has amplification function and can drive external loads directly.
- The ADC conversion priority mode reduces interference during ADC conversion.
- Independent pin inputs for reference voltages VREFH/VREFL

2.19 OTS

OTS can obtain the temperature inside the chip to support the reliable operation of the system. After using software or hardware to trigger the start of temperature measurement, OTS provides a set of

digital quantities related to temperature, and the temperature value can be calculated through the calculation formula.

2.20 Timer6

Advanced Control Timer 6 (Timer6) is a high-performance timer with 32/16-bit counting width, offering a rich and flexible combination of configurations suitable for various complex application scenarios. It supports multiple interrupts, events, and PWM outputs. This timer supports both sawtooth and triangular waveform modes and can generate various types of PWM signals (edge-aligned independent PWM, center-aligned independent PWM, center-aligned complementary PWM, and center-aligned asymmetric PWM, etc.). It enables both software and hardware synchronization between units (synchronized start, stop, clear, refresh, etc.). All reference registers support buffering (single-level and double-level buffering). Timer6 also supports pulse width and period measurement, 2-phase and 3-phase quadrature encoding count, and EMB control, units 1 through 5 and unit 7 support PTO (Pulse Train Output). This series of products is equipped with 8 units of Timer6 (unit 1 to unit 4 are 32-bit timers; unit 5 to unit 8 are 16-bit timers).

2.21 Timer4

The General Control Timer 4 is a timer module designed for three-phase motor control, offering a variety of solutions for different three-phase motor control applications. It supports both triangular and sawtooth waveform modes, enabling the generation of various PWM waveforms. It also features buffer functionality and supports EMB control. 3 unit of Timer4 is carried in this product family.

2.22 EMB

The emergency brake module is a function module that generates contorl events output to the timer when certain conditions are met to stop the timer or change the PWM signal output to the external motor. The following factors are used to generate control events:

- External port input level change
- Level of PWM output port occurs in phase (same high or same low)
- Voltage comparator comparison results
- System error occurred
- Write register software control

2.23 TimerA

The General Timer A (TimerA) is a timer with a 16-bit counting width and 4-channel PWM output. The timer supports two waveform modes, triangle wave and sawtooth wave, and can generate various PWM waveforms (single-side aligned PWM, double-side symmetrical PWM); supports synchronous start of counter; the compare reference value register supports buffer function; supports cascading between units to achieve 32-bit counting; supports 2-phase quadrature encoding count and 3-phase quadrature encoding count. This product series is equipped with 12 TimerA units, supporting up to 48 PWM outputs.

2.24 Timer2

General Timer 2 (Timer2) is a basic timer that can realize synchronous counting and asynchronous counting. The timer contains two channels (CH-A and CH-B). Each channel has an output port, which can realize basic square wave output. Each channel has two input ports, one is a clock input port, which can realize asynchronous port counting; the other one is a trigger input port, which can realize timer start, stop, clear, counting action and counting value capture input; support pulse width measurement and period measurement. This series of products is equipped with 4 units of Timer2.

2.25 Timer0

General Timer 0 (Timer0) is a basic timer that can realize synchronous counting and asynchronous counting. The timer contains two channels (CH-A and CH-B) that can generate compare match events and count overflow events during counting. This event can trigger an interrupt and can be used to trigger other module actions. This series of products is equipped with 5 units of Timer0.

2.26 RTC

A real time clock (RTC) is a counter that stores time information in BCD format. Record the specific calendar time from 00 to 99. Support 12/24 hour time system, automatically calculate the number of days 28, 29 (leap year), 30 and 31 according to the month and year.

2.27 WDT/SWDT

This product has two watchdog timers: one is a specialized watchdog timer (SWDT) with a dedicated internal RC (SWDTLRC: 10kHz) as the counting clock source, and the other is a universal watchdog timer (WDT) with a PCLK3 as the counting clock source. SWDT and WDT are 16-bit down-counters designed to detect software faults caused by applications deviating from normal operation due to external interference or unforeseen logical conditions.

Both watchdogs support the window function. The window interval can be preset before the count starts, and when the count value is within the window interval, the counter can be refreshed and the count restarted.

2.28 USART

This product is equipped with 10 units of Universal Synchronous Asynchronous Receiver/Transmitter (USART) modules, which can flexibly exchange full-duplex data with external devices; the USART equipped in this product supports universal asynchronous serial communication interface (UART) , clock synchronous communication interface, smart card interface (ISO/IEC7816-3) and LIN communication interface. Support modem operation (CTS/RTS operation), multiprocessor operation, DE function. UART receive timeout function is supported by cooperating with the Timer0 module. USART1 supports the STOP mode wake-up function via the RX line.

The specific function allocation is as follows:

Function	Support Module									
	USART1	USART2	USART3	USART4	USART5	USART6	USART7	USART8	USART9	USART10
UART	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Multiprocessor Communication	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Clock Synchronization Communication	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Wake-up from STOP Mode via RX Line	✓	-	-	-	-	-	-	-	-	-
Fractional Baud Rate	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LIN	-	-	-	-	✓	-	-	-	-	✓
Smart Card	✓	✓	✓	✓	-	✓	✓	✓	✓	-
UART Receive Timeout Function	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
RS485 Driver Enable	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

2.29 I2C

I2C (Inter-Integrated Circuit) used as an interface between the microcontroller and the I2C serial bus. Provide multi-master mode function, which can control the protocol and arbitration of all I2C buses. Standard mode and fast mode are supported. SMBus is also supported.

Main Features of I2C:

- I2C bus mode and SMBUS bus mode are optional. Master mode and slave mode are optional. Automatically ensure various preparation times, hold times, and bus idle times corresponding to the transfer rate
- Standard mode up to 100kbps, fast mode up to 400kbps
- The start condition, restart condition, and stop condition are automatically generated, and the start condition, restart condition, and stop condition of the bus can be detected
- Supports up to 128 slave mode addresses. Supports 7-bit address format and 10-bit address format. Broadcast call address, SMBus host address, SMBus device default address, SMBus alarm address can be detected
- Answer bits can be automatically determined when sent. Answer bits can be automatically sent when reception
- Handshake function
- Arbitration function
- Timeout function, can detect SCL clock stop for a long time
- SCL input and SDA input have built-in digital filters that are programmable to filter
- Communication error, receive data full, send data empty, one frame send end, address match unanimously interrupt
- 2-stage transmit FIFO and 2-stage receive FIFO

2.30 SPI

This product is equipped with 6-channel serial peripheral interface SPI, supports high-speed full-duplex serial synchronous transmission, and facilitates data exchange with peripheral devices. Users can set the range of 3/4-wire, master/slave and baud rate as as required.

Table 2-2 SPI Main Features

Essentials	Description
Serial Communication Function	● Supporting 4-wire SPI mode and 3-wire clock synchronization mode ● Supports full-duplex synchronous communication mode and transmit-only communication mode ● Polarity and phase of adjustable communication clock SCK
Data Format	● Selectable data shift order: MSB start/LSB start ● Selectable data width: 4/5/6/7/8/9/10/11/12/13/14/15/16/20/24/32 bits ● A maximum of 4 frames width of 32-bit data can be transmitted or received at a single time
Baud Rate	● The baud rate can be adjusted by the built-in special baud rate generator in master mode. The baud rate ranges from 2 to 256 frequency division of PCLK1. ● Maximum baud rate allowed in slave mode is 6 frequency division of PCLK1

Essentials	Description
Data Buffer	● With 16-byte data buffer ● Supports double buffering
Error Monitoring	● Mode fault error monitoring ● Data overload error monitoring ● Data underload error monitoring ● Parity error monitoring
Chip Selection Signal Control	● Each channel is configured with 4 chip-selected signal line ● The relative timing relationship between the chip select signal and the communication clock can be adjusted ● The inactive time of the chip select signal between two consecutive communications can be adjusted ● Polarity adjustable
Transmission Control in Master Mode	● Start transmission by writing data to the data register ● Communication auto suspend function
Interrupt	● Receive buffer is full ● Transmit buffer is empty ● SPI error (mode/overload/underload/parity) ● SPI vacant ● Transmit complete (event source only)
Low Power Control	● Configurable module stop
Other Functions	● SPI initialization function

2.31 QSPI

The Quad Serial Peripheral Interface (QSPI) is a memory control module designed to communicate with serial ROMs with an SPI-compatible interface. Its objects mainly include serial flash memory, serial EEPROM and serial FeRAM.

2.32 I2S

I2S (Inter_IC Sound Bus), an integrated circuit with built-in audio bus, is dedicated to data transmission between audio devices.

Table 2-3 I2S Main Features

Function	Main Features
Communication mode	● Support full-duplex and half-duplex communication ● Support master mode or slave mode operation

Function	Main Features
Data format	● Optional channel length: 16/32 bits ● Optional transmission data length: 16/24/32 bits ● Data shift order: MSB start
Baud rate	● 8-bit programmable linear prescaler for precise audio sampling frequency ● Support sampling frequencies 192kHz, 96kHz, 48kHz, 44.1kHz, 32kHz, 22.05kHz, 16kHz, 8kHz ● Can output driving clock to drive external audio components, the ratio is fixed at 256*Fs (Fs is the audio sampling frequency)
Support I2S protocol	● I2S Philips Standard ● MSB Alignment Standard ● LSB Alignment Standard ● PCM Standard
Data buffer	● With 4-word deep, 32-bit wide input and output FIFO buffer area
Clock source	● Can use internal I2SCLK (PLLAR/PLLAQ/PLLAP/PLLHR/PLLHQ/PLLHP) ● Can be provided by an external clock on the I2S_EXCK pin
Interrupt	● An interrupt is generated when the active space of the send buffer reaches the alarm threshold ● An interrupt is generated when the active space of the receive buffer reaches the alarm threshold ● The receiving data area is full and there is still a request to write data, the receiving overflow ● The transmit data area is empty and there are still sending requests, the sending underflow ● The transmit data area is full and there is still a request to write data, the sending overflow

2.33 USBHS

This product is equipped with one unit of USB2.0 high-speed module (USBHS), built-in on-chip full-speed PHY, and supports ULPI(SDR) interface. USBHS is a dual-role (DRD) controller, which supports both slave and host functions. In host mode, USBHS supports high-speed, full-speed and low-speed transceivers, while in slave mode, only high-speed and full-speed transceivers are supported. USBHS controller supports all four transmission modes defined by USB2.0 protocol (Control transfer, Bulk transfer, Interrupt transfer, and Isochronous transfer). The USBHS controller supports LPM (Link Power Management) function.

2.34 USBFS

USB full speed (USBFS) controller provides a set of USB communication solutions for portable devices. The USBFS controller supports host mode and device mode, and a full-speed PHY is integrated inside the chip. In host mode, the USBFS controller supports full-speed (FS, 12Mb/s) and low-speed (LS, 1.5Mb/s) transceivers, while in device mode it only supports full-speed (FS, 12Mb/s) transceivers. USBFS controller

supports all four transmission modes defined by USB2.0 protocol (Control transfer, Bulk transfer, Interrupt transfer, and Isochronous transfer). The USBFS controller supports LPM (Link Power Management) function.

2.35 CAN/MCAN

CAN FD controller follows CAN bus CAN2.0(2.0A, CAN2.0B) and CAN FD protocol.

CAN bus controller can handle data transmission and reception on the bus. This product is equipped with 4 channels of CAN FD (CAN1, CAN2, MCAN1 and MCAN2).

CAN1 and CAN2 FD controllers have 16 sets of filters. Filters are used to select messages for the application to receive.

The application programs in the CAN1 and CAN2 FD controllers can send the data to the bus through via 1 high-priority Primary Transmit Buffer (PTB) and 3 Secondary Transmit Buffer (STB), and the mailbox sending order is determined by the transmitting scheduler. Bus data is acquired through 8 Receive Buffer (hereinafter referred to as RB). 3 STBs and 8 RBs can be understood as a 3-level FIFO and an 8-level FIFO, and the FIFO is completely controlled by hardware. CAN1 and CAN2 FD bus controllers can also support Time-trigger communication.

Both MCAN1 and MCAN2 FD controllers conform to ISO 11898-1: 2015 (Part A and B of CAN Protocol Specification Version 2.0) and CAN FD Protocol Specification Version 1.0.

MCAN1 and MCAN2 FD controllers have 4KB message RAM memory, and can realize the functions of Rx Filter, Rx FIFO, Rx Buffer, Tx Event FIFO and Tx Buffer. The message RAM is shared between MCAN1 and MCAN2 modules.

2.36 ETHMAC

Ethernet MAC controller (ETHMAC) is used to send and receive data in Ethernet network according to IEEE802.3-2002 standard, and it has many application fields, such as switches and network interface cards. The MAC controller supports two industrial standard interfaces connected with external physical layer (PHY) : Media Independent Interface (MII) (defined in IEEE802.3 specification) and Simplified Media Independent Interface (RMII).

Mainly follow the following protocol specifications:

- IEEE802.3-2002, used for Ethernet MAC
- IEEE1588-2008 standard, used to specify network clock synchronization
- AMBA2.0, for AHB master/slave ports
- RMII interface specification

2.37 SDIOC

SDIOC provides an SD host interface and an MMC host interface for communicating with SD cards supporting the SD2.0 protocol, SDIO devices and MMC devices supporting the eMMC4.2 protocol. This product has 2 SDIO controllers, which can communicate with 2 SD/MMC/SDIO devices at the same time.

The features of SDIOC are as follows:

- Support SDSC, SDHC, SDXC format SD card and SDIO device
- Supports 1-bit and 4-bit SD bus
- Supports 1-bit, 4-bit and 8-bit MMC buses
- SD clock up to 50MHz
- With card identification and hardware write protection function

2.38 EXMC

The External Memory Controller (EXMC) is an independent block used to access various off-chip storage and achieve data exchange. Through configuration, EXMC can convert the internal AMBA protocol interface into various types of dedicated off-chip memory communication protocol interfaces, including SRAM, PSRAM, NOR Flash, NAND Flash, and SDRAM. EXMC is internally divided into multiple blocks, each supporting specific memory types. Users can control external corresponding memory types by configuring the registers of the block.

2.39 DVP

Digital Video Port (DVP) is a synchronous parallel interface, which can collect 8-bit, 10-bit, 12-bit or 14-bit high-speed data streams from external CMOS camera modules. Support software synchronization and hardware synchronization. Support data stream acquisition frequency control and window clipping control. Supports data stream acquisition in various formats such as monochrome or raw Bayer format, YCbCr4:2:2, RGB565 progressive video, and compressed data (JPEG).

2.40 CPM

The cryptographic co-processing module (CPM) includes 4 sub-modules: HASH, TRNG, SKE and PKE.

The HASH secure hash algorithm is the SHA-2 version of SHA-256 (Secure Hash Algorithm), which complies with the national standard "FIPS PUB 180-3" issued by the US National Institute of Standards and Technology, and can process messages with a length of no more than 2^{64} bits. Produces a 256-bit message digest output.

TRNG is a random number generator based on continuous analog noise, providing 64bit random numbers.

SKE supports the following functions:

- AES encryption and decryption algorithm, which supports 128, 192 and 256-bit keys, follows the description of algorithm principle in FIPS PUB 197.
- DES encryption and decryption algorithm follows the description of algorithm principle in FIPS PUB 46-3.
- SM4 encryption and decryption algorithm follows the description of the algorithm principle in GMT0002-2012.
- Support 8 operating modes, which are ECB, CBC, CTR, CFB, OFB, GCM, CCM and CMAC, and support data interleaving in GCM, CCM and CMAC modes.

The PKE public key engine module consists of 1 operation module and 2 dedicated RAM memories. With the software driver, RSA (RSA 1024/RSA 2048/RSA 3072/RSA 4096), ECC (brainpoolp 160/brainpoolp 256/brainpoolp 512/secp 192/secp 224/secp 256/secp 384/secp 521) and SM2 can be realized.

2.41 CRC

The CRC algorithm of this module follows the definition of ISO/IEC13239, and adopts 16-bit CRC, 32-bit CRC and 64-bit CRC respectively. It supports 11 kinds of polynomial counting, which are CRC16/CCITT, CRC16/CCITT-FALSE, CRC16/XMODE, CRC16/IBM, CRC16/MAXIM, CRC16/USB, CRC16/MODBUS, CRC16/X25, CRC32, CRC32/MPEG-2 and CRC64.

2.42 DCU

The Data Computing Unit (DCU) is a simple data processing block that does not rely on the CPU. Each DCU unit has three data registers capable of performing addition, subtraction, comparison, and window

comparison functions on two data values. It can also provide continuously varying digital values to the DAC module through timer triggers to generate triangular and sawtooth wave outputs. This product is equipped with 8 DCU units.

2.43 MAU

Math Arithmetical Unit (MAU) is a hardware accelerated operation module which contains two types of operations: root operation and sine operation, and supports root operation and sine operation of fixed points. The sine function supports $360°/2^{12}$ calculation accuracy.

2.44 FMAC

Filter Math Accelerator (FMAC) is a hardware acceleration module for FIR filter calculation. The module can carry out FIR digital filtering with a maximum of 16 orders and configurable orders. Built-in 16x16bits multiplier and 32+5bits adder, users can customize the output data precision. This series of products is equipped with 4 FMAC modules.

2.45 ERMU

Error Management Unit (ERMU) collects error notifications from the safety mechanisms of this product. Each error notification has three response behavior configurations: system interrupt, system reset, and output to the error output port to notify the system for further error handling operations.

2.46 HSM Light-Mid

Please refer to the "Safety Manual" for detailed description.

2.47 DBGC

This MCU's core is Cortex-M4, which includes hardware for advanced debugging functions and supports the Embedded Trace Macrocell (ETM). Using these debugging functions, the core can be stopped when fetching instructions (instruction breakpoint) or accessing data (data breakpoint). When the core is stopped, the internal state of the core and the external state of the system can be queried. After the query completes, the kernel and system are restored and program execution is restored.

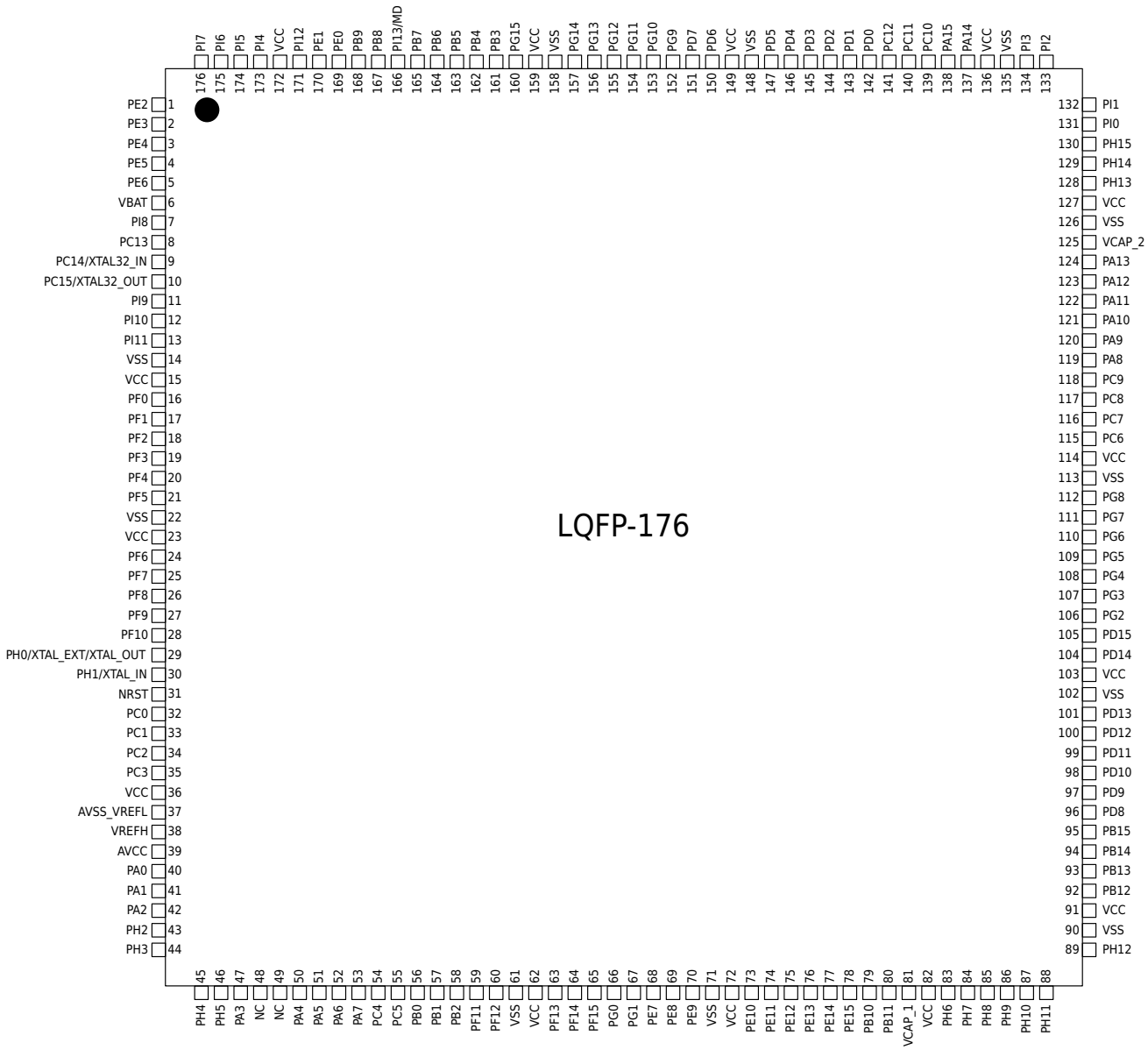
Two debugging interfaces are provided:

- Serial debug trace interface SWD
- Parallel debug trace interface JTAG

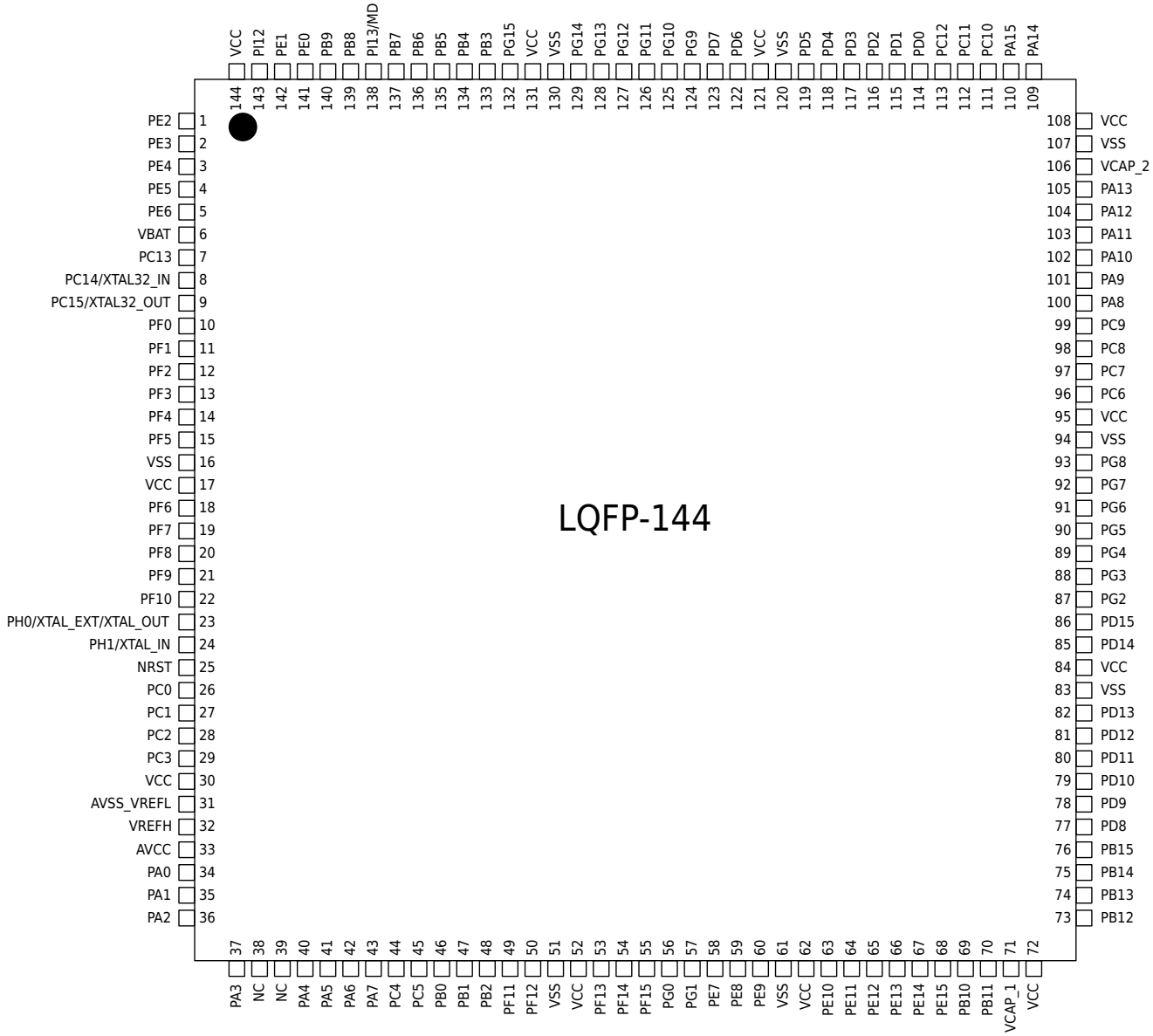
3 Pin Definitions

3.1 Pinout

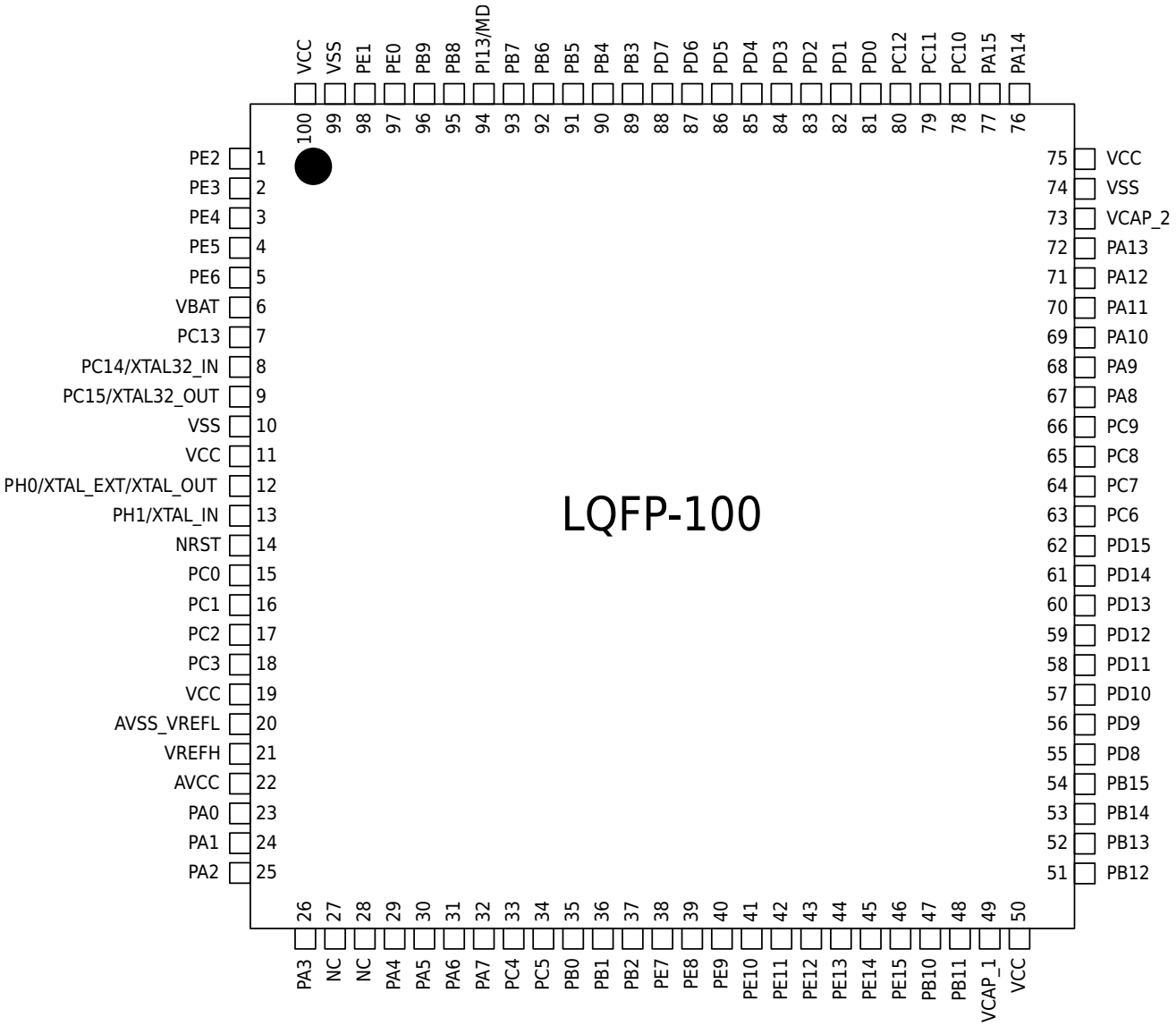
3.1.1 LQFP176 Package



3.1.2 LQFP144 Package



3.1.3 LQFP100 Package



3.2 Pin Function Table

LQFP 176	LQFP 144	LQFP 100	Pin Name	Analog	EIRQ/ WKUP	TRACE/JTAG/ ERMU	Func0 GPO	Func1 other	Func2 TMR4	Func3 TMR6	Func4 TMRA	Func5 TMRA	Func6 EMB,TMR6,TMRA	Func7 USART	Func8 KEYSCAN,TMR6	Func9 SDIO	Func10 USBFS,USBHS,TMR2	Func11 ETH	Func12 EXMC,USBHS	Func13 DVP,ERMU,EXMC	Func14 EVNTPT	Func15 EVENTOUT	Func16 TMR2,TMR4	Func17 I2S	Func18 SPI,QSPI	Func19 SPI	Func20 USART	Func21 EXMC	Func22 PLU_IN	Func23 PLU_OUT	Func28~63 Func Group
1	1	1	PE2		EIRQ2	TRACECLK	GPO	FCMREF	TMR4_3_ADSM		TMRA_9_PWM1/ TMRA_9_CLKA		TMRA_4_TRIG	USART3_CK				ETH_MII_TXD3	EXMC_ADD23			EVENTOUT		I2S3_MCK				PLU0_INA	PLU0_OUT	FG2
2	2	2	PE3		EIRQ3	TRACED0	GPO				TMRA_9_PWM2/ TMRA_9_CLKB	TMRA_4_PWM1/ TMRA_4_CLKA		USART6_CK				ETH_MII_RMII_TXEN	EXMC_ADD19			EVENTOUT	TMR2_1_CLKA	I2S4_SD	SPI2_NSS0				PLU0_INB	PLU1_OUT	FG2
3	3	3	PE4		EIRQ4	TRACED1	GPO				TMRA_9_PWM3	TMRA_4_PWM2/ TMRA_4_CLKB		USART6_CTS					EXMC_ADD20	DVP_DATA4		EVENTOUT	TMR2_1_CLKB			SPI4_NSS0			PLU0_INC	PLU2_OUT	FG2
4	4	4	PE5			TRACED2	GPO	CTCREF			TMRA_9_PWM4	TMRA_4_PWM3		USART6_RTS/ USART6_DE	TMR6_1_PWMZ				EXMC_ADD21	DVP_DATA6		EVENTOUT	TMR2_1_PWMA/ TMR2_1_TRIGA						PLU0_IND	PLU3_OUT	FG2
5	5	5	PE6		EIRQ6	TRACED3	GPO					TMRA_4_PWM4	TMRA_9_TRIG						EXMC_ADD22	DVP_DATA7		EVENTOUT	TMR2_1_PWMB/ TMR2_1_TRIGB						PLU1_INA	PLU0_OUT	FG2
6	6	6	VBAT																												
7	-	-	PI8	RTC_IC1	EIRQ8		GPO															EVENTOUT									
8	7	7	PC13	RTC_IC0	EIRQ13+ WKUP3_1		GPO	RTC_OUT			TMRA_10_PWM4					SDIO2_CK					EVNTP313	EVENTOUT		I2S3_MCK						
9	8	8	PC14	XTAL32_IN	EIRQ14		GPO				TMRA_10_PWM1/ TMRA_10_CLKA										EVNTP314	EVENTOUT								
10	9	9	PC15	XTAL32_OUT	EIRQ15		GPO				TMRA_10_PWM2/ TMRA_10_CLKB										EVNTP315	EVENTOUT								
11	-	-	PI9		EIRQ9		GPO						TMRA_6_TRIG						EXMC_DATA30			EVENTOUT						PLU1_INB	PLU1_OUT	FG3
12	-	-	PI10		EIRQ10		GPO				TMRA_6_PWM3				TMR6_2_PWMZ			ETH_MII_RXER	EXMC_DATA31			EVENTOUT						PLU1_INC	PLU2_OUT	FG3
13	-	-	PI11		EIRQ11		GPO				TMRA_6_PWM4				TMR6_3_PWMZ		USBHS_ULPI_DIR					EVENTOUT					EXMC_NFC_CE6	PLU1_IND	PLU3_OUT	FG3
14	-	-	VSS																												
15	-	-	VCC																												
16	10	-	PF0		EIRQ0		GPO	MCO_1				TMRA_11_PWM1/ TMRA_11_CLKA		USART10_CK					EXMC_ADD0			EVENTOUT			SPI3_NSS1				PLU2_INA	PLU0_OUT	FG3
17	11	-	PF1		EIRQ1		GPO					TMRA_11_PWM2/ TMRA_11_CLKB		USART10_CTS					EXMC_ADD1			EVENTOUT			SPI3_NSS2				PLU2_INB	PLU1_OUT	FG3
18	12	-	PF2		EIRQ2		GPO					TMRA_11_PWM3		USART10_RTS/ USART10_DE	TMR6_4_PWMZ				EXMC_ADD2			EVENTOUT			SPI3_NSS3				PLU2_INC	PLU2_OUT	FG3
19	13	-	PF3	ADC3_IN9	EIRQ3		GPO					TMRA_11_PWM4			TMR6_1_PWMZ				EXMC_ADD3			EVENTOUT	TMR2_3_CLKA		SPI4_NSS1				PLU2_IND	PLU3_OUT	FG3
20	14	-	PF4	ADC3_IN14	EIRQ4		GPO						TMRA_11_TRIG						EXMC_ADD4			EVENTOUT	TMR2_3_CLKB		SPI4_NSS2				PLU3_INA	PLU0_OUT	FG3
21	15	-	PF5	ADC3_IN15	EIRQ5		GPO						TMRA_10_TRIG						EXMC_ADD5			EVENTOUT			SPI4_NSS3				PLU3_INB	PLU1_OUT	FG3
22	16	10	VSS																												
23	17	11	VCC																												
24	18	-	PF6	ADC3_IN4	EIRQ6		GPO				TMRA_10_PWM1/ TMRA_10_CLKA								EXMC_RB2			EVENTOUT	TMR2_3_PWMA/ TMR2_3_TRIGA			SPI5_NSS0	USART7_RX		PLU3_INC	PLU2_OUT	FG3
25	19	-	PF7	ADC3_IN5	EIRQ7		GPO				TMRA_10_PWM2/ TMRA_10_CLKB								EXMC_RB3			EVENTOUT	TMR2_3_PWMB/ TMR2_3_TRIGB	I2S4_MCK		SPI5_SCK	USART7_TX		PLU3_IND	PLU3_OUT	FG3
26	20	-	PF8	ADC3_IN6	EIRQ8		GPO				TMRA_10_PWM3				TMR6_2_PWMZ				EXMC_RB4			EVENTOUT	TMR2_4_PWMA/ TMR2_4_TRIGA			SPI5_MISO			PLU0_INA	PLU0_OUT	FG3
27	21	-	PF9	ADC3_IN7	EIRQ9		GPO				TMRA_10_PWM4				TMR6_3_PWMZ				EXMC_RB5	DVP_PIXCLK		EVENTOUT	TMR2_4_PWMB/ TMR2_4_TRIGB			SPI5_MOSI			PLU0_INB	PLU1_OUT	FG3
28	22	-	PF10	ADC3_IN8	EIRQ10		GPO								TMR6_4_PWMZ				EXMC_RB6	DVP_DATA11		EVENTOUT							PLU0_INC	PLU2_OUT	FG3
29	23	12	PH0	XTAL_EXT/ XTAL_OUT	EIRQ0		GPO					TMRA_5_PWM3										EVENTOUT									
30	24	13	PH1	XTAL_IN	EIRQ1		GPO					TMRA_5_PWM4										EVENTOUT									
31	25	14	NRST																												
32	26	15	PC0	ADC123_IN10+ CMP3_INP4	EIRQ0		GPO				TMRA_8_PWM1/ TMRA_8_CLKA		TMRA_1_TRIG			SDIO2_D5	USBHS_ULPI_STP		EXMC_WE	ERMU_EOUT0C	EVNTP300	EVENTOUT	TMR2_4_PWMA/ TMR2_4_TRIGA	I2S1_EXCK				EXMC_DMC_WE	PLU0_IND	PLU3_OUT	FG3
33	27	16	PC1	ADC123_IN11	EIRQ1	ERMU_EOUT0M	GPO				TMRA_8_PWM2/ TMRA_8_CLKB		TMRA_1_TRIG			SDIO2_D6		ETH_SMI_MDC			EVNTP301	EVENTOUT	TMR2_4_PWMB/ TMR2_4_TRIGB	I2S1_MCK					PLU1_INA	PLU0_OUT	FG3
34	28	17	PC2	ADC123_IN12	EIRQ2		GPO		TMR4_2_ADSM	TMR6_8_PWMA	TMRA_8_PWM3		EMB_IN3			SDIO2_D7	USBHS_ULPI_DIR	ETH_MII_TXD2	EXMC_CE0	ERMU_EOUT1M	EVNTP302	EVENTOUT	TMR2_4_CLKA	I2S1_SDIN		SPI2_MISO		EXMC_DMC_CS0	PLU1_INB	PLU1_OUT	FG3
35	29	18	PC3	ADC123_IN13+ CMP1_INM4	EIRQ3		GPO		TMR4_2_PCT	TMR6_8_PWMB	TMRA_8_PWM4					SDIO1_WP	USBHS_ULPI_NXT	ETH_MII_TXCLK	EXMC_ALE	ERMU_EOUT1C	EVNTP303	EVENTOUT	TMR2_4_CLKB			SPI2_MOSI		EXMC_DMC_CKE	PLU1_INC	PLU2_OUT	FG3
36	30	19	VCC																												
-	-	-	VSS																												
-	-	-	AVSS																												
37	31	20	AVSS_VREFL																												
-	-	-	VREFL																												
38	32	21	VREFH																												
39	33	22	AVCC																												
-	-	-	AVCC																												
40	34	23	PA0	ADC123_IN0+ PGA1	EIRQ0+ WKUP0_0		GPO		TMR4_2_OUH	TMR6_TRIGC	TMRA_2_PWM1/ TMRA_2_CLKA	TMRA_2_TRIG	TMRA_5_PWM1/ TMRA_5_CLKA	USART5_CTS	TMR6_1_PWMZ	SDIO2_D4		ETH_MII_CRS		ERMU_EOUT2M	EVNTP100	EVENTOUT	TMR4_2_CLK		SPI5_NSS1		USART2_CTS		PLU1_IND	PLU3_OUT	FG2
41	35	24	PA1	ADC123_IN1+ PGA2	EIRQ1		GPO		TMR4_2_OUL		TMRA_2_PWM2/ TMRA_2_CLKB	TMRA_3_TRIG	TMRA_5_PWM2/ TMRA_5_CLKB	USART5_RTS/ USART5_DE		SDIO2_D5		ETH_MII_RMII_RXCLK		ERMU_EOUT2C	EVNTP101	EVENTOUT	TMR2_1_CLKA		SPI5_NSS2		USART2_RTS/ USART2_DE		PLU2_INA	PLU0_OUT	FG2
42	36	25	PA2	ADC123_IN2+ PGA3	EIRQ2		GPO		TMR4_2_OVH	TMR6_6_PWMA	TMRA_2_PWM3	TMRA_5_PWM1/ TMRA_5_CLKA	TMRA_5_PWM3			SDIO2_D6		ETH_SMI_MDIO		ERMU_EOUT3M	EVNTP102	EVENTOUT	TMR2_1_PWMA/ TMR2_1_TRIGA		SPI5_NSS3		USART2_TX		PLU2_INB	PLU1_OUT	FG2

LQFP 176	LQFP 144	LQFP 100	Pin Name	Analog	EIRQ/ WKUP	TRACE/JTAG/ ERMU	Func0 GPO	Func1 other	Func2 TMR4	Func3 TMR6	Func4 TMRA	Func5 TMRA	Func6 EMB,TMR6,TMRA	Func7 USART	Func8 KEYSCAN,TMR6	Func9 SDIO	Func10 USBFS,USBHS,TMR2	Func11 ETH	Func12 EXMC,USBHS	Func13 DVP,ERMU,EXMC	Func14 EVNTPT	Func15 EVENTOUT	Func16 TMR2,TMR4	Func17 I2S	Func18 SPI,QSPI	Func19 SPI	Func20 USART	Func21 EXMC	Func22 PLU_IN	Func23 PLU_OUT	Func28~63 Func Group
43	-	-	PH2	ADC3_IN16	EIRQ2		GPO	FCMREF	TMR4_2_CLK	TMR6_TRIGB	TMRA_10_PWM3		EMB_IN4		TMR6_1_PWMZ	SDIO2_D4		ETH_MII_CRS	EXMC_ALE			EVENTOUT		I2S3_EXCK				EXMC_DMC_CKE	PLU2_INC	PLU2_OUT	FG2
44	-	-	PH3	ADC3_IN17	EIRQ3		GPO								TMR6_2_PWMZ			ETH_MII_COL	EXMC_CE0			EVENTOUT						EXMC_DMC_CS1	PLU2_IND	PLU3_OUT	FG2
45	-	-	PH4	ADC3_IN18	EIRQ4		GPO								TMR6_3_PWMZ		USBHS_ULPI_NXT					EVENTOUT						EXMC_NFC_CE7	PLU3_INA	PLU0_OUT	FG2
46	-	-	PH5	ADC3_IN19	EIRQ5	ERMU_EOUT0M	GPO								TMR6_4_PWMZ				EXMC_WE			EVENTOUT	TMR2_1_CLKB		SPI5_NSS0			EXMC_DMC_WE	PLU3_INB	PLU1_OUT	FG2
47	37	26	PA3	ADC123_IN3+ PGA123_VSS+ CMP1_INP4	EIRQ3		GPO		TMR4_2_OVL	TMR6_6_PWMB	TMRA_2_PWM4	TMRA_5_PWM2/ TMRA_5_CLKB	TMRA_5_PWM4			SDIO2_D7	USBHS_ULPI_D0	ETH_MII_COL		ERMU_EOUT3C	EVNTP103	EVENTOUT	TMR2_1_PWMB/ TMR2_1_TRIGB				USART2_RX		PLU3_INC	PLU2_OUT	FG2
-	-	-	VSS																												
48	38	27	NC																												
49	39	28	NC																												
50	40	29	PA4	ADC12_IN4+ DAC1_OUT1+ CMP2_INP3	EIRQ4		GPO		TMR4_2_OWH	TMR6_7_PWMA		TMRA_9_PWM1/ TMRA_9_CLKA	TMRA_8_TRIG	USART5_CK	KEYOUT0				USBHS_SOF	DVP_HSYNC	EVNTP104	EVENTOUT	TMR2_4_CLKA	I2S1_EXCK		SPI1_NSS0	USART2_CK		PLU3_IND	PLU3_OUT	FG1
51	41	30	PA5	ADC12_IN5+ DAC1_OUT2+ CMP2_INP4	EIRQ5	ERMU_EOUT0M	GPO		TMR4_2_OWL	TMR6_7_PWMB	TMRA_2_PWM1/ TMRA_2_CLKA	TMRA_9_PWM2/ TMRA_9_CLKB	TMRA_2_TRIG		KEYOUT1		USBHS_ULPI_CLK				EVNTP105	EVENTOUT	TMR4_2_OUL	I2S1_MCK						PLU0_INA	PLU0_OUT	FG1
52	42	31	PA6	ADC12_IN6+ PGA4+ CMP1_INP2	EIRQ6		GPO					TMRA_3_PWM1/ TMRA_3_CLKA	EMB_IN2		KEYOUT2	SDIO1_CMD	TMR2_4_PWMA/ TMR2_4_TRIGA		EXMC_ADD26	DVP_PIXCLK	EVNTP106	EVENTOUT	TMR2_4_CLKB						PLU0_INB	PLU1_OUT	FG1
53	43	32	PA7	ADC12_IN7+ PGA4_VSS+ CMP123_INM3	EIRQ7		GPO		TMR4_1_OUL	TMR6_1_PWMB	TMRA_7_PWM1/ TMRA_7_CLKA	TMRA_3_PWM2/ TMRA_3_CLKB	EMB_IN3		KEYOUT3	SDIO2_WP	TMR2_4_PWMB/ TMR2_4_TRIGB	ETH_MII_RMII_RXDV	EXMC_ADD27		EVNTP107	EVENTOUT	TMR4_2_OUL						PLU0_INC	PLU2_OUT	FG1
54	44	33	PC4	ADC12_IN14+ DAC2_OUT1+ CMP2_INM4	EIRQ4		GPO		TMR4_2_OUH	TMR6_5_PWMA		TMRA_9_PWM3	TMRA_7_TRIG	USART1_CK		SDIO2_CD		ETH_MII_RMII_RXD0	EXMC_ADD28	ERMU_EOUT0C	EVNTP304	EVENTOUT	TMR2_4_PWMA/ TMR2_4_TRIGA		SPI1_NSS1				PLU0_IND	PLU3_OUT	FG1
55	45	34	PC5	ADC12_IN15+ DAC2_OUT2+ CMP3_INM4	EIRQ5		GPO		TMR4_2_OUL	TMR6_5_PWMB		TMRA_9_PWM4	EMB_IN1			SDIO2_CMD		ETH_MII_RMII_RXD1		ERMU_EOUT1M	EVNTP305	EVENTOUT	TMR2_4_PWMB/ TMR2_4_TRIGB		SPI1_NSS2				PLU1_INA	PLU0_OUT	FG1
56	46	35	PB0	ADC12_IN8+ CMP3_INP2	EIRQ0		GPO		TMR4_1_OVL	TMR6_2_PWMB	TMRA_7_PWM2/ TMRA_7_CLKB	TMRA_3_PWM3		USART4_CK	KEYOUT4	SDIO2_CMD	USBHS_ULPI_D1	ETH_MII_RXD2		ERMU_EOUT1C	EVNTP200	EVENTOUT	TMR4_2_OVL		SPI1_NSS3				PLU1_INB	PLU1_OUT	FG1
57	47	36	PB1	ADC12_IN9+ CMP3_INP3	EIRQ1+ WKUP0_1		GPO		TMR4_1_OWL	TMR6_3_PWMB	TMRA_7_PWM3	TMRA_3_PWM4			KEYOUT5	SDIO2_D3	USBHS_ULPI_D2	ETH_MII_RXD3			EVNTP201	EVENTOUT	TMR4_2_OWL	I2S2_EXCK	QSPI_NSS					PLU1_INC	PLU2_OUT	FG1
58	48	37	PB2	PVD2EXINP	EIRQ2+ WKUP0_2		GPO	CMP_VCOUT		TMR6_TRIGB	TMRA_7_PWM4	TMRA_9_TRIG	EMB_IN1	USART2_CK	TMR6_2_PWMZ	SDIO2_D2			EXMC_CLE	DVP_PIXCLK	EVNTP202	EVENTOUT		I2S2_MCK	QSPI_IO3			EXMC_DMC_AP	PLU1_IND	PLU3_OUT	FG1
59	49	-	PF11		EIRQ11		GPO		TMR4_2_PCT		TMRA_4_PWM1/ TMRA_4_CLKA			USART2_CTS					EXMC_OE	DVP_DATA12		EVENTOUT				SPI5_MOSI		EXMC_DMC_RAS	PLU2_INA	PLU0_OUT	FG1
60	50	-	PF12		EIRQ12		GPO		TMR4_2_ADSM		TMRA_4_PWM2/ TMRA_4_CLKB			USART2_RTS/ USART2_DE					EXMC_ADD6			EVENTOUT							PLU2_INB	PLU1_OUT	FG1
61	51	-	VSS																												
62	52	-	VCC																												
63	53	-	PF13		EIRQ13		GPO			TMR6_1_PWMA	TMRA_4_PWM3		TMRA_10_TRIG						EXMC_ADD7			EVENTOUT			SPI6_NSS3				PLU2_INC	PLU2_OUT	FG2
64	54	-	PF14		EIRQ14		GPO			TMR6_1_PWMB	TMRA_4_PWM4								EXMC_ADD8			EVENTOUT			SPI6_NSS2				PLU2_IND	PLU3_OUT	FG2
65	55	-	PF15		EIRQ15		GPO			TMR6_2_PWMA			TMRA_12_TRIG	USART7_RTS/ USART7_DE					EXMC_ADD9			EVENTOUT			SPI6_NSS1				PLU3_INA	PLU0_OUT	FG2
66	56	-	PG0		EIRQ0		GPO			TMR6_2_PWMB		TMRA_12_PWM3		USART7_CTS					EXMC_ADD10			EVENTOUT							PLU3_INB	PLU1_OUT	FG2
67	57	-	PG1		EIRQ1		GPO			TMR6_TRIGA		TMRA_12_PWM4		USART7_CK	TMR6_5_PWMZ				EXMC_ADD11			EVENTOUT							PLU3_INC	PLU2_OUT	FG2
68	58	38	PE7		EIRQ7		GPO	ADC1_ADTRG	TMR4_1_CLK	TMR6_TRIGB	TMRA_1_TRIG	TMRA_3_PWM3		USART1_CK	TMR6_3_PWMZ				EXMC_DATA4			EVENTOUT			SPI4_NSS1				PLU3_IND	PLU3_OUT	FG2
69	59	39	PE8		EIRQ8		GPO	CTCREF	TMR4_1_OUL	TMR6_1_PWMB	TMRA_7_PWM1/ TMRA_7_CLKA	TMRA_3_PWM4							EXMC_DATA5			EVENTOUT			SPI4_NSS2				PLU0_INA	PLU0_OUT	FG2
70	60	40	PE9		EIRQ9		GPO	ADC3_ADTRG	TMR4_1_OUH	TMR6_1_PWMA	TMRA_1_PWM1/ TMRA_1_CLKA								EXMC_DATA6			EVENTOUT			SPI4_NSS3				PLU0_INB	PLU1_OUT	FG2
71	61	-	VSS																												
72	62	-	VCC																												
73	63	41	PE10	CMP1_INP3	EIRQ10		GPO		TMR4_1_OVL	TMR6_2_PWMB	TMRA_7_PWM2/ TMRA_7_CLKB		TMRA_3_TRIG						EXMC_DATA7			EVENTOUT							PLU0_INC	PLU2_OUT	FG3
74	64	42	PE11		EIRQ11		GPO		TMR4_1_OVH	TMR6_2_PWMA	TMRA_1_PWM2/ TMRA_1_CLKB	TMRA_3_PWM1/ TMRA_3_CLKA					USBHS_ULPI_D7		EXMC_DATA8			EVENTOUT							PLU0_IND	PLU3_OUT	FG3
75	65	43	PE12	CMP4_INM3	EIRQ12		GPO		TMR4_1_OWL	TMR6_3_PWMB	TMRA_7_PWM3	TMRA_3_PWM2/ TMRA_3_CLKB					USBHS_ULPI_CLK		EXMC_DATA9			EVENTOUT	TMR2_2_CLKA		SPI1_NSS1				PLU1_INA	PLU0_OUT	FG3
76	66	44	PE13	CMP4_INM4	EIRQ13		GPO		TMR4_1_OWH	TMR6_3_PWMA	TMRA_1_PWM3	TMRA_3_PWM3					USBHS_ULPI_D0		EXMC_DATA10			EVENTOUT	TMR2_2_CLKB	I2S4_SDIN	SPI1_NSS2				PLU1_INB	PLU1_OUT	FG3
77	67	45	PE14	CMP4_INP3	EIRQ14		GPO		TMR4_1_CLK	TMR6_4_PWMA	TMRA_1_PWM4	TMRA_3_PWM4				SDIO1_CD	USBHS_ULPI_D1		EXMC_DATA11			EVENTOUT	TMR2_2_PWMA/ TMR2_2_TRIGA	I2S4_EXCK	SPI1_NSS3				PLU1_INC	PLU2_OUT	FG3
78	68	46	PE15	CMP4_INP4	EIRQ15		GPO		TMR4_1_PCT	TMR6_TRIGA	TMRA_7_PWM4	TMRA_5_TRIG	EMB_IN2	USART10_CK	TMR6_4_PWMZ	SDIO1_WP	USBHS_ULPI_D2		EXMC_DATA12			EVENTOUT	TMR2_2_PWMB/ TMR2_2_TRIGB	I2S4_MCK					PLU1_IND	PLU3_OUT	FG3
79	69	47	PB10		EIRQ10		GPO	ADC2_ADTRG	TMR4_2_OVH	TMR6_4_PWMB	TMRA_2_PWM3	TMRA_11_PWM4				SDIO1_D7	USBHS_ULPI_D3	ETH_MII_RXER			EVNTP210	EVENTOUT		I2S3_EXCK	QSPI_IO2	SPI2_SCK			PLU2_INA	PLU0_OUT	FG3
80	70	48	PB11		EIRQ11		GPO		TMR4_1_ADSM		TMRA_2_PWM4		EMB_IN2		TMR6_7_PWMZ		USBHS_ULPI_D4	ETH_MII_RMII_TXEN			EVNTP211	EVENTOUT							PLU2_INB	PLU1_OUT	FG3
81	71	49	VCAP_1																												
-	-	-	VSS																												
82	72	50	VCC																												
83	-	-	PH6		EIRQ6		GPO				TMRA_2_PWM3			USART5_CTS	TMR6_3_PWMZ			ETH_MII_RXD2	EXMC_CE1	DVP_DATA8		EVENTOUT	TMR2_2_PWMA/ TMR2_2_TRIGA					EXMC_DMC_CS2	PLU2_INC	PLU2_OUT	FG2

LQFP 176	LQFP 144	LQFP 100	Pin Name	Analog	EIRQ/ WKUP	TRACE/JTAG/ ERMU	Func0 GPO	Func1 other	Func2 TMR4	Func3 TMR6	Func4 TMRA	Func5 TMRA	Func6 EMB,TMR6,TMRA	Func7 USART	Func8 KEYSCAN,TMR6	Func9 SDIO	Func10 USBFS,USBHS,TMR2	Func11 ETH	Func12 EXMC,USBHS	Func13 DVP,ERMU,EXMC	Func14 EVNTPT	Func15 EVENTOUT	Func16 TMR2,TMR4	Func17 I2S	Func18 SPI,QSPI	Func19 SPI	Func20 USART	Func21 EXMC	Func22 PLU_IN	Func23 PLU_OUT	Func28~63 Func Group
84	-	-	PH7		EIRQ7		GPO				TMRA_2_PWM2/ TMRA_2_CLKB			USART5_RTS/ USART5_DE				ETH_MII_RXD3	EXMC_ALE	DVP_DATA9		EVENTOUT						EXMC_DMC_CKE	PLU2_IND	PLU3_OUT	FG2
85	-	-	PH8		EIRQ8		GPO			TMR6_3_PWMA	TMRA_2_PWM3			USART5_CK					EXMC_DATA16	DVP_HSYNC		EVENTOUT			SPI5_NSS0				PLU3_INA	PLU0_OUT	FG2
86	-	-	PH9		EIRQ9		GPO			TMR6_3_PWMB	TMRA_2_PWM4								EXMC_DATA17	DVP_DATA0		EVENTOUT	TMR2_2_PWMB/ TMR2_2_TRIGB		SPI5_NSS1				PLU3_INB	PLU1_OUT	FG2
87	-	-	PH10		EIRQ10		GPO			TMR6_4_PWMA		TMRA_5_PWM1/ TMRA_5_CLKA							EXMC_DATA18	DVP_DATA1		EVENTOUT			SPI5_NSS2				PLU3_INC	PLU2_OUT	FG2
88	-	-	PH11		EIRQ11		GPO			TMR6_4_PWMB		TMRA_5_PWM2/ TMRA_5_CLKB							EXMC_DATA19	DVP_DATA2		EVENTOUT			SPI5_NSS3				PLU3_IND	PLU3_OUT	FG2
89	-	-	PH12		EIRQ12		GPO					TMRA_5_PWM3			TMR6_4_PWMZ				EXMC_DATA20	DVP_DATA3		EVENTOUT							PLU0_INA	PLU0_OUT	FG2
90	-	-	VSS																												
91	-	-	VCC																												
92	73	51	PB12		EIRQ12		GPO	CMP1_VCOUT	TMR4_2_OVL	TMR6_TRIGB	TMRA_7_PWM4	TMRA_5_TRIG	EMB_IN2	USART3_CK	TMR6_5_PWMZ	SDIO2_D1	USBHS_ULPI_D5	ETH_MII_RMII_TXD0	USBHS_ID	ERMU_EOUT2M	EVNTP212	EVENTOUT		I2S3_MCK	QSPI_IO1	SPI2_NSS0			PLU0_INB	PLU1_OUT	FG1
93	74	52	PB13		EIRQ13		GPO	CMP2_VCOUT	TMR4_1_OUL	TMR6_1_PWMB	TMRA_7_PWM1/ TMRA_7_CLKA			USART3_CTS		SDIO2_D0	USBHS_ULPI_D6	ETH_MII_RMII_TXD1	USBHS_VBUS	ERMU_EOUT2C	EVNTP213	EVENTOUT			QSPI_IO0				PLU0_INC	PLU2_OUT	FG1
94	75	53	PB14	USBHS_DM	EIRQ14		GPO	CMP3_VCOUT	TMR4_1_OVL	TMR6_2_PWMB	TMRA_7_PWM2/ TMRA_7_CLKB			USART3_RTS/ USART3_DE		SDIO1_D6	TMR2_2_PWMA/ TMR2_2_TRIGA				EVNTP214	EVENTOUT	TMR4_2_OVL	I2S1_SDIN	QSPI_SCK				PLU0_IND	PLU3_OUT	FG1
95	76	54	PB15	USBHS_DP	EIRQ15		GPO	RTC_OUT	TMR4_1_OWL	TMR6_3_PWMB	TMRA_7_PWM3	TMRA_6_TRIG	EMB_IN4	USART3_CK		SDIO1_CK	TMR2_2_PWMB/ TMR2_2_TRIGB				EVNTP215	EVENTOUT	TMR4_2_OWL						PLU1_INA	PLU0_OUT	FG1
96	77	55	PD8		EIRQ8		GPO	CMP4_VCOUT	TMR4_3_OUL	TMR6_1_PWMB		TMRA_6_PWM1/ TMRA_6_CLKA		USART1_CTS	KEYOUT7		USBHS_DRVVBUS		EXMC_DATA13		EVNTP408	EVENTOUT	TMR2_2_CLKA		QSPI_IO0				PLU1_INB	PLU1_OUT	FG1
97	78	56	PD9		EIRQ9		GPO	CMP3_VCOUT	TMR4_3_OVL	TMR6_2_PWMB	TMRA_2_PWM1/ TMRA_2_CLKA	TMRA_6_PWM2/ TMRA_6_CLKB	EMB_IN3	USART1_RTS/ USART1_DE	KEYOUT6		USBHS_ULPI_D4		EXMC_DATA14		EVNTP409	EVENTOUT	TMR2_2_CLKB		QSPI_IO1				PLU1_INC	PLU2_OUT	FG1
98	79	57	PD10		EIRQ10		GPO	CAN2_TST_SAM-PLE	TMR4_3_OWL	TMR6_3_PWMB	TMRA_2_PWM2/ TMRA_2_CLKB	TMRA_6_PWM3		USART3_CK	KEYOUT5				EXMC_DATA15		EVNTP410	EVENTOUT	TMR2_2_PWMA/ TMR2_2_TRIGA	I2S2_EXCK	QSPI_IO2				PLU1_IND	PLU3_OUT	FG1
99	80	58	PD11		EIRQ11		GPO	CAN2_TST_CLOCK	TMR4_3_CLK	TMR6_TRIGB		TMRA_6_PWM4	TMRA_11_TRIG	USART3_CTS	KEYOUT4				EXMC_ADD16/DMC_ BA0_NFC_CLE		EVNTP411	EVENTOUT	TMR2_2_PWMB/ TMR2_2_TRIGB	I2S2_MCK	QSPI_IO3			EXMC_ADD16_NFC_CLE	PLU2_INA	PLU0_OUT	FG1
100	81	59	PD12		EIRQ12		GPO		TMR4_1_ADSM	TMR6_4_PWMB	TMRA_4_PWM1/ TMRA_4_CLKA	TMRA_11_PWM1/ TMRA_11_CLKA		USART3_RTS/ USART3_DE					EXMC_ADD17/DMC_ BA1_NFC_ALE		EVNTP412	EVENTOUT						EXMC_ADD17_NFC_ALE	PLU2_INB	PLU1_OUT	FG3
101	82	60	PD13		EIRQ13		GPO		TMR4_1_PCT	TMR6_4_PWMB	TMRA_4_PWM2/ TMRA_4_CLKB	TMRA_11_PWM2/ TMRA_11_CLKB		USART9_RTS/ USART9_DE					EXMC_ADD18		EVNTP413	EVENTOUT							PLU2_INC	PLU2_OUT	FG3
102	83	-	VSS																												
103	84	-	VCC																												
104	85	61	PD14		EIRQ14		GPO	ADC1_ADTRG			TMRA_4_PWM3	TMRA_11_PWM3		USART9_CTS	TMR6_1_PWMZ				EXMC_DATA0		EVNTP414	EVENTOUT		I2S4_EXCK					PLU2_IND	PLU3_OUT	FG3
105	86	62	PD15		EIRQ15		GPO	ADC2_ADTRG			TMRA_4_PWM4	TMRA_11_PWM4		USART9_CK	TMR6_2_PWMZ				EXMC_DATA1		EVNTP415	EVENTOUT		I2S4_MCK					PLU3_INA	PLU0_OUT	FG3
106	87	-	PG2		EIRQ2		GPO	ADC3_ADTRG							TMR6_5_PWMZ				EXMC_ADD12			EVENTOUT							PLU3_INB	PLU1_OUT	FG3
107	88	-	PG3		EIRQ3		GPO						TMRA_9_TRIG						EXMC_ADD13	DVP_DATA10		EVENTOUT							PLU3_INC	PLU2_OUT	FG3
108	89	-	PG4		EIRQ4		GPO				TMRA_9_PWM1/ TMRA_9_CLKA								EXMC_ADD14	EXMC_ADD16_DMC_ BA0_NFC_CLE		EVENTOUT						EXMC_ADD14_DMC_BA 0	PLU3_IND	PLU3_OUT	FG3
109	90	-	PG5		EIRQ5		GPO				TMRA_9_PWM2/ TMRA_9_CLKB								EXMC_ADD15	EXMC_ADD17_DMC_ BA1_NFC_ALE		EVENTOUT						EXMC_ADD15_DMC_BA 1	PLU0_INA	PLU0_OUT	FG3
110	91	-	PG6		EIRQ6		GPO				TMRA_9_PWM3				TMR6_7_PWMZ				EXMC_RB0	DVP_DATA12		EVENTOUT							PLU0_INB	PLU1_OUT	FG3
111	92	-	PG7		EIRQ7		GPO				TMRA_9_PWM4			USART8_CK	TMR6_1_PWMZ				EXMC_RB1	DVP_DATA13		EVENTOUT		I2S1_EXCK			USART6_CK		PLU0_INC	PLU2_OUT	FG3
112	93	-	PG8		EIRQ8		GPO							USART8_RTS/ USART8_DE	TMR6_2_PWMZ			ETH_PPS_OUT	EXMC_CLK			EVENTOUT		I2S1_SDIN		SPI6_NSS0	USART6_RTS/ USART6_DE	EXMC_DMC_CLK	PLU0_IND	PLU3_OUT	FG3
113	94	-	VSS																												
114	95	-	VCC																												
115	96	63	PC6		EIRQ6		GPO	CTCREF	TMR4_2_OUH		TMRA_3_PWM1/ TMRA_3_CLKA	TMRA_11_PWM4	TMR6_5_PWMA		KEYOUT3	SDIO1_D6				DVP_DATA0	EVNTP306	EVENTOUT	TMR4_3_ADSM	I2S1_MCK	QSPI_SCK		USART6_TX		PLU1_INA	PLU0_OUT	FG3
116	97	64	PC7		EIRQ7		GPO		TMR4_2_OVH	TMR6_TRIGD	TMRA_3_PWM2/ TMRA_3_CLKB	TMRA_11_PWM3	TMR6_6_PWMA		KEYOUT2	SDIO1_D7			I2S2_EXCK	DVP_DATA1	EVNTP307	EVENTOUT	TMR4_2_CLK	I2S2_MCK	QSPI_NSS		USART6_RX		PLU1_INB	PLU1_OUT	FG3
117	98	65	PC8		EIRQ8		GPO		TMR4_2_OWH	TMR6_8_PWMA	TMRA_3_PWM3	TMRA_11_PWM2/ TMRA_11_CLKB	TMR6_7_PWMA	USART8_CK	KEYOUT1	SDIO1_D0				DVP_DATA2	EVNTP308	EVENTOUT		I2S2_MCK			USART6_CK		PLU1_INC	PLU2_OUT	FG2
118	99	66	PC9		EIRQ9		GPO	MCO_2	TMR4_2_OWL	TMR6_8_PWMB	TMRA_3_PWM4	TMRA_11_PWM1/ TMRA_11_CLKA	TMR6_8_PWMA		KEYOUT0	SDIO1_D1	USBFS_DRVVBUS		EXMC_CLE	DVP_DATA3	EVNTP309	EVENTOUT		I2S3_EXCK					PLU1_IND	PLU3_OUT	FG2
119	100	67	PA8		EIRQ8+ WKUP2_0		GPO	MCO_1	TMR4_1_OUH	TMR6_1_PWMA	TMRA_1_PWM1/ TMRA_1_CLKA		TMRA_7_TRIG	USART4_CK		SDIO1_D1	USBFS_SOF				EVNTP108	EVENTOUT	TMR2_1_CLKA	I2S3_MCK			USART1_CK		PLU2_INA	PLU0_OUT	FG2
120	101	68	PA9		EIRQ9+ WKUP2_1		GPO		TMR4_1_OVH	TMR6_2_PWMA	TMRA_1_PWM2/ TMRA_1_CLKB		TMRA_2_TRIG			SDIO1_D2	USBFS_VBUS			DVP_DATA0	EVNTP109	EVENTOUT	TMR2_1_CLKB	I2S3_SDIN			USART1_TX		PLU2_INB	PLU1_OUT	FG2
121	102	69	PA10		EIRQ10+ WKUP2_2		GPO		TMR4_1_OWH	TMR6_3_PWMA	TMRA_1_PWM3	TMRA_5_TRIG	TMRA_11_TRIG			SDIO1_CD	USBFS_ID			DVP_DATA1	EVNTP110	EVENTOUT	TMR2_1_PWMA/ TMR2_1_TRIGA				USART1_RX		PLU2_INC	PLU2_OUT	FG2
122	103	70	PA11	USBFS_DM	EIRQ11+ WKUP2_3		GPO		TMR4_1_CLK	TMR6_4_PWMA	TMRA_1_PWM4		EMB_IN1	USART4_CTS		SDIO2_CD					EVNTP111	EVENTOUT	TMR2_1_PWMA/ TMR2_1_TRIGA				USART1_CTS		PLU2_IND	PLU3_OUT	FG2
123	104	71	PA12	USBFS_DP	EIRQ12+ WKUP3_0		GPO		TMR4_3_OWL	TMR6_TRIGA	TMRA_1_TRIG	TMRA_6_PWM1/ TMRA_6_CLKA		USART4_RTS/ USART4_DE	TMR6_7_PWMZ	SDIO2_WP					EVNTP112	EVENTOUT	TMR4_1_CLK				USART1_RTS/ USART1_DE		PLU3_INA	PLU0_OUT	FG2
124	105	72	PA13		EIRQ13	JTMS_SWDIO	GPO			TMR6_TRIGD	TMRA_8_PWM1/ TMRA_8_CLKA	TMRA_6_PWM2/ TMRA_6_CLKB			TMR6_3_PWMZ	SDIO2_D3				ERMU_EOUT3M	EVNTP113	EVENTOUT			SPI2_NSS1			EXMC_NFC_CE5	PLU3_INB	PLU1_OUT	FG2
125	106	73	VCAP_2																												
126	107	74	VSS																												
127	108	75	VCC																												
128	-	-	PH13		EIRQ13	ERMU_EOUT0M	GPO		TMR4_2_OUL	TMR6_5_PWMB	TMRA_6_PWM1/ TMRA_6_CLKA								EXMC_DATA21			EVENTOUT							PLU3_INC	PLU2_OUT	FG1

LQFP 176	LQFP 144	LQFP 100	Pin Name	Analog	EIRQ/ WKUP	TRACE/JTAG/ ERMU	Func0 GPO	Func1 other	Func2 TMR4	Func3 TMR6	Func4 TMRA	Func5 TMRA	Func6 EMB,TMR6,TMRA	Func7 USART	Func8 KEYSCAN,TMR6	Func9 SDIO	Func10 USBFS,USBHS,TMR2	Func11 ETH	Func12 EXMC,USBHS	Func13 DVP,ERMU,EXMC	Func14 EVNTPT	Func15 EVENTOUT	Func16 TMR2,TMR4	Func17 I2S	Func18 SPI,QSPI	Func19 SPI	Func20 USART	Func21 EXMC	Func22 PLU_IN	Func23 PLU_OUT	Func28~63 Func Group
129	-	-	PH14		EIRQ14		GPO		TMR4_2_OVL	TMR6_6_PWMB	TMRA_6_PWM2/ TMRA_6_CLKB								EXMC_DATA22	DVP_DATA4		EVENTOUT							PLU3_IND	PLU3_OUT	FG1
130	-	-	PH15		EIRQ15		GPO		TMR4_2_OWL	TMR6_7_PWMB									EXMC_DATA23	DVP_DATA11		EVENTOUT							PLU0_INA	PLU0_OUT	FG1
131	-	-	PI0		EIRQ0		GPO					TMRA_5_PWM4			TMR6_3_PWMZ				EXMC_DATA24	DVP_DATA13		EVENTOUT			SPI2_NSS0				PLU0_INB	PLU1_OUT	FG1
132	-	-	PI1		EIRQ1		GPO						TMRA_8_TRIG						EXMC_DATA25	DVP_DATA8		EVENTOUT							PLU0_INC	PLU2_OUT	FG1
133	-	-	PI2		EIRQ2		GPO			TMR6_8_PWMB									EXMC_DATA26	DVP_DATA9		EVENTOUT		I2S1_SDIN					PLU0_IND	PLU3_OUT	FG1
134	-	-	PI3		EIRQ3		GPO		TMR4_2_CLK	TMR6_TRIGD					TMR6_4_PWMZ				EXMC_DATA27	DVP_DATA10		EVENTOUT							PLU1_INA	PLU0_OUT	FG1
135	-	-	VSS																												
136	-	-	VCC																												
137	109	76	PA14		EIRQ14+ WKUP3_2	JTCK_SWCLK	GPO		TMR4_2_ADSM	TMR6_TRIGC	TMRA_8_PWM2/ TMRA_8_CLKB	TMRA_6_PWM3	TMRA_4_TRIG	USART2_RTS/ USART2_DE	TMR6_4_PWMZ	SDIO2_D2				ERMU_EOUT3C	EVNTP114	EVENTOUT		I2S1_EXCK	SPI2_NSS2			EXMC_SMC_BAA_NFC_ WP	PLU1_INB	PLU1_OUT	FG1
138	110	77	PA15		EIRQ15+ WKUP3_3	JTDI	GPO		TMR4_2_PCT	TMR6_TRIGA	TMRA_2_PWM1/ TMRA_2_CLKA	TMRA_6_PWM4	TMRA_2_TRIG	USART2_CTS	TMR6_1_PWMZ	SDIO2_D1					EVNTP115	EVENTOUT		I2S1_MCK	SPI2_NSS3	SPI1_NSS0			PLU1_INC	PLU2_OUT	FG1
139	111	78	PC10		EIRQ10		GPO	CAN1_TST_SAM-PLE	TMR4_3_OUH	TMR6_5_PWMA	TMRA_8_PWM3	TMRA_5_PWM1/ TMRA_5_CLKA	TMRA_9_TRIG	USART2_CK		SDIO1_D2				DVP_DATA8	EVNTP310	EVENTOUT		I2S2_CK	SPI1_NSS1	SPI3_SCK	USART4_TX		PLU1_IND	PLU3_OUT	FG3
140	112	79	PC11		EIRQ11		GPO	CAN1_TST_CLOCK	TMR4_3_OVH	TMR6_6_PWMA	TMRA_8_PWM4	TMRA_5_PWM2/ TMRA_5_CLKB	TMRA_9_PWM1/ TMRA_9_CLKA		KEYOUT0	SDIO1_D3				DVP_DATA4	EVNTP311	EVENTOUT	TMR2_4_PWMA/ TMR2_4_TRIGA	I2S2_SDIN	SPI1_NSS2	SPI3_MISO	USART4_RX		PLU2_INA	PLU0_OUT	FG3
141	113	80	PC12		EIRQ12		GPO		TMR4_3_OWH	TMR6_7_PWMA	TMRA_4_TRIG	TMRA_5_PWM3	TMRA_9_PWM2/ TMRA_9_CLKB	USART3_CK	KEYOUT1	SDIO1_CK				DVP_DATA9	EVNTP312	EVENTOUT	TMR2_4_PWMB/ TMR2_4_TRIGB	I2S2_SD	SPI1_NSS3	SPI3_MOSI	USART5_TX		PLU2_INB	PLU1_OUT	FG3
142	114	81	PD0		EIRQ0		GPO	CMP_VCOUT	TMR4_3_OUL	TMR6_5_PWMB		TMRA_5_PWM4	TMRA_9_PWM3	USART8_CTS	KEYOUT2				EXMC_DATA2		EVNTP400	EVENTOUT	TMR2_4_CLKA						PLU2_INC	PLU2_OUT	FG3
143	115	82	PD1		EIRQ1		GPO		TMR4_3_OVL	TMR6_6_PWMB	TMRA_3_TRIG	TMRA_12_PWM1/ TMRA_12_CLKA	TMRA_9_PWM4	USART8_RTS/ USART8_DE	KEYOUT3				EXMC_DATA3		EVNTP401	EVENTOUT	TMR2_4_CLKB						PLU2_IND	PLU3_OUT	FG3
144	116	83	PD2		EIRQ2		GPO	CMP4_VCOUT	TMR4_3_OWL	TMR6_7_PWMB	TMRA_2_PWM4	TMRA_12_PWM2/ TMRA_12_CLKB	TMRA_3_TRIG	USART7_CTS	KEYOUT4	SDIO1_CMD				DVP_DATA11	EVNTP402	EVENTOUT					USART5_RX	EXMC_SMC_CRE	PLU3_INA	PLU0_OUT	FG3
145	117	84	PD3		EIRQ3		GPO	CMP1_VCOUT				TMRA_12_PWM3	TMRA_6_TRIG	USART5_CTS	KEYOUT5				EXMC_CLK	DVP_DATA5	EVNTP403	EVENTOUT				SPI2_SCK	USART2_CTS	EXMC_SMC_CLK	PLU3_INB	PLU1_OUT	FG3
146	118	85	PD4		EIRQ4		GPO	CMP2_VCOUT			TMRA_6_PWM1/ TMRA_6_CLKA	TMRA_12_PWM4	EMB_IN4	USART5_RTS/ USART5_DE	KEYOUT6				EXMC_OE	DVP_DATA12	EVNTP404	EVENTOUT					USART2_RTS/ USART2_DE	EXMC_SMC_OE_NFC_RE	PLU3_INC	PLU2_OUT	FG2
147	119	86	PD5		EIRQ5		GPO	CMP3_VCOUT			TMRA_6_PWM2/ TMRA_6_CLKB			USART7_RTS/ USART7_DE	KEYOUT7				EXMC_WE		EVNTP405	EVENTOUT			SPI6_NSS1		USART2_TX	EXMC_SMC_NFC_WE	PLU3_IND	PLU3_OUT	FG2
148	120	-	VSS																												
149	121	-	VCC																												
150	122	87	PD6		EIRQ6		GPO	ADC1_ADTRG	TMR4_2_CLK	TMR6_TRIGC	TMRA_6_PWM3			USART7_CK	TMR6_5_PWMZ				EXMC_RB0	DVP_DATA10	EVNTP406	EVENTOUT		I2S2_SD	SPI6_NSS2	SPI3_MOSI	USART2_RX		PLU0_INA	PLU0_OUT	FG2
151	123	88	PD7		EIRQ7		GPO	ADC2_ADTRG		TMR6_TRIGD	TMRA_6_PWM4		EMB_IN1	USART5_CK	TMR6_7_PWMZ				EXMC_CE0		EVNTP407	EVENTOUT			SPI6_NSS3		USART2_CK	EXMC_SMC_NFC_CS0	PLU0_INB	PLU1_OUT	FG2
152	124	-	PG9		EIRQ9		GPO	ADC3_ADTRG				TMRA_12_PWM1/ TMRA_12_CLKA		USART4_CK					EXMC_CE1	DVP_VSYNC		EVENTOUT						EXMC_SMC_NFC_CS1	PLU0_INC	PLU2_OUT	FG2
153	125	-	PG10		EIRQ10		GPO		TMR4_3_ADSM	TMR6_8_PWMA		TMRA_12_PWM2/ TMRA_12_CLKB		USART4_CTS					EXMC_CE2	DVP_DATA2		EVENTOUT						EXMC_SMC_NFC_CS2	PLU0_IND	PLU3_OUT	FG2
154	126	-	PG11		EIRQ11		GPO		TMR4_3_PCT	TMR6_8_PWMB	TMRA_8_PWM1/ TMRA_8_CLKA			USART4_RTS/ USART4_DE				ETH_MII_RMII_TXEN	EXMC_RB7	DVP_DATA3		EVENTOUT							PLU1_INA	PLU0_OUT	FG2
155	127	-	PG12		EIRQ12		GPO				TMRA_8_PWM2/ TMRA_8_CLKB			USART6_RTS/ USART6_DE					EXMC_CE3			EVENTOUT						EXMC_SMC_NFC_CS3	PLU1_INB	PLU1_OUT	FG2
156	128	-	PG13		EIRQ13		GPO				TMRA_8_PWM3			USART6_CTS	TMR6_3_PWMZ			ETH_MII_RMII_TXD0	EXMC_ADD24	DVP_VSYNC		EVENTOUT							PLU1_INC	PLU2_OUT	FG2
157	129	-	PG14		EIRQ14		GPO		TMR4_3_ADSM	TMR6_4_PWMB	TMRA_8_PWM4							ETH_MII_RMII_TXD1	EXMC_ADD25	DVP_DATA2		EVENTOUT		I2S3_EXCK					PLU1_IND	PLU3_OUT	FG2
158	130	-	VSS																												
159	131	-	VCC																												
160	132	-	PG15		EIRQ15		GPO		TMR4_3_PCT	TMR6_4_PWMA			TMRA_5_TRIG	USART6_CTS					EXMC_BAA	DVP_DATA13		EVENTOUT		I2S3_MCK				EXMC_DMC_CAS	PLU2_INA	PLU0_OUT	FG1
161	133	89	PB3		EIRQ3+ WKUP0_3	JTDO_TRACE-SWO	GPO	FCMREF	TMR4_3_CLK	TMR6_TRIGC	TMRA_2_PWM2/ TMRA_2_CLKB	TMRA_12_PWM1/ TMRA_12_CLKA			TMR6_2_PWMZ	SDIO2_D0					EVNTP203	EVENTOUT							PLU2_INB	PLU1_OUT	FG1
162	134	90	PB4		EIRQ4+ WKUP1_0	NJTRST	GPO		TMR4_3_OWL	TMR6_3_PWMB	TMRA_3_PWM1/ TMRA_3_CLKA	TMRA_12_PWM2/ TMRA_12_CLKB				SDIO1_D0				DVP_DATA13	EVNTP204	EVENTOUT		I2S2_SDIN					PLU2_INC	PLU2_OUT	FG1
163	135	91	PB5		EIRQ5+ WKUP1_1		GPO	ADC3_ADTRG	TMR4_3_OWH	TMR6_3_PWMA	TMRA_3_PWM2/ TMRA_3_CLKB	TMRA_12_PWM3	TMRA_10_TRIG			SDIO1_D3	USBHS_ULPI_D7	ETH_PPS_OUT	EXMC_ALE	DVP_DATA10	EVNTP205	EVENTOUT		I2S4_EXCK	SPI3_NSS3			EXMC_DMC_CKE	PLU2_IND	PLU3_OUT	FG1
164	136	92	PB6		EIRQ6+ WKUP1_2		GPO	ADC2_ADTRG	TMR4_3_OVL	TMR6_2_PWMB	TMRA_4_PWM1/ TMRA_4_CLKA	TMRA_12_PWM4	TMRA_10_PWM1 /TMRA_10_CLKA			SDIO2_CK		ETH_MII_TXCLK	EXMC_CE1	DVP_DATA5	EVNTP206	EVENTOUT		I2S4_MCK	SPI3_NSS2			EXMC_DMC_CS3	PLU3_INA	PLU0_OUT	FG1
165	137	93	PB7		EIRQ7+ WKUP1_3		GPO	ADC1_ADTRG	TMR4_3_OVH	TMR6_2_PWMA	TMRA_4_PWM2/ TMRA_4_CLKB		TMRA_10_PWM2 /TMRA_10_CLKB			SDIO1_D0		ETH_MII_TXER	EXMC_ADV	DVP_VSYNC	EVNTP207	EVENTOUT		I2S2_EXCK	SPI3_NSS1			EXMC_SMC_ADV	PLU3_INB	PLU1_OUT	FG1
166	138	94	PI13/MD				GPO							USART3_TX																	
167	139	95	PB8		EIRQ8		GPO		TMR4_3_OUL	TMR6_1_PWMB	TMRA_4_PWM3		TMRA_10_PWM3	USART1_CK	KEYOUT7	SDIO1_D4	USBFS_DRVVBUS	ETH_MII_TXD3		DVP_DATA6	EVNTP208	EVENTOUT	TMR2_3_PWMA/ TMR2_3_TRIGA	I2S2_MCK	SPI2_NSS0				PLU3_INC	PLU2_OUT	FG1
168	140	96	PB9		EIRQ9		GPO		TMR4_3_OUH	TMR6_1_PWMA	TMRA_4_PWM4	TMRA_6_TRIG	TMRA_10_PWM4	USART1_CTS	KEYOUT6	SDIO1_D5		ETH_MII_TXD2		DVP_DATA7	EVNTP209	EVENTOUT	TMR2_3_PWMB/ TMR2_3_TRIGB	I2S2_SDIN	SPI2_NSS1	SPI2_NSS0			PLU3_IND	PLU3_OUT	FG1
169	141	97	PE0		EIRQ0		GPO	MCO_1	TMR4_3_PCT		TMRA_4_TRIG		TMRA_2_TRIG	USART1_RTS/ USART1_DE				ETH_MII_RMII_TXD1	EXMC_CE4	DVP_DATA2		EVENTOUT	TMR2_3_CLKA		SPI2_NSS2		USART8_RX	EXMC_SMC_DMC_BLS0	PLU0_INA	PLU0_OUT	FG1
170	142	98	PE1		EIRQ1		GPO	MCO_2	TMR4_3_CLK	TMR6_TRIGC			TMRA_12_TRIG		TMR6_5_PWMZ			ETH_MII_RMII_TXD0	EXMC_CE5	DVP_DATA3		EVENTOUT	TMR2_3_CLKB		SPI2_NSS3		USART8_TX	EXMC_SMC_DMC_BLS1	PLU0_INB	PLU1_OUT	FG1
171	143	-	PI12		EIRQ12		GPO								TMR6_4_PWMZ				EXMC_CLE									EXMC_NFC_CE4	PLU0_INC	PLU2_OUT	FG1
-	-	99	VSS																												
172	144	100	VCC																												
173	-	-	PI4		EIRQ4		GPO				TMRA_1_PWM1/ TMRA_1_CLKA		EMB_IN4						EXMC_CE6	DVP_DATA5		EVENTOUT						EXMC_SMC_DMC_BLS2	PLU0_IND	PLU3_OUT	FG1
174	-	-	PI5		EIRQ5		GPO		TMR4_2_OUH	TMR6_5_PWMA	TMRA_1_PWM2/ TMRA_1_CLKB								EXMC_CE7	DVP_VSYNC		EVENTOUT						EXMC_SMC_DMC_BLS3	PLU1_INA	PLU0_OUT	FG1
175	-	-	PI6		EIRQ6		GPO		TMR4_2_OVH	TMR6_6_PWMA	TMRA_1_PWM3								EXMC_DATA28	DVP_DATA6		EVENTOUT							PLU1_INB	PLU1_OUT	FG1

LQFP 176	LQFP 144	LQFP 100	Pin Name	Analog	EIRQ/ WKUP	TRACE/JTAG/ ERMU	Func0 GPO	Func1 other	Func2 TMR4	Func3 TMR6	Func4 TMRA	Func5 TMRA	Func6 EMB,TMR6,TMRA	Func7 USART	Func8 KEYSCAN,TMR6	Func9 SDIO	Func10 USBFS,USBHS,TMR2	Func11 ETH	Func12 EXMC,USBHS	Func13 DVP,ERMU,EXMC	Func14 EVNTPT	Func15 EVENTOUT	Func16 TMR2,TMR4	Func17 I2S	Func18 SPI,QSPI	Func19 SPI	Func20 USART	Func21 EXMC	Func22 PLU_IN	Func23 PLU_OUT	Func28~63 Func Group
176	-	-	PI7		EIRQ7		GPO		TMR4_2_OWH	TMR6_7_PWMA	TMRA_1_PWM4								EXMC_DATA29	DVP_DATA7		EVENTOUT							PLU1_INC	PLU2_OUT	FG1

Func28-63 are serial communication functions (including CAN, MCAN, USART, SPI, I2C, I2S), divided into 3 Function Groups (FG1, FG2, FG3). Detailed correspondence is shown in the following table.

Table 3-2 Func28-63 Table

	Func28	Func29	Func30	Func31	Func32	Func33	Func34	Func35	Func36	Func37	Func38	Func39	Func40	Func41
FG1	MCAN1_TX	MCAN1_RX	MCAN2_TX	MCAN2_RX	USART1_TX	USART1_RX	USART2_TX	USART2_RX	USART3_TX	USART3_RX	USART4_TX	USART4_RX	SPI1_SCK	SPI1_MOSI
FG2	MCAN1_TX	MCAN1_RX	MCAN2_TX	MCAN2_RX	USART4_TX	USART4_RX	USART5_TX	USART5_RX	USART6_TX	USART6_RX	USART7_TX	USART7_RX	SPI4_SCK	SPI4_MOSI
FG3	MCAN1_TX	MCAN1_RX	MCAN2_TX	MCAN2_RX	USART3_TX	USART3_RX	USART8_TX	USART8_RX	USART9_TX	USART9_RX	USART10_TX	USART10_RX	SPI1_SCK	SPI1_MOSI
	Func42	**Func43**	**Func44**	**Func45**	**Func46**	**Func47**	**Func48**	**Func49**	**Func50**	**Func51**	**Func52**	**Func53**	**Func54**	**Func55**
FG1	SPI1_MISO	SPI2_SCK	SPI2_MOSI	SPI2_MISO	SPI3_SCK	SPI3_MOSI	SPI3_MISO	SPI3_NSS0	I2C1_SDA	I2C1_SCL	I2C3_SDA	I2C3_SCL	I2S1_CK	I2S1_WS
FG2	SPI4_MISO	SPI5_SCK	SPI5_MOSI	SPI5_MISO	SPI6_SCK	SPI6_MOSI	SPI6_MISO	SPI6_NSS0	I2C2_SDA	I2C2_SCL	I2C4_SDA	I2C4_SCL	I2C5_SDA	I2C5_SCL
FG3	SPI1_MISO	SPI4_SCK	SPI4_MOSI	SPI4_MISO	SPI4_NSS0	SPI1_NSS0	I2C1_SDA	I2C1_SCL	I2C2_SDA	I2C2_SCL	I2C6_SDA	I2C6_SCL	I2S1_CK	I2S1_WS
	Func56	**Func57**	**Func58**	**Func59**	**Func60**	**Func61**	**Func62**	**Func63**						
FG1	I2S1_SD	I2S2_CK	I2S2_WS	I2S2_SD	CAN1_TX	CAN1_RX	CAN2_TX	CAN2_RX						
FG2	-	I2S3_CK	I2S3_WS	I2S3_SD	CAN1_TX	CAN1_RX	CAN2_TX	CAN2_RX						
FG3	I2S1_SD	I2S4_CK	I2S4_WS	I2S4_SD	CAN1_TX	CAN1_RX	CAN2_TX	CAN2_RX						

Table 3-3 Port Configuration

Package	Port Group	Bits																Pin Count Total	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
LQFP176	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	142
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortE	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortF	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortG	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortH	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortI	-	-	o	o	o	o	o	o	o	o	o	o	o	o	o	o	14	
LQFP144	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	116
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortE	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortF	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortG	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	2	
	PortI	-	-	o	o	-	-	-	-	-	-	-	-	-	-	-	-	2	
LQFP100	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	83
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortE	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	2	
	PortI	-	-	o	-	-	-	-	-	-	-	-	-	-	-	-	-	1	

Table 3-4 General Functional Specifications

Port		Pull-Up	Open-Drain Output	Driving Capacity	5V Tolerant
PortA	PA0-PA10 PA13-PA15	Support	Support	Low/Medium/High	Support
	PA11, PA12	Support	Support	Low/Medium/High	Not supported
PortB	PB0-PB13	Support	Support	Low/Medium/High	Support
	PB14, PB15	Support	Support	Low/Medium/High	Not supported
PortC	PC0-PC15	Support	Support	Low/Medium/High	Support
PortD	PD0-PD15	Support	Support	Low/Medium/High	Support
PortE	PE0-PE15	Support	Support	Low/Medium/High	Support
PortF	PF0-PF15	Support	Support	Low/Medium/High	Support
PortG	PG0-PG15	Support	Support	Low/Medium/High	Support
PortH	PH0-PH15	Support	Support	Low/Medium/High	Support
PortI	PI0-PI13	Support	Support	Low/Medium/High	Support

Note

Input voltage must not be higher than VREFH/AVCC when used as an analog function.

3.3 Pin Function Description

Table 3-5 Pin Function Description

Categories	Functional Name	I/O	Description
Power	VCC	I	Power supply
	VSS	I	Power ground
	VCAP_x (x=1-2)	-	Core voltage
	AVCC	I	Analog power
	VREFH	I	Analog reference voltage
	AVSS	I	Analog power ground
	VREFL	I	Analog reference voltage
	AVSS_VREFL	I	Analog power ground, share a common reference ground pin
	VBAT	I	Backup power
System	NRST	I	Reset terminal, active low
	MD	I	Mode terminal
PVD	PVD2EXINP	I	PVD2 external input comparison voltage
Clock	XTAL_IN	I	External main clock oscillator interface
	XTAL_EXT/XTAL_OUT	IO	XTAL_EXT external clock input/external main clock oscillator interface
	XTAL32_IN	I	External sub clock (32.768kHz) oscillator interface
	XTAL32_OUT	O	
	MCO_x (x=1-2)	O	Internal clock output
GPIO	GPIOxy (x=A-H y=0-15; x=I y=0-13)	IO	General input output
EVENTOUT	EVENTOUT	O	Cortex-M4 CPU event output
EIRQ	EIRQx (x=0-15)	I	Maskable external interrupt
	WKUPx_y (x=0-3 y=0-3)	I	Power-down mode external wake-up input
Event Port	EVNTPxy (x=1-4 y=0-15)	IO	Event port input and output functions
KEYSCAN	KEYOUTx (x=0-7)	O	KEYSCAN scan output signal
JTAG/SWD	JTCK_SWCLK	I	Online debugging interface
	JTMS_SWDIO	IO	
	JTDO_TRACESWO	O	
	JTDI	I	
	NJTRST	I	

Categories	Functional Name	I/O	Description
TRACE	TRACECLK	O	Trace debug synchronous clock output
	TRACEDx (x=0-3)	O	Trace debug data output
FCM	FCMREF	I	External reference clock input for clock frequency measurement
RTC	RTC_OUT	O	1Hz clock output
	RTC_ICx (x=0-1)	I	Timestamp event input
Timer2	TMR2_x_CLKA (x=1-4)	I	Counting clock port input
	TMR2_x_CLKB (x=1-4)	I	Counting clock port input
	TMR2_x_PWMA/TMR2_x_TRIGA (x=1-4)	IO	External event trigger input or PWM port output
	TMR2_x_PWMB/TMR2_x_TRIGB (x=1-4)	IO	External event trigger input or PWM port output
Timer4	TMR4_x_CLK (x=1-3)	I	Counting clock port input
	TMR4_x_OUH (x=1-3)	IO	PWM port U-phase output
	TMR4_x_OUL (x=1-3)	IO	PWM port U-phase output
	TMR4_x_OVH (x=1-3)	IO	PWM port V-phase output
	TMR4_x_OVL (x=1-3)	IO	PWM port V-phase output
	TMR4_x_OWH (x=1-3)	IO	PWM port W-phase output
	TMR4_x_OWL (x=1-3)	IO	PWM port W-phase output
	TMR4_x_ADSM (x=1-3)	O	Special event output monitoring
	TMR4_x_PCT (x=1-3)	O	PWM periodic output monitoring
Timer6	TMR6_TRIGA	I	External event trigger A input
	TMR6_TRIGB	I	External event trigger B input
	TMR6_TRIGC	I	External event trigger C input
	TMR6_TRIGD	I	External event trigger D input
	TMR6_x_PWMZ (x=1-5, 7)	IO	External event trigger input or PWM port output
	TMR6_x_PWMA (x=1-8)	IO	External event trigger input or PWM port output
	TMR6_x_PWMB (x=1-8)	IO	External event trigger input or PWM port output

Categories	Functional Name	I/O	Description
TimerA	TMRA_x_TRIG (x=1-12)	I	External event trigger input
	TMRA_x_PWM1/TMRA_x_CLKA (x=1-12)	IO	External event trigger input or PWM port output or count clock port input
	TMRA_x_PWM2/TMRA_x_CLKB (x=1-12)	IO	External event trigger input or PWM port output or count clock port input
	TMRA_x_PWMy (x=1-12 y=3-4)	IO	External event trigger input or PWM port output
EMB	EMB_INx (x=1-4)	I	Port input control signal
USART	USARTx_TX (x=1-10)	IO	Transmit data
	USARTx_RX (x=1-10)	IO	Receiving data
	USARTx_CK (x=1-10)	IO	Communication clock
	USARTx_RTS/USARTx_DE (x=1-10)	O	Request transmiting signal/driver enable
	USARTx_CTS (x=1-10)	I	Clear transmiting signal
SPI	SPIx_MISO (x=1-6)	IO	Master input/slave output data transfer pin
	SPIx_MOSI (x=1-6)	IO	Master output/slave input data transfer pin
	SPIx_SCK (x=1-6)	IO	Transmission clock
	SPIx_NSS0 (x=1-6)	IO	Slave selection input/output pin
	SPIx_NSSy (x=1-6 y=1-3)	O	Slave selection output pin
QSPI	QSPI_IOx (x=0-3)	IO	Data line
	QSPI_SCK	O	Clock output
	QSPI_NSS	O	Slave selection
I2C	I2Cx_SCL (x=1-6)	IO	Clock line
	I2Cx_SDA (x=1-6)	IO	Data line
I2S	I2Sx_SD (x=1-4)	IO	Serial data
	I2Sx_SDIN (x=1-4)	I	Full duplex serial data input
	I2Sx_WS (x=1-4)	IO	Word selection
	I2Sx_CK (x=1-4)	IO	Serial clock
	I2Sx_EXCK (x=1-4)	I	External clock source
	I2Sx_MCK (x=1-4)	O	Master clock
CAN	CANx_TX (x=1-2)	O	Transmit data
	CANx_RX (x=1-2)	I	Receiving data

Categories	Functional Name	I/O	Description
MCAN	MCANx_TX (x=1-2)	O	Transmit data
	MCANx_RX (x=1-2)	I	Receiving data
SDIO	SDIOx_Dy (x=1-2 y=0-7)	IO	SD data signal
	SDIOx_CK (x=1-2)	O	SD clock output signal
	SDIOx_CMD (x=1-2)	IO	SD command and reply signal
	SDIOx_CD (x=1-2)	I	SD card identification status signal
	SDIOx_WP (x=1-2)	I	SD card write protection status signal
USB_FS	USBFS_DM	IO	USBFS on-chip full-speed PHY D-signal
	USBFS_DP	IO	USBFS on-chip full-speed PHY D+signal
	USBFS_VBUS	I	USBFS VBUS signal
	USBFS_ID	I	USBFS ID signal
	USBFS_SOF	O	USBFS SOF pulse output signal
	USBFS_DRVVBUS	O	USBFS VBUS driver permission signal
USB_HS	USBHS_DM	IO	USBHS on-chip full-speed PHY D-signal
	USBHS_DP	IO	USBHS on-chip full-speed PHY D+signal
	USBHS_VBUS	I	USBHS VBUS signal
	USBHS_ID	I	USBHS ID signal
	USBHS_SOF	O	USBHS SOF pulse output signal
	USBHS_DRVVBUS	O	USBHS VBUS driver permission signal
	USBHS_ULPI_CLK	I	ULPI interface clock signal
	USBHS_ULPI_DIR	I	ULPI interface dir signal
	USBHS_ULPI_STP	O	ULPI interface stp signal
	USBHS_ULPI_NXT	I	ULPI interface nxt signal
	USBHS_ULPI_Dx (x=0-7)	IO	ULPI interface data signal
ETHMAC	ETH_SMI_MDC	O	SMI interface clock
	ETH_SMI_MDIO	IO	SMI interface data
	ETH_PPS_OUT	IO	PPS output
	ETH_MII_RMII_RXCLK	I	MII receive action clock or RMII reference clock

Categories	Functional Name	I/O	Description
ETHMAC	ETH_MII_RMII_RXDV	I	MII receive data valid or RMII receive data valid
	ETH_MII_RMII_RXD0	I	MII receive data 0 or RMII receive data 0
	ETH_MII_RMII_RXD1	I	MII receive data 1 or RMII receive data 1
	ETH_MII_RMII_TXEN	O	MII transmit data enable or RMII transmit data enable
	ETH_MII_RMII_TXD0	O	MII transmit data 0 or RMII transmit data 0
	ETH_MII_RMII_TXD1	O	MII transmit data 1 or RMII transmit data 1
	ETH_MII_RXD2	I	MII receive data 2
	ETH_MII_RXD3	I	MII receive data 3
	ETH_MII_RXER	I	MII receive data error
	ETH_MII_TXCLK	I	MII transmit action clock
	ETH_MII_TXD2	O	MII transmit data 2
	ETH_MII_TXD3	O	MII transmit data 3
	ETH_MII_TXER	O	MII transmit data error
	ETH_MII_COL	I	MII carrier sense
	ETH_MII_CRS	I	MII collision detection
CMP	CMP1_VCOUT	O	CMP1 result output
	CMP2_VCOUT	O	CMP2 result output
	CMP3_VCOUT	O	CMP3 result output
	CMP4_VCOUT	O	CMP4 result output
	CMP_VCOUT	O	CMP1-4 result OR output
	CMPx_INPy (x=1-4 y=3-4; x=1, 3 y=2)	I	CMPx positive analog input
	CMPx_INM4 (x=1-4)	I	CMPx negative analog input
	CMP123_INM3	I	CMP1,2,3 negative analog input
	CMP4_INM3	I	CMP4 negative analog input
ADC	ADC1_ADTRG	I	ADC1 AD conversion external start source
	ADC2_ADTRG	I	ADC2 AD conversion external start source
	ADC3_ADTRG	I	ADC3 AD conversion external start source

Categories	Functional Name	I/O	Description
ADC	ADC123_INx (x=0-2)	I	ADC1,2,3 shared external analog input port PGA analog input SH analog input
	ADC123_INx (x=3, 10-13)	I	ADC1,2,3 shared external analog input port
	ADC12_INx (x=4, 5, 7-9, 14, 15)	I	ADC1,2 shared external analog input port
	ADC12_IN6	I	ADC1,2 shared external analog input port PGA analog input
	ADC3_INx (x=4-9, 14-19)	I	ADC3 external analog input port
	PGA123_VSS	I	PGA1-3 Ground Input
	PGA4_VSS	I	PGA4 Ground Input
DAC	DACx_OUTy (x=1-2 y=1-2)	O	DAC analog output
DVP	DVP_HSYNC	I	Line sync input port
	DVP_VSYNC	I	Frame sync input port
	DVP_PIXCLK	I	Clock input port
	DVP_DATAx (x=0-13)	I	Data input port
PLU	PLUx_INy (x=0-3 y=A-D)	I	Logic Processing Unit Input
	PLUx_OUT (x=0-3)	O	Logic Processing Unit Output
ERMU	ERMU_EOUTxM (x=0-3)	O	Error output port **Note** ERMU_EOUT0M has higher priority than other functions when configured via ICG hardware.
	ERMU_EOUTxC (x=0-3)	O	Error output port (inverted from ERMU_EOUTxM)
EXMC	EXMC_CLK	IO	For detailed information, refer to the "EXMC Port Function Configuration" section in the "External Storage Controller (EXMC) - Functional Description - Protocol Interface" chapter of the "Reference Manual".
	EXMC_OE	O	
	EXMC_WE	O	
	EXMC_CLE	O	
	EXMC_ALE	O	
	EXMC_BAA	O	
	EXMC_ADV	O	
	EXMC_CEx (x=0-7)	O	
	EXMC_RBx (x=0-7)	I	
	EXMC_DMC_CLK	IO	

Categories	Functional Name	I/O	Description
EXMC	EXMC_SMC_CLK	IO	For detailed information, refer to the "EXMC Port Function Configuration" section in the "External Storage Controller (EXMC) - Functional Description - Protocol Interface" chapter of the "Reference Manual".
	EXMC_DMC_WE	O	
	EXMC_SMC_NFC_WE	O	
	EXMC_SMC_DMC_BLSx (x=0-3)	O	
	EXMC_SMC_NFC_CSx (x=0-3)	O	
	EXMC_DMC_CSx (x=0-3)	O	
	EXMC_NFC_CEx (x=4-7)	O	
	EXMC_DMC_RAS	O	
	EXMC_SMC_OE_NFC_RE	O	
	EXMC_DMC_CAS	O	
	EXMC_SMC_BAA_NFC_WP	O	
	EXMC_SMC_ADV	O	
	EXMC_DMC_CKE	O	
	EXMC_SMC_CRE	O	
	EXMC_DMC_AP	O	
	EXMC_ADD14_DMC_BA0	IO	
	EXMC_ADD15_DMC_BA1	IO	
	EXMC_ADD16_NFC_CLE	IO	
	EXMC_ADD17_NFC_ALE	IO	
	EXMC_ADD16_DMC_BA0_NFC_CLE	IO	
	EXMC_ADD17_DMC_BA1_NFC_ALE	IO	
	EXMC_ADDx (x=0-15, 18-28)	O	
	EXMC_DATAx (x=0-31)	IO	

3.4 Pin Instructions

Table 3-6 Pin Instruction

Pin Name	Usage Notes
VCC	Power Supply. Connect to 1.8V-3.63V and place a decoupling capacitor near the VSS pin (refer to "Electrical Specifications").
VSS	Source ground, connected to 0V.
VBAT	Backup power supply: Connect to a battery or other power source. When not in use, connect to VCC with a 100nF decoupling capacitor.
VCAP_x (x=1-2)	Core Voltage. Place a capacitor near the VSS pin to stabilize the core voltage (refer to "Electrical Specifications").
AVCC	Analog Power Supply. Supply power to analog modules; connect to the same voltage as VCC (refer to "Electrical Specifications"). When not using an independent analog power supply, connect the pin to VCC and ensure it is not left floating.
AVSS	Analog Power Ground. Supply ground to analog modules; connect to the same voltage as VSS (refer to "Electrical Specifications"). When not using an independent analog power supply, connect the pin to VSS and ensure it is not left floating.
VREFL	Analog Reference Voltage. Connect to the same voltage as AVSS (refer to "Electrical Specifications"). Connect to AVSS when not in use and do not leave it floating.
VREFH	Analog Reference Voltage, do not exceed AVCC when in use. Connect to AVCC when not in use and do not leave it floating.
PI13/MD	Mode input. When NRST is released (changing from low level to high level), this pin must be fixed at low level. Recommended to connect a resistor (4.7kΩ) to VSS (pull-down).
NRST	Reset pin (NRST), active low. Resistance to VCC when not in use (pull-up).
Pxy (x=A-H y=0-15; x=I y=0-13)	General pin. When used as an input function, for 5V-tolerant pins, the input voltage should not exceed 5V; for non-5V-tolerant pins, it should not exceed VCC. When used as an analog input, the analog voltage should not exceed VREFH/AVCC. When not in use, leave floating or connect a resistor to VCC (pull-up) or VSS (pull-down).

4 Electrical Specifications

4.1 Parameter Conditions

Unless otherwise specified, all voltages are based on VSS.

4.1.1 Minimum and Maximum Values

All Minimum Values and Maximum Values are measured under the worst conditions.

Data resulted from comprehensive evaluation, and/or guaranteed by design are indicated in the table footnotes, and they will not be tested on the production line.

4.1.2 Typical Values

Unless otherwise specified, typical data are given based on T_A=25℃ and VCC=3.3V. These data are only used for design guidance and have not been tested.

4.1.3 Typical Curve

Unless otherwise specified, all typical curves are untested and are for design reference only.

4.1.4 Load Capacitance

The left of Figure 4-1 : Pin Load Condition (Left) and Input Voltage Measurement (Right) displays the load conditions used to measure the pin parameters.

4.1.5 Pin Input Voltage

The right of Figure 4-1 : Pin Load Condition (Left) and Input Voltage Measurement (Right) displays the measurement method of the input voltage on the device pin.

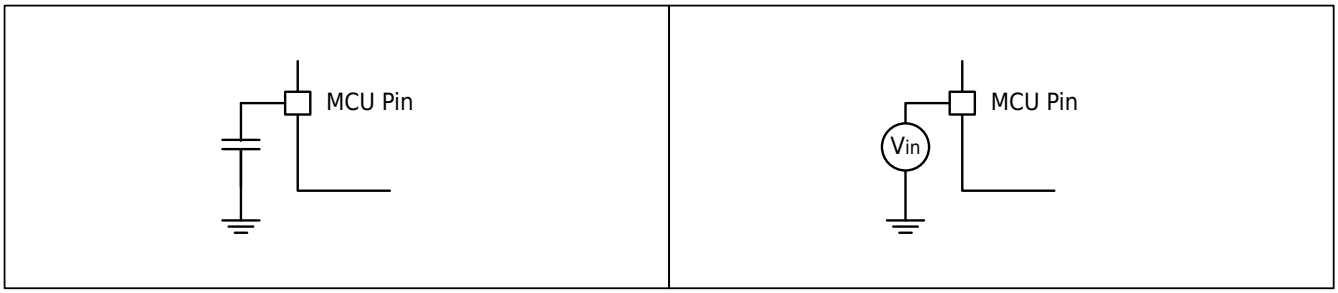


Figure 4-1 Pin Load Condition (Left) and Input Voltage Measurement (Right)

4.1.6 Power Scheme

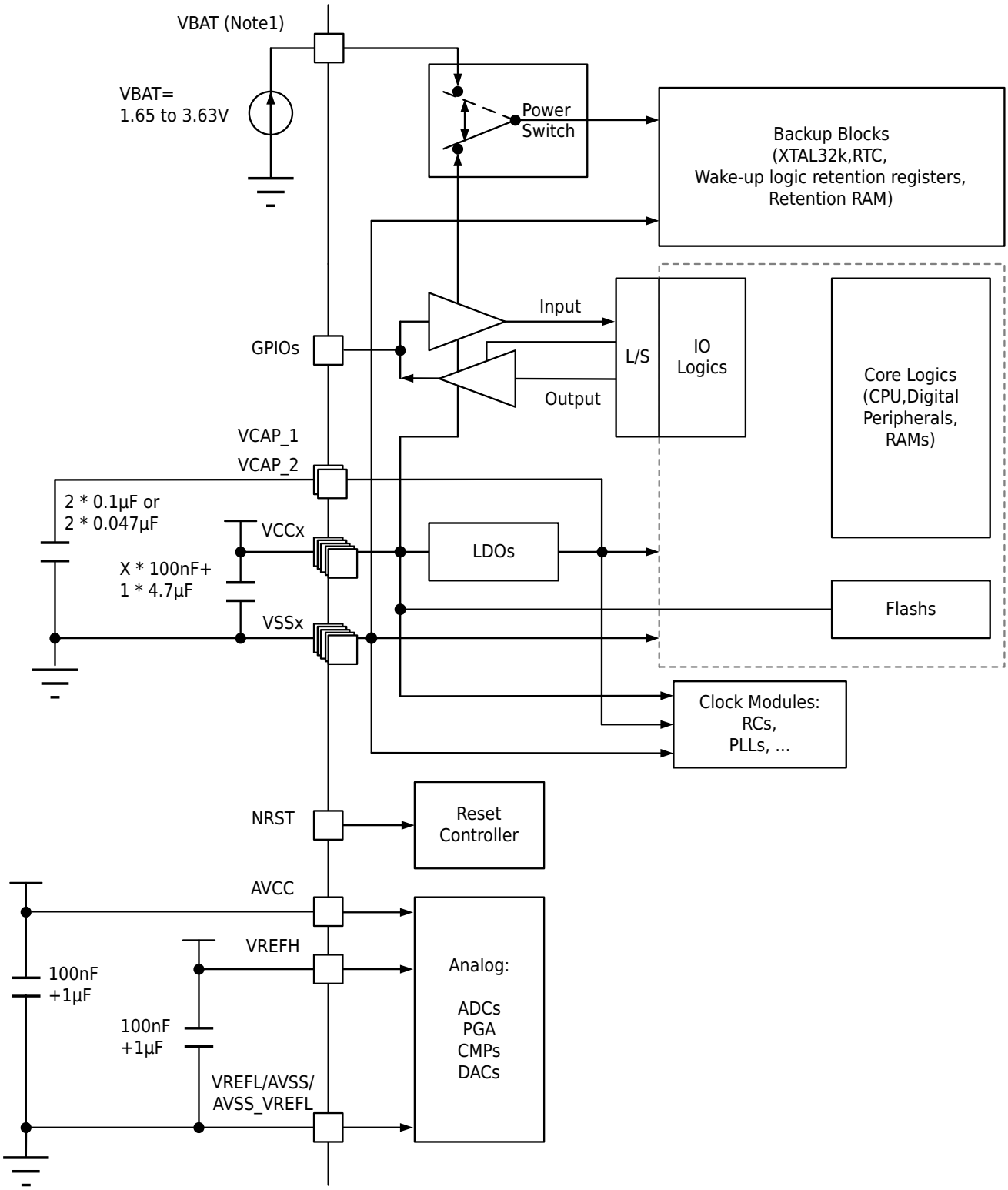


Figure 4-2 Power Scheme

Note

1. For non-rechargeable batteries, it is strongly recommended to connect a low-drop diode between the battery and the VBAT pin.
2. 4.7μF ceramic capacitor must be connected to one of VCC pins.
3. AVSS=VSS.
4. Each power supply pair (e.g. VCC/VSS, AVCC/AVSS...) must be decoupled with the above-mentioned filter ceramic capacitors. These capacitors must be as close as possible to or below that of the appropriate pins under the PCB to ensure the normal operation of the device. It is not recommended to remove the filter capacitor to reduce the size or cost of PCB, which may lead to abnormal operation of the device.
5. The capacitors used on the VCAP_1/VCAP_2 pins of the chip are as follows:
   - For chips with both VCAP_1 and VCAP_2 pins, each pin can use 0.047μF or 0.1μF capacitance (the total capacity is 0.094μF or 0.2μF). (TA: -40-105℃)
   - For chips with both VCAP_1 and VCAP_2 pins, each pin can use 0.1μF capacitance (with a total capacity of 0.2μF). (TA: -40-125℃)
   - For the chip with only VCAP_1 pin, it can use 0.1μF or 0.22μF capacitance (TA: -40-105℃)
   - Only the chip with VCAP_1 pin can use 0.22μF capacitor. (TA: -40-105℃)

   When the Power-down mode is wakened, it needs to charge VCAP_1/VCAP_2 during the process of kernel voltage establishment. On the one hand, the smaller VCAP_1/VCAP_2 total capacity can shorten the charging time and bring fast response capability to the application; on the other hand, the larger VCAP_1/VCAP_2 total capacity will prolong the charging time, but also provide stronger electromagnetic compatibility (EMC). The user can choose a larger or smaller capacitance value according to the requirements of electromagnetic compatibility and system response speed. The total capacity of VCAP_1/VCAP_2 of the chip must match the assignment of PWC_PWRC1.PDTS bit. When the total capacity of VCAP_1/VCAP_2 is 0.2μF or 0.22μF, it is necessary to ensure that the PWC_PWRC1.PDTS bit is cleared before entering Power-down mode. When the total capacity of VCAP_1/VCAP_2 is 0.094μF or 0.1μF, it is necessary to ensure that the PWC_PWRC1.PDTS bit is set before entering Power-down mode.
6. The stability of main regulator is achieved by connecting an external capacitor to VCAP_1 (or VCAP_1/VCAP_2) pin, and the capacitance value C_{EXT} is determined according to the stability requirements of the system. Capacitance values C_{EXT} and ESR are required as follows:

Table 4-1 VCAP_1/VCAP_2 Working Conditions

Symbol	Parameters	Typ	Unit
C_{EXT}	Capacitance value of external capacitance	0.047/0.1	μF
ESR	Equivalent series resistance ESR of external capacitor	<300	mΩ

4.1.7 Current Consumption Measurement

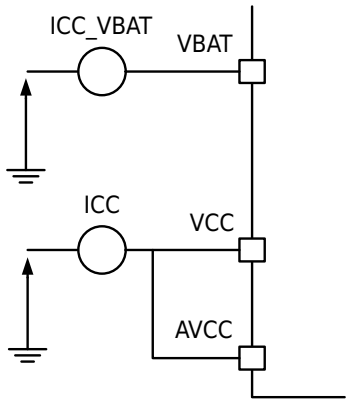


Figure 4-3 Current Consumption Measurement Solution

4.2 Absolute Maximum Ratings

If the load applied to the device exceeds the value given in the list of "Absolute Maximum Ratings", it may cause permanent damage to the device. The maximum load given here is for reference, which does not mean that the functional operation of the device is correct under this condition. Operation of the device under the condition of maximum value for a long time will affect the reliability of the device.

Table 4-2 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{CC}-V_{SS}	External main power voltage (Including AVCC, VCC and VBAT)(1)	-0.3	4.0	V
V_{IN}	Input voltage on other pins except PA11/USBFS_DM, PA12/ USBFS_DP, PB14/USBHS_DM and PB15/USBHS_DP(2)	V_{SS}-0.3	V_{CC}+4.0 (Maximum 5.8V)	V
	PA11/USBFS_DM, PA12/USBFS_DP Input voltages on the pins PB14/USBHS_DM and PB15/ USBHS_DP	V_{SS}-0.3	V_{CC}+0.7 (Maximum 4.0V)	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human model)	Please refer to "Electrical Sensitivity"		-

Note

1. All main power (VCC, AVCC, VBAT) and ground (VSS, AVSS) pins must always be connected to external power supplies within the enabled range.
2. The maximum value of V_{IN} must always be followed. For information on the maximum allowable injected current values, refer to "Table 4-3 : Current Characteristics".

Table 4-3 Current Characteristics

Symbol	Description	Max	Unit
ΣI_{VCC}	Total current flowing into all VCC_X power wires (pull current)(1)	240	mA
ΣI_{VSS}	Total current flowing out all VSS_X ground wires (sink current)(1)	-240	mA
I_{VCC}	Maximum current flowing into each VCC_X power wire (pull current)(1)	100	mA
I_{VSS}	Maximum current flowing out each VSS_X ground wire (sink current)(1)	-100	mA
I_{IO}	Output sink current on any I/O and control pins	20	mA
	Output pull current on any I/O and control pins	-20	mA
ΣI_{IO}	Total output sink current on all I/O and control pins	120	mA
	Total output pull current on all I/O and control pins	-120	mA

Note

1. All main power (VCC, AVCC, VBAT) and ground (VSS, AVSS) pins must always be connected to external power supplies within the enabled range.

Table 4-4 Temperature Characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-65-+150	℃

Symbol	Description	Value	Unit
T_J	Maximum Junction Temperature Range	-40-+150	℃

4.3 Operating Conditions

4.3.1 General Operating Conditions

Table 4-5 General Operating Conditions (HC32A4A8SITI/HC32A4A8RITI/HC32A4A8PITI)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{HCLK}	Internal AHB Clock Frequency	High Speed Mode PWRC2.DVS=0b11 PWRC2.DDAS=0b1111 PWRC3.DDAS=0xFF	-	-	240	MHz
		Ultra-low Speed Mode(1) PWRC2.DVS=0b10 PWRC2.DDAS=0b0000 PWRC3.DDAS=0x00	-	-	8	
V_{CC}(1)	Standard Operating Voltage	-	1.8	-	3.63	V
V_{AVCC}(1)(2)	Analog Operating Voltage	-	1.8	-	3.63	V
V_{BAT}(1)	Backup Operating Voltage	-	1.65	-	3.63	V
V_{IN}(1)	Input Voltage on 5V Tolerant Pin(3)(4)(5)	2V≤V_{CC}≤3.63V 2V≤V_{AVCC}≤3.63V	-0.3	-	5.5	V
		V_{CC}<2V V_{AVCC}<2V	-0.3	-	5.2	
	PA11/USBFS_DM, PA12/USBFS_DP, PB14/USBHS_DM, PB15/USBHS_DP, Pin Input Voltage	-	-0.3	-	V_{CC}+0.3	
T_J(1)	Junction Temperature Range	-	-40	-	125	℃
P_D(1)(6)	Power Consumption T_A =105℃	LQFP176	-	-	505	mW
		LQFP144	-	-	500	
		LQFP100	-	-	471	
T_A(1)	Working Temperature Range	-	-40	-	105	℃

Table 4-6 General Operating Conditions (HC32A4A8SITJ/HC32A4A8RITJ/HC32A4A8PITJ)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{HCLK}	Internal AHB Clock Frequency	High Speed Mode PWRC2.DVS=0b11 PWRC2.DDAS=0b1111 PWRC3.DDAS=0xFF	-	-	200	MHz
		Ultra-low Speed Mode(1) PWRC2.DVS=0b10 PWRC2.DDAS=0b0000 PWRC3.DDAS=0x00	-	-	8	
V_{CC}(1)	Standard Operating Voltage	-	2.7	-	3.63	V
V_{AVCC}(1)(2)	Analog Operating Voltage	-	2.7	-	3.63	V
V_{BAT}(1)	Backup Operating Voltage	-	1.65	-	3.63	V
V_{IN}(1)	Input Voltage on 5V Tolerant Pin(3)(4)(5)	2V≤V_{CC}≤3.63V 2V≤V_{AVCC}≤3.63V	–0.3	-	5.5	V
		V_{CC}<2V V_{AVCC}<2V	–0.3	-	5.2	
	PA11/USBFS_DM, PA12/USBFS_DP, PB14/USBHS_DM, PB15/USBHS_DP, Pin Input Voltage	-	–0.3	-	V_{CC}+0.3	
T_J(1)	Junction Temperature Range	-	-40	-	150	℃
P_D(1)(6)	Power consumption T_A =105℃	LQFP176	-	-	640	mW
		LQFP144	-	-	625	
		LQFP100	-	-	588	
T_A(1)	Working Temperature Range	-	-40	-	125	℃

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. If the VREFH pin is present, the following condition must be considered: 0≤V_{AVCC}-V_{REFH}≤1.2 V.
3. To keep the voltage above V_{CC}+0.3, the internal pull-up/pull-down resistors must be disabled.
4. Ensure that the power supply (VCC, AVCC) of the device is stabilized before this voltage is added to the 5V voltage-tolerant pin of the device.
5. It is forbidden to directly connect this input voltage to external power supply and grounding. It is suggested that external power supply and grounding should be connected in series through a resistor above 1kΩ.
6. If the T_A is low, a higher P_D value is permitted as long as the T_J does not exceed T_{Jmax}.

4.3.2 Working Conditions at Power On and Power Down

Table 4-7 Working Conditions at Power On and Power Down

Symbol	Parameters	Min	Max	Unit
t_{VCC}(1)	VCC rise time rate	20	20000	μs/V
	VCC fall time rate	20	20000	

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.3 Reset and Power Control Module Characteristics

Table 4-8 Reset and Power Control Module Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{BOR}	BOR Monitoring Voltage	ICG1.BOR_LEV=0b00	1.85	2.00	2.10	V
		ICG1.BOR_LEV=0b01(1)	1.96	2.10	2.20	V
		ICG1.BOR_LEV=0b10(1)	2.06	2.20	2.30	V
		ICG1.BOR_LEV=0b11	2.27	2.40	2.50	V
V_{PVD1}	PVD1 Monitoring Voltage(3)	PVD1LVL[2:0]=0b000	1.96	2.10	2.20	V
		PVD1LVL[2:0]=0b001(1)	2.06	2.20	2.30	V
		PVD1LVL[2:0]=0b010(1)	2.27	2.40	2.52	V
		PVD1LVL[2:0]=0b011(1)	2.48	2.60	2.72	V
		PVD1LVL[2:0]=0b100(1)	2.58	2.70	2.82	V
		PVD1LVL[2:0]=0b101(1)	2.69	2.80	2.92	V
		PVD1LVL[2:0]=0b110(1)	2.79	2.95	3.07	V
		PVD1LVL[2:0]=0b111	2.90	3.05	3.17	V
V_{PVD2}	PVD2 Monitoring Voltage(3)	PVD2LVL[2:0]=0b000	2.06	2.20	2.30	V
		PVD2LVL[2:0]=0b001(1)	2.27	2.40	2.50	V
		PVD2LVL[2:0]=0b010(1)	2.48	2.60	2.72	V
		PVD2LVL[2:0]=0b011(1)	2.58	2.70	2.82	V
		PVD2LVL[2:0]=0b100(1)	2.69	2.85	2.94	V
		PVD2LVL[2:0]=0b101(1)	2.79	2.95	3.07	V
		PVD2LVL[2:0]=0b110	2.90	3.05	3.17	V
		PVD2LVL[2:0]=0b111(5)	1.05	1.15	1.25	V
$V_{pvd}hyst$(1)	Hysteresis of PVD1/2(4)	-	-	100	-	mV
V_{POR}	Power On/Power Down Reset Threshold	Rising Edge VPOR	1.60	1.68	1.80	V
		Falling Edge VPDR	1.56	1.64	1.76	V
I_{RUSH}(1)	Surge Current When Voltage Regulator Powered On (POR or wake-up from Power-down)	-	-	160	250	mA

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
T_{NRST}(1)	NRST Reset Minimum Width	-	20	-	-	μs
T_{IPVD1}(2)	PVD1 Reset Release Time	-	300	380	460	μs
T_{IPVD2}(2)	PVD2 Reset Release Time	-	300	380	460	μs
T_{INRST}(2)	NRST Reset Release Time	-	25	35	50	μs
T_{RIPT}(2)	Internal Reset Time	-	140	160	200	μs
T_{RSTBOR}(2)	BOR Reset Release Time	-	440	520	610	μs
T_{RSTPOR}(2)	Power On Reset Release Time	-	-	2500	3000	μs

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. The monitoring voltage of PVD1 is the monitoring voltage when VCC voltage drops; when PVD2LVL[2:0] is set to 0b111, the PVD2 monitoring voltage is the monitoring voltage when the PVDEXINP voltage drops, and when PVD2LVD[2:0] is set to a value other than 0b111, the PVD2 monitoring voltage is the monitoring voltage when the VCC voltage drops.
4. The hysteresis of PVD1/2 is the difference between the monitoring voltages when VCC rises and falls.

   PVD1 monitoring voltage when VCC rises $=V_{PVD1}+V_{pvd}hyst$;

   PVD2 monitoring voltage when VCC rises $=V_{PVD2}+V_{pvd}hyst$.
5. When PVD2LVDL[2:0]=0b111, the comparison voltage is the external input comparison voltage of PVD2EXINP pin.

4.3.4 Supply Current Characteristics

Current consumption is affected by many parameters and factors, including operating voltage, ambient temperature, I/O pin load, device software configuration, operating frequency, I/O pin switching rate, program location in memory and running code.

Figure 4-3 : Current Consumption Measurement Solution describes the measurement method of current consumption. The measured values of current consumption in various modes described in this section are obtained by a set of test codes running in FLASH under laboratory conditions.

The specific conditions are as follows:

1. All I/O pins are in high impedance mode (no load).
2. The clock frequency selects the high-speed mode f_{HCLK}=240MHz/200MHz/120MHz/24MHz and the ultra-low-speed mode f_{HCLK}=8MHz/1MHz.
3. The power consumption modes are divided into: normal operating mode ICC_RUN, Sleep mode ICC_SLEEP, Stop mode ICC_STP, Power-down mode ICC_PD, Dhrystone operating mode ICC_DHRYSTONE and VBAT power supply mode ICC_VBAT.
4. Please refer to the specific current condition description for peripheral clock ON/OFF.
5. In high-speed mode f_{HCLK}=240MHz/200MHz/120MHz, the PLL is on in high-speed mode.

Table 4-9 High Speed Mode Current Consumption 1

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=240MHz T_A=-40℃ V_{CC}=3.3V	-	40	-	mA
	While (1), all peripherals clock ON		-	78	-	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	40	-	mA
	CACHE ON		-	43	-	mA
ICC_SLEEP	All peripherals clock OFF		-	27	-	mA
	All peripherals clock ON		-	68	-	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=240MHz T_A=25℃ V_{CC}=3.3V	-	40	-	mA
	While (1), all peripherals clock ON		-	79	-	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	41	-	mA
	CACHE ON		-	44	-	mA
ICC_SLEEP	All peripherals clock OFF		-	28	-	mA
	All peripherals clock ON		-	68	-	mA
ICC_RUN(1)	While (1), all peripherals clock OFF	f_{HCLK}=240MHz T_A=85℃ V_{CC}=1.8-3.63V	-	-	70	mA
	While (1), all peripherals clock ON		-	-	120	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	-	75	mA
	CACHE ON		-	-	78	mA
ICC_SLEEP(1)	All peripherals clock OFF		-	-	60	mA
	All peripherals clock ON		-	-	110	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=240MHz T_A=105℃ V_{CC}=1.8-3.63V	-	-	115	mA
	While (1), all peripherals clock ON		-	-	170	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	-	131	mA
	CACHE ON		-	-	134	mA
ICC_SLEEP	All peripherals clock OFF		-	-	105	mA
	All peripherals clock ON		-	-	160	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=200MHz T_A=125℃ V_{CC}=2.7-3.63V	-	-	100	mA
	While (1), all peripherals clock ON		-	-	165	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	-	125	mA
	CACHE ON		-	-	130	mA
ICC_SLEEP	All peripherals clock OFF		-	-	100	mA
	All peripherals clock ON		-	-	155	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-10 High Speed Mode Current Consumption 2(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=120MHz T_A=-40℃ V_{CC}=3.3V	-	28	-	mA
	While (1), all peripherals clock ON		-	46	-	mA
ICC_DHRYSTONE	CACHE OFF		-	22	-	mA
	CACHE ON		-	24	-	mA
ICC_SLEEP	All peripherals clock OFF		-	15	-	mA
	All peripherals clock ON		-	37	-	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=120MHz T_A=25℃ V_{CC}=3.3V	-	29	-	mA
	While (1), all peripherals clock ON		-	47	-	mA
ICC_DHRYSTONE	CACHE OFF		-	23	-	mA
	CACHE ON		-	25	-	mA
ICC_SLEEP	All peripherals clock OFF		-	16	-	mA
	All peripherals clock ON		-	37	-	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=120MHz T_A=85℃ V_{CC}=1.8-3.63V	-	-	56	mA
	While (1), all peripherals clock ON		-	-	79	mA
ICC_DHRYSTONE	CACHE OFF		-	-	56	mA
	CACHE ON		-	-	57	mA
ICC_SLEEP	All peripherals clock OFF		-	-	44	mA
	All peripherals clock ON		-	-	69	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=120MHz T_A=105℃ V_{CC}=1.8-3.63V	-	-	105	mA
	While (1), all peripherals clock ON		-	-	135	mA
ICC_DHRYSTONE	CACHE OFF		-	-	111	mA
	CACHE ON		-	-	112	mA
ICC_SLEEP	All peripherals clock OFF		-	-	95	mA
	All peripherals clock ON		-	-	130	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=120MHz T_A=125℃ V_{CC}=2.7~3.63V	-	-	113	mA
	While (1), all peripherals clock ON		-	-	143	mA
ICC_DHRYSTONE	CACHE OFF		-	-	119	mA
	CACHE ON		-	-	120	mA
ICC_SLEEP	All peripherals clock OFF		-	-	103	mA
	All peripherals clock ON		-	-	138	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-11 High Speed Mode Current Consumption 3(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=24MHz T_A=-40℃ V_{CC}=3.3V	-	8	-	mA
	While (1), all peripherals clock ON		-	14	-	mA
ICC_DHRYSTONE	CACHE OFF		-	7	-	mA
ICC_SLEEP	All peripherals clock OFF		-	5	-	mA
	All peripherals clock ON		-	14	-	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=24MHz T_A=25℃ V_{CC}=3.3V	-	8	-	mA
	While (1), all peripherals clock ON		-	15	-	mA
ICC_DHRYSTONE	CACHE OFF		-	8	-	mA
ICC_SLEEP	All peripherals clock OFF		-	6	-	mA
	All peripherals clock ON		-	14	-	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=24MHz T_A=85℃ V_{CC}=1.8-3.63V	-	-	35	mA
	While (1), all peripherals clock ON		-	-	44	mA
ICC_DHRYSTONE	CACHE OFF		-	-	38	mA
ICC_SLEEP	All peripherals clock OFF		-	-	31	mA
	All peripherals clock ON		-	-	42	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=24MHz T_A=105℃ V_{CC}=1.8-3.63V	-	-	85	mA
	While (1), all peripherals clock ON		-	-	100	mA
ICC_DHRYSTONE	CACHE OFF		-	-	90	mA
ICC_SLEEP	All peripherals clock OFF		-	-	80	mA
	All peripherals clock ON		-	-	95	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=24MHz T_A=125℃ V_{CC}=2.7~3.63V	-	-	90	mA
	While (1), all peripherals clock ON		-	-	105	mA
ICC_DHRYSTONE	CACHE OFF		-	-	95	mA
ICC_SLEEP	All peripherals clock OFF		-	-	85	mA
	All peripherals clock ON		-	-	100	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-12 Ultra-low Speed Mode Current Consumption 1

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=8MHz T_A=-40℃ V_{CC}=3.3V	-	4	-	mA
	While (1), all peripherals clock ON		-	8	-	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	3	-	mA
ICC_SLEEP	All peripherals clock OFF		-	4	-	mA
	All peripherals clock ON		-	8	-	mA

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=8MHz T_A=25℃ V_{CC}=3.3V	-	5	-	mA
	While (1), all peripherals clock ON		-	9	-	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	4	-	mA
ICC_SLEEP	All peripherals clock OFF		-	5	-	mA
	All peripherals clock ON		-	8	-	mA
ICC_RUN(1)	While (1), all peripherals clock OFF	f_{HCLK}=8MHz T_A=85℃ V_{CC}=1.8-3.63V	-	-	30	mA
	While (1), all peripherals clock ON		-	-	36	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	-	34	mA
ICC_SLEEP(1)	All peripherals clock OFF		-	-	29	mA
	All peripherals clock ON		-	-	36	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-13 Ultra-low Speed Mode Current Consumption 2(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=1MHz T_A=-40℃ V_{CC}=3.3V	-	3	-	mA
	While (1), all peripherals clock ON		-	5	-	mA
ICC_DHRYSTONE	CACHE OFF		-	2	-	mA
ICC_SLEEP	All peripherals clock OFF		-	3	-	mA
	All peripherals clock ON		-	5	-	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=1MHz T_A=25℃ V_{CC}=3.3V	-	4	-	mA
	While (1), all peripherals clock ON		-	6	-	mA
ICC_DHRYSTONE	CACHE OFF		-	3	-	mA
ICC_SLEEP	All peripherals clock OFF		-	4	-	mA
	All peripherals clock ON		-	6	-	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=1MHz T_A=85℃ V_{CC}=1.8-3.63V	-	-	29	mA
	While (1), all peripherals clock ON		-	-	33	mA
ICC_DHRYSTONE	CACHE OFF		-	-	32	mA
ICC_SLEEP	All peripherals clock OFF		-	-	29	mA
	All peripherals clock ON		-	-	33	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-14 Low Power Mode Current Consumption

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_STP	PWC_PWRC1.STPDAS=0b00	T_A=-40℃	-	350	-	μA

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
(Stop mode)	PWC_PWRC1.STPDAS=0b11	V_{CC}=3.3V	-	110	-	μA
	PWC_PWRC1.STPDAS=0b00	T_A=25℃ V_{CC}=3.3V	-	600	-	μA
	PWC_PWRC1.STPDAS=0b11		-	310	-	μA
	PWC_PWRC1.STPDAS=0b00	T_A=85℃ V_{CC}=1.8-3.63V	-	-	15	mA
	PWC_PWRC1.STPDAS=0b11		-	-	15	mA
	PWC_PWRC1.STPDAS=0b00	T_A=105℃ V_{CC}=1.8-3.63V	-	-	37	mA
	PWC_PWRC1.STPDAS=0b11		-	-	37	mA
	PWC_PWRC1.STPDAS=0b00	T_A=125℃ V_{CC}=2.7~3.63V	-	-	50	mA
ICC_PD Power-down mode	Power-down mode 1	T_A=-40℃ V_{CC}=3.3V	-	9	-	μA
	Power-down mode 2		-	4	-	μA
	Power-down mode 3		-	2	-	μA
	Power-down mode 4		-	2	-	μA
	Power-down mode 2+XTAL32+RTC(1)		-	5	-	μA
	Power-down mode 2+LRC+RTC		-	7	-	μA
	Power-down mode 2+XTAL32+RTC+Ret SRAM(1)		-	5	-	μA
	Power-down mode 1	T_A=25℃ V_{CC}=3.3V	-	11	-	μA
	Power-down mode 2		-	5	-	μA
	Power-down mode 3		-	3	-	μA
	Power-down mode 4		-	3	-	μA
	Power-down mode 2+XTAL32+RTC		-	6	-	μA
	Power-down mode 2+LRC+RTC		-	8	-	μA
	Power-down mode 2+XTAL32+RTC+Ret SRAM		-	6	-	μA
	Power-down mode 1(1)	T_A=85℃ V_{CC}=1.8-3.63V	-	-	25	μA
	Power-down mode 2(1)		-	-	17	μA
	Power-down mode 3(1)		-	-	13	μA
	Power-down mode 4(1)		-	-	13	μA
	Power-down mode 2+XTAL32+RTC(1)		-	-	18	μA
	Power-down mode 2+LRC+RTC(1)		-	-	13	μA
	Power-down mode 2+XTAL32+RTC+Ret SRAM(1)		-	-	22	μA
	Power-down mode 1	T_A=105℃ V_{CC}=1.8-3.63V	-	-	65	μA
	Power-down mode 2		-	-	57	μA
	Power-down mode 3		-	-	46	μA
	Power-down mode 4		-	-	46	μA
	Power-down mode 2+XTAL32+RTC(1)		-	-	57	μA
	Power-down mode 2+LRC+RTC		-	-	57	μA
	Power-down mode 2+XTAL32+RTC+Ret SRAM(1)		-	-	60	μA

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_PD Power-down mode	Power-down mode 1	T_A=125℃ V_{CC}=2.7-3.63V	-	-	170	μA
	Power-down mode 2		-	-	160	μA
	Power-down mode 3		-	-	156	μA
	Power-down mode 4		-	-	156	μA
	Power-down mode 2+XTAL32+RTC(1)		-	-	165	μA
	Power-down mode 2+LRC+RTC		-	-	163	μA
	Power-down mode 2+XTAL32+RTC+Ret SRAM(1)		-	-	180	μA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-15 Backup Domain Current Consumption

Symbol	Parameter(1)	Conditions	Min	Typ	Max	Unit
ICC_VBAT	VBAT Area Peripherals All OFF	T_A=-40℃ VBAT=3.3V	-	0.3	-	μA
	XTAL32 ON(2)		-	0.7	-	μA
	XTAL32 ON+ XTAL32 Filter ON(2)		-	1.0	-	μA
	XTAL32 ON + XTAL32 Filter ON + RTC Counting(2)		-	1.0	-	μA
	Ret SRAM ON		-	0.9	-	μA
	RTCLRC ON		-	3.4	-	μA
	RTCLRC ON +WKTM Counting		-	3.5	-	μA
	VBAT Area Peripherals All OFF	T_A=25℃ VBAT=3.3V	-	0.4	-	μA
	XTAL32 ON		-	1.0	-	μA
	XTAL32 ON+ XTAL32 filter on		-	1.2	-	μA
	XTAL32 ON+ XTAL32 Filter On +RTC Count		-	1.2	-	μA
	Ret SRAM ON		-	1.3	-	μA
	RTCLRC ON		-	3.6	-	μA
	RTCLRC ON +WKTM Counting		-	3.6	-	μA
	VBAT Area Peripherals All OFF(2)	T_A=85℃ VBAT=3.3V	-	-	2.7	μA
	XTAL32 ON(2)		-	-	2.7	μA
	XTAL32 ON+ XTAL32 Filter ON(2)		-	-	2.8	μA
	XTAL32 ON + XTAL32 Filter ON + RTC Counting(2)		-	-	2.8	μA
	Ret SRAM ON(2)		-	-	6.6	μA
	RTCLRC ON(2)		-	-	7.5	μA
	RTCLRC ON+WKTM Counting(2)		-	-	7.6	μA
	VBAT Area Peripherals All OFF	T_A=105℃ VBAT=3.3V	-	-	6.3	μA
	XTAL32 ON(2)		-	-	6.3	μA
	XTAL32 ON+ XTAL32 Filter ON(2)		-	-	6.4	μA

Symbol	Parameter[1]	Conditions	Min	Typ	Max	Unit
ICC_VBAT	XTAL32 ON + XTAL32 Filter ON + RTC Counting[2]	T_A=105℃ VBAT=3.3V	-	-	6.4	μA
	Ret SRAM ON		-	-	15.5	μA
	RTCLRC ON		-	-	11.2	μA
	RTCLRC ON +WKTM Counting		-	-	11.2	μA
	VBAT Area Peripherals All OFF	T_A=125℃ VBAT=3.3V	-	-	17	μA
	XTAL32 ON[2]		-	-	20	μA
	XTAL32 ON+ XTAL32 Filter ON[2]		-	-	20	μA
	XTAL32 ON + XTAL32 Filter ON + RTC Counting[2]		-	-	20	μA
	Ret SRAM ON		-	-	31	μA
	RTCLRC ON		-	-	19	μA
	RTCLRC ON +WKTM Counting		-	-	19	μA

Note

1. The unlisted VBAT power supply peripherals means they are in closed state.
2. Resulted from comprehensive evaluation, not tested in production.

Table 4-16 Analog Peripherals Current Consumption[2]

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_MODULE	XTAL oscillation mode high drive 24MHz	T_A=25℃ V_{CC}=V_{AVCC}=3.3V	-	1.8	-	mA
	Oscillation mode medium drive 16MHz		-	1.0	-	mA
	Oscillation mode low drive 10MHz		-	0.8	-	mA
	Oscillation mode ultra-low drive 8MHz		-	0.6	-	mA
	XTAL 32.768kHz		-	1.1	-	μA
	HRC		-	0.3	-	mA
	PLLH (VCO=1200MHz)		-	4.4	-	mA
	PLLH (VCO=600MHz)		-	2.7	-	mA
	PLLA (VCO=480MHz)		-	2.9	-	mA
	PLLA (VCO=240MHz)		-	1.7	-	mA
	ADC		-	1.5	-	mA
	DAC		-	0.2	-	mA
	CMP		-	0.4	-	mA
	PGA		-	0.7	-	mA
	USBFS[1]		-	6.0	-	mA

Note

1. Including the current when the control part communicates with USBPHY, with a load of 50pF.
2. Resulted from comprehensive evaluation, not tested in production.

4.3.5 Low Power Mode Wake-up Timing

Wake-up time is measured from the trigger of wake-up event to the first command executed by CPU:

- For Stop or Sleep mode: the wake-up event is WFE.
- The WKUP pin is used to wake up from Power-down, Stop and Sleep modes. All time series are measured at ambient temperature and V_{CC}=3.3V.

Table 4-17 Low Power Mode Wake-up Time(2)

Symbol	Parameters	Conditions	Typ	Max	Unit
T_{STOP1}	Wake up from Stop mode	PWC_PWRC1.VHRCSD=1 and PWC_PWRC1.VPLLSD=1, the system clock is MRC, and the program is executed on RAM.	2	5	μs
T_{STOP2}	Wake up from Stop mode	The system clock is MRC, and the program is executed on Flash.	8	15	μs
T_{PD1}(1)	Wake up from Power-down mode 1	The total capacity of VCAP_1/VCAP_2 is 0.094μF or 0.1μF.	25	35	μs
		The total capacity of VCAP_1/VCAP_2 is 0.2μF or 0.22μF.	30	40	μs
T_{PD2}(1)	Wake up from Power-down mode 2	The total capacity of VCAP_1/VCAP_2 is 0.094μF or 0.1μF.	70	80	μs
		The total capacity of VCAP_1/VCAP_2 is 0.2μF or 0.22μF.	75	85	μs
T_{PD3}(1)	Wake up from Power-down mode 3	The total capacity of VCAP_1/VCAP_2 is 0.094μF or 0.1μF.	2500	3000	μs
		The total capacity of VCAP_1/VCAP_2 is 0.2μF or 0.22μF.	2500	3000	μs
T_{PD4}(1)	Wake up from Power-down mode 4	The total capacity of VCAP_1/VCAP_2 is 0.094μF or 0.1μF.	130	140	μs
		The total capacity of VCAP_1/VCAP_2 is 0.2μF or 0.22μF.	140	150	μs

Note

1. The total capacity of VCAP_1/VCAP_2 of the chip must match the assignment of PWC_PWRC1.PDTS bit. When the total capacity of VCAP_1/VCAP_2 is 0.2μF or 0.22μF, it is necessary to ensure that the PWC_PWRC1.PDTS bit is cleared before entering Power-down mode. When the total capacity of VCAP_1/VCAP_2 is 0.094μF or 0.1μF, it is necessary to ensure that the PWC_PWRC1.PDTS bit is set before entering Power-down mode.
2. Resulted from comprehensive evaluation, not tested in production.

4.3.6 External Clock Source Characteristics

4.3.6.1 High-Speed External Clock Generated by External Source

In bypass mode, XTAL oscillator is disabled and the input pin is standard I/O. The external clock signal must consider the static characteristics of I/O.

Table 4-18 High-Speed External Clock Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{XTAL_EXT}	User external clock source frequency	-	1	-	25	MHz

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{IH_XTAL}	XTAL_EXT input pin high level voltage	-	0.8*V_{CC}	-	V_{CC}	V
V_{IL_XTAL}	XTAL_EXT input pin low level voltage	-	V_{SS}	-	0.2*V_{CC}	
$t_{r(XTAL)}$(1) $t_{f(XTAL)}$(1)	XTAL_EXT rise or fall time	-	-	-	5	ns
$Duty_{(XTAL)}$(1)	Duty period	-	40	-	60	%

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.6.2 High-Speed External Clock Generated by Crystal Oscillator/Ceramic Resonator

The high-speed external (XTAL) clock can be generated by a crystal oscillator/ceramic resonant oscillator with a frequency of 4-25MHz. In application, the resonator and load capacitor must be as close as possible to the pin of oscillator, so as to minimize the output distortion and the stabilization time. For detailed information about resonator characteristics (frequency, package, accuracy, etc.), please consult the crystal resonator manufacturer.

Table 4-19 XTAL 4-25MHz Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{XTAL_IN}(1)	Oscillator frequency	-	4	-	25	MHz
R_F	Feedback resistance	-	-	300	-	kΩ
A_{XTAL}(2)(3)	XTAL precision	-	-500	-	500	ppm
G_{mmax}(2)	Oscillator Gm	Oscillator start	4	-	-	mA/V
$t_{SU(XTAL)}$(1)(4)	Startup time	V_{CC} stable, crystal oscillator =8MHz.	-	2.0	-	ms
		V_{CC} stable, crystal oscillator =4MHz.	-	4.0	-	ms

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. This parameter depends on the resonator used in the application system.
4. $t_{SU(XTAL)}$ is the oscillation starting time, that is, the time from the software enabling XTAL to the stable 8MHz oscillation frequency. This value is measured based on a standard crystal resonator, and may vary significantly depending on the crystal oscillator manufacturer.

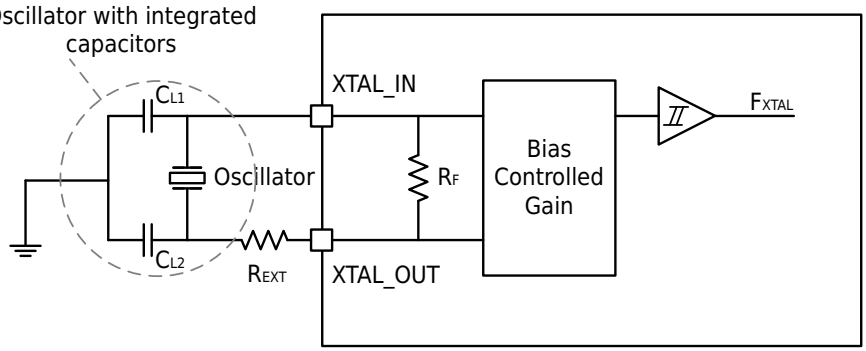


Figure 4-4 Typical application of 8MHz crystal oscillator

Note

- For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors designed for high-frequency applications, which can meet the requirements of crystal oscillator or resonator (see the figure above). C_{L1} and C_{L2} usually have the same size. $C_{L1}=C_{L2}=2*(C_L-C_S)$. C_S represents the total parasitic capacitance between the PCB and MCU pins (XTAL_IN, XTAL_OUT). C_L denotes the load capacitance of the crystal oscillator or ceramic resonator, please consult the crystal oscillator manufacturer for details.
- The damping resistor R_{EXT} is optional, and the value of the resistance depends on the crystal oscillation characteristics.

4.3.6.3 Low-Speed External Clock Generated by Crystal Oscillator/Ceramic Resonator

The low-speed external (XTAL32) clock can be generated by an oscillator composed of a crystal oscillator/ceramic resonator with a frequency of 32.768kHz. In application, the resonator and load capacitor must be as close as possible to the pin of oscillator, so as to minimize the output distortion and the stabilization time. For detailed information about resonator characteristics (frequency, package, accuracy, etc.), please consult the crystal resonator manufacturer.

Table 4-20 XTAL32 Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
F_{XTAL32} (1)	Frequency	-	-	32.768	-	kHz
R_F	Feedback resistance	-	-	15	-	MΩ
I_{DD_XTAL32} (1)	Power consumption	XTAL32DRV[2:0]=0b000	-	0.8	-	μA
A_{XTAL32} (2)(3)	XTAL32 accuracy	-	-500	-	500	ppm
G_{mmax} (2)	Oscillator G_m	XTAL32DRV[2:0]=0b000	5.6	-	-	μA/V
$T_{SUXTAL32}$ (1) (4)	Startup time	Under V_{CC} steady state	-	2	-	s

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. This parameter depends on the resonator used in the application system.
4. $T_{SUXTAL32}$ is the oscillation starting time, that is, the time from the software enabling XTAL32 to the stable 32.768kHz oscillation frequency. This value is measured based on a standard crystal resonator, and may vary significantly depending on the crystal oscillator manufacturer.

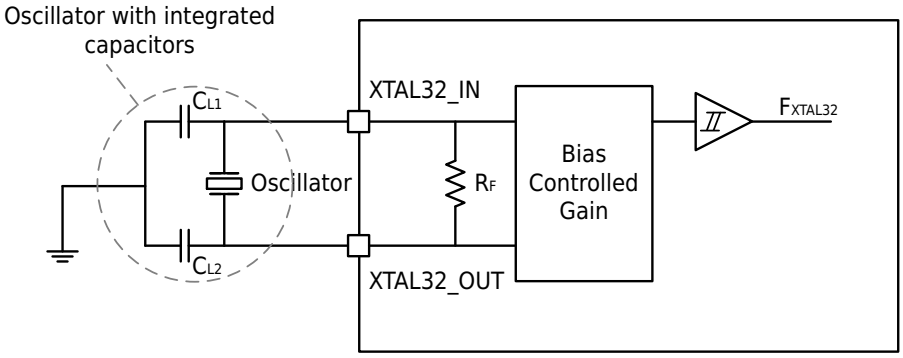


Figure 4-5 Typical application of 32.768kHz crystal oscillator

Note

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors (see the figure above). C_{L1} and C_{L2} usually have the same size, $C_{L1}=C_{L2}=2*(C_L-C_S)$. C_S represents the total parasitic capacitance between PCB and MCU pins (XTAL32_IN, XTAL32_OUT). If C_{L1} or C_{L2} is greater than 18pF, it is recommended to set XTAL32DRV=0b001 (high drive, typical power consumption increases by 0.2μA). C_L denotes the load capacitance of crystal resonator or ceramic resonator, please consult the crystal resonator manufacturer for details. When the load capacitance C_L of the crystal oscillator is selected within the range of $6pF \le C_L < 8$ pF, it is only supported when the junction temperature T_j is within the range of -40°C to 125°C. Additionally, it is necessary to set XTAL32DRV=0b010 (low drive).

4.3.7 Internal Clock Source Characteristics

4.3.7.1 HRC

Table 4-21 HRC Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{HRC}	Frequency	Mode 1	-	16	-	MHz
		Mode 2	-	20	-	
	User adjusts the scale(1)	-	-	-	0.2	%
	Frequency Accuracy	T_A=-40-125℃	-3	-	3	%
		T_A=-20-125℃(1)	-2.5	-	2.5	%
		T_A=25℃	-1.5	-	1.5	%
$t_{st(HRC)}$	HRC oscillation stabilization time	-	-	-	15	μs

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.7.2 MRC

Table 4-22 MRC Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{MRC}	Frequency	T_A=-40-105℃	7.2	8	8.8	MHz
		T_A=-40-125℃	6.8	8	9.2	MHz
$t_{st(MRC)}$	MRC oscillator stabilization time	-	-	-	3	μs

4.3.7.3 LRC

Table 4-23 LRC Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{LRC}	Frequency	-	27.853	32.768	37.683	kHz
$t_{st(LRC)}$	LRC oscillator stabilization time	-	-	-	36	μs

4.3.7.4 SWDTLRC

Table 4-24 SWDTLRC Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$f_{SWDTLRC}$	Frequency	-	9	10	11	kHz
$t_{st(SWDTLRC)}$	SWDTLRC oscillator stabilization time	-	-	-	57.1	μs

4.3.7.5 RTCLRC

Table 4-25 RTCLRC Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{RTCLRC}	Frequency	-	29.5	32.768	36	kHz
$t_{st(RTCLRC)}$	RTCLRC oscillator stabilization time	-	-	-	36	μs

4.3.8 PLL Characteristics

Table 4-26 I2S-PLL(PLLA) Main Performance Indicators

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	Input clock of PLL phase detector (PFD)	T_A=-40-105℃	1	-	25	MHz
		T_A=-40-125℃	2	-	25	MHz
f_{PLL_OUT}(1)	Output clock of PLL multiplier	-	15	-	240	MHz
f_{VCO_OUT}	PLL voltage controlled oscillator (VCO) output	-	240	-	480	MHz

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$Jitter_{PLL}$(1)	Periodic jitter	The input clock of PLL PFD is 8MHz, and the system clock is 120MHz, peak to peak.	-	±100	-	ps
	Jitter during adjacent periods	The input clock of PLL PFD is 8MHz, and the system clock is 120MHz, peak to peak.	-	±150	-	
t_{LOCK}	PLL lock time	-	-	80	120	μs

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-27 System PLL(PLLH) Main Performance Indicators

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	Input clock of PLL phase detector (PFD)	-	8	-	25	MHz
f_{PLL_OUT}(1)	Output clock of PLL multiplier	-	37.5	-	600	MHz
f_{VCO_OUT}	PLL voltage controlled oscillator (VCO) output	-	600	-	1200	MHz
$Jitter_{PLL}$(1)	Periodic jitter	The input clock of PLL PFD is 8MHz, and the system clock is 120MHz, peak to peak.	-	±70	-	ps
	Jitter during adjacent periods	The input clock of PLL PFD is 8MHz, and the system clock is 120MHz, peak to peak.	-	±100	-	ps
t_{LOCK}	PLL lock time	-	-	80	120	μs

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.9 Memory (Flash) Characteristics

When the device is delivered to the customer, the flash memory has been erased.

Table 4-28 Flash Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
I_{VCC}(1)	Supply current	Read mode, V_{CC}=1.8-3.63V	-	-	5	mA
		Programming mode, V_{CC}=1.8-3.63V	-	-	10	mA
		Block erase mode, V_{CC}=1.8-3.63V	-	-	10	mA
		Full erase mode, V_{CC}=1.8-3.63V	-	-	10	mA

Note

1. Guaranteed by design, not tested in production.

Table 4-29 Flash Programming Erase Time(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
T_{prog}	Word programming time	Single programming mode	43+2*t_{HCLK}	48+4*t_{HCLK}	53+6*t_{HCLK}	μs
	Word programming time	Continuous programming mode	12+2*t_{HCLK}	14+4*t_{HCLK}	16+6*t_{HCLK}	μs
T_{erase}	Block erase time	-	16+2*t_{HCLK}	18+4*t_{HCLK}	20+6*t_{HCLK}	ms
T_{mas}	Full erase time	-	16+2*t_{HCLK}	18+4*t_{HCLK}	20+6*t_{HCLK}	ms

Note

1. Guaranteed by design, not tested in production.
2. t_{HCLK} is 1 period of CPU clock.

Table 4-30 Flash Erase Write Cycles and Data Storage Period(1)

Symbol	Parameters	Conditions	Min	Unit
N_{end}	Program, block erase times	T_j≤125℃	10	kcycles
N_{end}	Full erase times	T_j≤125℃	10	kcycles
T_{ret}	Data storage period	T_A=85℃, after 10 kcycles	10	Year

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.10 Electrical Sensitivity

Different tests (ESD, LU) are carried out on the chip by using specific measurement methods to determine its electrical sensitivity.

4.3.10.1 ESD Characteristics

According to each pin combination, electrostatic discharge is applied to the pin of each sample. This test conforms to AEC-Q100-002 and AEC-Q100-011 standards.

Table 4-31 ESD Characteristics(1)

Symbol	Parameters	Conditions	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human model)	T_A=+25℃, compliant with AEC-Q100-002	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charging device model)	T_A=+25℃, compliant with AEC-Q100-011	500	V

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.10.2 Static Latch-up Characteristics

To evaluate the static latch-up performance, 2 complementary static Latch-up tests are needed to be performed on the chip:

- Apply overvoltage to each power supply and analog input pin.
- Apply current injection to other inputs, outputs and configurable I/O pins.

These tests conform to AEC-Q100-004 Latch-up standard.

Table 4-32 Static Latch-up Characteristics(1)

Symbol	Parameters	Conditions	Max	Unit
LU	Static Latch-up	T_A=+125℃, conforming to AEC-Q100-004 standard	100	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.11 I/O Port Characteristics

General-Purpose Input/Output Characteristics

Table 4-33 I/O Static Characteristics

Symbol	Parameters		Conditions	Min	Typ	Max	Unit
V_{IL}	Schmitt input low level		1.8≤V_{CC}≤3.63	-	-	0.2V_{CC}	V
V_{IH}	Schmitt input high level		1.8≤V_{CC}≤3.63	0.8V_{CC}	-	-	V
V_{HYS}(1)	Schmitt input hysteresis		1.8≤V_{CC}≤3.63	-	0.2	-	V
V_{IL}	CMOS input low level		1.8≤V_{CC}≤3.63	-	-	0.3V_{CC}	V
V_{IH}	CMOS input high level		1.8≤V_{CC}≤3.63	0.7V_{CC}	-	-	V
TTL_V_{IL}	CMOS-compatible TTL input low level		2.7≤V_{CC}≤3.63	-	-	0.8	V
TTL_V_{IH}	CMOS-compatible TTL input high level		2.7≤V_{CC}≤3.63	2.0	-	-	V
I_{LKG}	I/O input leakage current		V_{SS}≤V_{IN}≤V_{CC}	-	-	1	μA
			V_{IN}=5.5V	-	-	10	μA
R_{PU}(3)(4)	Weak pull up Equivalent resistance		V_{IN}=V_{SS}	-	30	-	kΩ
R_{PD}(2)(3)(5)	Weak pull down Equivalent resistance	PA11/USBFS_DM PA12/USBFS_DP PB14/USBHS_DM PB15/USBHS_DP	V_{IN}=V_{CC}	-	500	-	kΩ
C_{IO}(2)	I/O pin capacitance	PA11/USBFS_DM PA12/USBFS_DP PB14/USBHS_DM PB15/USBHS_DP	-	-	10	-	pF
		Input pins other than above	-	-	5	-	pF

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. To keep the voltage above V_{CC}+0.3V, the internal pull-up/pull-down resistors must be disabled.
4. For PA11/USBFS_DM, PA12/USBFS_DP, PB14/USBHS_DM and PB15/USBHS_DP, the resistance value indicated is the weak pull-up equivalent resistance of GPIO. For details on the pull-up/pull-down resistors related to the USB function, refer to the "USB Interface Characteristics" chapter.
5. Only PA11/USBFS_DM, PA12/USBFS_DP, PB14/USBHS_DM and PB15/USBHS_DP have weak pull-down resistance, and always active.

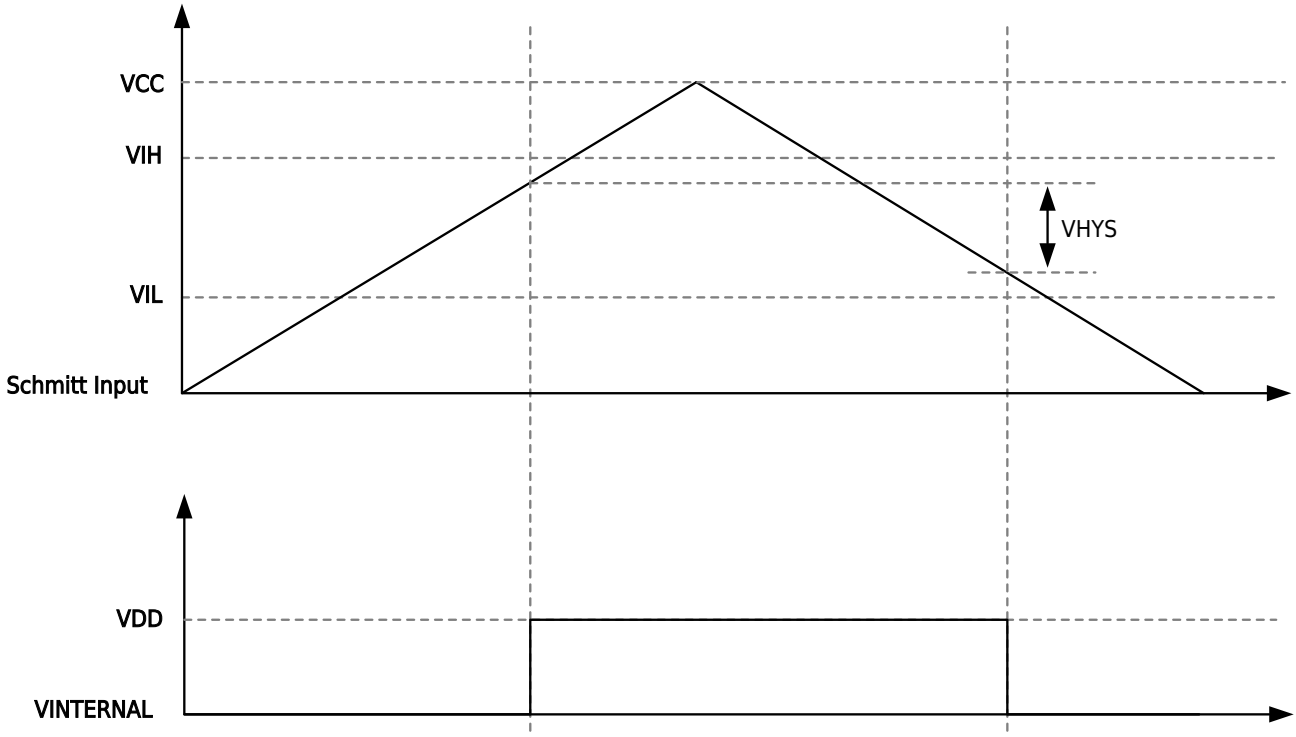


Figure 4-6 Schmitt Input DC Electrical Characteristics Definition

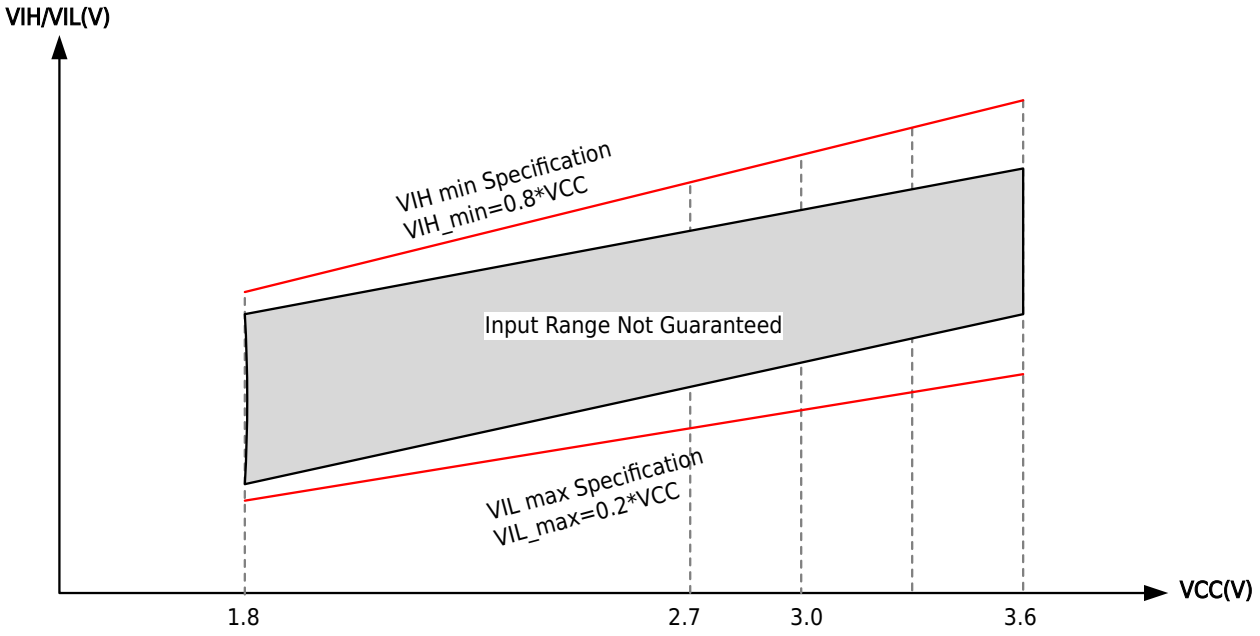


Figure 4-7 VIH/VIL versus VCC (Schmitt Input)

Output Current

GPIO can provide the maximum pull current or sink current of ±20mA.

The pull current or sinking current of PC13, PC14, PC15 and PI8 shall meet the following restrictions: $\sum I_{IO}$ (PC13, PC14, PC15, PI8) ≤20mA.

Output Voltage

Table 4-34 Output Voltage Characteristics

Driver	Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Low drive	V_{OL}(1)	Low level output	I_{IO}=±1.5mA 1.8≤V_{CC}<2.7	-	-	0.6	V
	V_{OH}(2)	High level output		V_{CC}-0.6	-	-	V
	V_{OL}(1)	Low level output	I_{IO}=±3mA 2.7≤V_{CC}≤3.63	-	-	0.6	V
	V_{OH}(2)	High level output		V_{CC}-0.6	-	-	V
	V_{OL}(1)	Low level output	I_{IO}=±6mA 2.7≤V_{CC}≤3.63	-	-	1.3	V
	V_{OH}(2)	High level output		V_{CC}-1.3	-	-	V
Medium drive	V_{OL}(1)	Low level output	I_{IO}=±3mA 1.8≤V_{CC}<2.7	-	-	0.4	V
	V_{OH}(2)	High level output		V_{CC}-0.4	-	-	V
	V_{OL}(1)	Low level output	I_{IO}=±5mA 2.7≤V_{CC}≤3.63	-	-	0.4	V
	V_{OH}(2)	High level output		V_{CC}-0.4	-	-	V
	V_{OL}(3)	Low level output	I_{IO}=±12mA 2.7≤V_{CC}≤3.63	-	-	1.3	V
	V_{OH}(4)	High level output		V_{CC}-1.3	-	-	V
High drive	V_{OL}(1)	Low level output	I_{IO}=±6mA 1.8≤V_{CC}<2.7	-	-	0.4	V
	V_{OH}(2)	High level output		V_{CC}-0.4	-	-	V

Driver	Symbol	Parameters	Conditions	Min	Typ	Max	Unit
High drive	V_{OL}(1)	Low level output	I_{IO}=±8mA 2.7≤V_{CC}≤3.63	-	-	0.4	V
	V_{OH}(2)	High level output		V_{CC}-0.4	-	-	V
	V_{OL}(3)	Low level output	I_{IO}=±20mA 2.7≤V_{CC}≤3.63	-	-	1.3	V
	V_{OH}(4)	High level output		V_{CC}-1.3	-	-	V

Note

1. The device's I_{IO} sinking current must always take into account the absolute maximum ratings specified in Table 4-3 : Current Characteristics. The sum of I_{IO} (I/O port and control pin) must not exceed I_{VSS}. The total output sink current on all I/O and control pins must not exceed 50 mA.
2. The device's I_{IO} pull current must always conform to the absolute maximum ratings specified in Table 4-3 : Current Characteristics. The sum of I_{IO} (I/O port and control pin) must not exceed I_{VCC}. The total output pull current on all I/O and control pins must not exceed -50 mA.
3. The device's I_{IO} sinking current must always take into account the absolute maximum ratings specified in Table 4-3 : Current Characteristics. The sum of I_{IO} (I/O port and control pin) must not exceed I_{VSS}. The total output sink current on all I/O and control pins must not exceed 100 mA.
4. The device's I_{IO} pull current must always conform to the absolute maximum ratings specified in Table 4-3 : Current Characteristics. The sum of I_{IO} (I/O port and control pin) must not exceed I_{VCC}. The total output pull current on all I/O and control pins must not exceed -100 mA.

Input/Output AC Characteristics

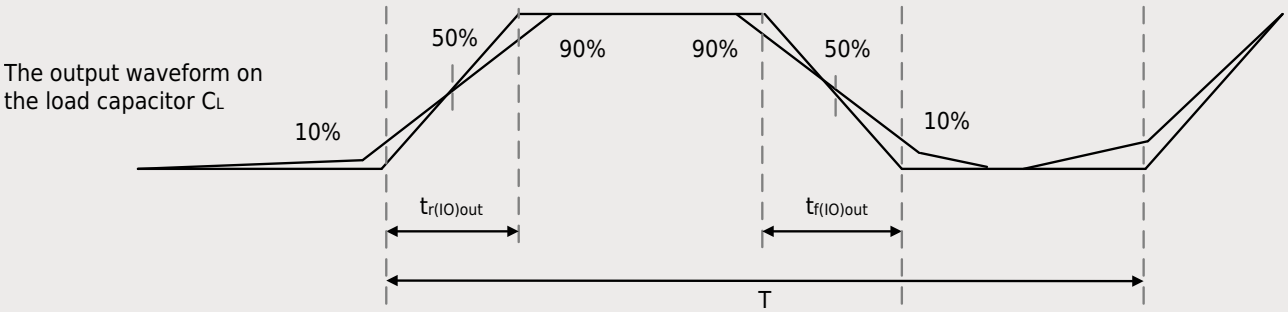
Table 4-35 I/O AC Characteristics

Driver	Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Low drive	$f_{max(IO)out}$(2)(3)	Maximum frequency	C_L=30pF, V_{CC}≥2.7V	-	-	20	MHz
			C_L=30pF, V_{CC}≥1.8V	-	-	10	
			C_L=10pF, V_{CC}≥2.7V	-	-	40	
			C_L=10pF, V_{CC}≥1.8V	-	-	20	
	$t_{f(IO)out}$(1) $t_{r(IO)out}$(1)	Rise/Fall Time	C_L=30pF, V_{CC}≥2.7V	-	-	15	ns
			C_L=30pF, V_{CC}≥1.8V	-	-	25	
			C_L=10pF, V_{CC}≥2.7V	-	-	7.5	
			C_L=10pF, V_{CC}≥1.8V	-	-	15	
Medium drive	$f_{max(IO)out}$(2)(3)	Maximum frequency	C_L=30pF, V_{CC}≥2.7V	-	-	45	MHz
			C_L=30pF, V_{CC}≥1.8V	-	-	22.5	
			C_L=10pF, V_{CC}≥2.7V	-	-	90	
			C_L=10pF, V_{CC}≥1.8V	-	-	45	

Driver	Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Medium drive	$t_{f(IO)out}$(1) $t_{r(IO)out}$(1)	Rise/Fall Time	C_L=30pF, V_{CC}≥2.7V	-	-	6	ns
			C_L=30pF, V_{CC}≥1.8V	-	-	10	
			C_L=10pF, V_{CC}≥2.7V	-	-	4	
			C_L=10pF, V_{CC}≥1.8V	-	-	6	
High drive	$f_{max(IO)out}$(2)(3)	Maximum frequency	C_L=30pF, V_{CC}≥2.7V	-	-	100	MHz
			C_L=30pF, V_{CC}≥1.8V	-	-	50	
			C_L=10pF, V_{CC}≥1.8V	-	-	100	
	$t_{f(IO)out}$(1) $t_{r(IO)out}$(1)	Rise/Fall Time	C_L=30pF, V_{CC}≥2.7V	-	-	4	ns
			C_L=30pF, V_{CC}≥1.8V	-	-	6	
			C_L=10pF, V_{CC}≥2.7V	-	-	2.5	
			C_L=10pF, V_{CC}≥1.8V	-	-	3.5	

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. The maximum frequency is defined in the figure below.
4. Load capacitance C_L should take into account the capacitance of PCB and MCU pins (the capacitance between pins and circuit board can be roughly estimated as 10pF).



Maximum frequency condition ($t_r + t_f$) ≤ (2/3)T and Duty cycle= 50% ± 5%
C_L is indicated in the "Conditions" column of the "I/O AC Characteristics" table)

Figure 4-8 I/O AC Characteristics Definition

4.3.12 I2C Interface Characteristics

Table 4-36 I2C Characteristics

Symbol	Parameters	Standard Mode (SM)		Fast Mode (FM)		Unit
		Min	Max	Min	Max	
f_{SCL}(1)	SCL frequency	0	100	0	400	kHz
$t_{HD;STA}$(1)	Start condition/restart condition hold time	4.0	-	0.6	-	μs
t_{LOW}(1)	SCL low level	4.7	-	1.3	-	μs
t_{HIGH}(1)	SCL high level	4	-	0.6	-	μs

Symbol	Parameters	Standard Mode (SM)		Fast Mode (FM)		Unit
		Min	Max	Min	Max	
$t_{SU;STA}$(1)	Restart condition setup time	4.7	-	0.6	-	μs
$t_{HD;DAT}$	Data hold time	0	-	0	-	μs
$t_{SU;DAT}$	Data setup time	50+t_{I2C_REFCLK}(2)	-	50+t_{I2C_REFCLK}(2)	-	ns
t_R(1)	SCL/SDA rise time	-	1000	6.5	300	ns
t_F(1)	SCL/SDA fall time	-	300	6.5	300	ns
$t_{SU;STO}$(1)	Stop condition setup time	4	-	0.6	-	μs
t_{BUF}(1)	BUS idle time from stop condition to start condition	4.7	-	1.3	-	μs
C_b(1)	Load capacitance	-	400	-	400	pF

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. The t_{I2C_REFCLK}, i.e., the I2C reference clock period, is determined by the I2C_CCR.FREQ bits.

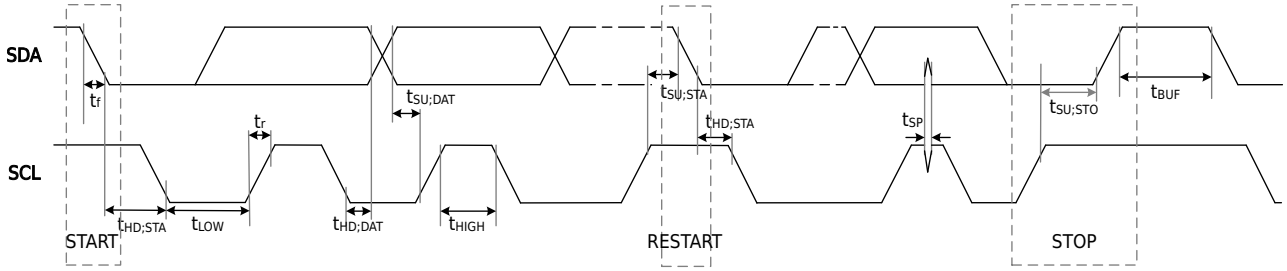


Figure 4-9 I2C Bus Timing Definition

4.3.13 SPI Interface Characteristics

Table 4-37 SPI Characteristics

Symbol	Parameters	Conditions	Min	Max	Unit
t_w(SCKH)(1)	SCK high level time	Master mode(4) 1.8V≤V_{CC}≤3.63V	t_{PCLK1}-1(5)	t_{PCLK1}+1(5)	ns
		Slave mode(4) 1.8V≤V_{CC}≤3.63V	3*t_{PCLK1}-1(5)	3*t_{PCLK1}+1(5)	ns
t_w(SCKL)(1)	SCK low level time	Master mode(4) 1.8V≤V_{CC}≤3.63V	t_{PCLK1}-1(5)	t_{PCLK1}+1(5)	ns
		Slave mode(4) 1.8V≤V_{CC}≤3.63V	3*t_{PCLK1}-1(5)	3*t_{PCLK1}+1(5)	ns
t_{su}(SI)	Data input setup time	Slave mode 1.8V≤V_{CC}≤3.63V	4	-	ns

Symbol	Parameters	Conditions	Min	Max	Unit
t_h(SI)	Data input hold time	Slave mode 1.8V≤V_{CC}≤3.63V	3	-	ns
t_v(SO)	Data output active time	Slave mode 2.7V≤V_{CC}≤3.63V	-	15	ns
		Slave mode 1.8V≤V_{CC}<2.7V	-	26	ns
t_{su}(MI)	Data input setup time	Master mode 2.7V≤V_{CC}≤3.63V	5	-	ns
		Master mode 1.8V≤V_{CC}<2.7V	9	-	ns
t_h(MI)	Data input hold time	Master mode 1.8V≤V_{CC}≤3.63V	$t_{PCLK1*1}$	-	ns
t_{su}(SS)(1)	SS setup time	Slave mode 1.8V≤V_{CC}≤3.63V	$6*t_{PCLK1}$(5)	-	ns
		Master mode 2.7V≤V_{CC}≤3.63V	$-5+N*t_{SCK}$(2)(5)	-	ns
		Master mode 1.8V≤V_{CC}<2.7V	$-10+N*t_{SCK}$(2)(5)	-	ns
t_h(SS)(1)	SS hold time	Slave mode 1.8V≤V_{CC}≤3.63V	$6*t_{PCLK1}$(5)	-	ns
		Master mode 2.7V≤V_{CC}≤3.63V	$-5+N*t_{SCK}$(3)(5)	-	ns
		Master mode 1.8V≤V_{CC}<2.7V	$-10+N*t_{SCK}$(3)(5)	-	ns
t_v(MO)	Data output active time	Master mode 2.7V≤V_{CC}≤3.63V	-	4	ns
		Master mode 1.8V≤V_{CC}≤2.7V	-	9	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. N=1-8, determined by register SPI_CFG1.MSSI.
3. N=1-8, determined by register SPI_CFG1.MSSDL.
4. The values of t_w(SCKH) and t_w(SCKL) are determined by SPI_CFG2.MBR, and the values listed in the table are the values of SPI_CFG2.MBR=0.
5. t_{PCLK1} refers to 1 period of clock PCLK1, and t_{SCK} refers to 1 period of SPI communication clock.

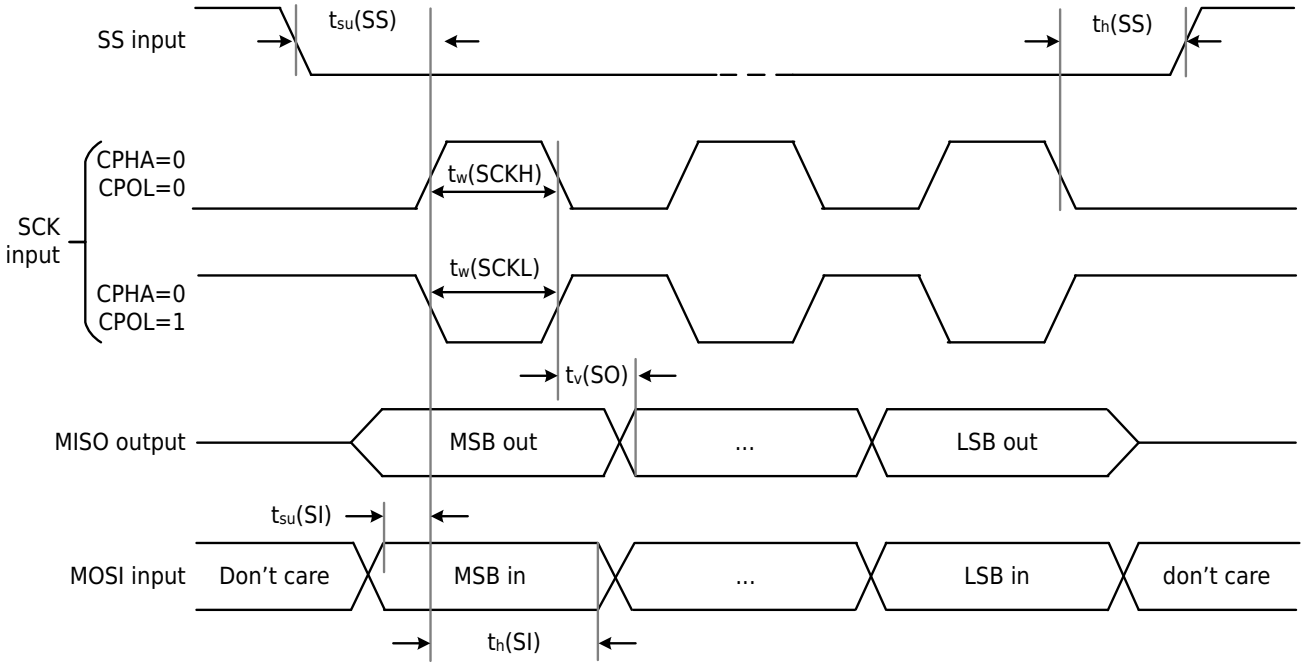


Figure 4-10 SPI Timing Definition (Slave mode, CPHA=0)

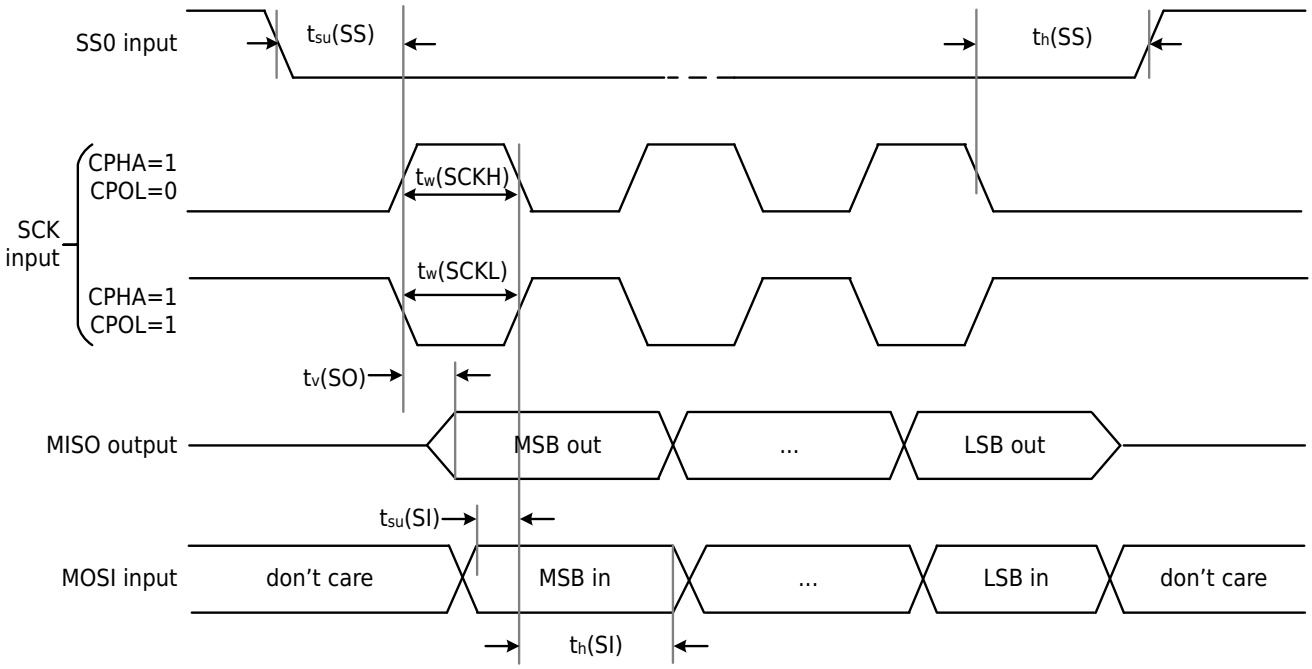


Figure 4-11 SPI Timing Definition (Slave mode, CPHA=1)

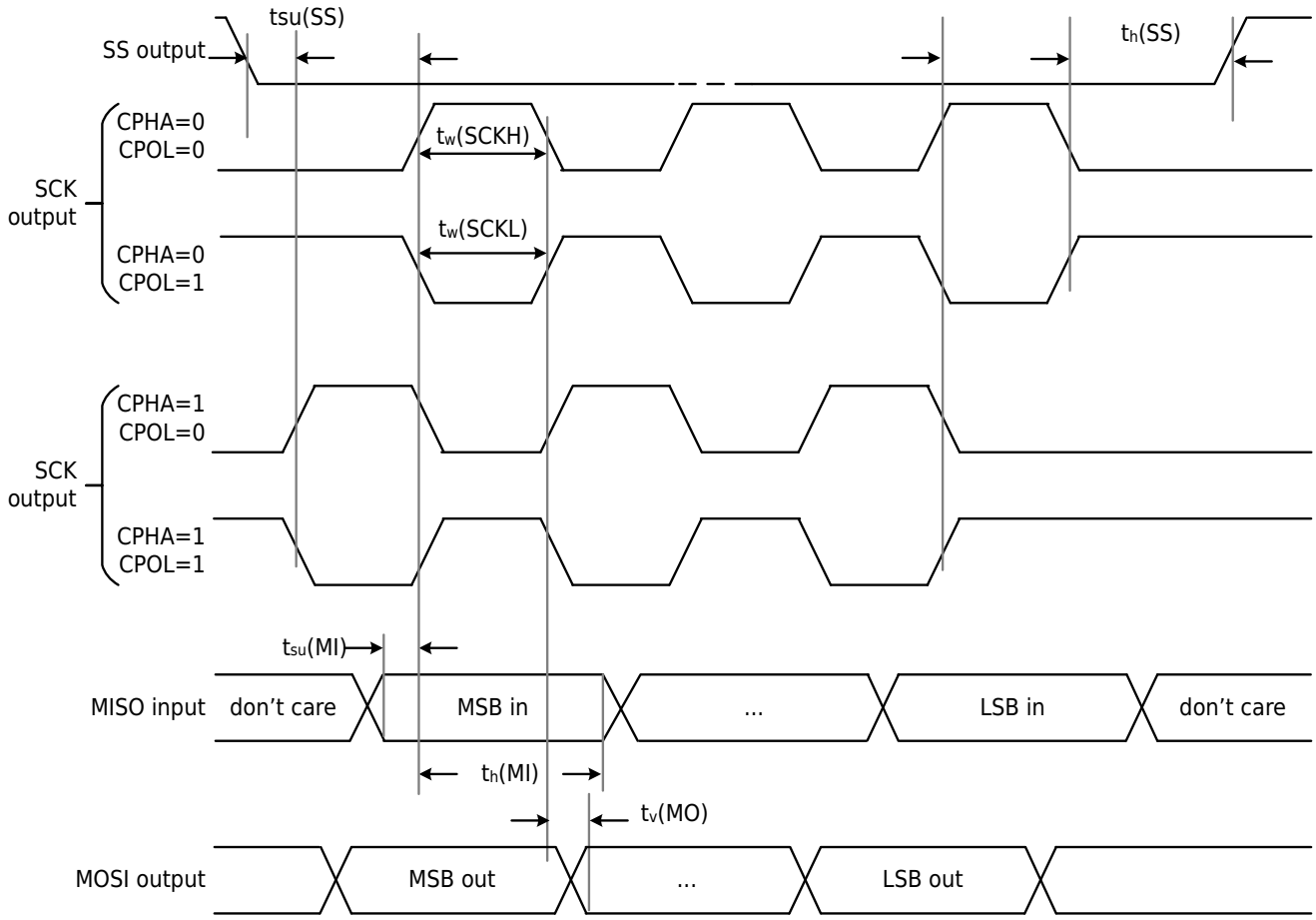


Figure 4-12 SPI Timing Definition (Master mode)

4.3.14 QSPI Interface Characteristics

Table 4-38 QSPI Characteristics

Symbol	Parameters	Conditions	Min	Max	Unit
t_{QSCYC}(1)	SCK clock periods	-	2	48	t_{HCLK}
t_{QSWH}(1)	SCK high level	-	t_{QSCYC}*0.4	-	ns
t_{QSWL}(1)	SCK low level	-	t_{QSCYC}*0.4	-	ns
t_{SU}	Data input setup time	-	5	-	ns
t_{IH}	Data input hold time	2.7V≤V_{CC}≤3.63V	11	-	ns
		1.8V≤V_{CC}<2.7V	15	-	ns
t_{OD}	Data output delay	-	-	4	ns
t_{OH}(1)	Data output hold time	-	0	-	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.

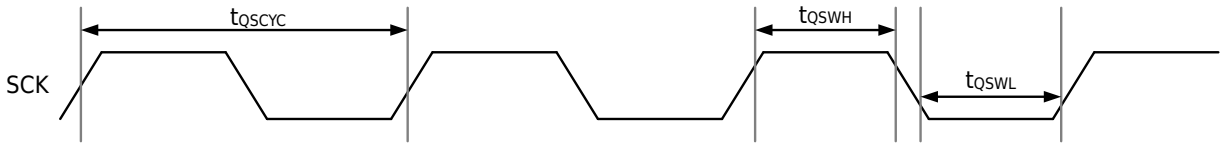


Figure 4-13 QSPI Clock Timing

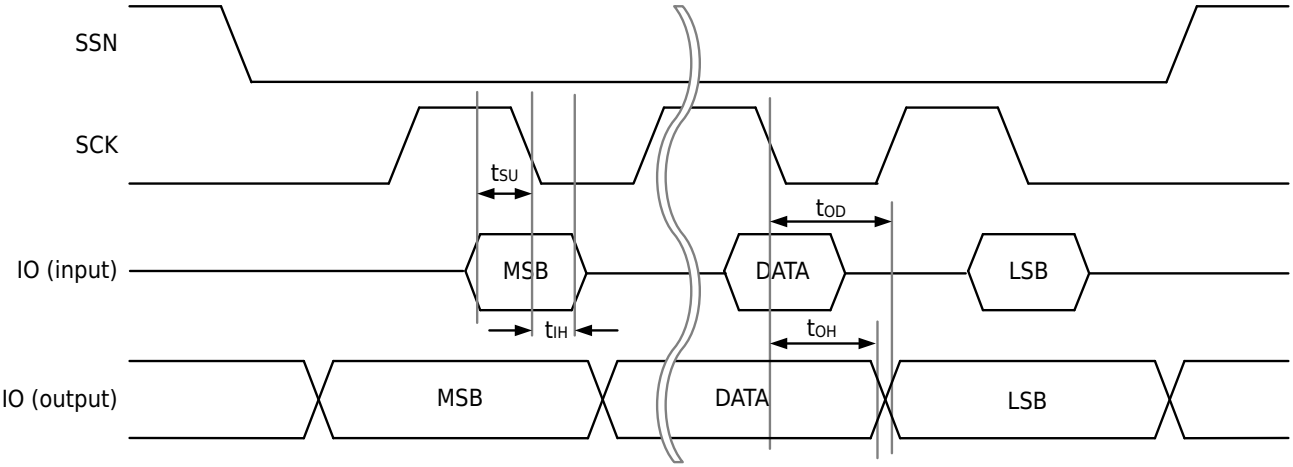


Figure 4-14 QSPI Timing Definition

4.3.15 I2S Interface Characteristics

Table 4-39 I2S Characteristics

Symbol	Parameters	Conditions	Min	Max	Unit
f_{MCK}(1)	I2S master clock output frequency	-	256*8K	256*Fs	MHz
f_{CK}(1)	I2S clock frequency	Master data: 32bits	20	64*Fs	MHz
		Slave data: 32bits	-	64*Fs	
D_{CK}(1)	I2S clock duty period	Slave reception	30	70	%
t_v(WS)	WS active time	Master mode	-	6	ns
t_{su}(WS)	WS setup time	Slave mode	7.5	-	ns
t_h(WS)	WS hold time	Slave mode	6	-	ns
t_{su}(SD_MR)	Data input setup time	Master reception (2.7V-3.63V)	22	-	ns
		Master reception (1.8V-2.7V)	25	-	ns
t_{su}(SD_SR)		Slave reception	7	-	ns
t_h(SD_MR)	Data input hold time	Master reception	0	-	ns
t_h(SD_SR)		Slave reception	7	-	ns
t_v(SD_ST) t_h(SD_ST)	Data output active time	Slave signaling (after active edge)	-	24	ns
t_v(SD_MT)		Master signaling (after the active edge)	-	10	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Fs: I2S sampling frequency.

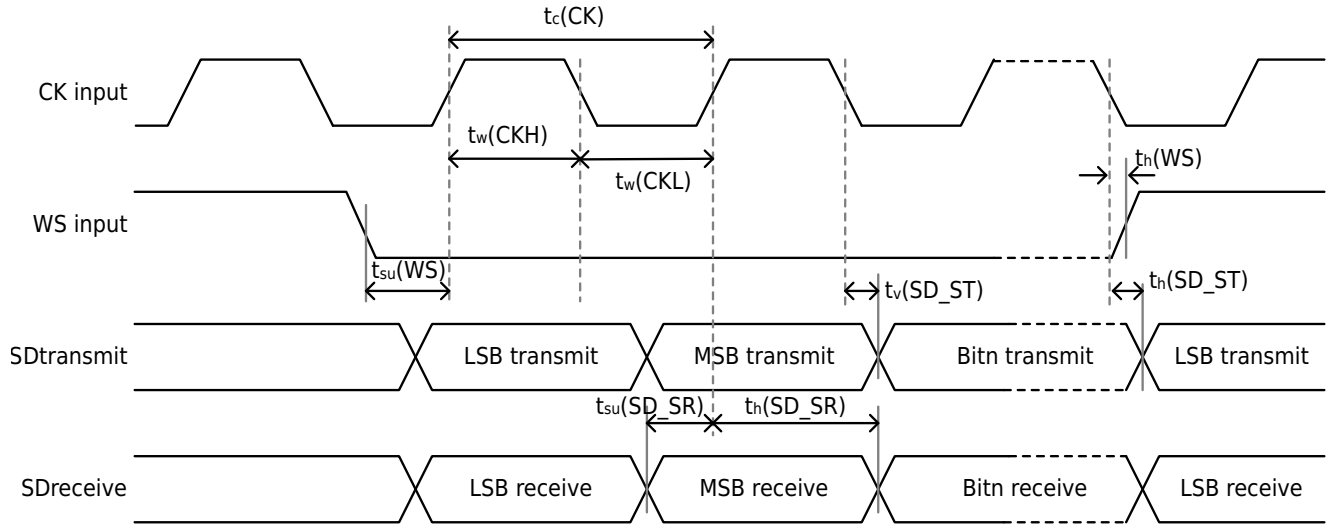


Figure 4-15 I2S Slave Mode Timing (Philips Protocol)

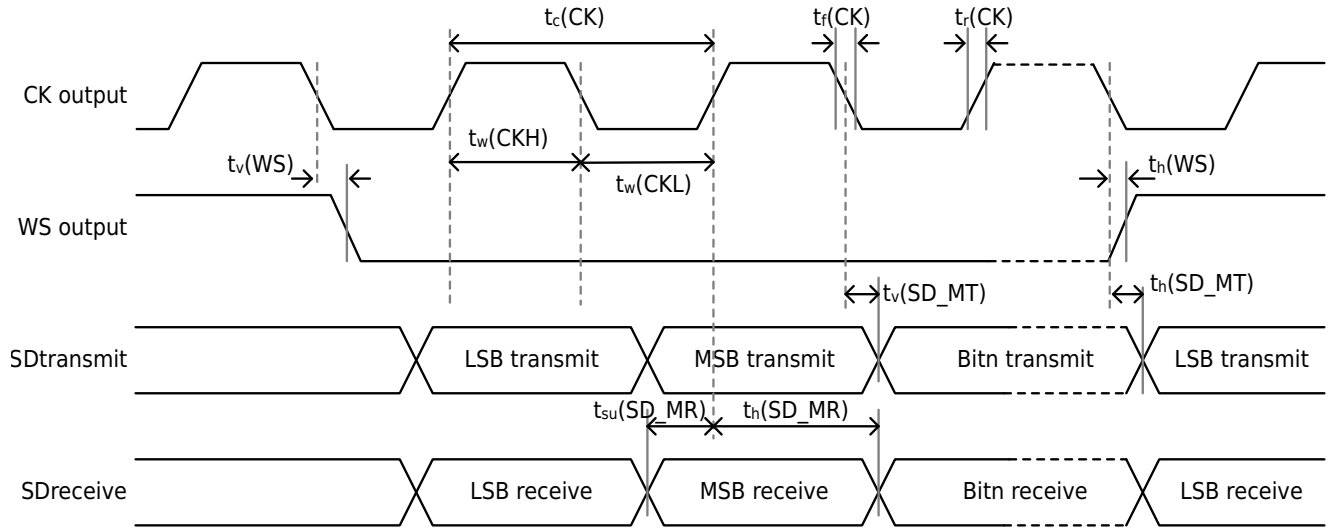


Figure 4-16 I2S Master Mode Timing (Philips Protocol)

4.3.16 CAN FD Interface Characteristics

For the port characteristics of CANx_TX/RX and MCANx_TX/RX, please refer to "I/O Port Characteristics".

4.3.17 USB Interface Characteristics

Table 4-40 USB Full-Speed Characteristics

Symbol		Parameters	Conditions	Min(1)	Typ	Max(1)	Unit
In-put	V_{CC}(3)	Operating voltage	-	3.0(2)	-	3.63	V
	V_{IL}	Input low level	-	-	-	0.8	V
	V_{IH}	Input high level	-	2.0	-	-	V
	V_{DI}	Differential input sensitivity	-	0.2	-	-	V
	V_{CM}	Differential common mode voltage	-	0.8	-	2.5	V
Out-put	V_{OL}(3)	Static output low level	R_L=1.5kΩ to 3.63V(4)	-	-	0.3	V
	V_{OH}(3)	Static output high level	R_L=15kΩ to VSS(4)	2.8	-	3.63	V
	V_{CRS}(3)	Cross-over voltage	C_L=50pF	1.3	-	2.0	V
	t_R(3)	Rise time	C_L=50pF 10%-90% of $\|V_{OH}-V_{OL}\|$	4	-	20	ns
	t_F(3)	Fall time	C_L=50pF 10%-90% of $\|V_{OH}-V_{OL}\|$	4	-	20	ns
	t_{RFMA}(3)	Rise and fall time ratio t_R/t_F	C_L=50pF	90	-	111	%
R_{PD}		Pull-down resistor	$V_{IN}=V_{CC}$, in host mode	-	15.0	-	kΩ
R_{PU}		Pull-up resistor	$V_{IN}=V_{SS}$, idle state	0.900	1.2	1.575	kΩ
			$V_{IN}=V_{SS}$, in device mode	1.425	2.3	3.090	kΩ
Z_{DRV}(3)(5)		Output impedance	Driving high or low	28	36	44	Ω

Note

1. All voltages are measured based on local ground potential.
2. The function of the USB full-speed transceiver is still guaranteed when the operating voltage is reduced to 2.7V, but the complete USB full-speed electrical characteristics are not guaranteed, which will be degraded in the V_{CC} voltage range of 2.7 to 3.0V.
3. Resulted from comprehensive evaluation, not tested in production.
4. R_L is the load connected to the USB full speed drive.
5. DP and DM ports do not need external series resistors for impedance matching, and the Driver output already includes this matching resistor.
6. DP and DM ports do not need external pull-up/pull-down resistors, and the PHY is already integrated internally.

Table 4-41 USB Low-Speed Characteristics

Symbol		Parameters	Conditions	Min(1)	Typ	Max(1)	Unit
In-put	V_{CC}(3)	Operating voltage	-	3.0(2)	-	3.63	V
	V_{IL}	Input low level	-	-	-	0.8	V
	V_{IH}	Input high level	-	2.0	-	-	V
	V_{DI}	Differential input sensitivity	-	0.2	-	-	V
	V_{CM}	Differential common mode voltage	-	0.8	-	2.5	V
Out-put	V_{OL}(3)	Static output low level	R_L=1.5kΩ to 3.63V(4)	-	-	0.3	V
	V_{OH}(3)	Static output high level	R_L=15kΩ to VSS(4)	2.8	-	3.63	V
	V_{CRS}(3)	Cross-over voltage	C_L=200pF-600pF	1.3	-	2.0	V
	t_R(3)	Rise time	C_L=200pF-600pF 10%-90% of $\|V_{OH}-V_{OL}\|$	75	-	300	ns
	t_F(3)	Fall time	C_L=200pF-600pF 10%-90% of $\|V_{OH}-V_{OL}\|$	75	-	300	ns
	t_{RFMA}(3)	Rise and fall time ratio t_R/t_F	C_L=200pF-600pF	80	-	125	%
R_{PD}(3)		Pull-down resistor	$V_{IN}=V_{CC}$, in host mode	-	15.0	-	kΩ
Z_{DRV}(3)(5)		Output impedance	Driving high or low	28	36	44	Ω

Note

1. All voltages are measured based on local ground potential.
2. When the operating voltage drops to 2.7V, the function of the USB low-speed transceiver can still be guaranteed, but the complete USB low-speed electrical characteristics cannot be guaranteed, and the latter will be degraded in the V_{CC} voltage range of 2.7 to 3.0V.
3. Resulted from comprehensive evaluation, not tested in production.
4. R_L is the load connected to the USB low-speed drive.
5. DP and DM ports do not need external series resistors for impedance matching, and the Driver output already includes this matching resistor.
6. DP and DM ports do not need external pull-up/pull-down resistors, and the PHY is already integrated internally.

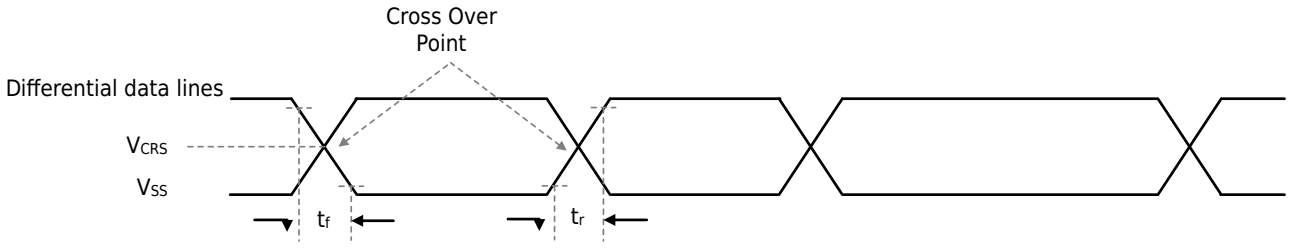


Figure 4-17 Definition of USB Rise/Fall Time and Cross Over-voltage

Table 4-42 ULPI HS Clock Timing Parameters

Symbol	Parameter[1]	Conditions	Min[2]	Typ[2]	Max[2]	Unit
t_{SC}[3]	Control signal set-up time (ULPI_DIR,ULPI_NXT) setup time	2.7V≤V_{CC}≤3.63V C_L=20pF -40-125℃	3.0	-	-	ns
t_{HC}[3]	Control signal hold time (ULPI_DIR,ULPI_NXT) hold time		2.0	-	-	ns
t_{SD}	Data setup time		3.0	-	-	ns
t_{HD}	Data hold time		2.2	-	-	ns
t_{DC}/t_{DD}	Data/control signal output delay		4.5	7.5	10.6	ns

Note

1. The ULPI_CLK clock should comply with UTMI+ Low Pin Interface Specification, Revision 1.1,20/10/2004 protocol.
2. The corresponding IO should be set to high drive.
3. Resulted from comprehensive evaluation, not tested in production.

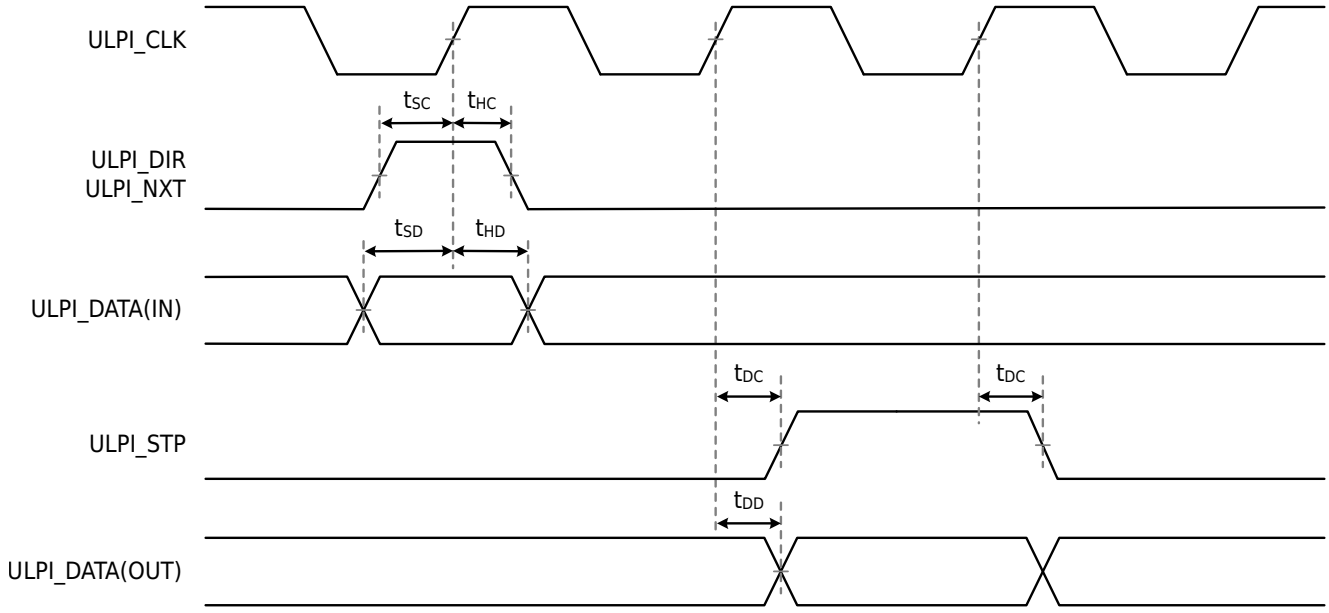


Figure 4-18 ULPI Timing Diagram

4.3.18 ETHMAC Characteristics

4.3.18.1 SMI Interface Characteristics

Table 4-43 ETHMAC_SMI interface characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
t_mdc[1]	SMI_MDC output frequency	-	405	420	425	ns
t_mdo_d	SMI_MDO output delay time	2.7V≤V_{CC}≤3.63V	-	-	t_{PCLK1}+9	ns
		1.8V≤V_{CC}<2.7V	-	-	t_{PCLK1}+12	ns

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
t_mdi_s	SMI_MDI input Setup time	2.7V≤V_{CC}≤3.63V	15	-	-	ns
		1.8V≤V_{CC}<2.7V	20	-	-	ns
t_mdi_h	SMI_MDI input Hold time	-	0	-	-	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.

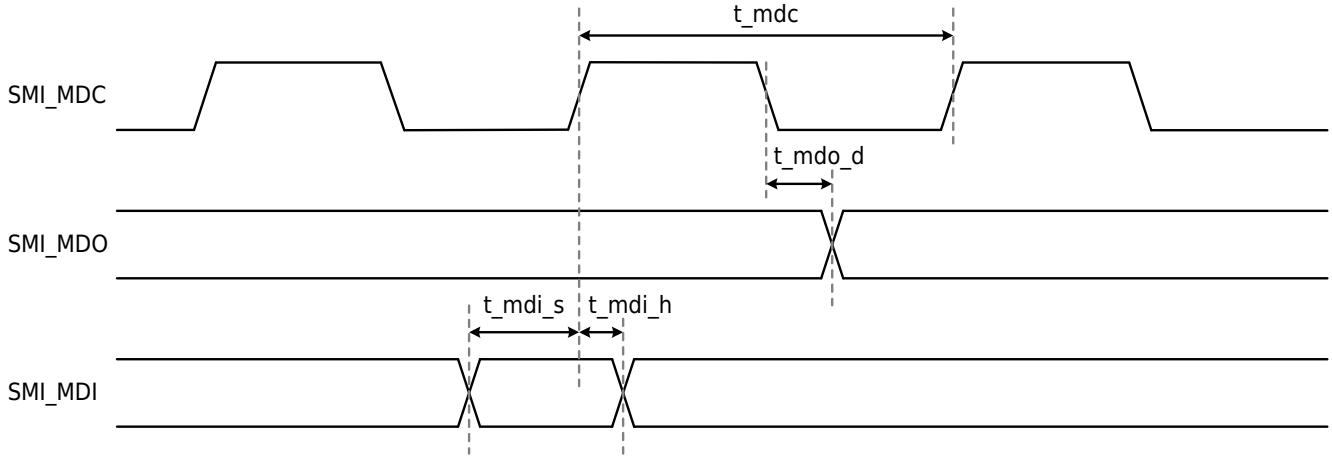


Figure 4-19 ETHMAC-SMI Interface Timing Diagram

4.3.18.2 MII Interface Characteristics

Table 4-44 ETHMAC_MII interface characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
t_mii_tx_clk(1)	MII_TX_CLK input clock frequency	-	-	40	-	ns
t_mii_txen_d	MII_TX_EN output delay time	2.7V≤V_{CC}≤3.63V	5	-	15	ns
		1.8V≤V_{CC}<2.7V	5	-	21	ns
t_mii_txer_d	MII_TX_ER output delay time	2.7V≤V_{CC}≤3.63V	5	-	15	ns
		1.8V≤V_{CC}<2.7V	5	-	21	ns
t_mii_txd_d	MII_TXD output delay time	2.7V≤V_{CC}≤3.63V	5	-	15	ns
		1.8V≤V_{CC}<2.7V	5	-	21	ns
t_mii_rx_clk(1)	MII_RX_CLK input clock frequency	-	-	40	-	ns
t_mii_rxdv_s	MII_RX_DV input Setup time	-	8	-	-	ns
t_mii_rxdv_h	MII_RX_DV input Hold time	-	4	-	-	ns
t_mii_rxer_s	MII_RX_ER input Setup time	-	8	-	-	ns
t_mii_rxer_h	MII_RX_ER input Hold time	-	4	-	-	ns
t_mii_rxd_s	MII_RXD input Setup time	-	8	-	-	ns
t_mii_rxd_h	MII_RXD input Hold time	-	4	-	-	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.

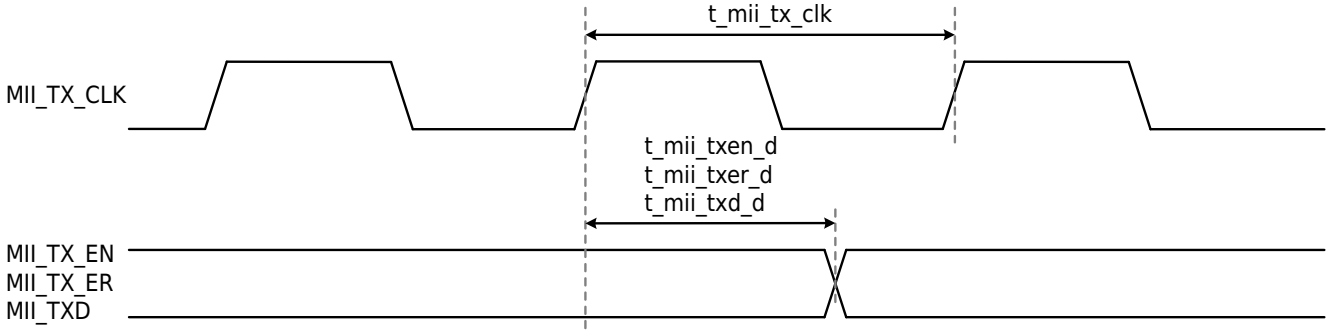


Figure 4-20 ETHMAC-MII interface output signal timing diagram

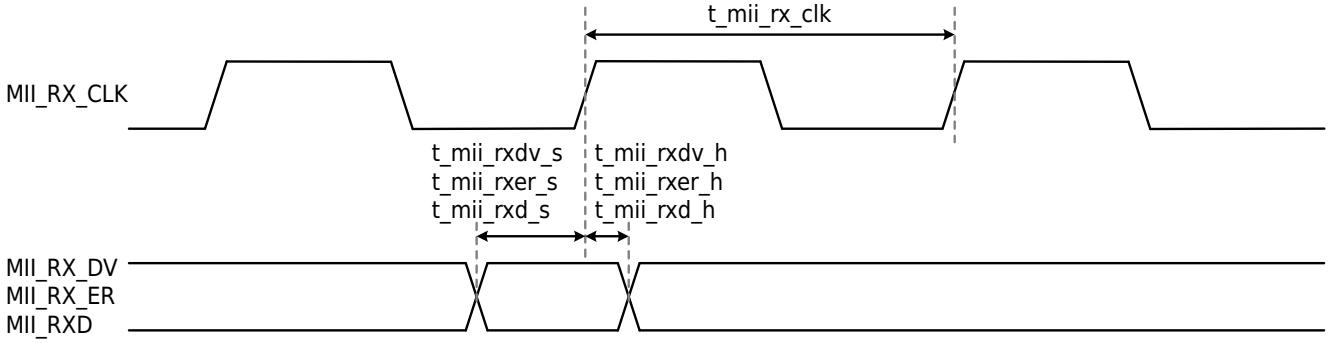


Figure 4-21 ETHMAC-MII interface input signal timing diagram

4.3.18.3 RMII Interface Characteristics

Table 4-45 ETHMAC_RMII interface characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
t_rmii_clk(1)	RMII_REF_CLK reference clock input frequency	-	-	20	-	ns
t_rmii_txen_d	RMII_TX_EN output delay time	2.7V≤V_{CC}≤3.63V	5	-	12.5	ns
		1.8V≤V_{CC}<2.7V	5	-	16	ns
t_rmii_txd_d	RMII_TXD output delay time	2.7V≤V_{CC}≤3.63V	5	-	12.5	ns
		1.8V≤V_{CC}<2.7V	5	-	16	ns
t_rmii_crsdv_s	RMII_CRS_DV input Setup time	-	4	-	-	ns
t_rmii_crsdv_h	RMII_CRS_DV input Hold time	-	2	-	-	ns
t_rmii_rxd_s	RMII_RXD input Setup time	-	4	-	-	ns
t_rmii_rxd_h	RMII_RXD input Hold time	-	2	-	-	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.

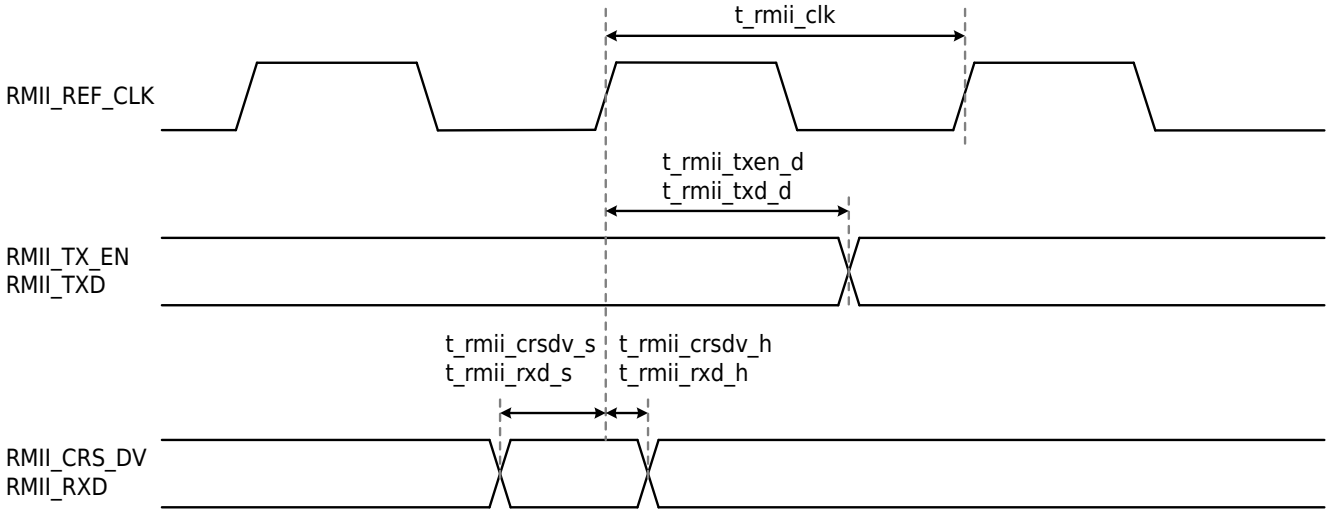


Figure 4-22 ETHMAC-RMII interface timing diagram

4.3.19 USART Interface Characteristics

Table 4-46 USART AC Timing

Symbol	Parameters	Conditions	Min	Max	Unit
t_{cyc} (1)	Input clock cycles	UART	4	-	t_{PCLK1}
		Clock Synchronization Mode	6	-	
t_{CKw} (1)	Input clock width	-	0.4	0.6	t_{cyc}
t_{CKr} (1)	Input clock rise time	-	-	5	ns
t_{CKf} (1)	Input clock fall time	-	-	5	ns
t_{TD}	Transmit delay time	Clock Synchronization Mode, $2.7V \le V_{CC} \le 3.63V$	-	23	ns
		Clock Synchronization Mode, $1.8V \le V_{CC} < 2.7V$	-	30	ns
t_{RDS}	Receive data setup time	Clock Synchronization Mode, $2.7V \le V_{CC} \le 3.63V$	17	-	ns
		Clock Synchronization Mode, $1.8V \le V_{CC} < 2.7V$	23	-	ns
t_{RDH}	Receive data hold time	Clock Synchronization Mode	5	-	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-47 USART Maximum Baud Rate(1)

Mode		Max Baud Rate
UART	Internal clock source	PCLK1/8
	External clock source	PCLK1/32
Clock synchronization mode, $2.7V \le V_{CC} \le 3.63V$		12.0Mbps
Clock synchronization mode, $1.8V \le V_{CC} < 2.7V$		8.0Mbps

Note

1. Guaranteed by design, not tested in production.

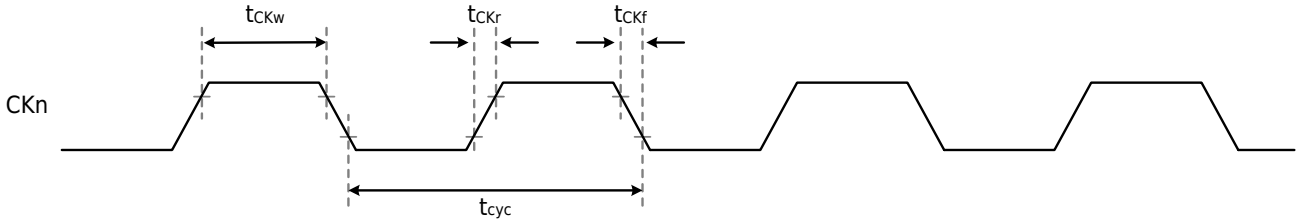


Figure 4-23 USART Clock Timing

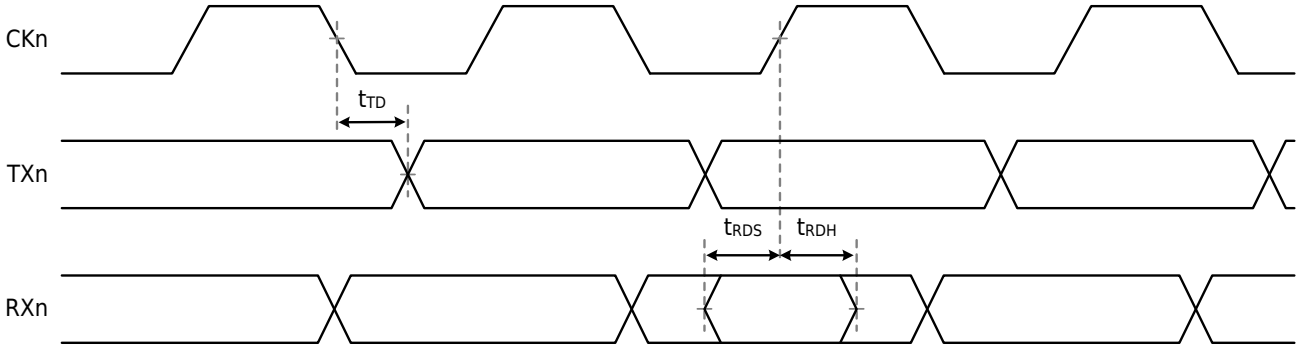


Figure 4-24 USART(CSI) Input and Output Timing

4.3.20 JTAG Interface Characteristics

Table 4-48 JTAG Interface Features

Symbol	Parameters	Min	Typ	Max	Unit
t_{TCKcyc}(1)	JTCK clock period	50	-	-	ns
t_{TCKH}(1)	JTCK clock high level	15	-	-	ns
t_{TCKL}(1)	JTCK clock low level	15	-	-	ns
t_{TCKr}(1)	JTCK clock rise time	-	-	5	ns
t_{TCKf}(1)	JTCK clock fall time	-	-	5	ns
t_{TMSs}	JTMS setup time	10	-	-	ns
t_{TMSh}	JTMS hold time	10	-	-	ns
t_{TDIs}	JTDI setup time	10	-	-	ns
t_{TDIh}	JTDI hold time	10	-	-	ns
t_{TDOd}	JTDO data delay	-	-	25	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.

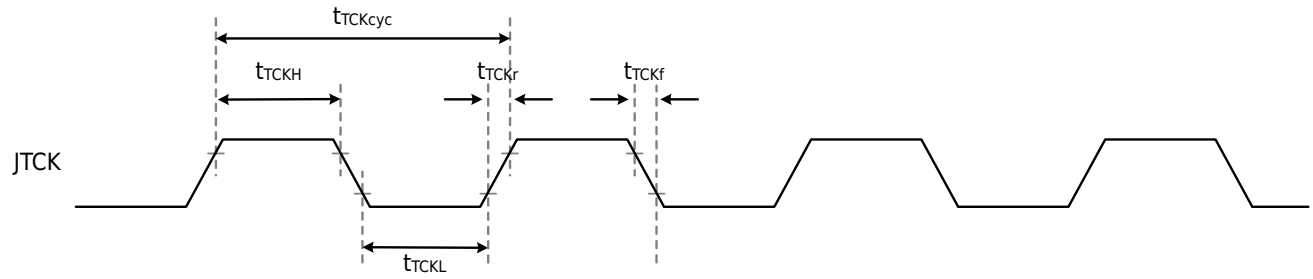


Figure 4-25 JTAG TCK clock

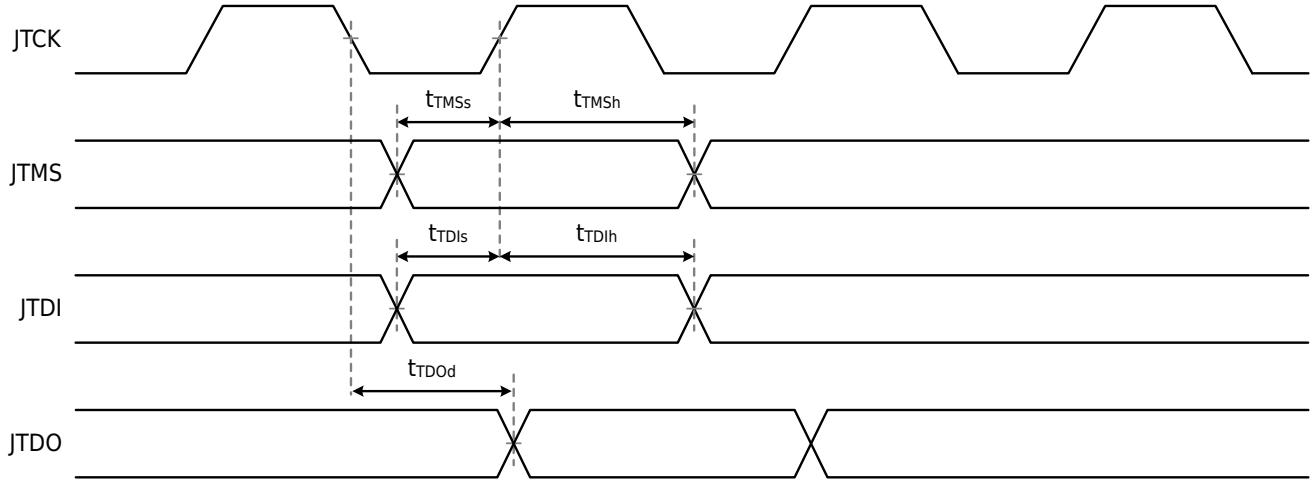


Figure 4-26 JTAG input and output

4.3.21 SWD Interface Characteristics

Table 4-49 SWD Interface Characteristics

Symbol	Parameters	Min	Typ	Max	Unit
$t_{SWCLKcyc}$(1)	SWCLK clock period	50	-	-	ns
t_{SWCLKH}(1)	SWCLK clock high level	15	-	-	ns
t_{SWCLKL}(1)	SWCLK clock low level	15	-	-	ns
t_{SWCLKr}(1)	SWCLK clock rise time	-	-	5	ns
t_{SWCLKf}(1)	SWLCK clock fall time	-	-	5	ns
t_{SWDIs}	SWDI setup time	10	-	-	ns
t_{SWDIh}	SWDI hold time	10	-	-	ns
t_{SWDOd}	SWDO data delay	2	-	25	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.

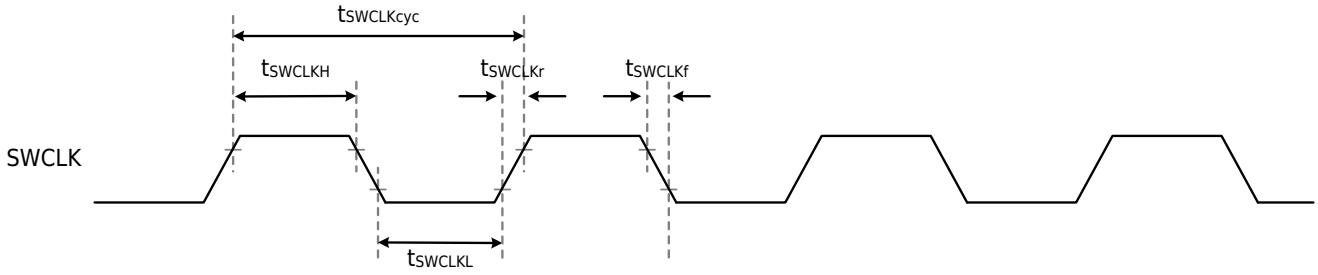


Figure 4-27 SWCLK Clock

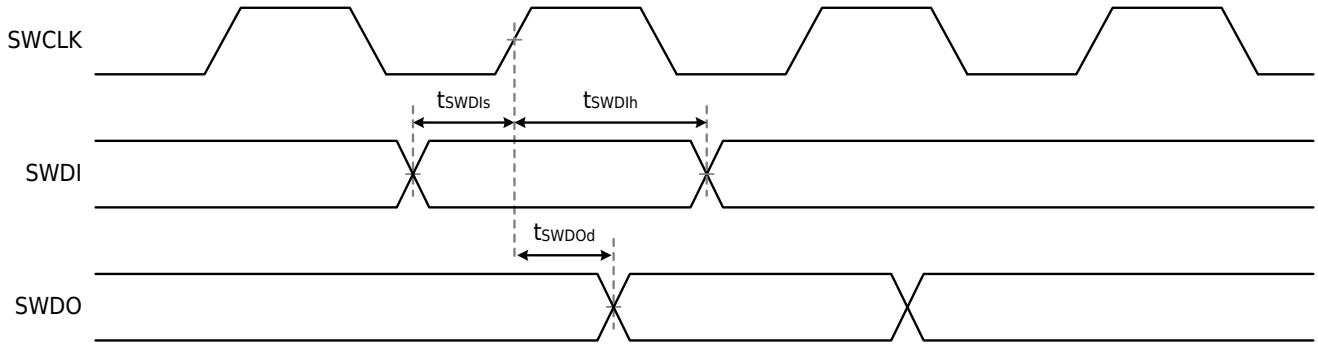


Figure 4-28 SWDIO Input and Output

4.3.22 ETM Interface Characteristics

Table 4-50 ETM Interface Characteristics

Symbol	Parameters	Min	Typ	Max	Unit
$t_{TRCLKcyc}$ (1)	TRACECK clock period	20	-	-	ns
t_{TRCKH} (1)	TRACECK clock high level	7	-	-	ns
t_{TRCKL} (1)	TRACECK clock low level	7	-	-	ns
t_{TRCKr} (1)	TRACECK clock rise time	-	-	2.5	ns
t_{TRCKf} (1)	TRACECK clock fall time	-	-	2.5	ns
t_{TRDd}	TRACED 0-3 data delay	1.6	-	8.4	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.

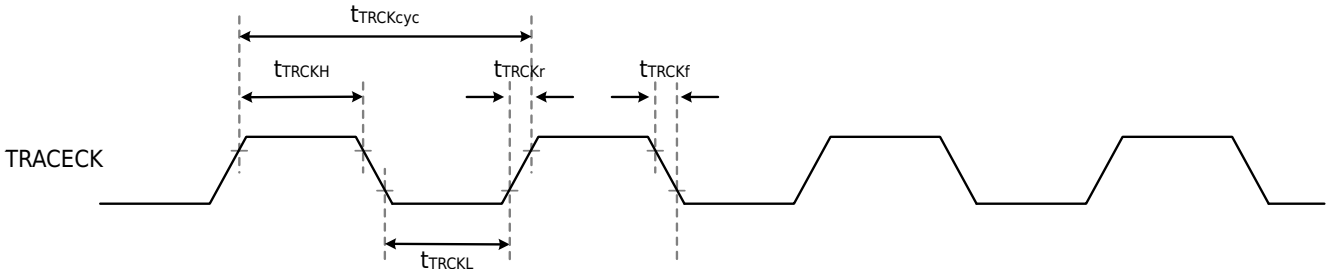


Figure 4-29 TRACE Clock

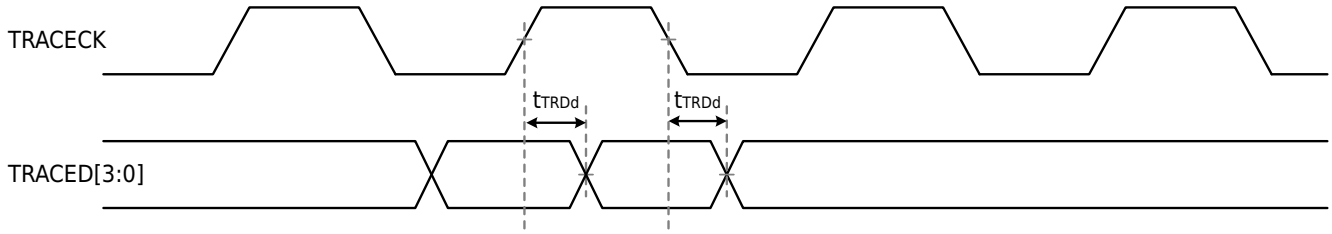


Figure 4-30 TRACE Data Output

4.3.23 12-bit ADC Characteristics

Table 4-51 ADC Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{AVCC}(3)	Power Supply	-	1.8	-	3.63	V
V_{REFH}(3)	Positive Reference Voltage(2)	-	1.8	-	V_{AVCC}	V
f_{ADC}(3)	ADC Conversion Clock Frequency	High-speed working mode 2.4V≤V_{AVCC}≤3.63V	1	-	60	MHz
		Low-speed working mode 1.8V≤V_{AVCC}<2.4V	1	-	30	
		Ultra-low speed working mode	1	-	8	
V_{AIN}(3)	Conversion Voltage Range	-	V_{REFL}	-	V_{REFH}	V
R_{AIN}(1)	External Input Impedance	See formula 1 for details.	-	-	50	kΩ
R_{ADC}(1)	Sample Switch Resistance	-	-	3	6	kΩ
C_{ADC}(1)	Internal Sampling and Holding Capacitor	-	-	4	7	pF
t_D(1)	Trigger Conversion Delay	f_{ADC}=60MHz	-	-	0.3	μs
t_S(1)	Sample Time	f_{ADC}=60MHz	0.183	-	4.266	μs
			11	-	255	1/f_{ADC}
t_{CONV}(1)	Single Channel Total Conversion Time (Including sampling time, the calculation method is: sampling time Ts+ gradually approaching n-bit resolution +1)	f_{ADC}=60MHz 12-bit resolution	0.4	-	-	μs
			24	-	268	1/f_{ADC}
		f_{ADC}=60MHz 10-bit resolution	0.37	-	-	μs
			22	-	266	1/f_{ADC}
		f_{ADC}=60MHz 8-bit resolution	0.34	-	-	μs
			20	-	264	1/f_{ADC}

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_S(1)	Sample Rate f_{ADC}=60MHz	12-bit resolution Single ADC -40-105℃	-	-	2.5	Msps
		12-bit resolution Single ADC -40-125℃	-	-	2	Msps
t_{ST}(1)	Startup Time	-	-	1	2	μs

Note

1. Guaranteed by design, not tested in production.
2. $0 \le V_{AVCC}\text{-}V_{REFH} \le 1.2V$.
3. Resulted from comprehensive evaluation, not tested in production.

Formula 1: RAIN Maximum Formula

$$R_{AIN} = \frac{k}{f_{ADC} * C_{ADC} * \ln\left(2^{N+2}\right)} - R_{ADC}$$

The above formula (Formula 1) is used to determine the maximum external impedance that makes the error less than 1/4LSB. Where N=12 (12-bit resolution) and k is the number of sampling periods defined in ADC_SSTR register.

Table 4-52 Input Channel Accuracy @f_{ADC}=60MHz(1)

Symbol	Parameters	Conditions	Min	Max	Unit
E_T	Total Unadjusted Error	f_{ADC}=60MHz Input Source Impedance<1kΩ V_{REFH}=V_{AVCC}=2.4V/3.63V T_A=-40℃/125℃	±5.5	±7	LSB
E_O	Offset Error		±4.5	±7	LSB
E_G	Gain Error		±4.5	±7	LSB
E_D	Differential Nonlinearity Error		±1.5	±3	LSB
E_L	Integral Nonlinearity Error		±2.0	±4	LSB

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-53 Input Channel Accuracy @f_{ADC}=8MHz/30MHz(1)

Symbol	Parameters	Conditions	Min	Max	Unit
E_T	Total Unadjusted Error	f_{ADC}=8MHz/30MHz Input Source Impedance<1kΩ V_{REFH}=V_{AVCC}=1.8V T_A=-40℃/105℃	±5.5	±7	LSB
E_O	Offset Error		±4.5	±7	LSB
E_G	Gain Error		±4.5	±7	LSB
E_D	Differential Nonlinearity Error		±1.5	±3	LSB
E_L	Integral Nonlinearity Error		±2.0	±4	LSB

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-54 Input Channel Accuracy @f_{ADC}=60MHz(1)

Symbol	Parameters	Conditions	Min	Max	Unit
ENOB	Active Bits	f_{ADC}=60MHz	10.5	-	Bits
SINAD	Signal-to-Noise and Distortion Ratio	Input Signal Frequency=2kHz Input Source Impedanc=0Ω	64.4	-	dB
SNR	Signal-to-Noise Ratio	V_{REFH}=V_{AVCC}=2.4V/3.63V	64.4	-	dB
THD	Total Harmonic Distortion	T_A=-40℃/125℃	-	-80.3	dB

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-55 Input Channel Accuracy @f_{ADC}=8MHz/30MHz(1)

Symbol	Parameters	Conditions	Min	Max	Unit
ENOB	Active Bits	f_{ADC}=8MHz/30MHz	10.6	-	Bits
SINAD	Signal-to-Noise and Distortion Ratio	Input Signal Frequency=2kHz Input Source Impedanc=0Ω	66.6	-	dB
SNR	Signal-to-Noise Ratio	V_{REFH}=V_{AVCC}=1.8V	66.8	-	dB
THD	Total Harmonic Distortion	T_A=-40℃/105℃	-	-79.4	dB

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-56 ADC + Sample and Hold Circuit Channel Accuracy @f_{ADC}=60MHz(1)

Symbol	Parameters	Conditions	Min	Max	Unit
E_T	Total Unadjusted Error	f_{ADC}=60MHz	±6	±8	LSB
E_O	Offset Error	Input Source Impedance<1kΩ	±6	±8	LSB
E_G	Gain Error	V_{REFH}=V_{AVCC}=2.7V/3.63V	±6	±8	LSB
E_D	Differential Nonlinearity Error	T_A=-40℃/125℃	±2	±3	LSB
E_L	Integral nonlinearity error		±3	±4	LSB

Note

1. Resulted from comprehensive evaluation, not tested in production.

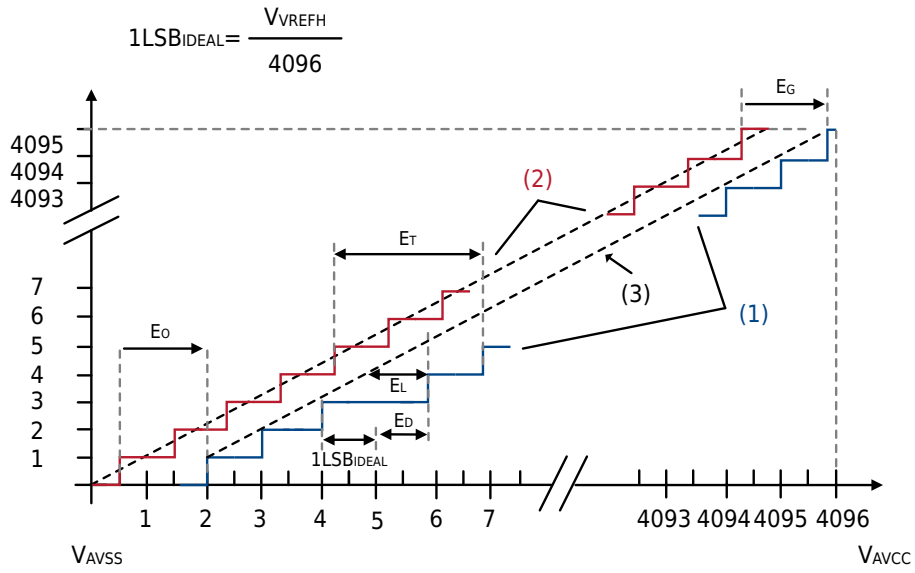


Figure 4-31 ADC Presision Characteristics

1. Examples of actual transmission curves.
2. Ideal transfer curve.
3. End point correlation line.
4. E_T=Total Unadjusted Error: The maximum deviation between the actual and ideal transfer curve.
   E_O=Offset Error: The deviation between the first actual transition and the first ideal transition.
   E_G=Gain Error: The deviation between the last ideal transition and the last actual transition.
   E_D=Differential Nonlinearity Error: The maximum deviation between the actual step and the ideal.
   E_L=Integral Nonlinearity Error: The maximum deviation between any actual transformation and the line associated with the endpoints.

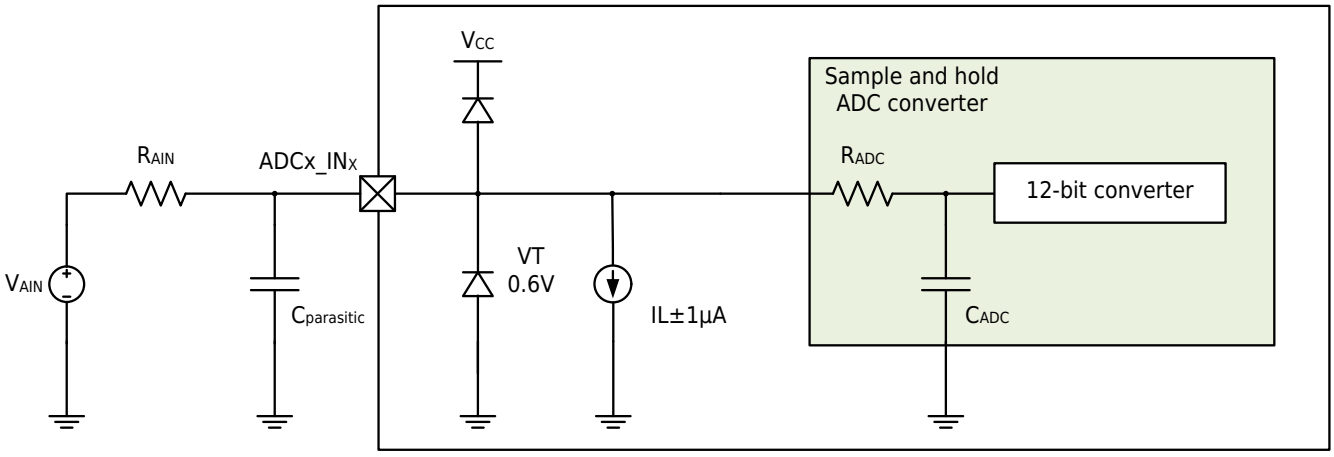


Figure 4-32 Typical connection using ADC

1. For information on R_{AIN}, R_{ADC}, and C_{ADC} values, refer to Table 4-51 : ADC Characteristics.
2. $C_{parasitic}$ indicates PCB capacitance (depending on the quality of soldering and PCB wiring) and bonding pad capacitance (about 5pF). Higher values of $C_{parasitic}$ result in less accurate conversions. To solve this problem, f_{ADC} should be reduced.

General PCB Design Guidelines

The power supply should be decoupled as shown in the following figure and the details depend on the connection of VREFH and AVCC and the number of AVCC pins. 0.1μF capacitor should be (high quality) ceramic capacitor. These capacitors should be as close to the chip as possible.

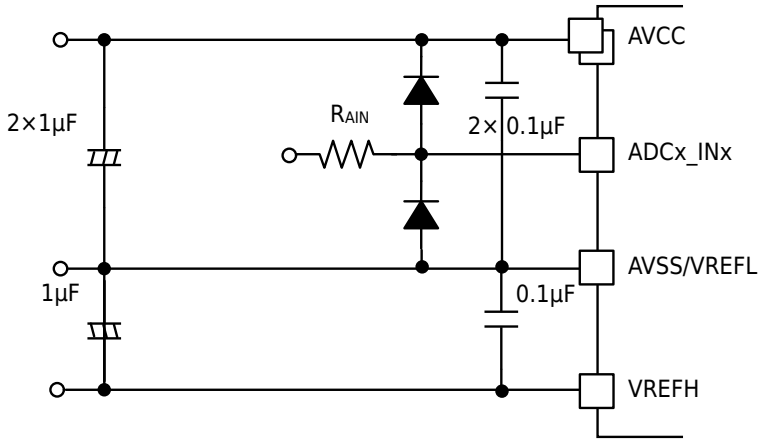


Figure 4-33 Power and Reference Power Decoupling Instances

1. For information about R_{AIN} values, refer to Table 4-51 : ADC Characteristics.

4.3.24 12-bit DAC Characteristics

Table 4-57 12-bit DAC Port Output Enabled and Output Amplifier Enabled Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{AVCC}(2)	Analog Power Voltage	-	1.8	3.3	3.63	V
Aref(2)	Reference power supply voltage (V_{REFH})	=V_{AVCC}	1.8	3.3	3.63	V
AO(2)	Output Voltage Range	-	0.2	-	Aref-0.2	-
RL(2)	Load Resistance	-	5	-	-	kΩ
CL(2)	Load Capacitance	-	-	-	50	pF
DNL(2)	Differential nonlinear error (deviation between two consecutive codes -1LSB)	-	-	-	3	LSB
INL(2)	Integral nonlinear error (the difference between the value measured at code I and the value at code I on the line between code 0 and the last code 4095)	-	-	-	5	LSB
OE(2)	Offset error (the difference between measured value at code 0x800 and ideal value VREF+/2)	V_{REFH}=3.63 V	-	-	±15	LSB
		V_{REFH}=1.8V	-	-	±25	LSB
GE(2)	Gain Error	-	-	-	±1	%
T_{st}(1)	Settling time (full scale: suitable for 12-bit input code conversion between the lowest input code and the highest input code when the DAC output reaches the final value of ±4LSB)	T_A=-40-105℃	-	1.2	2.5	μs
		T_A=-40-125℃	-	1.2	5	μs

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Iavcc(2)	Analog power supply current (quiescent current, no load)	-	-	604	800	μA
Iaref(2)	Reference supply current (quiescent current)	-	-	161	270	μA

Note

1. Guaranteed by design, not tested in production.
2. Resulted from comprehensive evaluation, not tested in production.

Table 4-58 12-bit DAC Port Output Enabled and Output Amplifier Disabled Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{AVCC}(2)	Analog Power Voltage	-	1.8	3.3	3.63	V
Aref(2)	Reference power supply voltage	=V_{AVCC}	1.8	3.3	3.63	V
AO(2)	Output Voltage Range	-	0	-	Aref-1LSB	V
CL(2)	Load Capacitance	-	-	-	20	pF
RO(2)	Output Resistance	-	-	8.6	12	kΩ
DNL	Differential nonlinear error (deviation between two consecutive codes -1LSB)	-	-	-	±2	LSB
TUE(2)	Total Unadjustable Error	-	-	-	±24	LSB
T_{st}(1)	Settling time (applicable to 12-bit input code conversion between the lowest input code and the highest input code when the DAC output reaches the final value of ±4LSB, CL=10pF)	T_A=-40-105℃	-	0.9	2	μs
		T_A=-40-125℃	-	0.9	5	μs
Iavcc(2)	Analog supply current (quiescent current)	-	-	0.1	2	μA
Iaref(2)	Reference supply current (quiescent current)	-	-	146	260	μA

Note

1. Guaranteed by design, not tested in production.
2. Resulted from comprehensive evaluation, not tested in production.

Table 4-59 12-bit DAC Port Output Disabled and Output Amplifier Disabled Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{AVCC}(2)	Analog Power Voltage	-	1.8	3.3	3.63	V
Aref(2)	Reference power supply voltage	=V_{AVCC}	1.8	3.3	3.63	V
AO(1)	Output Voltage Range	-	0	-	Aref-1LSB	V
DNL(1)	Differential nonlinear error (deviation between two consecutive codes -1LSB)	-	-	-	±2	LSB
TUE(1)	Total Unadjustable Error	-	-	-	±5	LSB

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
T_{st}(1)	Settling time (applicable to 12-bit input code conversion between the lowest input code and the highest input code when the DAC output reaches the final value of ±1LSB)	V_{AVCC}≥2.7	-	65.3	81	ns
	Settling time (applicable to 12-bit input code conversion between the lowest input code and the highest input code when the DAC output reaches the final value of ±32LSB)	V_{AVCC}≥2.7	-	36	44.9	ns
	Settling time (applicable to 12-bit input code conversion between the lowest input code and the highest input code when the DAC output reaches the final value of ±1LSB)	V_{AVCC}<2.7	-	-	83.82	ns
	Settling time (applicable to 12-bit input code conversion between the lowest input code and the highest input code when the DAC output reaches the final value of ±32LSB)	V_{AVCC}<2.7	-	-	48.55	ns
Iavcc(2)	Analog supply current (quiescent current)	-	-	0.1	2	μA
Iaref(2)	Reference supply current (quiescent current)	-	-	146	260	μA

Note

1. Guaranteed by design, not tested in production.
2. Resulted from comprehensive evaluation, not tested in production.

4.3.25 Temperature Sensor Characteristics

Table 4-60 Temperature Sensor Characteristics(2)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
T_L	Temperature Linearity	T_A=-40~105℃	-2	-	+2	℃
T_E	Absolute Accuracy(1)	25℃, 105℃ two-point calibration T_A=-40~105℃	-5	-	+4	℃

Note

1. The actual characteristics are related to the accuracy of the calibration point temperature. If the data preset by the chip is used for calibration, the characteristics are not guaranteed because of the temperature deviation in the mass production test environment.
2. Resulted from comprehensive evaluation, not tested in production.

4.3.26 Comparator Characteristics

Table 4-61 Comparator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{AVCC}(2)	Analog Power Voltage	-	1.8	3.3	3.63	V
V_I(2)	Input Voltage Range	-	0	-	V_{AVCC}	V
T_{cmp}(1)	compare Time	Comparator Resolution Voltage =100mV	-	30	50	ns
T_{set}(2)	Input Channel Switching Stabilization Time	-	-	100	200	ns

Note

1. Guaranteed by design, not tested in production.
2. Resulted from comprehensive evaluation, not tested in production.

4.3.27 EXMC Characteristics

Table 4-62 EXMC Characteristics in Internal EXCLK Mode

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
t_add_d	Address line output delay time	2.7V≤V_{CC}≤3.63V	-	-	5	ns
		1.8V≤V_{CC}<2.7V	-	-	7	ns
t_data_d	Data line output delay time	2.7V≤V_{CC}≤3.63V	-	-	5	ns
		1.8V≤V_{CC}<2.7V	-	-	7	ns
t_ce_d	CE output delay time	2.7V≤V_{CC}≤3.63V	-	-	5	ns
		1.8V≤V_{CC}<2.7V	-	-	7	ns
t_we_d	WE output delay time	2.7V≤V_{CC}≤3.63V	-	-	5	ns
		1.8V≤V_{CC}<2.7V	-	-	7	ns
t_oe_d	OE output delay time	2.7V≤V_{CC}≤3.63V	-	-	5	ns
		1.8V≤V_{CC}<2.7V	-	-	7	ns
t_baa_d	BAA output delay time	2.7V≤V_{CC}≤3.63V	-	-	5	ns
		1.8V≤V_{CC}<2.7V	-	-	7	ns
t_adv_d	ADV output delay time	2.7V≤V_{CC}≤3.63V	-	-	5	ns
		1.8V≤V_{CC}<2.7V	-	-	7	ns
t_ale_d	ALE output delay time	2.7V≤V_{CC}≤3.63V	-	-	5	ns
		1.8V≤V_{CC}<2.7V	-	-	7	ns
t_data_s	Data line input setup time	2.7V≤V_{CC}≤3.63V	5	-	-	ns
		1.8V≤V_{CC}<2.7V	7	-	-	ns
t_data_h	Data line input Hold time	-	0	-	-	ns

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
t_rb_s	RB input Setup time	2.7V≤V_{CC}≤3.63V	5	-	-	ns
		1.8V≤V_{CC}<2.7V	7	-	-	ns
t_rb_h	RB input Hold time	-	0	-	-	ns

Table 4-63 EXMC Characteristics in Feedback EXCLK Mode

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
t_add_d	Address line output delay time	2.7V≤V_{CC}≤3.63V	-	-	5	ns
		1.8V≤V_{CC}<2.7V	-	-	7	ns
t_data_d	Data line output delay time	2.7V≤V_{CC}≤3.63V	-	-	5	ns
		1.8V≤V_{CC}<2.7V	-	-	7	ns
t_ce_d	CE output delay time	2.7V≤V_{CC}≤3.63V	-	-	5	ns
		1.8V≤V_{CC}<2.7V	-	-	7	ns
t_we_d	WE output delay time	2.7V≤V_{CC}≤3.63V	-	-	5	ns
		1.8V≤V_{CC}<2.7V	-	-	7	ns
t_oe_d	OE output delay time	2.7V≤V_{CC}≤3.63V	-	-	5	ns
		1.8V≤V_{CC}<2.7V	-	-	7	ns
t_baa_d	BAA output delay time	2.7V≤V_{CC}≤3.63V	-	-	5	ns
		1.8V≤V_{CC}<2.7V	-	-	7	ns
t_adv_d	ADV output delay time	2.7V≤V_{CC}≤3.63V	-	-	5	ns
		1.8V≤V_{CC}<2.7V	-	-	7	ns
t_ale_d	ALE output delay time	2.7V≤V_{CC}≤3.63V	-	-	5	ns
		1.8V≤V_{CC}<2.7V	-	-	7	ns
t_data_s	Data line input setup time	-	2	-	-	ns
t_data_h	Data line input Hold time	2.7V≤V_{CC}≤3.63V	2	-	-	ns
		1.8V≤V_{CC}<2.7V	5	-	-	ns
t_rb_s	RB input Setup time	-	2	-	-	ns
t_rb_h	RB input Hold time	2.7V≤V_{CC}≤3.63V	2	-	-	ns
		1.8V≤V_{CC}<2.7V	5	-	-	ns

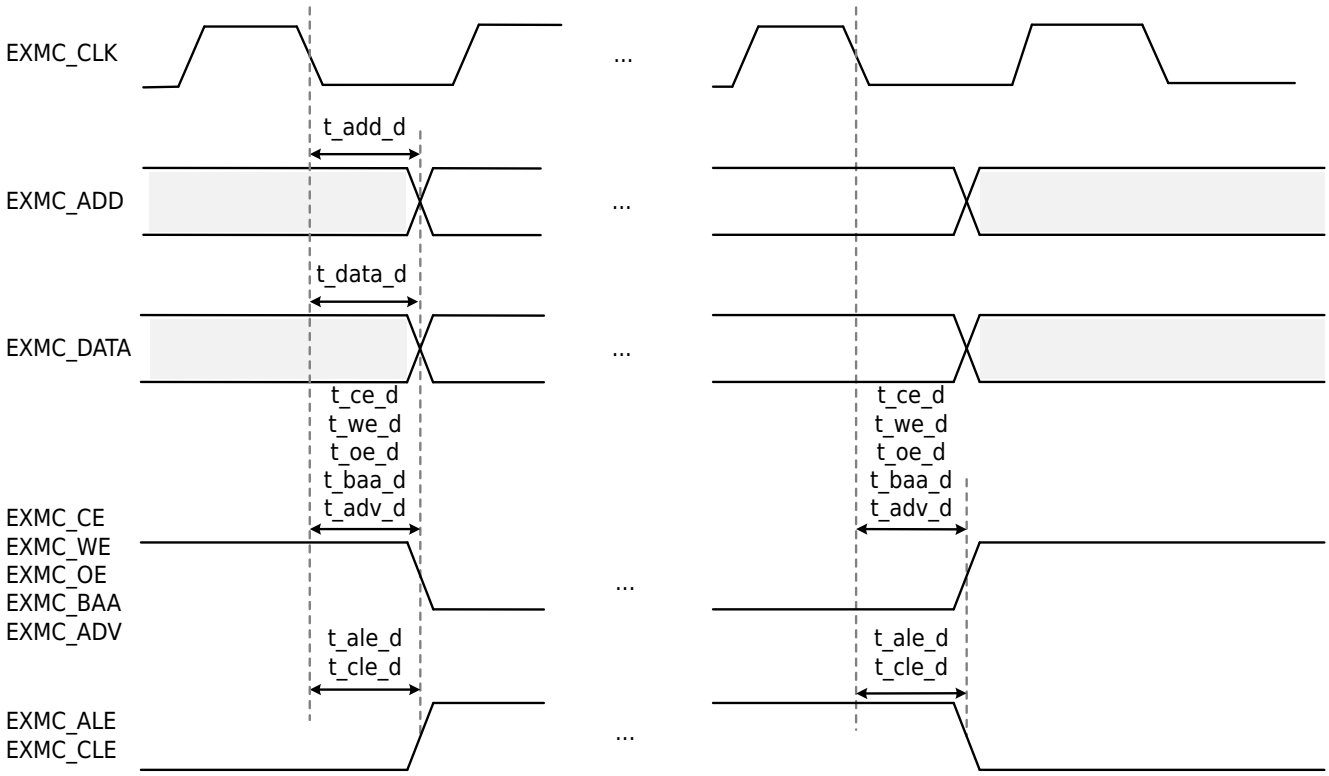


Figure 4-34 EXMC Output Signal Timing Diagram

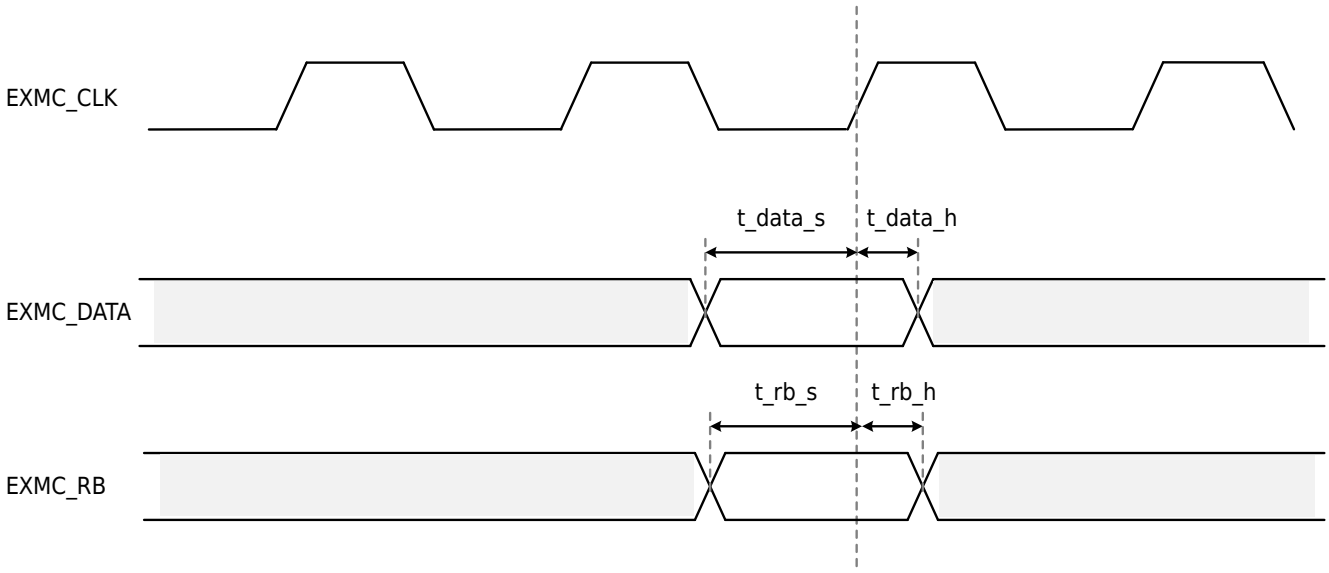


Figure 4-35 EXMC Input Signal Timing Diagram

4.3.28 DVP Characteristics

Table 4-64 DVP Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
t_pixclk_s(1)	Input data DVP_PIXCLK setup time	2.7V≤V_{CC}≤3.63V	6	-	-	ns
		1.8V≤V_{CC}<2.7V	9	-	-	ns
t_pixclk_h(1)	Input data DVP_PIXCLK hold time	2.7V≤V_{CC}≤3.63V	6	-	-	ns
		1.8V≤V_{CC}<2.7V	9	-	-	ns
t_data_s	Input data DVP_DATA setup time	2.7V≤V_{CC}≤3.63V	2.5	-	-	ns
		1.8V≤V_{CC}<2.7V	4	-	-	ns
t_data_h	Input data DVP_DATA hold time	2.7V≤V_{CC}≤3.63V	2	-	-	ns
		1.8V≤V_{CC}<2.7V	3	-	-	ns
t_vsync_s	Input data DVP_VSYNC setup time	2.7V≤V_{CC}≤3.63V	2.5	-	-	ns
		1.8V≤V_{CC}<2.7V	4	-	-	ns
t_vsync_h	Input data DVP_VSYNC hold time	2.7V≤V_{CC}≤3.63V	1.5	-	-	ns
		1.8V≤V_{CC}<2.7V	3	-	-	ns
t_hsync_s	Input data DVP_HSYNC setup time	2.7V≤V_{CC}≤3.63V	2.5	-	-	ns
		1.8V≤V_{CC}<2.7V	4	-	-	ns
t_hsync_h	Input data DVP_HSYNC hold time	2.7V≤V_{CC}≤3.63V	1.5	-	-	ns
		1.8V≤V_{CC}<2.7V	3	-	-	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.

The following figure takes the high level of DVP_VSYNC and DVP_HSYNC as the synchronization interval and the falling edge of DVP_PIXCLK as an example.

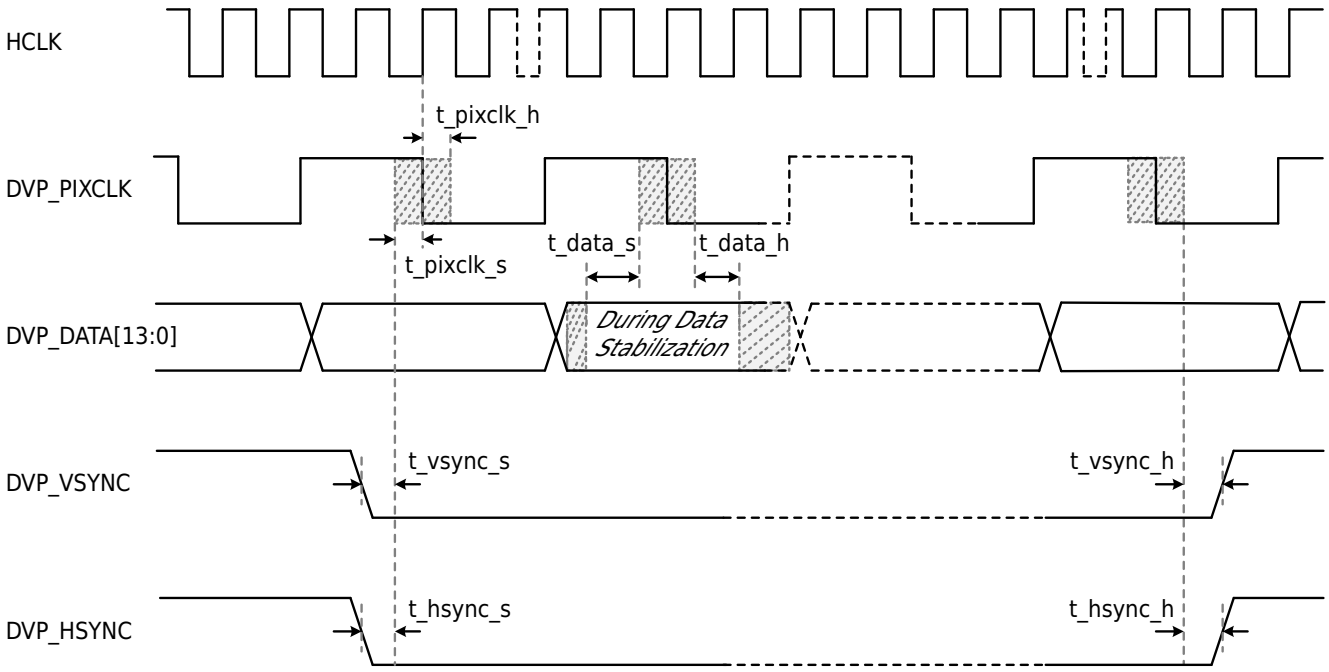


Figure 4-36 DVP Input Signal Timing Diagram

4.3.29 SDIO Characteristics

Table 4-65 Default Speed Mode Timing Parameters

Symbol	Parameters	Conditions	Min	Max	Unit
-	Operating Voltage	-	1.8	3.63	V
f_{PP}(1)	Transfer mode clock frequency	Load C=30pF	-	25	MHz
f_{OD}(1)	Card identification mode clock frequency	Load C=30pF	-	400	kHz
t_{WL}(1)	Clock low level time	Load C=30pF	10	-	ns
t_{WH}(1)	Clock high level time	Load C=30pF	10	-	ns
t_{TLH}(1)	Clock rise time	Load C=30pF	-	10	ns
t_{THL}(1)	Clock fall time	Load C=30pF	-	10	ns
t_{ISU}(1)	Data input setup time	Load C=30pF	5	-	ns
t_{IH}(1)	Data input hold time	Load C=30pF	14	-	ns
t_{ODLY}(1)	Data output delay	Load C=30pF	1	14	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.

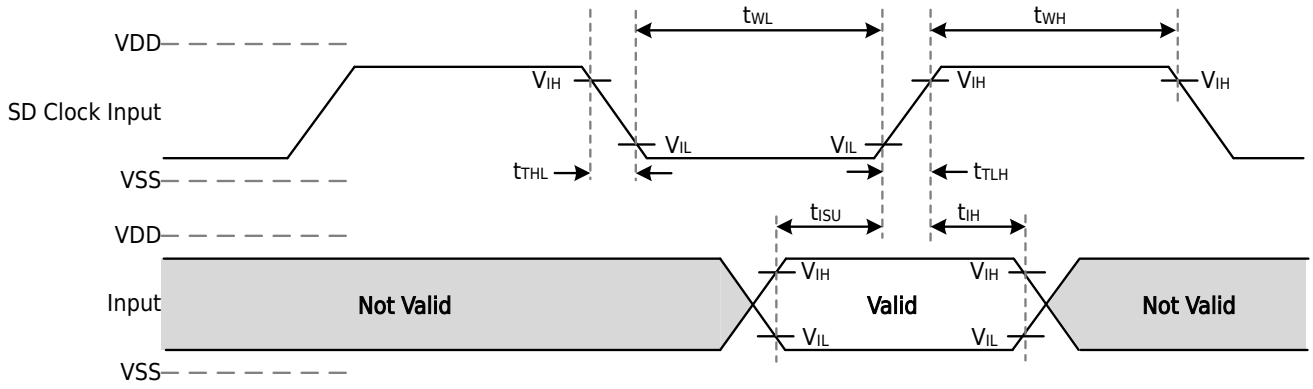


Figure 4-37 Default Speed Mode Input Timing Diagram

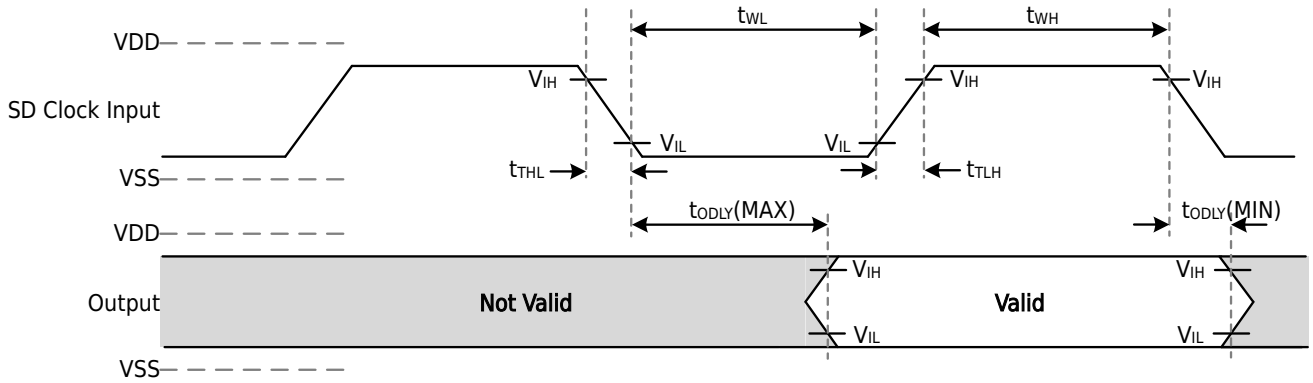


Figure 4-38 Default Speed Mode Output Timing Diagram

Table 4-66 High-Speed Mode Timing Parameters

Symbol	Parameters	Conditions	Min	Max	Unit
-	Operating Voltage	-	1.8	3.63	V
f_{PP}(1)	Transfer mode clock frequency	Load C=30pF	-	50	MHz
f_{OD}(1)	Card identification mode clock frequency	Load C=30pF	-	400	kHz
t_{WL}(1)	Clock low level time	Load C=30pF	7	-	ns
t_{WH}(1)	Clock high level time	Load C=30pF	7	-	ns
t_{TLH}(1)	Clock rise time	Load C=30pF	-	3	ns
t_{THL}(1)	Clock fall time	Load C=30pF	-	3	ns
t_{ISU}(1)	Data input setup time	Load C=30pF	5	-	ns
t_{IH}(1)	Data input hold time	Load C=30pF	14	-	ns
t_{ODLY}(1)	Data output delay	Load C=30pF	-	14	ns
t_{OH}(1)	Data output hold time	Load C=30pF	3	-	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.

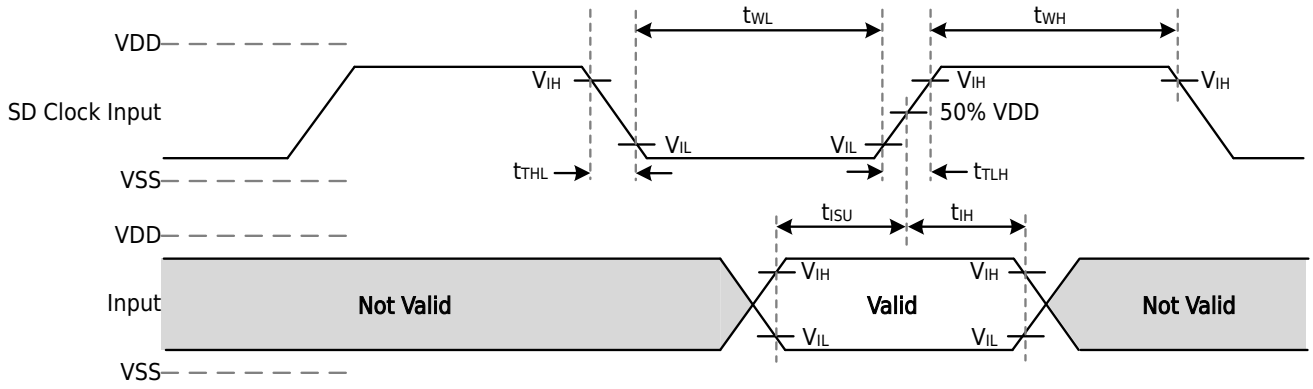


Figure 4-39 High-Speed Mode Input Timing Diagram

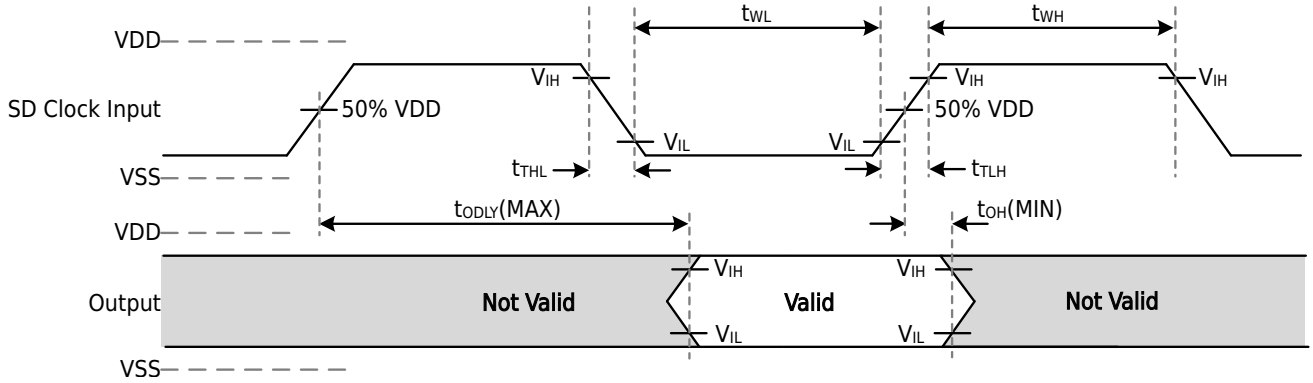


Figure 4-40 High-Speed Mode Output Timing Diagram

4.3.30 Programmable Gain Amplifier Characteristics

Table 4-67 Programmable Gain Amplifier Characteristics

Symbol	Parameters		Conditions	Min	Typ	Max	Unit
V_{AVCC}(1)	Analog Power Voltage		-	1.8	3.3	3.63	V
V_{OS}	Input Offset Voltage		-	-8	-	8	mV
V_I(1)	Input Voltage Range		Gain=2~32	0.1*V_{AVCC}/ Gain	-	0.9*V_{AVCC}/ Gain	V
G_E	Gain Error	Use external port PGAVSS as PGA negative phase input	Gain=2	-1	-	1	%
			Gain=2.133(1)	-1	-	1	%
			Gain=2.286(1)	-1	-	1	%
			Gain=2.667(1)	-1	-	1	%
			Gain=2.909(1)	-1	-	1	%
			Gain=3.2(1)	-1.5	-	1.5	%
			Gain=3.556(1)	-1.5	-	1.5	%
			Gain=4.0(1)	-1.5	-	1.5	%
			Gain=4.571(1)	-2	-	2	%
			Gain=5.333(1)	-2	-	2	%
			Gain=6.4(1)	-3.0	-	3.0	%
			Gain=8(1)	-3.0	-	3.0	%

Symbol	Parameters		Conditions	Min	Typ	Max	Unit
G_E	Gain Error	Use external port PGAVSS as PGA negative phase input	Gain=10.667(1)	-4.0	-	4.0	%
			Gain=16(1)	-4.0	-	4.0	%
			Gain=32	-7.0	-	7.0	%
		Use the internal analog ground AVSS as the PGA negative phase input	Gain=2	-2	-	2	%
			Gain=2.133(1)	-2	-	2	%
			Gain=2.286(1)	-2	-	2	%
			Gain=2.667(1)	-2	-	2	%
			Gain=2.909(1)	-2	-	2	%
			Gain=3.2(1)	-2.5	-	2.5	%
			Gain=3.556(1)	-2.5	-	2.5	%
			Gain=4.0(1)	-2.5	-	2.5	%
			Gain=4.571(1)	-3.0	-	3.0	%
			Gain=5.333(1)	-3.0	-	3.0	%
			Gain=6.4(1)	-4.0	-	4.0	%
			Gain=8(1)	-4.0	-	4.0	%
			Gain=10.667(1)	-5.0	-	5.0	%
			Gain=16(1)	-5.0	-	5.0	%
			Gain=32	-8.0	-	8.0	%

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.31 VBAT Characteristics

Table 4-68 VBAT Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{BATLVD}(1)	Low voltage monitoring voltage	PWC_PWRC4.VBATREFSEL=0	1.70	1.80	1.90	V
		PWC_PWRC4.VBATREFSEL=1	2.00	2.10	2.20	V

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.32 EIRQ Filter Characteristics

Table 4-69 EIRQ Filter Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
W_{F_EIRQ}(1)	EIRQ input filter width	INTC_NOCCR.NOCSEL=0b00	0.4	-	1.4	μs
		INTC_NOCCR.NOCSEL=0b01	0.8	-	2.8	μs
		INTC_NOCCR.NOCSEL=0b10	1.7	-	5.6	μs
		INTC_NOCCR.NOCSEL=0b11	3.4	-	11.2	μs

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.33 RX Filter Characteristics in STOP Mode of USART1

Table 4-70 RX Filter Characteristics in STOP Mode of USART1

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
W_{F_USART1}(1)	USART1 input filter width	USART1_NFC.USART1_NFS=0b00	0.4	-	1.4	μs
		USART1_NFC.USART1_NFS=0b01	0.8	-	2.8	μs
		USART1_NFC.USART1_NFS=0b10	1.7	-	5.6	μs
		USART1_NFC.USART1_NFS=0b11	3.4	-	11.2	μs

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.34 Filter Characteristics in STOP Mode of USB chip-integrated Full-Speed PHY

Table 4-71 Filter Characteristics in STOP Mode of USB chip-integrated Full-Speed PHY

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
W_{F_USB}(1)	USB input filter width	USB_SYCTLREG.USBFS_NFS=0b00 USB_SYCTLREG.USBHS_NFS=0b00	0.4	-	1.4	μs
		USB_SYCTLREG.USBFS_NFS=0b01 USB_SYCTLREG.USBHS_NFS=0b01	0.8	-	2.8	μs
		USB_SYCTLREG.USBFS_NFS=0b10 USB_SYCTLREG.USBHS_NFS=0b10	1.7	-	5.6	μs
		USB_SYCTLREG.USBFS_NFS=0b11 USB_SYCTLREG.USBHS_NFS=0b11	3.4	-	11.2	μs

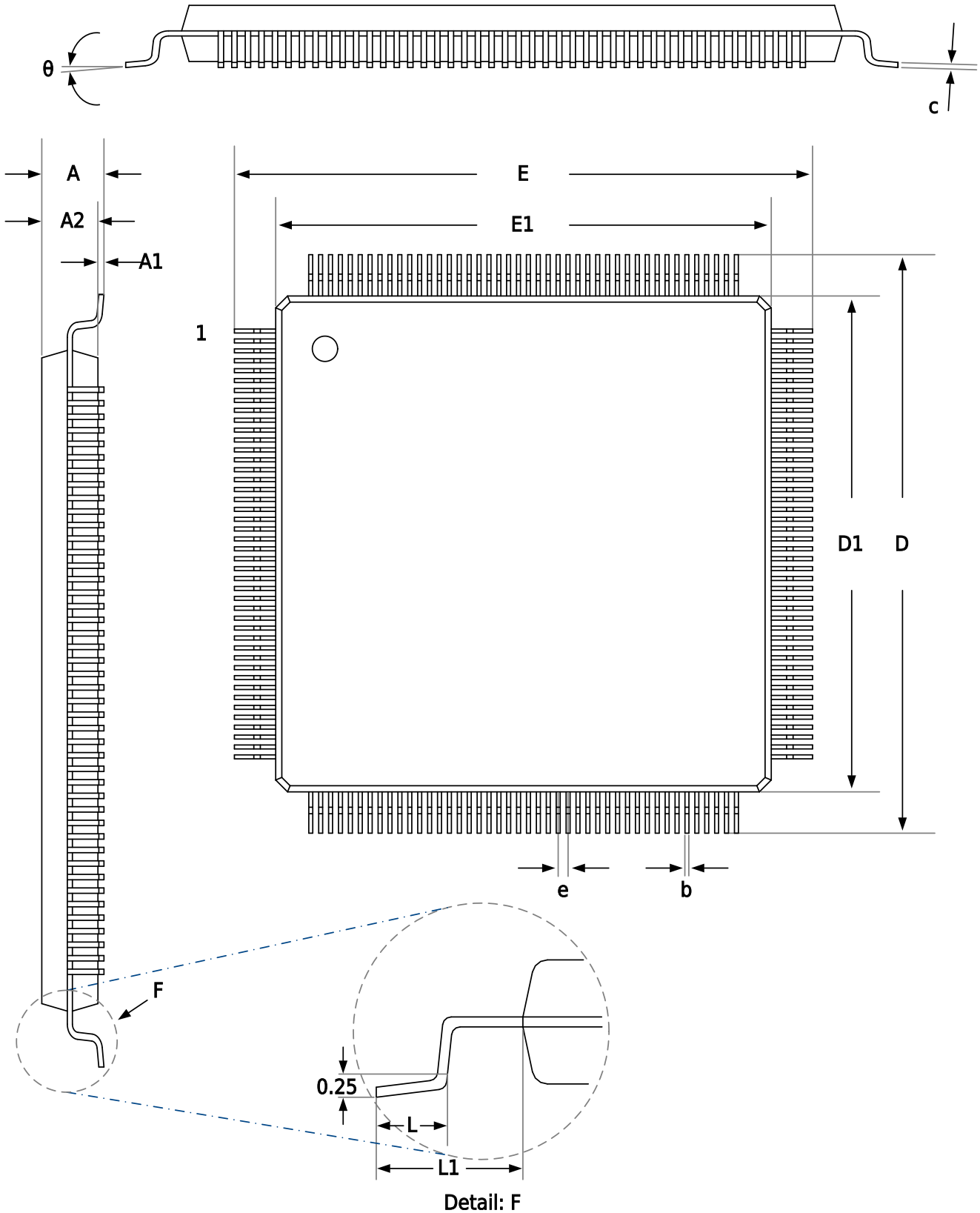
Note

1. Resulted from comprehensive evaluation, not tested in production.

5 Package Specifications

5.1 Package Dimensions

5.1.1 LQFP176 Package

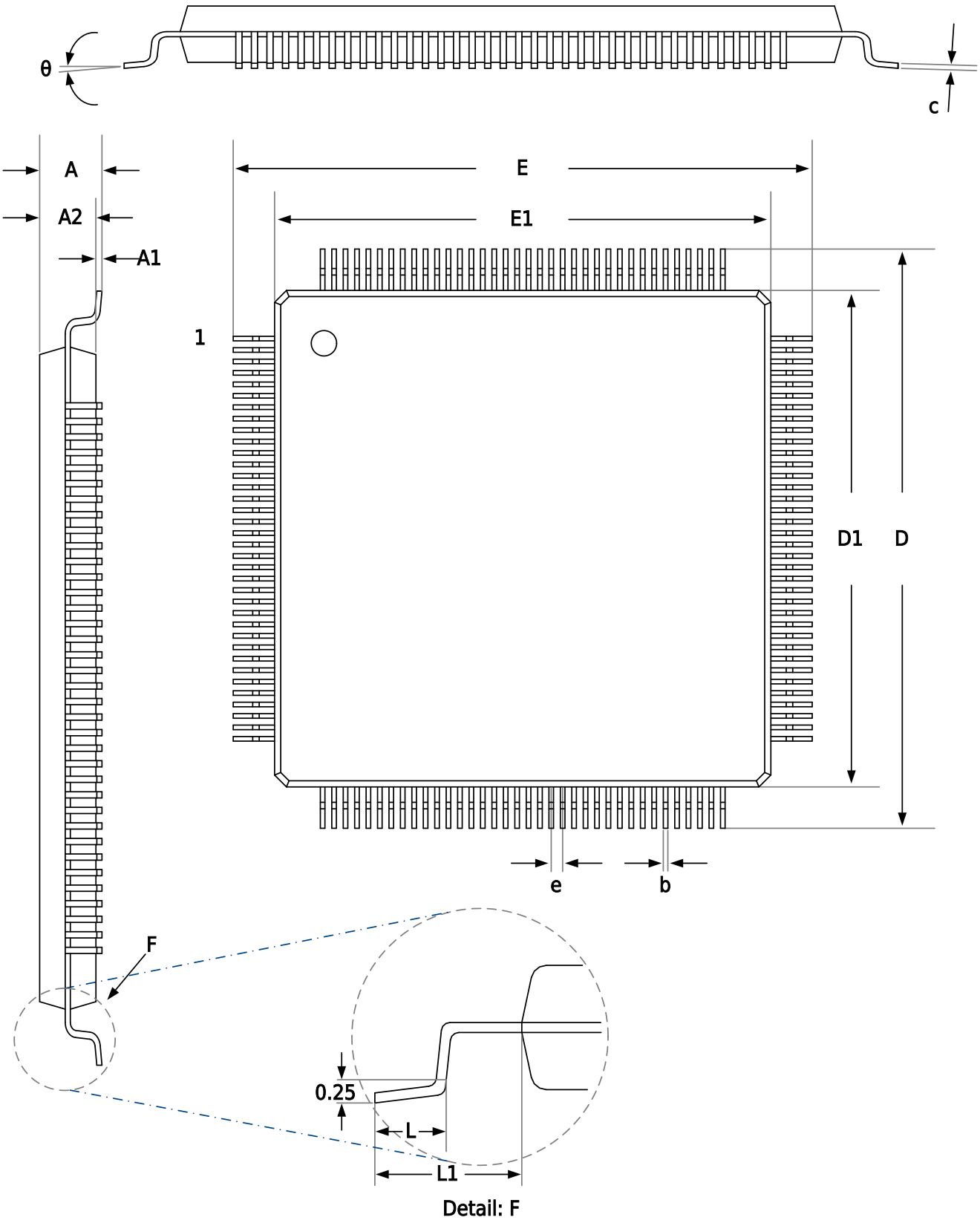


Symbol	24*24 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	25.80	26.00	26.20
D1	23.90	24.00	24.10
E	25.80	26.00	26.20
E1	23.90	24.00	24.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	3.5°	7°

Note

Dimensions "D1" and "E1" do not include mold flash.

5.1.2 LQFP144 Package

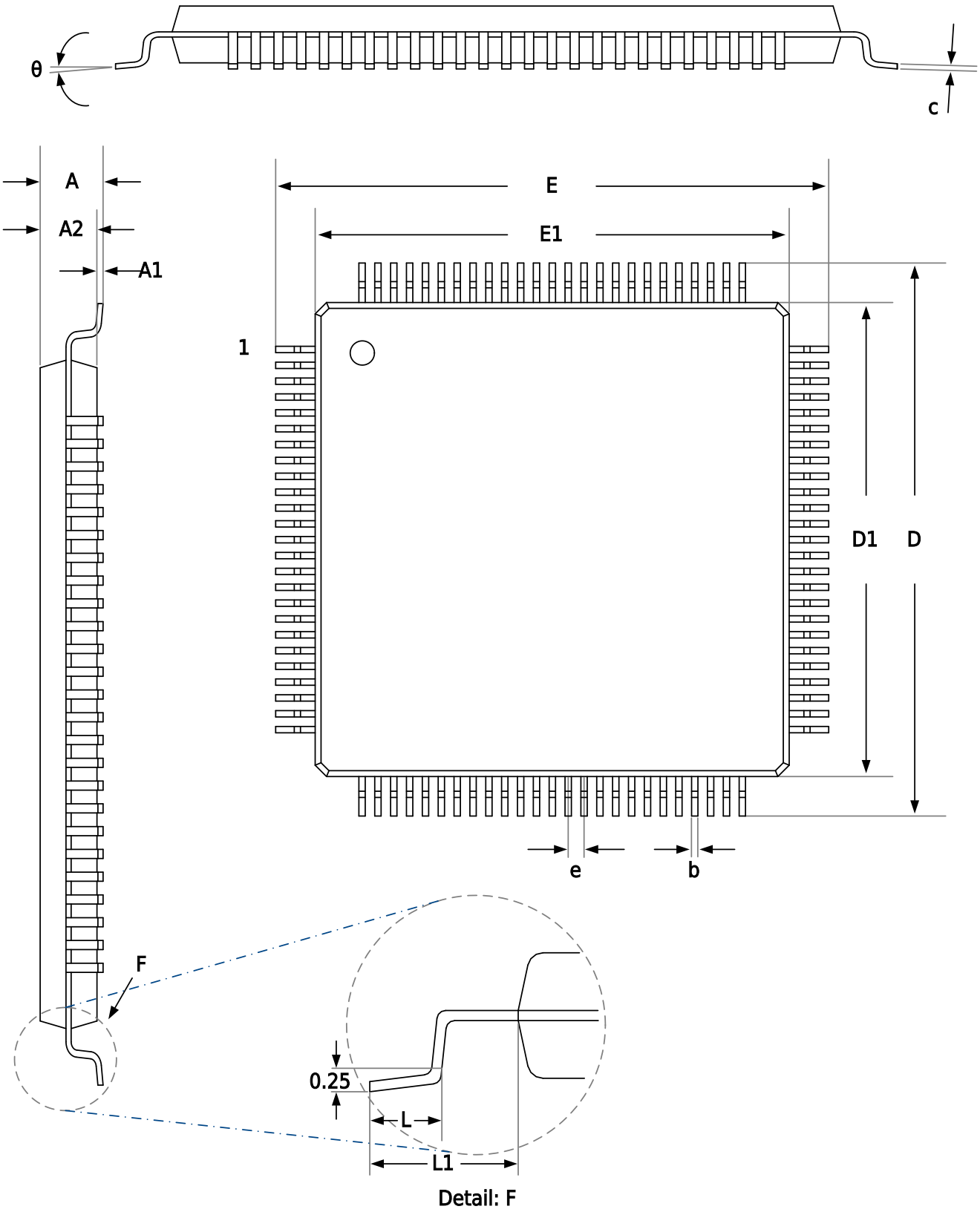


Symbol	20*20 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	3.5°	7°

Note

Dimensions "D1" and "E1" do not include mold flash.

5.1.3 LQFP100 Package



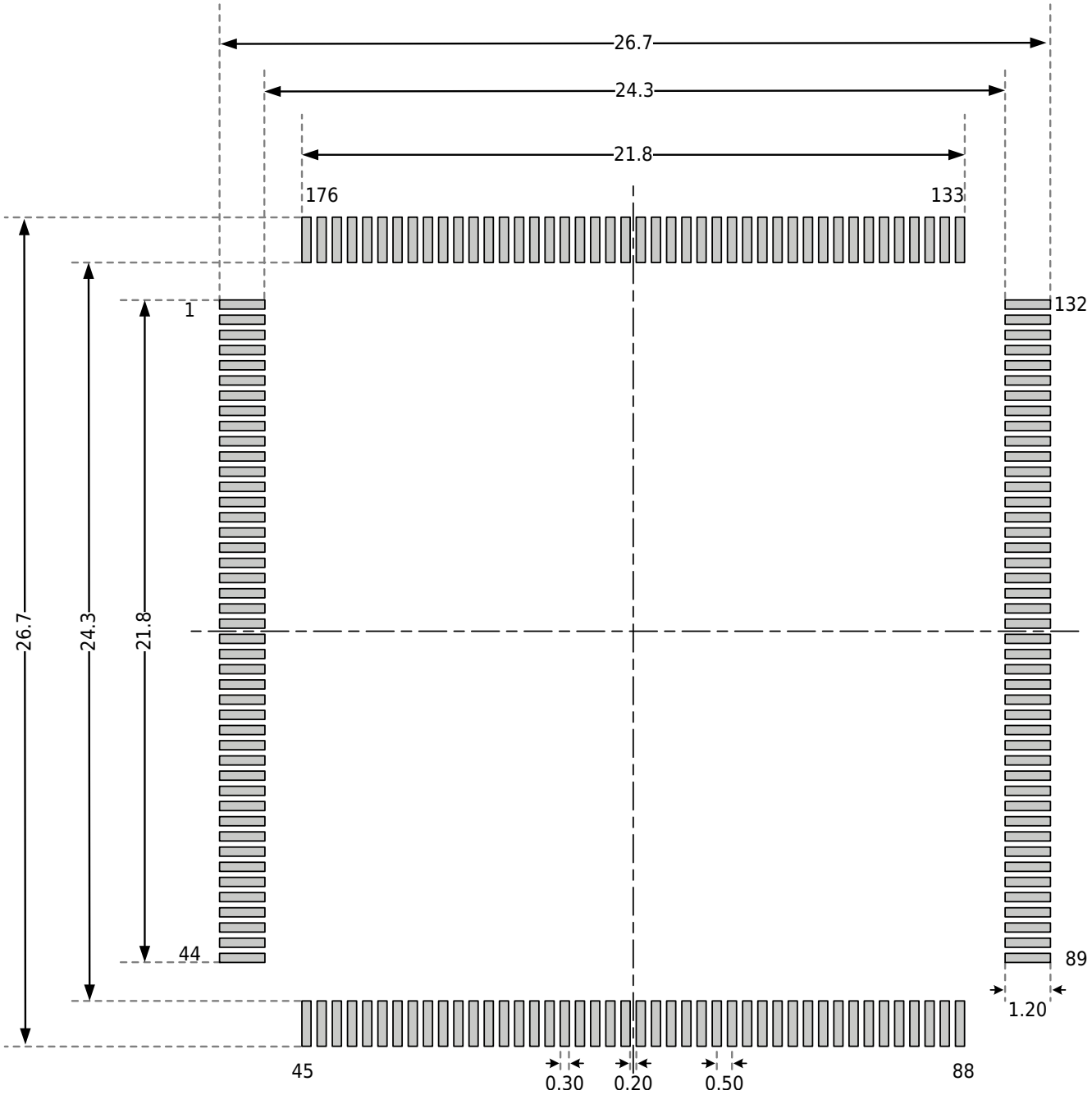
Symbol	14*14 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	3.5°	7°

Note

Dimensions "D1" and "E1" do not include mold flash.

5.2 PCB Land Pattern

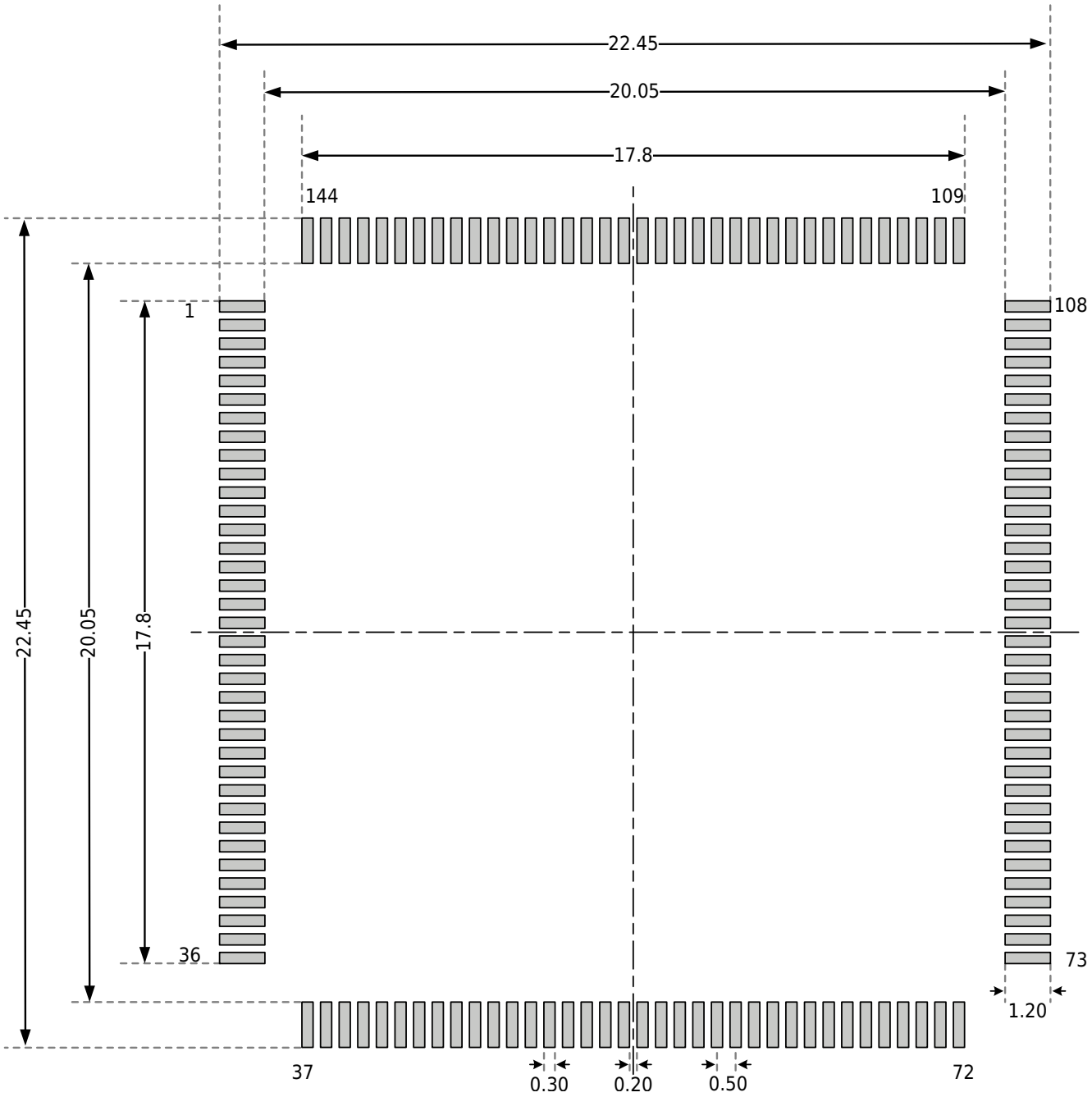
5.2.1 LQFP176 Package (24mm*24mm)



Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

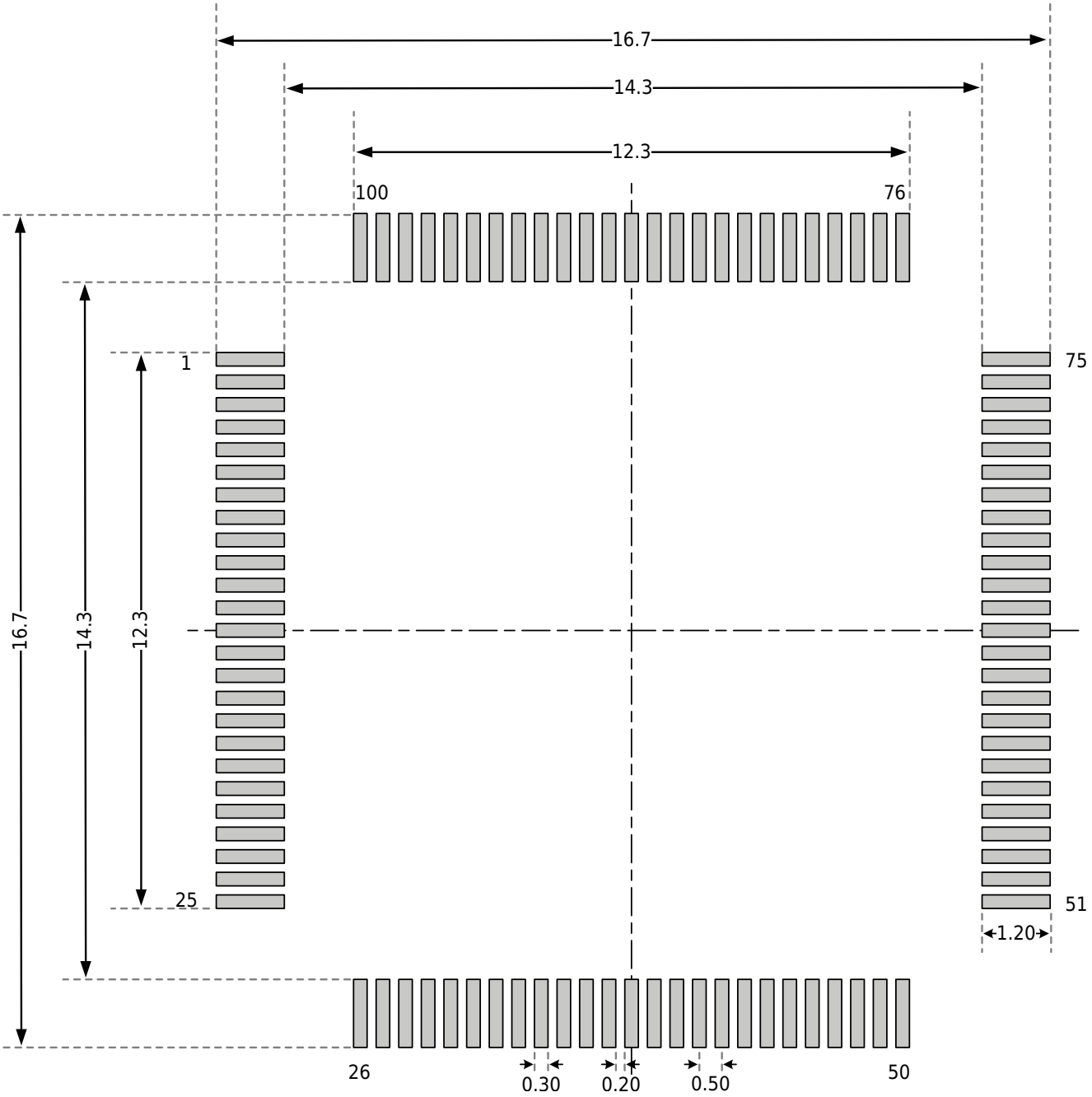
5.2.2 LQFP144 Package (20mm*20mm)



Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

5.2.3 LQFP100 Package (14mm*14mm)



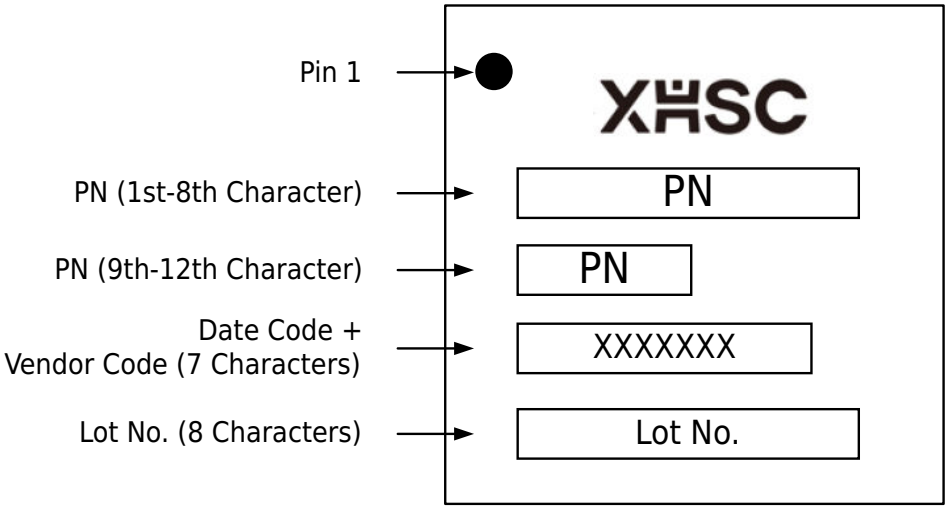
Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

5.3 Package Marking

The location and information description of Pin1 on the front of each package are given below.

LQFP100 Package (14mm*14mm)/LQFP144 Package (20mm*20mm)/LQFP176 Package (24mm*24mm)



5.4 Packaging Thermal Resistance Coefficient

When the packaged chip is working at the specified working environment temperature, the junction temperature T_j(℃) of the chip surface can be calculated according to the following formula:

$T_j = T_A + (P_D * \theta_{JA})$

- T_A refers to the working environment temperature when the packaged chip is working, the unit is ℃;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is ℃/W;
- P_D refers to total power dissipation, which is the sum of internal power consumption (P_{INT}) and I/O pin power consumption (P_{IO}), the unit is W.

  $P_D = P_{INT} + P_{IO}$

  - P_{INT}: Internal power consumption, calculated as the product of Icc and Vcc.
  - P_{IO}: I/O pin power consumption, calculated as: $P_{IO} = \Sigma(V_{OL} * I_{OL}) + \Sigma((V_{CC} - V_{OH}) * I_{OH})$

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable junction temperature T_J of the chip.

Table 5-4 Thermal Resistance Coefficient Table For Each Package

Package Type and Dimensions	Thermal Resistance Parameters (θ_{JA})	Unit
LQFP176 24mm*24mm/0.5mm pitch	39.06±10%	℃/W
LQFP144 20mm*20mm/0.5mm pitch	40±10%	℃/W
LQFP100 14mm*14mm/0.5mm pitch	42.5±10%	℃/W

6 Ordering Information

Part Number		HC32A4A8SITI-LQFP176	HC32A4A8RITI-LQFP144	HC32A4A8PITI-LQFP100	HC32A4A8SITJ-LQFP176	HC32A4A8RITJ-LQFP144	HC32A4A8PITJ-LQFP100
GPIO		142	116	83	142	116	83
CPU	Core	Cortex-M4	Cortex-M4	Cortex-M4	Cortex-M4	Cortex-M4	Cortex-M4
	Frequency	240MHz	240MHz	240MHz	200MHz	200MHz	200MHz
Memory	Flash	2048KB	2048KB	2048KB	2048KB	2048KB	2048KB
	OTP	134KB	134KB	134KB	134KB	134KB	134KB
	SRAM	512+4KB	512+4KB	512+4KB	512+4KB	512+4KB	512+4KB
Power supply voltages		1.8~3.63V	1.8~3.63V	1.8~3.63V	2.7~3.63V	2.7~3.63V	2.7~3.63V
Temp Range		-40~105℃	-40~105℃	-40~105℃	-40~125℃	-40~125℃	-40~125℃
DMA		2unit*8ch	2unit*8ch	2unit*8ch	2unit*8ch	2unit*8ch	2unit*8ch
TIMER	Timer0	5unit	5unit	5unit	5unit	5unit	5unit
	Timer2	4unit	4unit	4unit	4unit	4unit	4unit
	TimerA	12unit	12unit	12unit	12unit	12unit	12unit
	Timer4	3unit	3unit	3unit	3unit	3unit	3unit
	Timer6	8unit	8unit	8unit	8unit	8unit	8unit
RTC		1ch	1ch	1ch	1ch	1ch	1ch
WDT		1ch	1ch	1ch	1ch	1ch	1ch
SWDT		1ch	1ch	1ch	1ch	1ch	1ch
Connectivity	USART	10ch	10ch	10ch	10ch	10ch	10ch
	I2C	6ch	6ch	6ch	6ch	6ch	6ch
	SPI	6ch	6ch	6ch	6ch	6ch	6ch
	QSPI	1ch	1ch	1ch	1ch	1ch	1ch
	USB	USB2.0 OTG_FS+ USB2.0 OTG_HS	USB2.0 OTG_FS+ USB2.0 OTG_HS	USB2.0 OTG_FS+ USB2.0 OTG_HS	USB2.0 OTG_FS+ USB2.0 OTG_HS	USB2.0 OTG_FS+ USB2.0 OTG_HS	USB2.0 OTG_FS+ USB2.0 OTG_HS
	CAN FD	4ch	4ch	4ch	4ch	4ch	4ch
	EXMC	√	√	√	√	√	√
	ETHMAC	1ch	1ch	1ch	1ch	1ch	1ch
	I2S	4ch	4ch	4ch	4ch	4ch	4ch
	SDIO	2ch	2ch	2ch	2ch	2ch	2ch

Part Number		HC32A4A8SITI-LQFP176	HC32A4A8RITI-LQFP144	HC32A4A8PITI-LQFP100	HC32A4A8SITJ-LQFP176	HC32A4A8RITJ-LQFP144	HC32A4A8PITJ-LQFP100
Connectivity	DVP	√	√	√	√	√	√
Analog	12-bit ADC	3unit, 28ch	3unit, 24ch	3unit, 16ch	3unit, 28ch	3unit, 24ch	3unit, 16ch
	12-bit DAC	4ch	4ch	4ch	4ch	4ch	4ch
	PGA	4ch	4ch	4ch	4ch	4ch	4ch
	OTS	√	√	√	√	√	√
	CMP	4ch	4ch	4ch	4ch	4ch	4ch
	PVD	√	√	√	√	√	√
Security	HSM Light-Mid	√	√	√	√	√	√
	SKE	√	√	√	√	√	√
	PKE	√	√	√	√	√	√
	TRNG	√	√	√	√	√	√
	Hash	SHA256	SHA256	SHA256	SHA256	SHA256	SHA256
Co-processing	FMAC	√	√	√	√	√	√
	MAU	√	√	√	√	√	√
	DCU	8ch	8ch	8ch	8ch	8ch	8ch
ERMU		√	√	√	√	√	√
Package (mm*mm)		LQFP176(24*24)	LQFP144(20*20)	LQFP100(14*14)	LQFP176(24*24)	LQFP144(20*20)	LQFP100(14*14)
Packing		Tray	Tray	Tray	Tray	Tray	Tray
Pitch		0.5mm	0.5mm	0.5mm	0.5mm	0.5mm	0.5mm

Please contact the sales window for the latest mass production information before ordering.

Revision History

Revision/Date	Changes
Rev1.00 Jul. 16, 2025	First official release.