

HC32F002 Series

32-bit ARM[®] Cortex[®]-M0+ Microcontroller

Datasheet

Rev1.50
August 2026

Feature List

Support Features

- 48MHz Cortex-M0+ 32-bit CPU platform
- HC32F002 Series has a flexible power management system:
 - ▶ 5μA@3V DeepSleep mode: all clocks off, power-on reset active, IO state retention, IO interrupt active, all registers, RAM and CPU data save state power consumption
 - ▶ 15μA/MHz@3V@48MHz Sleep mode: CPU halted, peripherals are enable to run, main clock running
 - ▶ 100μA/MHz@3V@48MHz operating mode: CPU and peripherals are enable to run, program running from Flash
- 18KB FLASH memory, with erase and write protection function, supports ISP, ICP, IAP, security protection level-4
- 2KB RAM memory
- GPIO: 22IO/24pin, 18IO/20pin
- Clock, Crystal
 - ▶ RCH: 44.24/48MHz
 - ▶ RCL: 32.768/38.4kHz
 - ▶ External input: 1-16MHz
- Timer/Counter
 - ▶ 1 CTIM can be configured either as one 16-bit General-Purpose Timer (GTIM) or as three 16-bit Basic Timers (BTIMs). In GTIM mode, it supports 4-channel capture/compare and 4-channel PWM output. In BTIM mode, each timer provides two toggle outputs
 - ▶ 1 advanced 16-bit timer (ATIM3) , supports 3-phase complementary PWM output
 - ▶ 1 Independent Watchdog, Internal Low-Speed Clock provides IWDG counting
 - ▶ 1 window watchdog circuit uses system clock
 - ▶ 1 low-power 16-bit timer supports automatic wake
 - ▶ 1 CM0+ integrated 24-bit SysTick Timer
- Communication interface
 - ▶ 2-channel LPUART communication interface
 - ▶ 1-channel SPI standard communication interface
 - ▶ 1-channel I2C standard communication interface
- Timer as buzzer frequency generator
- Globally unique 10-byte ID number
- 128-byte OTP memory, writable only via a dedicated programmer
- Integrate a high-speed and high-precision SAR ADC with a 10-bit 1Msps sampling
- Integrate LVD, configurable 16-level comparison level, can monitor port voltage and power supply voltage
- SWD debugging solution provides a full-featured debugger
- Working Conditions:
 - 20-105°C, 1.7-5.5V
 - 40-105°C, 2.7-5.5V
- Package: QFN24/20, TSSOP24/20

Support Model

HC32F002C4PZ-TSSOP20	HC32F002C4UZ-ZFN20TR
HC32F002D4PZ-TSSOP24	HC32F002D4UZ-QFN24TR
HC32F002C4PZ-TSSOP20TR	HC32F002D4PZ-TSSOP24TR
HC32F002C4PB-TSSOP20	HC32F002C4UB-ZFN20TR
HC32F002D4PB-TSSOP24	HC32F002D4UB-QFN24TR
HC32F002C4PB-TSSOP20TR	HC32F002D4PB-TSSOP24TR

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Preface

Number Format

- 0x prefix is used for hexadecimal numbers
- 0b prefix is used for binary numbers
- Numbers without prefix are in decimal representation

Security Statement

There may be potential security problems due to the use of a certain function or protocol, which need to be declared to remind users and avoid security risks.

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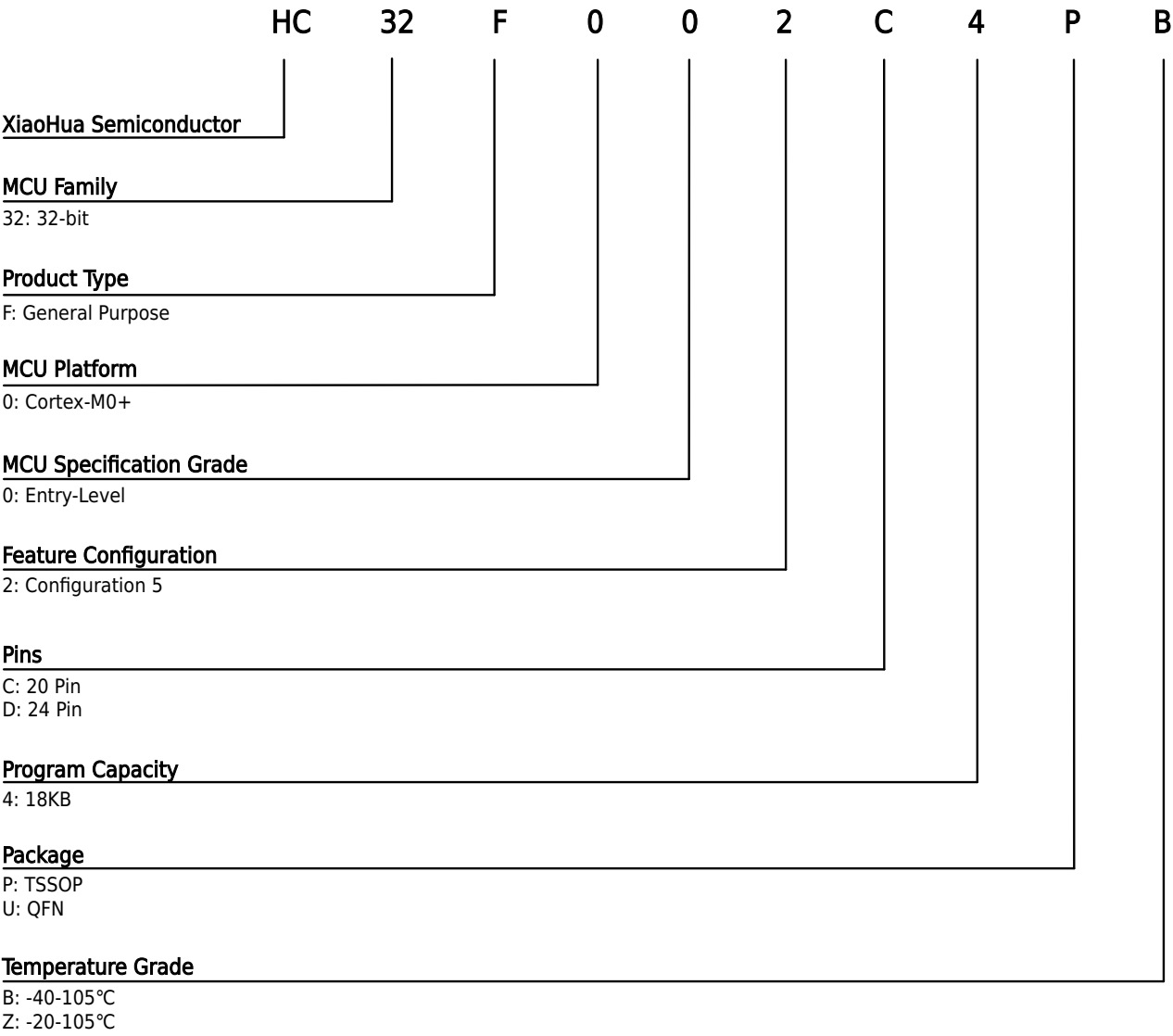
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1 Product Overview

1.1 Product Lineup

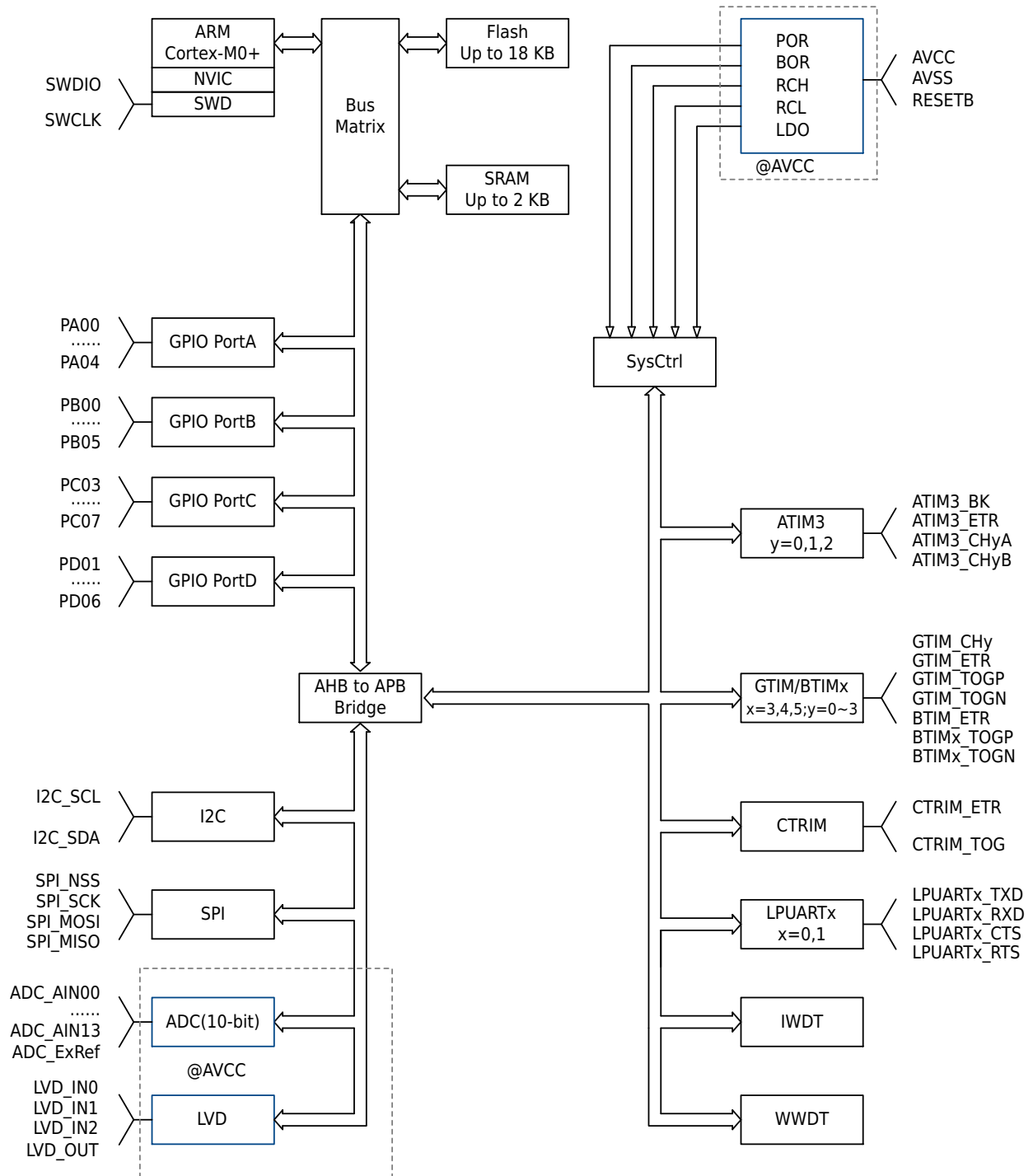
Product Name



Model Function Comparison Table

Product Name		HC32F002C4PZ	HC32F002C4UZ	HC32F002D4PZ	HC32F002D4UZ	HC32F002C4PB	HC32F002C4UB	HC32F002D4PB	HC32F002D4UB
Pins		20	20	24	24	20	20	24	24
GPIOs		18	18	22	22	18	18	22	22
CPU	Core	Cortex-M0+							
	Frequency	48MHz							
Memory	Flash	18KB							
	RAM	2KB							
Clock	RCH	44.24/48MHz							
	RCL	32.768/38.4kHz							
Power Voltage Range		1.7-5.5V				2.7-5.5V			
Temperature Range		-20-105℃				-40-105℃			
Timer		Advanced Timer ATIM3 General Timer GTIM of BTIM3/4/5 Low Power Timer CTRIM							
Watchdog Timer		IWDT *1 WWDT *1							
Connectivity	LPUART	LPUART0/1							
	I2C	I2C							
	SPI	SPI							
ADC, 10-bit		11ch+1ch (internal)		14ch+1ch (internal)		11ch+1ch (internal)		14ch+1ch (internal)	
LVD		Support							
Buzzer		Support (Max 4ch)							
Flash Security Protection		Support							
Debug Function		SWD debug interface							
Package (mm*mm)		TSSOP20	QFN20 (3*3)	TSSOP24	QFN24 (4*4)	TSSOP20	QFN20 (3*3)	TSSOP24	QFN24 (4*4)

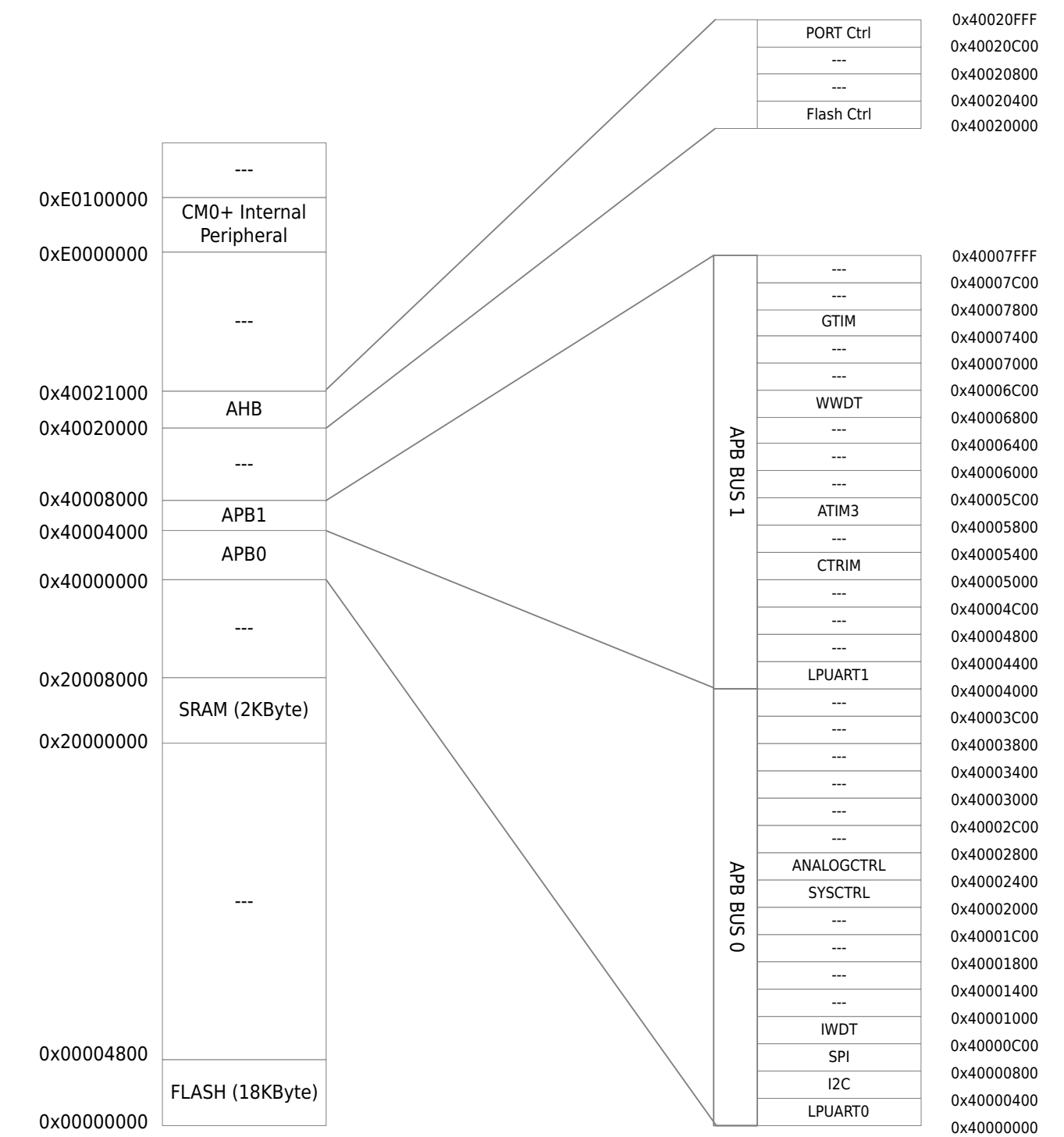
1.2 Functional Block Diagram



Note

Products in different packages support varying resources. For detailed specifications, please refer to [Model Function Comparison Table](#).

1.3 Memory Map



2 Functional Description

2.1 32-bit Cortex-M0+ Core

The ARM Cortex-M0+ processor is based on the Cortex-M0 and integrates a 32-bit RISC processor with a computing performance of 0.95 Dhrystone MIPS/MHz. It also incorporates multiple new designs, including improved debugging and tracing capabilities, reduced instructions per cycle (IPC) count, an enhanced two-stage pipeline for Flash access, and integrates energy-saving technologies. The Cortex-M0+ processor fully supports Keil & IAR debuggers.

The Cortex-M0+ includes a hardware debug circuit supporting the 2-pin SWD debug interface.

ARM Cortex-M0+ support features:

Instruction set	Thumb/Thumb-2
Assembly line	2-stage assembly line
Performance efficiency	2.46 CoreMark/MHz
Performance efficiency	0.95 DMIPS/MHz in Dhrystone
Interrupt	32 fast interrupts (For detailed interrupt specifications of this product, please refer to "NVIC")
Interrupt priority	Configurable 4-level interrupt priority
Enhanced instruction	Multi-cycle 32-bit multiplier
Debugging	Serial-wire debug port, supports four break points and one watch point.

2.2 18KB FLASH

Built-in fully integrated FLASH controller, no need for external high voltage input, high voltage generated by the fully built-in circuit for programming. Supports ISP, IAP, ICP functions. Features 4-level security protection.

2.3 2KB RAM

RAM data is retained in any power mode.

2.4 Clock System

- A high-precision internal clock RCH with a frequency of 44-48MHz. Factory pre-calibrated values for 44.24MHz and 48MHz are preset.
- An internal RCL clock with frequencies of 32.768/38.4kHz.

2.5 Operating Mode

1. Active Mode: CPU running, on-chip peripherals running.
2. Sleep mode: CPU halted, on-chip peripherals running.
3. DeepSleep mode: CPU halted, low-power on-chip peripherals running.

2.6 GPIO

It can provide up to 22 GPIO ports, some of which are multiplexed with analog ports. Each port is controlled by independent control register bits. Supports edge-triggered interrupts and level-triggered

interrupts, and can wake up the MCU to working mode from various ultra-low power consumption modes. Supports bit set, bit clear, and bit set clear operations. Supports CMOS Push-Pull output, Open-Drain output. Built-in pull-up resistor, with Schmitt trigger function. Each IO supports a maximum current drive capability of 18mA.

2.7 NVIC

The Cortex-M0+ processor integrates a Nested Vectored Interrupt Controller (NVIC) supporting up to 15 interrupt request (IRQ) inputs. With 4 interrupt priority levels, it can handle complex logic for real-time control and interrupt processing.

2.8 RESET

This product features 7 reset signal sources. Each reset signal can restart the CPU, reset most registers, and point the program counter (PC) to the starting address.

- Digital area power-on and power-off reset POR
- External Reset PAD, low level is reset signal
- WWDT reset
- IWDT reset
- LVD low voltage reset
- Cortex-M0+ SYSRESETREQ software reset
- Cortex-M0+ LOCKUP hardware reset

2.9 Timer

Name	Width	Prescaler	Count Direction	PWM	Capture	Complementary Output
ATIM3	16/32	1/2/4/8/16/32/64/256	Up count/ Count down/ Up and down count	6	6	3
GTIM	16	1-32768	Up count	4	4	-
BTIM3-5	16	1-32768	Up count	-	-	-
CTRM	16	1-32768	Up count	-	-	-

The general-purpose timer supports 4-channel compare/capture functionality and can be configured as three basic timers.

The low-power timer is an asynchronous 16-bit timer/counter that continues operating via RCL for timing/counting even after system clock shutdown. Wake up the system in low-power mode through interrupts.

Advanced Timer includes timer ATIM3, supporting the following functions:

- PWM independent output, complementary output
- Capture input
- Pulse width measurement
- Quadrature encoder counting function
- Single pulse mode
- External counting function

- Dead-time control
- Braking control
- Edge alignment, symmetric center alignment and asymmetric center alignment PWM output

ATIM3 is a multi-channel general-purpose timer, capable of generating 3 sets of complementary PWM outputs or 6 independent PWM channels, with up to 6 input capture channels. With dead zone control function.

2.10 WDT

The IWDG is a configurable 12-bit timer that provides a reset in case of MCU malfunction, with RCL clock input as the counter clock. The WDT can only be restarted by writing a specific sequence.

WWDT is a 7-bit timer. When external interference or unforeseen logic conditions cause the application program to deviate from the normal running sequence, WWDT can detect such software failures and generate interrupts or resets.

2.11 LPUART

2-channel Low-Power Universal Asynchronous Receiver/Transmitter (LPUART) that can operate in low-power mode.

Basic functions of LPUART:

- Configuration clock PCLK
- Transmission clock SCLK (SCLK can select RCL and PCLK, the clock accuracy is the same as that of RCL or PCLK)
- Support synchronous half-duplex, asynchronous full-duplex and single-wire half-duplex transmission.
- Programmable serial communication function
 - ▶ 2 character lengths: 8 bits, 9 bits
 - ▶ 3 check methods: no check, odd check, even check
 - ▶ 3 stop lengths: 1 bit, 1.5 bits, 2 bits
- Supports transmitting and receiving data in low power mode
- 16-bit baud rate counter
- Support hardware flow control (RTS, CTS)
- Support multi-machine communication and automatic address recognition

2.12 SPI

Basic features of SPI:

- Can be configured as master or slave, support multi-machine mode
- The maximum division factor in master mode is PCLK/2
- The maximum division factor in slave mode is PCLK/4
- Multiple communication modes: full-duplex, single-wire half-duplex, simplex
- 2 transmission orders: MSB first or LSB first
- Various data frame lengths: 4bits-16bits
- 2 NSS methods: hardware control, software control
- Configurable serial clock polarity and phase

2.13 I2C

1-channel I2C, using serial synchronous clock, can realize data transmission between devices at different rates.

Basic features of I2C:

- Support 4 working modes of master sending/receiving and slave sending/receiving
- Support 3 operating rates: Standard (100kbps)/Fast (400kbps)/High-speed (1Mbps)
- Slave supports 7-bit addressing function; Master supports 10-bit addressing function
- Support noise filtering function
- Support 3 slave addresses
- Support broadcast address
- Support interrupt status query function

2.14 CTRIM

The clock calibration timer can adjust and calibrate the RC clock frequency and the clock frequencies of other RC oscillations. It can also be used as a general timer or an automatic wake-up timer.

2.15 Buzzer

The timer function multiplexing output provides a programmable drive frequency for the Buzzer. The buzzer port can provide 18mA sink current, complementary output, no additional transistor is needed.

2.16 ADC

External analog signals need to be converted into digital signals to be further processed by the MCU. 10-bit successive approximation analog-to-digital converter (SAR ADC) module with high precision and high conversion rate is integrated inside.

- 10-bit conversion accuracy
- 1Msps conversion speed
- Up to 15 input channels are supported, including 14 external pin inputs, 1 internal built-in BGR 0.9V voltage channel



Note

By selecting AVCC as the reference source and measuring the BGR 0.9V, the AVCC voltage can be calculated.

- 2 reference sources: AVCC voltage, ExRef pins
- ADC voltage input range: 0-Vref
- Support single conversion and continuous conversion
- Support on-chip peripherals to automatically trigger ADC conversion, effectively reducing chip power consumption and improving real-time conversion

2.17 LVD

Detects chip supply voltage or pin voltage, supporting the following functions:

- 4 monitoring sources: AVCC, PA03, PC03, PD04
- 16-stage threshold voltage, 1.8-3.3V optional
- 8 trigger conditions, combinations of high level, rising edge and falling edge

- 2 trigger results: reset and interrupt
- 8-stage filter configuration to prevent false triggering
- With hysteresis function, strong anti-interference

2.18 Embedded Debugging System

Embedded debugging solution, providing a full-featured real-time debugger, with standard mature Keil/IAR and other debugging and development softwares. Support four hard breakpoints and multiple soft breakpoints.

2.19 Programming Mode

Support programming modes: online programming and offline programming.

Support programming protocols: ISP protocol, SWD protocol.

Support programming interface: ISP protocol and SWD protocol share SWD port.

2.20 Electronic Signature

Each chip has a unique 10-byte device identification number before leaving the factory, including wafer lot information, chip coordinate information, and so on. Built-in 128-byte OTP memory, writable only once via a programmer.

2.21 High Security

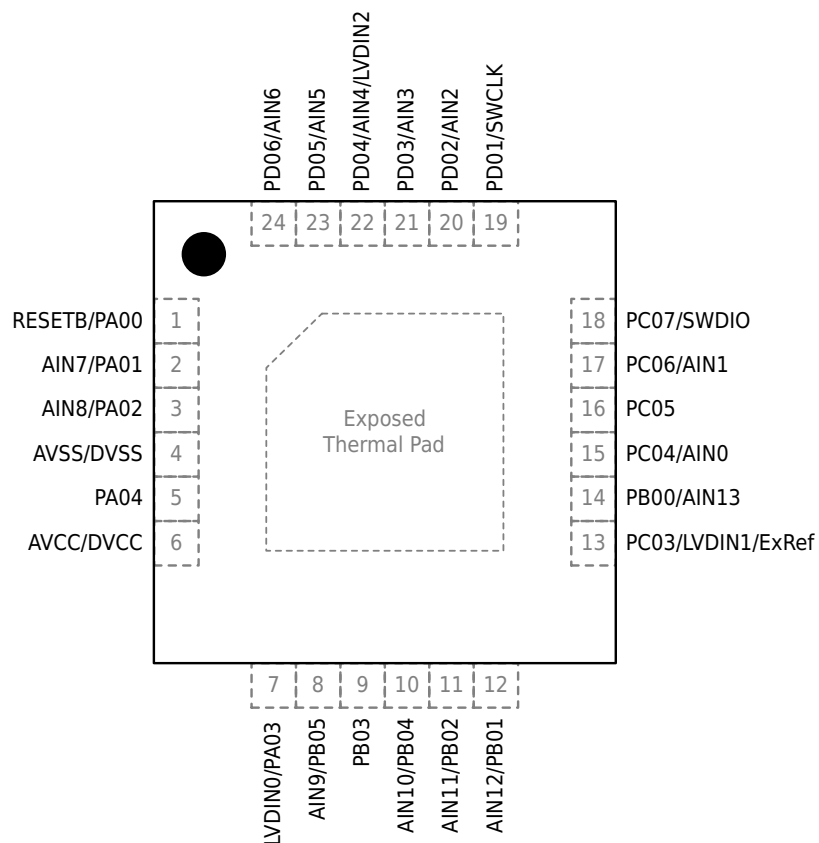
Encrypted embedded debugging solution, providing a full-featured real-time debugger.

3 Pin Definitions

3.1 Pinout

3.1.1 QFN24 Package

HC32F002D4UZ-QFN24TR/HC32F002D4UB-QFN24TR

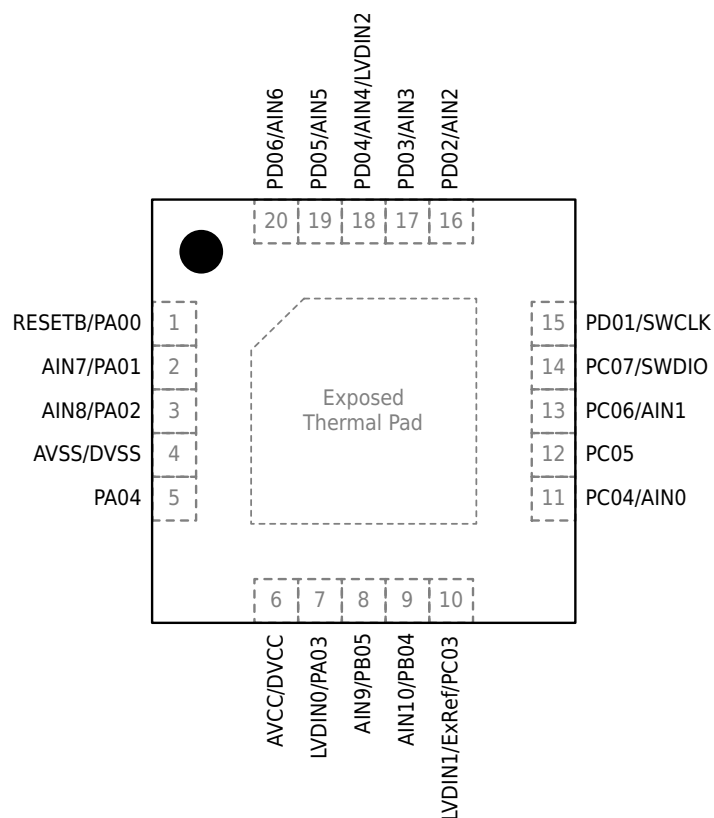


Note

- Exposed Thermal Pad needs to be connected to DVSS.

3.1.2 QFN20 Package

HC32F002C4UZ-ZFN20TR/HC32F002C4UB-ZFN20TR



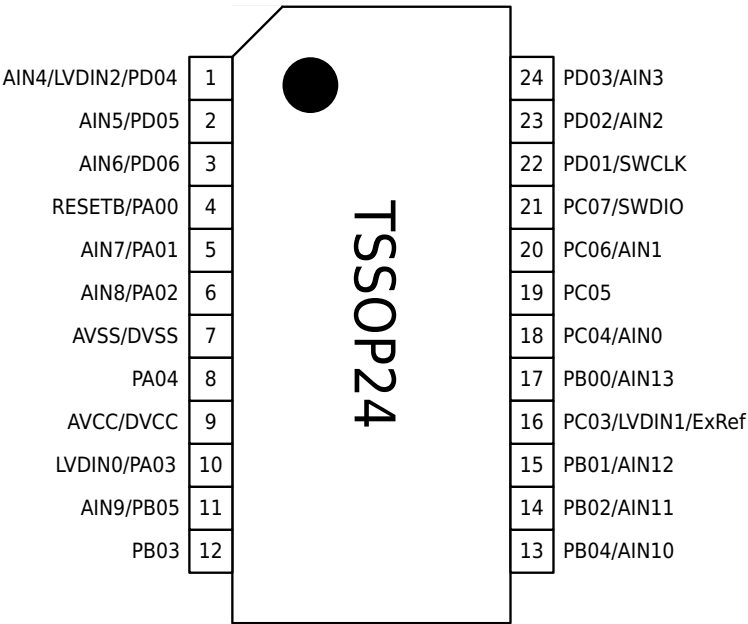
Note

- Exposed Thermal Pad needs to be connected to DVSS.
- In the application, it is necessary to set the unlead IO pin of the package as input and enable the pull-up.
- For details on the IOs not brought out by this package, please refer to [Pin Function Description](#).

3.1.3 TSSOP24 Package

HC32F002D4PZ-TSSOP24/HC32F002D4PZ-TSSOP24TR

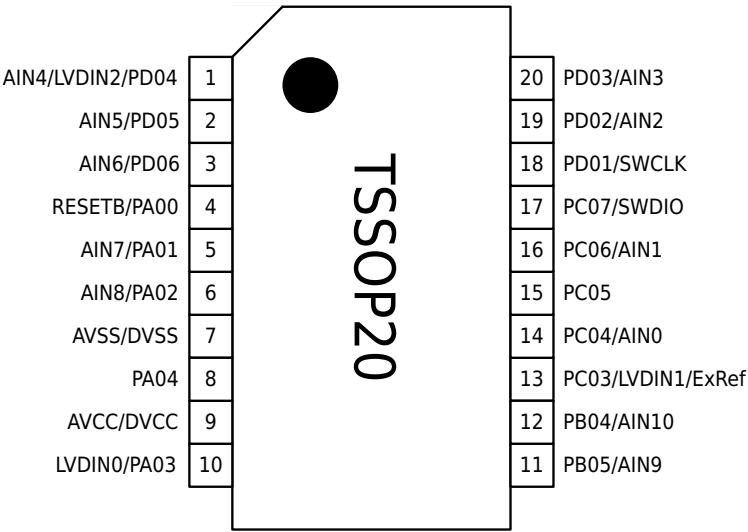
HC32F002D4PB-TSSOP24/HC32F002D4PB-TSSOP24TR



3.1.4 TSSOP20 Package

HC32F002C4PZ-TSSOP20/HC32F002C4PZ-TSSOP20TR

HC32F002C4PB-TSSOP20/HC32F002C4PB-TSSOP20TR



 **Note**

- In the application, it is necessary to set the unleaded IO pin of the package as input and enable the pull-up.
- For details on the IOs not brought out by this package, please refer to [Pin Function Description](#).

3.2 Pin Function Description

QFN20	QFN24	TSSOP20	TSSOP24	Name	Digital	Analog
1	1	4	4	PA00	-	RESETB
2	2	5	5	PA01	LPUART0_RXD I2C_SDA GTIM_TOGP HCLK_OUT	ADC_AIN7
3	3	6	6	PA02	LPUART0_TXD I2C_SCL GTIM_TOGN LVD_OUT	ADC_AIN8
4	4	7	7	AVSS/DVSS	-	-
5	5	8	8	PA04	GTIM_TOGP LVD_OUT SPI_NSS	-
6	6	9	9	AVCC/DVCC	-	-
7	7	10	10	PA03	GTIM_CH2 SPI_NSS CTRM_ETR CTIRM_TOG	LVD_IN0
8	8	11	11	PB05	I2C_SDA ATIM3_BK CTRM_ETR CTIRM_TOG	ADC_AIN9
-	9	-	12	PB03	ATIM3_ETR GTIM_CH0 LPUART1_CTS	-
9	10	12	13	PB04	I2C_SCL ATIM3_CH2B LPUART0_CTS	ADC_AIN10
-	11	-	14	PB02	ATIM3_CH2B GTIM_CH1 LPUART1_RTS	ADC_AIN11
-	12	-	15	PB01	ATIM3_CH1B GTIM_CH2 LPUART0_CTS	ADC_AIN12
10	13	13	16	PC03	ATIM3_CH2A ATIM3_CH0B LPUART0_RTS	LVD_IN1 ADC_ExRef
-	14	-	17	PB00	ATIM3_CH0B GTIM_CH3 LPUART0_RTS	ADC_AIN13
11	15	14	18	PC04	ATIM3_CH0B ATIM3_CH1B TCLK_OUT	ADC_AIN0
12	16	15	19	PC05	SPI_SCK GTIM_CH3 ATIM3_ETR	-
13	17	16	20	PC06	SPI_MOSI ATIM3_CH0A LPUART1_RTS	ADC_AIN1

QFN20	QFN24	TSSOP20	TSSOP24	Name	Digital	Analog
14	18	17	21	PC07 SWDIO	SPI_MISO ATIM3_CH1A LPUART0_RXD	-
15	19	18	22	PD01 SWCLK	GTIM_ETR ATIM3_BK LPUART0_TXD	-
16	20	19	23	PD02	GTIM_CH2 ATIM3_CH2A LPUART1_CTS	ADC_AIN2
17	21	20	24	PD03	GTIM_CH1 ATIM3_CH1A LPUART1_RXD	ADC_AIN3
18	22	1	1	PD04	GTIM_CH0 LPUART1_TXD SPI_SCK	ADC_AIN4 LVD_IN2
19	23	2	2	PD05	LPUART1_TXD ATIM3_CH0A SPI_MISO	ADC_AIN5
20	24	3	3	PD06	LPUART1_RXD GTIM_ETR SPI_MOSI	ADC_AIN6

The digital function of each pin is controlled by the AFRx register. For details, refer to the section "General-Purpose I/O (GPIO)-Functional Description-Port Multiplexing" in the "Reference Manual".

3.3 Module Signal Description

Table 3-2 Module Signal Description

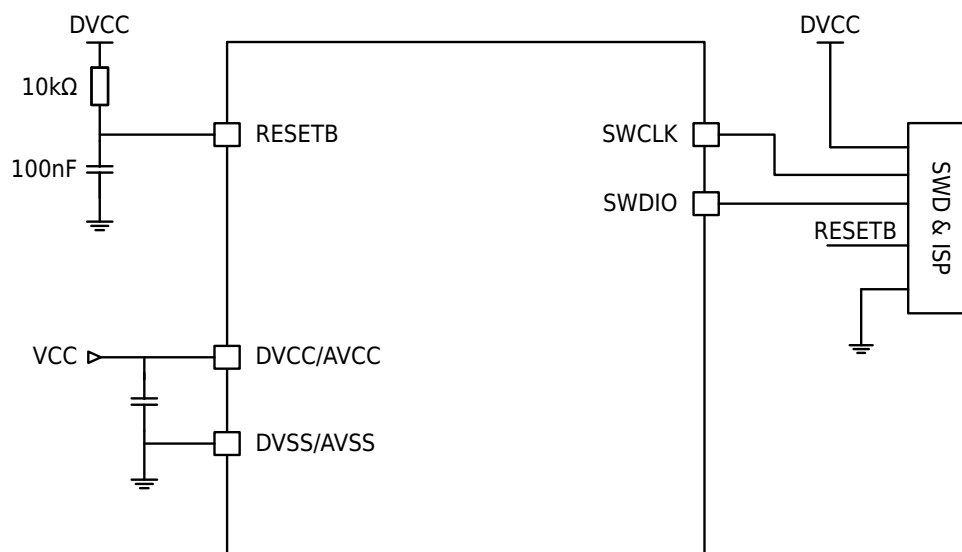
Modules	Pin Name	Description
Power supply	DVCC	Digital power supply
	AVCC	Analog power
	DVSS	Digital ground
	AVSS	Analog ground
ADC	ADC_AINx (x=0-13)	ADC input channel
	ADC_ExRef	ADC external reference voltage
LVD	LVD_INx (x=0-2)	Voltage detection input
	LVD_OUT	Voltage detection output
LPUART	LPUARTx_TXD (x=0-1)	LPUART data transmitter
	LPUARTx_RXD (x=0-1)	LPUART data receiver
	LPUARTx_CTS (x=0-1)	LPUART transmit hardware flow control
	LPUARTx_RTS (x=0-1)	LPUART receive hardware flow control
CTRIM	CTRIM_ETR	CTRIM external synchronization signal
	CTRIM_TOG	CTRIM inverted output signal

Modules	Pin Name	Description
SPI	SPI_MISO	SPI master input and slave output data signal
	SPI_MOSI	SPI master output and slave input data signal
	SPI_SCK	SPI clock signal
	SPI_NSS	SPI chip selection
I2C	I2C_SDA	I2C data signal
	I2C_SCL	I2C clock signal
BTIM	BTIMx_TOGP (x=3-5)	BTIM inverted output signal
	BTIMx_TOGN (x=3-5)	
GTIM	GTIM_CHy (y=0-3)	Capture input compare output of GTIM
	GTIM_ETR	External count input signal of GTIM
	GTIM_TOGP/TOGN	Inverted output signal of GTIM
ATIM3	ATIM3_CHyA (y=0-2)	Capture input and compare output A of ATIM3
	ATIM3_CHyB (y=0-2)	Capture input and compare output B of ATIM3
	ATIM3_ETR	External counting input signal of ATIM3
	ATIM3_BK	External brake input signal of ATIM3

**Note**

The IO port is reset to the input high impedance stat, while the port states are maintained in Sleep mode and DeepSleep mode.

4 Typical Application Circuit Diagram



Notice

- Power supply requires external decoupling capacitors. For better anti-interference capability, it is preferable to route the power supply/ground lines through the decoupling capacitors first before connecting them to the chip.

5 Electrical Specifications

5.1 Parameter Conditions

Unless otherwise specified, all voltages are based on VSS.

5.1.1 Minimum and Maximum Values

All Minimum Values and Maximum Values are measured under the worst conditions.

Data resulted from comprehensive evaluation, and/or guaranteed by design are indicated in the table footnotes, and they will not be tested on the production line.

5.1.2 Typical Values

Unless otherwise specified, typical data are given based on $T_A=25^{\circ}\text{C}$ and $V_{CC}=3.3\text{V}$. These data are only used for design guidance and have not been tested.

5.2 Absolute Maximum Ratings

If the load applied to the device exceeds the value given in the list of "Absolute Maximum Ratings", it may cause permanent damage to the device. The maximum load given here is for reference, which does not mean that the functional operation of the device is correct under this condition. Operation of the device under the condition of maximum value for a long time will affect the reliability of the device.

Table 5-1 Voltage and Current Characteristics

Symbol	Parameters	Min	Max	Unit
VCC-VSS	External main supply voltage (including AVCC and DVCC) ⁽¹⁾	-0.3	5.5	V
V _{IN}	Input voltage on other pins ⁽²⁾	VSS-0.3	VCC+0.3	V
ΔVCCx	Voltage difference between different power supply pins	-	50	mV
VSSx-VSS	Voltage difference between different grounding pins	-	50	mV
V _{ESD} (HBM)	Electrostatic discharge voltage (Human model)	Refer to absolute maximum electrical parameters		V
I _{VCC}	Total current through DVCC/AVCC power line (supply current) ⁽¹⁾	-	300	mA
I _{VSS}	Total current through DVSS/AVSS ground wire (outflow current) ⁽¹⁾	-	300	mA
I _{IO}	Output sink current on any I/O and control pins	-	25	mA
	Output current on any I/O and control pins	-	-25	mA
I _{INJ(PIN)} ⁽²⁾⁽³⁾	Injection current of RESETB pin	-	±5	mA
	Injection current of other pins ⁽⁴⁾	-	±5	mA
ΣI _{INJ(PIN)} ⁽²⁾	Total injection current on all I/O and control pin ⁽⁴⁾	-	±25	mA

**Note**

1. All power supply (DVCC, AVCC) and grounding (DVSS, AVSS) pins should always be connected to the power supply system within the external allowable range.
2. $I_{INJ(PIN)}$ should not exceed its limit, that is, ensure that V_{IN} does not exceed its maximum value. If V_{IN} cannot be guaranteed not to exceed its maximum value, it is also necessary to ensure that $I_{INJ(PIN)}$ does not exceed its maximum value externally. When $V_{IN} > V_{CC}$, there is a forward injection current; When $V_{IN} < V_{SS}$, there is a reverse injection current.
3. The reverse injection current will interfere with the simulation performance of the device.
4. When several I/O ports have injection currents at the same time, the maximum value of $\sum I_{INJ(PIN)}$ is the sum of the instantaneous absolute values of the forward injection current and the reverse injection current. This result is based on the features of the maximum value of $\sum I_{INJ(PIN)}$ at four I/O ports of the device.

Table 5-2 Temperature Characteristics

Symbol	Parameters	Value	Unit
T_{STG}	Storage temperature range	-65~+150	°C
T_{Jmax}	Maximum Junction Temperature	125	°C

5.3 Operating Conditions

5.3.1 General Operating Conditions

Table 5-3 General Operating Conditions (Suitable for HC32F002C4PZ/HC32F002C4UZ/HC32F002D4PZ/HC32F002D4UZ)

Symbol	Parameters	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK0}	Internal APB0 clock frequency	-	0	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	48	MHz
DVCC	Digital operating voltage	-	1.7	5.5	V
AVCC ⁽¹⁾	Analog operating voltage	Must be the same as DVCC ⁽²⁾	1.7	5.5	V
T_A	Ambient temperature	Maximum power consumption	-20	105	°C
		Low power consumption ⁽³⁾	-20	125	°C
T_J	Junction temperature range	-	-20	125	°C

Table 5-4 General Operating Conditions (Suitable for HC32F002C4PB/HC32F002C4UB/HC32F002D4PB/HC32F002D4UB)

Symbol	Parameters	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK0}	Internal APB0 clock frequency	-	0	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	48	MHz
DVCC	Digital operating voltage	-	2.7	5.5	V

Symbol	Parameters	Conditions	Min	Max	Unit
AVCC ⁽¹⁾	Analog operating voltage	Must be the same as DVCC ⁽²⁾	2.7	5.5	V
T _A	Ambient temperature	Maximum power consumption	-40	105	°C
		Low power consumption ⁽³⁾	-40	125	°C
T _J	Junction temperature range	-	-40	125	°C

**Note**

1. When using an ADC, see ADC Electrical Specifications.
2. It is recommended to use the same power supply for DVCC and AVCC, allowing a maximum of 300mV difference between DVCC and AVCC during power-up and normal operation.
3. In a state of lower power consumption, as long as T_J does not exceed T_{Jmax}, T_A can be extended to this range.

5.3.2 Working Conditions at Power-On and Power-Down

Table 5-5 Working Conditions at Power-On and Power-Down

Symbol	Parameters	Conditions	Min	Max	Unit
t _{VCC} ⁽¹⁾	VCC rise rate	-	0.2	20000	μs/V
t _{VCC} ⁽¹⁾	VCC fall rate	-	0.2	20000	μs/V

**Note**

1. Resulted from comprehensive evaluation, not tested in production.

5.3.3 Embedded Reset and LVD Module Characteristics

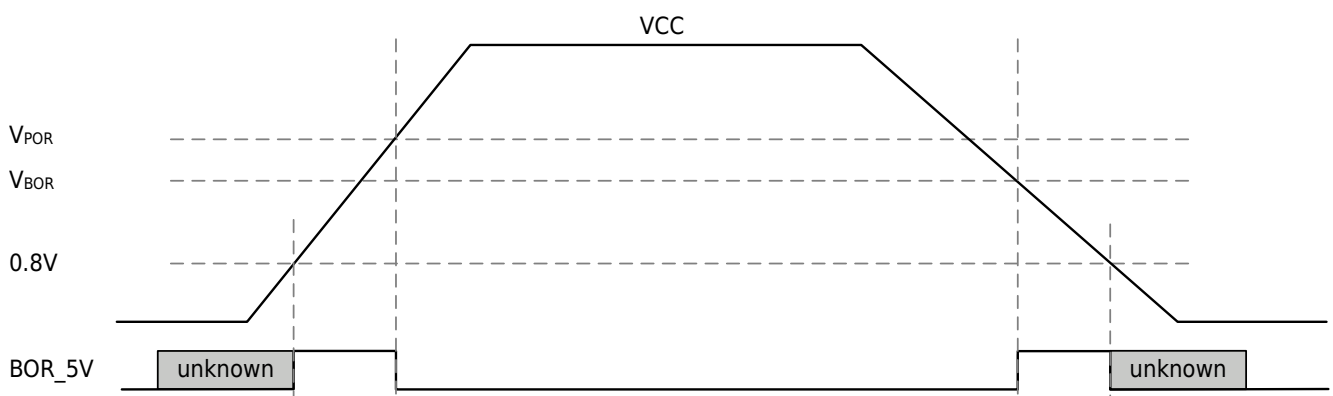


Figure 5-1 POR/Brown Out Schematic Diagram

Table 5-6 POR/Brown Out

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V _{POR}	POR release voltage (power on process)	-	-	1.65	1.7	V

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V _{PDR}	BOR detection voltage (power down process)	-	-	1.55	-	V

**Note**

1. Guaranteed by design, not tested in production.

Table 5-7 LVD Module Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V _{ex}	External input voltage range	-	0	-	VCC	V
V _{level}	Detection threshold	LVD_CR.VTDS=0b0000 LVD_CR.VTDS=0b0001 LVD_CR.VTDS=0b0010 LVD_CR.VTDS=0b0011 LVD_CR.VTDS=0b0100 LVD_CR.VTDS=0b0101 LVD_CR.VTDS=0b0110 LVD_CR.VTDS=0b0111 LVD_CR.VTDS=0b1000 LVD_CR.VTDS=0b1001 LVD_CR.VTDS=0b1010 LVD_CR.VTDS=0b1011 LVD_CR.VTDS=0b1100 LVD_CR.VTDS=0b1101 LVD_CR.VTDS=0b1110 LVD_CR.VTDS=0b1111	-	1.8±3.5% 1.9±3.5% 2.0±3.5% 2.1±3.5% 2.2±3.5% 2.3±3.5% 2.4±3.5% 2.5±3.5% 2.6±3.5% 2.7±3.5% 2.8±3.5% 2.9±3.5% 3.0±3.5% 3.1±3.5% 3.2±3.5% 3.3±3.5%	-	V
I _{comp}	Power consumption	-	-	0.36	-	μA
T _{response}	Response time	-	-	100	-	μs
T _{setup}	Settling time	-	-	300	-	μs
V _{hyste}	Hysteresis voltage	-	-	40	-	mV
T _{filter}	Filter time	LVD_CR.FLTTIME=0b000 LVD_CR.FLTTIME=0b001 LVD_CR.FLTTIME=0b010 LVD_CR.FLTTIME=0b011 LVD_CR.FLTTIME=0b100 LVD_CR.FLTTIME=0b101 LVD_CR.FLTTIME=0b110 LVD_CR.FLTTIME=0b111	25 75 175 375 1575 6375 25575 102375	50 100 200 400 1600 6400 25600 102400	-	μs

**Note**

1. Resulted from comprehensive evaluation, not tested in production.

5.3.4 Built-In Reference Voltage BGR

Table 5-8 Built-In Reference Voltage Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{BGR09}	Internal 0.9V reference voltage	Room temperature 25°C, 3.3V	-	0.9	-	V
V_{BGR09}	Internal 0.9V reference voltage	-	0.875	-	0.925	V
T_{Coeff}	Internal 0.9V temperature coefficient	-	-	50	-	ppm/°C



Note

1. Resulted from comprehensive evaluation, not tested in production.

5.3.5 Supply Current Characteristics

Current consumption is a comprehensive index of multiple parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin flip rate, and the location of the program in memory and the executed code, etc.

The MCU is in the following conditions:

- All I/O pins are in input mode and connected to VCC or VSS(no load).
- All peripherals are turned off, unless otherwise specified.
- The access time of the flash memory is adjusted to the frequency f_{HCLK} (0 wait cycle for 0-24MHz, 1 wait cycle for 24-48MHz)
- When peripherals is used: $f_{PCLK0}=f_{HCLK}$, $f_{PCLK1}=f_{HCLK}$.

Table 5-9 Operating Current Characteristics (HC32F002C4PZ/HC32F002C4UZ/HC32F002D4PZ/HC32F002D4UZ)

Symbol	Parameters	Conditions			Typ ⁽¹⁾⁽³⁾	Max ⁽²⁾⁽³⁾	Unit
I_{DD} (Run in RAM)	All peripherals clock ON, Run while(1) in RAM	$V_{CC}=3.3V$ $T_A=25^{\circ}C$	RCH clock source	4M	505	-	μA
				8M	730	-	
				12M	955	-	
				22.12M	1515	-	
				24M	1630	-	
				44.24M	2755	-	
				48M	2980	-	
	All peripherals clock OFF, Run while(1) in RAM	$V_{CC}=3.3V$ $T_A=2x^{\circ}C$	RCH clock source	4M	410	-	μA
				8M	545	-	
				12M	680	-	
				22.12M	1005	-	
				24M	1080	-	
				44.24M	1735	-	
				48M	1870	-	
I_{DD} (Run mode)	All peripherals clock ON, Run while(1) in Flash	$V_{CC}=1.7-5.5V$ $T_A=-20-105^{\circ}C$	RCH clock source	4M	725	870	μA
				8M	1160	1350	
				12M	1575	1820	
				22.12M	2545	2960	

Symbol	Parameters	Conditions			Typ ⁽¹⁾⁽³⁾	Max ⁽²⁾⁽³⁾	Unit
I _{DD} (Run mode)	All peripherals clock ON, Run while(1) in Flash	V _{CC} =1.7-5.5 V T _A = -20-105 °C		24M	2735	3170	μA
				44.24M FlashWait=1	3515	4070	
				48M Flash-Wait=1	3790	4380	
	All peripherals clock OFF, Run while(1) in Flash	V _{CC} =1.7-5.5 V T _A = -20-105 °C	RCH clock source	4M	635	770	μA
				8M	970	1140	
				12M	1295	1510	
				22.12M	2035	2390	
				24M	2185	2550	
				44.24M FlashWait=1	2500	2930	
				48M Flash-Wait=1	2685	2950	
I _{DD} (Sleep mode)	All peripherals clock ON, Run while(1) in Flash	V _{CC} =1.7-5.5 V T _A = -20-105 °C	RCH clock source	4M	400	470	μA
				8M	520	610	
				12M	635	740	
				22.12M	925	1070	
				24M	990	1140	
				44.24M FlashWait=1	1570	1800	
				48M Flash-Wait=1	1695	1930	
	All peripherals clock OFF, Run while(1) in Flash	V _{CC} =1.7-5.5 V T _A = -20-105 °C	RCH clock source	4M	305	370	μA
				8M	335	400	
				12M	360	430	
				22.12M	415	490	
				24M	435	520	
				44.24M FlashWait=1	550	640	
				48M Flash-Wait=1	585	680	
I _{DD} (LP Run)	All peripherals clock ON, Run while(1) in Flash	V _{CC} =1.7-5.5 V	RCL32K clock source	T _A = -20-25°C	7.4	14.4	μA
				T _A =50°C	7.9	14.9	
				T _A =85°C	9.3	16.0	
				T _A =105°C	11.4	22.0	
	All peripherals clock OFF, Run while(1) in Flash	V _{CC} =1.7-5.5 V	RCL32K clock source	T _A = -20-25°C	6.7	12.8	μA
				T _A =50°C	7.2	13.6	
				T _A =85°C	8.5	14.9	
				T _A =105°C	10.6	21.0	
I _{DD} (LP Sleep)	All peripherals clock ON,	V _{CC} =1.7-5.5 V	RCL32K clock source	T _A = -20-25°C	4.4	10.3	μA
				T _A =50°C	4.8	10.7	
				T _A =85°C	6.1	11.2	
				T _A =105°C	8.1	18.8	

Symbol	Parameters	Conditions			Typ ⁽¹⁾⁽³⁾	Max ⁽²⁾⁽³⁾	Unit
I _{DD} (LP Sleep)	All peripherals clock OFF,	V _{CC} =1.7-5.5 V	RCL32K clock source	T _A =-20-25°C	3.7	7.3	μA
				T _A =50°C	4.0	7.8	
				T _A =85°C	5.3	10.5	
				T _A =105°C	7.4	18.3	
I _{DD} (Deep-Sleep)	WDT+LVD+RCL32K+Deep-Sleep	V _{CC} =1.7-5.5 V	-	T _A =-20-25°C	3.2	6.9	μA
				T _A =50°C	3.7	7.5	
				T _A =85°C	4.9	9.2	
				T _A =105°C	6.7	14.6	
	LVD+RCL32K+DeepSleep	V _{CC} =1.7-5.5 V	-	T _A =-20-25°C	2.6	6.2	μA
				T _A =50°C	3.0	6.7	
				T _A =85°C	4.0	8.7	
				T _A =105°C	5.5	13	
	WDT+RCL32K+DeepSleep	V _{CC} =1.7-5.5 V	-	T _A =-20-25°C	3.0	6.5	μA
				T _A =50°C	3.4	7.0	
				T _A =85°C	4.6	8.8	
				T _A =105°C	6.3	14.0	
	RCL38K+ DeepSleep	V _{CC} =1.7-5.5 V	-	T _A =-20-25°C	3.0	6.5	μA
				T _A =50°C	3.4	7.0	
				T _A =85°C	4.6	8.8	
				T _A =105°C	6.3	14.0	
	RCL32K+ DeepSleep	V _{CC} =1.7-5.5 V	-	T _A =-20-25°C	3.0	6.5	μA
				T _A =50°C	3.4	7.0	
				T _A =85°C	4.6	8.8	
				T _A =105°C	6.3	14.0	
	DeepSleep	V _{CC} =1.7-5.5 V	-	T _A =-20-25°C	2.4	5.8	μA
				T _A =50°C	2.7	6.3	
				T _A =85°C	3.8	8.2	
				T _A =105°C	5.2	12.5	

**Note**

1. If there are no other specified conditions, the value of the Typ is 25°C & V_{CC}=3.3V measured.
2. If there are no other specified conditions, the value of Max is the maximum value in the range of V_{CC}=1.7-5.5V & Temperature=-20-105°C.
3. Resulted from comprehensive evaluation, not tested in production.

Table 5-10 Operating Current Characteristics(HC32F002C4PB/HC32F002C4UB/HC32F002D4PB/HC32F002D4UB)

Symbol	Parameters	Conditions			Typ ⁽¹⁾⁽³⁾	Max ⁽²⁾⁽³⁾	Unit
I _{DD} (Run in RAM)	All peripherals clock ON, Run while(1) in RAM	V _{CC} =3.3V T _A =25°C	RCH clock source	4M	505	-	μA
				8M	730	-	
				12M	955	-	
				22.12M	1515	-	

Symbol	Parameters	Conditions			Typ ⁽¹⁾⁽³⁾	Max ⁽²⁾⁽³⁾	Unit
I _{DD} (Run in RAM)	All peripherals clock ON, Run while(1) in RAM	V _{CC} =3.3V T _A =25°C		24M	1630	-	μA
				44.24M	2755	-	
				48M	2980	-	
	All peripherals clock OFF, Run while(1) in RAM	V _{CC} =3.3V T _A =2x°C	RCH clock source	4M	410	-	μA
				8M	545	-	
				12M	680	-	
				22.12M	1005	-	
				24M	1080	-	
				44.24M	1735	-	
				48M	1870	-	
I _{DD} (Run mode)	All peripherals clock ON, Run while(1) in Flash	V _{CC} =2.7-5.5 V T _A =-40-105 °C	RCH clock source	4M	725	870	μA
				8M	1160	1350	
				12M	1575	1820	
				22.12M	2545	2960	
				24M	2735	3170	
				44.24M FlashWait=1	3515	4070	
				48M Flash-Wait=1	3790	4380	
	All peripherals clock OFF, Run while(1) in Flash	V _{CC} =2.7-5.5 V T _A =-40-105 °C	RCH clock source	4M	635	770	μA
				8M	970	1140	
				12M	1295	1510	
				22.12M	2035	2390	
				24M	2185	2550	
				44.24M FlashWait=1	2500	2930	
				48M Flash-Wait=1	2685	2950	
I _{DD} (Sleep mode)	All peripherals clock ON, Run while(1) in Flash	V _{CC} =2.7-5.5 V T _A =-40-105 °C	RCH clock source	4M	400	470	μA
				8M	520	610	
				12M	635	740	
				22.12M	925	1070	
				24M	990	1140	
				44.24M FlashWait=1	1570	1800	
				48M Flash-Wait=1	1695	1930	
	All peripherals clock OFF, Run while(1) in Flash	V _{CC} =2.7-5.5 V T _A =-40-105 °C	RCH clock source	4M	305	370	μA
				8M	335	400	
				12M	360	430	
				22.12M	415	490	
				24M	435	520	
				44.24M FlashWait=1	550	640	
				48M Flash-Wait=1	585	680	

Symbol	Parameters	Conditions			Typ ⁽¹⁾⁽³⁾	Max ⁽²⁾⁽³⁾	Unit
I _{DD} (LP Run)	All peripherals clock ON, Run while(1) in Flash	V _{CC} =2.7-5.5 V	RCL32K clock source	T _A =-40-25°C	7.4	14.4	μA
				T _A =50°C	7.9	14.9	
				T _A =85°C	9.3	16.0	
				T _A =105°C	11.4	22.0	
	All peripherals clock OFF, Run while(1) in Flash	V _{CC} =2.7-5.5 V	RCL32K clock source	T _A =-40-25°C	6.7	12.8	μA
				T _A =50°C	7.2	13.6	
				T _A =85°C	8.5	14.9	
				T _A =105°C	10.6	21.0	
I _{DD} (LP Sleep)	All peripherals clock ON,	V _{CC} =2.7-5.5 V	RCL32K clock source	T _A =-40-25°C	4.4	10.3	μA
				T _A =50°C	4.8	10.7	
				T _A =85°C	6.1	11.2	
				T _A =105°C	8.1	18.8	
	All peripherals clock OFF,	V _{CC} =2.7-5.5 V	RCL32K clock source	T _A =-40-25°C	3.7	7.3	μA
				T _A =50°C	4.0	7.8	
				T _A =85°C	5.3	10.5	
				T _A =105°C	7.4	18.3	
I _{DD} (Deep-Sleep)	WDT+LVD+RCL32K+Deep-Sleep	V _{CC} =2.7-5.5 V	-	T _A =-40-25°C	3.2	6.9	μA
				T _A =50°C	3.7	7.5	
				T _A =85°C	4.9	9.2	
				T _A =105°C	6.7	14.6	
	LVD+RCL32K+DeepSleep	V _{CC} =2.7-5.5 V	-	T _A =-40-25°C	2.6	6.2	μA
				T _A =50°C	3.0	6.7	
				T _A =85°C	4.0	8.7	
				T _A =105°C	5.5	13	
	WDT+RCL32K+DeepSleep	V _{CC} =2.7-5.5 V	-	T _A =-40-25°C	3.0	6.5	μA
				T _A =50°C	3.4	7.0	
				T _A =85°C	4.6	8.8	
				T _A =105°C	6.3	14.0	
	RCL38K+ DeepSleep	V _{CC} =2.7-5.5 V	-	T _A =-40-25°C	3.0	6.5	μA
				T _A =50°C	3.4	7.0	
				T _A =85°C	4.6	8.8	
				T _A =105°C	6.3	14.0	
	RCL32K+ DeepSleep	V _{CC} =2.7-5.5 V	-	T _A =-40-25°C	3.0	6.5	μA
				T _A =50°C	3.4	7.0	
				T _A =85°C	4.6	8.8	
				T _A =105°C	6.3	14.0	
	DeepSleep	V _{CC} =2.7-5.5 V	-	T _A =-40-25°C	2.4	5.8	μA
				T _A =50°C	2.7	6.3	
				T _A =85°C	3.8	8.2	
				T _A =105°C	5.2	12.5	

**Note**

1. If there are no other specified conditions, the value of the Typ is 25°C & $V_{CC}=3.3V$ measured.
2. If there are no other specified conditions, the value of Max is the maximum value in the range of $V_{CC}=2.7-5.5V$ & Temperature=-40-105°C.
3. Resulted from comprehensive evaluation, not tested in production.

5.3.6 Time to Wake-Up from Low-Power Mode

The wake-up time is measured during the wake-up phase of the RCH oscillator. The clock source used when waking up depends on the current operating mode:

- Sleep mode: clock source is RCH oscillator
- DeepSleep mode: clock source is RCH oscillator

Table 5-11 Low-Power Mode Wake-Up Time

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
T_{wu}	Sleep mode wake-up time	-	-	2.0	-	μs
	DeepSleep mode wake-up time	$F_{RCH}=4-48MHz$	-	5.0	-	μs

**Note**

1. The wake-up time is measured from the start of the wake-up event to the user program reading the first instruction.

5.3.7 Internal Clock Source Characteristics

5.3.7.1 RCH

Table 5-12 Internal High-Speed Clock RCH Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Dev	RCH oscillator accuracy	User trimming step for given VCC and T_A conditions	-	0.25	-	%
		$T_A=-40-105^{\circ}C$	-3.5	-	+3.5	%
		$T_A=-20-105^{\circ}C$	-2	-	+3.5	%
		$T_A=-20-50^{\circ}C$	-2	-	+2	%
F_{CLK}	Oscillator frequency	-	40.0	-	48.0	MHz
I_{CLK}	Electro-rheograph	$F_{MCLK}=48MHz$	-	170	-	μA
$DC_{CLK}^{(1)}$	Duty cycle	-	45	50	55	%

**Note**

1. Resulted from comprehensive evaluation, not tested in production.

5.3.7.2 RCL

Table 5-13 Internal Low-Speed Clock RCL Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Dev	RCL oscillator accuracy	User trimming step for given VCC and T _A conditions	-	0.5	-	%
		T _A =-40-105°C	-5	-	+5	%
		T _A =-20-105°C	-3	-	+5	%
		T _A =-20-50°C	-3	-	+3	%
F _{CLK}	Oscillator frequency	-	-	38.4	-	kHz
		-	-	32.768	-	kHz
T _{CLK}	Start time	-	-	150	-	μs
DC _{CLK} ⁽¹⁾	Duty Cycle	-	25	50	75	%
I _{CLK}	Power consumption	-	-	1.5	-	μA

**Note**

1. Resulted from comprehensive evaluation, not tested in production.

5.3.8 Memory Characteristics

Table 5-14 Memory Characteristics

Symbol	Parameters	Conditions		Min	Typ	Max	Unit
EC _{FLASH}	Program, Sector Erase times	T _A =-40 °C-105°C	Data Storage Period (RET _{FLASH}): 10 years, T _A =85°C	-	100000	-	times
			Data Storage Period (RET _{FLASH}): 20 years, T _A =85°C	20000	-	-	times
T _{b_prog} ⁽²⁾	Programming time (bytes)	-		22	-	30	μs
T _{w_prog} ⁽²⁾	Programming time (words)	-		40	-	52	μs
T _{p_erase} ⁽²⁾	Page erase time	-		4	-	5	ms
T _{m_erase} ⁽²⁾	Full chip erase time	-		30	-	40	ms

**Note**

1. Resulted from comprehensive evaluation, not tested in production.

2. Guaranteed by design, not tested in production.

5.3.9 EFT Characteristics

A chip reset can restore the system to normal operation.

Table 5-15 EFT Characteristics

Symbol	Level/Type
EFT to IO (IEC61000-4-4)	Class: 4A
EFT to Power (IEC61000-4-4)	Class: 4A



Note

1. Resulted from comprehensive evaluation, not tested in production.

Software Recommendations

The software process must include control to deal with program runaway, such as:

- Corrupted program counter
- Unexpected reset
- Critical data is destroyed (control registers, etc.)

During the EFT test, interference that exceeds the application requirements can be directly applied to the chip power supply or IO. When an unexpected action is detected, the software part is strengthened to prevent unrecoverable errors.

5.3.10 ESD Characteristics

Using specific measurement methods, the chip is subjected to strength testing to determine its electrical sensitivity performance.

Table 5-16 ESD Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
VESD _{HBM} ⁽¹⁾	ESD @ Human Body Mode	-	-	4	-	kV
VESD _{CDM} ⁽¹⁾	ESD @ Charge Device Mode	-	-	1	-	kV
VESD _{MM} ⁽¹⁾	ESD @ Machine Mode	-	-	200	-	V
I _{latchup} ⁽¹⁾	Latch up current	-	-	200	-	mA



Note

1. Resulted from comprehensive evaluation, not tested in production.

5.3.11 I/O Port Characteristics

5.3.11.1 Output Characteristics-Port

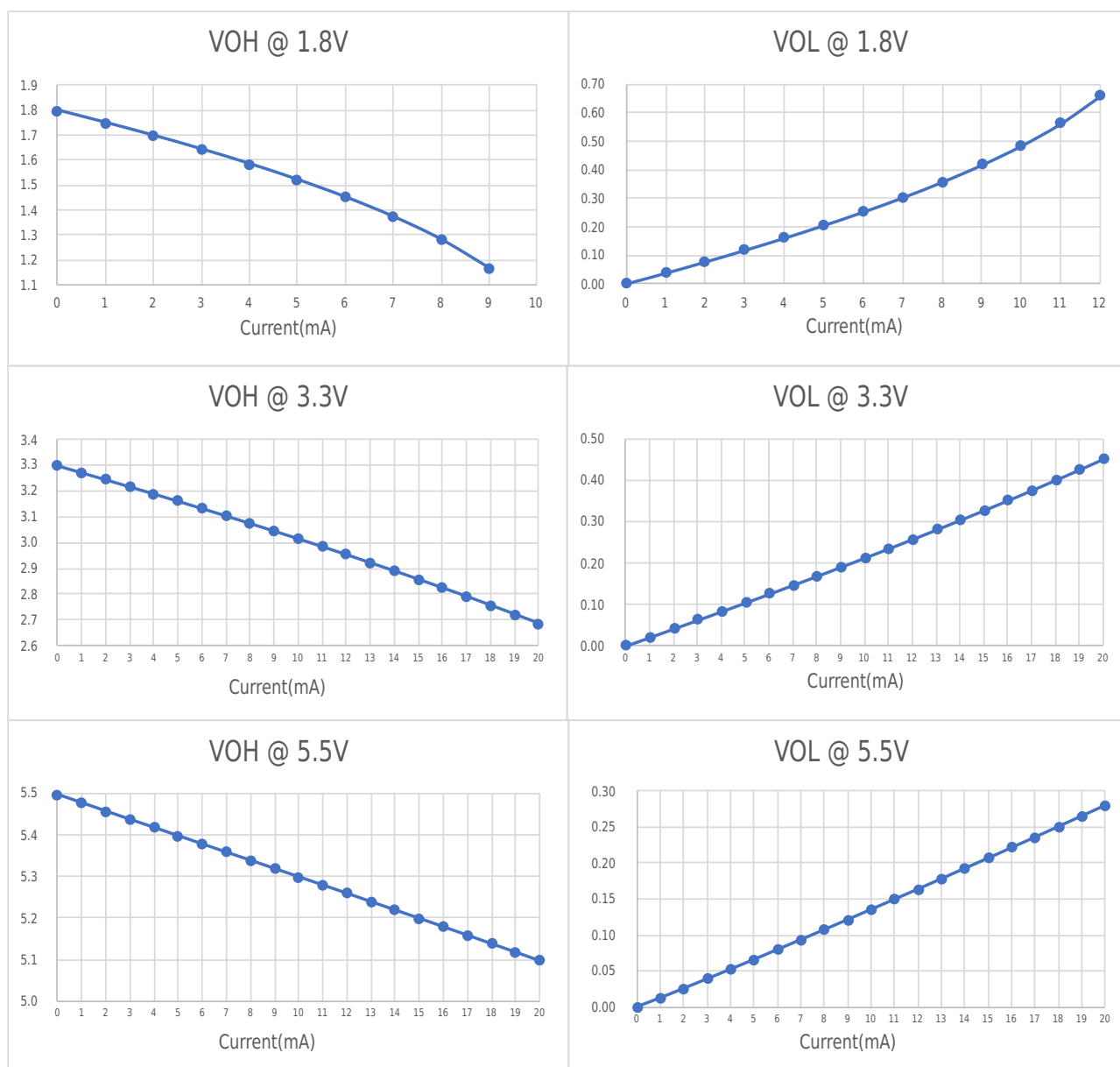
Table 5-17 Port Output Characteristics

Symbol	Parameters	Conditions	Min	Max	Unit
V _{OH}	High level output voltage Source Current	Sourcing 4mA, VCC=3.3V ⁽¹⁾	VCC-0.25	-	V
		Sourcing 8mA, VCC=3.3V ⁽²⁾	VCC-0.60	-	V

Symbol	Parameters	Conditions	Min	Max	Unit
V_{OL}	Low level output voltage Sink Current	Sinking 5mA, $V_{CC}=3.3V^{(1)}$	-	$V_{SS}+0.25$	V
		Sinking 14mA, $V_{CC}=3.3V^{(2)}$	-	$V_{SS}+0.60$	V
V_{OHD}	High level output voltage Double source Current	Sourcing 8mA, $V_{CC}=3.3V^{(1)}$	$V_{CC}-0.25$	-	V
		Sourcing 18mA, $V_{CC}=3.3V^{(2)}$	$V_{CC}-0.60$	-	V
V_{OLD}	Low level output voltage Double Sink Current	Sinking 8mA, $V_{CC}=3.3V^{(1)}$	-	$V_{SS}+0.25$	V
		Sinking 18mA, $V_{CC}=3.3V^{(2)}$	-	$V_{SS}+0.60$	V

**Note**

1. The maximum total current, $I_{OH}(\max)$ and $I_{OL}(\max)$, for all outputs combined, should not exceed 40mA to satisfy the maximum specified voltage drop.
2. The maximum total current, $I_{OH}(\max)$ and $I_{OL}(\max)$, for all outputs combined, should not exceed 100mA to satisfy the maximum specified voltage drop.
3. For QFN20/TSSOP20 packages, pins PC3/PC4/PB4/PB5 are implemented with dual-pad sharing structures, delivering significantly higher drive capacity compared to standard pins.

Figure 5-2 Output port V_{OH}/V_{VOL} measured curve

5.3.11.2 Input Characteristics-PA/PB/PC/PD Port

Table 5-18 PA/PB/PC/PD Port Input Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V _{IH}	Positive-going input threshold voltage	VCC=1.8V	0.7VCC	-	-	V
		VCC=3.3V	0.7VCC	-	-	V
		VCC=5.5V	0.7VCC	-	-	V
V _{IL}	Negative-going input threshold voltage	VCC=1.8V	-	-	0.3VCC	V
		VCC=3.3V	-	-	0.3VCC	V
		VCC=5.5V	-	-	0.3VCC	V

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{\text{hys}}^{(1)}$	Input voltage hysteresis ($V_{\text{IH}}-V_{\text{IL}}$)	VCC=1.8V	-	0.3	-	V
		VCC=3.3V	-	0.4	-	V
		VCC=5.5V	-	0.6	-	V
R_{pullhigh}	Pullup resistor	Pullup enabled VCC=3.3V	-	80	-	k Ω
C_{input}	Input capacitance	-	-	5	-	pF

**Note**

1. Resulted from comprehensive evaluation, not tested in production.

5.3.11.3 Sampling Requirements for External Clock Input at Timer Port-Timer Clock

Table 5-19 Timer Gate/Timer Clock External Input Sampling Requirements

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$t_{(\text{int})}$	External interrupt timing	External trigger signal for the interrupt flag ⁽¹⁾	-	30	-	ns
$t_{(\text{cap})}$	Timer capture timing	Timer capture pulse width	-	0.5	-	μ s
$t_{(\text{clk})}$	Timer clock frequency applied to pin	Timer external clock input $f_{\text{HCLK}}=4\text{MHz}$	-	-	PCLK/2	MHz

**Note**

1. The external signal sets the interrupt flag every time the minimum $t_{(\text{int})}$ parameters are met. It may be set even with trigger signals shorter than $t_{(\text{int})}$.
2. Resulted from comprehensive evaluation, not tested in production.

5.3.11.4 Port Leakage Characteristics-PA/PB/PC/PD Port

Table 5-20 PA/PB/PC/PD Port Leakage Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$I_{\text{kg(Px.y)}}$	Leakage current	$V_{(\text{Px.y})}^{(1)(2)}$	-	± 50	-	nA

**Note**

1. The leakage current is measured with VSS or VCC applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input.

5.3.12 RESETB Pin Characteristics

The RESETB pin input driver uses CMOS technology, which is connected with a pull-up resistor that cannot be disconnected.

Table 5-21 RESETB Pin Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{IL(RES\overline{E}TB)}$	Input low-level voltage	-	-0.3	-	0.3VCC	V
$V_{IH(RES\overline{E}TB)}$	Input high-level voltage	-	0.7VCC	-	VCC+0.3	V
$V_{hys(RES\overline{E}TB)}$	Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistance	$V_{IN}=V_{SS}$	-	80	-	k Ω
$T_{F(RES\overline{E}TB)}$	Filtered input pulse	-	-	-	3	μ s
$T_{NF(RES\overline{E}TB)}$	Non-filtered input pulse	-	20	-	-	μ s



Note

1. Guaranteed by design, not tested in production.

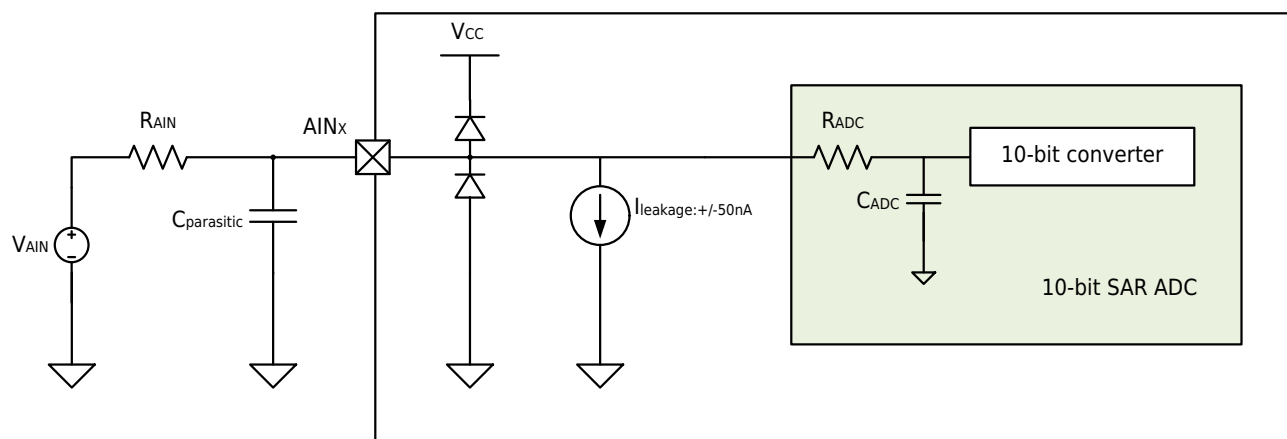
5.3.13 ADC Characteristics

Table 5-22 ADC Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{ADCIN}	Input voltage range	Single ended	0	-	$V_{ADCREFIN}$	V
$V_{ADCREFIN}$	Input range of external reference voltage	Single ended	0	-	AVCC	V
I_{ADC1}	Active current including reference generator and buffer	200ksps	-	0.16	-	mA
I_{ADC2}	Active current including reference generator and buffer	1Msps	-	0.22	-	mA
C_{ADCIN}	ADC input capacitance	-	-	1.6	2	pF
$R_{ADC}^{(1)}$	ADC sampling switch impedance	-	-	5	-	k Ω
$R_{AIN}^{(1)(2)}$	ADC external input resistor	-	-	-	100	k Ω
F_{ADCCLK}	ADC clock frequency	-	-	-	24	MHz
$T_{ADCSTART}$	Startup time of reference generator and ADC core	-	-	5	-	μ s
$T_{ADCCONV}$	Conversion time	-	19	24	25	cycles

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ENOB	Effective bits	1Msps@VCC≥2.7V 500ksps@VCC≥2.4V 200ksps@VCC≥1.7V REF=ExRef	-	9.5	-	bits
		1Msps@VCC≥2.7V 500ksps@VCC≥2.4V 200ksps@VCC≥1.7V REF=VCC	-	9.4	-	bits
SNR	Signal to noise ratio	1Msps@VCC≥2.7V 500ksps@VCC≥2.4V 200ksps@VCC≥1.7V REF=ExRef	-	63	-	dB
		1Msps@VCC≥2.7V 500ksps@VCC≥2.4V 200ksps@VCC≥1.7V REF=VCC	-	63	-	dB
DNL ⁽¹⁾	Differential non-linearity	500ksps, VREF=ExRef/ AVCC	-1	-	1	LSB
INL ⁽¹⁾	Integral non-linearity	500ksps, VREF=ExRef/ AVCC	-2	-	2	LSB
E _o ⁽¹⁾	Offset error	-	-1	-	1	LSB
E _g ⁽¹⁾	Gain error	-	-1	-	1	LSB

1. Guaranteed by design, not tested in production.
2. The typical application of ADC is shown in the figure below:



Under the condition of 0.5LSB sampling error accuracy requirement, the calculation formula of external input impedance is as follows:

$$R_{AIN} = \frac{M}{F_{ADCCLK} * C_{ADC} * (N+1) * \ln(2)} - R_{ADC}$$

F_{ADCCLK} represents the ADC clock frequency, and register ADC_CR0[4:2] can be configured to set its relationship with PCLK as shown in the following table.

The following table shows the ADC clock frequency relationship F_{ADCCLK} with PCLK frequency division ratio:

ADC_CR0[4:2]	N
0b000	1
0b001	2
0b010	4
0b011	8
...	...
0b111	128

M is the number of sampling periods, which is set by the register ADC_CR0[13:12].

The following table shows the relationship between t_{sa} sampling time and ADC clock frequency

F_{ADCCLK} :

ADC_CR0[13:12]	M
0b00	6
0b01	8
0b10	11
0b11	12

The following table shows the relationship between ADC clock frequency F_{ADCCLK} and external resistance R_{AIN} (M=12, under the condition of sampling error 0.5LSB):

R_{AIN} (k Ω)	F_{ADCCLK} (kHz)
10	24000
30	22000
35	18000
60	12000
120	6000
180	4000
360	2000
720	1000
1440	500
2200	350
3600	200
7200	100

For the above typical applications, you should pay attention to:

- Minimize parasitic capacitance $C_{parasitic}$ at the ADC input pins AIN_x .
- In addition to consider R_{AIN} value, if the internal resistance of signal source V_{AIN} is large, it also needs to be considered.

5.3.14 TIM Timer Characteristics

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), see the table below.

Table 5-26 Advanced Timer (ATIM) Characteristics

Symbol	Parameters	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	$f_{TIMCLK}=48MHz$	1	-	t_{TIMCLK}
			20.8	-	ns
f_{ext}	External clock frequency	$f_{TIMCLK}=48MHz$	0	$f_{TIMCLK}/2$	MHz
			0	24	MHz
Res_{Tim}	Timer resolution	Free count	-	16	Bit
			-	32	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle	$f_{TIMCLK}=48MHz$	1	65536	t_{TIMCLK}
			0.0208	1363	μs
T_{MAX_COUNT}	Maximum count value	$f_{TIMCLK}=48MHz$	-	16777216	t_{TIMCLK}
			-	349.5	ms



Note

1. Guaranteed by design, not tested in production.

Table 5-27 General Timer Characteristics

Symbol	Parameters	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	$f_{TIMCLK}=48MHz$	1	-	t_{TIMCLK}
			20.8	-	ns
f_{ext}	External clock frequency	$f_{TIMCLK}=48MHz$	0	$f_{TIMCLK}/2$	MHz
			0	24	MHz
Res_{Tim}	Timer resolution	-	-	16	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle	$f_{TIMCLK}=48MHz$	1	65536	t_{TIMCLK}
			0.0208	1363	μs
T_{MAX_COUNT}	Maximum count value	$f_{TIMCLK}=48MHz$	-	2147483648	t_{TIMCLK}
			-	44.7	s



Note

1. Guaranteed by design, not tested in production.

Table 5-28 Low-Power Timer Characteristics

Symbol	Parameters	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	$f_{TIMCLK}=48MHz$	1	-	t_{TIMCLK}
			20.8	-	ns
f_{ext}	External clock frequency	$f_{TIMCLK}=48MHz$	0	$f_{TIMCLK}/2$	MHz
			0	24	MHz
Res_{Tim}	Timer resolution	-	-	16	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle	$f_{TIMCLK}=48MHz$	1	65536	t_{TIMCLK}
			0.0208	1363	μs
T_{MAX_COUNT}	Maximum count value	$f_{TIMCLK}=48MHz$	-	2147483648	t_{TIMCLK}
			-	44.7	s

**Note**

1. Guaranteed by design, not tested in production.

Table 5-29 IWDTC Characteristics

Symbol	Parameters	Conditions	Min	Max	Unit
t_{res}	WDT overflow time	$f_{WDTCLK}=32.768k$ Hz	0.13	64000	ms

**Note**

1. Guaranteed by design, not tested in production.

Table 5-30 WWDTC Characteristics

Symbol	Parameters	Conditions	Min	Max	Unit
t_{res}	WDT overflow time	$f_{WDTCLK}=48MHz$	0.085	699	ms

**Note**

1. Guaranteed by design, not tested in production.

5.3.15 Communication Interface

5.3.15.1 I2C Characteristics

I2C interface features are as follows:

Table 5-31 I2C Interface Characteristics⁽¹⁾

Symbol	Parameters	Standard Mode (100k)		Fast Mode (400k)		High-Speed Mode (1M)		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCLL}	SCL clock low time	5	-	1.25	-	0.5	-	μs
t_{SCLH}	SCL clock high time	5	-	1.25	-	0.5	-	μs
$t_{SU.SDA}$	SDA establishment time	250	-	100	-	50	-	ns
$t_{HD.SDA}$	SDA hold time	0	-	0	-	0	-	μs
$t_{HD.STA}$	Start Condition Hold Time	2.5	-	0.625	-	0.25	-	μs
$t_{SU.STA}$	Repeated start condition establishment time	2.5	-	0.625	-	0.25	-	μs
$t_{SU.STO}$	Stop condition setup time	0.25	-	0.25	-	0.25	-	μs
t_{BUF}	Bus idle (stop condition to start condition)	4.7	-	1.3	-	0.5	-	μs



Note

1. Guaranteed by design, not tested in production.

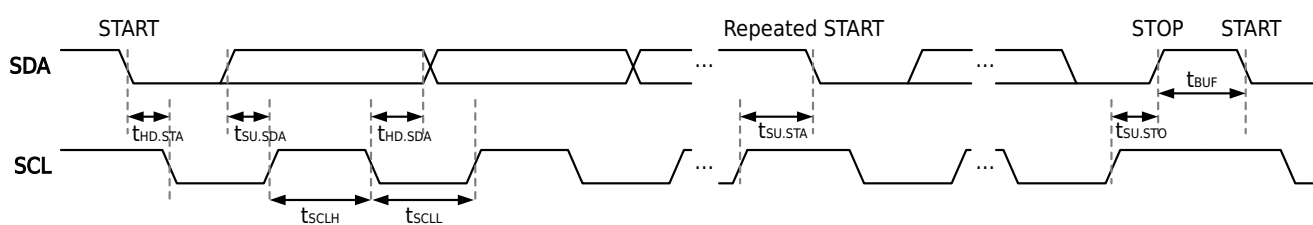


Figure 5-4 I2C interface timing

5.3.15.2 SPI Characteristics

Table 5-32 SPI Interface Characteristics⁽¹⁾⁽²⁾

Symbol	Parameters	Conditions	Min	Max	Unit
$t_{c(SCK)}$	Serial clock period ⁽³⁾	Master transmit mode $f_{PCLK}=32\text{MHz}$	62.5	-	ns
		Master receiving mode $f_{PCLK}=48\text{MHz}$	160	-	ns
		Slave transmit mode $f_{PCLK}=48\text{MHz}$	160	-	ns
		Slave receiving mode $f_{PCLK}=48\text{MHz}$	84	-	ns
$t_{w(SCKH)}$	High level time of serial clock	Master mode	$0.45 \times t_{c(SCK)}$	-	ns
		Slave mode	$0.45 \times t_{c(SCK)}$	-	ns
$t_{w(SCKL)}$	Low level time of serial clock	Master mode	$0.45 \times t_{c(SCK)}$	-	ns
		Slave mode	$0.45 \times t_{c(SCK)}$	-	ns
$t_{su(NSS)}$	Setup time selected by slave	Slave Mode	$0.45 \times t_{c(SCK)}$	-	ns
$t_{h(NSS)}$	Hold time selected by slave	Slave Mode	$0.45 \times t_{c(SCK)}$	-	ns
$t_{v(MO)}$	Effective time of master data output	-	-	3	ns
$t_{h(MO)}$	Hold time of master data output	-	2	-	ns
$t_{v(SO)}$	Effective time of slave data output	-	-	$20 + 1.5 \times T_{PCLK}$	ns
$t_{h(SO)}$	Hold time of slave data output	-	$10 + 0.5 \times T_{PCLK}$	-	ns
$t_{su(MI)}$	Setup time of master data input	-	10	-	ns
$t_{h(MI)}$	Hold time of master data input	-	2	-	ns
$t_{su(SI)}$	Setup time of slave data input	-	10	-	ns
$t_{h(SI)}$	Hold time of slave data input	-	2	-	ns

**Note**

1. Guaranteed by design, not tested in production.
2. The data is provided under the condition of $V_{CC}=3.0\text{V}$.
3. The maximum frequency division factor of the master mode is $PCLK/2$, and the The maximum frequency division factor of slave mode is $PCLK/4$.

The waveform and timing parameters of the SPI interface signal are as follows:

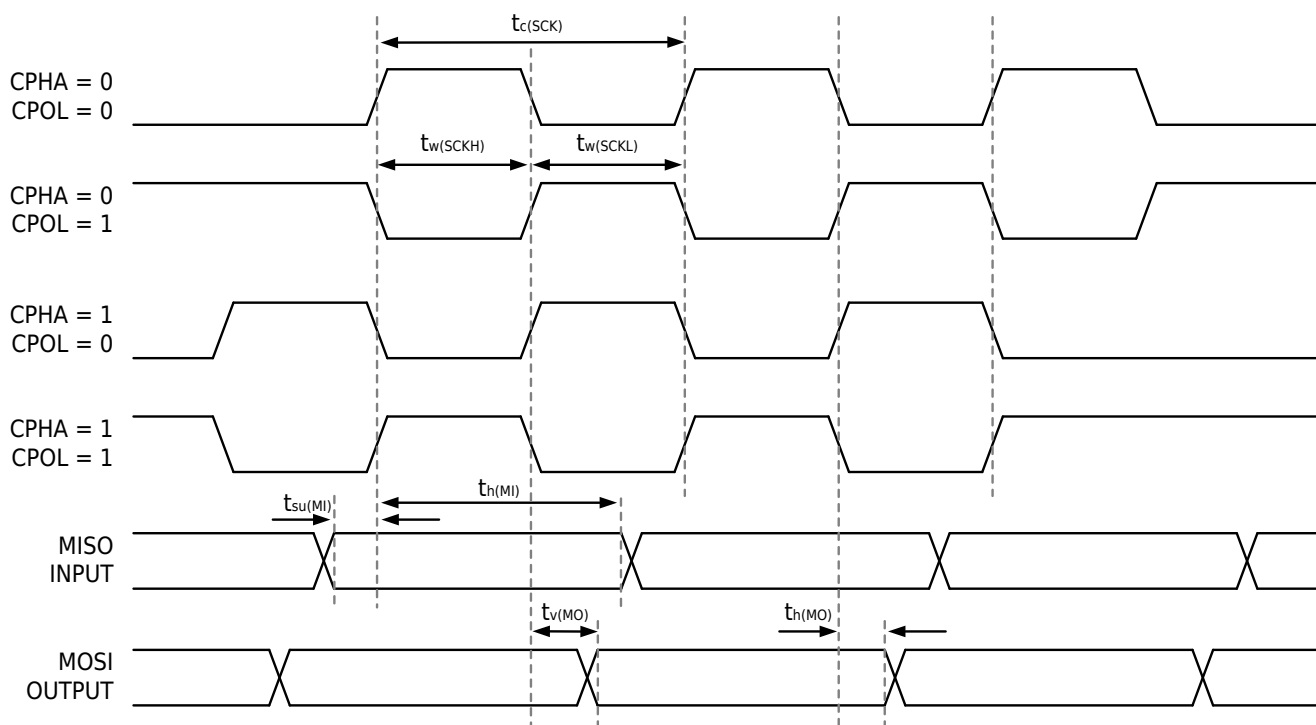


Figure 5-5 SPI Timing Diagram (Master Mode)

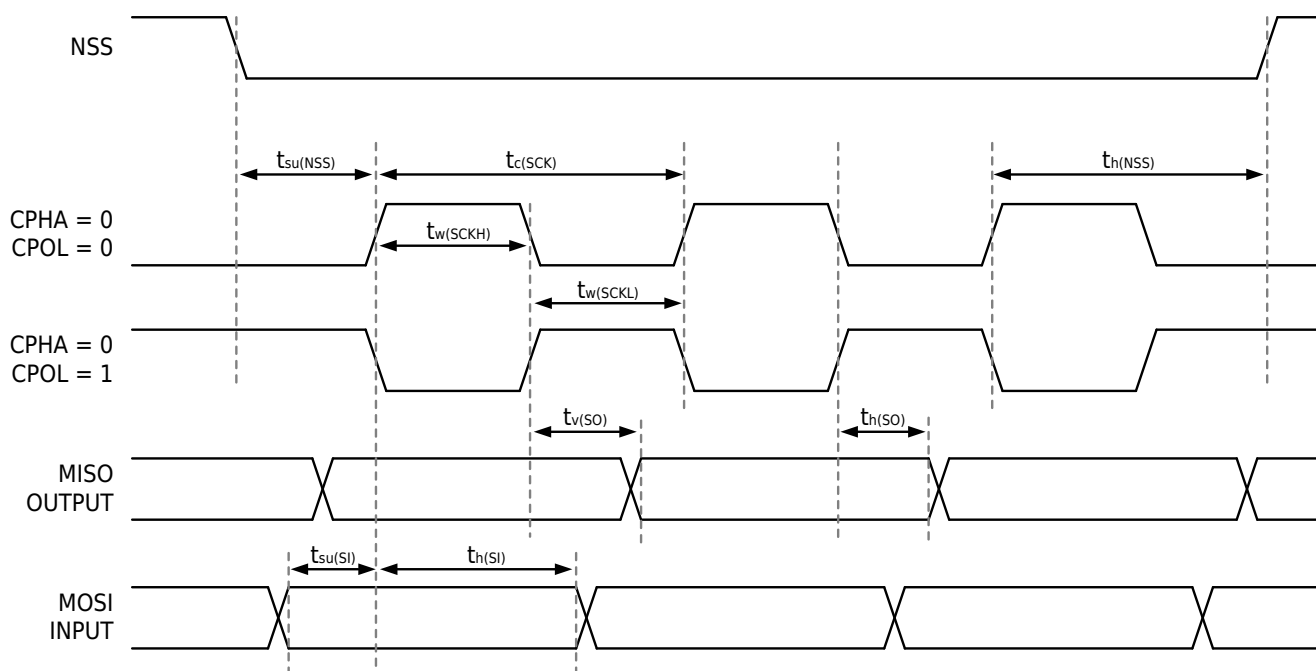


Figure 5-6 SPI Timing Diagram (Slave Mode CPHA=0)

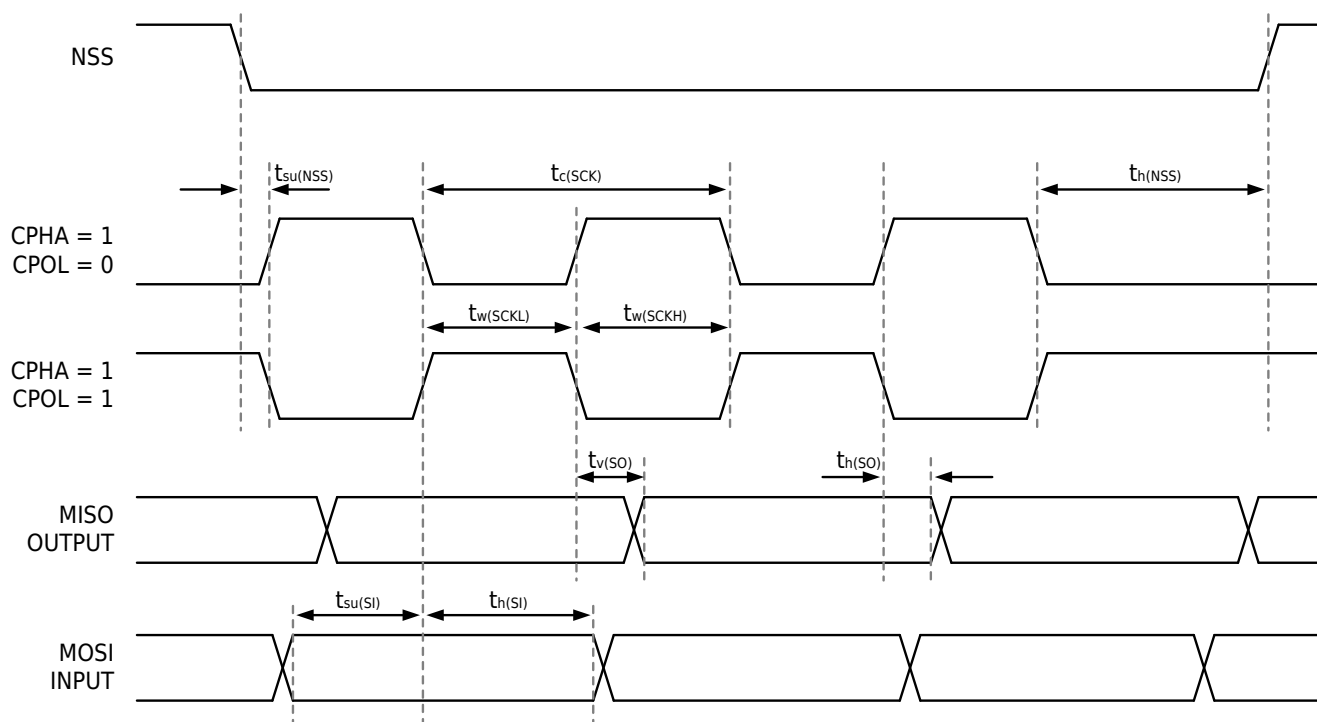
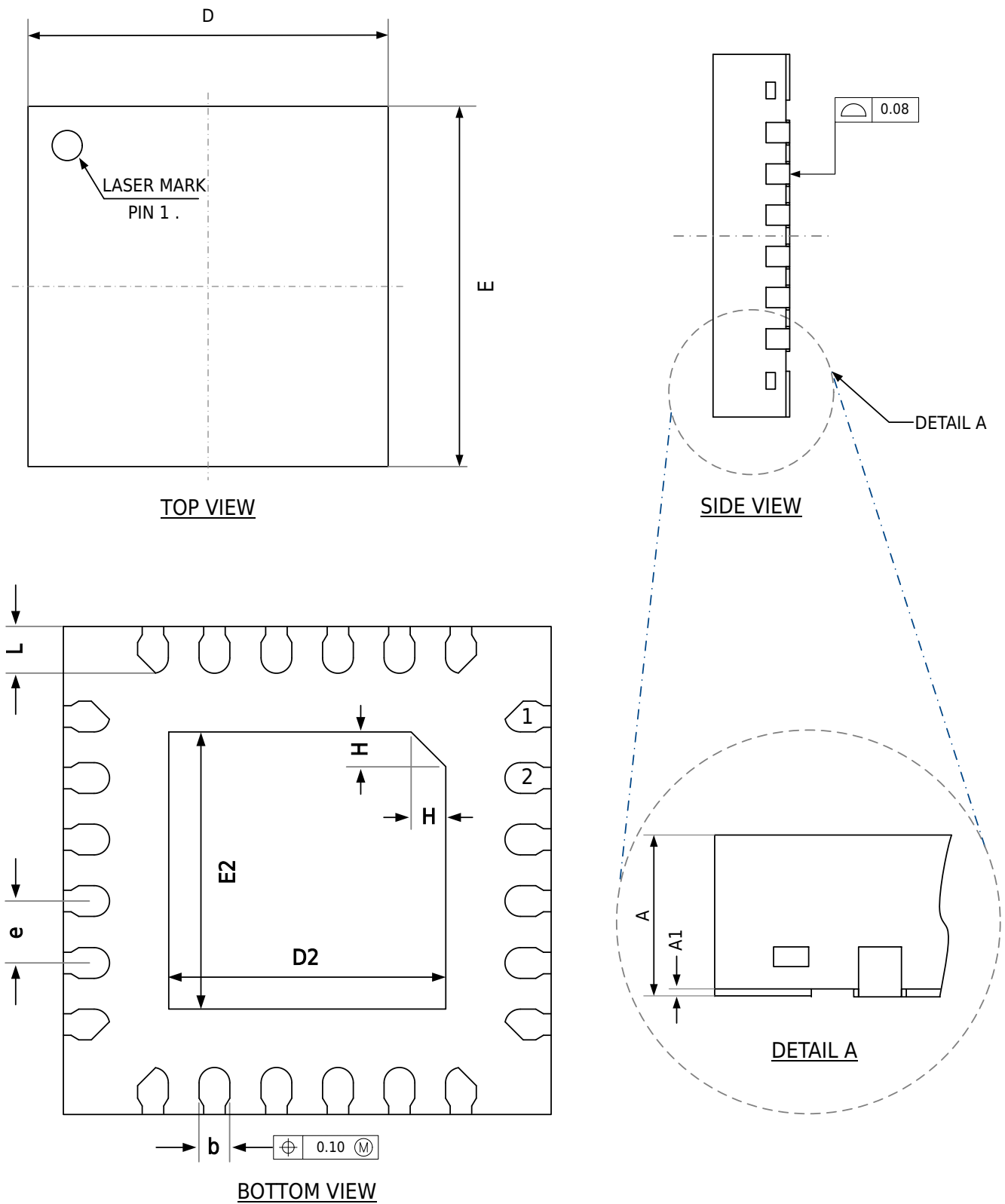


Figure 5-7 SPI Timing Diagram (Slave Mode CPHA=1)

6 Package Specifications

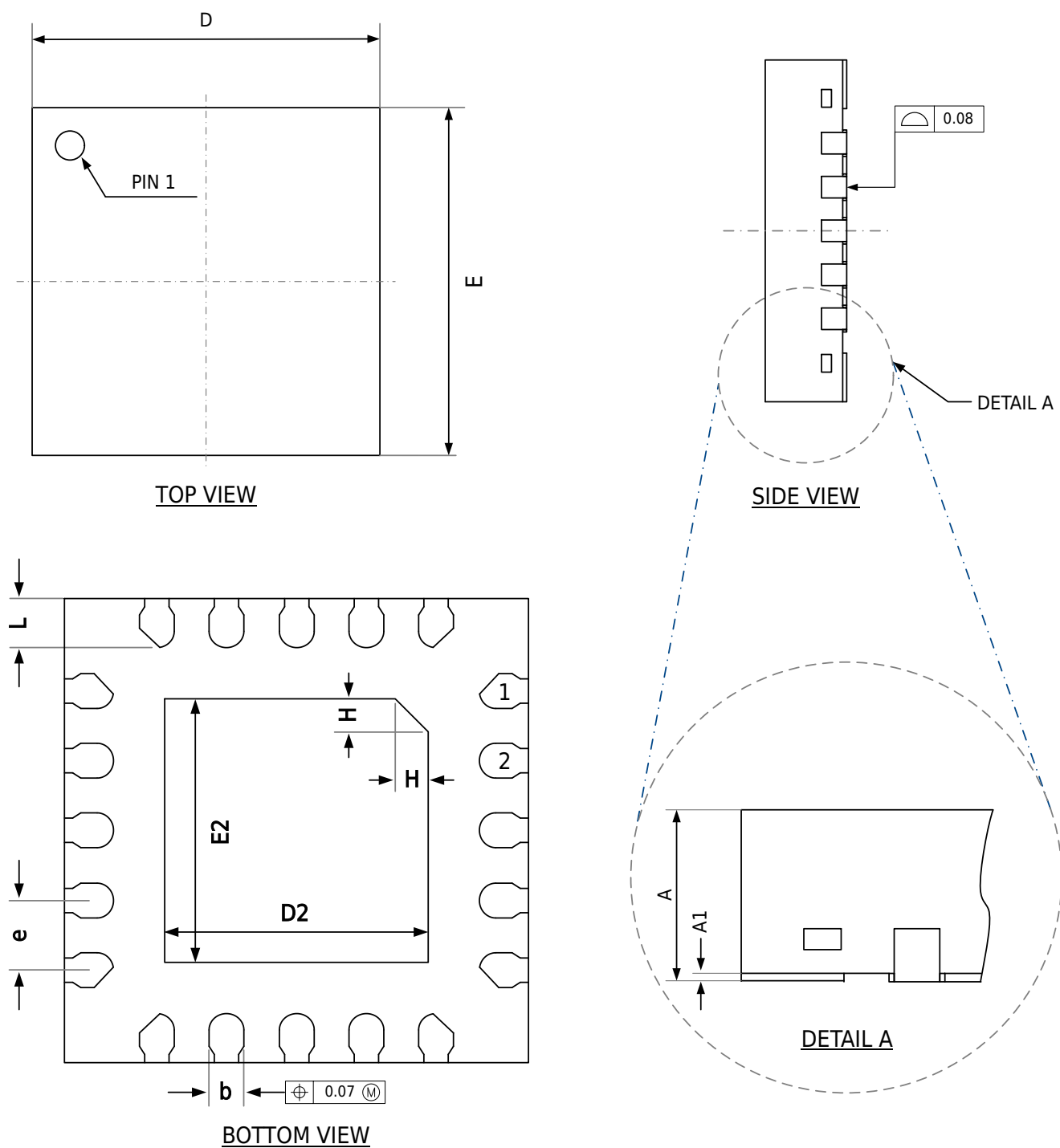
6.1 Package Dimensions

6.1.1 QFN24 Package



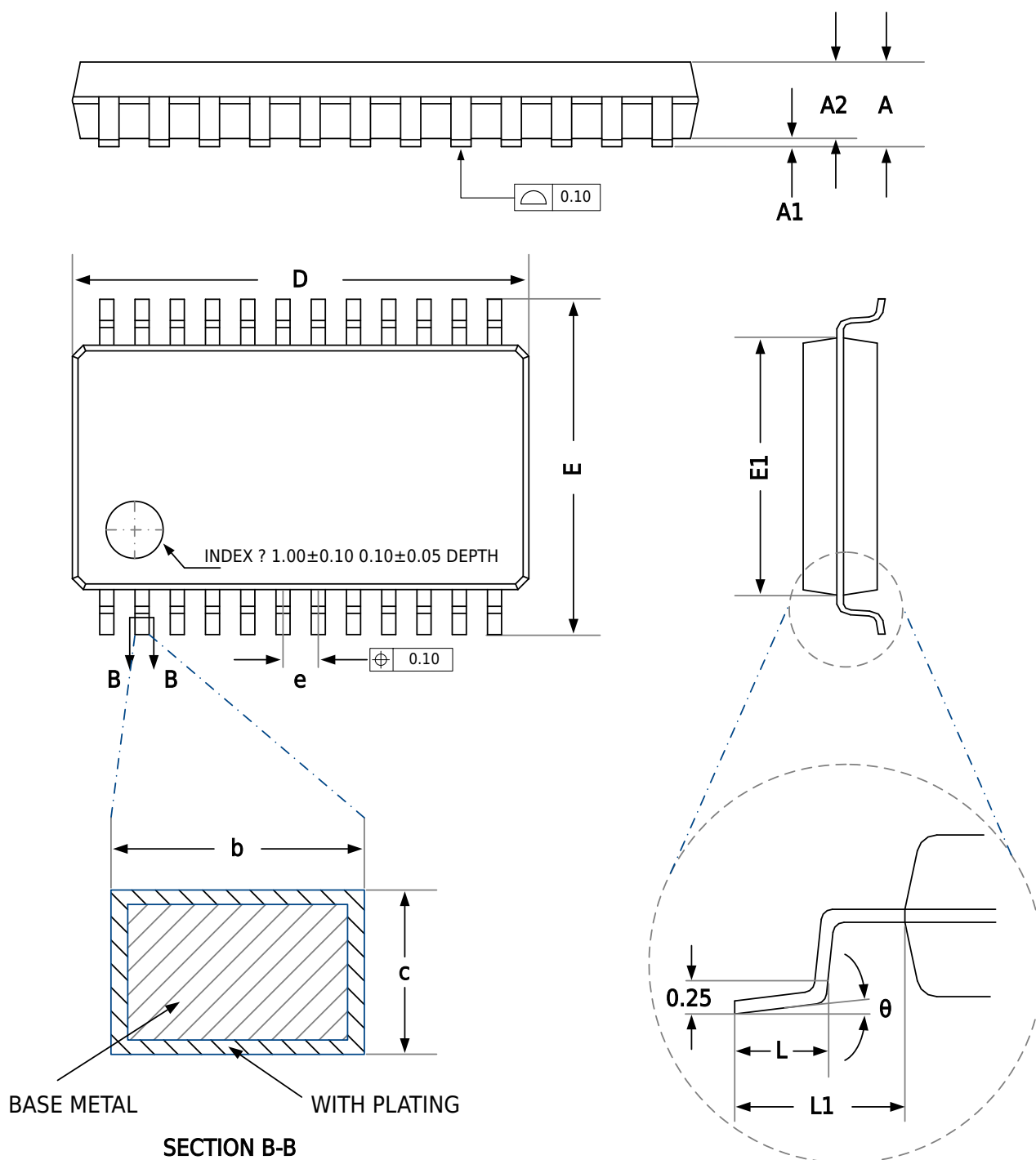
Symbol	4*4 Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D2	2.15	2.25	2.35
E	3.90	4.00	4.10
E2	2.15	2.25	2.35
e	0.40	0.50	0.60
L	0.35	0.40	0.45
H	0.35REF		

6.1.2 QFN20 Package



Symbol	3*3 Millimeter		
	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
D	2.90	3.00	3.10
D2	1.60	1.70	1.80
E	2.90	3.00	3.10
E2	1.60	1.70	1.80
e	0.30	0.40	0.50
L	0.25	0.30	0.35
H	0.25REF		

6.1.3 TSSOP24 Package

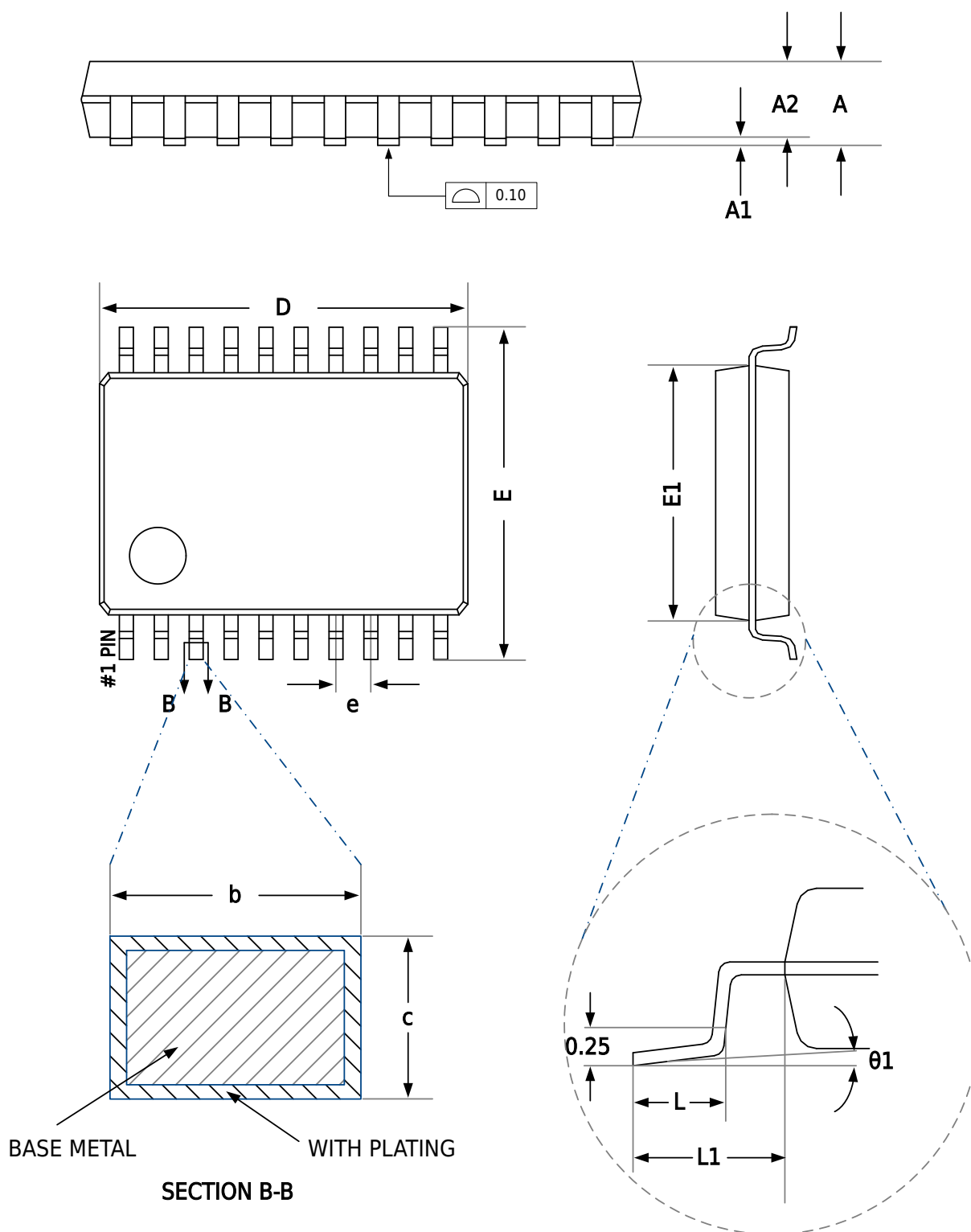


Symbol	Millimeter		
	Min	Nom	Max
A	--	--	1.20
A1	0.05	--	0.15
A2	0.80	0.90	1.00
b	0.20	--	0.29
c	0.10	--	0.19
D	7.70	7.80	7.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	--	8°

**Note**

Dimensions "D1" and "E1" do not include mold flash.

6.1.4 TSSOP20 Package



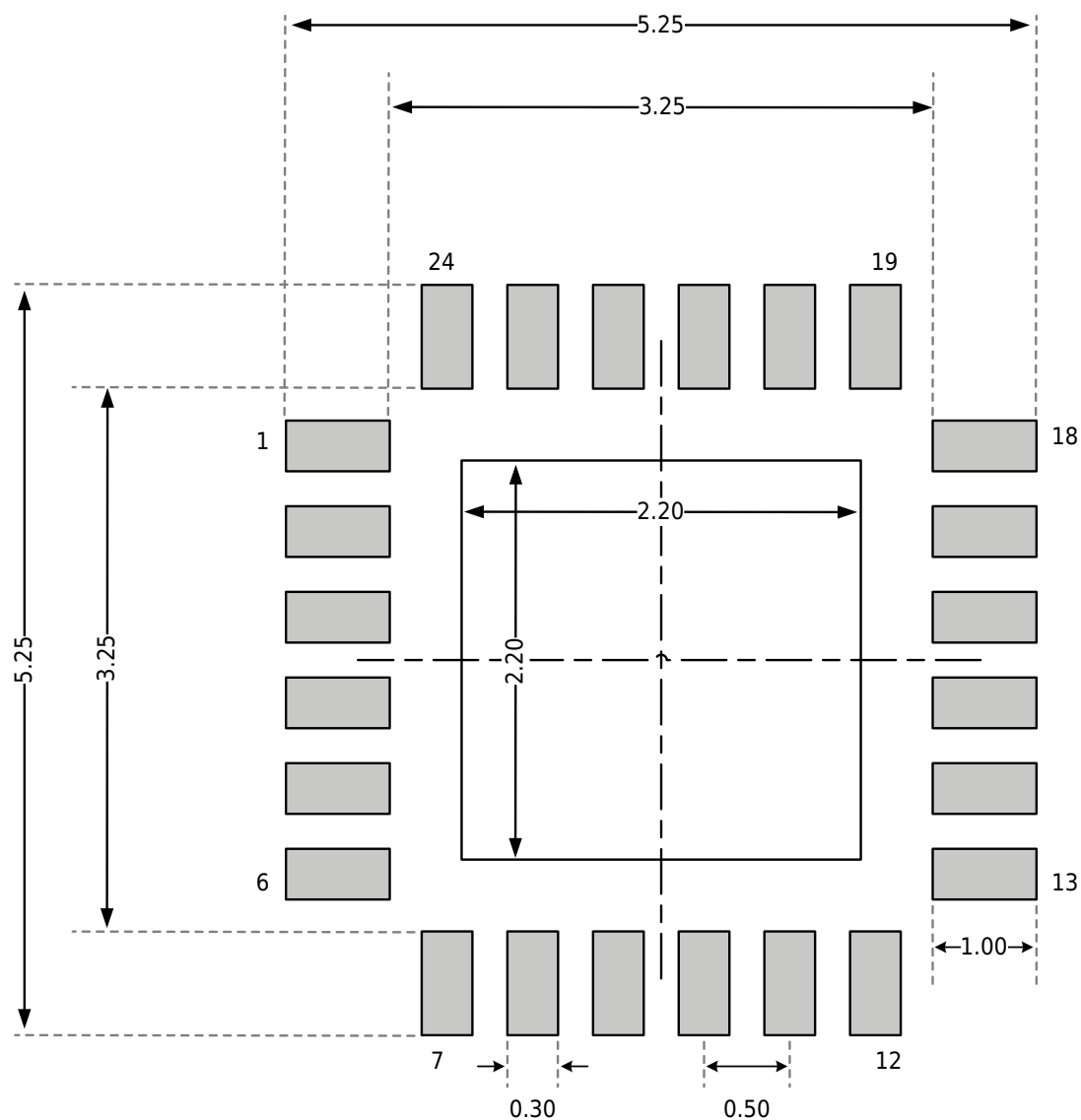
Symbol	Millimeter		
	Min	Nom	Max
A	--	--	1.20
A1	0.05	--	0.15
A2	0.90	1.00	1.05
b	0.20	--	0.28
c	0.10	--	0.19
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ1	0°	--	8°

**Note**

Dimensions "D1" and "E1" do not include mold flash.

6.2 PCB Land Pattern

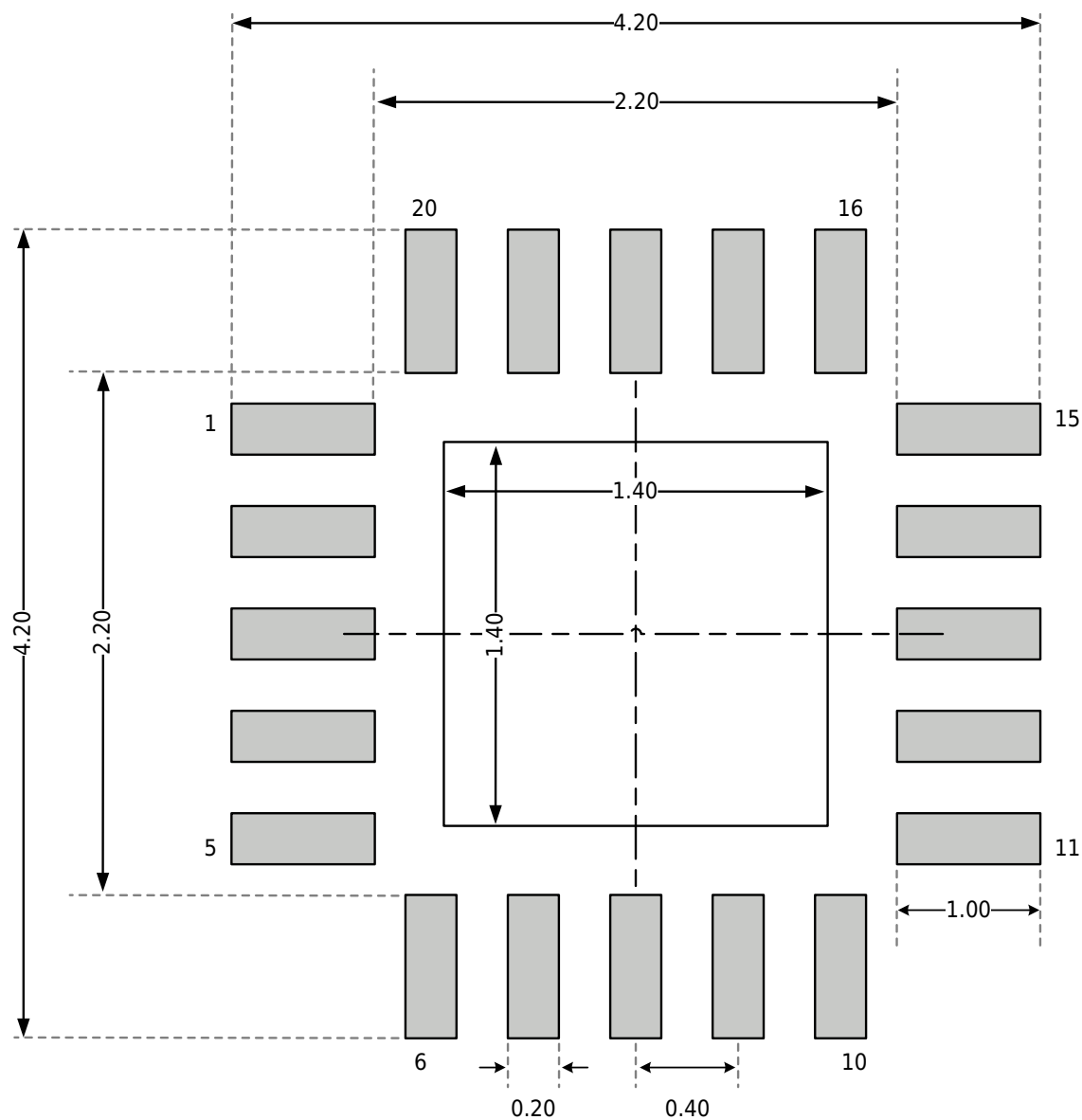
6.2.1 QFN24 Package (4mm*4mm)



Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

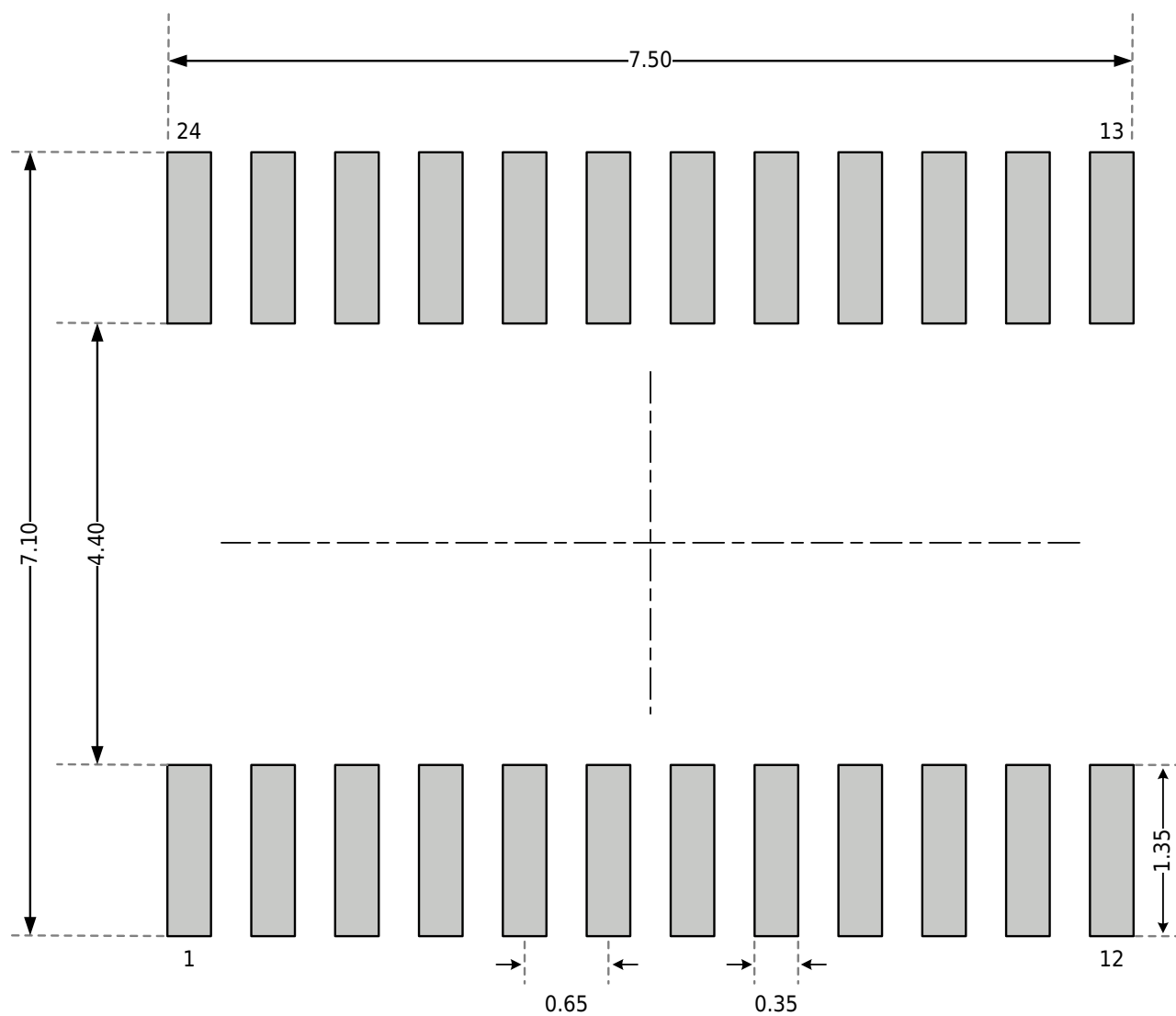
6.2.2 QFN20 Package (3mm*3mm)



Note

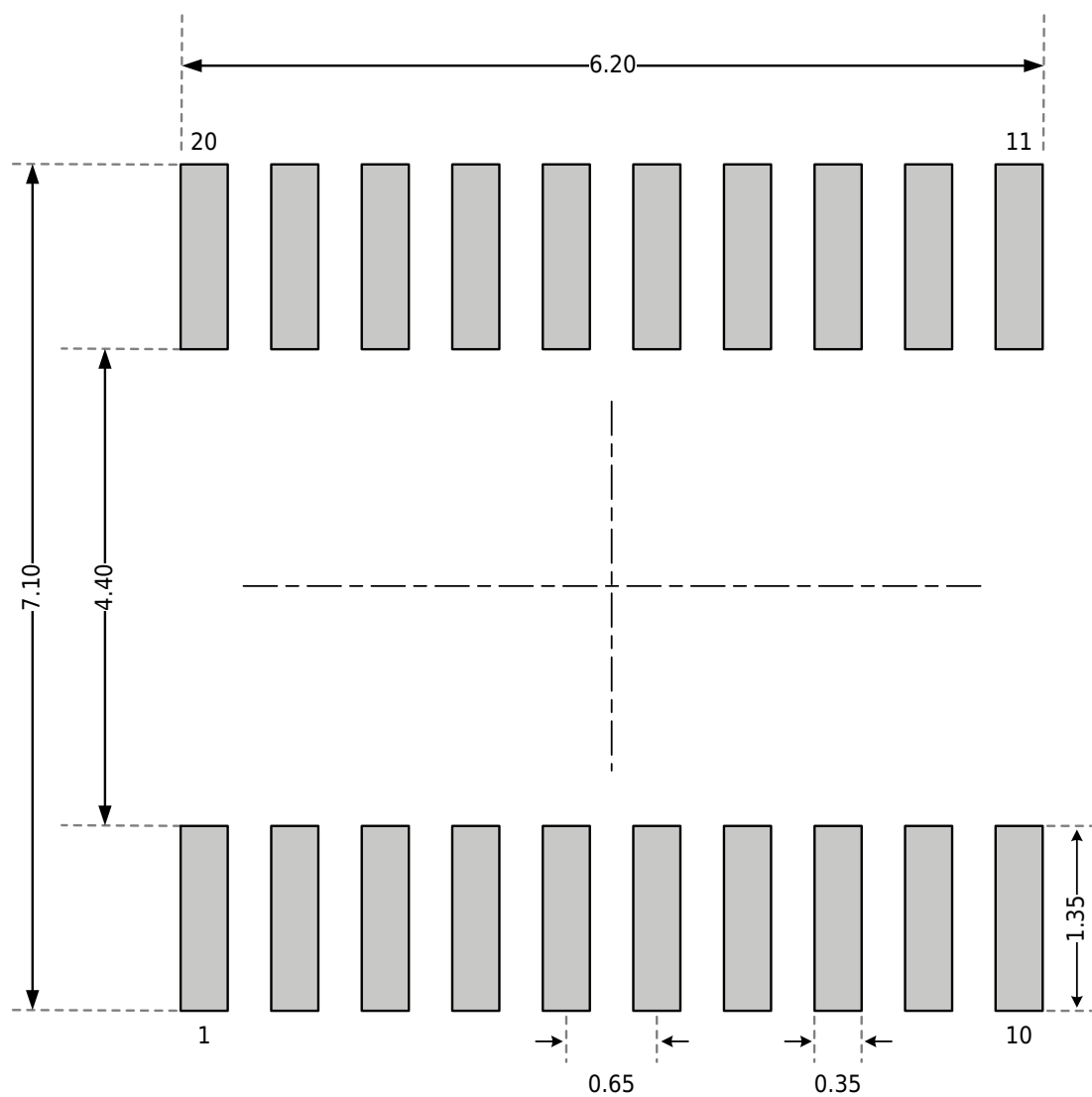
- Dimensions are in millimeters.
- Dimensions are for reference only.

6.2.3 TSSOP24 Package

**Note**

- Dimensions are in millimeters.
- Dimensions are for reference only.

6.2.4 TSSOP20 Package



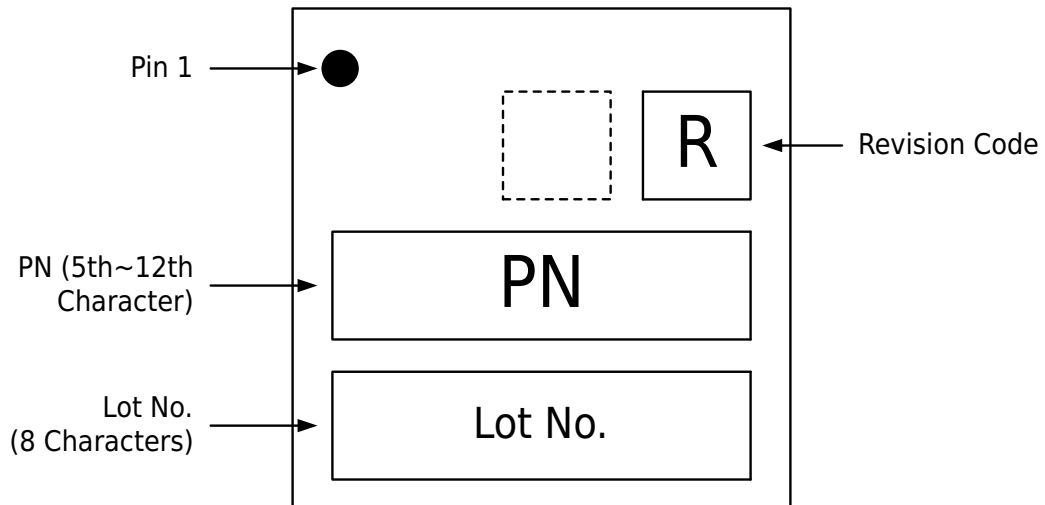
Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

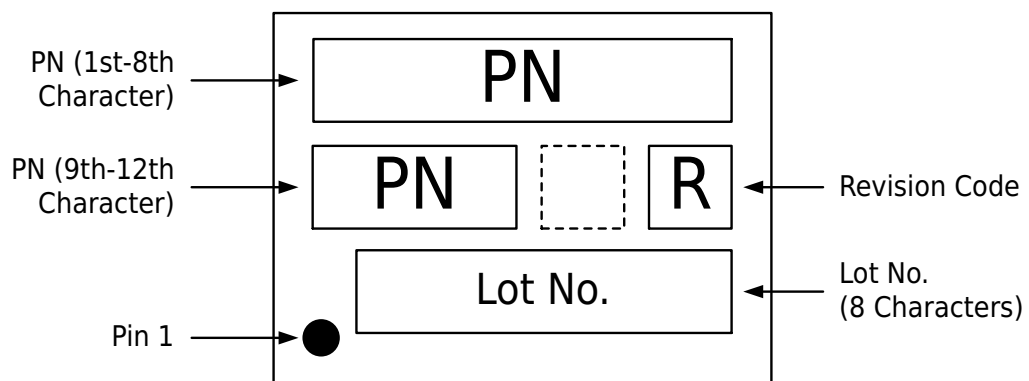
6.3 Package Marking

The location and information description of Pin1 on the front of each package are given below.

QFN24 package (4mm*4mm)/QFN20 package (3mm*3mm)



TSSOP24 package/TSSOP20 package



Note

The blank boxes in the above figure indicate optional marks related to production, which are not explained in this section.

6.4 Packaging Thermal Resistance Coefficient

When the packaged chip is working at the specified working environment temperature, the junction temperature $T_j(^{\circ}\text{C})$ of the chip surface can be calculated according to the following formula:

$$T_j = T_A + (P_D * \theta_{JA})$$

- T_A refers to the working environment temperature when the packaged chip is working, the unit is $^{\circ}\text{C}$;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is $^{\circ}\text{C}/\text{W}$;
- P_D refers to total power dissipation, which is the sum of internal power consumption (P_{INT}) and I/O pin power consumption (P_{IO}), the unit is W.

$$P_D = P_{INT} + P_{IO}$$

- ▶ P_{INT} : Internal power consumption, calculated as the product of I_{VCC} and V_{CC} .

- P_{IO} : I/O pin power consumption, calculated as: $P_{IO} = \Sigma(V_{OL} * I_{OL}) + \Sigma((V_{CC} - V_{OH}) * I_{OH})$

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable junction temperature T_{jmax} of the chip.

Table 6-5 Thermal Resistance Coefficient Reference Table For Each Package

Package Type and Dimensions	Thermal Resistance Parameters (θ_{JA})	Unit
QFN24 4mm*4mm/0.5mm pitch	53±10%	°C/W
QFN20 3mm*3mm/0.4mm pitch	70±10%	°C/W
TSSOP24	80±10%	°C/W
TSSOP20	91±10%	°C/W

7 Ordering Information

Part Number	HC32F002C4PZ-TSSOP20	HC32F002C4PZ-TSSOP20TR	HC32F002C4UZ-ZFN20TR	HC32F002D4PZ-TSSOP24	HC32F002D4PZ-TSSOP24TR	HC32F002D4UZ-QFN24TR
GPIO	17+1	17+1	17+1	21+1	21+1	21+1
Core	Cortex-M0+	Cortex-M0+	Cortex-M0+	Cortex-M0+	Cortex-M0+	Cortex-M0+
Frequency	48MHz	48MHz	48MHz	48MHz	48MHz	48MHz
Flash	18KB	18KB	18KB	18KB	18KB	18KB
RAM	2KB	2KB	2KB	2KB	2KB	2KB
Power Supply Voltages	1.7-5.5V	1.7-5.5V	1.7-5.5V	1.7-5.5V	1.7-5.5V	1.7-5.5V
Temp Range	-20-105°C	-20-105°C	-20-105°C	-20-105°C	-20-105°C	-20-105°C
LPTimer	1	1	1	1	1	1
Basic Timer	[3] ⁽¹⁾	[3] ⁽¹⁾	[3] ⁽¹⁾	[3] ⁽¹⁾	[3] ⁽¹⁾	[3] ⁽¹⁾
General Timer	1	1	1	1	1	1
Advanced Timer	1	1	1	1	1	1
IWDT	1	1	1	1	1	1
WWDT	1	1	1	1	1	1
LPUART	2	2	2	2	2	2
I2C	1	1	1	1	1	1
SPI	1	1	1	1	1	1
10-bit ADC	11ch	11ch	11ch	14ch	14ch	14ch
LVD	√	√	√	√	√	√
Package (mm*mm)	TSSOP20	TSSOP20	QFN20(3*3)	TSSOP24	TSSOP24	QFN24(4*4)
Pins	20	20	20	24	24	24
Packing	Tube	Tape & Reel	Tape & Reel	Tube	Tape & Reel	Tape & Reel
Pitch	0.65mm	0.65mm	0.4mm	0.65mm	0.65mm	0.5mm
Thickness	1.2mm	1.2mm	0.55mm	1.2mm	1.2mm	0.75mm



Note

1. This module is time-division multiplexed with the General Timer.

Part Number	HC32F002C4PB-TSSOP20	HC32F002C4PB-TSSOP20TR	HC32F002C4UB-ZFN20TR	HC32F002D4PB-TSSOP24	HC32F002D4PB-TSSOP24TR	HC32F002D4UB-QFN24TR
GPIO	17+1	17+1	17+1	21+1	21+1	21+1
Core	Cortex-M0+	Cortex-M0+	Cortex-M0+	Cortex-M0+	Cortex-M0+	Cortex-M0+
Frequency	48MHz	48MHz	48MHz	48MHz	48MHz	48MHz
Flash	18KB	18KB	18KB	18KB	18KB	18KB
RAM	2KB	2KB	2KB	2KB	2KB	2KB
Power Supply Voltages	2.7-5.5V	2.7-5.5V	2.7-5.5V	2.7-5.5V	2.7-5.5V	2.7-5.5V
Temp Range	-40-105°C	-40-105°C	-40-105°C	-40-105°C	-40-105°C	-40-105°C
LPTimer	1	1	1	1	1	1
Basic Timer	[3] ⁽¹⁾	[3] ⁽¹⁾	[3] ⁽¹⁾	[3] ⁽¹⁾	[3] ⁽¹⁾	[3] ⁽¹⁾
General Timer	1	1	1	1	1	1
Advanced Timer	1	1	1	1	1	1
IWDT	1	1	1	1	1	1
WWDT	1	1	1	1	1	1
LPUART	2	2	2	2	2	2
I2C	1	1	1	1	1	1
SPI	1	1	1	1	1	1
10-bit ADC	11ch	11ch	11ch	14ch	14ch	14ch
LVD	√	√	√	√	√	√
Package (mm*mm)	TSSOP20	TSSOP20	QFN20(3*3)	TSSOP24	TSSOP24	QFN24(4*4)
Pins	20	20	20	24	24	24
Packing	Tube	Tape & Reel	Tape & Reel	Tube	Tape & Reel	Tape & Reel
Pitch	0.65mm	0.65mm	0.4mm	0.65mm	0.65mm	0.5mm
Thickness	1.2mm	1.2mm	0.55mm	1.2mm	1.2mm	0.75mm

**Note**

1. This module is time-division multiplexed with the General Timer.

Please contact the sales window for the latest mass production information before ordering.

Revision History

Revision/Date	Changes
Rev1.50 Aug. 28, 2026	1. Typical Application Circuit Diagram: the decoupling capacitor description is optimized. 2. Electrical Specifications: In the "Absolute Maximum Ratings" chapter, the voltage and current tables is combined; 3. Package Specifications: In the "PCB Land Pattern" section, the redundant data is removed;
Rev1.42 Feb. 12, 2026	1. Electrical Specifications: In the "Absolute Maximum Ratings" chapter, the symbol "T_J" representing temperature characteristics is revised to "T_{Jmax}"; In the "General Operating Conditions" chapter, the descriptions related to power dissipation have been removed; In the "Memory Characteristics" chapter, the data of EC_{FLASH} parameters have been optimized and updated based on new conditions; 2. Package Specifications: In the "Package Dimensions" chapter, the A2, A3, K, R, c1, c2 of QFN package have been removed; In the "QFN24 Package" chapter, the min value of b is modified to "0.18"; In the "QFN20 Package" chapter, the max value of L is modified to "0.35", the max and min value of D2/E2 is modified to "1.80, 1.60", the value of H is modified to "0.25REF".
Rev1.41 May 12, 2025	1. Electrical Specifications: In the "Operating Conditions-General Operating Conditions" chapter, delete P_D; In the "Operating Conditions-Supply Current Characteristics" chapter, describe data according to product categories; In the "Operating Conditions-Internal Clock Source Characteristics-RCH" chapter, for RCH oscillator accuracy conditions, delete voltage description, change temperature condition from "$T_{AMB}=-40-50^{\circ}C$" to "$T_A=-20-50^{\circ}C$", and add data corresponding to "$-20-105^{\circ}C$" condition; In the "Operating Conditions-Internal Clock Source Characteristics-RCL" chapter, for RCL oscillator accuracy conditions, delete voltage description, change temperature condition from "$T_{AMB}=-40-50^{\circ}C$" to "$T_A=-20-50^{\circ}C$", and add data corresponding to "$T_A=-20-105^{\circ}C$" condition; In the "Operating Conditions-Communication Interface-SPI Characteristics" chapter, adjust parameters such as serial clock cycle, slave data output valid time, and slave data output hold time, and add table notes: "Data is based on $CC=3.0V$ condition", "The maximum division factor in master mode is $PCLK/2$, and in slave mode is $PCLK/4$"; 2. Package Specifications: In the "Package Dimensions" chapter, the b1 and b2 in SECTION B-B have been removed.
Rev1.40 Dec. 24, 2024	1. The manual style is refreshed according to the structured development process. 2. Product Overview: In the "Product Lineup" chapter, adjust the format of the model feature comparison table, update the ADC supported channels description, add "Memory", "Watchdog Timer" and "Package Type", and delete "Unique Identification Code" and "Port Interrupt".

Revision/Date	Changes
Rev1.40 Dec. 24, 2024	- Functional Description: In the "32-bit Cortex-M0+ Core" chapter, change the description from "15 fast interrupts" to "32 fast interrupts (for detailed interrupt specifications supported by this product, refer to 'Interrupt Controller NVIC')"; In the "Serial Peripheral Interface SPI" chapter, modify the description from "The maximum division factor in master mode is PCLK/2 with a maximum communication rate of 12Mbps" to "The maximum division factor in master mode is PCLK/2 with a maximum communication rate of 16Mbps". - Pin Definitions: In the "QFN20 Package" chapter, add the description "Exposed Thermal Pad must be connected to DVSS". - Electrical Specifications: Optimize the definitions of maximum, minimum, and typical parameter values in the "Parameter Conditions" chapter; Adjust data sources throughout the chapter according to the latest specifications; In the "I2C Characteristics" chapter, change the unit of $t_{SU,SDA}$ from "μs" to "ns"; In the "SPI Characteristics" chapter, modify the minimum value of $t_{h(MO)}$ from "-2" to "2". - Package Specifications: in the "Packaging Thermal Resistance Coefficient" chapter, the description of P_D is adjusted to make it more practical. - Ordering Information: Adjust the sorting of some information, add support status for IWDG and WWDG, and delete "LVR" and "Number of Pins".
Rev1.30 Aug. 22, 2024	- Delete the EXTCLK clock related content in both the "Functional Description" chapter and the "Pin Definitions" chapter. - Change the storage temperature from "-60-+150" to "-65-+150". - Delete the "7.3.7 External Clock Source Characteristics" chapter. - Added six product model: HC32F002C4PB-TSSOP20/HC32F002C4UB-ZFN20TR/HC32F002D4PB-TSSOP24/HC32F002D4UB-QFN24TR/HC32F002C4PB-TSSOP20TR/HC32F002D4PB-TSSOP24TR, modify the voltage and temperature information.
Rev1.21 Jun. 21, 2023	In the "Pinout" chapter, add GND connection information for QFN packages.
Rev1.20 Oct. 14, 2022	- Add two new models: HC32F002C4PZ-TSSOP20TR, HC32F002D4PZ-TSSOP24TR; - In the "Pinout" chapter, add TR models and modify the corresponding figure titles accordingly. - In the "Ordering Information" chapter, add the new models with packaging method as Tape & Reel.
Rev1.10 Mar. 9, 2022	The company logo is updated.
Rev1.00 Dec. 31, 2021	First official release.