

HC32F005_F003 Series

32-bit ARM[®] Cortex[®]-M0+ Microcontroller

Datasheet

Rev3.00 August 2026

Features

- 32MHz Cortex-M0+ 32-bit CPU platform
- HC32F003 series/ HC32F005 series has a flexible power management system
 - 5μA @ 3V Deep-sleep mode: all clocks off, power-on reset active, IO state retention, IO interrupt active, all registers, RAM and CPU data save state power consumption
 - 10μA @ 32kHz low-speed working mode: CPU and peripheral modules run, run programs from Flash
 - 30μA/MHz @3V@16MHz sleep mode: CPU stops working, peripheral modules run, and main clock runs
 - 150μA/MHz@3V@16MHz working mode: CPU and peripheral modules run, and programs run from Flash
 - 4μs low power consumption wake-up time, making mode switching more flexible and efficient, and system response more agile
 - The above characteristics are typical values at room temperature. For specific electrical characteristics and power consumption characteristics, refer to the [Electrical characteristics] chapter
- Flash memory, with erase and write protection function
 - The HC32F003 series supports 16KB Flash
 - The HC32F005 series supports 32KB Flash
- RAM memory with parity check to enhance system stability
 - The HC32F003 series supports 2KB RAM
 - The HC32F005 series supports 4KB RAM
- General I/O pins (16IO/20pin, 12IO/16pin)
- Clock, crystal
 - Internal high-speed clock 4/8/16/22.12/24MHz
 - Internal low-speed clock 32.8/38.4KHz
 - External high-speed crystal oscillator 8 ~ 32MHz
 - Hardware supports internal and external clock calibration and monitoring
- Timer/counter
 - 3 general-purpose 16-bit timer / counters
 - 3 high-performance 16-bit timers/counters, support PWM complementary, dead zone protection function
 - 1 programmable 16-bit timer / counter, support capture compare, PWM output
- 1 20-bit programmable counting watchdog circuit, built-in dedicated low power RC -OSC to provide WDT counting
- Communication Interface
 - UART0-UART1 standard communication interface
 - SPI standard communication interface
 - I²C standard communication interface
- Buzzer frequency generator, support complementary output
- Hardware CRC-16 module
- Unique 10-byte ID number
- 12-bit 1Msps sampling high-speed and high-precision SARADC, built-in op amp, can measure external weak signals
- 2-way voltage comparator VC with integrated 6-bit DAC and programmable reference input
- Integrated low voltage detector LVD, configurable 16-level comparison level, can monitor port voltage and power supply voltage
- Embedded debug solution that provides a full-featured real-time debugger
- Working temperature: -40 ~ 85 °C/ -40 ~ 105°C
- Working voltage: 1.8 ~ 5.5V
- Package form: QFN20, QFN24, TSSOP20, SOP20

Support Model:

HC32F003C4UA	HC32F003C4PA
HC32F005C6UA	HC32F005C6PA
HC32F005C6PB	HC32F003C4PB

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Contents

Features	2
Statement	3
Contents	4
Table Index	6
Figure Index	7
1 Introduction	8
2 Product lineup	18
2.1 Product name	18
2.2 Function	19
3 Pin configuration	20
4 Pin function description	22
5 Block diagram	27
6 Storage area map	28
7 Electrical characteristics	30
7.1 Test Conditions	30
7.1.1 Minimum and maximum values	30
7.1.2 Typical value	30
7.2 Absolute maximum ratings	31
7.3 Operating conditions	32
7.3.1 General working conditions	32
7.3.2 Working conditions at power-up and power-down	32
7.3.3 Embedded reset and LVD module features	32
7.3.4 Built-in reference voltage	34
7.3.5 Operating Current Characteristics	35
7.3.6 Time to wake up from low power mode	36
7.3.7 External timer characteristic	37
7.3.8 Internal timer characteristics	40
7.3.9 Memory Characteristics	41
7.3.10 EFT Characteristic	41
7.3.11 ESD Characteristic	41
7.3.12 Port characteristics	42
7.3.13 RESETB pin characteristics	46
7.3.14 ADC Characteristic	46
7.3.15 VC Characteristic	49
7.3.16 TIM timer features	50
7.3.17 Communication Interface	52

8	Typical application circuit diagram	56
9	Package information	57
9.1	Packaging Size.....	57
9.2	Schematic diagram of pad	60
9.3	Silkscreen instructions.....	63
9.4	Packaging Thermal Resistance Coefficient	64
10	Ordering Information	65
	Version revision history	66

Table Index

Table 7-1	Voltage and Current Characteristics.....	31
Table 7-2	temperature characteristics	31
Table 7-3	General Operating Conditions	32
Table 7-4	Power-up and power-down operating conditions	32
Table 7-5	POR/Brown Out.....	33
Table 7-6	LVD module characteristics	33
Table 7-7	Operating Current Characteristics.....	35
Table 7-8	Port output characteristics	42
Table 7-9	Advanced Timer (ADVTIM) Features	50
Table 7-10	Basic Timer Characteristics	50
Table 7-11	PCA Characteristics	51
Table 7-12	WDT Characteristics.....	51
Table 7-13	I2C Interface Characteristics	52
Table 7-14	SPI Interface Features ⁽¹⁾⁽²⁾	53
Table 9-1	Thermal resistance coefficient table for each package	64

Figure Index

Figure 5-1	Functional modules.....	27
Figure 7-1	POR/Brown Out Diagram.....	32
Figure 7-2	VOH/VOL measured curve of output port.....	43
Figure 7-3	I2C Interface Timing	52
Figure 7-4	SPI Timing Diagram (Host Mode)	54
Figure 7-5	SPI Timing Diagram (slave mode cpha=0)	54
Figure 7-6	SPI Timing Diagram (slave mode cpha=1)	55

1 Introduction

The HC32F003 series/ HC32F005 series is a Low Pin Count, wide voltage operating range MCU. Integrating 12-bit 1Msps high-precision SARADC and integrating rich communication peripherals such as comparator, multi-channel UART, SPI, I2C, etc., it has the characteristics of high integration, high anti-interference, and high reliability. The core of this product adopts the Cortex-M0+ core, cooperates with mature Keil & IAR debugging and development software, supports C language, assembly language, and assembly instructions.

Low Pin Count MCU typical applications

- Small household appliances, chargers, reclosing devices, remote controls, e-cigarettes, gas alarms, digital meters, thermostats, recorders and other industries;
- Smart transportation, smart city, smart home;
- Fire alarm probes, smart door locks, wireless monitoring and other smart sensor applications;
- Motor drive.

32-bit CORTEX M0+ core

The ARM® Cortex®-M0+ processor is derived from Cortex-M0 and includes a 32-bit RISC processor with a computing power of 0.95 Dhrystone MIPS/MHz. At the same time, a number of new designs have been added to improve debugging and tracing capabilities, reduce the number of each instruction cycle (IPC) and improve the two-stage pipeline for Flash access, and incorporate energy-saving and consumption-reducing technologies. The Cortex-M0+ processor fully supports the integrated Keil & IAR debugger.

Cortex-M0+ includes a hardware debugging circuit that supports 2-pin SWD debugging interface.

ARM Cortex-M0+ features:

Instruction Set	Thumb / Thumb-2
Assembly line	2-stage assembly line
Performance efficiency	2.46 CoreMark / MHz
Performance efficiency	0.95 DMIPS / MHz in Dhrystone
Interrupt	32 fast interrupts
Interrupt priority	Configurable 4-level interrupt priority
Enhanced instruction	Single-cycle 32-bit multiplier
Debugging	Serial-wire debug port, supports 4 hard interrupts (break points) and 2 watch points (watch points)

16K/32K Byte Flash

The built-in fully integrated Flash controller does not require external high voltage input, and the high voltage is generated by the fully built-in circuit for programming. Support ISP, IAP, ICP functions.

- The HC32F003 series supports 16K Byte Flash
- The HC32F005 series supports 32K Byte Flash

2K/4K Byte RAM

According to different power modes selected by customers, RAM data will be retained. With hardware parity bit, in case the data is accidentally damaged, when the data is read, the hardware circuit will immediately generate an interrupt to ensure the reliability of the system.

- The HC32F003 series supports 2K Byte RAM
- The HC32F005 series supports 4K Byte RAM

Clock system

A high-precision internal clock RCH with a configurable frequency of 4-24MHz. Under the configuration of 16MHz, the wake-up time from low power consumption mode to working mode is 4 μ s, and the frequency deviation within the full voltage and full temperature range is small, and it is not necessary to connect an expensive high-frequency crystal.

An external crystal oscillator XTH with a frequency of 8-32MHz.

An internal clock RCL with a frequency of 32.8/38.4kHz.

Operating mode

- 1) Active Mode: CPU running, peripheral function modules running.
- 2) Sleep Mode: The CPU stops running, and the peripheral function modules run.
- 3) Deep sleep mode: The CPU stops running, the high-speed clock stops running, and the low-power function modules run.

Port controller GPIO

It can provide up to 16 GPIO ports, some of which are multiplexed with analog ports. Each port is controlled by an independent control register bit. Supports edge-triggered interrupts and level-triggered interrupts, and can wake up the MCU to working mode from various power consumption modes. Support Push-Pull CMOS push-pull output, Open-Drain open-drain output. Built-in pull-up resistor, pull-down resistor, with Schmitt trigger input filter function. The output drive capability is configurable, and the maximum current drive capability is 12mA. 16 general-purpose IOs can support external asynchronous interrupts.

Interrupt Controller NVIC

The Cortex-M0+ processor has a built-in nested vectored interrupt controller (NVIC), which supports up to 32 interrupt request (IRQ) inputs; it has four interrupt priority levels, can handle complex logic, and can perform real-time control and interrupt processing.

The 32 interrupt entry vector addresses are:

Interrupt vector number	Interrupt source
[0]	GPIO_P0
[1]	GPIO_P1
[2]	GPIO_P2
[3]	GPIO_P3
[4]	-
[5]	-
[6]	UART0
[7]	UART1
[8]	-
[9]	-
[10]	SPI
[11]	-
[12]	I ² C
[13]	-
[14]	Timer0
[15]	Timer1
[16]	Timer2
[17]	-
[18]	Timer4
[19]	Timer5
[20]	Timer6
[21]	PCA
[22]	WDT
[23]	-
[24]	ADC
[25]	-
[26]	VC0
[27]	VC1
[28]	LVD
[29]	-
[30]	RAM FLASH fault
[31]	Clock trim

Reset controller RESET

This product has 7 reset signal sources, each reset signal can make the CPU run again, most of the registers will be reset, and the program counter PC will be reset to point to 00000000.

	Reset source
[0]	Power-on brown-out reset POR BOR
[1]	External Reset Pin reset
[2]	WDT reset
[3]	PCA reset
[4]	Cortex-M0+ LOCKUP hardware reset
[5]	Cortex-M0+ SYSRESETREQ software reset
[6]	LVD reset

Timer TIM

		Bit width	Prescaler	Counting direction	PWM	capture	Complementary output
Basic timer	Timer0	16/32	1/2/4/8/16/32/64/256	Up count	No	No	No
	Timer1	16/32	1/2/4/8/16/32/64/256	Up count	No	No	No
	Timer2	16/32	1/2/4/8/16/32/64/256	Up count	No	No	No
Programmable counting array	PCA	16	2/4/8/16/32	Up count	5	5	No
Advanced timer	Timer4	16	1/2/4/8/16/64/256/1024	Up count/ Count down/ Up and down count	2	2	1
	Timer5	16	1/2/4/8/16/64/256/1024	Up count/ Count down/ Up and down count	2	2	1
	Timer6	16	1/2/4/8/16/64/256/1024	Up count/ Count down/ Up and down count	2	2	1

The basic timer contains three timers Timer0/1/2. Timer0/1/2 have exactly the same function. Timer0/1/2 is a synchronous timer/counter, which can be used as a 16-bit timer/counter with automatic reloading function, or as a 32-bit timer/counter without reloading function. Timer0/1/2 can count external pulses or implement system timing.

PCA (Programmable Counter Array) supports up to 5 16-bit capture/compare modules. The timer/counter can be used as a common clock count/event counter capture/compare function. Each module of PCA can be independently programmed to provide input capture, output comparison or pulse width modulation. In addition, module 4 has an additional watchdog timer mode.

Timer4/5/6 which contains three timers. Timer4/5/6 are high-performance counters with the same function, which can be used to count and generate different forms of clock waveforms. One timer

can generate a complementary pair of PWM or independent 2- way PWM output, which can capture external input for pulse width or period Measurement.

The basic functions and characteristics of the advanced timer are shown in the table:

Waveform mode	Sawtooth wave, triangular wave
Basic functions	• Direction of increments and decrements
	• Software synchronization
	• Hardware synchronization
	• Cache function
	• Orthogonal coding count
	• General PWM output
	• Protection mechanism
	• AOS related actions
Interrupt type	Count comparison match interrupt
	Count cycle match interrupt
	Dead time error interrupt
	Short-circuit monitoring interrupt

Watchdog WDT

WDT (Watch Dog Timer) is a configurable 20-bit timer that provides reset in the case of MCU abnormality; built-in 10K low-speed clock input is used as the counter clock. In debug mode, you can choose to pause or continue to run; WDT can only be restarted by writing a specific sequence.

Universal synchronous asynchronous transceiver UART0~UART1

2- way Universal Asynchronous Receiver/Transmitter (Universal Asynchronous Receiver/Transmitter)

Basic functions of universal UART:

- Half-duplex and full-duplex transmission
- 8/9-Bit transmission data length
- Hardware parity
- 1 Bit stop bit
- Four different transmission modes
- Multi-machine communication
- Hardware address recognition

Serial Peripheral Interface SPI

synchronous serial interface (Serial Peripheral Interface), supporting master-slave mode.

Basic characteristics of SPI:

- Can be configured as master or slave through programming
- Four-wire transmission mode, full duplex communication
- Host mode 7 kinds of baud rate configurable
- The maximum frequency division factor of the host mode is PCLK/2, and the maximum communication rate is 16M bps
- The maximum frequency division factor of slave mode is PCLK/8, and the maximum communication rate is 4M bps
- Configurable serial clock polarity and phase
- Support interrupt
- 8-bit data transmission, first transmit high bit and then low bit

I²C bus

1 channel I²C, using serial synchronous clock, can realize data transmission between devices at different rates.

Basic characteristics of I2C:

- Support four working modes of master sending/receiving and slave sending/receiving
- Support standard (100Kbps) / fast (400Kbps) / high speed (1Mbps) three working rates
- Support 7-bit addressing function
- Support noise filtering function
- Support broadcast address
- Support interrupt status query function

Buzzer

Three basic timers function alternately output to provide a programmable drive frequency for the buzzer. The buzzer port can provide 12mA sink current, complementary output, no additional transistor is needed.

Clock calibration circuit module CLKTRIM

The built-in clock calibration circuit can calibrate the internal RC clock through an external precise crystal oscillator clock, and can also use the internal RC clock to check whether the external crystal oscillator clock is working properly.

Basic features of clock calibration:

- Calibration mode

- Monitoring mode
- 32-bit reference clock counter can be loaded with initial value
- 32-bit clock counter to be calibrated with configurable overflow value
- 6 reference clock sources
- 4 clock sources to be calibrated
- Support interrupt mode

Device electronic signature

Each chip has a unique 10-byte device identification number before leaving the factory, including wafer lot information and chip coordinate information. ID address 0x0010_0E74-0x0010_0E7F

Cyclic Redundancy Check (CRC)

Complies with the polynomial $F(x) = X^{16} + X^{12} + X^5 + 1$ given in ISO/IEC13239.

Analog-to-digital converter ADC

A 12-bit successive approximation analog-to-digital converter with monotonous and no missing codes, when working under a 24MHz ADC clock, the sampling rate reaches 1Msps. The reference voltage can be selected from the on-chip precision voltage (1.5V or 2.5V) or from an external input or power supply voltage. 11 input channels, including 9 external pin inputs, 1 internal temperature sensor voltage and 1 1/3 supply voltage. Built-in configurable input signal amplifier to detect weak signals.

Basic characteristics of SAR ADC:

- 12-bit conversion accuracy;
- 1Msps conversion speed;
- 11 input channels, including 9 external pin inputs, 1 internal temperature sensor voltage and 1 VCC/3 voltage;
- 4 reference sources: VCC voltage, ExRef pin, built-in 1.5V reference voltage, built-in 2.5V reference voltage;
- ADC voltage input range: 0~Vref;
- 3 conversion modes: single conversion, sequential scan continuous conversion, continuous conversion accumulation;
- Input channel voltage threshold monitoring;
- Software can configure ADC conversion rate;
- Built-in signal amplifier, can convert high impedance signal;

- Support on-chip peripherals to automatically trigger ADC conversion, effectively reducing chip power consumption and improving real-time conversion.

Analog Voltage Comparator VC

Chip pin voltage monitoring / comparison circuit. 8 configurable positive/negative external input channels; 4 internal input channels, including 1 internal temperature sensor voltage, 1 built-in BGR 2.5V reference voltage, 1 64-order resistor Partial pressure. VC output can be used for basic timer, advanced timer and programmable count array PCA capture, gating, external count clock. An asynchronous interrupt can be generated according to the rising/falling edge to wake up the MCU from the low-power mode. Configurable software anti-shake function.

Low voltage detector LVD

Detect the chip power supply voltage or chip pin voltage. 16-shift voltage monitoring values (1.8 - 3.3V). An asynchronous interrupt or reset can be generated based on the rising/falling edge. With hardware hysteresis circuit and configurable software anti-shake function.

LVD basic characteristics:

- 4 -channel monitoring sources, VCC, PC13, PB08, PB07;
- 16-stage threshold voltage, 1.8-3.3V optional;
- 8 trigger conditions, combinations of high level, rising edge and falling edge;
- 2 trigger results, reset and interrupt;
- 8-stage filter configuration to prevent false triggering;
- With hysteresis function, strong anti-interference.

Embedded debugging system

Embedded debugging solution, providing a full-featured real-time debugger, with standard mature Keil/IAR and other debugging and development software. Support 4 hard breakpoints and multiple soft breakpoints.

Programming mode

Support one programming mode: offline programming.

Support two programming protocols: ISP protocol, SWD protocol.

ISP protocol programming interface: P35, P36 or P27, P31.

SWD protocol programming interface: P27, P31.

When the chip receives the ISP programming command within a few milliseconds time window after the reset is completed, the chip works in the ISP programming mode, and the programmer can be used to program the FLASH.

When the chip does not receive the ISP programming instruction within a few milliseconds time window after the reset is completed, the chip works in the user mode, and the chip executes the program code in the FLASH.

Note:

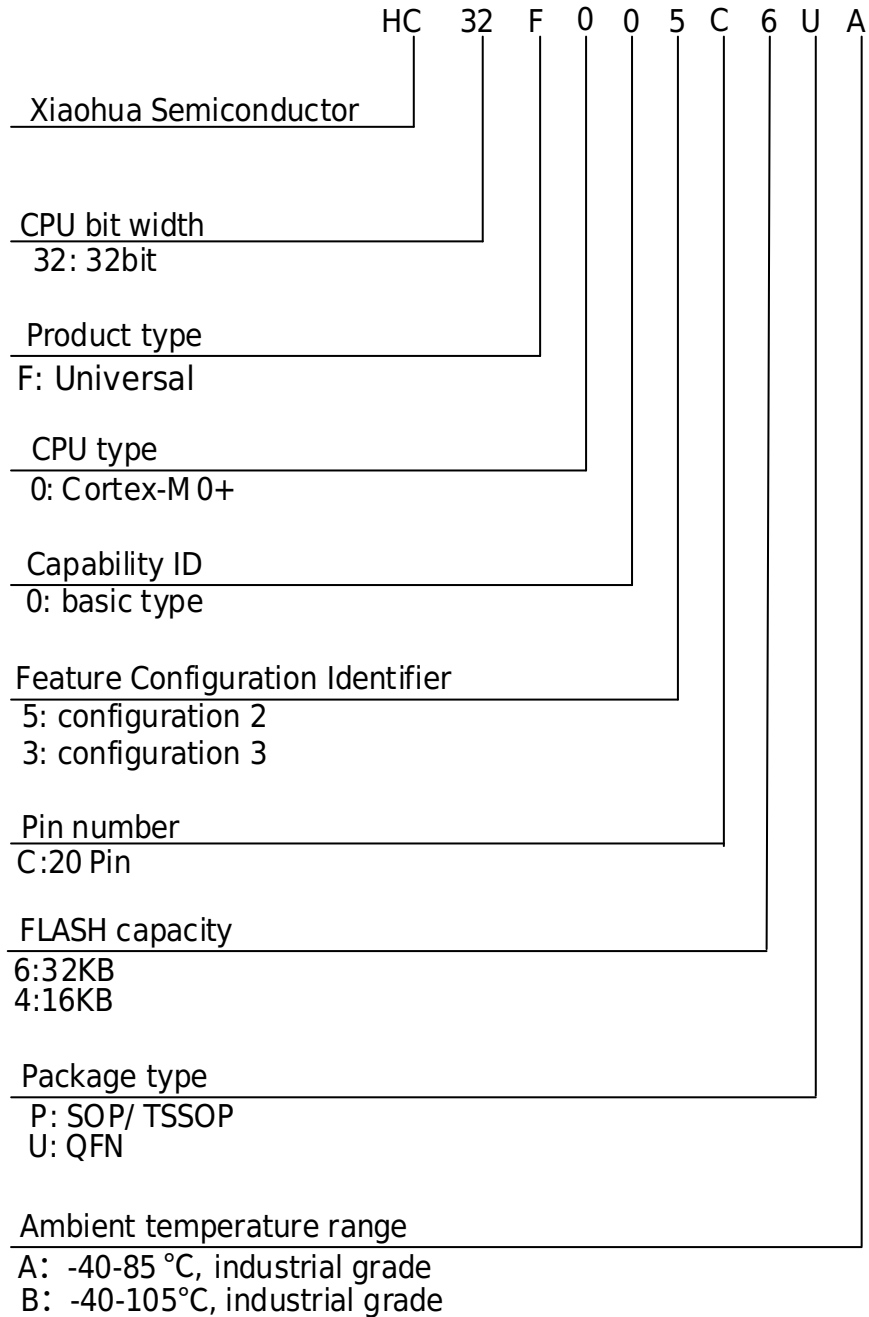
- It is recommended to reserve P35 and P36 as the ISP programming interface; if you need to use P27 and P31 as the ISP programming interface, please refer to PCN: PCN20200304-1_HC32L110HC32F003HC32F005 to increase the programming speed.

High security

Encrypted embedded debugging solution, providing a full-featured real-time debugger.

2 Product lineup

2.1 Product name

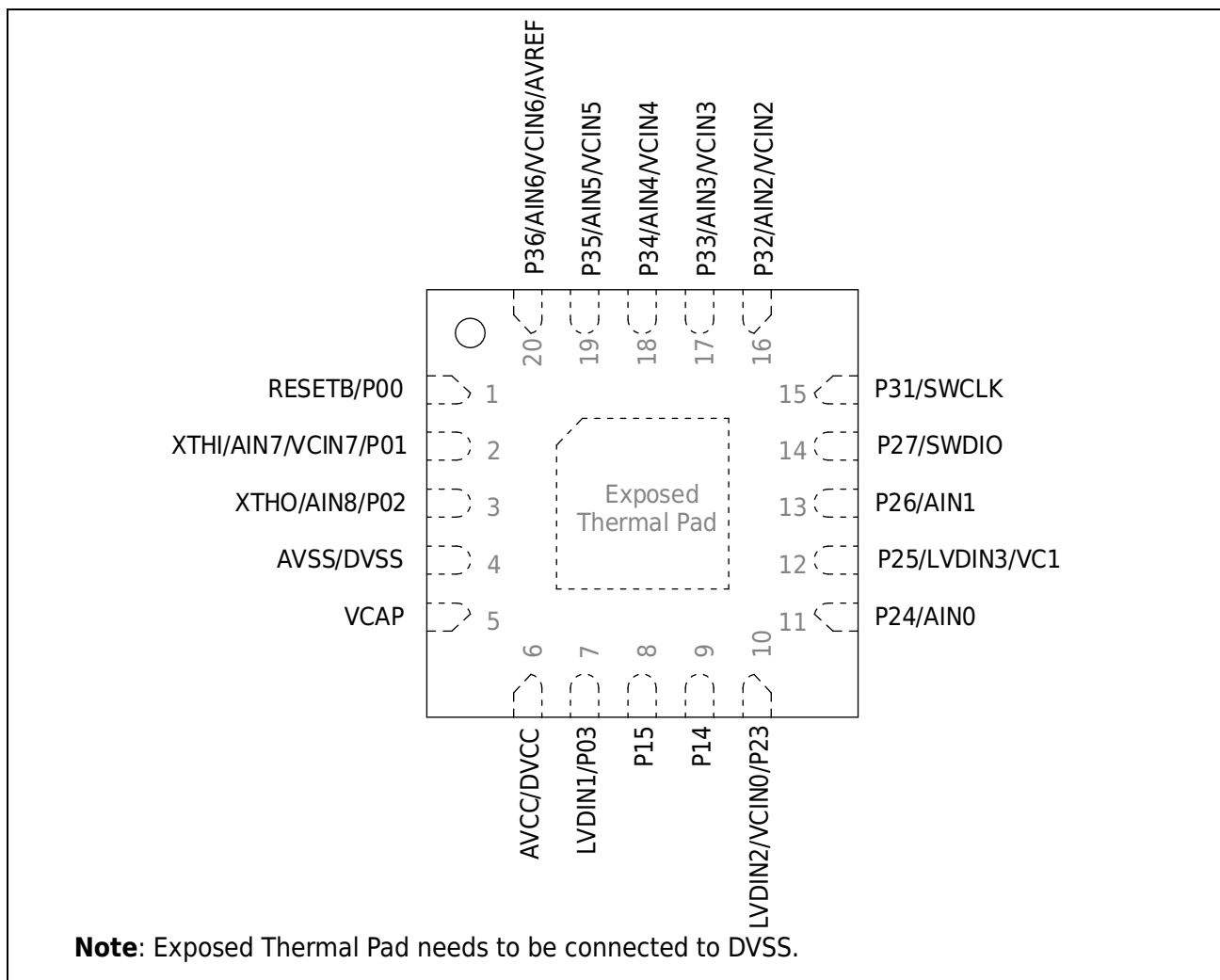


2.2 Function

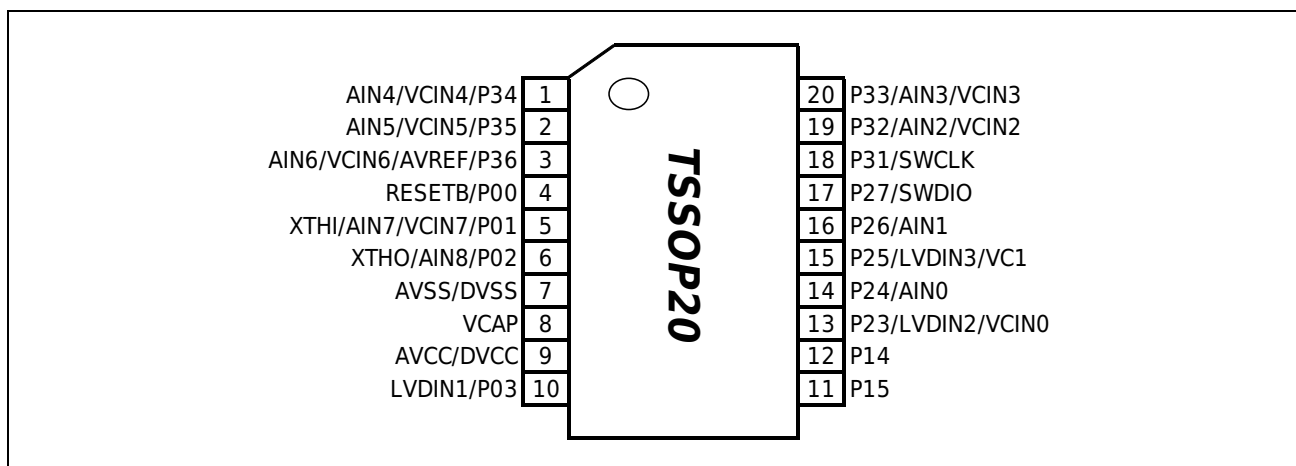
Product name		HC32F005C6UA HC32F005C6PA HC32F003C4UA HC32F003C4PA	HC32F005C6PB HC32F003C4PB
Pin number		20	
GPIO pin number		16	
CPU	Kernel	Cortex M0+	
	Frequency	32MHz	
Supply voltage range		1.8 ~5.5V	
Single / dual power supply		Single power supply	
Temperature range		-40 ~ 85℃	-40 ~ 105℃
Debug function		SWD debug interface	
Unique identification code		Support	
Communication Interface		UART0/1 SPI I ² C	
Timer		General-purpose timer TIM0/1/2 Advanced timer TIM4/5/6	
Liquid crystal Controller (LCDC)		no	
12-bit A/D converter		9ch	
Analog voltage comparator		VC0/1	
Port interrupt		16	
Low voltage detection reset / interrupt		1	
Clock	Internal high-speed oscillator	RCH 4/8/16/22.12/24MHz	
	Internal low-speed oscillator	RCL 32.8/38.4KHz	
	External high-speed crystal oscillator	8~32MHz	
Buzzer		Max 3ch	
FLASH security protection		Support	
RAM parity		Support	

3 Pin configuration

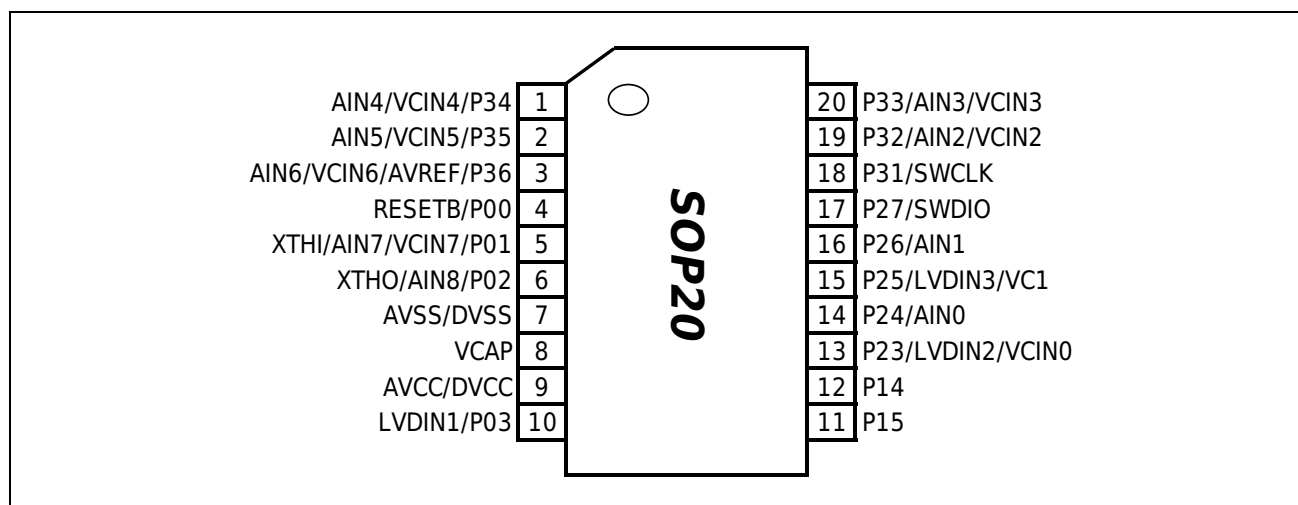
HC32F005C6UA / HC32F003C4UA



HC32F005C6PA / HC32F003C4PA / HC32F005C6PB / HC32F003C4PB



HC32F005C6PA / HC32F003C4PA



4 Pin function description

Pin No. QFN20	Pin No. TSSOP20	Pin No. SOP20	Pin Name	Pin Type	Description
1	4	4	RESETB P00	RESETB GPIO	Reset input port, low effective, chip reset P00 digital input
2	5	5	P01	GPIO UART0_RXD I ² C_SDA UART1_TXD TIM0_TOG TIM5_CHB SPI_SCK TIM2_EXT AIN7/VC7 XTHI	P01 General purpose digital input / output pin UART0 RXD I ² C data UART1 TXD Timer0 flip output Timer5 capture input / comparison output B SPI clock Timer2 external clock Analog input External XTH crystal clock enter
3	6	6	P02	GPIO UART0_TXD I ² C_SCL UART1_RXD TIM0_TOGN TIM6_CHA SPI_CS TIM2_GATE AIN8 XTHO	P02 General purpose digital input / output pin UART0 TXD I ² C Clock UART1 RXD Timer0 flips the inverted output Timer6 capture input / comparison output A SPI CS Timer2 Gating Analog input External XTH crystal clock output
4	7	7	DVSS	GND	Chip ground
5	8	8	VCAP	Power	LDO core power supply output (only for internal circuit use, connect a 4.7uF capacitor)
6	9	9	DVCC	Power	Chip power supply 1.8~5.5v
				/	/
				/	/
7	10	10	P03	GPIO PCA_CH3 SPI_CS TIM6_CHB PCA_ECI VC0_OUT	P03 General purpose digital input / output pin PCA capture input / comparison output 3 SPI CS Timer6 capture input / comparison output B PCA external clock input VC0 output

Pin No.	Pin No.	Pin No.	Pin Name	Pin Type	Description
QFN20	TSSOP20	SOP20			
				LVDIN1	Analog input
8	11	11	P15	GPIO	P15 General purpose digital input / output pin
				I ² C_SDA	I ² C data
				TIM2_TOG	Timer2 toggle output
				TIM4_CHB	Timer4 capture input / compare output B
				SPI_SCK	SPI clock
				UART0_RXD	UART0 RXD
				LVD_OUT	LVD Output
9	12	12	P14	GPIO	P14 General purpose digital input / output pin
				I ² C_SCL	I ² C Clock
				TIM2_TOGN	Timer2 flips the inverted output
				ECI	PCA external clock input
				ADC_RDY	ADC ready
				SPI_CS	SPI CS
				UART0_TXD	UART0 TXD
10	13	13	P23	GPIO	P23 General purpose digital input / output pin
				TIM6_CHA	Timer6 capture input / comparison output A
				TIM4_CHB	Timer4 capture input / compare output B
				TIM4_CHA	Timer4 capture input / comparison output A
				PCA_CH0	PCA capture input / comparison output 0
				SPI_MISO	SPI module host input and slave output data signal
				UART1_TXD	UART1 TXD
				IR_OUT	38K carrier output
				LVDIN2/VC0	Analog input
11	14	14	P24	GPIO	P24 General purpose digital input / output pin
				TIM4_CHB	Timer4 capture input / compare output B
				TIM5_CHB	Timer5 capture input / comparison output B
				HCLK_OUT	HCLK Output
				PCA_CH1	PCA capture input / comparison output 1
				SPI_MOSI	SPI module master output slave input data signal
				UART1_RXD	UART1 RXD
				VC1_OUT	VC1 output
				AIN0	Analog input
12	15	15	P25	GPIO	P25 General purpose digital input / output pin

Pin No.	Pin No.	Pin No.	Pin Name	Pin Type	Description
QFN20	TSSOP20	SOP20			
				SPI_SCK	SPI clock
				PCA_CH0	PCA capture input / comparison output 0
				TIM5_CHA	Timer5 capture input / comparison output A
				LVD_OUT	LVD Output
				I ² C_SDA	I ² C data
				TIM1_GATE	Timer1 Gating
				LVDIN3/VC1	Analog input
13	16	16	P26	GPIO	P26 General purpose digital input / output pin
				SPI_MOSI	SPI module master output slave input data signal
				TIM4_CHA	Timer4 capture input / comparison output A
				TIM5_CHB	Timer5 capture input / comparison output B
				PCA_CH2	PCA capture input / comparison output 2
				I ² C_SCL	I ² C Clock
				TIM1_EXT	Timer1 clock input
14	17	17	P27	AIN1	Analog input
				GPIO	P27 General purpose digital input / output pin
				SPI_MISO	SPI module host input and slave output data signal
				TIM5_CHA	Timer5 capture input / comparison output A
				TIM6_CHA	Timer6 capture input / comparison output A
				PCA_CH3	PCA capture input / comparison output 3
				UART0_RXD	UART0 RXD
				RCH_OUT	RCH oscillation output
				XTH_OUT	XTH oscillation output
15	18	18	P31	SWDIO	SWDIO
				GPIO	P31 General purpose digital input / output pin
				PCA_ECI	PCA external clock
				PCLK_OUT	PCLK Output
				VC0OUT	VC0 output
				UART0_TXD	UART0 TXD
				RCL_OUT	RCL oscillator output
				HCLK_OUT	HCLK Output
				SWCLK	SWCLK
				/	/
				/	/
				/	/
16	19	19	P32	GPIO	P32 General purpose digital input / output pin

Pin No.	Pin No.	Pin No.	Pin Name	Pin Type	Description
QFN20	TSSOP20	SOP20			
				PCA_CH2	PCA capture input / comparison output 2
				TIM6_CHB	Timer6 capture input/compare output B
				VC1OUT	VC1 output
				UART1_TXD	UART1 TXD
				PCA_CH4	PCA capture input / comparison output 4
				AIN2/VC2	Analog input
17	20	20	P33	GPIO	P33 General purpose digital input / output pin
				PCA_CH1	PCA capture input / comparison output 1
				TIM5_CHB	Timer5 capture input / comparison output B
				PCA_ECI	PCA external clock
				UART1_RXD	UART1 RXD
				TIM1_TOGN	Timer1 flips reverse output
18	1	1	P34	AIN3/VC3	Analog input
				GPIO	P34 General purpose digital input / output pin
				PCA_CH0	PCA capture input / comparison output 0
				TIM5_CHA	Timer5 capture input / comparison output A
				TIM0_EXT	Timer0 clock input
				TIM4_CHA	Timer4 capture input / comparison output A
19	2	2	P35	TIM1_TOG	Timer1 toggle output
				AIN4/VC4	Analog input
				GPIO	P35 General purpose digital input / output pin
				UART1_TXD	UART1 TXD
				TIM6_CHB	Timer6 capture input/compare output B
				UART0_TXD	UART0 TXD
20	3	3	P36	TIM0_GATE	Timer0 Gating
				TIM4_CHB	Timer4 capture input / compare output B
				SPI_MISO	SPI module host input and slave output data signal
				I ² C_SDA	I ² C data
				AIN5/VC5	Analog input
				GPIO	P36 General purpose digital input / output pin
				UART1_RXD	UART1 RXD
				TIM6_CHA	Timer6 capture input / comparison output A
				UART0_RXD	UART0 RXD
				PCA_CH4	PCA capture input / comparison output 4
				TIM5_CHA	Timer5 capture input / comparison output A

Pin No.	Pin No.	Pin No.	Pin Name	Pin Type	Description
QFN20	TSSOP20	SOP20			
				SPI_MOSI	SPI module master output slave input data signal
				I ² C_SCL	I ² C Clock
				AIN6/VC6/ AVREF	Analog input

5 Block diagram

Functional module

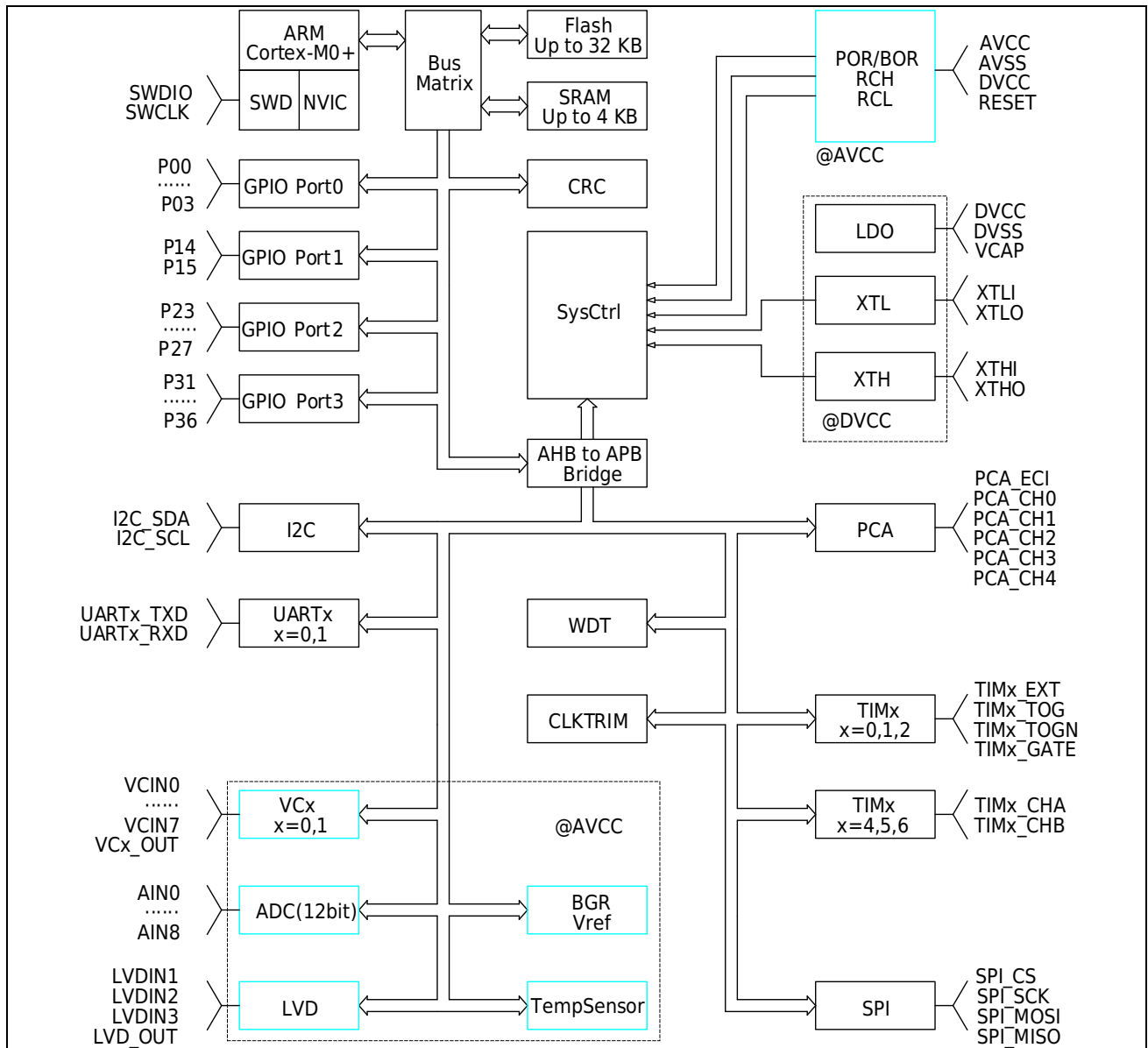
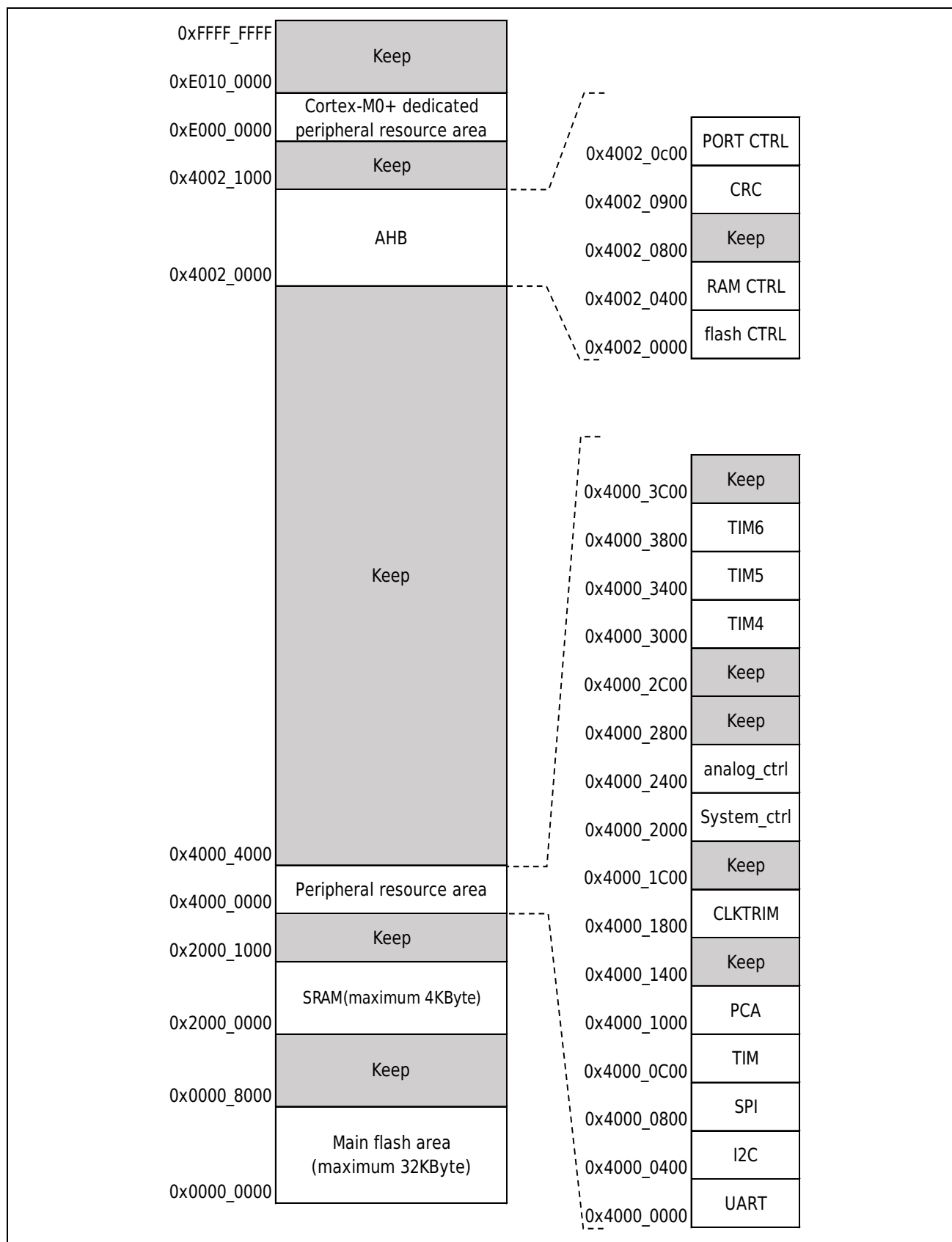
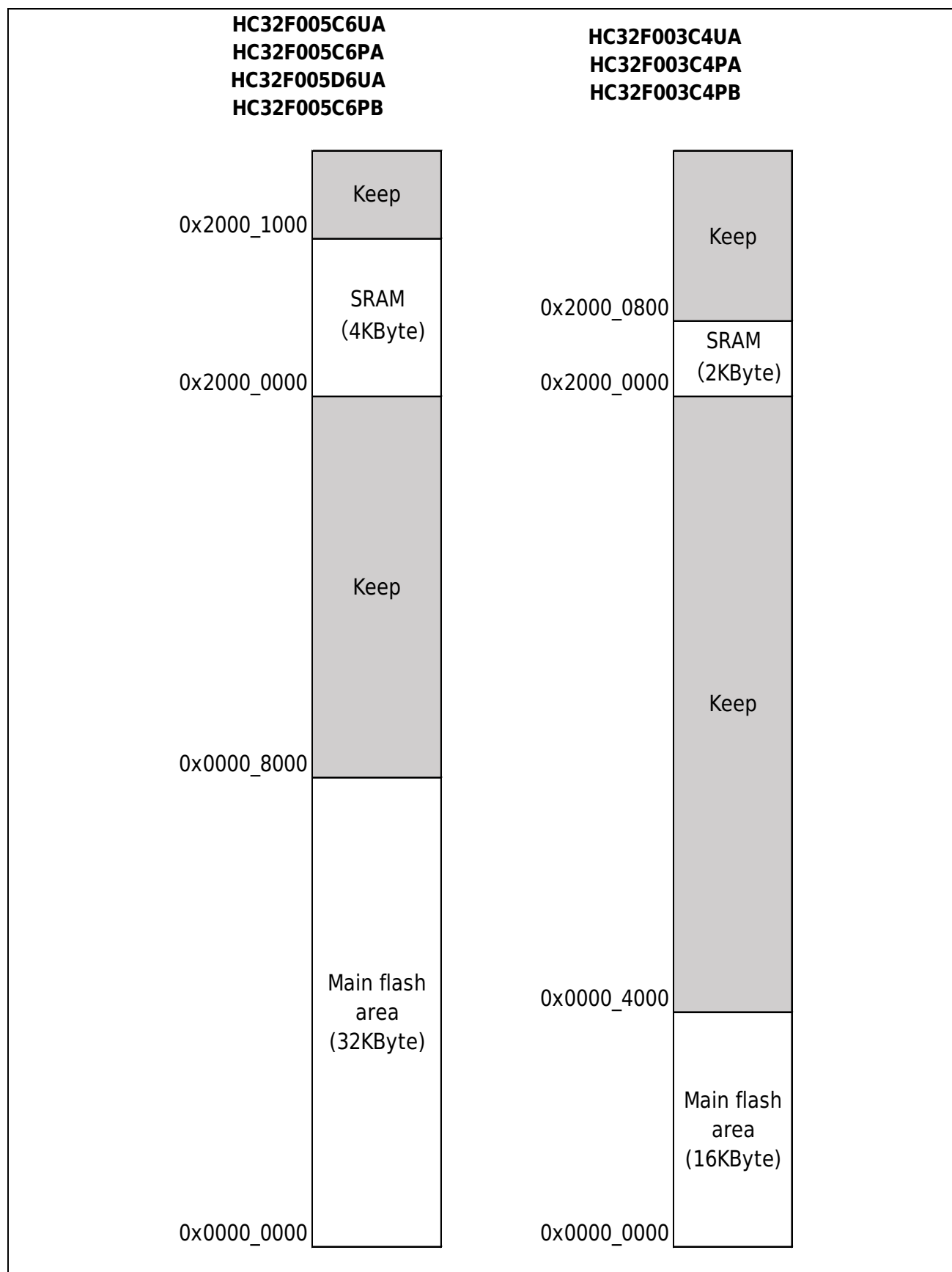


Figure 5-1 Functional modules

6 Storage area map





7 Electrical characteristics

7.1 Test Conditions

All voltages are referenced to VSS unless otherwise noted.

7.1.1 Minimum and maximum values

Unless otherwise specified, all minimum and maximum values will be in the worst environment through the test performed on 100% of the products in the production line at ambient temperature $T_A=25^{\circ}\text{C}$ and $T_A=T_{\text{Amax}}$ (T_{Amax} matches the selected temperature range) Guaranteed over temperature, supply voltage, and clock frequency.

The notes at the bottom of each table indicate data obtained through comprehensive evaluation, design simulation and/or process characteristics, and will not be tested on the production line; on the basis of comprehensive evaluation, the minimum and maximum values are after sample testing. Take the average value and add or subtract three times the standard distribution (mean $\pm 3\sigma$).

7.1.2 Typical value

Unless otherwise specified, typical data is based on $T_A=25^{\circ}\text{C}$ and $V_{CC}=3.3\text{V}$ ($1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$ voltage range). These data are only used for design guidance and not tested.

The typical ADC accuracy value is obtained by sampling a standard batch and testing under all temperature ranges. The error of 95% of the products is less than or equal to the given value (average $\pm 2\sigma$).

7.2 Absolute maximum ratings

If the load on the device exceeds the value given in the "Absolute Maximum Ratings" list, it may cause permanent damage to the device. This only gives the maximum load that can be withstood, and does not mean that the functional operation of the device under this condition is correct. Long-term operation of the device under the maximum condition will affect the reliability of the device.

Table 7-1 Voltage and Current Characteristics

Symbol	Description	Minimum Value	Maximum Value	Unit
VCC - VSS	External main supply voltage (includes AVCC and DVCC) ⁽¹⁾	-0.3	5.5	V
V _{IN}	Input voltage on other pins ⁽²⁾	VSS-0.3	VCC + 0.3	V
ΔVCC _x	Voltage difference between different power supply pins		50	mV
VSS _x - VSS	Voltage difference between different ground pins		50	mV
V _{ESD} (HBM)	ESD electrostatic discharge voltage (human body model)	Refer to absolute maximum electrical parameters		V
I _{VCC}	The total current (supply current) through the DVCC/AVCC power cord ⁽¹⁾		300	mA
I _{VSS}	The total current through the VSS ground wire (outflow current) ⁽¹⁾		300	mA
I _{IO}	Output sink current on any I/O and control pin		25	mA
	Output current on any I/O and control pin		-25	mA
I _{INJ(PIN)} ⁽²⁾⁽³⁾	Injection current of RESETB pin		+/-5	mA
	Injection current of XTHI pin of XTH and XTLL pin of XTL		+/-5	mA
	Injection current of other pins ⁽⁴⁾		+/-5	mA
ΣI _{INJ(PIN)} ⁽²⁾	Total injection current on all I/O and control pins ⁽⁴⁾		+/-25	mA

1. All power (DVCC, AVCC) and ground (DVSS, AVSS) pins must always be connected to an external power supply within the allowable range.
2. I_{INJ(PIN)} must not exceed its limit, which means that V_{IN} does not exceed its maximum value. If it cannot be guaranteed that V_{IN} does not exceed its maximum value, it is also necessary to ensure that the external limit I_{INJ(PIN)} does not exceed its maximum value. When V_{IN}>V_{CC}, there is a forward injection current; when V_{IN}<V_{SS}, there is a reverse injection current.
3. The reverse injection current will interfere with the analog performance of the device.
4. When several I/O ports have injection current at the same time, the maximum value of ΣI_{INJ(PIN)} is the sum of the instantaneous absolute value of the forward injection current and the reverse injection current. This result is based on the characteristics of the maximum ΣI_{INJ(PIN)} on the 4 I/O ports of the device.

Table 7-2 temperature characteristics

Symbol	Description	Numerical Value	Unit
T _{STG}	Storage temperature range	-65 ~ + 150	°C
T _{Jmax}	Maximum junction temperature	105	°C

7.3 Operating conditions

7.3.1 General working conditions

Table 7-3 General Operating Conditions

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
f _{HCLK}	Internal AHB clock frequency		0	32	MHz
f _{PCLK}	Internal APB clock frequency		0	32	MHz
DVCC	Working voltage of digital part		1.8	5.5	V
AVCC ⁽¹⁾	Analog part working voltage	Must be the same as DVCC ⁽²⁾	1.8	5.5	V
T _A	Ambient temperature	Maximum power consumption	-40	85	°C
		Low power consumption	-40	105	°C
T _J	Junction temperature range		-40	105	°C

1. When using an ADC, see ADC Electrical Specifications.
2. It is recommended to use the same power supply for DVCC and AVCC, allowing a maximum of 300mV difference between DVCC and AVCC during power-up and normal operation.
3. In a state of lower power consumption, as long as T_J does not exceed T_{Jmax}, T_A can be extended to this range.

7.3.2 Working conditions at power-up and power-down

Table 7-4 Power-up and power-down operating conditions

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t _{VCC}	VCC rising rate		0	5	V/μs
t _{VCC}	VCC falling rate		0	5	V/μs

7.3.3 Embedded reset and LVD module features

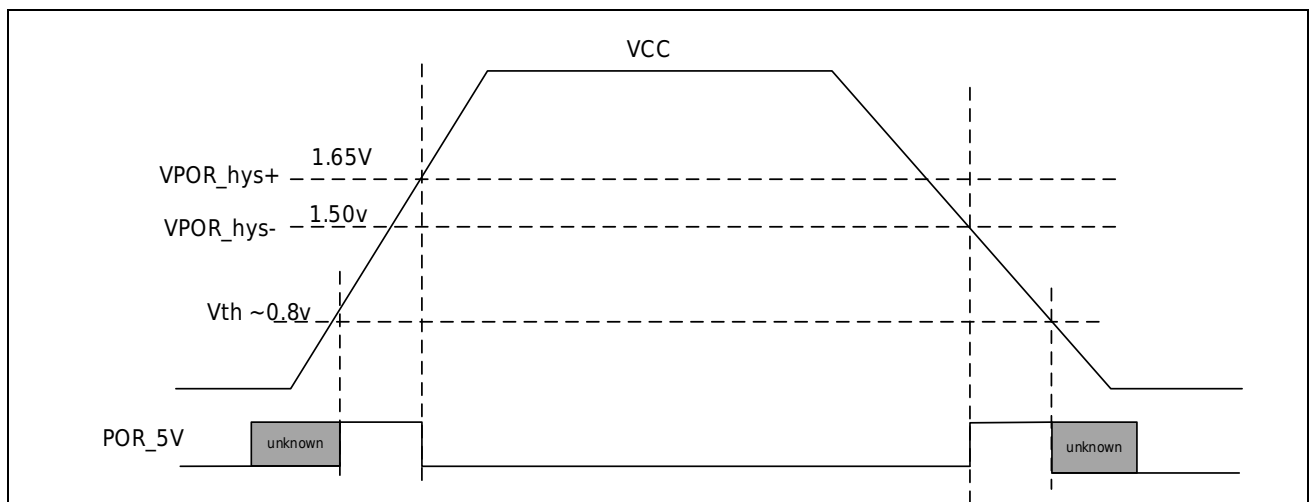


Figure 7-1 POR/Brown Out Diagram

1. Guaranteed by design, not tested in production.

Table 7-5 POR/Brown Out

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Vpor	POR release voltage (power-on process) BOR detection voltage (power-down process)		1.45	1.50	1.65	V

Table 7-6 LVD module characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Vex	External input voltage range		0		VCC	V
Vlevel	Detection threshold	LVD_CR.VTDS=0000 LVD_CR.VTDS =0001 LVD_CR.VTDS =0010 LVD_CR.VTDS =0011 LVD_CR.VTDS =0100 LVD_CR.VTDS=0101 LVD_CR.VTDS=0110 LVD_CR.VTDS=0111 LVD_CR.VTDS=1000 LVD_CR.VTDS=1001 LVD_CR.VTDS=1010 LVD_CR.VTDS=1011 LVD_CR.VTDS=1100 LVD_CR.VTDS=1101 LVD_CR.VTDS=1110 LVD_CR.VTDS=1111		1.8 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2 3.3		V
Icomp	Power consumption			0.12		μA
Tresponse	Response time			80		μs
Tsetup	Establishment time			400		μs
Vhyste	Hysteresis voltage			40		mV
Tfilter	Filter time	LVD_debounce = 000 LVD_debounce = 001 LVD_debounce = 010 LVD_debounce = 011 LVD_debounce = 100 LVD_debounce = 101 LVD_debounce = 110 LVD_debounce = 111		7 14 28 112 450 1800 7200 28800		μs

7.3.4 Built-in reference voltage

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V _{REF25}	Internal 2.5V Reference Voltage	Room temperature 25°C 3.3V	2.475	2.5	2.525	V
		-40~85°C 2.8~5.5V	2.438	2.5	2.563	V ^[1]
		-40~105°C 2.8~5.5V	2.431	2.5	2.525	V ^[1]
V _{REF15}	Internal 1.5V Reference Voltage	Room temperature 25°C 3.3V	1.485	1.5	1.515	V
		-40~85°C 1.8~5.5V	1.463	1.5	1.538	V ^[1]
		-40~105°C 1.8~5.5V	1.477	1.5	1.519	V ^[1]
T _{Coeff}	Internal 2.5V 1.5V temperature coefficient	-40~85°C			120	ppm/°C
		-40~105°C			190	ppm/°C

1. The data is based on the assessment results and is not tested in production.

7.3.5 Operating Current Characteristics

Current consumption is a comprehensive index of multiple parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin flip rate, and program in memory. The location in and executed code, etc.

The microcontroller is in the following conditions:

- All I/O pins are in input mode and connected to a static level-VCC or VSS (no load).
- All peripherals are turned off, unless otherwise specified.
- The access time of the flash memory is adjusted to the frequency of f_{HCLK} (0 wait cycle for 0~24MHz, 1 wait cycle for 24~48MHz).
- When the peripheral is turned on: $f_{PCLK} = f_{HCLK}$.

Table 7-7 Operating Current Characteristics

Symbol	Parameter	Conditions			Typ ⁽¹⁾	Max ⁽²⁾	Max ⁽³⁾	Unit
I_{DD} (Run in RAM)	All peripherals clock OFF, Run While(1) in RAM.	$V_{CAP}=1.55V$ $V_{DD}=3.3V$	RCH clock source	4M	220			μA
				8M	400			
				16M	740			
				24M	1080			
I_{DD} (Run CoreMark)	All peripherals clock OFF, Run CoreMark in Flash.	$V_{CAP}=1.55V$ $V_{DD}=3.3V$	RCH clock source	4M	670			μA
				8M	1300			
				16M	2380			
				24M	3410			
I_{DD} (Run mode)	All peripherals clock ON, Run while(1) in Flash	$V_{CAP}=1.55V$ $V_{DD}=1.8-5.5V$	RCH clock source	4M	700	970	980	μA
				8M	1350	1770	1790	
				16M	2500	3310	3330	
				24M	3600	4740	4770	
	All peripheral clock OFF, Run while(1) in Flash	$V_{CAP}=1.55V$ $V_{DD}=1.8-5.5V$	RCH clock source	4M	550	830	840	
				8M	1050	1440	1460	
				16M	1900	2650	2660	
				24M	2700	3640	3730	
I_{DD} (Sleep mode)	All peripheral clock ON	$V_{CAP}=1.55V$ $V_{DD}=1.8-5.5V$	RCH clock source	4M	260	310	320	μA
				8M	500	580	590	
				16M	950	1070	1090	
				24M	1400	1570	1620	
	All peripheral clock OFF	$V_{CAP}=1.55V$ $V_{DD}=1.8-5.5V$	RCH clock source	4M	110	140	150	
				8M	190	240	250	
				16M	330	400	410	
				24M	470	560	580	

Symbol	Parameter	Conditions	Typ ⁽¹⁾	Max ⁽²⁾	Max ⁽³⁾	Unit
I _{DD} (DeepSleep mode)	All peripherals clock OFF except WDT	V _{CAP} =1.55V V _{DD} =1.8-5.5V	TA = -40~25°C	1.32	1.5	
			TA = 50°C	1.65	2.0	
			TA = 85°C	3.41	4.1	
			TA = 105°C	5.12	5.8	
	All peripherals clock OFF	V _{CAP} =1.55V V _{DD} =1.8-5.5V	TA = -40~25°C	0.46	0.7	
			TA = 50°C	0.83	1.1	
			TA = 85°C	2.42	3.0	
			TA = 105°C	4.13	5.0	

1. If there are no other specified conditions, the value of this Typ was measured at 25 °C & V_{CC} = 3.3V.
2. If there are no other specified conditions, the value of this Max is the maximum within the range of V_{CC} = 1.8-5.5 & Temperature = N40-85 °C.
3. If there are no other specified conditions, the value of this Max is the maximum within the range of V_{CC} = 1.8-5.5 & Temperature = N40-105 °C.
4. The data is based on the assessment results and is not tested in production.

7.3.6 Time to wake up from low power mode

The wake-up time is measured during the wake-up phase of the RCH oscillator. The clock source used when waking up depends on the current operating mode:

- Sleep mode: clock source is RCH oscillator
- RCH oscillator when entering deep sleep

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T _{wu}	Sleep mode wake-up time			1.8		μs
	Deep sleep wake-up time	F _{MCLK} = 4MHz		9.0		μs
		F _{MCLK} = 8MHz		6.0		μs
		F _{MCLK} = 16MHz		5.0		μs
		F _{MCLK} = 24MHz		4.0		μs

1. The wake-up time is measured from the start of the wake-up event to the user program reading the first instruction.

7.3.7 External timer characteristic

External input high-speed clock

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
f _{XTH_ext}	User external clock frequency ⁽¹⁾		0	8	32	MHz
V _{XTHH}	Input pin high level voltage		0.7VCC		VCC	V
V _{XTHL}	Input pin low voltage		VSS		0.3VCC	V
T _{r(XTH)}	Rise time ⁽¹⁾				20	ns
T _{f(XTH)}	Falling time ⁽¹⁾				20	ns
T _{w(XTH)}	Enter high or low time ⁽¹⁾		16			ns
C _{in(XTH)}	Input capacitive reactance ⁽¹⁾			5		pF
Duty	Duty ratio		40		60	%
I _L	Input leakage current				±1	μA

1. Guaranteed by design, not tested in production.

High-speed external clock XTH

The high-speed external clock (XTH) can be generated using a 8-32MHz crystal/ceramic resonator oscillator. The information given in this section is based on the results obtained through comprehensive characteristic evaluation using the typical external components listed in the table below. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and settling time at startup. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
F _{CLK}	Oscillation frequency	-	8	-	32	MHz
ESR _{CLK}	Supported crystal oscillator range	32MHz	-	-	60	Ω
		24MHz	-	-	80	
		16MHz	-	-	100	
		8MHz	-	-	120	
C _{LX} ⁽³⁾	Matching capacitance	Configure as required by the crystal manufacturer.	4	12	20	pF
Duty	Duty ratio	-	40	50	60	%
I _{dd} ⁽⁴⁾	Current	XTH_CR[3:0]=0b1111	-	1000	-	μA
		XTH_CR[3:0]=0b1110	-	600	-	
		XTH_CR[3:0]=0b1010	-	370	-	
		XTH_CR[3:0]=0b0110	-	300	-	
		XTH_CR[3:0]=0b0010	-	160	-	
g _m	transconductance	XTH_CR[3:0]=0b1111	-	11.75	-	mA/V

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
		XTH_CR[3:0]=0b1110 (32MHz, 24MHz recommended value)	-	6.34	-	
		XTH_CR[3:0]=0b1101	-	4.38	-	
		XTH_CR[3:0]=0b1100	-	3.38	-	
		XTH_CR[3:0]=0b1011	-	7.41	-	
		XTH_CR[3:0]=0b1010 (16MHz recommended value)	-	4.01	-	
		XTH_CR[3:0]=0b1001	-	2.77	-	
		XTH_CR[3:0]=0b1000	-	2.14	-	
		XTH_CR[3:0]=0b0111	-	5.59	-	
		XTH_CR[3:0]=0b0110 (12MHz recommended value)	-	3.01	-	
		XTH_CR[3:0]=0b0101	-	2.08	-	
		XTH_CR[3:0]=0b0100	-	1.60	-	
		XTH_CR[3:0]=0b0011	-	2.50	-	
		XTH_CR[3:0]=0b0010 (8MHz recommended value)	-	1.30	-	
		XTH_CR[3:0]=0b0001	-	0.93	-	
		XTH_CR[3:0]=0b0000	-	0.72	-	
T _{start} ⁽⁵⁾	Start time	32MHz, CL=16pF @ XTH_CR[3:0]=0b1110	-	500	-	μs
		8MHz, CL=16pF @ XTH_CR[3:0]=0b0010	-	2	-	ms

1. The characteristic parameters of the resonator are provided by the crystal/ceramic resonator manufacturer.
2. According to comprehensive evaluation, it is not tested in production.
3. CL_x refers to the two pin matching capacitors CL₁ and CL₂ of the crystal. It is recommended to use high-quality ceramic capacitors, and select a crystal or resonator that meets the requirements. Usually CL₁ and CL₂ have the same parameters. When selecting CL_x, one should take into account parameters such as the crystal oscillator's frequency and ESR, as well as the total parasitic capacitance to ground (C_P) from the PCB and MCU pins.

The CL_x is recommended to be configured in accordance with the requirements of the crystal manufacturer's technical manual.

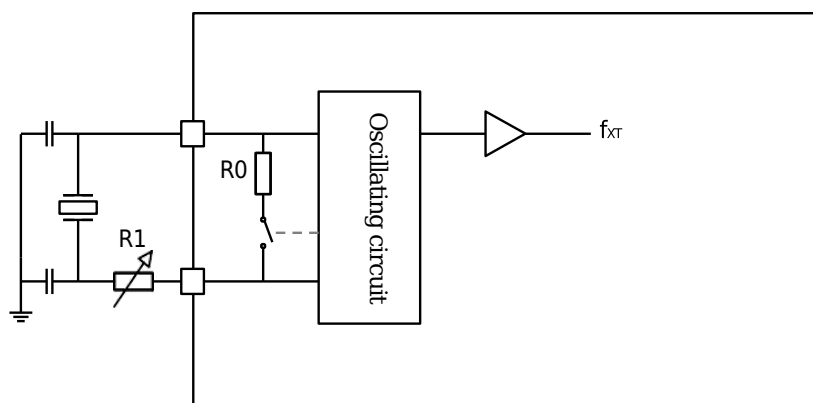
- If the crystal manufacturer gives the value of the load capacitance (CL), the matching capacitance $CL_x = 2 * CL - C_P$.

- If the crystal manufacturer gives *the value of the matching capacitance*, the matching capacitance $C_{Lx} = \text{matching capacitance value} - C_p$.

In practical applications, if a larger C_{Lx} is selected, it is recommended to choose an appropriate current level setting.

Example:

- When the crystal manufacturer gives the load capacitance of the crystal as 8pF, considering the distributed capacitance between the PCB and MCU pins, it is recommended to choose a matching capacitor with a capacitance of 12pF.
 - When the crystal manufacturer gives the matching capacitance of the crystal as 12pF, considering the distributed capacitance between the PCB and MCU pins, it is recommended to choose a matching capacitor with a capacitance of 10pF or 8pF.
4. The current varies with the choice of frequency and driving capability. The higher the frequency, the stronger the driving ability, and the greater the current consumption..
 5. T_{start} is the startup time, which is measured from the software enabling XTH until a stable oscillation of 32MHz/8MHz is obtained. This value was measured using a standard crystal resonator with XTH_CR [5:4]=0b10 setting, and it may vary greatly depending on the crystal manufacturer and model.



Note:

- The chip has integrated feedback resistor R_0 .
 - Damping resistor R_1 is optional, and the value of the resistance depends on the crystal characteristics, with a default value of 0 Ω .

7.3.8 Internal timer characteristics

Internal RCH oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dev	RCH oscillator accuracy	User trimming step for given VCC and TA conditions		0.25		%
		VCC = 1.8 ~ 5.5V T _{AMB} = -40 ~ 105°C	-3.5		+3.5	%
		VCC = 1.8 ~ 5.5V T _{AMB} = -20 ~ 50°C	-2.0		+2.0	%
F _{CLK}	Oscillation frequency		4.0	4.0 8.0 16.0 22.12 24.0	24.0	MHz
I _{CLK}	Power consumption	F _{MCLK} = 4MHz		80		μA
		F _{MCLK} = 8MHz		100		μA
		F _{MCLK} = 16MHz		120		μA
		F _{MCLK} = 24MHz		140		μA
DC _{CLK}	Duty Cycle ⁽¹⁾		45	50	55	%

1. Resulted from comprehensive evaluation, not tested in production.

Internal RCL oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dev	RCL oscillator accuracy	User trimming step for given VCC and TA conditions		0.5		%
		VCC = 1.8 ~ 5.5V T _{AMB} = -40 ~ 105°C	-5		+5	%
		VCC = 1.8 ~ 5.5V T _{AMB} = -20 ~ 50°C	-3		+3	%
F _{CLK}	Oscillation frequency			38.4 32.768		kHz
T _{CLK}	Start time			150		μs
DC _{CLK}	Duty Cycle ⁽¹⁾		25	50	75	%
I _{CLK}	Power consumption			0.25		μA

1. Resulted from comprehensive evaluation, not tested in production.

Internal low-speed clock 10k oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V	Operation voltage	-	1.8		5.5	V
Dev	Oscillator accuracy ⁽¹⁾	VCC = 1.8 ~ 5.5V T _{AMB} = -20 ~ 50°C	-50	-	50	%
F _{CLK}	Oscillation frequency	VCC=3.3V T _{AMB} = 25°C		10		KHz

1. Resulted from comprehensive evaluation, not tested in production.

7.3.9 Memory Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
EFLASH	Program, Sector Erase times	T _A =-40°C~105°C	Data Storage Period (RET _{FLASH}): 10 years, T _A =85°C	100000		times
			Data Storage Period (RET _{FLASH}): 20 years, T _A =85°C	20000		times
Tw_prog	Programming time		6		7.5	μs
Tp_erase	Page erase time		4		5	ms
Tm_erase	Whole chip erase time		30		40	ms

7.3.10 EFT Characteristic

A chip reset can restore the system to normal operation.

Symbol	Level/Type
EFT to IO (IEC61000-4-4)	Class:4(B)
EFT to Power (IEC61000-4-4)	Class:4(B)

Software recommendations

The software process must include control to deal with program runaway, such as:

- Corrupted program counter
- Unexpected reset
- Critical data is destroyed (control registers, etc.)

During the EFT test, interference that exceeds the application requirements can be directly applied to the chip power supply or IO. When an unexpected action is detected, the software part is strengthened to prevent unrecoverable errors.

7.3.11 ESD Characteristic

Using specific measurement methods, the chip is subjected to strength testing to determine its electrical sensitivity performance.

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
VESD _{HBM}	ESD @ Human Body Mode			4		KV
VESD _{CDM}	ESD @ Charge Device Mode			1		KV
VESD _{MM}	ESD @ machine Mode			200		V
Ilatchup	Latch up current			200		mA

7.3.12 Port characteristics

Output characteristics——ports

Table 7-8 Port output characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V _{OH}	High level output voltage Source Current	Sourcing 4 mA, VCC = 3.3 V (see Note 1)	VCC-0.25		V
		Sourcing 6 mA,, VCC = 3.3 V (see Note 2)	VCC-0.6		V
V _{OL}	Low level output voltage Sink Current	Sinking 4 mA,, VCC = 3.3 V (see Note 1)		VSS+0.25	V
		Sinking 6 mA,, VCC = 3.3 V (see Note 2)		VSS+0.6	V
V _{OHD}	High level output voltage Double source Current	Sourcing 8 mA,, VCC = 3.3 V (see Note 1)	VCC-0.25		V
		Sourcing 12 mA,, VCC = 3.3V (see Note 2)	VCC-0.6		V
V _{OLD}	Low level output voltage Double Sink Current	Sinking 8 mA,, VCC = 3.3 V (see Note 1)		VSS+0.25	V
		Sinking 12 mA,, VCC = 3.3 V (see Note 2)		VSS+0.6	V

NOTE:

1. The maximum total current, IOH(max) and IOL(max), for all outputs combined, should not exceed 40 mA, to satisfy the maximum specified voltage drop.
2. The maximum total current, IOH(max) and IOL(max), for all outputs combined, should not exceed 100 mA, to satisfy the maximum specified voltage drop.

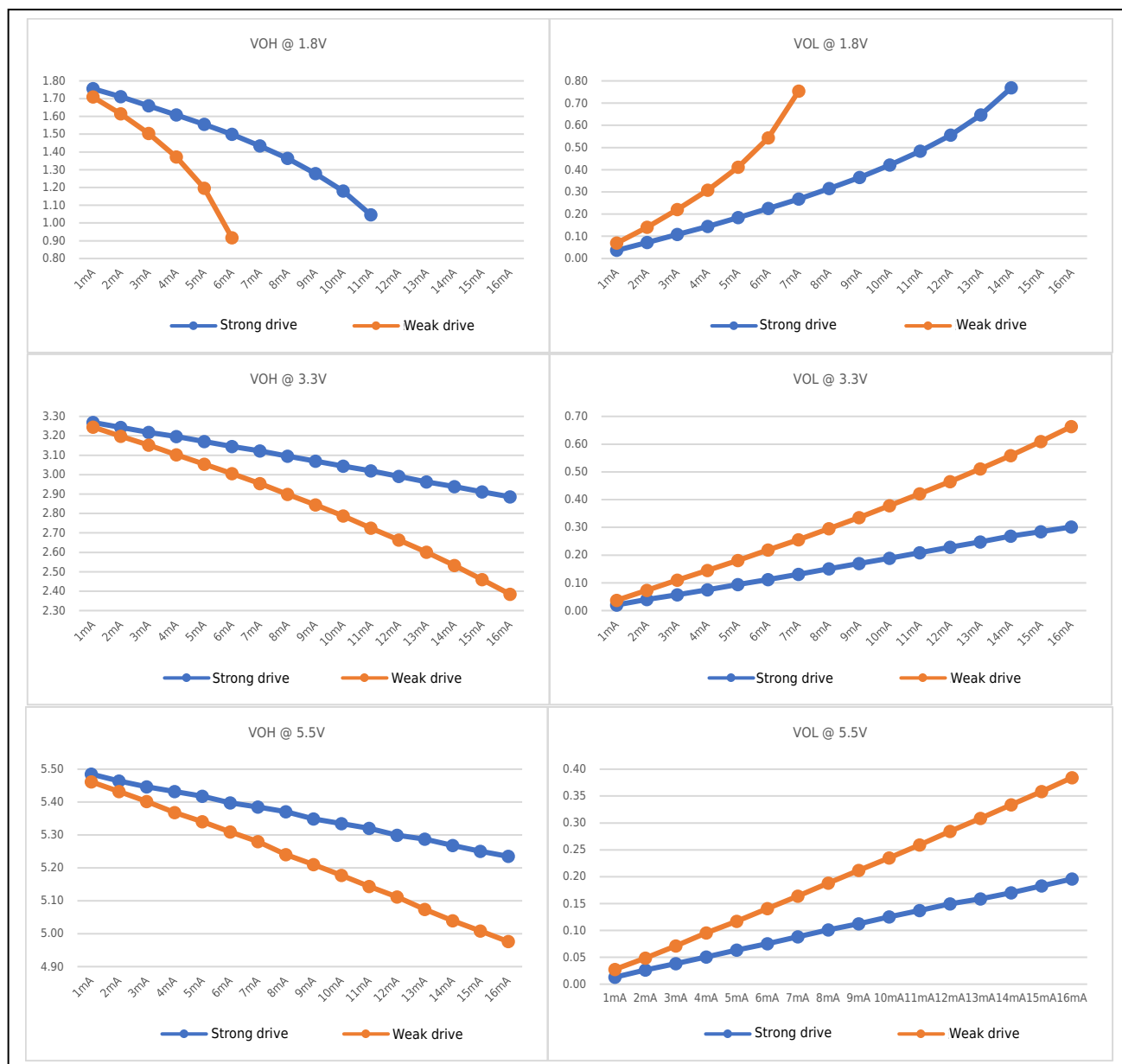


Figure 7-2 VOH/VOL measured curve of output port

Input Characteristics - Ports P0, P1, P2, P3

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{IH}	Positive-going input threshold voltage	VCC=1.8V	0.7VCC			V
		VCC=3.3V	0.7VCC			V
		VCC=5.5V	0.7VCC			V
V_{IL}	Negative-going input threshold voltage	VCC=1.8V			0.3VCC	V
		VCC=3.3V			0.3VCC	V
		VCC=5.5V			0.3VCC	V
$V_{hys(1)}$	Input voltage hysteresis ($V_{IH} - V_{IL}$)	VCC=1.8V		0.3		V
		VCC=3.3V		0.4		V
		VCC=5.5V		0.6		V
$R_{pullhigh}$	Pullup resistor	Pullup enabled VCC=3.3V		80		k Ω
$R_{pulllow}$	Pulldown resistor	Pulldown enabled VCC=3.3V		40		k Ω
C_{input}	Input capacitance			5		pF

1. Resulted from comprehensive evaluation, not tested in production.

Port external input sampling requirements—Timer Gate/Timer Clock

Symbol	Parameter	Conditions	VCC	Min	Max	Unit
$t_{(int)}$	External interrupt timing	External trigger signal for the interrupt flag (see Note 1)	1.8V	30		ns
			3.3V	30		ns
			5.5V	30		ns
$t_{(cap)}$	Timer capture timing	Timer4/5/6 capture pulse width $F_{system} = 4\text{MHz}$	1.8V	0.5		μs
			3.3V	0.5		μs
			5.5V	0.5		μs
$t_{(clk)}$	Timer clock frequency applied to pin	Timer0/1/2/4/5/6 external clock input $F_{system} = 4\text{MHz}$	1.8V		PCLK/2	MHz
			3.3V		PCLK/2	MHz
			5.5V		PCLK/2	MHz
$t_{(pca)}$	PCA clock frequency applied to pin	PCA external clock input $F_{system} = 4\text{MHz}$	1.8V		PCLK/8	MHz
			3.3V		PCLK/8	MHz
			5.5V		PCLK/8	MHz

NOTE:

1. The external signal sets the interrupt flag every time the minimum $t_{(int)}$ parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$.

Port leakage characteristics - P0, P1, P2, P3

Symbol	Parameter	Conditions	VCC	Max	Unit
$I_{lkg}(P_{x,y})$	Leakage current	$V_{(P_{x,y})}$ (see Note 1,2)	1.8 V/3.6 V	± 50	nA

NOTE:

1. The leakage current is measured with VSS or VCC applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input.

7.3.13 RESETB pin characteristics

The RESETB pin input driver uses CMOS technology, which is connected with a pull-up resistor that cannot be disconnected.

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
$V_{IL}(\text{RESETB})^{(1)}$	Input low level voltage		-0.3		0.3VCC	V
$V_{IH}(\text{RESETB})$	Input high level voltage		0.7VCC		VCC+0.3	V
$V_{hys}(\text{RESETB})$	Schmitt trigger voltage hysteresis			200		mV
R_{PU}	Weak pull-up equivalent resistance	$V_{IN} = V_{SS}$		80		K Ω
$T_F(\text{RESETB})^{(1)}$	Input filter pulse				2	μ s
$T_{NF}(\text{RESETB})^{(1)}$	Input unfiltered pulse		10			μ s

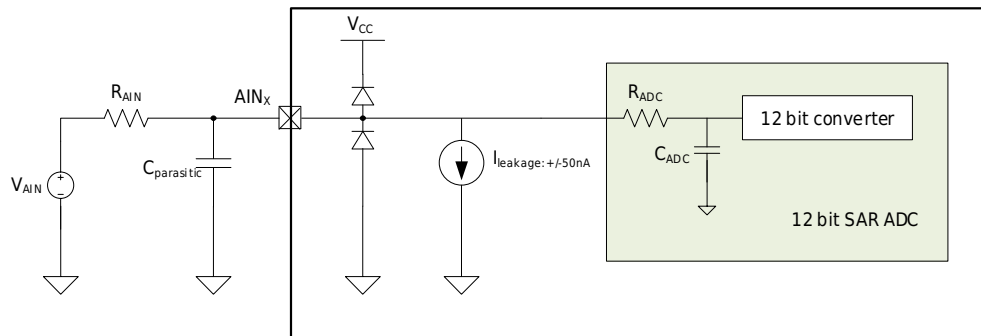
1. Guaranteed by design, not tested in production.

7.3.14 ADC Characteristic

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{ADCIN}	Input voltage range	Single ended	0		$V_{ADCREFIN}$	V
$V_{ADCREFIN}$	Input range of external reference voltage	Single ended	0		VCC	V
$DEV_{VCC/3}$	VCC/3 accuracy			3		%
I_{ADC1}	Active current including reference generator and buffer	200Ksps		2		mA
I_{ADC2}	Active current without reference generator and buffer	1Msps		0.5		mA
C_{ADCIN}	ADC input capacitance			16	19.2	pF
$R_{ADC}^{(1)}$	ADC sampling switch impedance			1.5		K Ω
$R_{AIN}^{(1)}$	ADC external input resistor ⁽²⁾				100	K Ω
F_{ADCCLK}	ADC clock Frequency				24M	Hz
$T_{ADCSTART}$	Startup time of reference generator and ADC core			30		μ s
$T_{ADCCONV}$	Conversion time		20	24	28	cycles
ENOB	Effective Bits	1Msps@VCC $\geq$ 2.7V 500Ksps@VCC $\geq$ 2.4V 200Ksps@VCC $\geq$ 1.8V REF=EXREF		10.3		Bit
		1Msps@VCC $\geq$ 2.7V 500Ksps@VCC $\geq$ 2.4V 200Ksps@VCC $\geq$ 1.8V REF=VCC		10.3		Bit
		200Ksps@VCC $\geq$ 1.8V REF=internal 1.5V		9.4		Bit
		200Ksps@VCC $\geq$ 2.8V REF=internal 2.5V		9.4		Bit
SNR	Signal to Noise Ratio	1Msps@VCC $\geq$ 2.7V 500Ksps@VCC $\geq$ 2.4V		68.2		dB

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
		200Ksps@VCC>=1.8V REF=EXREF				
		1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=VCC		68.2		dB
		200Ksps@VCC>=1.8V REF=internal 1.5V		60		dB
		200Ksps@VCC>=2.8V REF=internal 2.5V		60		dB
DNL ⁽¹⁾	Differential non-linearity	200Ksps; VREF=EXREF/VCC	-1		1	LSB
INL ⁽¹⁾	Integral non-linearity	200Ksps; VREF=EXREF/VCC	-3		3	LSB
E _o	Offset error			0		LSB
E _g	Gain error			0		LSB

1. Guaranteed by design, not tested in production.
2. The typical application of ADC is shown in the figure below:



Under the condition of 0.5LSB sampling error accuracy requirement, the calculation formula of external input impedance is as follows:

$$R_{AIN} = \frac{M}{F_{ADC} * C_{ADC} * (N + 1) * \ln(2)} - R_{ADC}$$

Among them F_{ADC} is the ADC clock frequency, the register ADC_CR0<3:2> can set the relationship between it and PCLK, as shown in the following table:

The following table shows the ADC clock frequency F_{ADC} Relationship with PCLK frequency division ratio:

ADC_CR0<3:2>	N
00	1
01	2
10	4
11	8

M is the number of sampling periods, which is set by the register ADC_CR0<13:12>.

The following table shows the relationship between sampling time t_{sa} and ADC clock frequency F_{ADC} :

ADC_CR0<13:12>	M
00	4
01	6
10	8
11	12

The following table shows the relationship between ADC clock frequency F_{ADC} and external resistance R_{AIN} (M=12, under the condition of sampling error 0.5LSB):

R_{AIN} (k Ω)	F_{ADC} (kHz)
10	5600
30	2100
50	1300
80	820
100	660
120	550
150	450

For the above typical applications, you should pay attention to:

- Minimize the ADC input port AIN_X parasitic capacitance $C_{PARACITIC}$;
- In addition to considering R_{AIN} the value, if the internal resistance of the signal source V_{AIN} is large, it also needs to be considered.

7.3.15 VC Characteristic

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Vin	Input voltage range		0		5.5	V
Vincom	Input common mode range		0		VCC-0.2	V
Voffset	Input offset	Room temperature 25°C 3.3V	-10		+10	mV
Icomp	Comparator's current	VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11		0.3 1.2 10 20		μA
Tresponse	Comparator's response time when one input cross another	VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11		20 5 1 0.2		μs
Tsetup	Comparator's setup time when ENABLE. Input signals unchanged.	VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11		20 5 1 0.2		μs
Twarmup	From main bandgap enable to Temp sensor voltage、ADC internal 1.5V, 2.5V reference stable			20		μs
Tfilter	Digital filter time	VC_debounce = 000 VC_debounce = 001 VC_debounce = 010 VC_debounce = 011 VC_debounce = 100 VC_debounce = 101 VC_debounce = 110 VC_debounce = 111		7 14 28 112 450 1800 7200 28800		μs

7.3.16 TIM timer features

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), see the table below.

Table 7-9 Advanced Timer (ADVTIM) Features

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t _{res}	Timer to distinguish time		1		t _{TIMCLK}
		f _{TIMCLK} =32MHz	31.3		ns
f _{ext}	External clock frequency		0	f _{TIMCLK} /2	MHz
		f _{TIMCLK} =32MHz	0	16	MHz
Re _{STim}	Timer resolution			16	位
T _{counter}	When the internal clock is selected, the 16-bit counter clock cycle		1	65536	t _{TIMCLK}
		f _{TIMCLK} =32MHz	0.0313	2051	μs
T _{MAX_COUNT}	Maximum possible count			67108864	t _{TIMCLK}
		f _{TIMCLK} =32MHz		2.1	s

1. Guaranteed by design, not tested in production.

Table 7-10 Basic Timer Characteristics

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t _{res}	Timer to distinguish time		1		t _{TIMCLK}
		f _{TIMCLK} =32MHz	31.3		ns
f _{ext}	External clock frequency		0	f _{TIMCLK} /2	MHz
		f _{TIMCLK} =32MHz	0	16	MHz
Re _{STim}	Timer resolution	reload count		16	位
		free count		32	位
T _{counter}	When the internal clock is selected, the 16-bit counter clock cycle		1	65536	t _{TIMCLK}
		f _{TIMCLK} =32MHz	0.0313	2051	μs
T _{MAX_COUNT}	Maximum possible count (reload mode)			16777216	t _{TIMCLK}
		f _{TIMCLK} =32MHz		524.3	ms

1. Guaranteed by design, not tested in production.

Table 7-11 PCA Characteristics

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t _{res}	Timer to distinguish time		1		t _{TIMCLK}
		f _{TIMCLK} =32MHz	31.3		ns
f _{ext}	External clock frequency		0	f _{TIMCLK} /2	MHz
		f _{TIMCLK} =32MHz	0	16	MHz
Res _{Tim}	Timer resolution			16	Bit
T _{counter}	When the internal clock is selected, the 16-bit counter clock cycle		1	65536	t _{TIMCLK}
		f _{TIMCLK} =32MHz	0.0313	2051	μs
T _{MAX_COUNT}	Maximum possible count			2097152	t _{TIMCLK}
		f _{TIMCLK} =32MHz		65.54	ms

1. Guaranteed by design, not tested in production.

Table 7-12 WDT Characteristics

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t _{res}	WDT overflow time	f _{WDTCLK} =10kHz	1.6	52000	ms

1. Guaranteed by design, not tested in production.

7.3.17 Communication Interface

I2C features

I2C interface characteristics are as follows:

Table 7-13 I2C Interface Characteristics

Sym bol	Parameter	Standard mode (100K)		Fast mode (400K)		High speed mode (1M)		U ni t
		Minimum Value	Maximum Value	Minimum Value	Maximum Value	Minimum Value	Maximum Value	
t _{SCLL}	SCL clock low time	4.7		1.25		0.5		μs
t _{SCLH}	SCL clock high time	4.0		0.6		0.26		μs
t _{SU.SDA}	SDA establishment time	250		100		50		ns
t _{HD.SDA}	SDA hold time	0		0		0		μs
t _{HD.STA}	Start condition hold time	2.5		0.625		0.25		μs
t _{SU.STA}	Repeated start condition establishment time	2.5		0.6		0.25		μs
t _{SU.STO}	Stop condition establishment time	0.25		0.25		0.25		μs
t _{BUF}	Bus idle (stop condition to start condition)	4.7		1.3		0.5		μs

1. Guaranteed by design, not tested in production.

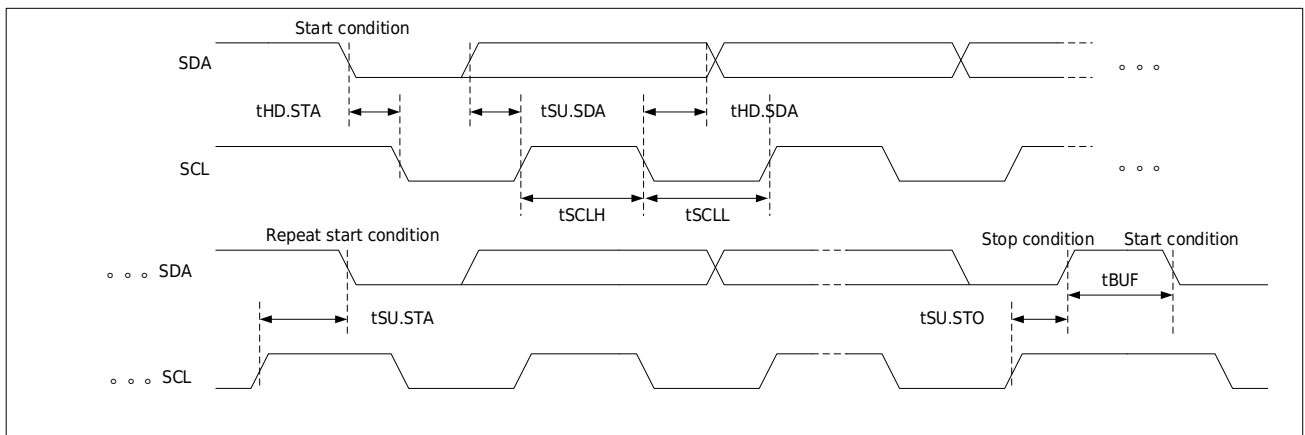


Figure 7-3 I2C Interface Timing

SPI features

Table 7-14 SPI Interface Features⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions	Minimum value	Maximum Value	Unit
$t_{c(SCK)}$	Serial clock period ⁽³⁾	Host Transmit Mode $f_{PCLK} = 32\text{ MHz}$	62.5	-	ns
		Host Receive Mode $f_{PCLK} = 32\text{ MHz}$	160	-	ns
		Slave Transmit Mode $f_{PCLK} = 32\text{ MHz}$	160	-	ns
		Slave Receive Mode $f_{PCLK} = 32\text{ MHz}$	84	-	ns
$t_{w(SCKH)}$	High level time of serial clock	Host mode	$0.45 \times t_{c(SCK)}$	-	ns
		Slave mode	$0.45 \times t_{c(SCK)}$	-	ns
$t_{w(SCKL)}$	Low level time of serial clock	Host mode	$0.45 \times t_{c(SCK)}$	-	ns
		Slave mode	$0.45 \times t_{c(SCK)}$	-	ns
$t_{su(SSN)}$	Setup time selected by slave	Slave mode	$0.45 \times t_{c(SCK)}$	-	ns
$t_h(SSN)$	Hold time selected by slave	Slave mode	$0.45 \times t_{c(SCK)}$	-	ns
$t_v(MO)$	Effective time of host data output	-	-	3	ns
$t_h(MO)$	Hold time of host data output	-	2	-	ns
$t_v(SO)$	Effective time of slave data output	-	-	$1.5 \times T_{pclk} + 20$	ns
$t_h(SO)$	Hold time of slave data output	-	$0.5 \times T_{pclk} + 10$	-	ns
$t_{su(MI)}$	Setup time of host data input	-	10	-	ns
$t_h(MI)$	Hold time of host data input	-	2	-	ns
$t_{su(SI)}$	Setup time of slave data input	-	10	-	ns
$t_h(SI)$	Hold time of slave data input	-	2	-	ns

1. Guaranteed by design and not tested in production.
2. The data is based on the condition of $V_{CC} = 3.0V$.
3. The maximum prescaler factor in host mode is $PCLK/2$, and in slave mode, it is $PCLK/4$.

The waveform and timing parameters of the SPI interface signal are as follows:

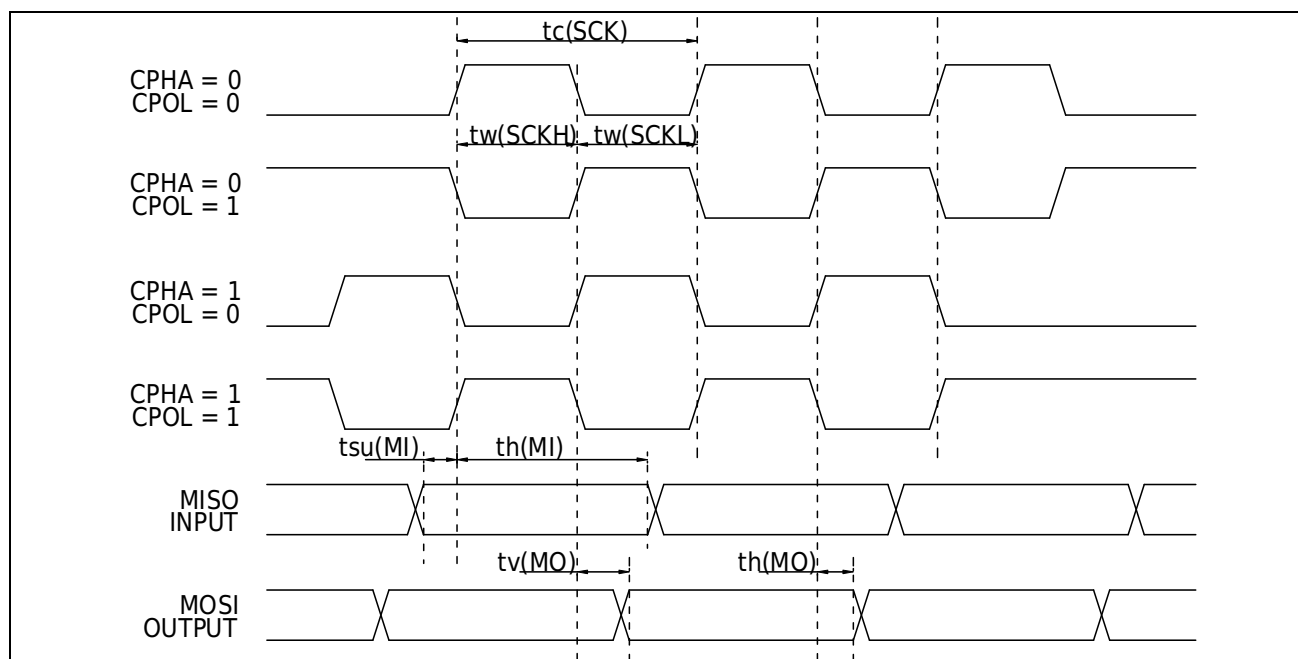


Figure 7-4 SPI Timing Diagram (Host Mode)

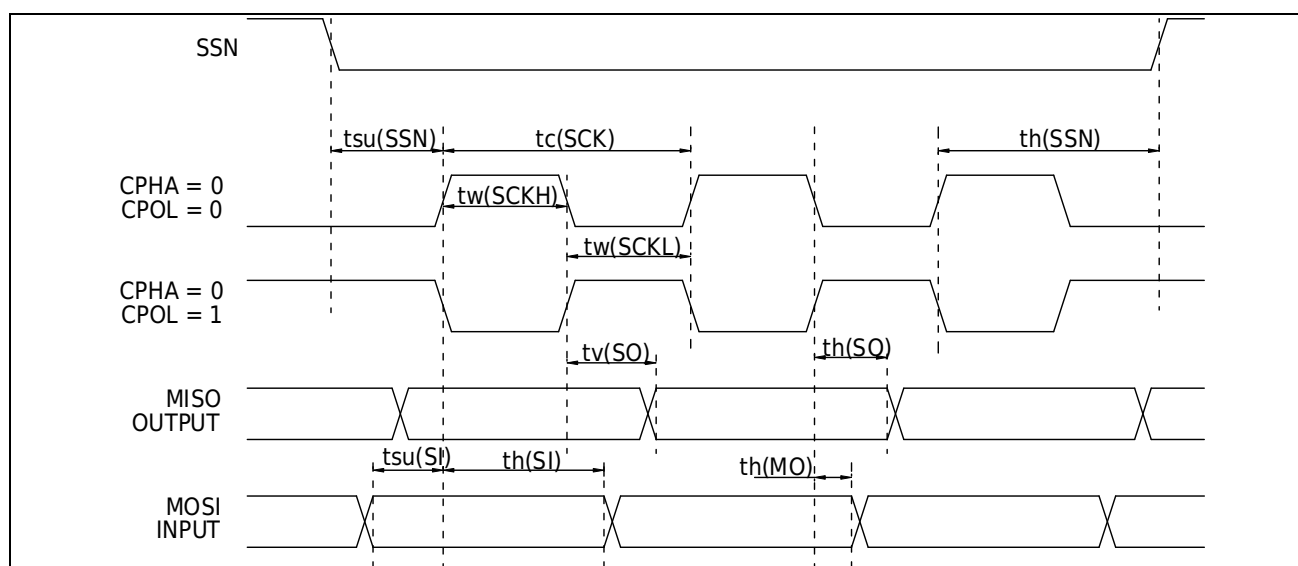


Figure 7-5 SPI Timing Diagram (slave mode cpha=0)

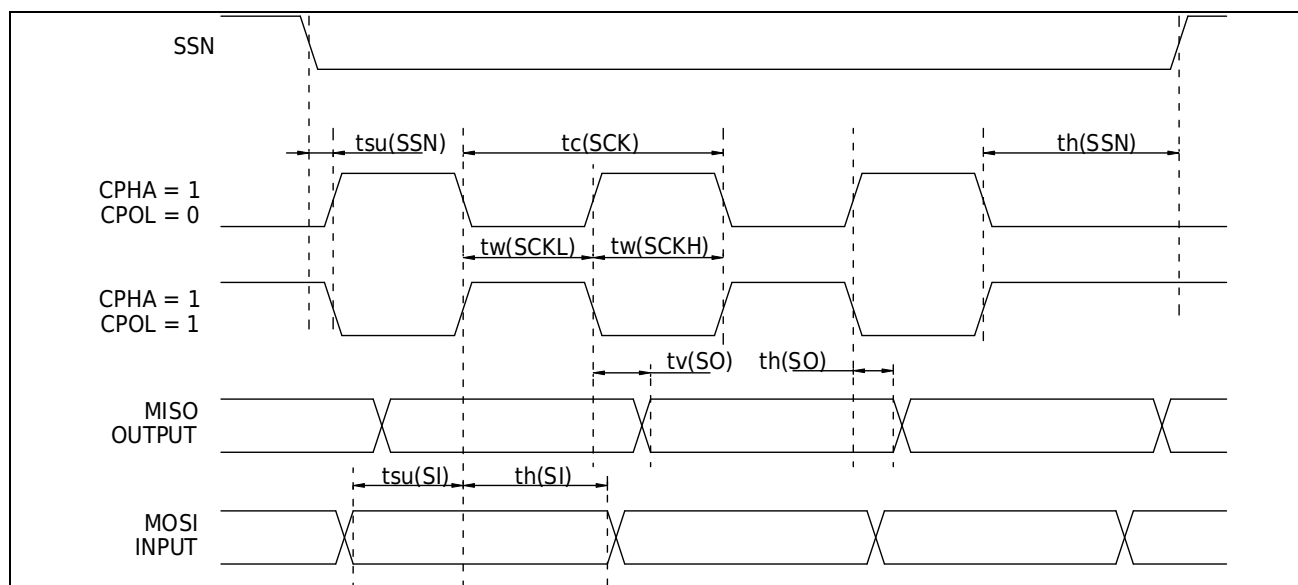
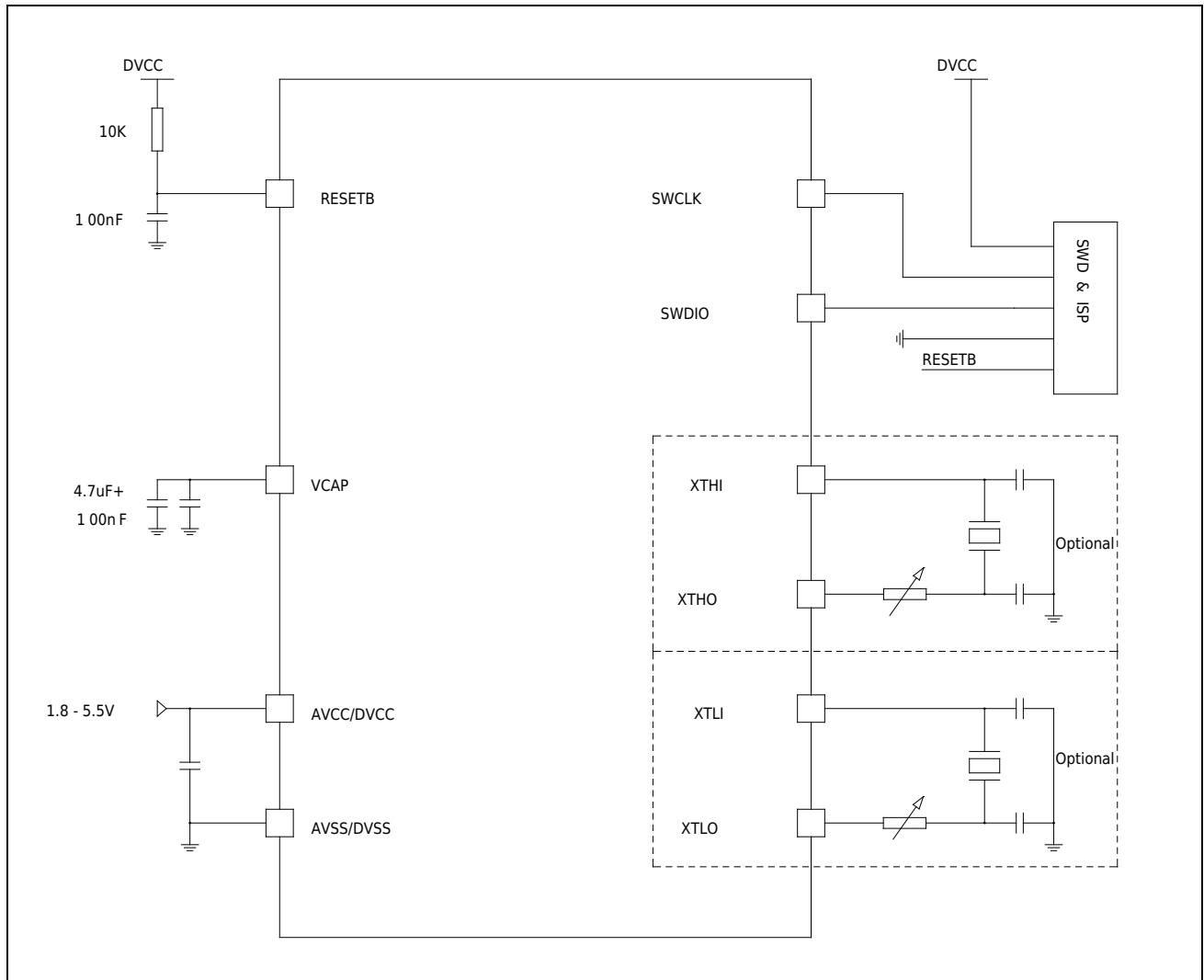


Figure 7-6 SPI Timing Diagram (slave mode cpha=1)

8 Typical application circuit diagram



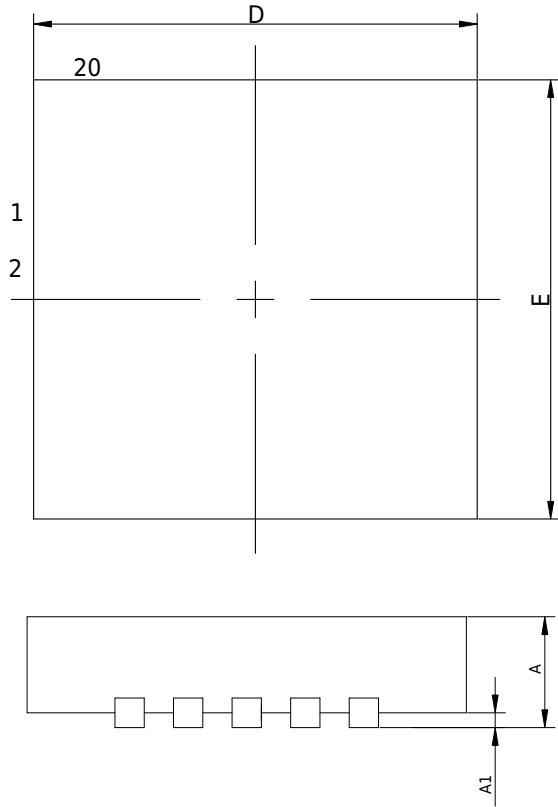
Note:

- Power supply for each group requires external decoupling capacitors. For better anti-interference capability, it is preferable to route the power supply/ground lines through the decoupling capacitors first before connecting them to the chip.

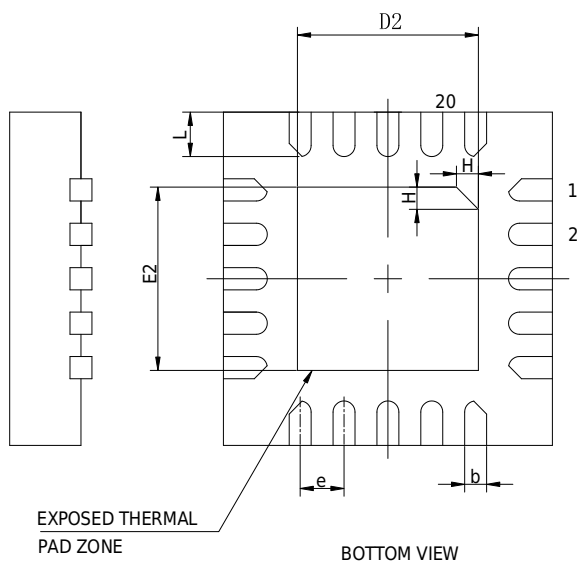
9 Package information

9.1 Packaging Size

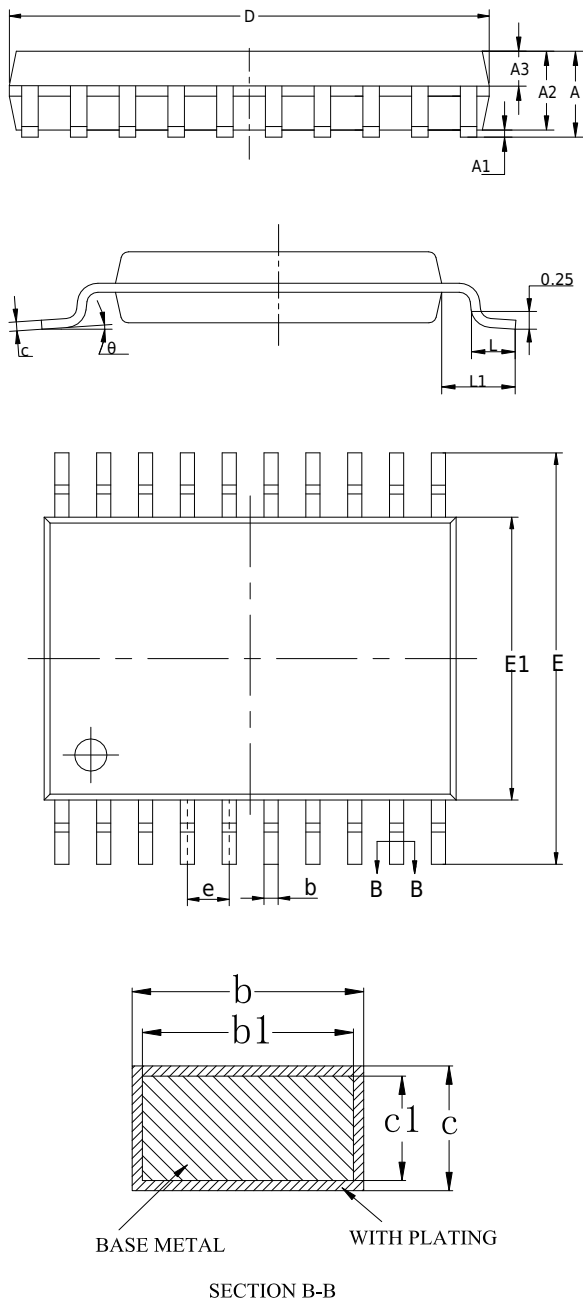
QFN20 packaging



Symbol	QFN20 (3x3 0.75) millimeter			QFN20 (3x3 0.55) millimeter		
	Min	Nom	Max	Min	Nom	Max
A	0.70	0.75	0.80	0.50	0.55	0.60
A1	--	0.02	0.05	--	0.02	0.05
b	0.15	0.20	0.25	0.15	0.20	0.25
D	2.90	3.00	3.10	2.90	3.00	3.10
D2	1.55	1.65	1.75	1.60	1.70	1.80
e	0.40BSC					
E	2.90	3.00	3.10	2.90	3.00	3.10
E2	1.55	1.65	1.75	1.60	1.70	1.80
L	0.35	0.40	0.45	0.25	0.30	0.35
H	0.25REF			0.25REF		



TSSOP20 packaging

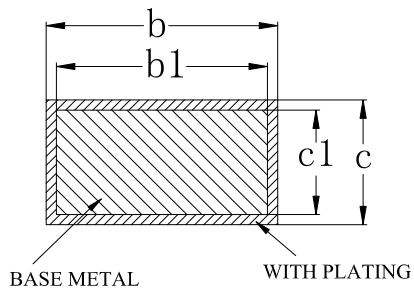
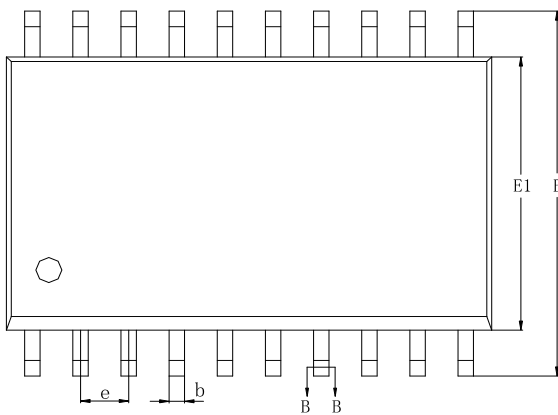
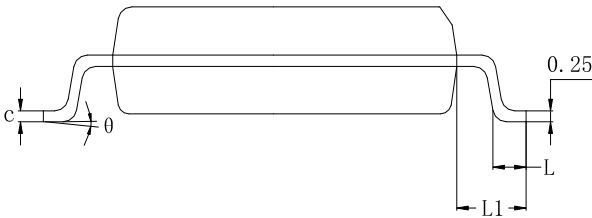
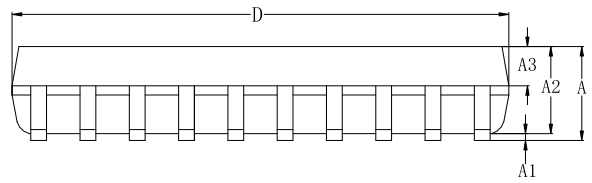


Symbol	TSSOP20 millimeter		
	Min	Nom	Max
A	--	--	1.20
A1	0.05	--	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	--	0.28
b1	0.19	0.22	0.25
c	0.13	--	0.18
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	--	8°

NOTE:

- Dimensions "D" and "E1" do not include mold flash.

SOP20 packaging



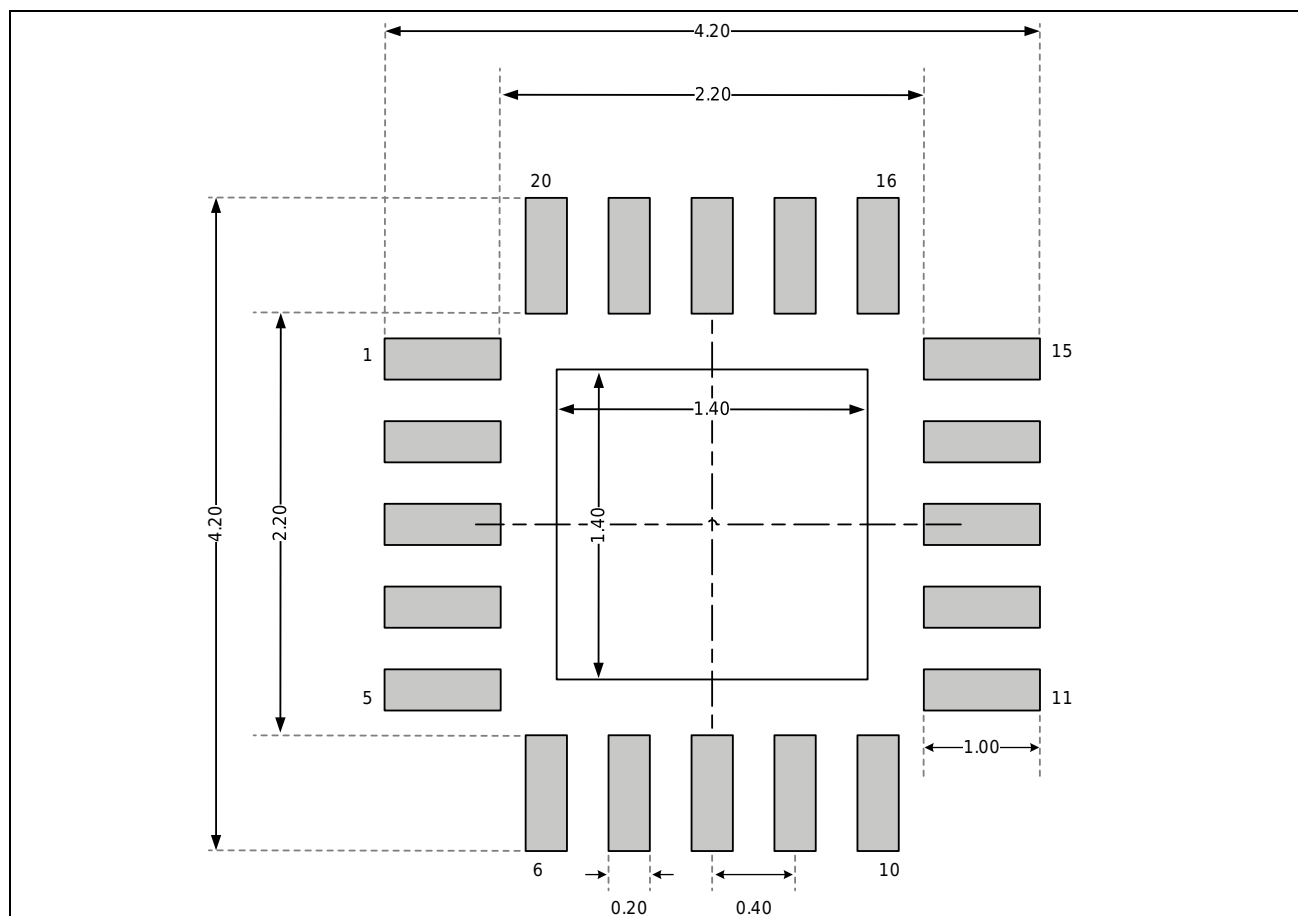
SECTION B-B

Symbol	SOP20 millimeter		
	Min	Nom	Max
A	--	--	2.65
A1	0.10	--	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	--	0.47
b1	0.38	0.41	0.44
c	0.25	--	0.29
c1	0.24	0.25	0.26
D	12.70	12.80	12.90
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.70	--	1.00
L1	1.40REF		
θ	0	--	8°

NOTE:

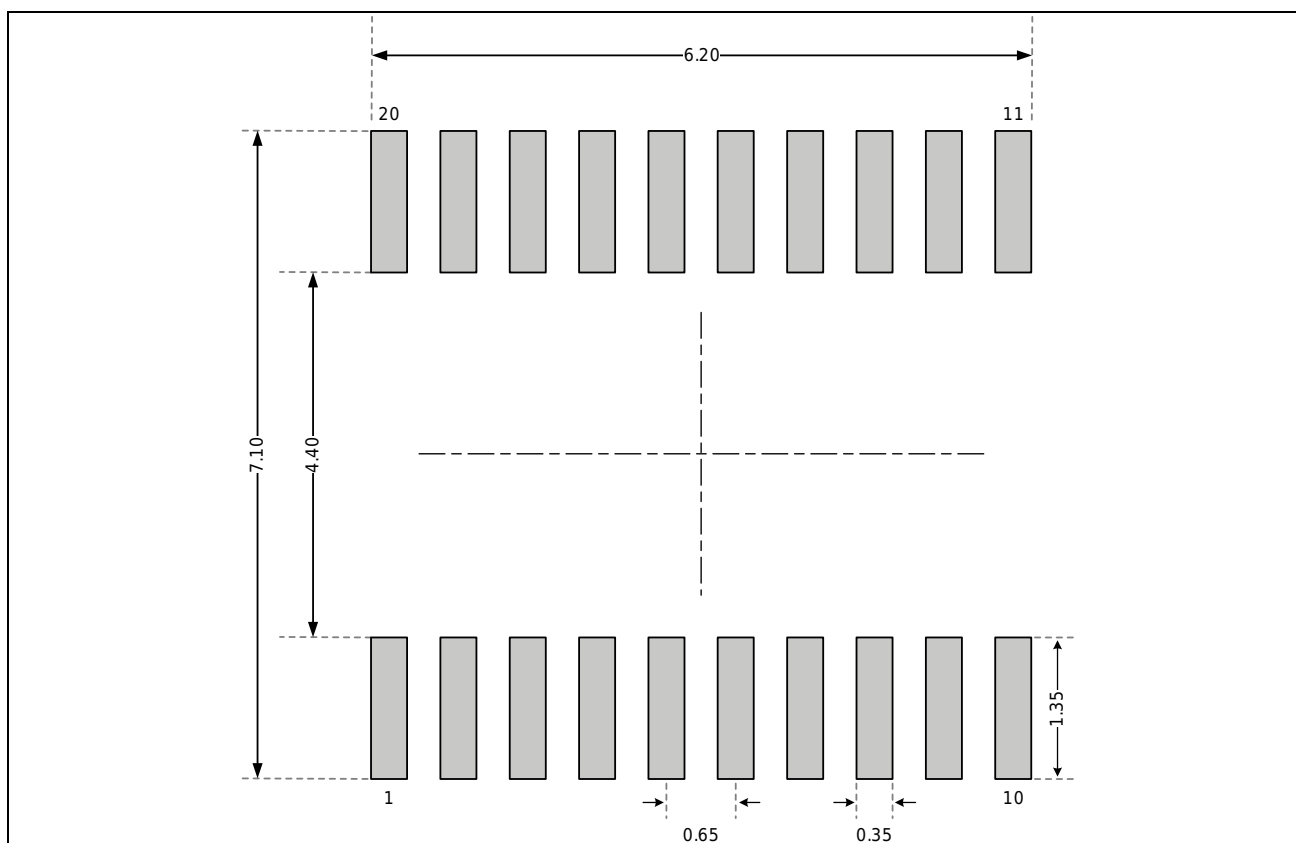
- Dimensions “D” and “E1” do not include mold flash.

QFN20 packaging (3mm x 3mm)



- Dimensions are expressed in millimeters.
- Dimensions are for reference only.

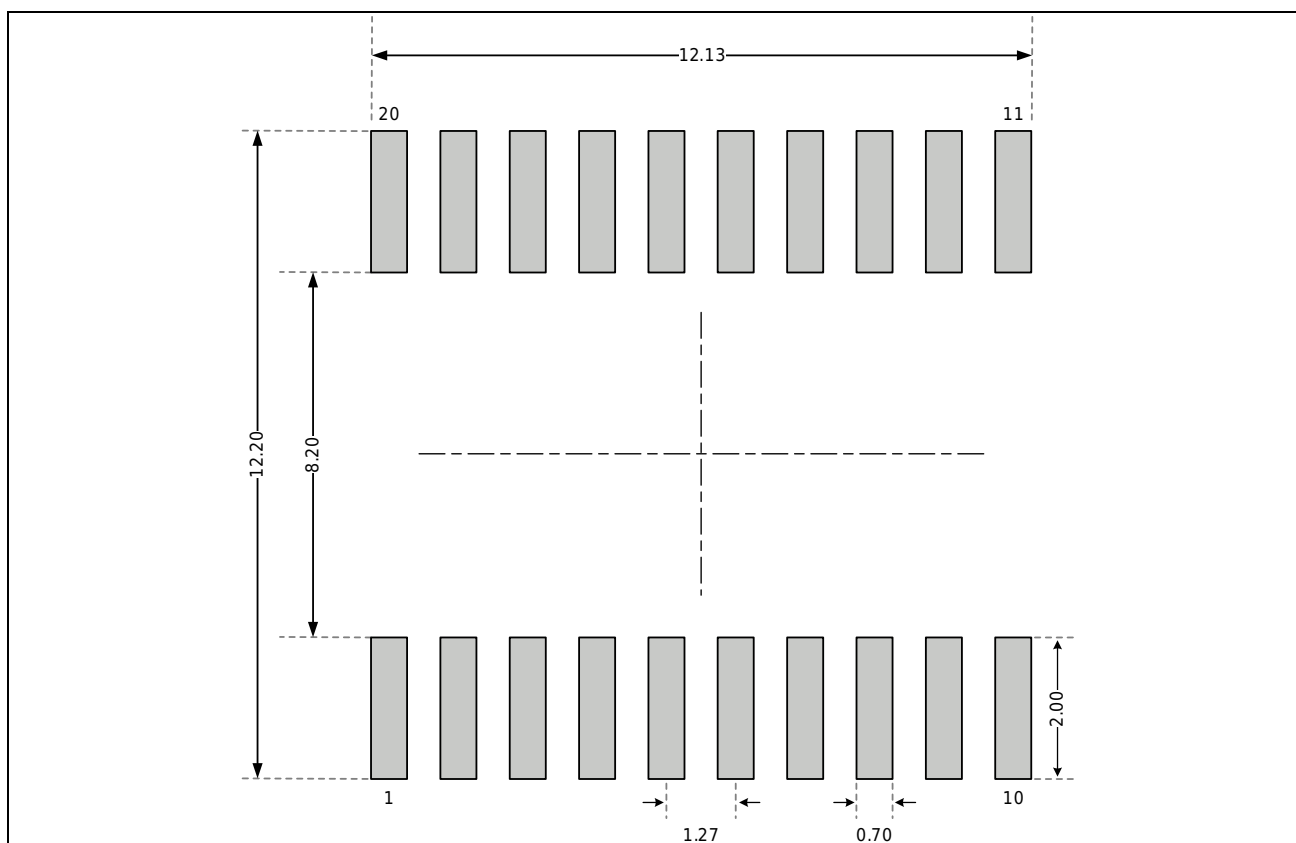
TSSOP20 packaging



NOTE:

- Dimensions are expressed in millimeters.
- Dimensions are for reference only.

SOP20 packaging



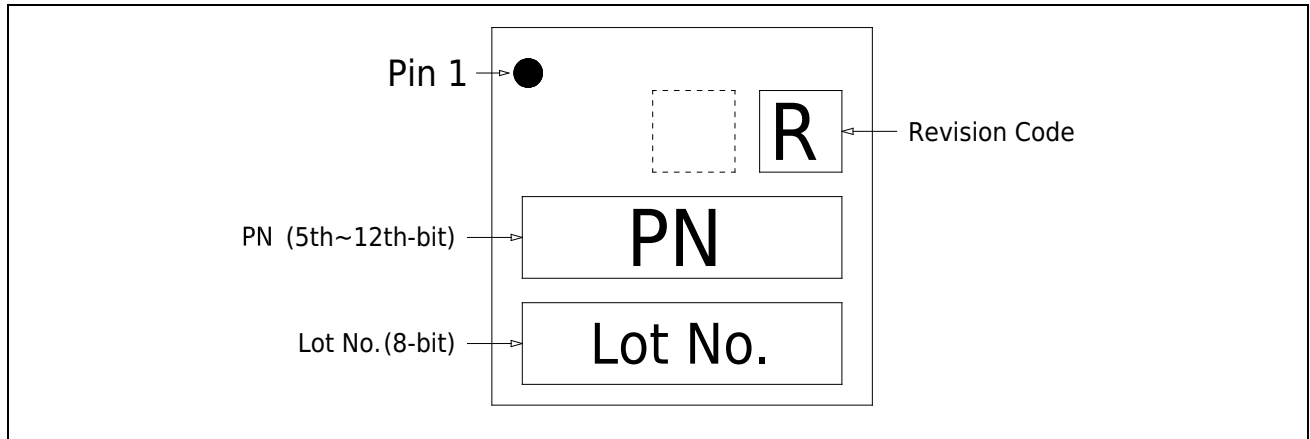
NOTE:

- Dimensions are expressed in millimeters.
- Dimensions are for reference only.

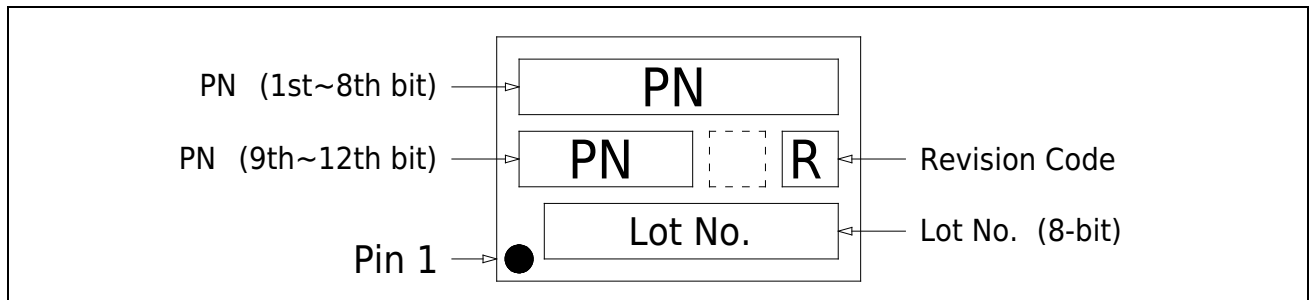
9.3 Silkscreen instructions

The position and information of Pin 1 printed on the front of each package are given below.

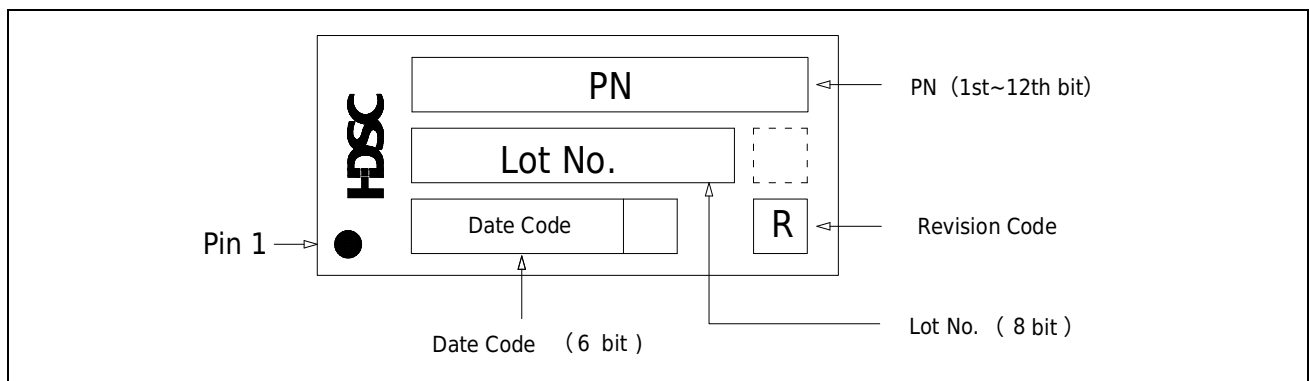
QFN20 packaging (3mm x 3mm)



TSSOP20 package



SOP20 packaging



Note:

- The blank boxes in the above figure indicate optional marks related to production, which are not explained in this section.

9.4 Packaging Thermal Resistance Coefficient

When the packaged chip is working at the specified working environment temperature, the junction temperature T_j (°C) of the chip surface can be calculated according to the following formula:

$$T_j = T_{amb} + (P_D \times \theta_{JA})$$

- T_{amb} refers to the working environment temperature when the packaged chip is working, the unit is °C;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is °C/W;
- P_D is equal to the sum of internal power consumption of the chip and I/O power consumption, and the unit is W. The internal power consumption of the chip is the product's $I_{DD} \times V_{DD}$. I/O power consumption refers to the power consumption generated by the I/O pins when the chip is working. Usually this part of the value is very small and can be ignored.

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable junction temperature T_j of the chip.

Table 9-1 Thermal resistance coefficient table for each package

Package Type and Size	Thermal Resistance Junction-ambient Value (θ_{JA})	Unit
QFN20 3mm x 3mm / 0.4mm pitch	70 +/- 10%	°C/W
SOP20	92 +/- 10%	°C/W
TSSOP20	91 +/- 10%	°C/W

10 Ordering Information

Part Number	Flash	RAM	UART	SPI	I2C	ADC (12Bit)	VComp	I/O	LVD	Timer	PWM	PCA	CRC16	Vdd	Package	Foot spacing	Shipping Form	Working temperature	Chip thickness
HC32F005C6UA-SFN20TR	32K	4K	2	1	1	9ch	2	16+1	✓	6*16Bit	6*16Bit	✓	✓	1.8~5.5v	QFN20(3*3)	0.4mm	Tape	-40~85°C	0.75mm
HC32F005C6PA-SOP20	32K	4K	2	1	1	9ch	2	16+1	✓	6*16Bit	6*16Bit	✓	✓	1.8~5.5v	SOP20	1.27mm	Tube	-40~85°C	2.65mm
HC32F005C6PA-TSSOP20	32K	4K	2	1	1	9ch	2	16+1	✓	6*16Bit	6*16Bit	✓	✓	1.8~5.5v	TSSOP20	0.65mm	Tube	-40~85°C	1.2mm
HC32F005C6PB-TSSOP20	32K	4K	2	1	1	9ch	2	16+1	✓	6*16Bit	6*16Bit	✓	✓	1.8~5.5v	TSSOP20	0.65mm	Tube	-40~105°C	1.2mm
HC32F005C6PB-TSSOP20TR	32K	4K	2	1	1	9ch	2	16+1	✓	6*16Bit	6*16Bit	✓	✓	1.8~5.5v	TSSOP20	0.65mm	Tape	-40~105°C	1.2mm
HC32F005C6PA-TSSOP20TR	32K	4K	2	1	1	9ch	2	16+1	✓	6*16Bit	6*16Bit	✓	✓	1.8~5.5v	TSSOP20	0.65mm	Tape	-40~85°C	1.2mm
HC32F003C4UA-SFN20TR	16K	2K	2	1	1	9ch	2	16+1	✓	6*16Bit	6*16Bit	✓	✓	1.8~5.5v	QFN20(3*3)	0.4mm	Tape	-40~85°C	0.75mm
HC32F003C4PA-SOP20	16K	2K	2	1	1	9ch	2	16+1	✓	6*16Bit	6*16Bit	✓	✓	1.8~5.5v	SOP20	1.27mm	Tube	-40~85°C	2.65mm
HC32F003C4PA-TSSOP20	16K	2K	2	1	1	9ch	2	16+1	✓	6*16Bit	6*16Bit	✓	✓	1.8~5.5v	TSSOP20	0.65mm	Tube	-40~85°C	1.2mm
HC32F003C4PB-TSSOP20	16K	2K	2	1	1	9ch	2	16+1	✓	6*16Bit	6*16Bit	✓	✓	1.8~5.5v	TSSOP20	0.65mm	Tube	-40~105°C	1.2mm
HC32F003C4PA-TSSOP20TR	16K	2K	2	1	1	9ch	2	16+1	✓	6*16Bit	6*16Bit	✓	✓	1.8~5.5v	TSSOP20	0.65mm	Tape	-40~85°C	1.2mm

Before ordering, please contact the sales window for the latest mass production information.

Version revision history

version number	Revision Date	modify the content
Rev1.00	2018/01/24	The first edition of the HC32F003/ HC32F005 series data sheet was released.
Rev1.10	2018/04/04	New version updated.
Rev1.20	2018/04/17	Corrected Flash parameters.
Rev1.30	2018/04/27	Added three types of business numbers.
Rev1.40	2018/05/02	Revised the product selection table, updated VC electrical parameters.
Rev1.50	2018/05/22	Revised the product selection table and updated the electrical parameters of ADC & XTH.
Rev1.60	2018/11/01	Added Chapter 1 description, updated Chapter 7 Electrical Characteristics, and added Chapter 9 ordering information.
Rev1.70	2018/11/15	Added "Silkscreen Instructions" in Chapter 8, and corrected the package size of QFN20 / QFN24 / TSSOP20.
Rev1.80	2018/12/28	Corrected TSSOP20 package size.
Rev1.90	2019/02/22	Corrected the following data: ① ADC characteristics ② ESD characteristics ③ Minimum value of ECFLASH in memory characteristics ④ TSSOP20 package size ⑤ QFN20/24 package silk-screen description ⑥ Added NOTE to the package size ⑦ Updated the order information ⑧ Added AVSS/AVCC to the pin configuration.
Rev2.00	2019/07/01	Corrected the following data: ①Corrected the UID address to 0x0010_0E74-0x0010_0E7F ②Corrected the programming mode ③ Updated the QFN pin configuration diagram style ④ Added the shipping form to the Ordering Information.
Rev2.10	2019/09/06	Added the commercial number (operating temperature -40 ~ 105°C), updated the value of 7.3.2, and updated the typical application circuit diagram.
Rev2.20	2019/12/06	Corrected the following data: ① Typical application circuit diagram ②ADC characteristic unit ③ XTH illustration and precautions in external clock source characteristics.
Rev2.30	2020/01/17	Updated the silk-screen printing instructions.
Rev2.40	2020/03/06	Added a note to the "Programming Mode" in the introduction.
Rev2.50	2020/04/30	Corrected the following data: ① Added VCC/3 accuracy to the ADC characteristics; ② Accuracy of the RCL oscillator in 7.3.8.
Rev2.60	2020/07/31	Corrected the following data: ① Added sections 7.3.16 and 7.3.17; ② Added the schematic diagram of the pad and the thermal resistance coefficient of the package; ③ Grade 7.3.10; ④7.3.1 Internal AHB/APB clock frequency; ⑤0 input characteristics - The values of V _{IH} and V _{IL} in port P0,P1,P2,P3, and RESET.
Rev2.70	2020/09/30	Corrected the following data: ① The description of the clock system in the introduction; ② The accuracy of the RCH oscillator in 7.3.8 ③ V _{IL} and V _{IH} of 7.3.13; ④ Added SPI features.
Rev2.80	2021/05/31	Corrected the following data: ① Modified the statement; ② The parameters t _{HD,STA} and t _{SU,STO} in the I2C characteristics; ③ The serial peripheral interface SPI in the introduction; ④ Data retention period in memory characteristics; ⑤ Added the gm parameter to the characteristics of the external clock source.
Rev2.90	2022/03/09	Company logo update.
Rev2.91	2022/08/13	Corrected the following data: ① Embedded reset and LVD module characteristics. The signal names in Figure 7-1 were inconsistent with

version number	Revision Date	modify the content
		those in the reference manual. Modified them to be unified; ② The built-in reference voltage, based on the assessment results, expanded the accuracy range at all temperatures and voltages to $\pm 2.5\%$. ③ RESETB pin characteristics, modification of input filter pulse time.
Rev2.92	2022/10/25	Updated the "Pin Configuration" chapter drawing display is not clear.
Rev2.93	2023/06/21	Deleted RTC real-time clock function in section "2.2 Function".
Rev2.94	2024/06/25	Corrected the following data: ① Modified the number of ADC and VC channels in the 1 introduction, deleted the relevant description of 1.2V, and deleted the relevant description of 1.2V in 7.3.15; ② Modified the storage temperature range in Table 7-3 Temperature Characteristics; ③ 7.3.8 Added the section of "Internal Low-Speed Clock 10k Oscillator" to the internal clock source characteristics.
Rev2.95	2024/12/12	Updated the content of "High-Speed External Clock XTH" in "7.3.7 External timer characteristic".
Rev2.96	2025/03/28	Corrected the following data: ① Updated the relevant parameters in the SPI interface characteristics of Table 7-15; ② Modified the maximum value of the input filter pulse and the minimum value of the input non-filter pulse in the 7.3.13 RESETB pin characteristics.
Rev2.97	2026/02/11	Corrected the following data: ① The "Absolute Maximum Ratings" section: changed the symbol "To" to " T_{jmax} "; in Table 7-3 temperature characteristics, revised the description of "To" from working temperature range to maximum junction temperature; ② The "General working Conditions" section: added the description and notes for T_j in Table 7-4; ③ The "External timer characteristic - High-Speed External Clock XTH" section: updated the C_{Lx} description to "matching capacitance" and optimized its notes; ④ The "Memory Characteristics" section: optimized EC_{FLASH} parameters per new conditions and added the 100K data; ⑤ The "Package Size" section: QFN20 package, modified the L, H (original h), D2, E2 size information, deleted the c, Ne, Nd, L/F carrier size information, and optimized the package drawing; QFN24 package, modified the b, H (original h) size information, deleted the c, Ne, Nd, L/F carrier size information, and optimized the package drawing.
Rev3.00	2026/08/19	Corrected the following data: ① The "Absolute Maximum Ratings" section, merged the voltage and current characteristic tables; ② The "Typical Application Circuit Diagram" section, revised the description of decoupling capacitors; ③ The "Schematic diagram of pad" section, optimized pad dimensions and removed redundant data; ④ The "Ordering Information" section, removed chip models HC32F005D6UA-QFN24TR and HC32F005C6UA-ZFN20TR, and added chip model HC32F005C6PB-TSSOP20TR.