XIAOHUA SEMICONDUCTOR

HC32F431 Series

32-bit ARM® Cortex®-M4 Microcontroller

Datasheet

Rev1.00

July 2026

Feature List

ARM Cortex-M4 32-bit MCU+FPU, 150DMIPS, 128KB Code Flash, 16KB SRAM, 10Timers, 1ADC, 1DAC, 3CMPs, 3OPAs, 4UARTs, 1SPI, 1I2C, 1HALL

- ARMv7-M architecture, 32-bit Cortex-M4 CPU, integrated with FPU, MPU, DSP supporting SIMD instructions, and CoreSight standard debug unit. The highest operating frequency 120MHz can reach 150DMIPS or 408Coremarks computing performance
- Built-in memory
  - Up to 128KB Code Flash Memory
  - Up to 16KB single-cycle access high-speed SRAM
- Power, clock, and reset management
  - System power supply (V_{CC}): 2.7-5.5V
  - 5 independent clock sources: XTAL (4-24MHz); HRC (12MHz); MRC (8MHz); LRC (32.768kHz); PLL
  - 12 reset sources: including POR, PVD1R/PVD2R, NRST, etc. Each with an independent flag bit
- Low-power operation
  - Peripheral functions can be independently disabled or enabled
  - 2 low-power modes: Sleep mode, Stop mode
- Peripheral operation support system significantly reduces CPU processing load
  - 4-channel DMAC
  - 1 data calculation unit (DCU)
  - 1 math acceleration unit (MAU)
  - Supports action on signal (AOS) for peripheral events
- High-performance analog
  - 1 independent 12-bit 3.6Msps ADC
  - 1 independent 12-bit DAC (output only used for CMP negative terminal reference voltage input)
  - 3 independent voltage comparators (CMP)
  - 3 independent operational amplifiers (OPA)
- Timers
  - 1 16-bit motor PWM timer (Timer4)
  - 5 16-bit general-purpose timers (TimerA)
  - 2 16-bit basic timers (Timer0)
  - 2 WDTs
- Up to 52 GPIOs
- Up to six communication interfaces
  - 4 USARTs, supporting ISO7816-3, LIN protocol
  - 1 SPI
  - 1 I2C, supporting SMBus
- Other functions: CRC16/32/64
- Package: LQFP64/48/32

Support Model

HC32F431KATB-LQFP64	HC32F431JATB-LQFP48
HC32F431FATB-LQFP32	-

Statement

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Preface

Number Format

- 0x prefix is used for hexadecimal numbers
- 0b prefix is used for binary numbers
- Numbers without prefix are in decimal representation

Security Statement

There may be potential security problems due to the use of a certain function or protocol, which need to be declared to remind users and avoid security risks.

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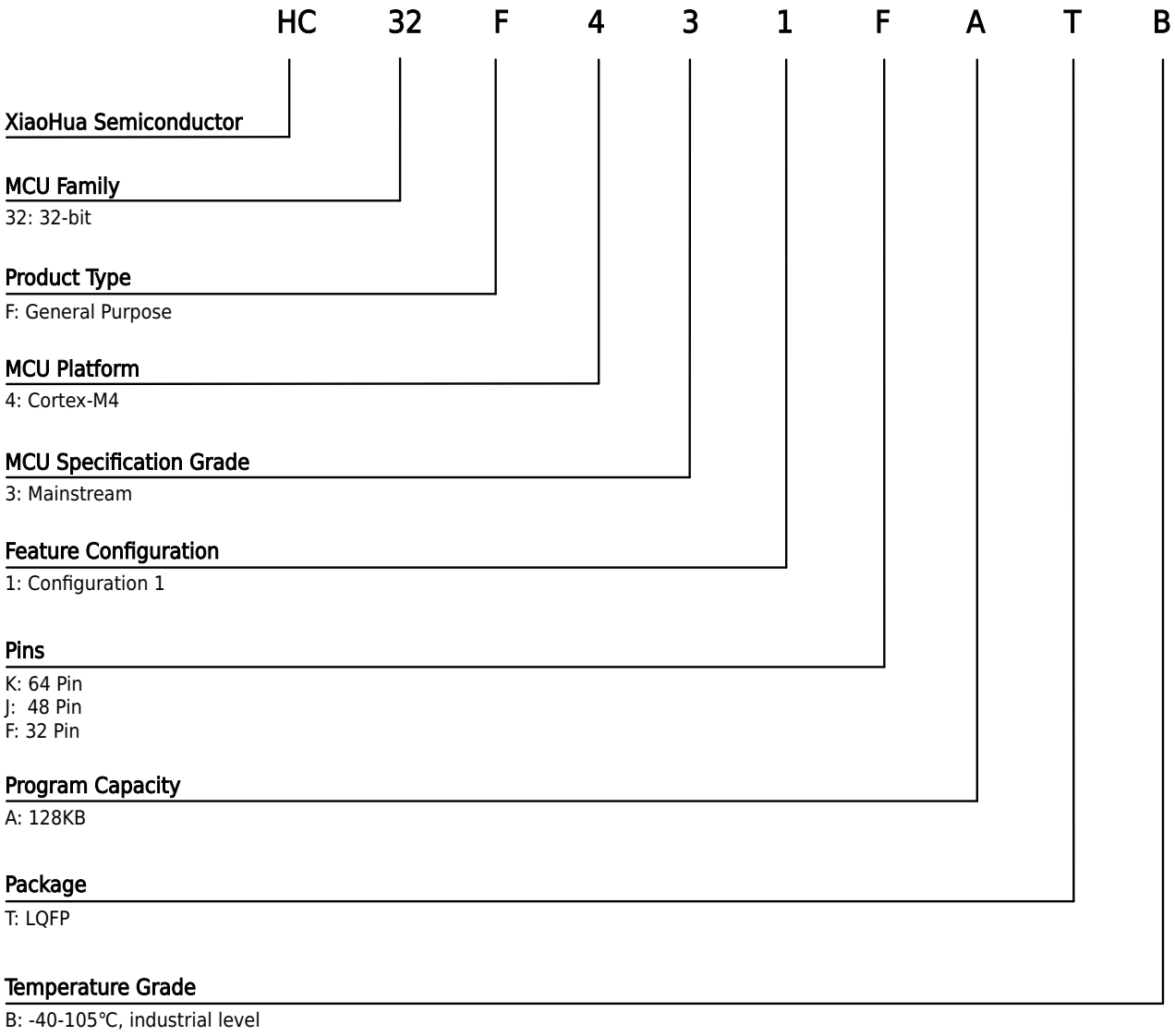
1 Product Overview

1.1 Product Lineup

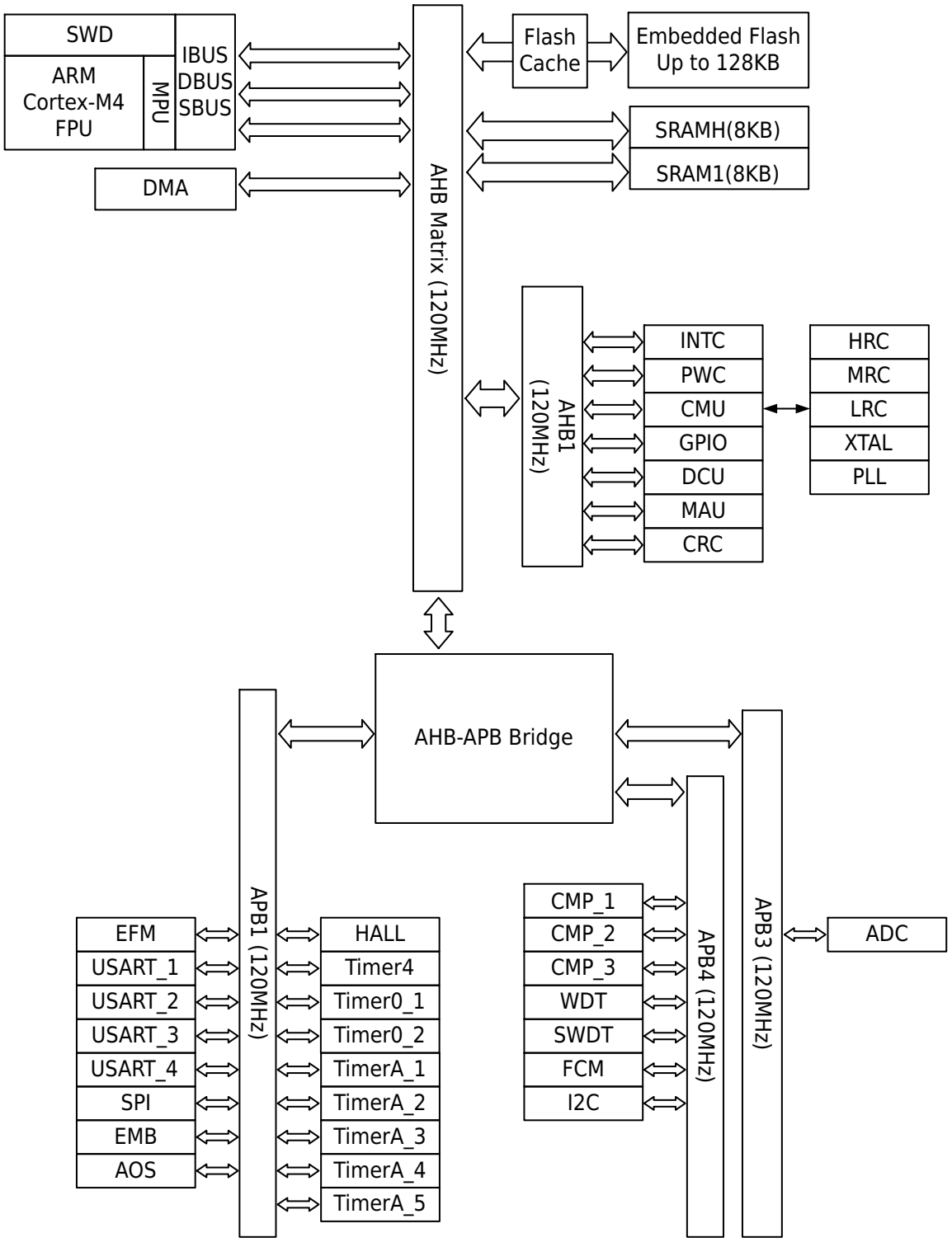
Product Name



Model Function Comparison Table

Product Name		HC32F431FATB	HC32F431JATB	HC32F431KATB
Pins		32	48	64
GPIOs		24	40	52
CPU	Core	Cortex-M4		
	Frequency	120MHz		
Storage Space	Flash	128KB		
	SRAM	16KB		
Clock	HRC	12MHz		
	MRC	8MHz		
	LRC	32.768kHz		
	XTAL	4-24MHz		
Supply Voltage Range		2.7-5.5V		
Temperature Range		-40-105℃		
External Port Interrupt		EIRQ * 8		
DMA Controller		1unit * 4ch		
Timer and Counter	Timer0	2unit		
	TimerA	5unit		
	Timer4	1unit		
	WDT	1ch		
	SWDT	1ch		
Connectivity	USART	4ch		
	I2C	1ch		
	SPI	1ch		
Analog	12-bit ADC	1unit, 6ch	1unit, 14ch	1unit, 16ch
	12-bit DAC	1ch (Only used for CMP negative input reference voltage)		
	CMP	3ch		
	OPA	1ch	3ch	3ch
	PVD	√		
Co-processing	DCU	√		
	MAU	√		
FCM		√		
HALL		√		
CRC		√		
Debugging Interface	SWD	√		
	TOOL0	√		
Package		LQFP		

1.2 Functional Block Diagram



Note

Products in different packages support varying resources. For detailed specifications, please refer to Model Function Comparison Table.

2 Functional Description

2.1 CPU

HC32F431 Series integrates embedded ARM® Cortex-M4 with FPU 32-bit simplified command CPU, which realizes less pins and low power consumption, and provides excellent computing performance and rapid interrupt response capability. The on-chip integrated storage capacity can give full play to the excellent command efficiency of ARM® Cortex-M4. The CPU supports DSP command, which can realize efficient signal processing operations and complex algorithms. Single-point precision FPU (Floating Point Unit) can avoid command saturation and speed up software development.

2.2 BUS

The main system consists of a 32-bit multi-layer AHB bus matrix, enabling the interconnection of the following host buses and slave buses:

- Host bus
  - Cortex-M4 core CPU-I bus, CPU-D bus, CPU-S bus
  - System DMA bus
- Slave bus
  - Code Flash ICODE bus
  - Code Flash DCODE bus
  - Code Flash MCODE bus (The bus for accessing Code Flash by components other than the CPU on the host)
  - System SRAMH (SRAMH 8KB) bus
  - System SRAM (SRAM1 8KB) bus
  - APB1 peripheral bus (AOS/EMB/Timer0/Timer4/TimerA/SPI/USART/EFM/HALL)
  - APB3 peripheral bus (ADC)
  - APB4 peripheral bus (FCM/WDT/SWDT/CMP/I2C)
  - AHB1 peripheral bus (INTC/DCU/GPIO/DMA/FCG/CMU/PWC/MAU/CRC)

With the bus matrix, efficient concurrent access from host buses to slave buses can be achieved.

2.3 RMU

The chip is configured with 12 reset modes:

- Power-on Reset (POR)
- NRST Pin Reset (NRST)
- Brown-out Reset (BOR)
- Programmable Voltage Detection 1 Reset (PVD1R)
- Programmable Voltage Detection 2 Reset (PVD2R)
- Watchdog Reset (WDTR)
- Special Watchdog Reset (SWDTR)
- Software Reset (SRST)
- RAM Parity Reset (RAMPR)
- Clock Frequency Error Reset (CKFER)

- XTAL Error Reset (XTALER)
- Cortex-M4 Lockup Reset (LKUPR)

2.4 CMU

The clock control unit provides a series of clock functions with different frequencies, including: an external high-speed oscillator, one PLL clock, an internal high-speed oscillator, an internal medium-speed oscillator, an internal low-speed oscillator, a clock prescaler, clock multiplexing, and clock gating circuit.

The clock control unit also provides a clock frequency measurement function. The clock frequency measurement circuit (FCM) monitors and measures the measurement target clock using the measurement reference clock. An interrupt or reset occurs when the setting range is exceeded.

AHB, APB, and Cortex-M4 clocks are derived from the System Clock. The maximum operating clock frequency of the System Clock can reach 120MHz, with 5 selectable clock sources:

1. External High-speed Oscillator (XTAL)
2. PLL Clock (PLL)
3. Internal High-speed Oscillator (HRC)
4. Internal Medium-speed Oscillator (MRC)
5. Internal Low-speed Oscillator (LRC)

For each clock source, it can be individually turned on and off when not in use to reduce power consumption. SWDT uses the internal low-speed oscillator as its counting clock source.

2.5 PWC

Power controller is used to control the supply, switching and detection in run modes and low power modes. The power controller consists of a power consumption control logic (PWCL), a power supply voltage detection unit (PVD).

The operating voltage (VCC) of the chip is 2.7V to 5.5V. The voltage regulator (LDO) supplies power to the VDD domain. The chip provides two low-power modes: SLEEP mode and STOP mode through the power consumption control logic (PWCL).

The power voltage detection unit (PVD) provides functions such as power on reset (POR), power down reset (PDR), brown out reset (BOR), programmable voltage detection 1 (PVD1), programmable voltage detection 2 (PVD2). Among them, POR, PDR, and BOR control the chip reset action by detecting the VCC voltage. PVD1 detects the VCC voltage and resets or interrupts the chip according to the register settings. PVD2 detects VCC voltage or external input detection voltage, and generates reset or interrupt according to register selection.

The analog blocks are equipped with dedicated supply pins for improved analog performance.

2.6 ICG

After the chip's reset is released, the hardware circuit reads data from FLASH addresses 0x00020000-0x00020010 and loads it into the Initialization Configuration (ICG) register. Users can modify the ICG register by programming or erasing the corresponding FLASH addresses of the sectors. Addresses 0x00020018-0x0002001F are the data security protection enable region. The register reset value is determined by FLASH data.

2.7 EFM

The Flash interface accesses Flash through the ICODE, DCODE, and MCODE buses. The interface can perform programming, erasing and full erasing operations on Flash. Besides, it can accelerate code execution through caching mechanisms.

Main Features:

- Two independent cache areas: ICODE bus cache space 1KBytes (128x64); DCODE bus cache space 64Bytes (8x64)
- Supports proprietary code read protection (PCROP) function
- Supports Flash data CRC check function
- Support data security protection

2.8 SRAM

This product has 16KB system SRAM (SRAMH/SRAM1).

Each SRAM can be accessed as a byte, half-word (16 bits), or full-word (32 bits). All SRAM read and write operations can be performed at the fastest CPU speed (120MHz) with 0 wait period (i.e., in 1 clock cycle).

SRAM1 and SRAMH have a parity check, with one check bit for each byte of data. When the RAM parity check reset function is enabled, an SRAM parity check reset will be generated if a parity error occurs during the reading of SRAM data.

2.9 GPIO

Main features of GPIO:

- Each port group has 8 I/O pins, which may be less than 8 depending on actual configuration
- Supports pull-up input
- Supports push-pull, open-drain output mode
- Supports high and low drive modes
- Supports free switching between CMOS/Schmitt input modes
- Supports for external interrupt input
- Supports I/O pin peripheral function multiplexing, one I/O pin can have up to 10 optional multiplexing functions
- Individual I/O pins can be programmed independently

2.10 INTC

The interrupt controller (INTC) selects an interrupt event as an interrupt request and sends it to NVIC to wake up WFI; selects interrupt event as event input (RXEV) to wake up WFE; select low power consumption mode (Sleep mode and Stop mode) of interrupt event wake-up system ; control external interrupts and software interrupts.

The main features of INTC are as follows:

1. Maskable interrupts: INTC is equipped with 124 interrupt events, which are processed and sent to NVIC as interrupt requests (IRQ). It supports 74 IRQs, each IRQ corresponds to one or more interrupt events.

> **Note**
> For more instructions on exception and NVIC programming, please refer to the "Arm Cortex-M4 Processor Technical Reference Manual".

2. Programmable priority of NVIC: 16 programmable priorities (4-bit interrupt priority register is used).
3. Non-maskable interrupts: Multiple system interrupt event requests can be independently selected as non-maskable interrupts, and each interrupt event is equipped with independent enable, flag and flag clear registers.
4. Equipped with 8 external pin interrupt events.
5. Equipped with multiple interrupt events, please refer to the "Interrupt Event List" in the "Interrupt Controller (INTC)" chapter of "Reference Manual" for the specific number.
6. Equipped with 24 software interrupt events.
7. Interrupt wakes up system Sleep mode and Stop mode.

2.11 AOS

The Automatic Operation System (AOS) is used to achieve coordination between peripherals without the assistance of the CPU. It utilizes events generated by peripherals as AOS sources, such as timer comparison matches, timer counting overflow, various states of the sending and receiving data of the communication module (idle, receive data full, transmit data end, transmit data empty), ADC conversion end events, etc., to trigger actions of other peripherals. The triggered peripheral actions are referred to as AOS targets.

Users can select one or more AOS sources to trigger the same AOS target based on their needs.

2.12 DMA

DMA is used to transfer data between memory and peripheral function modules, enabling data exchange between memories, between memory and peripheral function modules, and between peripheral function modules without CPU involvement.

Main features of DMA:

- The DMA bus is independent of the CPU bus and transmits data according to the AMBA AHB-Lite bus protocol
- With 1 DMA control units, a total of 4 independent channels, which can independently operate different DMA transfer functions
- The start source of each channel is configured through an independent trigger source selection register
- 1 block per request
- The data block is a minimum of one data and can be up to 1024 data
- The width of each data item can be configured as 8-bit, 16-bit, or 32-bit
- It can be configured for 1-65535 transfers or infinite transfers
- The source address and destination address can be independently configured as fixed, incrementing, decrementing, repeated jump, or specified offset jump
- 3 types of interrupts can be generated: block transfer completed interrupt, transfer completed interrupt, and transfer error interrupt. Each interrupt can be configured to be masked or unmasked. Among them, block transfer completed and transfer completed can be used as event outputs, serving as trigger sources for other peripheral modules
- Support chain transfer function, enabling the transfer of multiple data blocks in a single request

- Support channel reset triggered by external events
- Support software-triggered start of transfer and software-triggered channel reset
- When not in use, it can be set to stop state to reduce power consumption

2.13 CMP

Voltage Comparator (hereinafter referred to as CMP) is a peripheral module that compares two analog voltages and outputs the comparison result. This product is equipped with two groups of 3 comparison channels: CMP1 and CMP2, and CMP3.

CMP Main features:

- 3 comparison channels can independently perform normal comparison
- The combination of CMP1 and CMP2 can implement the window comparison function
- Each comparison channel's positive and negative voltage inputs have multiple input sources (IO, DAC) to choose from
- Hysteresis voltage is configurable
- A noise filter can filter the comparator output, with 7 sampling clocks to choose from
- Timer PWM can be used for comparator blanking window control
- Interrupts can be generated at the edges of comparison result changes, other peripherals can be triggered, and STOP mode can be woken up
- Compare results can be monitored through registers and output to the external pin VCOUT
- Compare results can be used for EMB control events

2.14 ADC

The 12-bit ADC is an analog-to-digital converter that adopts the successive approximation method. This MCU is equipped with 1 ADC units, a maximum of 16 channels, which can convert analog signals from external pins. Analog input channels can be arbitrarily combined into a sequence for single scan or continuous scan conversion. Supports continuous multiple conversions on any specified channel and averaging of the conversion results. The ADC block also includes an analog watchdog function that monitors the conversion results of any specified channel to detect if they exceed user-set ranges.

The main features of the ADC are as follows:

- High Performance
  - 12-bit resolution
  - The clock source of the ADC sampling conversion clock ADCLK is PCLK4 (set by the CMU_ADCKSEL register)
  - Sampling Rate: 3.6Msps (ADCLK=80MHz, 12-bit, 8 sampling cycles, 14 conversion cycles)
  - Independent programming of channel sampling time is supported
  - Each channel has an independent data register
  - Data registers can be configured for left/right alignment
  - Continuous multiple conversion averaging function
  - Oversampling function
  - Analog watchdog to monitor conversion results
  - The ADC module can be set to stop when not in use
- Analog Input Channel
  - Total of 16 external analog inputs

- Conversion Start Conditions
  - Software setup conversion started
  - Peripheral synchronously trigger the conversion to start
  - External pin trigger the conversion to start
- Conversion Mode
  - 3 scan sequences A, B, C, optionally specifying a single or multiple channels
  - Sequence A single scan
  - Sequence A continuous scan
  - Dual sequence scan, with sequences A and B independently selecting trigger sources, and sequence B having higher priority than A
  - Triple sequence scan, with sequences A, B, and C independently selecting trigger sources, sequence C having higher priority than B, and sequence B having higher priority than A.
- Interrupt and Event Signal Output
  - Sequence A scan end interrupt and event ADC_EOCA
  - Sequence B scan end interrupt and event ADC_EOCB
  - Sequence C scan end interrupt and event ADC_EOCC
  - Analog watchdog 0 compare interrupt and event ADC_CMP0
  - Analog watchdog 1 compare interrupt and event ADC_CMP1
  - All the event outputs mentioned above can start DMA

2.15 DAC

This MCU is equipped with 1 12-bit digital-to-analog converter (DAC) unit. DAC unit includes 1 DAC conversion channel. The analog voltage output range has two selectable settings.

DAC Main features:

- 1 DAC conversion channel
- The output can be used as the negative-end voltage for the voltage comparator (CMP)

2.16 Timer4

The General Control Timer 4 is a timer module designed for three-phase motor control, offering a variety of solutions for different three-phase motor control applications. It supports both triangular and sawtooth waveform modes, enabling the generation of various PWM waveforms. It also features buffer functionality and supports EMB control. 1 unit of Timer4 is carried in this product family.

2.17 EMB

The emergency brake module is a function module that generates contorl events output to the timer when certain conditions are met to stop the timer or change the PWM signal output to the external motor. The following factors are used to generate control events:

- External port input level change
- Level of Timer4 PWM output port occurs in phase (same high or same low)
- Voltage comparator comparison results
- XTAL stops oscillating
- Write register software control

2.18 TimerA

The General Timer A (TimerA) is a timer with a 16-bit counting width and 2/6-channel PWM output. The timer supports two waveform modes, triangle wave and sawtooth wave, and can generate various PWM waveforms (single-side aligned PWM, double-side symmetrical PWM); supports synchronous start of counter; the compare reference value register supports buffer function; supports cascading between units to achieve 32-bit counting; supports 2-phase quadrature encoding count and 3-phase quadrature encoding count. This product series is equipped with 5 TimerA units, Unit 1 (TimerA_1) to Unit 4 (TimerA_4) each have 2 channels of PWM output, Unit 5 (TimerA_5) has 6 channels of PWM output. The 5 units can achieve a maximum of 14 channels of PWM output in total.

2.19 Timer0

General Timer 0 (Timer0) is a basic timer that can realize synchronous counting and asynchronous counting. The timer contains two channels (CH-A and CH-B) that can generate compare match events and count overflow events during counting. This event can trigger an interrupt and can be used to trigger other module actions. This series of products is equipped with 2 units of Timer0.

2.20 WDT/SWDT

This product has two watchdog counters: one is a dedicated watchdog counter (SWDT) with an internal RC (32.768kHz) as its count clock source, and the other is a general-purpose watchdog counter (WDT) with PCLK3 as its count clock source. Both the dedicated watchdog and the general-purpose watchdog are 16-bit down counters used to monitor software faults caused by external interference or unforeseen logic conditions that cause the application to deviate from normal operation.

Both watchdogs support the window function. The window interval can be preset before the count starts, and when the count value is within the window interval, the counter can be refreshed and the count restarted.

2.21 HALL

The Hall Signal Processing Module (HALL) features a 32-bit counting width and 3-channel HALL signal input. It supports digital filtering for the 3-channel HALL signal input.

- Hall signal change capture
- Digital filtering of Hall input signals
- Capture and overflow event output

2.22 USART

This product is equipped with 4 units of Universal Synchronous Asynchronous Receiver/Transmitter (USART) modules, which can flexibly exchange full-duplex data with external devices; the USART equipped in this product supports universal asynchronous serial communication interface (UART) , clock synchronous communication interface, smart card interface (ISO/IEC7816-3) and LIN communication interface. Support modem operation (CTS/RTS operation), multiprocessor operation, DE function, receive timeout function. USART1 supports the STOP mode wake-up function via the RX line.

The specific function allocation is as follows:

Function	Support Module			
	USART1	USART2	USART3	USART4
UART	✓	✓	✓	✓

Function	Support Module			
	USART1	USART2	USART3	USART4
Multiprocessor Communication	✓	✓	✓	✓
Clock Synchronization Communication	✓	✓	✓	✓
Wake-up from STOP Mode via RX Line	✓	-	-	-
Fractional Baud Rate	✓	✓	✓	✓
LIN	-	✓	✓	✓
Smart Card	✓	-	-	-
UART Receive Timeout Function	✓	✓	✓	✓
RS485 Driver Enable	✓	✓	✓	✓

2.23 I2C

I2C (Inter-Integrated Circuit) used as an interface between the microcontroller and the I2C serial bus. Provide multi-master mode function, which can control the protocol and arbitration of all I2C buses. Standard mode and fast mode are supported. SMBus is also supported.

Main features of I2C:

- I2C bus mode and SMBUS bus mode are optional. Master mode and slave mode are optional. Automatically ensure various preparation times, hold times, and bus idle times corresponding to the transfer rate
- Standard mode up to 100kbps, fast mode up to 400kbps
- The start condition, restart condition, and stop condition are automatically generated, and the start condition, restart condition, and stop condition of the bus can be detected
- Supports up to 128 slave mode addresses. Supports 7-bit address format and 10-bit address format. Broadcast call address, SMBus host address, SMBus device default address, SMBus alarm address can be detected
- Answer bits can be automatically determined when sent. Answer bits can be automatically sent when reception
- Handshake function
- Arbitration function
- Timeout function, can detect SCL clock stop for a long time
- SCL input and SDA input have built-in digital filters that are programmable to filter
- Communication error, receive data full, send data empty, one frame send end, address match unanimously interrupt
- 2-stage transmit FIFO and 2-stage receive FIFO

2.24 SPI

This product is equipped with 1-channel serial peripheral interface SPI, supports high-speed full-duplex serial synchronous transmission, and facilitates data exchange with peripheral devices. Users can set the range of 3/4-wire, master/slave and baud rate as required.

Table 2-2 SPI Main Features

Essentials	Description
Serial Communication Function	● Supporting 4-wire SPI mode and 3-wire clock synchronization mode ● Supports full-duplex synchronous communication mode and transmit-only communication mode ● Polarity and phase of adjustable communication clock SCK
Data Format	● Selectable data shift order: MSB start/LSB start ● Selectable data width: 4/5/6/7/8/9/10/11/12/13/14/15/16/20/24/32 bits ● A maximum of 4 frames width of 32-bit data can be transmitted or received at a single time
Baud Rate	● The baud rate can be adjusted by the built-in special baud rate generator in master mode. The baud rate ranges from 2 to 256 frequency division of PCLK1. ● Maximum baud rate allowed in slave mode is 6 frequency division of PCLK1
Data Buffer	● With 16-byte data buffer ● Supports double buffering
Error Monitoring	● Mode fault error monitoring ● Data overload error monitoring ● Data underload error monitoring ● Parity error monitoring
Chip Selection Signal Control	● Each channel is configured with 4 chip-selected signal line ● The relative timing relationship between the chip select signal and the communication clock can be adjusted ● The inactive time of the chip select signal between two consecutive communications can be adjusted ● Polarity adjustable
Transmission Control in Master Mode	● Start transmission by writing data to the data register ● Communication auto suspend function
Interrupt	● Receive buffer is full ● Transmit buffer is empty ● SPI error (mode/overload/underload/parity) ● SPI vacant ● Transmit complete (event source only)
Low Power Control	● Configurable module stop
Other Functions	● SPI initialization function

2.25 CRC

The CRC algorithm of this module follows the definition of ISO/IEC13239, and adopts 16-bit CRC, 32-bit CRC and 64-bit CRC respectively. It supports 11 kinds of polynomial counting, which are CRC16/CCITT, CRC16/CCITT-FALSE, CRC16/XMODE, CRC16/IBM, CRC16/MAXIM, CRC16/USB, CRC16/MODBUS, CRC16/X25, CRC32, CRC32/MPEG-2 and CRC64.

2.26 DCU

The Data Computing Unit (DCU) is a simple data processing block that does not rely on the CPU. Each DCU unit has three data registers capable of performing addition, subtraction, comparison, and window comparison functions on two data values. This product is equipped with 1 DCU unit.

2.27 MAU

The Math Arithmetical Unit (MAU) is a hardware-accelerated computing module that includes three types of operations: square root, sine, and arctangent. It supports square root, sine, and arctangent operations for fixed-point numbers. The sine function supports an operation precision of $360°/2^{12}$.

2.28 DBGC

This MCU's core is Cortex-M4, which includes hardware for advanced debugging functions. Using these debugging functions, the core can be stopped when fetching instructions (instruction breakpoint) or accessing data (data breakpoint). When the core is stopped, the internal state of the core and the external state of the system can be queried. After the query completes, the kernel and system are restored and program execution is restored.

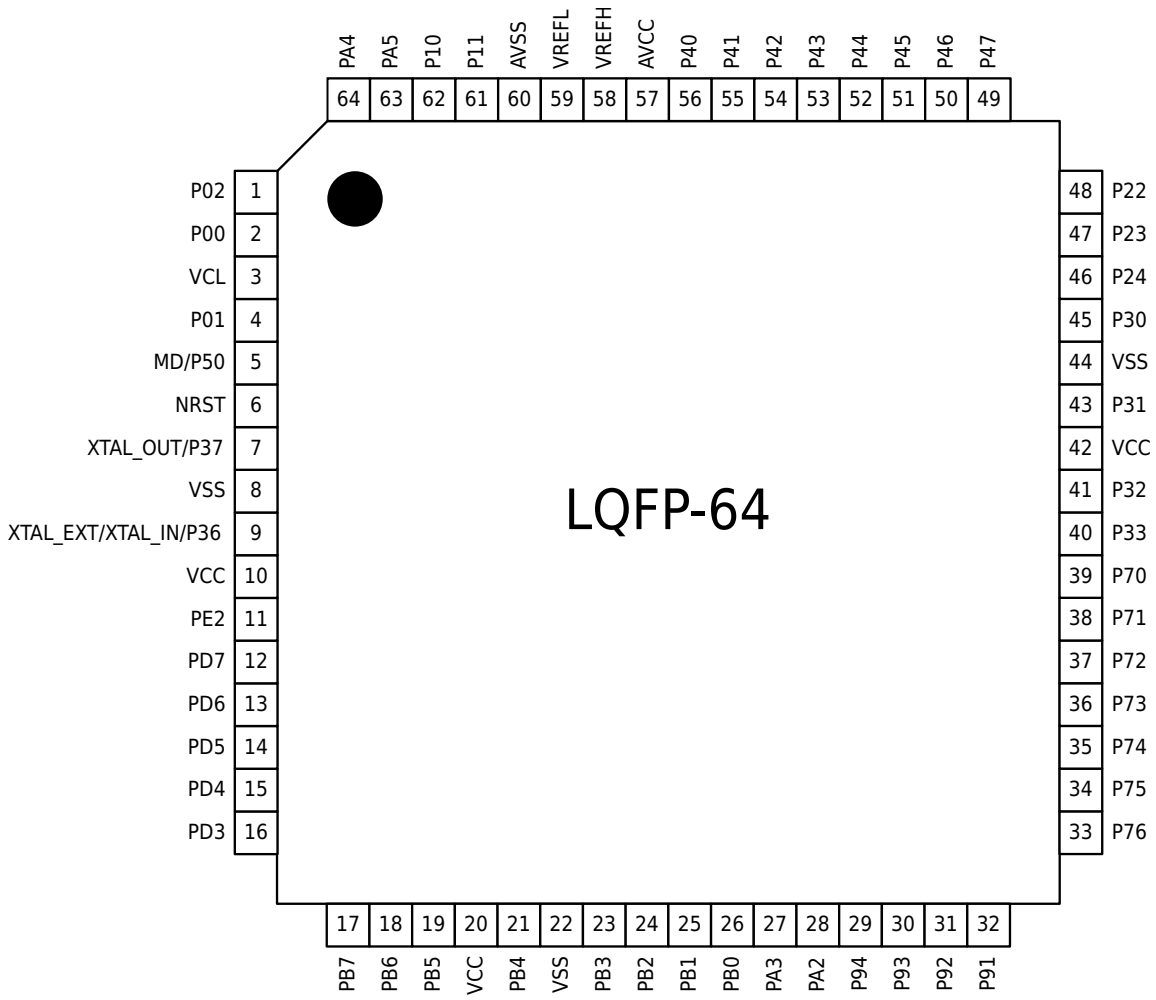
Debugging interface supported:

- Serial debug trace interface SWD
- Single-wire serial debug interface TOOL0

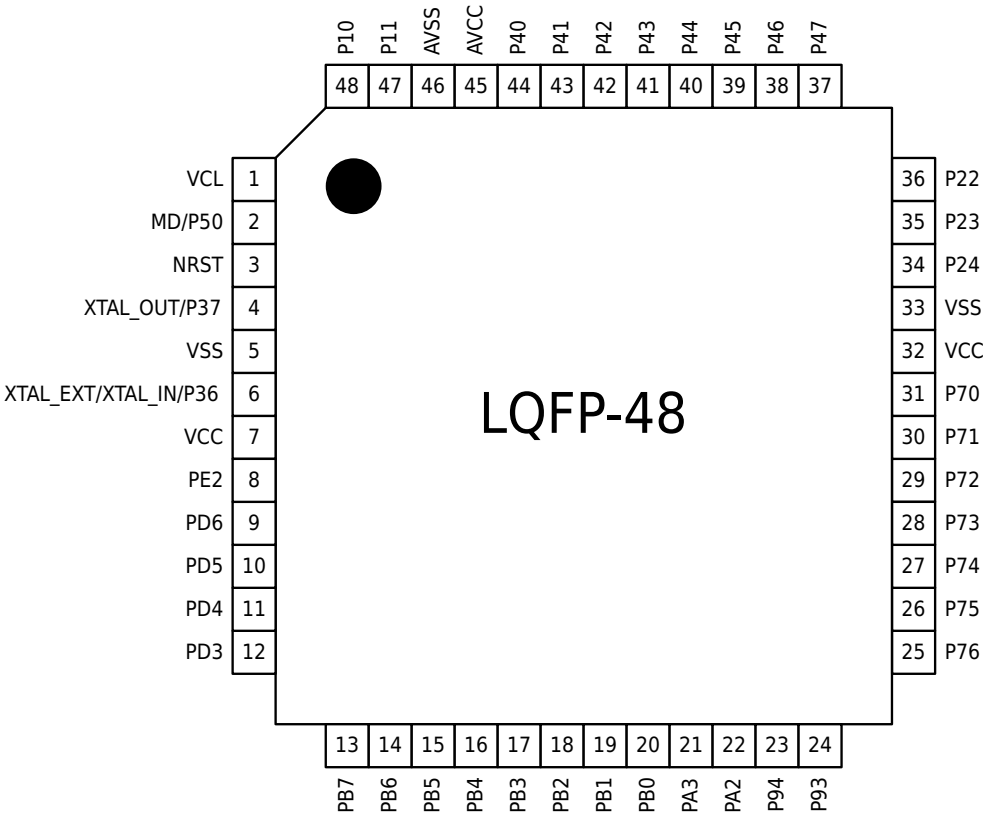
3 Pin Definitions

3.1 Pinout

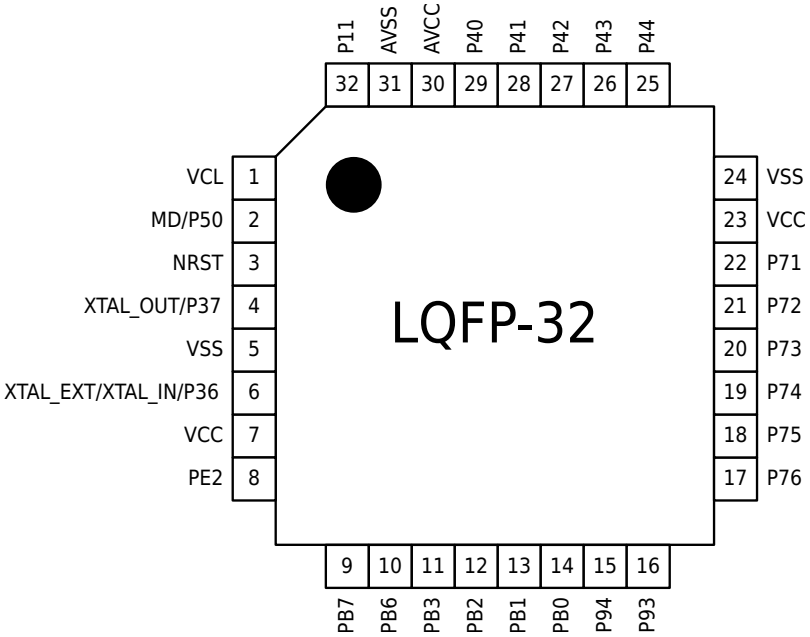
3.1.1 LQFP64 Package



3.1.2 LQFP48 Package



3.1.3 LQFP32 Package



3.2 Pin Function Table

LQFP64	LQFP48	LQFP32	Pin Name	Analog	EIRQ	SWD/TOOL0	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9
							GPO	other	EMB/FCM/TMR4	TMRA	TMRA/HALL	USART	SPI	TMRA	I2C/USART	USART
1	-	-	P02		EIRQ5			ADST	TMR4_ADSM	TMRA_5_PWM1/ TMRA_5_CLKA		USART1_CTS	SPI_NSS0			USART1_RTS_DE
2	-	-	P00	PVD2EXINP	EIRQ2				EMB_IN3			USART3_CTS				USART3_RTS_DE
3	1	1	VCL	REGC												
4	-	-	P01		EIRQ4				FCMREF	TMRA_5_PWM2/ TMRA_5_CLKB						
5	2	2	P50/MD			TOOL0						USART4_TX				USART4_RX
6	3	3	NRST													
7	4	4	P37	XTAL_OUT												
8	5	5	VSS													
9	6	6	P36	XTAL_IN				EXTAL								
10	7	7	VCC													
11	8	8	PE2		NMI/EIRQ0				EMB_IN3			USART1_CK				
12	-	-	PD7		EIRQ7							USART4_RX	SPI_NSS1	TMRA_1_TRIG		
13	9	-	PD6		EIRQ5			ADST		TMRA_5_PWM4	HALL_A	USART1_CTS	SPI_NSS0	TMRA_1_PWM2/ TMRA_1_CLKB		USART1_RTS_DE
14	10	-	PD5		EIRQ3					TMRA_5_PWM3	HALL_B	USART1_RX	SPI_MISO	TMRA_1_TRIG	I2C_SCL	
15	11	-	PD4		EIRQ2					TMRA_5_PWM2/ TMRA_5_CLKB	HALL_C	USART1_CK	SPI_SCK	TMRA_1_PWM1/ TMRA_1_CLKA		
16	12	-	PD3		EIRQ6			MCO		TMRA_5_PWM1/ TMRA_5_CLKA	TMRA_3_TRIG	USART1_TX	SPI_MOSI	TMRA_1_PWM1/ TMRA_1_CLKA	I2C_SDA	
17	13	9	PB7		EIRQ5					TMRA_5_PWM3	TMRA_4_PWM2/ TMRA_4_CLKB	USART2_CK	SPI_SCK	TMRA_1_PWM2/ TMRA_1_CLKB	I2C_SCL	USART1_RX
18	14	10	PB6		EIRQ5			MCO	TMR4_ADSM	TMRA_5_PWM1/ TMRA_5_CLKA	TMRA_3_PWM2/ TMRA_3_CLKB	USART2_RX	SPI_MISO	TMRA_1_PWM2/ TMRA_1_CLKB	I2C_SCL	USART1_TX
19	15	-	PB5		EIRQ6			ADTRG			TMRA_4_TRIG	USART2_TX	SPI_MOSI	TMRA_2_PWM2/ TMRA_2_CLKB	I2C_SDA	
20	-	-	VCC													
21	16	-	PB4		EIRQ3			ADTRG	EMB_IN2	TMRA_5_TRIG		USART4_CK		TMRA_1_PWM2/ TMRA_1_CLKB		
22	-	-	VSS													
23	17	11	PB3		EIRQ7			VCOUT	FCMREF	TMRA_5_PWM1/ TMRA_5_CLKA	TMRA_4_TRIG	USART2_CK	SPI_SCK	TMRA_2_TRIG		USART4_CK
24	18	12	PB2		EIRQ6	SWDIO		MCO	TMR4_ADSM	TMRA_5_PWM2/ TMRA_5_CLKB	TMRA_4_PWM1/ TMRA_4_CLKA	USART2_TX	SPI_MOSI	TMRA_2_PWM2/ TMRA_2_CLKB	I2C_SDA	
25	19	13	PB1		EIRQ2	SWCLK			EMB_IN2	TMRA_5_PWM3	TMRA_3_PWM1/ TMRA_3_CLKA	USART2_RX	SPI_MISO	TMRA_5_PWM4	I2C_SCL	
26	20	14	PB0		EIRQ0			VCOUT1		TMRA_5_PWM4	TMRA_4_PWM1/ TMRA_4_CLKA	USART4_TX	SPI_MOSI	TMRA_1_PWM1/ TMRA_1_CLKA	I2C_SDA	
27	21	-	PA3	OPA3P	EIRQ3					TMRA_3_PWM2/ TMRA_3_CLKB	TMRA_4_PWM1/ TMRA_4_CLKA	USART4_CTS	SPI_NSS0	TMRA_2_PWM1/ TMRA_2_CLKA		USART4_RTS_DE
28	22	-	PA2	OPA3N	EIRQ4			VCOUT3	USART3_RTS_DE	TMRA_3_PWM1/ TMRA_3_CLKA	TMRA_4_PWM2/ TMRA_4_CLKB	USART2_CTS	SPI_NSS1	TMRA_2_PWM1/ TMRA_2_CLKA	USART3_CTS	USART2_RTS_DE
29	23	15	P94	OPA1P	EIRQ1			VCOUT2	FCMREF	TMRA_5_PWM3	TMRA_4_PWM2/ TMRA_4_CLKB	USART4_RX	SPI_MISO	TMRA_1_PWM2/ TMRA_1_CLKB	I2C_SCL	
30	24	16	P93	OPA1N	EIRQ0			ADTRG		TMRA_5_PWM2/ TMRA_5_CLKB	TMRA_3_PWM1/ TMRA_3_CLKA	USART2_CK	SPI_SCK	TMRA_1_TRIG		USART4_CK
31	-	-	P92		EIRQ1					TMRA_5_PWM6	TMRA_4_PWM1/ TMRA_4_CLKA		SPI_NSS2	TMRA_1_PWM2/ TMRA_1_CLKB		
32	-	-	P91		EIRQ0				TMR4_OXL	TMRA_5_PWM5		USART4_CTS	SPI_NSS3	TMRA_1_PWM2/ TMRA_1_CLKB		USART4_RTS_DE
33	25	17	P76		EIRQ6				TMR4_OWL	TMRA_5_PWM4	TMRA_3_TRIG	USART1_CTS			I2C_SDA	USART1_RTS_DE
34	26	18	P75		EIRQ7				TMR4_OVL	TMRA_5_PWM3	TMRA_3_TRIG	USART2_CTS			I2C_SCL	USART2_RTS_DE
35	27	19	P74		EIRQ4				TMR4_OUL	TMRA_5_PWM4	TMRA_3_PWM1/ TMRA_3_CLKA	USART3_CTS				USART3_RTS_DE
36	28	20	P73		EIRQ3			VCOUT	TMR4_OWH	TMRA_5_PWM3	TMRA_3_PWM2/ TMRA_3_CLKB	USART3_CK				
37	29	21	P72		EIRQ2				TMR4_OVH	TMRA_5_PWM1/ TMRA_5_CLKA	TMRA_3_PWM2/ TMRA_3_CLKB	USART3_TX				
38	30	22	P71		EIRQ1				TMR4_OUH	TMRA_5_PWM2/ TMRA_5_CLKB	TMRA_3_PWM1/ TMRA_3_CLKA	USART3_RX				
39	31	-	P70	ADC_IN15	EIRQ5			MCO	EMB_IN1	TMRA_5_PWM6		USART4_TX				
40	-	-	P33		EIRQ7				TMR4_OXH	TMRA_5_PWM1/ TMRA_5_CLKA	TMRA_3_PWM1/ TMRA_3_CLKA	USART4_RX	SPI_NSS3			
41	-	-	P32		EIRQ6				TMR4_PCT	TMRA_5_PWM3	TMRA_3_PWM2/ TMRA_3_CLKB		SPI_NSS2			
42	32	23	VCC													
43	-	-	P31		EIRQ1					TMRA_5_PWM1/ TMRA_5_CLKA	TMRA_4_PWM1/ TMRA_4_CLKA		SPI_NSS1			
44	33	24	VSS													
45	-	-	P30		EIRQ0					TMRA_5_PWM2/ TMRA_5_CLKB	TMRA_4_PWM2/ TMRA_4_CLKB	USART4_CK	SPI_NSS0	TMRA_2_PWM2/ TMRA_2_CLKB		

LQFP64	LQFP48	LQFP32	Pin Name	Analog	EIRQ	SWD/TOOL0	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9
							GPO	other	EMB/FCM/TMR4	TMRA	TMRA/HALL	USART	SPI	TMRA	I2C/USART	USART
46	34	-	P24	ADC_IN14	EIRQ3			VCOUT1	TMR4_CLK	TMRA_5_PWM6		USART3_RX	SPI_MISO	TMRA_2_PWM1/ TMRA_2_CLKA	I2C_SCL	
47	35	-	P23	ADC_IN13/OPA2P	EIRQ4			VCOUT2	FCMREF	TMRA_5_PWM5		USART3_TX	SPI_MOSI	TMRA_2_PWM1/ TMRA_2_CLKA	I2C_SDA	
48	36	-	P22	ADC_IN12/OPA2N	EIRQ2			VCOUT3	EMB_IN1	TMRA_5_PWM4		USART3_CK	SPI_SCK	TMRA_2_TRIG		
49	37	-	P47	ADC_IN7/CMP2_INP3/ CMP3_INP3/OPA2O												
50	38	-	P46	ADC_IN6/CMP1_INP3/ OPA3O												
51	39	-	P45	ADC_IN5/CMP3_INP2												
52	40	25	P44	ADC_IN4/CMP2_INP2/ OPA1O												
53	41	26	P43	ADC_IN3/CMP1_INP2												
54	42	27	P42	ADC_IN2/CMP3_INP1							HALL_A					
55	43	28	P41	ADC_IN1/CMP2_INP1							HALL_B					
56	44	29	P40	ADC_IN0/CMP1_INP1							HALL_C					
57	45	30	AVCC													
58	-	-	VREFH													
59	-	-	VREFL													
60	46	31	AVSS													
61	47	32	P11	ADC_IN8/CMP123_INM1/ DAC_OUT	EIRQ1				TMR4_PCT	TMRA_5_PWM1/ TMRA_5_CLKA	TMRA_4_PWM1/ TMRA_4_CLKA			TMRA_2_PWM2/ TMRA_2_CLKB		
62	48	-	P10	ADC_IN9/CMP123_INM2	EIRQ0					TMRA_5_PWM1/ TMRA_5_CLKA	TMRA_4_PWM2/ TMRA_4_CLKB	USART1_TX		TMRA_2_TRIG		
63	-	-	PA5	ADC_IN10	EIRQ5					TMRA_5_PWM2/ TMRA_5_CLKB	TMRA_3_PWM1/ TMRA_3_CLKA	USART1_RX	SPI_MISO	TMRA_2_PWM2/ TMRA_2_CLKB		
64	-	-	PA4	ADC_IN11	EIRQ4			ADTRG		TMRA_5_TRIG	TMRA_3_PWM2/ TMRA_3_CLKB		SPI_SCK	TMRA_2_PWM2/ TMRA_2_CLKB		

Table 3-2 Port Configuration

Package	Port Group	Bits								Pin Count Total	
		7	6	5	4	3	2	1	0		
LQFP64	Port0	-	-	-	-	-	o	o	o	3	52
	Port1	-	-	-	-	-	-	o	o	2	
	Port2	-	-	-	o	o	o	-	-	3	
	Port3	o	o	-	-	o	o	o	o	6	
	Port4	o	o	o	o	o	o	o	o	8	
	Port5	-	-	-	-	-	-	-	o	1	
	Port7	-	o	o	o	o	o	o	o	7	
	Port9	-	-	-	o	o	o	o	-	4	
	PortA	-	-	o	o	o	o	-	-	4	
	PortB	o	o	o	o	o	o	o	o	8	
	PortD	o	o	o	o	o	-	-	-	5	
	PortE	-	-	-	-	-	o	-	-	1	
LQFP48	Port1	-	-	-	-	-	-	o	o	2	40
	Port2	-	-	-	o	o	o	-	-	3	
	Port3	o	o	-	-	-	-	-	-	2	
	Port4	o	o	o	o	o	o	o	o	8	
	Port5	-	-	-	-	-	-	-	o	1	
	Port7	-	o	o	o	o	o	o	o	7	
	Port9	-	-	-	o	o	-	-	-	2	
	PortA	-	-	-	-	o	o	-	-	2	
	PortB	o	o	o	o	o	o	o	o	8	
	PortD	-	o	o	o	o	-	-	-	4	
	PortE	-	-	-	-	-	o	-	-	1	
LQFP32	Port1	-	-	-	-	-	-	o	-	1	24
	Port3	o	o	-	-	-	-	-	-	2	

Package	Port Group	Bits								Pin Count Total	
		7	6	5	4	3	2	1	0		
LQFP32	Port4	-	-	-	o	o	o	o	o	5	24
	Port5	-	-	-	-	-	-	-	o	1	
	Port7	-	o	o	o	o	o	o	-	6	
	Port9	-	-	-	o	o	-	-	-	2	
	PortB	o	o	-	-	o	o	o	o	6	
	PortE	-	-	-	-	-	o	-	-	1	

Table 3-3 General Functional Specifications

Port		Pull-Up	Open-Drain Output	Driving Capacity
Port0	P00-P02	Support	Support	Low/High
Port1	P10-P11	Support	Support	Low/High
Port2	P22-P24	Support	Support	Low/High
Port3	P30-P33, P36-P37	Support	Support	Low/High
Port4	P40-P47	Support	Support	Low/High
Port5	P50	Support	Support	Low/High
Port7	P70-P76	Support	Support	Low/High
Port9	P91-P94	Support	Support	Low/High
PortA	PA2-PA5	Support	Support	Low/High
PortB	PB0-PB7	Support	Support	Low/High
PortD	PD3-PD7	Support	Support	Low/High
PortE	PE2	Support	Support	Low/High

Note

Input voltage must not be higher than VREFH/AVCC when used as an analog function.

3.3 Pin Function Description

Table 3-4 Pin Function Description

Categories	Functional Name	I/O	Description
Power	VCC	I	Power supply
	VSS	I	Power ground
	VCL/REGC	IO	Core voltage
	AVCC/VREFH	I	Analog power supply/analog reference voltage
	AVSS/VREFL	I	Analog power ground/analog reference voltage
System	NRST	I	Reset terminal, active low, with built-in pull-up resistors(1)
	MD	I	Mode terminal, with built-in pull-up resistors(1)
PVD	PVD2EXINP	I	PVD2 external input comparison voltage
Clock	XTAL_OUT	O	External main clock oscillator interface
	XTAL_EXT/XTAL_IN	I	External main clock oscillator interface
	EXTAL	I	XTAL external clock input
	MCO	O	Internal clock output
GPIO	Pxy (x=0-5, 7, 9, A, B, D, E y=0-7)	IO	General input output
EIRQ	EIRQx (x=0-7)	I	Maskable external interrupt
	NMI	I	Non-maskable external interrupt
SWD	SWCLK	I	Online debugging interface, with built-in pull-up resistors(1)
	SWDIO	IO	
TOOL0	TOOL0	IO	Single wire debug interface
FCM	FCMREF	I	External reference clock input for clock frequency measurement
Timer4	TMR4_CLK	I	Counting clock port input
	TMR4_OUH	IO	PWM port U-phase output
	TMR4_OUL	IO	PWM port U-phase output
	TMR4_OVH	IO	PWM port V-phase output
	TMR4_OVL	IO	PWM port V-phase output
	TMR4_OWH	IO	PWM port W-phase output
	TMR4_OWL	IO	PWM port W-phase output
	TMR4_OXH	IO	PWM port X-phase output

Categories	Functional Name	I/O	Description
Timer4	TMR4_OXL	IO	PWM port X-phase output
	TMR4_ADSM	O	Special event output monitoring
	TMR4_PCT	O	PWM periodic output monitoring
TimerA	TMRA_x_TRIG (x=1-5)	I	External event trigger input
	TMRA_x_PWM1/TMRA_x_CLKA (x=1-5)	IO	External event trigger input or PWM port output or count clock port input
	TMRA_x_PWM2/TMRA_x_CLKB (x=1-5)	IO	External event trigger input or PWM port output or count clock port input
	TMRA_x_PWMy (x=5 y=3-6)	IO	External event trigger input or PWM port output
EMB	EMB_INx (x=1-3)	I	Port input control signal
HALL	HALL_x (x=A,B,C)	I	Hall signal input
USART	USARTx_TX (x=1-4)	IO	Transmit data
	USARTx_RX (x=1-4)	IO	Receiving data
	USARTx_CK (x=1-4)	IO	Communication clock
	USARTx_RTS_DE (x=1-4)	O	Request transmiting signal/driver enable
	USARTx_CTS (x=1-4)	I	Clear transmiting signal
SPI	SPI_MISO	IO	Master input/slave output data transfer pin
	SPI_MOSI	IO	Master output/slave input data transfer pin
	SPI_SCK	IO	Transmission clock
	SPI_NSS0	IO	Slave selection input/output pin
	SPI_NSSy (y=1-3)	O	Slave selection output pin
I2C	I2C_SCL	IO	Clock line
	I2C_SDA	IO	Data line
CMP	VCOUT1	O	CMP1 result output
	VCOUT2	O	CMP2 result output
	VCOUT3	O	CMP3 result output
	VCOUT	O	CMP1-3 result OR output
	CMPx_INPy (x=1-3 y=1-3)	I	CMP1-3 positive terminal analog input
	CMP123_INMy (y=1-2)	I	CMP1,3 negative analog input

Categories	Functional Name	I/O	Description
ADC	ADTRG	I	ADC AD convert external startup source
	ADST	O	ADC conversion action status
	ADC_INx (x=0-15)	I	ADC external analog input port
DAC	DAC_OUT	O	DAC analog output
OPA	OPAxO (x=1-3)	O	OPA output
	OPAxP (x=1-3)	I	OPA positive terminal input
	OPAxN (x=1-3)	I	OPA negative terminal input

Note

1. For the resistance value of the built-in pull-up resistor, please refer to the relevant description in "Electrical Specifications - I/O Port Characteristics".

3.4 Pin Instructions

Table 3-5 Pin Instruction

Pin Name	Usage Notes
VCC	Power Supply. Connect to 2.7V-5.5V and place a decoupling capacitor near the VSS pin (refer to "Electrical Specifications").
VSS	Source ground, connected to 0V.
VCL/REGC	Core Voltage. Place a capacitor near the VSS pin to stabilize the core voltage (refer to "Electrical Specifications").
AVCC	Analog Power Supply. Supply power to analog modules; connect to the same power supply as VCC (refer to "Electrical Specifications"). When not using an independent analog power supply, connect the pin to VCC and ensure it is not left floating.
AVSS	Analog Power Ground. Supply ground to analog modules; connect to the same voltage as VSS (refer to "Electrical Specifications"). When not using an independent analog power supply, connect the pin to VSS and ensure it is not left floating.
VREFL	Analog Reference Voltage. Connect to the same voltage as AVSS, recommended to be short-circuited with AVSS (refer to "Electrical Specifications"). Connect to AVSS when not in use and do not leave it floating.
VREFH	Analog Reference Voltage, do not exceed AVCC when in use, recommended to be short-circuited with AVCC. Connect to AVCC when not in use and do not leave it floating.
P50/MD	Mode input. When NRST is released (changing from low level to high level), this pin must be fixed at high level. Recommended to connect a resistor (4.7kΩ) to VCC (pull-up).
NRST	Reset pin (NRST), active low. Resistance to VCC when not in use (pull-up).
Pxy (x=0 to 5,7,9,A,B,D,E y=0-7)	General pin. Input voltage should not exceed VCC. When used as an analog input, the analog voltage should not exceed VREFH/AVCC. When not in use, leave floating or connect a resistor to VCC (pull-up) or VSS (pull-down).

4 Electrical Specifications

4.1 Parameter Conditions

Unless otherwise specified, all voltages are based on VSS.

4.1.1 Minimum and Maximum Values

All Minimum Values and Maximum Values are measured under the worst conditions.

Data resulted from comprehensive evaluation, and/or guaranteed by design are indicated in the table footnotes, and they will not be tested on the production line.

4.1.2 Typical Values

Unless otherwise specified, typical data are given based on T_A=25℃ and VCC=5.0V. These data are only used for design guidance and have not been tested.

4.1.3 Typical Curve

Unless otherwise specified, all typical curves are untested and are for design reference only.

4.1.4 Load Capacitance

The left of Figure 4-1 : Pin Load Condition (Left) and Input Voltage Measurement (Right) displays the load conditions used to measure the pin parameters.

4.1.5 Pin Input Voltage

The right of Figure 4-1 : Pin Load Condition (Left) and Input Voltage Measurement (Right) displays the measurement method of the input voltage on the device pin.

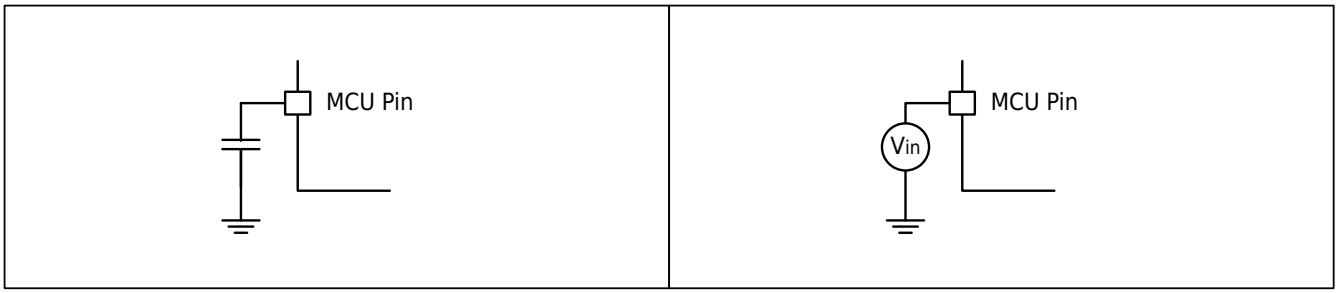


Figure 4-1 Pin Load Condition (Left) and Input Voltage Measurement (Right)

4.1.6 Power Scheme

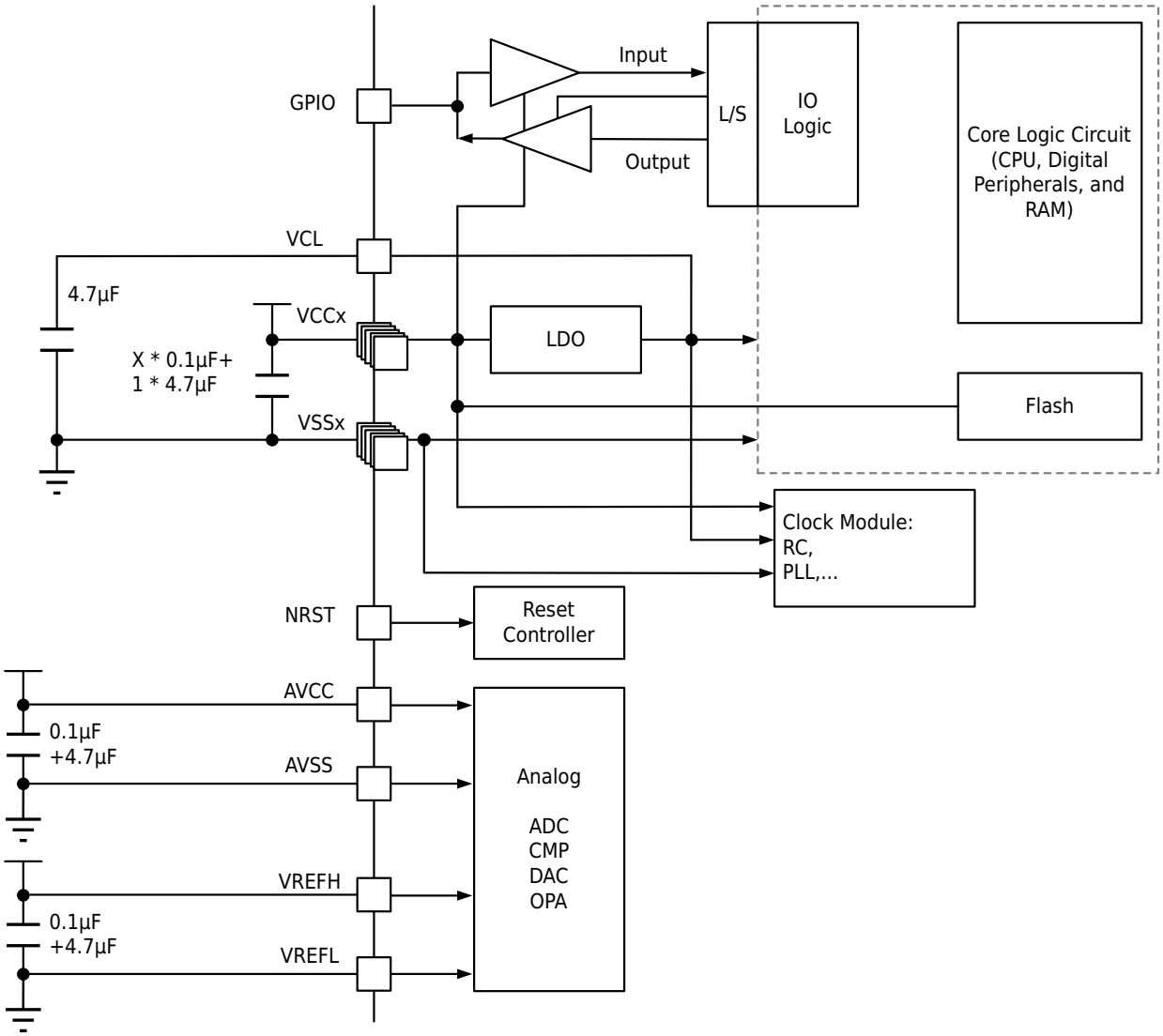


Figure 4-2 Power Scheme

Note

1. 4.7μF ceramic capacitor must be connected to one of VCC pins.
2. AVSS=VSS.
3. Each power supply pair (e.g. VCC/VSS, AVCC/AVSS...) must be decoupled with the above-mentioned filter ceramic capacitors. These capacitors must be as close as possible to or below that of the appropriate pins under the PCB to ensure the normal operation of the device. It is not recommended to remove the filter capacitor to reduce the size or cost of PCB, which may lead to abnormal operation of the device.
4. Under the LQFP64 package, VREFH and VREFL pins are available. For other packages, AVCC and AVSS pins should be used to replace VREFH and VREFL, respectively.

4.1.7 Current Consumption Measurement

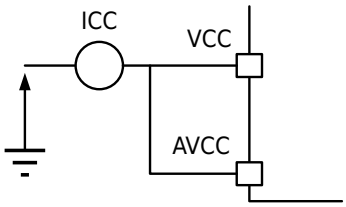


Figure 4-3 Current Consumption Measurement Solution

4.2 Absolute Maximum Ratings

If the load applied to the device exceeds the value given in the list of "Absolute Maximum Ratings", it may cause permanent damage to the device. The maximum load given here is for reference, which does not mean that the functional operation of the device is correct under this condition. Operation of the device under the condition of maximum value for a long time will affect the reliability of the device.

Table 4-1 Voltage and Current Characteristics

Symbol	Description	Min	Max	Unit
V_{CC}-V_{SS}	External main power voltage (including AVCC, VCC)(1)	-0.3	5.8	V
V_{IN}	Input voltage of other pins(2)	V_{SS}0.3	V_{CC}+0.3	V
|VSSx-VSS|	Voltage difference between different ground pins	-	50	mV
ΣI_{VCC}	Total current flowing into all VCC_X power wires (pull current) (1)	-	100	mA
ΣI_{VSS}	Total current flowing out all VSS_X ground wires (sink current) (1)	-	-100	mA
I_{VCC}	Maximum current flowing into each VCC_X power wire (pull current)(1)	-	50	mA
I_{VSS}	Maximum current flowing out each VSS_X ground wire (sink current)(1)	-	-50	mA
I_{IO}	Output sink current on any I/O and control pins	-	16	mA
	Output pull current on any I/O and control pins	-	-16	mA
ΣI_{IO}	Total output sink current on all I/O and control pins(3)	-	50	mA
	Total output pull current on all I/O and control pins(3)	-	-50	mA

Note

1. All main power supplies (VCC, AVCC) and ground (VSS, AVSS) pins must always be connected to the external supply within the allowed range.
2. The maximum value for V_{IN} must always be conformed.
3. This total output current must be properly distributed across all power domains.

Table 4-2 Temperature Characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage Temperature Range	-65-+150	℃

Symbol	Description	Value	Unit
T_{Jmax}	Maximum Junction Temperature	125	℃

4.3 Operating Conditions

4.3.1 General Operating Conditions

Table 4-3 General Operating Conditions

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{HCLK}	Internal AHB Clock Frequency	-	-	-	120	MHz
V_{CC}(1)	Standard Operating Voltage	-	2.7	-	5.5	V
V_{AVCC}(1)	Analog Operating Voltage	-	V_{CC}	-	5.5	V
T_J(1)	Junction Temperature Range	-	-40	-	125	℃
T_A(1)	Operating Temperature Range	-	-40	-	105	℃

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.2 Working Conditions at Power On and Power Down

Table 4-4 Working Conditions at Power On and Power Down

Symbol	Parameters	Min	Max	Unit
t_{VCC}(1)(2)	VCC rising time rate	20	1000000	μs/V
	VCC falling time rate	20	1000000	

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. VCC and AVCC require simultaneous power-on or AVCC should be powered on first followed by VCC. Additionally, VCC and AVCC need to be powered off simultaneously.

4.3.3 Reset and Power Control Module Characteristics

Table 4-5 Reset and Power Control Module Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{BOR}	BOR monitoring voltage	ICG1.BOR_LEV=0b00	2.4	2.50	2.65	V
		ICG1.BOR_LEV=0b01(1)	2.65	2.80	2.95	V
		ICG1.BOR_LEV=0b10(1)	3.40	3.55	3.70	V
		ICG1.BOR_LEV=0b11	3.70	3.85	4.00	V
V_{PVD1}	PVD1 monitoring voltage(3)	PVD1LVL=0b0000	2.4	2.5	2.65	V
		PVD1LVL=0b0001(1)	2.5	2.65	2.80	V

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{PVD1}	PVD1 monitoring voltage[3]	PVD1LVL=0b0010[1]	2.65	2.80	2.95	V
		PVD1LVL=0b0011[1]	2.80	2.95	3.10	V
		PVD1LVL=0b0100[1]	2.95	3.10	3.25	V
		PVD1LVL=0b0101[1]	3.10	3.25	3.40	V
		PVD1LVL=0b0110[1]	3.25	3.40	3.55	V
		PVD1LVL=0b0111	3.40	3.55	3.70	V
		PVD1LVL=0b1000[1]	3.55	3.70	3.85	V
		PVD1LVL=0b1001[1]	3.70	3.85	4.00	V
		PVD1LVL=0b1010[1]	3.85	4.00	4.15	V
		PVD1LVL=0b1011[1]	4.00	4.15	4.30	V
		PVD1LVL=0b1100[1]	4.15	4.30	4.45	V
		PVD1LVL=0b1101[1]	4.30	4.45	4.60	V
		PVD1LVL=0b1110[1]	4.45	4.60	4.75	V
		PVD1LVL=0b1111[1]	4.60	4.75	4.90	V
V_{PVD2}	PVD2 monitoring voltage[3]	PVD2LVL=0b0000	2.4	2.5	2.65	V
		PVD2LVL=0b0001[1]	2.5	2.65	2.80	V
		PVD2LVL=0b0010[1]	2.65	2.80	2.95	V
		PVD2LVL=0b0011[1]	2.80	2.95	3.10	V
		PVD2LVL=0b0100[1]	2.95	3.10	3.25	V
		PVD2LVL=0b0101[1]	3.10	3.25	3.40	V
		PVD2LVL=0b0110	3.25	3.40	3.55	V
		PVD2LVL=0b0111[1]	3.40	3.55	3.70	V
		PVD2LVL=0b1000[1]	3.55	3.70	3.85	V
		PVD2LVL=0b1001[1]	3.70	3.85	4.00	V
		PVD2LVL=0b1010[1]	3.85	4.00	4.15	V
		PVD2LVL=0b1011[1]	4.00	4.15	4.30	V
		PVD2LVL=0b1100[1]	4.15	4.30	4.45	V
		PVD2LVL=0b1101[1]	4.30	4.45	4.60	V
		PVD2LVL=0b1110[1]	4.45	4.60	4.75	V
		PVD2LVL=0b1111	4.60	4.75	4.90	V
$V_{pvd}hyst$[1]	PVD1/2 hysteresis[4]	-	-	70	-	mV
V_{POR}	Power-on reset threshold	Rising Edge VPOR	-	2.25	-	V
		Falling Edge VPDR	-	2.15	-	V
$V_{POR}hyst$[1]	POR hysteresis	-	-	100	-	mV

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
I_{RUSH}(1)	Inrush current during regulator power-on (POR)	-	-	150	300	mA
T_{NRST}(1)	NRST reset minimum pulse width	-	10	-	-	μs
T_{IPVD1}(2)	PVD1 reset removal time	-	-	380	-	μs
T_{IPVD2}(2)	PVD2 reset removal time	-	-	380	-	μs
T_{INRST}(2)	NRST reset removal time	-	-	380	-	μs
T_{RIPT}(2)	Internal reset time	-	-	380	-	μs
T_{RSTBOR}(2)	BOR reset removal time	-	-	380	-	μs
T_{RSTPOR}(2)	Power-on reset removal time	-	-	2500	3000	μs

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. PVD1 monitoring voltage is the monitoring voltage when VCC voltage is falling; PVD2 monitoring voltage is the monitoring voltage when VCC voltage is falling or when PVD2EXINP voltage is falling.
4. PVD1/2 hysteresis is the difference between the monitoring voltage when VCC or PVD2EXINP is rising and the monitoring voltage when it is falling.

   PVD1 monitoring voltage when VCC is rising = V_{PVD1}+V_{pvd}hyst;

   PVD2 monitoring voltage when VCC or PVD2EXINP is rising = V_{PVD2}+V_{pvd}hyst.
5. The PVD2EXINP voltage must be less than the chip supply voltage.

4.3.4 Built-in Reference Voltage

Table 4-6 Built-in Reference Voltage

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{REF12}(1)	Internal 1.2V reference voltage	T_A=-40-105℃ V_{CC}=2.7-5.5V	1.17	1.20	1.23	V
V_{REF25}	Internal 2.5V reference voltage	T_A=-40-105℃ V_{CC}=2.7-5.5V	2.425	2.50	2.575	V
V_{REF42}	Internal 4.2V reference voltage	T_A=-40-105℃ V_{CC}=4.5-5.5V	4.074	4.20	4.326	V

Note

1. Guaranteed by design, not tested in production.

4.3.5 Supply Current Characteristics

Current consumption is affected by many parameters and factors, including operating voltage, ambient temperature, I/O pin load, device software configuration, operating frequency, I/O pin switching rate, program location in memory and running code.

Figure 4-3 : Current Consumption Measurement Solution describes the measurement method of current consumption. The measured values of current consumption in various modes described in this section are obtained by a set of test codes running in FLASH under laboratory conditions.

The specific conditions are as follows:

1. All I/O pins are in high-impedance mode (no load).
2. Clock frequencies selected are high-speed mode f_{HCLK}=120MHz/24MHz and ultra-low-speed mode f_{HCLK}=8MHz/1MHz.
3. Power modes are divided into: normal operating mode ICC_RUN, sleep mode ICC_SLEEP, stop mode ICC_STP, and Dhrystone operating mode ICC_DHRYSTONE.
4. Please refer to the specific current condition description for peripheral clock ON/OFF.
5. In high-speed mode f_{HCLK}=120MHz, the PLL is in the ON state.

Table 4-7 High-speed mode current consumption 1(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN(1)	While (1), all peripherals clock OFF	f_{HCLK}=120MHz T_A=-40℃ V_{CC}=5.0V	-	9.1	-	mA
	While (1), all peripherals clock ON		-	13.9	-	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	10.0	-	mA
	CACHE ON		-	11.0	-	mA
ICC_SLEEP(1)	All peripherals clock OFF		-	5.1	-	mA
	All peripherals clock ON		-	9.8	-	mA
ICC_RUN(1)	While (1), all peripherals clock OFF	f_{HCLK}=120MHz T_A=25℃ V_{CC}=5.0V	-	4.2	-	mA
	While (1), all peripherals clock ON		-	14.0	-	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	10.2	-	mA
	CACHE ON		-	11.2	-	mA
ICC_SLEEP(1)	All peripherals clock OFF		-	5.2	-	mA
	All peripherals clock ON		-	10.0	-	mA
ICC_RUN(1)	While (1), all peripherals clock OFF	f_{HCLK}=120MHz T_A=85℃ V_{CC}=2.7-5.5V	-	-	12	mA
	While (1), all peripherals clock ON		-	-	17	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	-	13	mA
	CACHE ON		-	-	13	mA
ICC_SLEEP(1)	All peripherals clock OFF		-	-	8	mA
	All peripherals clock ON		-	-	13	mA

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=120MHz T_A=105℃ V_{CC}=2.7-5.5V	-	-	14	mA
	While (1), all peripherals clock ON		-	-	19	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	-	15	mA
	CACHE ON		-	-	15	mA
ICC_SLEEP	All peripherals clock OFF		-	-	10	mA
	All peripherals clock ON		-	-	15	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-8 High-speed mode current consumption 2(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=24MHz T_A=-40℃ V_{CC}=5.0V	-	4.1	-	mA
	While (1), all peripherals clock ON		-	5.3	-	mA
ICC_DHRYSTONE	CACHE OFF		-	4.9	-	mA
ICC_SLEEP	All peripherals clock OFF		-	2.1	-	mA
	All peripherals clock ON		-	3.2	-	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=24MHz T_A=25℃ V_{CC}=5.0V	-	4.2	-	mA
	While (1), all peripherals clock ON		-	5.4	-	mA
ICC_DHRYSTONE	CACHE OFF		-	5.0	-	mA
ICC_SLEEP	All peripherals clock OFF		-	2.2	-	mA
	All peripherals clock ON		-	3.4	-	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=24MHz T_A=85℃ V_{CC}=2.7-5.5V	-	-	7	mA
	While (1), all peripherals clock ON		-	-	8.6	mA
ICC_DHRYSTONE	CACHE OFF		-	-	8.1	mA
ICC_SLEEP	All peripherals clock OFF		-	-	4.8	mA
	All peripherals clock ON		-	-	6.4	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=24MHz T_A=105℃ V_{CC}=2.7-5.5V	-	-	8	mA
	While (1), all peripherals clock ON		-	-	10	mA
ICC_DHRYSTONE	CACHE OFF		-	-	9	mA
ICC_SLEEP	All peripherals clock OFF		-	-	7.5	mA
	All peripherals clock ON		-	-	9.5	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-9 Ultra-low speed mode current consumption 1

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN(1)	While (1), all peripherals clock OFF	f_{HCLK}=8MHz T_A=-40℃ V_{CC}=5.0V	-	1.8	-	mA
	While (1), all peripherals clock ON		-	2.3	-	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	2.0	-	mA
ICC_SLEEP(1)	All peripherals clock OFF		-	0.5	-	mA
	All peripherals clock ON		-	1.0	-	mA
ICC_RUN(1)	While (1), all peripherals clock OFF	f_{HCLK}=8MHz T_A=25℃ V_{CC}=5.0V	-	1.9	-	mA
	While (1), all peripherals clock ON		-	2.4	-	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	2.0	-	mA
ICC_SLEEP(1)	All peripherals clock OFF		-	0.6	-	mA
	All peripherals clock ON		-	1.1	-	mA
ICC_RUN(1)	While (1), all peripherals clock OFF	f_{HCLK}=8MHz T_A=85℃ V_{CC}=2.7-5.5V	-	-	4.4	mA
	While (1), all peripherals clock ON		-	-	6	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	-	5.5	mA
ICC_SLEEP(1)	All peripherals clock OFF		-	-	4	mA
	All peripherals clock ON		-	-	5.2	mA
ICC_RUN(1)	While (1), all peripherals clock OFF	f_{HCLK}=8MHz T_A=105℃ V_{CC}=2.7-5.5V	-	-	7	mA
	While (1), all peripherals clock ON		-	-	9	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	-	8.5	mA
ICC_SLEEP	All peripherals clock OFF		-	-	5.5	mA
	All peripherals clock ON		-	-	8.3	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-10 Ultra-low speed mode current consumption 2(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=1MHz T_A=-40℃ V_{CC}=5.0V	-	0.6	-	mA
	While (1), all peripherals clock ON		-	0.8	-	mA
ICC_DHRYSTONE	CACHE OFF		-	0.7	-	mA
ICC_SLEEP	All peripherals clock OFF		-	0.4	-	mA
	All peripherals clock ON		-	0.6	-	mA

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=1MHz T_A=25℃ V_{CC}=5.0V	-	0.7	-	mA
	While (1), all peripherals clock ON		-	0.9	-	mA
ICC_DHRYSTONE	CACHE OFF		-	0.7	-	mA
ICC_SLEEP	All peripherals clock OFF		-	0.4	-	mA
	All peripherals clock ON		-	0.6	-	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=1MHz T_A=85℃ V_{CC}=2.7-5.5V	-	-	2.2	mA
	While (1), all peripherals clock ON		-	-	2.6	mA
ICC_DHRYSTONE	CACHE OFF		-	-	2.3	mA
ICC_SLEEP	All peripherals clock OFF		-	-	1.9	mA
	All peripherals clock ON		-	-	2.3	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=1MHz T_A=105℃ V_{CC}=2.7-5.5V	-	-	2.9	mA
	While (1), all peripherals clock ON		-	-	3.3	mA
ICC_DHRYSTONE	CACHE OFF		-	-	3	mA
ICC_SLEEP	All peripherals clock OFF		-	-	2.6	mA
	All peripherals clock ON		-	-	2.6	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-11 Low Power Mode Current Consumption(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_STP (Stop Mode)	-	T_A=-40℃ V_{CC}=5.0V	-	33	-	μA
	-	T_A=25℃ V_{CC}=5.0V	-	56	-	μA
	-	T_A=85℃ V_{CC}=2.7-5.5V	-	-	1.9	mA
	-	T_A=105℃ V_{CC}=2.7-5.5V	-	-	3.9	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-12 Analog Module Current Consumption(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_MODULE	XTAL Oscillation Mode High Drive 24MHz	T_A=25℃ V_{CC}=V_{AVCC}=5.0V	-	1.8	-	mA
	Oscillation Mode Ultra Low Drive 4MHz		-	0.15	-	mA
	HRC		-	0.16	-	mA
	PLL (VCO=480MHz)		-	1.18	-	mA
	ADC		-	0.92	-	mA
	DAC		-	0.20	-	mA
	CMP		-	0.18	-	mA
	OPA		-	0.7	-	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.6 Low Power Mode Wake-up Timing

The wake-up time is measured from the trigger of the wake-up event to the first instruction executed by the CPU:

- For Stop or Sleep mode: the wake-up event is WFE.
- All timings are measured at ambient temperature and V_{CC}=5.0V.

Table 4-13 Low-power Mode Wake-up Time(1)

Symbol	Parameters	Conditions	Typical	Maximum	Unit
T_{STOP}	Wake-up from Stop mode	Thhe system clock is MRC	8	15	μs

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.7 External Clock Source Characteristics

4.3.7.1 High-Speed External Clock Generated by External Source

In bypass mode, XTAL oscillator is disabled and the input pin is a standard I/O. The external clock signal must consider the static characteristics of the I/O.

Table 4-14 High-Speed External Clock Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{EXTAL}	User external clock source frequency	-	1(1)	-	24	MHz
V_{IH_XTAL}(1)	EXTAL input pin high-level voltage	-	0.7*V_{CC}	-	V_{CC}	V
V_{IL_XTAL}(1)	EXTAL input pin low-level voltage	-	V_{SS}	-	0.3*V_{CC}	V
$t_{r(XTAL)}$(1) $t_{f(XTAL)}$(1)	EXTAL rising or falling time	-	-	-	20	ns
$Duty_{(XTAL)}$(1)	Duty cycle	-	40	-	60	%

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.7.2 High-Speed External Clock Generated by Crystal Oscillator/Ceramic Resonator

The high-speed external clock (XTAL) can be generated by a crystal/ceramic resonator oscillator with a frequency of 424MHz. In application, the resonator and load capacitor must be as close as possible to the pin of oscillator, so as to minimize the output distortion and the stabilization time. For detailed information about resonator characteristics (frequency, package, accuracy, etc.), please consult the crystal resonator manufacturer.

Table 4-15 XTAL 424 MHz Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{XTAL_IN} (1)	Oscillator frequency	-	4	-	24	MHz
R_F	Feedback resistance	-	-	0.6	-	MΩ
G_{mmax} (2)	Oscillator Gm	Startup	0.36	-	-	mA/V
$t_{SU(XTAL)}$ (1)(4)	Startup time	V_{CC} stable, crystal oscillator frequency = 24 MHz	-	300	-	μs
		V_{CC} stable, crystal oscillation frequency = 4 MHz	-	3	-	ms

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. This parameter depends on the resonator used in the application system.
4. $t_{SU(XTAL)}$ is the oscillation starting time, that is, the time from the software enabling XTAL to the stable 8MHz oscillation frequency. This value is measured based on a standard crystal resonator, and may vary significantly depending on the crystal oscillator manufacturer.

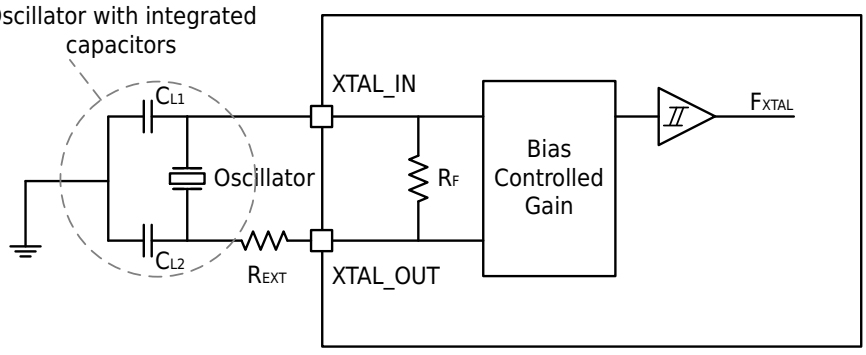


Figure 4-4 Typical Application with 8 MHz Crystal Osicillator

Note

- For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors designed for high-frequency applications, which can meet the requirements of crystal oscillator or resonator (see the figure above). C_{L1} and C_{L2} usually have the same size. $C_{L1}=C_{L2}=2*(C_L-C_S)$. C_S is the total parasitic capacitance between the PCB and the MCU pins (XTAL_IN, XTAL_OUT). C_L denotes the load capacitance of the crystal oscillator or ceramic resonator, please consult the crystal oscillator manufacturer for details.
- The value of R_{EXT} depends on the crystal oscillation characteristics.

4.3.8 Internal Clock Source Characteristics

4.3.8.1 HRC

Table 4-16 HRC Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{HRC}	Frequency(2)	-	-	12	-	MHz
	Frequency accuracy(1)	T_A=-40-105℃	-1	-	1	%
		T_A=25℃	-0.5	-	0.5	%
$t_{st(HRC)}$(2)	HRC oscillator stabilization time	-	-	8	-	μs

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.

4.3.8.2 MRC

Table 4-17 MRC Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{MRC}	Frequency	-	7.2	8	8.8	MHz
$t_{st(MRC)}$	MRC oscillator stabilization time	-	-	-	15	μs

4.3.8.3 LRC

Table 4-18 LRC Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{LRC}	Frequency	-	29.5	32.768	36.0	kHz
$t_{st(LRC)}$	LRC oscillator stabilization time	-	-	-	100	μs

4.3.9 PLL Characteristics

Table 4-19 System PLL (PLL) Key Performance Indicators

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}(2)	Input clock of PLL phase detector (PFD)	-	4	-	8	MHz

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{PLL_OUT}(1)	Output clock of PLL multiplier	-	20	-	120	MHz
f_{VCO_OUT}	PLL voltage controlled oscillator (VCO) output	-	320	-	480	MHz
$Jitter_{PLL}$(1)	Periodic jitter	The input clock of PLL PFD is 8MHz, and the system clock is 120MHz, peak to peak.	-	±70	-	ps
	Jitter during adjacent periods	The input clock of PLL PFD is 8MHz, and the system clock is 120MHz, peak to peak.	-	±100	-	ps
t_{LOCK}(1)	PLL lock time	-	-	50	80	µs

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. It is recommended to use a higher input clock to obtain jittering characteristics.

4.3.10 Memory (Flash) Characteristics

When the flash memory is erased when it is delivered to the customer.

Table 4-20 Flash Memory Characteristics(1)

Symbol	Parame-ters	Conditions	Min	Typ	Max	Unit
I_{VCC}	Supply Current	Read mode, V_{CC}=2.75.5V	-	-	5	mA
		Programming mode, V_{CC}=2.75.5V	-	-	10	mA
		Block erase mode, V_{CC}=2.75.5V	-	-	10	mA
		Mass erase mode, V_{CC}=2.75.5V	-	-	10	mA

Note

1. Guaranteed by design, not tested in production.

Table 4-21 Flash Memory Program and Erase Times(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
T_{prog}	Byte Programming Time	Single programming mode	-	168	-	µs
	Word Programming Time	Single programming mode	-	178	-	µs
T_{erase}	Block Erase Time	-	-	2.6	-	ms
T_{mas}	Mass Erase Time	-	-	38	-	ms

Note

1. Guaranteed by design, not tested in production.

Table 4-22 Flash Erase Write Times and Data Storage Period[1]

Symbol	Parameters	Conditions	Min	Typ	Unit
N_{END}	Program, Block Erase Cycles	T_A=-40℃~105℃	-	100000	Cycles
T_{RET}	Data Storage Period	20 kcycles at T_A=85℃	10	-	Year

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.11 Electrical Sensitivity

The chip is subjected to different tests (ESD, LU) by a specific measurement method to determine its performance in terms of electrical sensitivity.

4.3.11.1 Electrostatic Discharge (ESD)

Electrostatic discharge is applied to the pins of each sample according to each pin combination. This test complies with the ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 standards.

Table 4-23 ESD Characteristics[1]

Symbol	Parameters	Conditions	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A=25℃, compliant with ANSI/ESDA/JEDEC JS-001 standard	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charged device model)	T_A=25℃, compliant with ANSI/ESDA/JEDEC JS-002 standard	1000	V

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.11.2 Static Latch-up

To evaluate static Latch-up performance, two complementary static Latch-up tests should be performed on the chip by:

- Applying overvoltage to each power supply and analog input pin.
- Applying current to other input, output, and configurable I/O pins.

These tests comply with the EIA/JESD 78 IC Latch-up standard.

Table 4-24 Static Latch-up Characteristics[1]

Symbol	Parameters	Conditions	Max	Unit
LU	Static Latch-up	T_A=105℃, compliant with JESD78 standard	200	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.12 I/O Port Characteristics

General-Purpose Input/Output Characteristics

Table 4-25 I/O Static Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{IL}	Schmitt input low level	Except NRST pin	-	-	$0.3V_{CC}$	V
		NRST pin	-	-	$0.2V_{CC}$	V
V_{IH}	Schmitt input high level	Except NRST pin	$0.7V_{CC}$	-	-	V
		NRST pin	$0.8V_{CC}$	-	-	V
V_{HYS}(1)	Schmitt input hysteresis	-	$0.1V_{CC}$	-	-	V
V_{IL}	CMOS input low level	-	-	-	$0.3V_{CC}$	V
V_{IH}	CMOS input high level	-	$0.7V_{CC}$	-	-	V
I_{LKG}	I/O input leakage current	$V_{SS} \le V_{IN} \le V_{CC}$	-	-	1	μA
R_{PU}(3)	Weak pull-up equivalent resistance	$V_{IN}=V_{SS}$ $2.7 \le V_{CC} \le 5.5$	20	55	100	kΩ
C_{IO}(2)	I/O pin capacitance	-	-	-	10	pF

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. To keep the voltage above V_{CC}+0.3V, the internal pull-up resistor must be disabled.

Output Current

The GPIO (General-Purpose Input/Output) can provide a maximum source or sink current of ±16mA.

Output Voltage

Table 4-26 Output Voltage Characteristics

Driver	Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Low Drive	V_{OL}(1)(3)	Low-Level Output	I_{IO}=±4mA V_{CC}=3.3V	-	-	0.4	V
	V_{OH}(2)(3)	High-Level Output		V_{CC}-0.9	-	-	V
	V_{OL}(1)	Low-Level Output	I_{IO}=±8mA V_{CC}=5V	-	-	0.6	V
	V_{OH}(2)	High-Level Output		V_{CC}-0.9	-	-	V

Driver	Symbol	Parameters	Conditions	Min	Typ	Max	Unit
High Drive	V_{OL}(1)(3)	Low-Level Output	I_{IO}=±8mA V_{CC}=3.3V	-	-	0.4	V
	V_{OH}(2)(3)	High-Level Output		V_{CC}-0.9	-	-	V
	V_{OL}(1)	Low-Level Output	I_{IO}=±16mA V_{CC}=5V	-	-	0.6	V
	V_{OH}(2)	High-Level Output		V_{CC}-0.9	-	-	V

Note

1. The device's I_{IO} sinking current must always take into account the absolute maximum ratings specified in Table 4-1 : Voltage and Current Characteristics. The sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The device's I_{IO} pull current must always conform to the absolute maximum ratings specified in Table 4-1 : Voltage and Current Characteristics. The total sum of I_{IO} (I/O ports and control pins) must not exceed I_{VCC}.
3. Resulted from comprehensive evaluation, not tested in production.

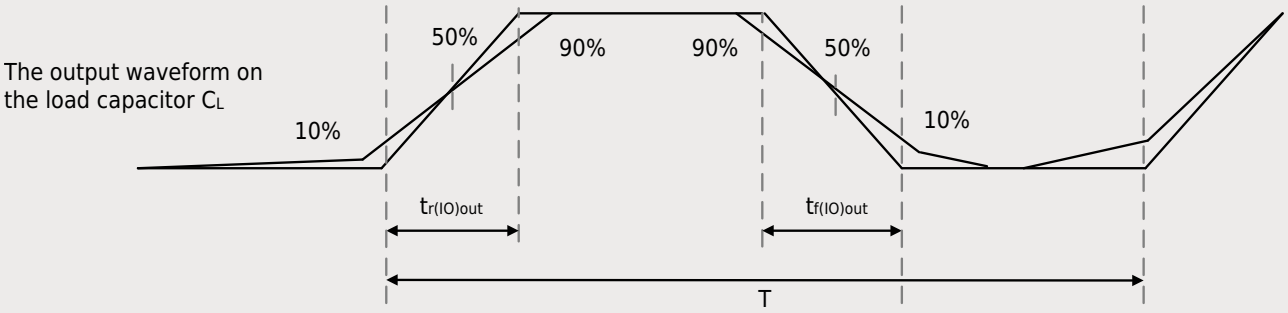
Input/Output AC Characteristics

Table 4-27 I/O AC Characteristics(1)

Drive Setting	Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Low Drive	$f_{max(IO)out}$(2)	Maximum Frequency	C_L=25pF, V_{CC}≥4.5V	-	-	45	MHz
			C_L=25pF, V_{CC}≥2.7V	-	-	40	
			C_L=50pF, V_{CC}≥4.5V	-	-	30	
			C_L=50pF, V_{CC}≥2.7V	-	-	18	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Rise/Fall Time	C_L=25pF, V_{CC}≥4.5V	-	-	5.1	ns
			C_L=25pF, V_{CC}≥2.7V	-	-	7.9	
			C_L=50pF, V_{CC}≥4.5V	-	-	10.2	
			C_L=50pF, V_{CC}≥2.7V	-	-	16	
High Drive	$f_{max(IO)out}$(2)	Maximum Frequency	C_L=25pF, V_{CC}≥4.5V	-	-	55	MHz
			C_L=25pF, V_{CC}≥2.7V	-	-	50	
			C_L=50pF, V_{CC}≥4.5V	-	-	50	
			C_L=50pF, V_{CC}≥2.7V	-	-	36	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Rise/Fall Time	C_L=25pF, V_{CC}≥4.5V	-	-	2.9	ns
			C_L=25pF, V_{CC}≥2.7V	-	-	4.3	
			C_L=50pF, V_{CC}≥4.5V	-	-	5.2	
			C_L=50pF, V_{CC}≥2.7V	-	-	8	

Note

1. Based on a comprehensive evaluation, it is not tested in production.
2. Guaranteed by design, not tested in production. The maximum frequency is defined in the figure below. Among them, $t_{f(IO)out}$ and $t_{r(IO)out}$ of terminals P44, P46, and P47 are defined as 30%-70%.
3. The load capacitance C_L must take into account the capacitance of the PCB and the MCU pins (the pin-to-board capacitance can be roughly estimated as 15pF).



Maximum frequency condition ($t_r + t_f$) ≤ (2/3)T and Duty cycle= 50% ± 5%
C_L is indicated in the "Conditions" column of the "I/O AC Characteristics" table)

Figure 4-5 I/O Communication Characteristics Definition

4.3.13 I2C Interface Characteristics

Table 4-28 I2C Electrical Specifications

Symbol	Parameter	Standard Mode (SM)		Fast Mode (FM)		Unit
		Min	Max	Min	Max	
f_{SCL}(1)	SCL Frequency	0	100	0	400	kHz
$t_{HD;STA}$(1)	Start Condition/Repeated Start Condition Hold	4.0	-	0.6	-	μs
t_{LOW}(1)	SCL Low-level Time	4.7	-	1.3	-	μs
t_{HIGH}(1)	SCL High-level Time	4	-	0.6	-	μs
$t_{SU;STA}$(1)	Repeated Start Condition Setup	4.7	-	0.6	-	μs
$t_{HD;DAT}$	Data Hold	0	-	0	-	μs
$t_{SU;DAT}$	Data Setup	30+t_{I2C_REFCLK}(2)	-	30+t_{I2C_REFCLK}(2)	-	ns
t_R(1)	SCL/SDA Rising Time	-	1000	-	300	ns
t_F(1)	SCL/SDA Falling Time	-	300	-	300	ns
$t_{SU;STO}$(1)	STOP Condition Setup	4	-	0.6	-	μs
t_{BUF}(1)	Bus Free Time between Stop and Start Conditions	4.7	-	1.3	-	μs
C_b(1)	Load Capacitance	-	400	-	400	pF

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. The t_{I2C_REFCLK}, i.e., the I2C reference clock period, is determined by the I2C_CCR.FREQ bit.

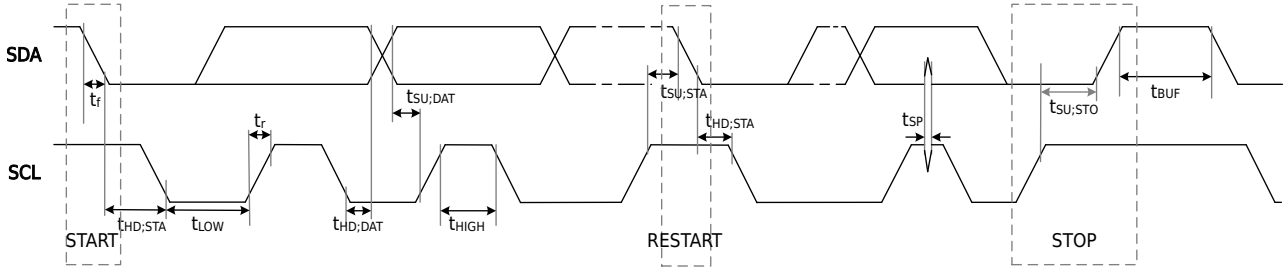


Figure 4-6 I2C Bus Timing Definition

4.3.14 SPI Interface Characteristics

Table 4-29 SPI Interface Characteristics

Symbol	Parameters	Conditions	Min	Max	Unit
$t_w(SCKH)^{(1)}$	SCK high-level time	Master mode(4)	T_{PCLK1}-1(5)	T_{PCLK1}+1(5)	ns
		Slave mode(4)	3*T_{PCLK1}-1(5)	3*T_{PCLK1}+1(5)	ns
$t_w(SCKL)^{(1)}$	SCK low-level time	Master mode(4)	T_{PCLK1}-1(5)	T_{PCLK1}+1(5)	ns
		Slave mode(4)	3*T_{PCLK1}-1(5)	3*T_{PCLK1}+1(5)	ns
$t_{su}(SI)$	Data input setup time	Slave mode	4	-	ns
$t_h(SI)$	Data input hold time	Slave mode	3	-	ns
$t_v(SO)$	Data output valid time	Slave mode	-	26	ns
$t_{su}(MI)$	Data input setup time	Master mode	9	-	ns
$t_h(MI)$	Data input hold time	Master mode	T_{PCLK1}(5)	-	ns
$t_{su}(SS)^{(1)}$	SS setup time	Slave mode	6*T_{PCLK1}(5)	-	ns
		Master mode	-10+N*T_{SCK}(2)(5)	-	ns
$t_h(SS)^{(1)}$	SS hold time	Slave mode	6*T_{PCLK1}(5)	-	ns
		Master mode	-10+N*T_{SCK}(3)(5)	-	ns
$t_v(MO)$	Data output valid time	Master mode	-	9	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. N=1-8, determined by register SPI_CFG1.MSSI.
3. N=1-8, determined by register SPI_CFG1.MSSDL.
4. The values of $t_w(SCKH)$ and $t_w(SCKL)$ are determined by SPI_CFG2.MBR. The values listed in the table are for SPI_CFG2.MBR=0.
5. T_{PCLK1} refers to 1 period of clock PCLK1, and T_{SCK} refers to 1 period of SPI communication clock.

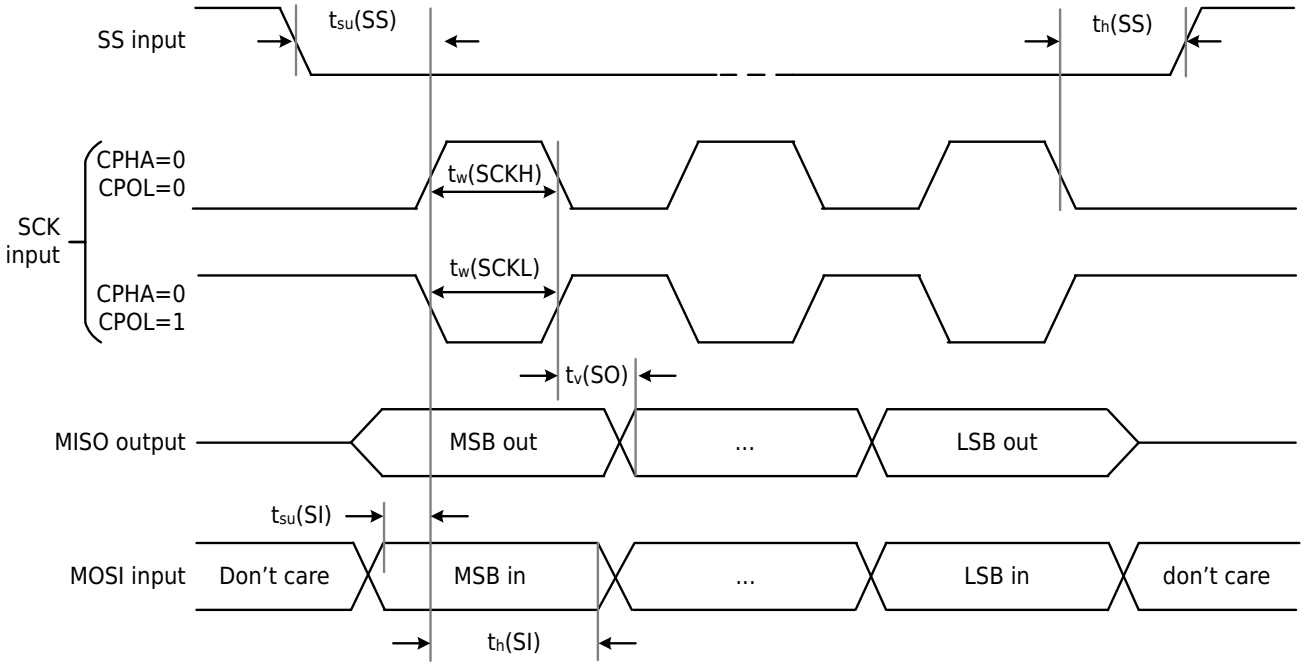


Figure 4-7 SPI Timing Definition (Slave mode, CPHA=0)

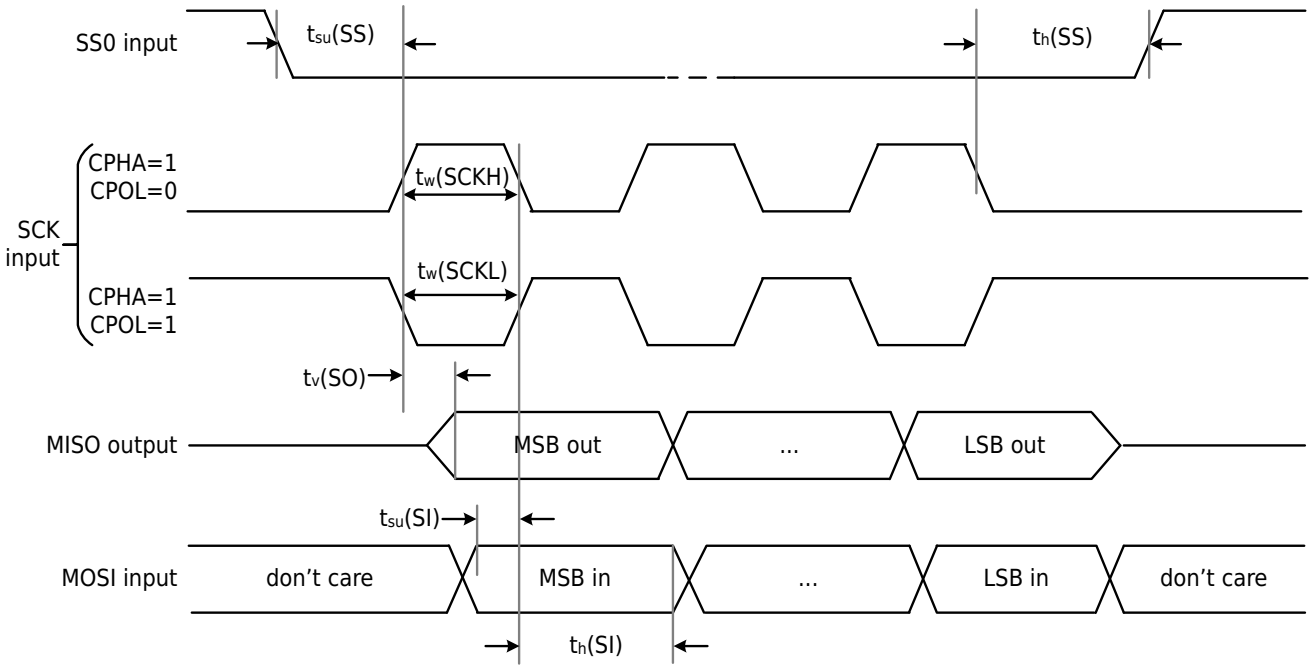


Figure 4-8 SPI Timing Definition (Slave mode, CPHA=1)

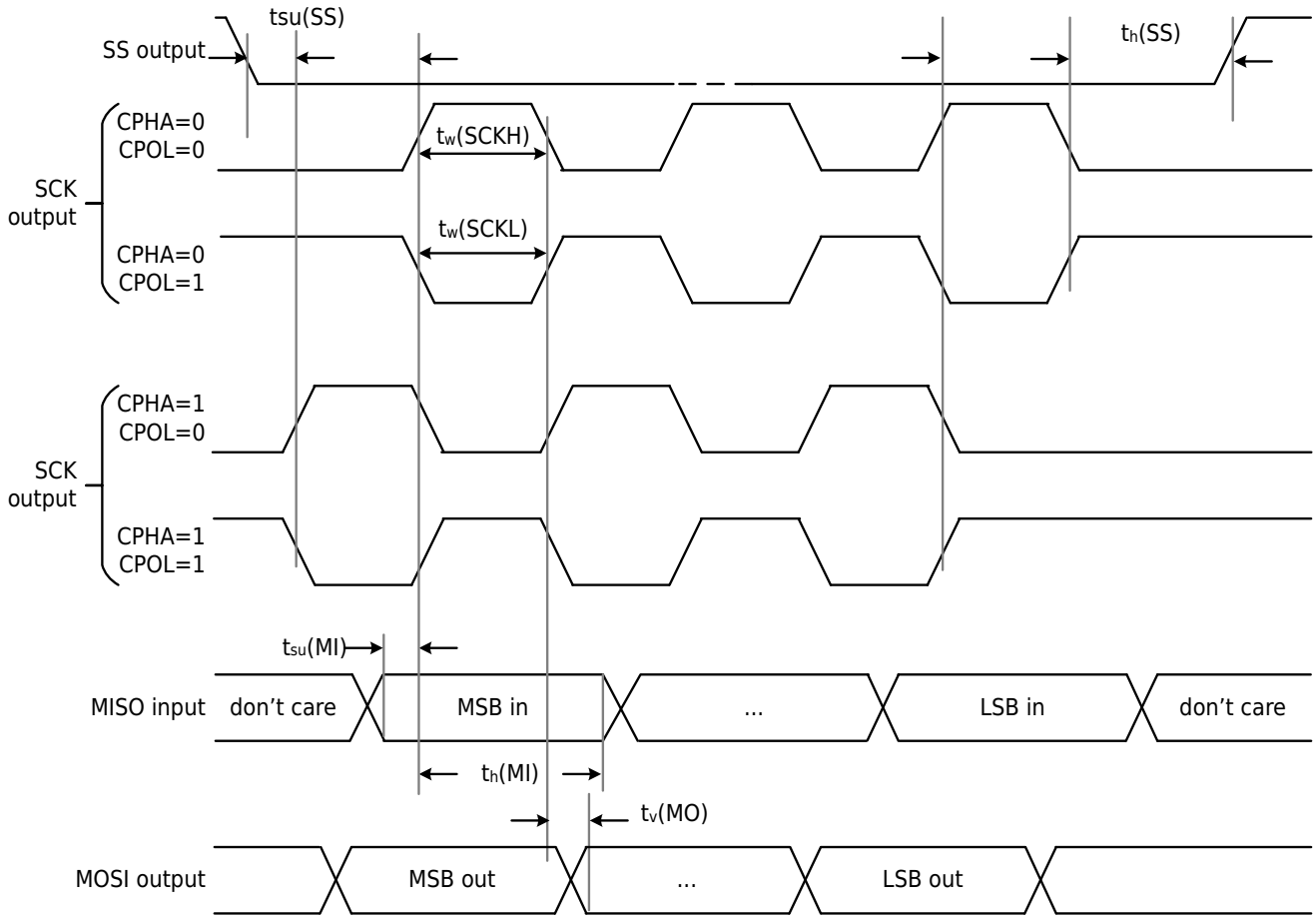


Figure 4-9 SPI Timing Definition (Master mode)

4.3.15 USART Interface Characteristics

Table 4-30 USART AC Timing[1]

Symbol	Parameters	Conditions	Min	Max	Unit
t_{cyc}	Input clock cycles	UART	4	-	t_{PCLK1}
		Clock Synchronization Mode	6	-	
t_{CKw}	Input clock width	-	0.4	0.6	t_{cyc}
t_{CKr}	Input clock rising time	-	-	5	ns
t_{CKf}	Input clock falling time	-	-	5	ns
t_{TD}	Transmission delay time	Clock Synchronization Mode	-	30	ns
t_{RDS}	Received data setup time	Clock Synchronization Mode	17	-	ns
t_{RDH}	Received data hold time	Clock Synchronization Mode	5	-	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-31 USART Maximum Baud Rate

Mode		Max Baud Rate
UART	Internal Clock Source	PCLK1/8
	External Clock Source	PCLK1/32
Clock Synchronous Mode		8.0 Mbps

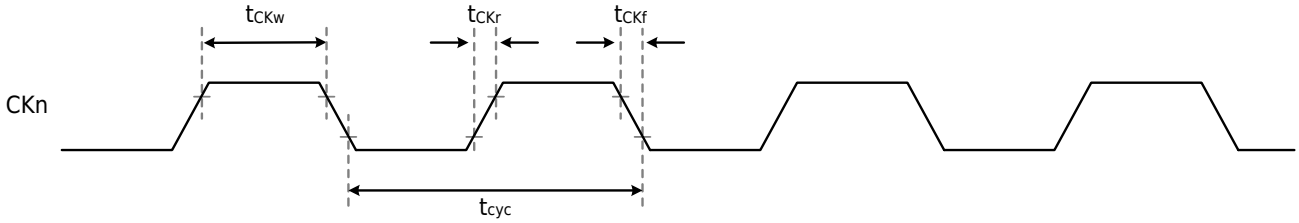


Figure 4-10 USART Clock Timing

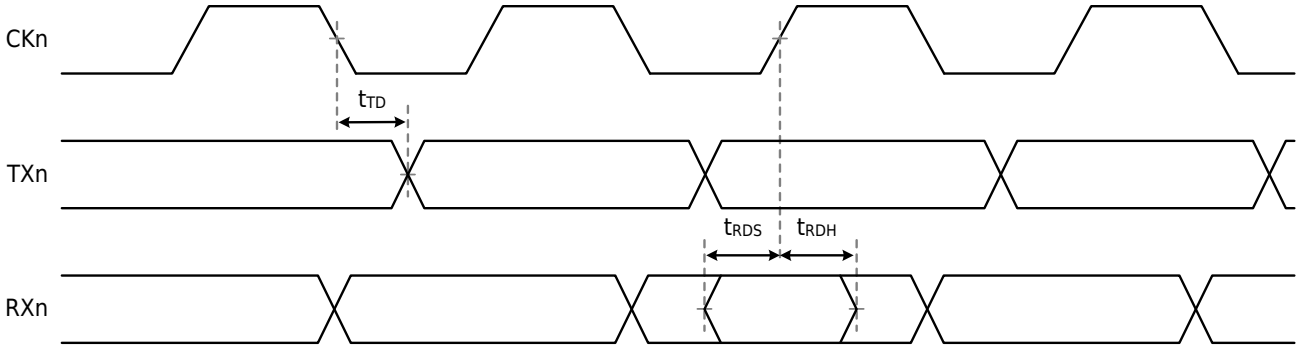


Figure 4-11 USART (CSI) Input/Output Timing

Note

The value of n in the diagram ranges from 1 to 4.

4.3.16 SWD Interface Characteristics

Table 4-32 SWD Interface Characteristics

Symbol	Parameters	Min	Typ	Max	Unit
$t_{SWCLKcyc}$ (1)	SWCLK Clock Period	50	-	-	ns
t_{SWCLKH} (1)	SWCLK Clock High Level	15	-	-	ns
t_{SWCLKL} (1)	SWCLK Clock Low Level	15	-	-	ns
t_{SWCLKr} (1)	SWCLK Clock Rising Time	-	-	5	ns
t_{SWCLKf} (1)	SWCLK Clock Falling Time	-	-	5	ns
t_{SWDIs}	SWDI Setup Time	10	-	-	ns
t_{SWDIh}	SWDI Hold Time	10	-	-	ns
t_{SWDOd}	SWDO Data Delay	-	-	28	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.

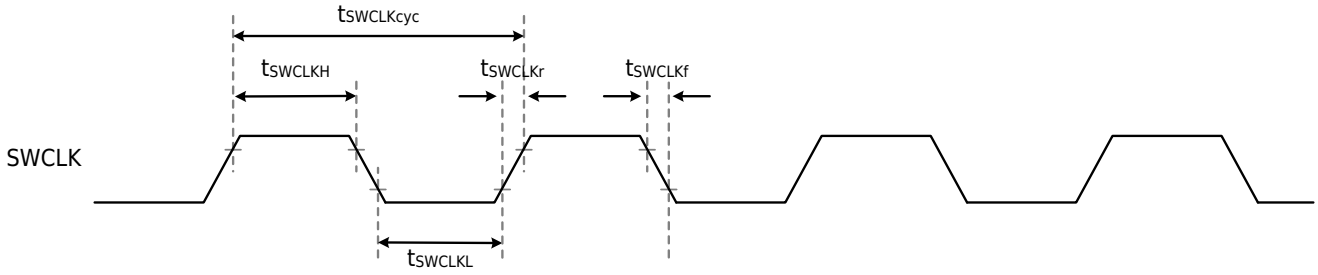


Figure 4-12 SWCLK Clock

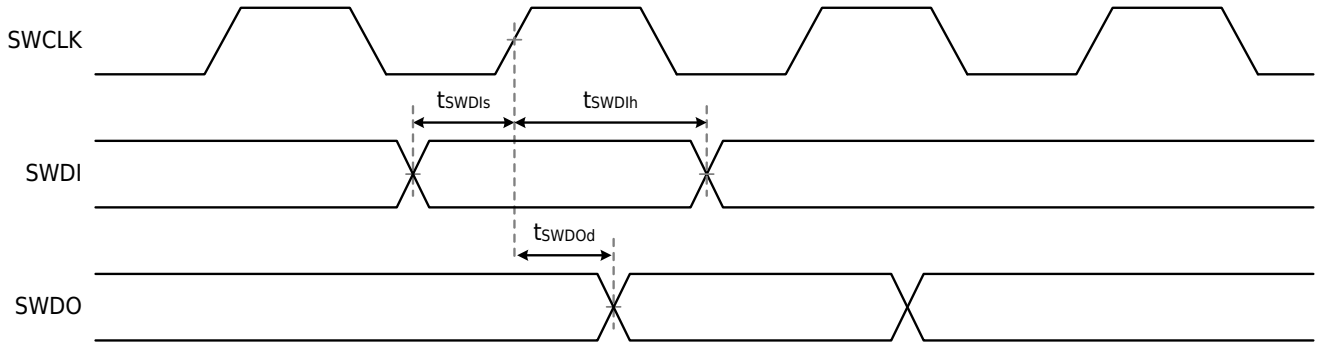


Figure 4-13 SWDIO Input/Output

4.3.17 12-bit ADC Characteristics

Table 4-33 ADC Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{AVCC/VREFH}$ (2)	Power Supply	-	2.7	-	5.5	V
f_{ADC} (2)	ADC Conversion Clock Frequency	Reference voltage is VREFH/AVCC	-	-	80	MHz
		Reference voltage is internal 2.5V/4.2V	-	-	22	MHz
V_{AIN} (2)	Conversion Voltage Range	-	V_{AVSS}	-	$V_{AVCC/VREFH}$	V
R_{AIN} (1)	External Input Impedance	-	-	-	2	kΩ
R_{ADC} (1)	Sampling Switch Resistance	-	-	1.5	-	kΩ
C_{ADC} (1)	Internal Sample and Hold Capacitance	-	-	5.1	-	pF
t_S (1)	Sampling Time	f_{ADC}=80MHz	0.1	-	3.188	μs
			8	-	255	1/ f_{ADC}
t_{CONV} (1)	Single Channel Total Conversion Time (Includes sampling time, calculated as: Sampling Time Ts + 14)	f_{ADC}=80MHz	0.275	-	-	μs
			22	-	269	1/ f_{ADC}
f_S (1)	Sampling Rate	-	-	-	3.6	Msps

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
t_{ST}(1)	Startup Time	-	-	-	5	μs

Note

1. Guaranteed by design, not tested in production.
2. Resulted from comprehensive evaluation, not tested in production.

Formula 1: R_{AIN} maximum formula

$$R_{AIN} = \frac{k}{f_{ADC} * C_{ADC} * \ln\left(2^{N+2}\right)} - R_{ADC}$$

The above formula (Formula 1) is used to determine the maximum external impedance that makes the error less than 1/4LSB. Where, N=12 (12-bit resolution), and k is the number of sampling periods defined in the ADC_SSTR register.

Table 4-34 Input Channel Static Accuracy @ f_{ADC}=80MHz(1)

Symbol	Parameters	Conditions	Min	Max	Unit
E_T	Total Unadjustable Error	f_{ADC}=80MHz VREFH as reference V_{AVCC}=2.7V/5.5V T_A=-40℃/105℃	±5.5	±7	LSB
E_O	Offset Error		±4.5	±7	LSB
E_G	Gain Error		±4.5	±7	LSB
E_D	Differential Nonlinearity Error		±1.5	±3	LSB
E_L	Integral Nonlinearity Error		±2.0	±4	LSB

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-35 Input Channel Dynamic Accuracy @ f_{ADC}=80MHz(1)

Symbol	Parameters	Conditions	Min	Max	Unit
ENOB	Effective Number of Bits	f_{ADC}=80MHz Input signal frequency = 2kHz Input source impedance = 0Ω V_{AVCC}=2.7V/5.5V T_A=-40℃/105℃	10	-	Bits
SINAD	Signal-to-noise and Distortion Ratio		62.0	-	dB
SNR	Signal-to-noise Ratio		62.1	-	dB
THD	Total Harmonic Distortion		-	-78.1	dB

Note

1. Resulted from comprehensive evaluation, not tested in production.

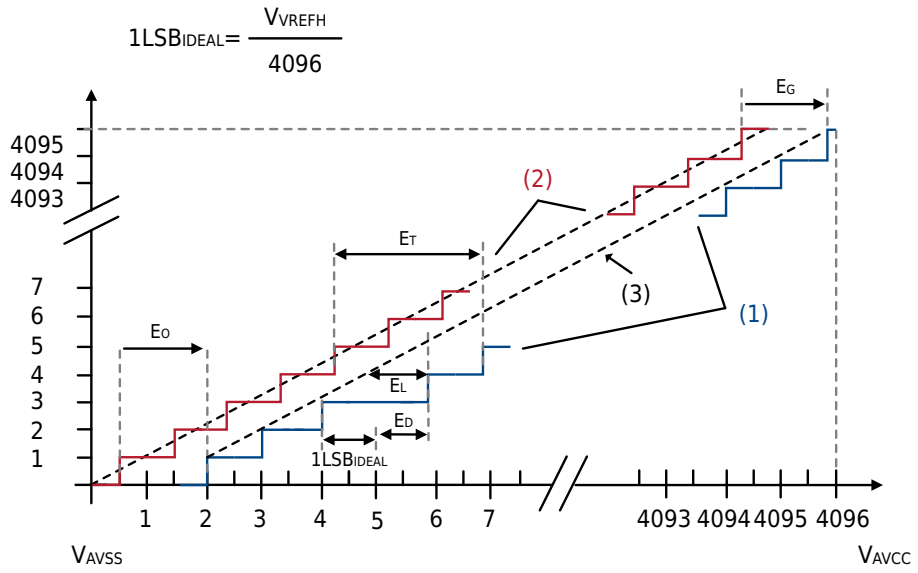


Figure 4-14 ADC Accuracy Characteristics

1. Example of actual transfer curve.
2. Ideal transfer curve.
3. Endpoint correlation line.
4. E_T = Total Unadjusted Error: Maximum deviation between actual and ideal transfer curves.
   E_O = Offset Error: Deviation between the first actual conversion and the first ideal conversion.
   E_G = Gain Error: Deviation between the last ideal conversion and the last actual conversion.
   E_D = Differential Nonlinearity Error: Maximum deviation between actual step and ideal value.
   E_L = Integral Nonlinearity Error: Maximum deviation between any actual conversion and the endpoint correlation line.

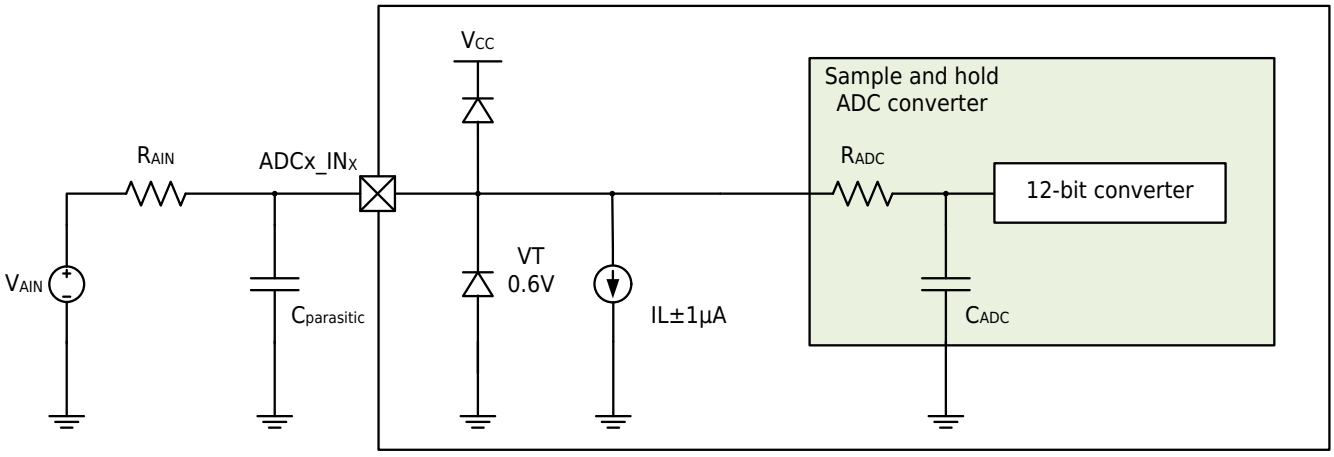


Figure 4-15 Typical Connection Using ADC

1. For information on R_{AIN}, R_{ADC}, and C_{ADC} values, refer to Table 4-33 : ADC Characteristics.
2. $C_{parasitic}$ indicates PCB capacitance (depending on the quality of soldering and PCB wiring) and bonding pad capacitance (about 5pF). Higher values of $C_{parasitic}$ result in less accurate conversions. To solve this problem, f_{ADC} should be reduced.

General PCB Design Guidelines

The power supply should be decoupled as shown in the figure below. The 0.1μF capacitor should be a (high-quality) ceramic capacitor. These capacitor should be placed as close to the chip as possible.

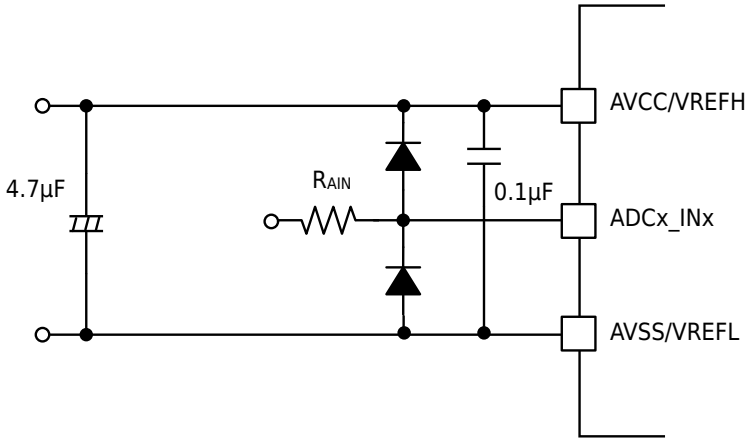


Figure 4-16 Example of Power Supply and Reference Supply Decoupling

1. For information on R_{AIN} value, refer to Table 4-33 : ADC Characteristics.

4.3.18 12-bit DAC Characteristics

Table 4-36 12-bit DAC Characteristics with Output Disabled

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{AVCC}(2)	Analog Power Voltage	-	2.7	5.0	5.5	V
AO(2)	Output Voltage Range	Reference voltage is AVCC	0	-	V_{AVCC}-1LSB	V
		Reference voltage is internal 1.2V	0	-	V_{REF12}-1LSB	V
DNL	Differential Non-linearity Error (deviation between two consecutive codes)	-	-	-	±3	LSB
TUE(2)	Total Unadjustable Error	Reference voltage is AVCC	-	-	±5	LSB
T_{wakeup}(1)	Startup Time (DAC enabled, output settled to ±1 LSB)	-	-	0.1	1	µs
T_{dacst}(1)	Setup Time (for 12-bit input code transition from lowest to highest code, until DAC output reaches final value ±1LSB)	-	-	214	291	ns
	Setup Time (for 12-bit input code transition from lowest to highest code, until DAC output reaches final value ±16LSB)	-	-	155	200	ns

Note

1. Guaranteed by design, not tested in production.
2. Resulted from comprehensive evaluation, not tested in production.

4.3.19 Comparator Characteristics

Table 4-37 Comparator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{AVCC}(2)	Analog Power Voltage	-	2.7	5.0	5.5	V
V_I(2)	Input Voltage Range	-	0	-	V_{AVCC}	V
V_{offset}(2)	Input Offset Voltage	-	-	-	10	mV
V_{hyst}(2)	Hysteresis Voltage	CMP_MDR.HYST=0b000	-	0	-	mV
		CMP_MDR.HYST=0b001	-	10	-	mV
		CMP_MDR.HYST=0b010	-	20	-	mV
		CMP_MDR.HYST=0b011	-	30	-	mV
		CMP_MDR.HYST=0b100	-	40	-	mV
		CMP_MDR.HYST=0b101	-	50	-	mV
		CMP_MDR.HYST=0b110	-	60	-	mV
		CMP_MDR.HYST=0b111	-	70	-	mV
T_{cmp}(1)	Comparison Time	Comparator resolution voltage = 100mV	-	-	100	ns
T_{start}(1)	Stabilization Time	-	-	-	300	ns
T_{set}(2)	Stabilization Time for Input Channel Switching	-	-	100	200	ns

Note

1. Guaranteed by design, not tested in production.
2. Resulted from comprehensive evaluation, not tested in production.

4.3.20 OPA Characteristics

Table 4-38 OPA Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{AVCC}(2)	Analog Power Voltage	-	2.7	5.0	5.5	V
I_{CMR}(1)	Input Common Mode Range	-	0	-	V_{AVCC}-1.2	V
V_{OUT}(1)	Output Voltage Range	-	0.2	-	V_{AVCC}-0.2	V
V_{OS}(2)	Input Offset Voltage	T_A=-40-105℃ V_{AVCC}=2.7-5.5V	-	±2	-	mV
C_{LOAD}(2)	Output Load Capacitance	-	-	-	50	pF
R_{LOAD}(2)	Output Load Resistance	-	10K	-	-	Ω
SR(1)	Slew Rate	rising/falling	-	10	-	V/us
GBW(1)	Unity Gain Bandwidth	-	-	13	-	MHz
G_{DC}(1)	DC gain	-	-	100	-	dB
CMRR(1)	Common Mode Rejection Ratio	V_{IN}=0.2V-V_{AVCC}-1.2	-	100	-	dB
PSRR(1)	Power Supply Rejection Ratio	V_{IN}=0.2V-V_{AVCC}-1.2	-	75	-	dB
T_{set}(2)	Setup Time	-	-	-	5	μs
I_{LOAD}(2)	Output Current	V_{AVCC}=5.0V V_{OUT}=1V or V_{AVCC}-1V OPAxP-OPAxN=100mV	30	-	-	mA

Note

1. Guaranteed by design, not tested in production.
2. Resulted from comprehensive evaluation, not tested in production.

4.3.21 EIRQ Filter Characteristics

Table 4-39 EIRQ Filter Characteristics(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
W_{F_EIRQ}	EIRQ Input Filter Width	INTC_EIRQCR.NOCSEL=0b00	0.6	-	2.0	μs
		INTC_EIRQCR.NOCSEL=0b01	1.1	-	3.0	μs
		INTC_EIRQCR.NOCSEL=0b10	2.2	-	5.0	μs
		INTC_EIRQCR.NOCSEL=0b11	4.3	-	9.0	μs

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.22 NMI Filter Characteristics

Table 4-40 NMI Filter Characteristics(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
W_{F_NMI}	NMI Input Filter Width	INTC_NMICR.NOCSEL=0b00	0.6	-	2.0	μs
		INTC_NMICR.NOCSEL=0b01	1.1	-	3.0	μs
		INTC_NMICR.NOCSEL=0b10	2.2	-	5.0	μs
		INTC_NMICR.NOCSEL=0b11	4.3	-	9.0	μs

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.23 RX Filter Characteristics in USART1 STOP Mode

Table 4-41 RX Filter Characteristics in USART1 STOP Mode(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
W_{F_USART1}	USART1 Input Filter Width	USART1_NFC.USART1_NFS=0b00	0.6	-	2.0	μs
		USART1_NFC.USART1_NFS=0b01	1.1	-	3.0	μs
		USART1_NFC.USART1_NFS=0b10	2.2	-	5.0	μs
		USART1_NFC.USART1_NFS=0b11	4.3	-	9.0	μs

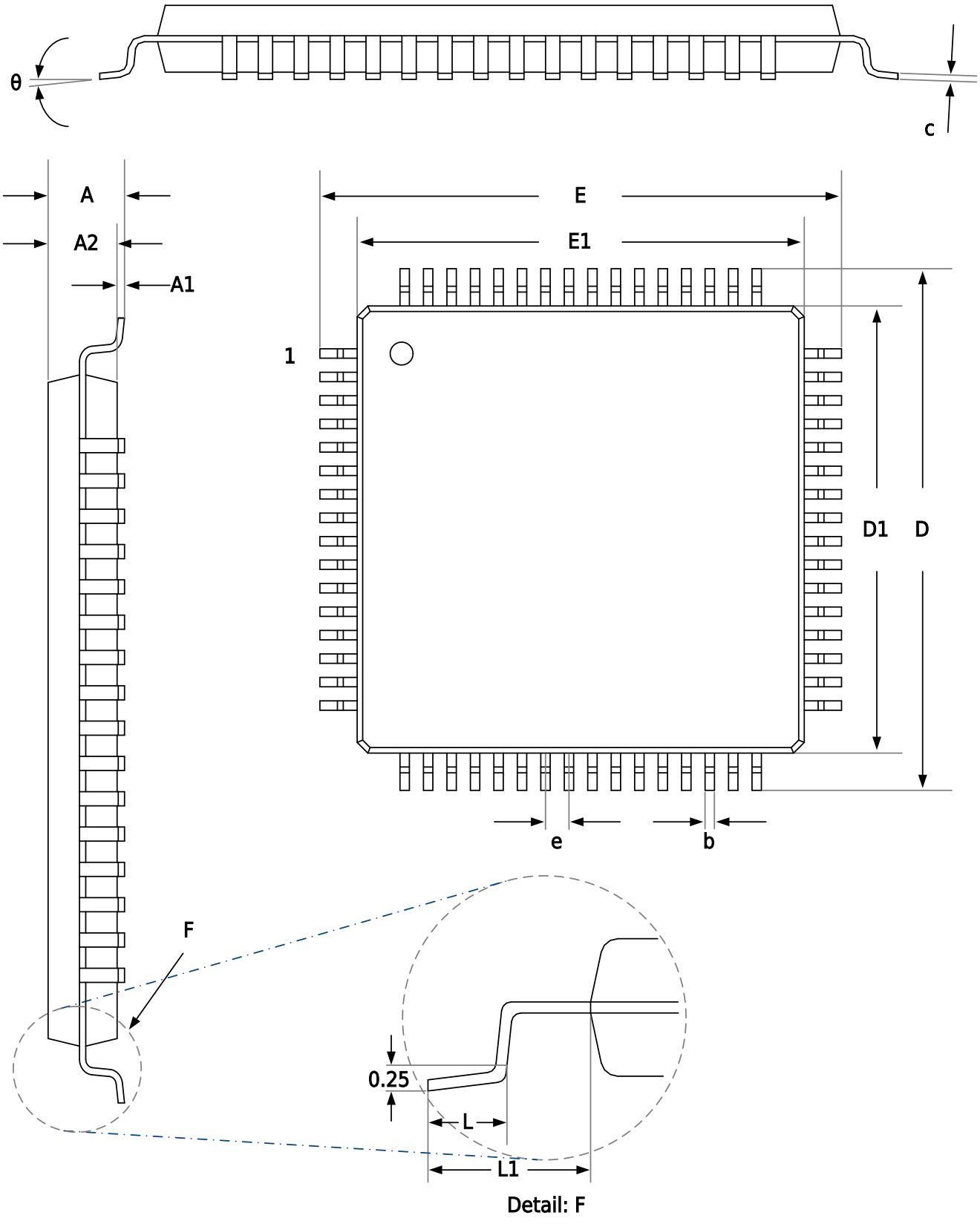
Note

1. Resulted from comprehensive evaluation, not tested in production.

5 Package Specifications

5.1 Package Dimensions

5.1.1 LQFP64 Package

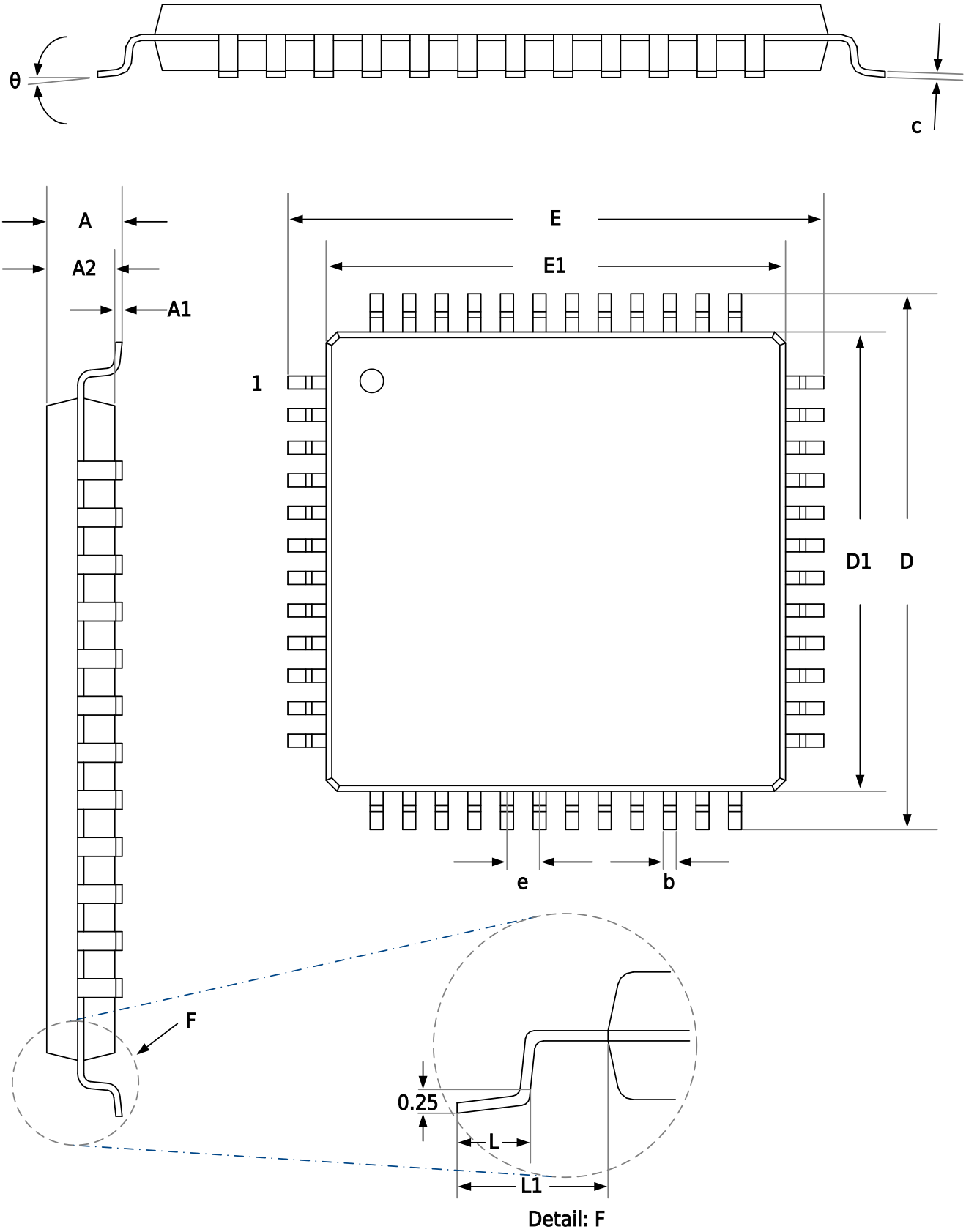


Symbol	10*10 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0°	--	7°

Note

Dimensions "D1" and "E1" do not include mold flash.

5.1.2 LQFP48 Package

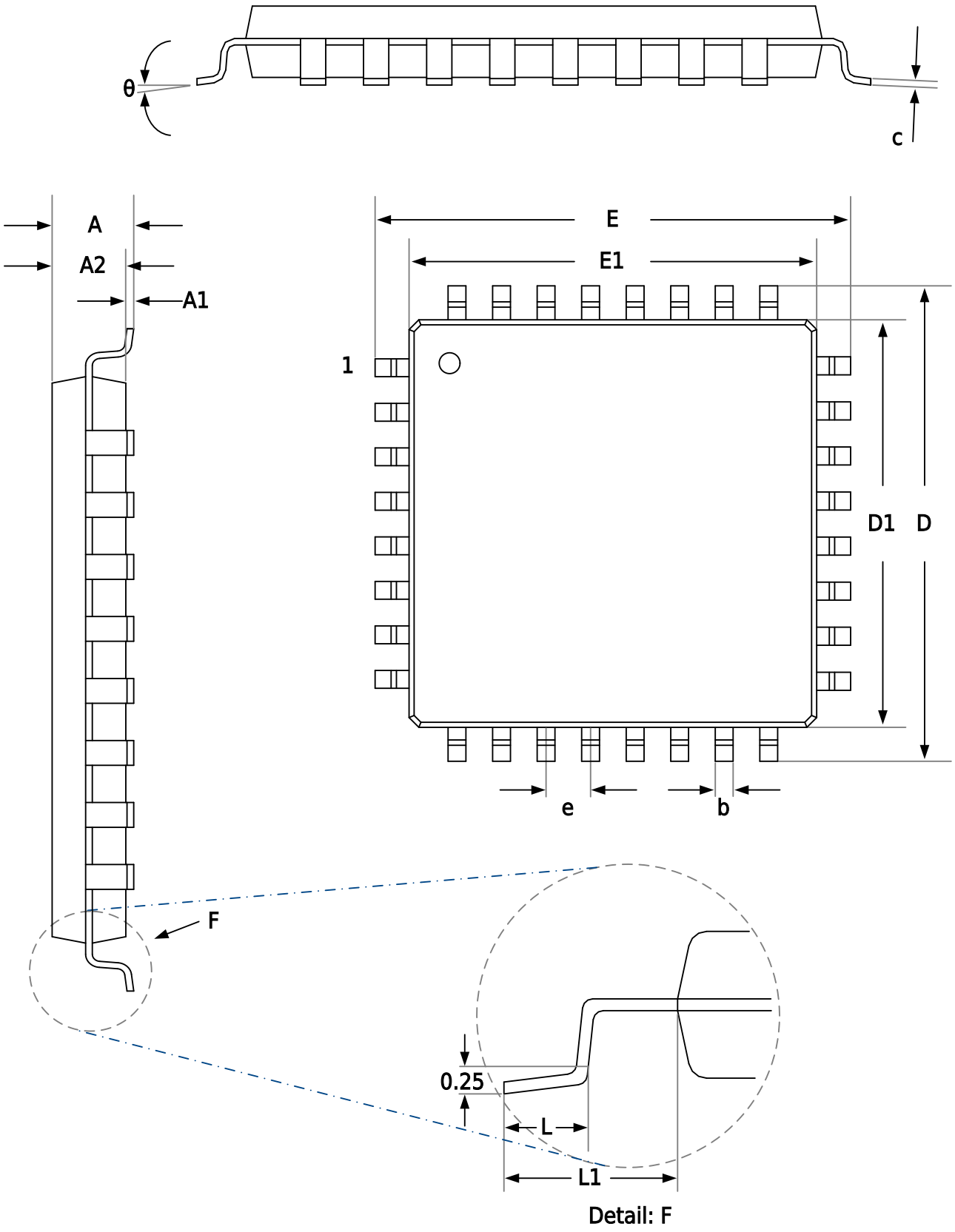


Symbol	7*7 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0	--	7°

Note

Dimensions "D1" and "E1" do not include mold flash.

5.1.3 LQFP32 Package



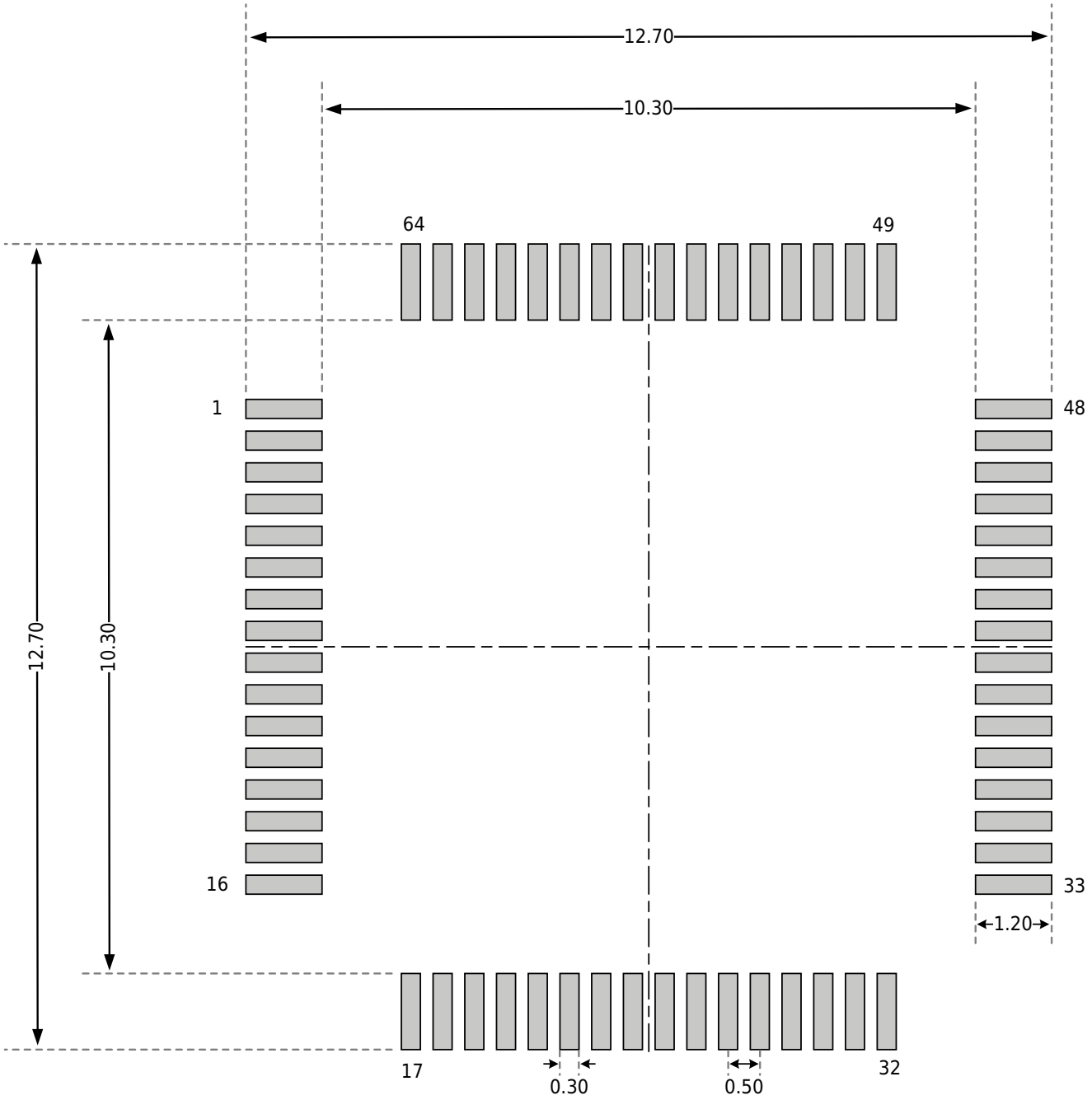
Symbol	7*7 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	--	0.45
c	0.09	--	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.80BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0	--	7°

Note

Dimensions "D1" and "E1" do not include mold flash.

5.2 PCB Land Pattern

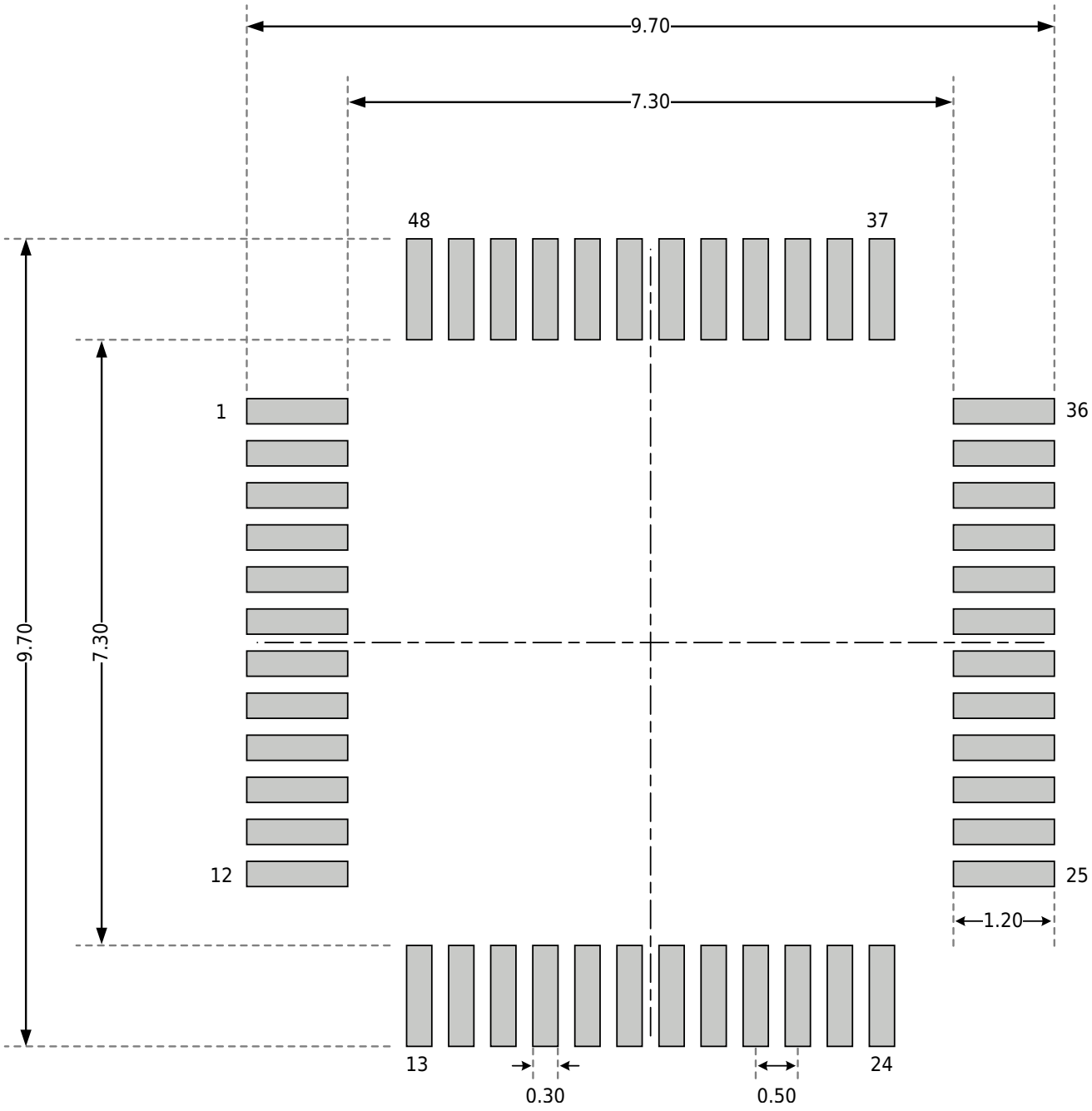
5.2.1 LQFP64 Package (10mm*10mm)



Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

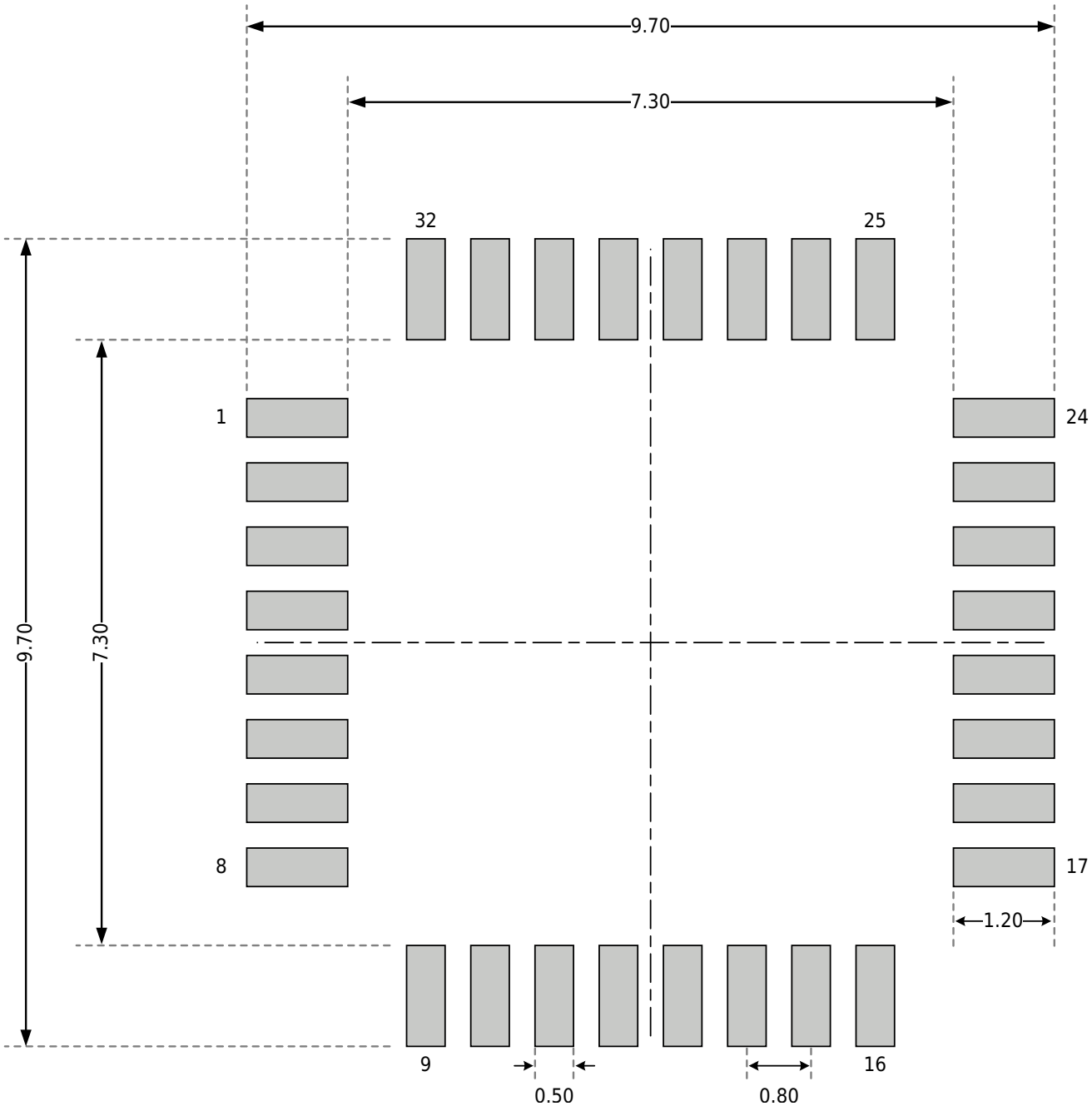
5.2.2 LQFP48 Package (7mm*7mm)



Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

5.2.3 LQFP32 Package (7mm*7mm)



Note

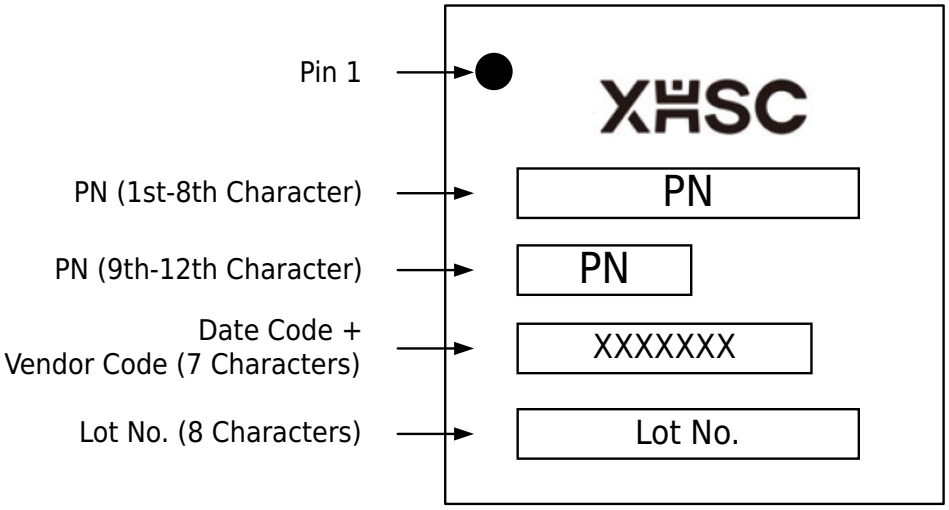
- Dimensions are in millimeters.
- Dimensions are for reference only.

5.3 Package Marking

The location and information description of Pin1 on the front of each package are given below.

LQFP64 package (10mm*10mm)

LQFP48 package (7mm*7mm)/LQFP32 package (7mm*7mm)



5.4 Packaging Thermal Resistance Coefficient

When the packaged chip is working at the specified working environment temperature, the junction temperature T_j(℃) of the chip surface can be calculated according to the following formula:

$T_j = T_A + (P_D * \theta_{JA})$

- T_A refers to the working environment temperature when the packaged chip is working, the unit is ℃;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is ℃/W;
- P_D refers to total power dissipation, which is the sum of internal power consumption (P_{INT}) and I/O pin power consumption (P_{IO}), the unit is W.

  $P_D = P_{INT} + P_{IO}$

  - P_{INT}: Internal power consumption, calculated as the product of I_{VCC} and VCC.
  - P_{IO}: I/O pin power consumption, calculated as: $P_{IO} = \Sigma(V_{OL} * I_{OL}) + \Sigma((VCC - V_{OH}) * I_{OH})$

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable junction temperature T_{Jmax} of the chip.

Table 5-4 Thermal Resistance Coefficient Reference Table For Each Package

Package Type and Dimensions	Thermal Resistance Parameters (θ_{JA})	Unit
LQFP64 10mm*10mm/0.5mm pitch	65±10%	℃/W
LQFP48 7mm*7mm/0.5mm pitch	75±10%	℃/W
LQFP32 7mm*7mm/0.8mm pitch	80±10%	℃/W

6 Ordering Information

Part Number		HC32F431KATB-LQFP64	HC32F431JATB-LQFP48	HC32F431FATB-LQFP32
GPIO		52	40	24
CPU	Core	Cortex-M4	Cortex-M4	Cortex-M4
	Frequency	120MHz	120MHz	120MHz
Memory	Flash	128KB	128KB	128KB
	SRAM	16KB	16KB	16KB
Power supply voltages		2.7~5.5V	2.7~5.5V	2.7~5.5V
Temp Range		-40~105℃	-40~105℃	-40~105℃
DMA		1unit*4ch	1unit*4ch	1unit*4ch
TIMER	Timer0	2unit	2unit	2unit
	TimerA	5unit	5unit	5unit
	Timer4	1unit	1unit	1unit
HALL		1unit*3ch	1unit*3ch	1unit*3ch
WDT		1ch	1ch	1ch
SWDT		1ch	1ch	1ch
Connectivity	USART	4ch	4ch	4ch
	I2C	1ch	1ch	1ch
	SPI	1ch	1ch	1ch
Analog	12-bit ADC	1unit, 16ch	1unit, 14ch	1unit, 6ch
	12-bit DAC	1ch	1ch	1ch
	CMP	3ch	3ch	3ch
	OPA	3ch	3ch	1ch
	PVD	√	√	√
Co-processing	DCU	√	√	√
	MAU	√	√	√
Package (mm*mm)		LQFP64(10*10)	LQFP48(7*7)	LQFP32(7*7)
Packing		Tray	Tray	Tray
Pitch		0.5mm	0.5mm	0.8mm
Thickness		1.4mm	1.4mm	1.4mm

Please contact the sales window for the latest mass production information before ordering.

Revision History

Revision/Date	Changes
Rev1.00 Jul. 24, 2026	First official release.