XIAOHUA SEMICONDUCTOR

HC32K11x Series

32-bit ARM® Cortex®-M0+ Microcontroller

Datasheet

Rev1.00

November 2025

Feature List

ARM Cortex-M0+ 32-bit MCU, 64MHz, 256KB ProgramFLASH, 32KB DataFLASH, 32KB SRAM, DMA, 7 Timers, 12-bit ADC, 1 CMP, 8 communication interfaces

- ARMv6-M architecture, 32-bit Cortex-M0+ CPU, maximum operating frequency 64MHz
- Built-in memory
  - Up to 256KByte ProgramFLASH with ECC
  - Up to 32KByte DataFLASH with ECC
  - Up to 2KByte EDataFLASH with ECC
  - Up to 32KByte SRAM with ECC
- Power, clock, and reset management
  - System power supply (VCC): 2.7-5.5V
  - 4 independent clock sources: XTAL (4-40MHz); XTAL32 (32.768kHz); HRC (up to 64MHz); LRC (32.768kHz)
  - 11 reset sources: including POR, low-voltage detection 1 reset, low-voltage detection 2 reset, NRST, etc. Each with an independent flag
- Low-power operation
  - Peripheral functions can be independently disabled or enabled
  - Low-power modes: Sleep mode, Stop mode
- Peripheral operation support system significantly reduces CPU load
  - 4-channel DMAC
  - Supports action on signal (AOS) for peripheral events
- Analog functions
  - Up to 16 channels with 12-bit 1Msps ADC, supporting single/scan conversion, triggered by various Timer events
  - 1 independent voltage comparator (CMP) with built-in 8-bit DAC
- Timers
  - 1 16-bit motor PWM Timer (Timer4), supporting 3-phase complementary PWM output
  - 1 multifunction 16-bit general-purpose Timer (TimerA), supporting input capture, output comparison, PWM output, and quadrature encoder input
  - 1 32-bit general-purpose Timer (Timer2), 1 16-bit general-purpose Timer (Timer2), both of which support asynchronous counting
  - 1 16-bit basic Timer (Timer0)
  - Real-time clock Timer (RTC)
  - 1 SWDT
- Up to 58 GPIOs
- Up to 8 communication interfaces
  - 4 USARTs (Two of which support LIN bus protocol), supporting full-duplex and half-duplex asynchronous communication
  - 2 SPIs
  - 1 I2C, supporting 7-bit/10-bit address format
  - 1 CAN FD controller (MCAN), compatible with CAN2.0A/B
- 96-bit global Unique ID
- Package types
  - QFN32 (5*5mm Wettable)
  - LQFP48 (7*7mm)
  - LQFP64 (10*10mm)
- Wide temperature range
  - -40-125℃
- Compliant with AEC-Q100 G1

Support model

HC32K118KCTJ-LQFP64	HC32K116KATJ-LQFP64
HC32K118JCTJ-LQ48	HC32K116JATJ-LQ48
HC32K118FCUJ-QFN32	HC32K116FAUJ-QFN32

Statement

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Preface

Number Format

- 0x prefix is used for hexadecimal numbers
- 0b prefix is used for binary numbers
- Numbers without prefix are in decimal representation

Security Statement

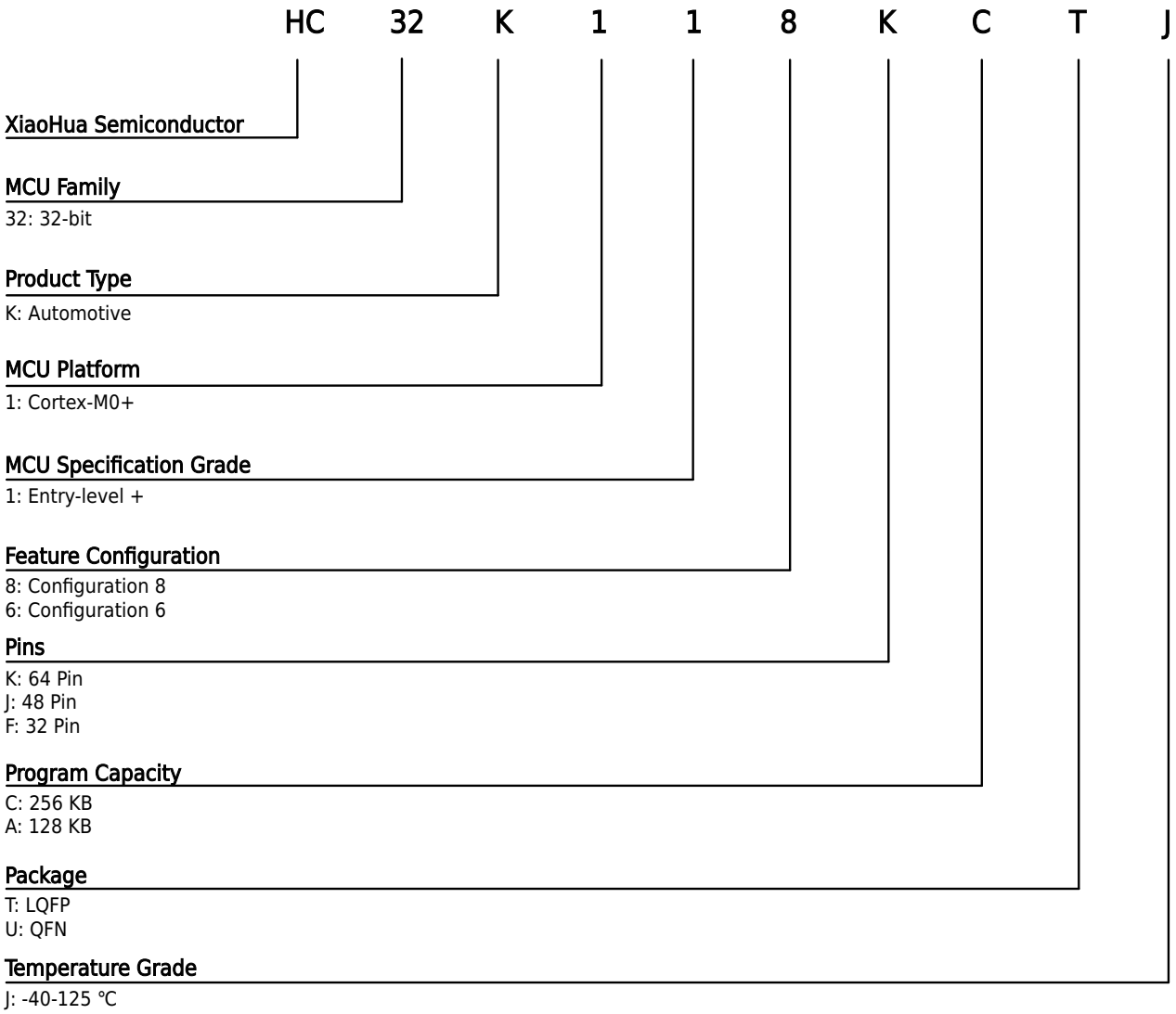
There may be potential security problems due to the use of a certain function or protocol, which need to be declared to remind users and avoid security risks.

Contents

1 Product Overview

1.1 Product Lineup

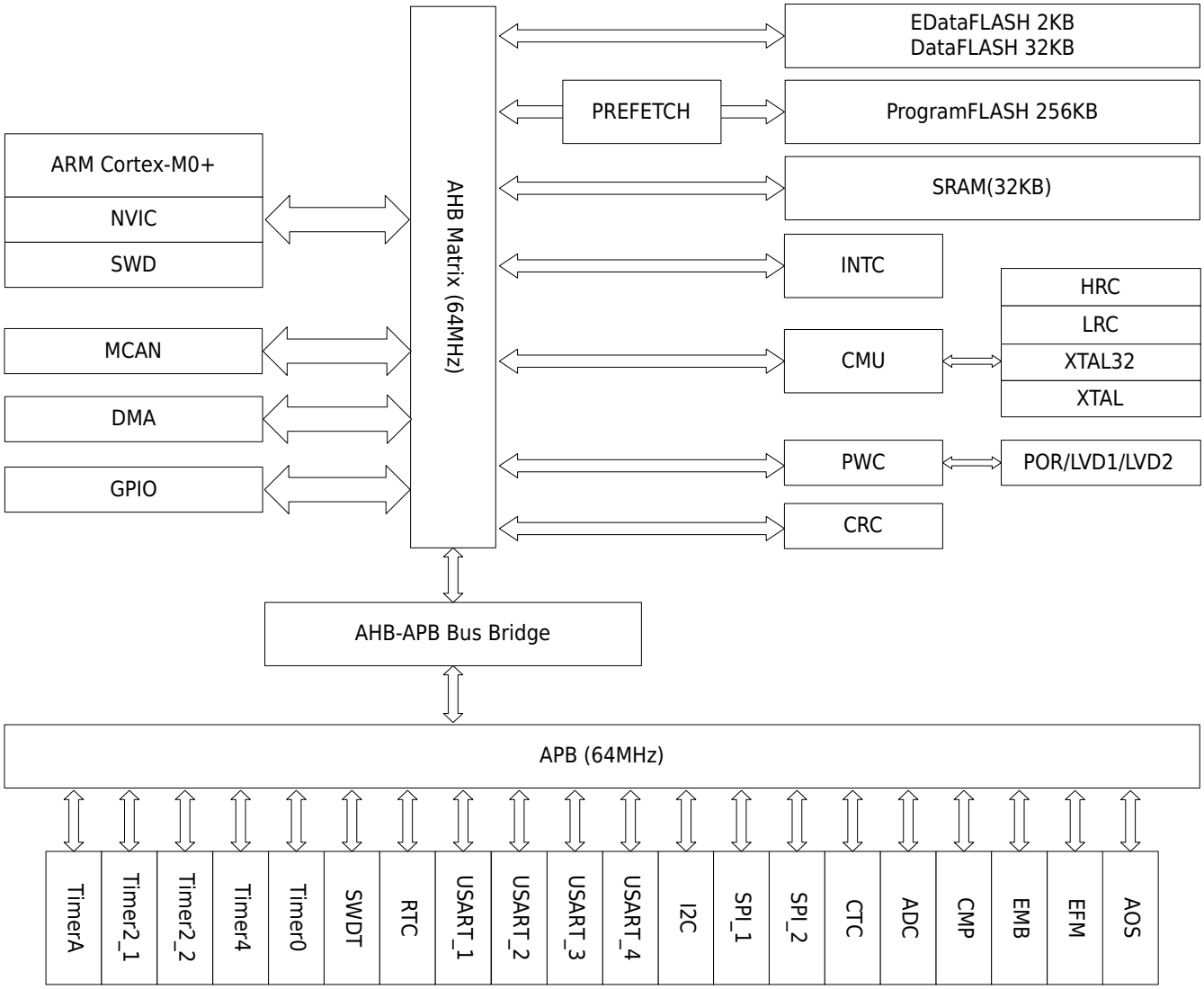
Product Name



Model Function Comparison Table

Product Name		HC32K118KCTJ	HC32K118JCTJ	HC32K118FCUJ	HC32K116KATJ	HC32K116JATJ	HC32K116FAUJ
Pins		64	48	32	64	48	32
GPIOs		58	43	28	58	43	28
CPU	Core	Cortex-M0+					
	Frequency	Maximum frequency 64MHz					
Storage Space	ProgramFLASH	256KB with ECC			128KB with ECC		
	DataFLASH	32KB with ECC					
	EDataFLASH	2KB with ECC					
	SRAM	32KB with ECC					
Clock	HRC	Maximum 64MHz					
	LRC	32.768kHz					
	XTAL	4-40MHz					
	XTAL32	32.768kHz					
Supply Voltage Range		2.7-5.5V					
Temperature Range		-40-125℃					
External Port Interrupt		EIRQ * 8					
DMA Controller		4ch					
Timer and Counter	Timer0	1unit					
	Timer2	2unit					
	TimerA	1unit					
	Timer4	1unit					
	RTC	1ch					
	SWDT	1ch					
Connectivity	USART	4ch (2ch with LIN)					
	I2C	1ch					
	SPI	2ch					
	CAN FD	1ch					
Analog	12-bit ADC	16ch	13ch	9ch	16ch	13ch	9ch
	CMP	1 built-in DAC					
LVD		2unit					
CRC		√					
CTC		1ch					
SWD		√					
Package		LQFP	LQFP	QFN	LQFP	LQFP	QFN

1.2 Functional Block Diagram



Note

Products in different packages support varying resources. For detailed specifications, please refer to Model Function Comparison Table.

2 Functional Description

2.1 CPU

HC32K11x Series integrates embedded ARM® Cortex-M0+ simplified command CPU, which realizes less pins and low power consumption, and provides excellent computing performance and rapid interrupt response capability. The on-chip integrated storage capacity can give full play to the excellent command efficiency of ARM® Cortex-M0+.

2.2 BUS

The main system consists of a 32-bit AHB bus matrix, enabling the interconnection of the following host buses and slave buses:

- Host bus
  - Cortex-M0+ core CPU bus

    The CPU fetches instructions and data via this bus, with access targets including internal memory and peripherals.
  - System DMA bus

    The system DMA has a dedicated bus through which it accesses memory and peripherals.
- Slave bus
  - FLASH bus
  - SRAM bus
  - Peripheral bus

With the bus matrix, efficient concurrent access from host buses to slave buses can be achieved. The bus matrix employs a fixed-priority arbitration scheme, where DMA access has higher priority than CPU access, to ensure the continuity of DMA data transfers.

2.3 RMU

The chip is configured with 11 reset modes:

- Power-on Reset (POR)
- NRST Pin Reset (NRST)
- Low Voltage Detect 1 Reset (LVD1R)
- Low Voltage Detect 2 Reset (LVD2R)
- Special Watchdog Reset (SWDTR)
- Software Reset (SRST)
- RAMECC Reset (RAMECCR)
- FLASHECC Reset (FLASHECCR)
- Clock Frequency Error Reset (CKFER)
- XTAL Error Reset (XTALER)
- Cortex-M0+ Lockup Reset

2.4 CMU

The clock control unit provides a series of clock functions with different frequencies, including: an external high-speed oscillator, an external low-speed oscillator, an internal high-speed oscillator, an internal low-speed oscillator, a clock prescaler, and clock gating circuit.

The clock control unit also provides a clock frequency measurement function. The clock frequency measurement circuit (FCM) monitors and measures the measurement target clock using the measurement reference clock. An interrupt or reset occurs when the setting range is exceeded.

AHB, APB, and Cortex-M0+ clocks are derived from the System Clock. The maximum operating clock frequency of the System Clock can reach 64MHz, with 4 selectable clock sources:

1. External High-speed Oscillator (XTAL)
2. External Low-speed Oscillator (XTAL32)
3. Internal High-speed Oscillator (HRC)
4. Internal Low-speed Oscillator (LRC)

For each clock source, it can be individually turned on and off when not in use to reduce power consumption.

2.5 PWC

Power controller is used to control the supply, switching and detection of multiple power domains in multiple run modes and low power modes.

The operating voltage (VCC) of the chip is 2.7V to 5.5V.

The voltage detection unit provides functions such as power-on reset (POR), power-off reset (PDR), low voltage detection 1 (LVD1), and low voltage detection 2 (LVD2). Among them, POR and PDR control the reset action of the chip by detecting the VCC voltage. LVD1 detects the VCC voltage and reset or non-maskable interrupt the chip according to the register setting. LVD2 detects the VCC voltage or external input comparison, and sets the chip to reset or non-maskable interrupt according to the register setting.

2.6 ICG

After the chip's reset is released, the hardware circuit will read the data from the ProgramFLASH addresses ranging from 0x01000A00 to 0x01000A4F and from 0x01000B00 to 0x01000B2F, as well as the DataFLASH addresses from 0x40017800 to 0x4001781F. Subsequently, it will load this data into the Initialization Configuration A (ICGA) register and the Initialization Configuration B (ICGB) register. Users can modify the ICGA register by programming, erasing specific sectors, or performing a full erase of the entire ProgramFLASH (256KB). Users can modify the ICGB register by programming or erasing specific sectors. Addresses 0x01000B00-0x01000B2F are the data security protection enable region. The register reset value is determined by FLASH data.

2.7 EFM

This product features a maximum of 256KB of ProgramFLASH, 32KB of DataFLASH, and 2KB of EDataFLASH. Programming, sector erase, and full erase operations can be performed on ProgramFLASH, DataFLASH, and EDataFLASH. ProgramFLASH can accelerate code execution through instruction prefetch.

ProgramFLASH is connected to the Flash bus and is primarily used for instruction execution and constant reading. DataFLASH and EDataFLASH are located on the AHB peripheral bus and are commonly used for data access:

- ProgramFLASH: 256KBytes capacity, 72-bit width (including 64-bit data and 8-bit ECC code), programming unit of 8Bytes, sector erase unit of 512Bytes.
- DataFLASH: 32KBytes capacity, 39-bit width (including 32-bit data and 7-bit ECC code), programming unit of 4Bytes, sector erase unit of 512Bytes.
- EDataFLASH: 2KBytes capacity, 39-bit width (including 32-bit data and 7-bit ECC code), programming unit of 4Bytes, sector erase unit of 32Bytes.

Main Features:

- ProgramFLASH and DataFLASH, EDataFLASH can implement BGO (BackGround Operation) function
- ProgramFLASH and DataFLASH each have an OTP space:
  - ProgramFLASH-OTP space (OTPA): 8 data areas, 7 of 64Bytes, 1 of 16KBytes
  - DataFLASH-OTP space (OTPB): 24 data areas, each 16Bytes
- Flash bus 8Bytes prefetching
- Supports boot swap function
- Support data security protection
- Supports MARGIN read mode, can predict Flash read errors in advance
- Provides error injection function for ECC circuit self-test
- D-BUS read protection function
- ProgramFLASH, DataFLASH and EDataFLASH have ECC (Error Checking and Correcting) function, correct 1 and detect 2, can correct 1-bit error and detect 2-bit errors for data

2.8 SRAM

This product has 32KB system SRAM.

SRAM can be accessed as a byte, half-word (16 bits), or full-word (32 bits). Read and write operations can be performed at the CPU speed.

SRAM has ECC check. The ECC check is a one-correction-two-check code, which can correct one-bit error and check 2-bit errors. When an ECC error occurs during the reading of SRAM data, an SRAM ECC check reset will be triggered.

2.9 GPIO

Main features of GPIO:

- Each port group has 18 I/O pins, which may be less than 18 depending on actual configuration
- Support pull-up and pull-down input
- Support push-pull, open-drain output mode
- Support normal and high drive modes
- Supports free switching between CMOS/Schmitt input modes
- Support for external interrupt input
- Support I/O pin peripheral function multiplexing, one I/O pin can have up to 17 optional multiplexing functions
- Individual I/O pins can be programmed independently
- Each I/O pin can select 2 functions to be enable at the same time (does not support 2 output functions to be enable at the same time)
- Some registers support the FASTIO interface, enabling single-cycle access

2.10 INTC

The interrupt controller (INTC) selects an interrupt event as an interrupt request and sends it to NVIC to wake up WFI; selects interrupt event as event input (RXEV) to wake up WFE; select low power consumption mode (Sleep mode and Stop mode) of interrupt event wake-up system ; interrupt or event control functions for external pins NMI and INTP.

The main features of INTC are as follows:

1. NVIC interrupt vector: The actual number of interrupt vectors used, please refer to the interrupt vector table chapter (excluding the 16 interrupt lines of Cortex™-M0+).

   Note

   For more instructions on exception and NVIC programming, please refer to Chapter 5: Nested Vectored Interrupt Controller in "ARM Cortex™-M0+ Technical Reference Manual".

2. Programmable priority of NVIC: 4 programmable priorities .
3. Non-maskable interrupts: In addition to the NMI pin serving as a non-maskable interrupt source, various system interrupt event requests can also be independently selected as non-maskable interrupts. Each interrupt event request is equipped with independent enable selection, flag, and flag clear registers.
4. Equipped with 8 external EIRQ pins (INTP) for interrupts.
5. Equipped with multiple interrupt events, please refer to the "Interrupt Event List" in the "Interrupt Controller (INTC)" chapter of "Reference Manual" for the specific number.
6. Interrupt wakes up system Sleep mode and Stop mode.

2.11 AOS

The Automatic Operation System (AOS) is used to achieve coordination between peripherals without the assistance of the CPU. It utilizes events generated by peripherals as AOS sources, such as timer comparison matches, timer counting overflow, RTC periodic signals, various states of the sending and receiving data of the communication module (idle, receive data full, transmit data end, transmit data empty), ADC conversion end events, etc., to trigger actions of other peripherals. The triggered peripheral actions are referred to as AOS targets.

2.12 CTC

Clock Trimming Controller (CTC) can automatically calibrate internal high-speed oscillator (HRC). Due to the influence of the working environment, the frequency of HRC may deviate. Based on the external high-precision reference clock, CTC is used to automatically adjust the frequency of HRC by hardware to get an accurate HRC clock.

The CTC main features are as follows:

- Three external reference clock sources: XTAL, XTAL32, CTCREF
- 16-bit calibration counter for frequency measurement with reload function
- 8-bit calibration deviation value and 4-bit calibration value for frequency calibration
- Error interrupt for indicating calibration failure

2.13 DMA

DMA is used to transfer data between memory and peripheral function modules, enabling data exchange between memories, between memory and peripheral function modules, and between peripheral function modules without CPU involvement.

Main features of DMA:

- The DMA bus is independent of the CPU bus and transmits data according to the AMBA AHB-Lite bus protocol
- With 4 independent channels, which can independently operate different DMA transfer functions
- The start source of each channel is configured through an independent trigger source selection register
- 1 block per request
- The data block is a minimum of one data and can be up to 256 data
- The width of each data item can be configured as 8-bit, 16-bit, or 32-bit
- It can be configured for 1-1023 transfers or infinite transfers
- The source address and destination address can be independently configured as fixed, incrementing, decrementing, repeated jump, or specified offset jump
- 3 types of interrupts can be generated: block transfer completed interrupt, transfer completed interrupt, and transfer error interrupt. Each interrupt can be configured to be masked or unmasked. Among them, block transfer completed and transfer completed can be used as event outputs, serving as trigger sources for other peripheral modules
- Support chain transfer function, enabling the transfer of multiple data blocks in a single request
- When not in use, it can be set to stop state to reduce power consumption

2.14 CMP

Voltage Comparator (hereinafter referred to as CMP) is a peripheral module that compares two analog voltages and outputs the comparison result. This product is equipped with 1 comparison channel CMP.

CMP Main features:

- 1 comparison channels can independently perform normal comparison
- Each comparison channel's positive and negative voltage inputs have multiple input sources to choose from
- An 8-bit Digital-to-Analog Converter (8-bit DAC) provides one independent internal comparison voltage DA1
- A noise filter can filter the comparator output, with 7 sampling clocks to choose from
- Timer PWM can be used for comparator blanking window control
- Interrupts can be generated at the edges of comparison result changes, other peripherals can be triggered, and STOP mode can be woken up
- Compare results can be monitored through registers and output to the external pin VCOUT
- Compare results can be used for EMB control events

2.15 ADC

The 12-bit ADC is an analog-to-digital converter that adopts the successive approximation method. This MCU is equipped with 1 ADC units, a maximum of 16 channels. Analog input channels can be arbitrarily combined into a sequence for single scan or continuous scan conversion. The ADC block also includes an

analog watchdog function that monitors the conversion results of any specified channel to detect if they exceed user-set ranges.

The main features of the ADC are as follows:

- High Performance
  - Configurable 12-bit, 10-bit and 8-bit resolution
  - The A/D conversion clock (ADCLK) frequency can be selected as 1, 2, 4, 8, 16, or 32 divisions of the peripheral clock (HCLK)
  - Supports 1Msps Sampling Rate
  - Sampling time is programmable
  - Each channel has an independent data register
  - Data registers can be configured for left/right alignment
  - Analog watchdog to monitor conversion results
  - The ADC module can be set to stop when not in use
- Analog Input Channel
  - Up to 16 external analog inputs
- Conversion Start Conditions
  - Software setup conversion started
  - Peripheral synchronously trigger the conversion to start
  - External pin trigger the conversion to start
- Conversion Mode
  - 2 scan sequences A, B, optionally specifying a single or multiple channels
  - Sequence A single scan
  - Sequence A continuous scan
  - Dual sequence scan, with sequences A and B independently selecting trigger sources, and sequence B having higher priority than A
- Interrupt and Event Signal Output
  - Sequence A scan end interrupt and event ADC_EOCA
  - Sequence B scan end interrupt and event ADC_EOCB
  - Analog watchdog 0 compare interrupt and event ADC_CMP0
  - Analog watchdog 1 compare interrupt and event ADC_CMP1
  - All the event outputs mentioned above can start DMA

2.16 Timer4

The General Control Timer 4 is a timer module designed for three-phase motor control, offering a variety of solutions for different three-phase motor control applications. It supports both triangular and sawtooth waveform modes, enabling the generation of various PWM waveforms. It also features buffer functionality and supports EMB control. 1 unit of Timer4 is carried in this product family.

2.17 EMB

The emergency brake module is a function module that generates contorl events output to the timer when certain conditions are met to stop the timer or change the PWM signal output to the external motor. The following factors are used to generate control events:

- External port input level change

- Level of PWM output port occurs in phase (same high or same low)
- Voltage comparator comparison results
- System error occurred
- Write register software control

2.18 TimerA

The General Timer A (TimerA) is a timer with a 16-bit counting width and 8-channel PWM output. The timer supports two waveform modes, triangle wave and sawtooth wave, and can generate various PWM waveforms (single-side aligned PWM, double-side symmetrical PWM); supports synchronous start of counter; the compare reference value register supports buffer function; supports 2-phase quadrature encoding count and 3-phase quadrature encoding count. This product series is equipped with 1 TimerA.

2.19 Timer2

General Timer 2 (Timer2) is a basic timer with a 32/16-bit counting width that can implement synchronous and asynchronous counting modes. This timer contains 2 channels (CH-A and CH-B). Each channel has an output port, enabling basic square wave output; each channel has 2 input ports: one is a clock input port, enabling port asynchronous counting; the other is a trigger input port, enabling timer start, stop, clear, counting actions, and count value capture input; it supports pulse width measurement and period measurement; it supports free-running counting and compare stop counting. This product series incorporates 2 units of Timer2, where unit 1 has a 16-bit counting width and unit 2 has a 32-bit counting width.

2.20 Timer0

General Timer 0 (Timer0) is a basic timer that can implement both synchronous counting and asynchronous counting. This timer contains one channel, which can generate compare match events and counter overflow events during counting. These events can trigger interrupts or serve as event outputs to control other modules. This product series is equipped with one unit of Timer0.

2.21 RTC

A real time clock (RTC) is a counter that stores time information in BCD format. Record the specific calendar time from 00 to 99. Support 12/24 hour time system, automatically calculate the number of days 28, 29 (leap year), 30 and 31 according to the month and year.

2.22 SWDT

The watchdog counter is a dedicated watchdog counter (SWDT) with an internal low-speed RC (32.768kHz) as its count clock source. The dedicated watchdog is a 16-bit down counter used to monitor software faults caused by external interference or unforeseen logic conditions that cause the application to deviate from normal operation. The watchdog counter supports a window function. A window interval can be preset before counting starts. When the count value is within the window interval, the counter can be refreshed and counting restarts.

2.23 USART

This product is equipped with 4 units of Universal Synchronous Asynchronous Receiver/Transmitter (USART) modules, which can flexibly exchange full-duplex data with external devices; the USART equipped in this product supports universal asynchronous serial communication interface (UART) , clock synchronous communication interface, smart card interface (ISO/IEC7816-3) and LIN communication

interface. Support modem operation (CTS/RTS operation), multiprocessor operation, DE function, receive timeout function. USART3/USART4 supports the STOP mode wake-up function via the RX line.

The specific function allocation is as follows:

Function	Support Module			
	USART1	USART2	USART3	USART4
UART	✓	✓	✓	✓
Multiprocessor Communication	✓	✓	✓	✓
Clock Synchronization Communication	✓	✓	✓	✓
Wake-up from STOP Mode via RX Line	-	-	✓	✓
Fractional Baud Rate	✓	✓	✓	✓
LIN	-	-	✓	✓
Smart Card	✓	✓	-	-
UART Receive Timeout Function	✓	✓	✓	✓
RS485 Driver Enable	✓	✓	✓	✓

2.24 I2C

I2C (Inter-Integrated Circuit) used as an interface between the microcontroller and the I2C serial bus. Provide multi-master mode function, which can control the protocol and arbitration of all I2C buses. Standard mode and fast mode are supported. SMBus is also supported.

Main Features of I2C:

- I2C bus mode and SMBUS bus mode are optional. Master mode and slave mode are optional. Automatically ensure various preparation times, hold times, and bus idle times corresponding to the transfer rate
- Standard mode up to 100kbps, fast mode up to 400kbps
- The start condition, restart condition, and stop condition are automatically generated, and the start condition, restart condition, and stop condition of the bus can be detected
- Supports up to 128 slave mode addresses. Supports 7-bit address format and 10-bit address format. Broadcast call address, SMBus host address, SMBus device default address, SMBus alarm address can be detected
- Answer bits can be automatically determined when sent. Answer bits can be automatically sent when reception
- Handshake function
- Arbitration function
- Timeout function, can detect SCL clock stop for a long time
- SCL input and SDA input have built-in digital filters that are programmable to filter
- Communication error, receive data full, send data empty, one frame send end, address match unanimously interrupt

2.25 SPI

This product is equipped with 2-channel serial peripheral interface SPI, supports high-speed full-duplex serial synchronous transmission, and facilitates data exchange with peripheral devices. Users can set the range of 3/4-wire, master/slave and baud rate as as required.

2.26 MCAN

This product is equipped with one units of MCAN communication interface modules (MCAN), which is equipped with 1KB RAM.

CAN modules (MCAN) comply with ISO 11898-1:2015 (CAN Protocol Specification Version 2.0 Parts A, B) and CAN with Flexible Data-Rate Specification Version 1.0.

The 1KB message RAM memory can realize the filter (Rx Filter), receive FIFO (Rx FIFO), receive buffer (Rx Buffer), transmit event FIFO (Tx Event FIFO), and transmit buffer (Tx Buffer) functions.

The message RAM features ECC (Error Checking and Correcting). The ECC is a single-error-correcting, double-error-detecting (SECDED) code, meaning it can correct a single-bit error and detect a double-bit error.

2.27 CRC

The CRC algorithm of this module follows the definition of ISO/IEC13239, and adopts 32-bit CRC and 16-bit CRC respectively. The CRC32 generating polynomial is $X^{32}+ X^{26}+ X^{23}+ X^{22}+ X^{16}+ X^{12}+ X^{11}+ X^{10}+ X^{8}+ X^{7}+ X^{5}+ X^{4}+ X^{2}+ X+ 1$, and the initial value of 32 bits is 0xFFFFFFFF. The generating polynomial of CRC16 is $X^{16}+ X^{12}+ X^{5}+ 1$, and the initial value of 16 bits is 0xFFFF.

2.28 DBGC

This MCU's core is Cortex-M0+, which includes hardware for advanced debugging functions. Using these debugging functions, the core can be stopped when fetching instructions (instruction breakpoint) or accessing data (data breakpoint). When the core is stopped, the internal state of the core and the external state of the system can be queried. After the query completes, the kernel and system are restored and program execution is restored. This MCU does not incorporate an MTB (Micro Trace Buffer) debugging component. When a debugger is connected to the MCU for debugging purposes, access permissions to system resources will be determined based on the security level.

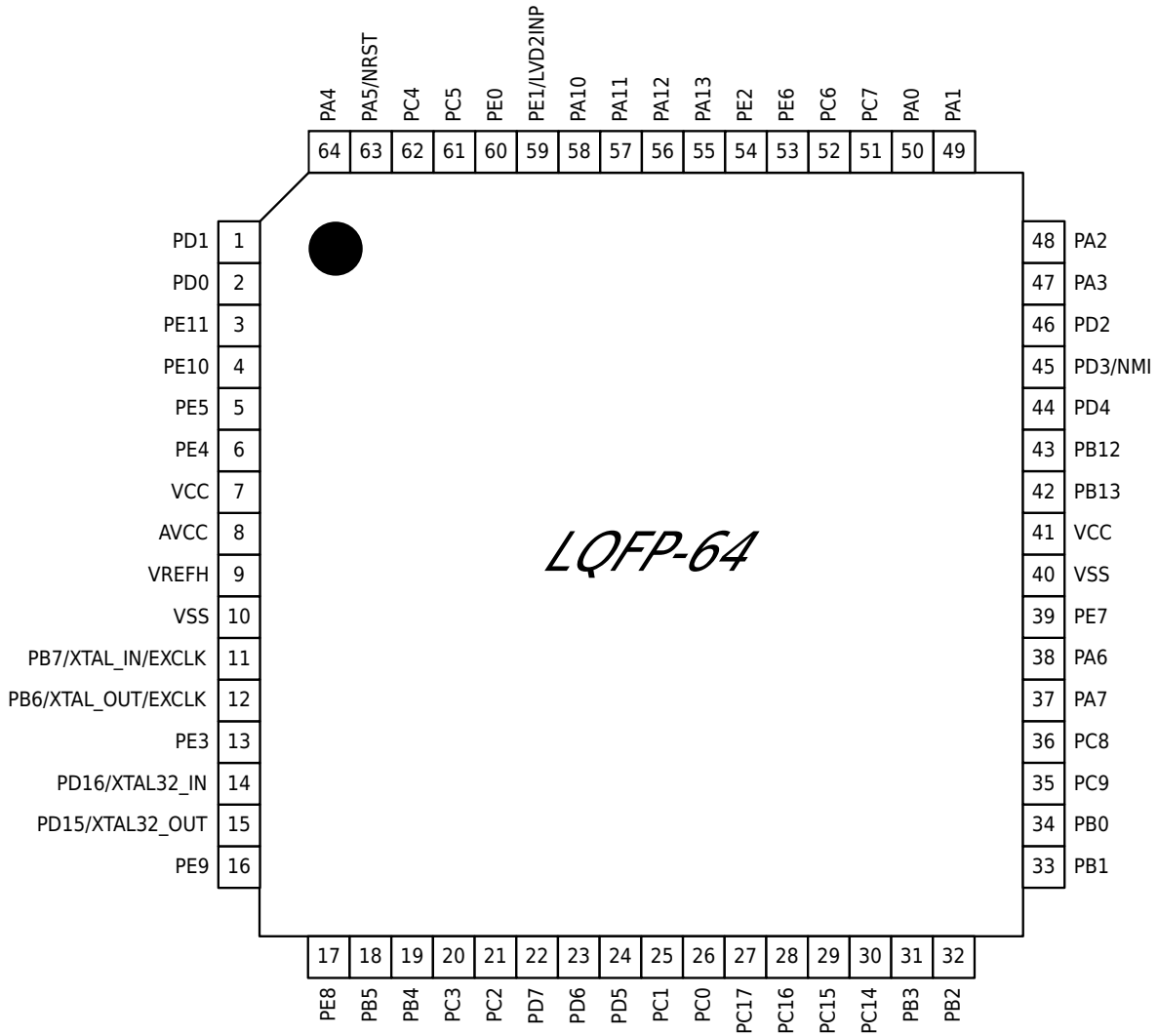
Debugging interface supported:

- Serial debug trace interface SWD

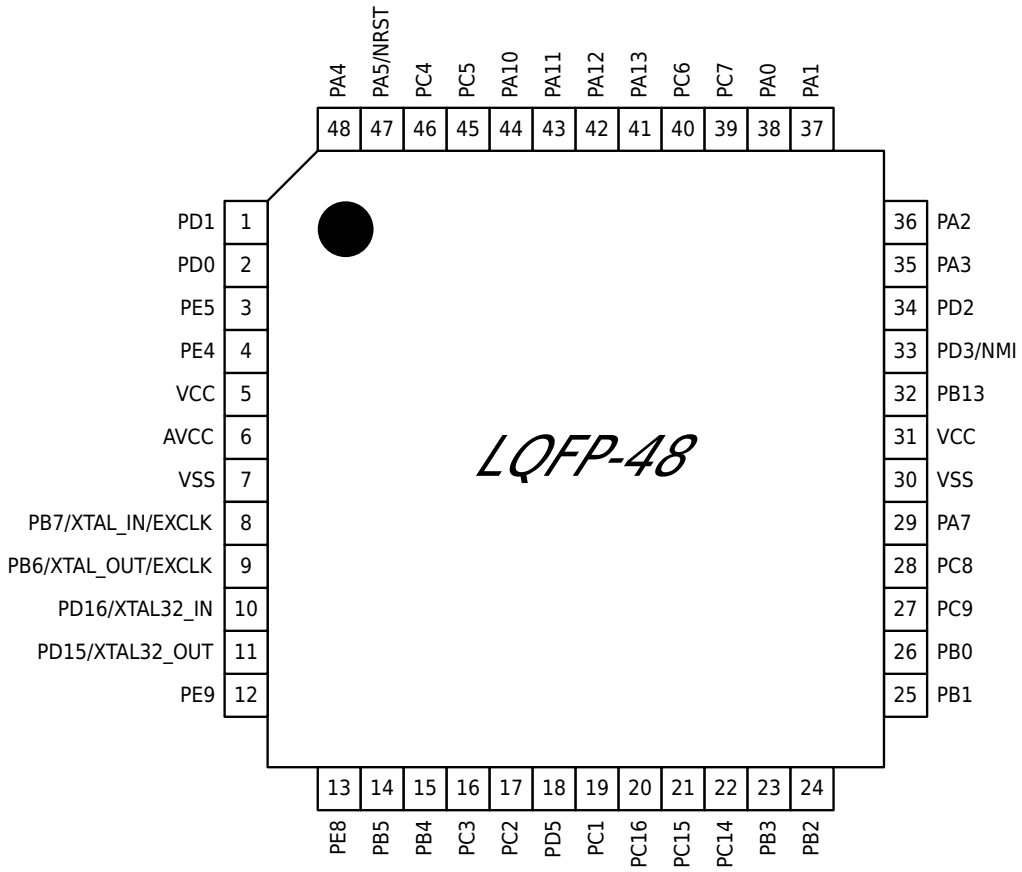
3 Pin Definitions

3.1 Pinout

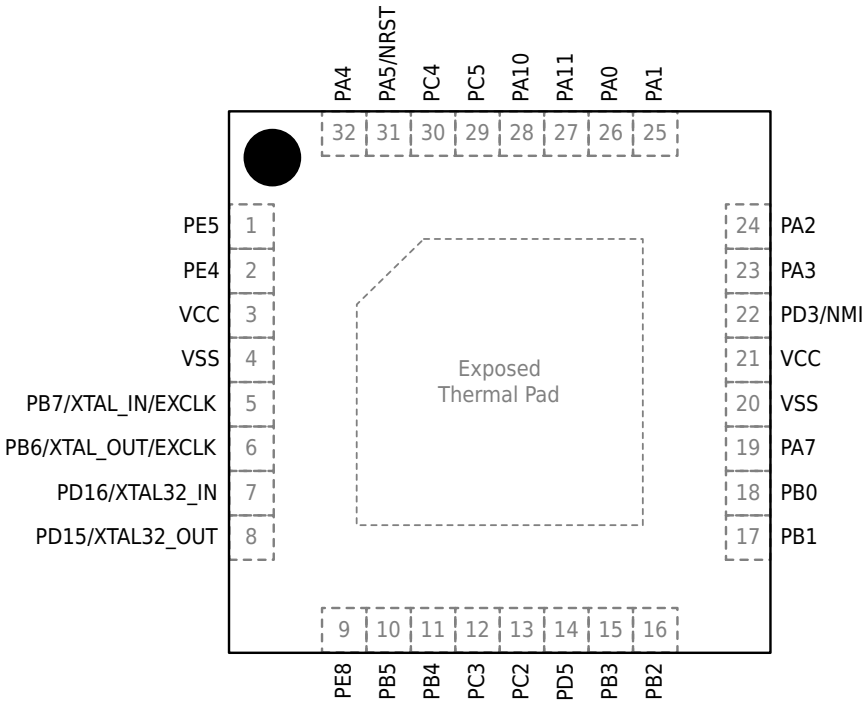
3.1.1 LQFP64 Package



3.1.2 LQFP48 Package



3.1.3 QFN32 Package



Note

Exposed Thermal Pad needs to be connected to VSS.

3.2 Pin Function Table

LQFP64	LQFP48	QFN32	Pin Name	EIRQ	SWD	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16
						GPO	Analog/other	TMRA	TMR2/TMRA	TMR4/EMB	USART	SPI/USART/CAN	SPI/I2C	EVENTPORT	IRQ	IRQ	IRQ	IRQ	IRQ	IRQ	IRQ	IRQ
1	1	-	PD1	EIRQ1	-	GPO		TMRA_PWM4		TMR4_OVL			SPI2_MISO	EVENTP31	EIRQ0		EIRQ2	EIRQ3	EIRQ4	EIRQ5	EIRQ6	EIRQ7
2	2	-	PD0	EIRQ0	-	GPO		TMRA_PWM3		TMR4_OVH			SPI2_SCK	EVENTP30		EIRQ1	EIRQ2	EIRQ3	EIRQ4	EIRQ5	EIRQ6	EIRQ7
3	-	-	PE11	EIRQ3	-	GPO			TMR2_1_CLKA					EVENTP45	EIRQ0	EIRQ1	EIRQ2		EIRQ4	EIRQ5	EIRQ6	EIRQ7
4	-	-	PE10	EIRQ2	-	GPO	MCO						SPI2_NSS1	EVENTP44	EIRQ0	EIRQ1		EIRQ3	EIRQ4	EIRQ5	EIRQ6	EIRQ7
5	3	1	PE5	EIRQ5	-	GPO	FCMREF	TMRA_TRIG	TMR2_1_PWMA	TMR4_CLK	USART1_TX	MCAN_TX			EIRQ0	EIRQ1	EIRQ2	EIRQ3	EIRQ4		EIRQ6	EIRQ7
6	4	2	PE4	EIRQ4	-	GPO		TMRA_PWM8	TMR2_1_PWMB	TMR4_ADSM	USART1_RX	MCAN_RX	SPI2_MOSI		EIRQ0	EIRQ1	EIRQ2	EIRQ3		EIRQ5	EIRQ6	EIRQ7
7	5	3	VCC	-	-																	
8	6	-	AVCC	-	-																	
9	-	-	VREFH	-	-																	
10	7	4	VSS	-	-																	
11	8	5	PB7/EXCLK	EIRQ7	-	GPO	XTAL_IN				USART2_TX		I2C1_SCL	EVENTP16	EIRQ0	EIRQ1	EIRQ2	EIRQ3	EIRQ4	EIRQ5	EIRQ6	
12	9	6	PB6/EXCLK	EIRQ6	-	GPO	XTAL_OUT				USART2_RX		I2C1_SDA	EVENTP17	EIRQ0	EIRQ1	EIRQ2	EIRQ3	EIRQ4	EIRQ5		EIRQ7
13	-	-	PE3	EIRQ3	-	GPO	VCOUT			EMB_PORT0				EVENTP43	EIRQ0	EIRQ1	EIRQ2		EIRQ4	EIRQ5	EIRQ6	EIRQ7
14	10	7	PD16	EIRQ6	-	GPO	XTAL32_IN	TMRA_PWM2	VCOUT1	TMR4_OUL		USART2_RTS/USART2_DE	SPI1_MISO		EIRQ0	EIRQ1	EIRQ2	EIRQ3	EIRQ4	EIRQ5		EIRQ7
15	11	8	PD15	EIRQ7	-	GPO	XTAL32_OUT	TMRA_PWM1		TMR4_OUH		USART2_CTS	SPI1_SCK		EIRQ0	EIRQ1	EIRQ2	EIRQ3	EIRQ4	EIRQ5	EIRQ6	
16	12	-	PE9	EIRQ1	-	GPO		TMRA_PWM8	TMR4_OWL	TMR4_OUL	TMR4_OVL				EIRQ0		EIRQ2	EIRQ3	EIRQ4	EIRQ5	EIRQ6	EIRQ7
17	13	9	PE8	EIRQ0	-	GPO	CMP_IN3	TMRA_PWM7	TMR4_OWH	TMR4_OUH	TMR4_OVH		SPI1_NSS3			EIRQ1	EIRQ2	EIRQ3	EIRQ4	EIRQ5	EIRQ6	EIRQ7
18	14	10	PB5	EIRQ5	-	GPO	MCO	TMRA_PWM6		TMR4_OWL	USART3_CK	SPI1_NSS1	SPI1_NSS0	EVENTP15	EIRQ0	EIRQ1	EIRQ2	EIRQ3	EIRQ4		EIRQ6	EIRQ7
19	15	11	PB4	EIRQ4	-	GPO	FCMREF	TMRA_PWM5		TMR4_OWH			SPI1_MOSI	EVENTP14	EIRQ0	EIRQ1	EIRQ2	EIRQ3		EIRQ5	EIRQ6	EIRQ7
20	16	12	PC3	EIRQ3	-	GPO	ANI11+CMP_IN4	TMRA_PWM4		TMR4_OVL	USART3_TX	MCAN_TX		EVENTP23	EIRQ0	EIRQ1	EIRQ2		EIRQ4	EIRQ5	EIRQ6	EIRQ7
21	17	13	PC2	EIRQ2	-	GPO	ANI10+CMP_IN5	TMRA_PWM3	TMR2_1_CLKA	TMR4_OVH	USART3_RX	MCAN_RX	SPI2_NSS2	EVENTP22	EIRQ0	EIRQ1		EIRQ3	EIRQ4	EIRQ5	EIRQ6	EIRQ7
22	-	-	PD7	EIRQ7	-	GPO	CMP_IN6				USART2_TX			EVENTP37	EIRQ0	EIRQ1	EIRQ2	EIRQ3	EIRQ4	EIRQ5	EIRQ6	
23	-	-	PD6	EIRQ6	-	GPO	CMP_IN7				USART2_RX			EVENTP36	EIRQ0	EIRQ1	EIRQ2	EIRQ3	EIRQ4	EIRQ5		EIRQ7
24	18	14	PD5	EIRQ5	-	GPO	CTCREF	TMRA_CLKB	TMR2_1_CLKB			USART1_CK	SPI2_SCK	EVENTP35	EIRQ0	EIRQ1	EIRQ2	EIRQ3	EIRQ4		EIRQ6	EIRQ7
25	19	-	PC1	EIRQ1	-	GPO	ANI9	TMRA_PWM8	TMR4_OWL	TMR4_OUL	TMR4_OVL	TMRA_PWM2		EVENTP21	EIRQ0		EIRQ2	EIRQ3	EIRQ4	EIRQ5	EIRQ6	EIRQ7
26	-	-	PC0	EIRQ0	-	GPO	ANI8	TMRA_PWM7	TMR4_OWH	TMR4_OUH	TMR4_OVH	TMRA_PWM1		EVENTP20		EIRQ1	EIRQ2	EIRQ3	EIRQ4	EIRQ5	EIRQ6	EIRQ7
27	-	-	PC17	EIRQ1	-	GPO	ANI15			EMB_PORT3					EIRQ0		EIRQ2	EIRQ3	EIRQ4	EIRQ5	EIRQ6	EIRQ7
28	20	-	PC16	EIRQ0	-	GPO	ANI14			EMB_PORT2	USART2_TX		I2C1_SCL			EIRQ1	EIRQ2	EIRQ3	EIRQ4	EIRQ5	EIRQ6	EIRQ7
29	21	-	PC15	EIRQ7	-	GPO	ANI13	TMRA_PWM4		TMR4_OVL	USART2_RX		I2C1_SDA	EVENTP27	EIRQ0	EIRQ1	EIRQ2	EIRQ3	EIRQ4	EIRQ5	EIRQ6	
30	22	-	PC14	EIRQ6	-	GPO	ANI12	TMRA_PWM3		TMR4_OVH				EVENTP26	EIRQ0	EIRQ1	EIRQ2	EIRQ3	EIRQ4	EIRQ5		EIRQ7
31	23	15	PB3	EIRQ3	-	GPO	ANI7	TMRA_CLKA	TMRA_PWM2	TMR4_OUL		USART1_RTS/USART1_DE	SPI1_MISO	EVENTP12	EIRQ0	EIRQ1	EIRQ2		EIRQ4	EIRQ5	EIRQ6	EIRQ7
32	24	16	PB2	EIRQ2	-	GPO	ANI6	TMRA_CLKB	TMRA_PWM1	TMR4_OUH		USART1_CTS	SPI1_SCK	EVENTP13	EIRQ0	EIRQ1		EIRQ3	EIRQ4	EIRQ5	EIRQ6	EIRQ7
33	25	17	PB1	EIRQ1	-	GPO	ANI5	TMRA_TRIG	TMR2_2_PWMB	TMR4_CLK	USART3_TX	MCAN_TX	SPI1_MOSI		EIRQ0		EIRQ2	EIRQ3	EIRQ4	EIRQ5	EIRQ6	EIRQ7
34	26	18	PB0	EIRQ0	-	GPO	ANI4		TMR2_2_CLKA		USART3_RX	MCAN_RX	SPI1_NSS0			EIRQ1	EIRQ2	EIRQ3	EIRQ4	EIRQ5	EIRQ6	EIRQ7
35	27	-	PC9	EIRQ1	-		ADTRG			EMB_PORT1	USART3_RTS/USART3_DE	USART4_TX			EIRQ0		EIRQ2	EIRQ3	EIRQ4	EIRQ5	EIRQ6	EIRQ7
36	28	-	PC8	EIRQ0	-	GPO	ADTRG			EMB_PORT0	USART3_CTS	USART4_RX				EIRQ1	EIRQ2	EIRQ3	EIRQ4	EIRQ5	EIRQ6	EIRQ7
37	29	19	PA7	EIRQ7	-	GPO	ANI3		TMR2_2_PWMA	EMB_PORT2	USART4_RTS/USART4_DE	USART2_TX	RTC_CLKIN		EIRQ0	EIRQ1	EIRQ2	EIRQ3	EIRQ4	EIRQ5	EIRQ6	
38	-	-	PA6	EIRQ6	-	GPO	ANI2			EMB_PORT1	USART4_CTS		SPI2_NSS1		EIRQ0	EIRQ1	EIRQ2	EIRQ3	EIRQ4	EIRQ5		EIRQ7
39	-	-	PE7	EIRQ7	-	GPO		TMRA_PWM8	TMR4_OWL	TMR4_OUL	TMR4_OVL	USART2_RTS/USART2_DE		EVENTP46	EIRQ0	EIRQ1	EIRQ2	EIRQ3	EIRQ4	EIRQ5	EIRQ6	
40	30	20	VSS	-	-																	
41	31	21	VCC	-	-																	
42	32	-	PB13	EIRQ5	-	GPO		TMRA_PWM2		TMR4_OUL		USART2_CTS			EIRQ0	EIRQ1	EIRQ2	EIRQ3	EIRQ4		EIRQ6	EIRQ7
43	-	-	PB12	EIRQ4	-	GPO		TMRA_PWM1		TMR4_OUH		USART3_RTS/USART3_DE			EIRQ0	EIRQ1	EIRQ2	EIRQ3		EIRQ5	EIRQ6	EIRQ7
44	-	-	PD4	EIRQ4	-	GPO				EMB_PORT3		USART3_CTS		EVENTP34	EIRQ0	EIRQ1	EIRQ2	EIRQ3		EIRQ5	EIRQ6	EIRQ7
45	33	22	PD3	EIRQ3+NMI	-	GPO	FCMREF		TMR2_2_PWMB	TMR4_ADSM	USART4_CK	USART2_RX	SPI2_NSS0	EVENTP33	EIRQ0	EIRQ1	EIRQ2		EIRQ4	EIRQ5	EIRQ6	EIRQ7
46	34	-	PD2	EIRQ2	-	GPO					USART3_CK		SPI2_MOSI	EVENTP32	EIRQ0	EIRQ1		EIRQ3	EIRQ4	EIRQ5	EIRQ6	EIRQ7
47	35	23	PA3	EIRQ3	-	GPO			TMR2_2_CLKA		USART1_CK	USART3_TX	I2C1_SCL		EIRQ0	EIRQ1	EIRQ2		EIRQ4	EIRQ5	EIRQ6	EIRQ7
48	36	24	PA2	EIRQ2	-	GPO	MCO		TMR2_2_CLKB		USART2_CK	USART3_RX	I2C1_SDA		EIRQ0	EIRQ1		EIRQ3	EIRQ4	EIRQ5	EIRQ6	EIRQ7
49	37	25	PA1	EIRQ1	-	GPO	ANI1+CMP_IN1	TMRA_CLKA	TMRA_PWM2	TMR4_OUL	USART3_RTS/USART3_DE	USART1_TX	SPI1_NSS2	EVENTP11	EIRQ0		EIRQ2	EIRQ3	EIRQ4	EIRQ5	EIRQ6	EIRQ7
50	38	26	PA0	EIRQ0	-	GPO	ANI0+CMP_IN0	TMRA_TRIG	TMR2_2_PWMA		USART3_CTS	USART1_RX	SPI2_NSS3	EVENTP10		EIRQ1	EIRQ2	EIRQ3	EIRQ4	EIRQ5	EIRQ6	EIRQ7
51	39	-	PC7	EIRQ7	-	GPO		TMRA_CLKA			USART4_TX				EIRQ0	EIRQ1	EIRQ2	EIRQ3	EIRQ4	EIRQ5	EIRQ6	
52	40	-	PC6	EIRQ6	-	GPO		TMRA_CLKB		TMR4_PCT	USART4_RX				EIRQ0	EIRQ1	EIRQ2	EIRQ3	EIRQ4	EIRQ5		EIRQ7
53	-	-	PE6	EIRQ6	-	GPO					USART4_RTS/USART4_DE		SPI1_NSS2	EVENTP47	EIRQ0	EIRQ1	EIRQ2	EIRQ3	EIRQ4	EIRQ5		EIRQ7
54	-	-	PE2	EIRQ2	-	GPO			TMR2_2_CLKA		USART4_CTS		SPI1_MOSI	EVENTP42	EIRQ0	EIRQ1		EIRQ3	EIRQ4	EIRQ5	EIRQ6	EIRQ7
55	41	-	PA13	EIRQ5	-	GPO	FCMREF	TMRA_PWM8	TMR4_OUL	TMR4_OWL	TMR4_OVL				EIRQ0	EIRQ1	EIRQ2	EIRQ3	EIRQ4		EIRQ6	EIRQ7
56	42	-	PA12	EIRQ4	-	GPO		TMRA_PWM7	TMR4_OUH	TMR4_OWH	TMR4_OVH	USART4_CK			EIRQ0	EIRQ1	EIRQ2	EIRQ3		EIRQ5	EIRQ6	EIRQ7
57	43	27	PA11	EIRQ3	-	GPO	VCOUT	TMRA_PWM6		TMR4_OWL	USART2_CK	USART4_TX	SPI2_MISO		EIRQ0	EIRQ1	EIRQ2		EIRQ4	EIRQ5	EIRQ6	EIRQ7
58	44	28	PA10	EIRQ2	-	GPO	ADTRG	TMRA_PWM5	TMR2_1_CLKB	TMR4_OWH		USART4_RX	SPI2_MOSI		EIRQ0	EIRQ1		EIRQ3	EIRQ4	EIRQ5	EIRQ6	EIRQ7
59	-	-	PE1	EIRQ1	-	GPO	LVD2INP			EMB_PORT1		SPI2_NSS0	SPI1_MISO	EVENTP41	EIRQ0		EIRQ2	EIRQ3	EIRQ4	EIRQ5	EIRQ6	EIRQ7
60	-	-	PE0	EIRQ0	-	GPO		TMRA_TRIG	TMR2_1_PWMA	EMB_PORT2	TMR4_CLK	SPI2_MOSI	SPI1_SCK	EVENTP40		EIRQ1	EIRQ2	EIRQ3	EIRQ4	EIRQ5	EIRQ6	EIRQ7
61	45	29	PC5	EIRQ5	-	GPO			TMR2_1_PWMB		RTC_OUT	USART1_RTS/USART1_DE		EVENTP25	EIRQ0	EIRQ1	EIRQ2	EIRQ3	EIRQ4		EIRQ6	EIRQ7
62	46	30	PC4	EIRQ4	SWCLK	GPO	CMP_IN2	TMRA_PWM1	TMRA_CLKB	TMR4_OUH	RTC_OUT	USART1_CTS	SPI2_NSS2	EVENTP24	EIRQ0	EIRQ1	EIRQ2	EIRQ3		EIRQ5	EIRQ6	EIRQ7
63	47	31	PA5/NRST	EIRQ5	-	GPO		TMRA_TRIG			TMR4_CLK				EIRQ0	EIRQ1	EIRQ2	EIRQ3	EIRQ4		EIRQ6	EIRQ7
64	48	32	PA4	EIRQ4	SWDIO	GPO	VCOUT			TMR4_PCT	USART3_CK	USART2_CTS	SPI1_NSS1		EIRQ0	EIRQ1	EIRQ2	EIRQ3		EIRQ5	EIRQ6	EIRQ7

Table 3-2 Port Configuration

Package	Port Group	Bits																		Pin Count Total	
		17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
LQFP64	PortA	-	-	-	-	o	o	o	o	-	-	o	o	o	o	o	o	o	o	12	58
	PortB	-	-	-	-	o	o	-	-	-	-	o	o	o	o	o	o	o	o	10	
	PortC	o	o	o	o	-	-	-	-	o	o	o	o	o	o	o	o	o	o	14	
	PortD	-	o	o	-	-	-	-	-	-	-	o	o	o	o	o	o	o	o	10	
	PortE	-	-	-	-	-	-	o	o	o	o	o	o	o	o	o	o	o	o	12	
LQFP48	PortA	-	-	-	-	o	o	o	o	-	-	o	-	o	o	o	o	o	o	11	43
	PortB	-	-	-	-	o	-	-	-	-	o	o	o	o	o	o	o	o	o	9	
	PortC	-	o	o	o	-	-	-	-	o	o	o	o	o	o	o	o	o	-	12	
	PortD	-	o	o	-	-	-	-	-	-	-	-	-	o	-	o	o	o	o	7	
	PortE	-	-	-	-	-	-	-	-	o	o	-	-	o	o	-	-	-	-	4	
QFN32	PortA	-	-	-	-	-	-	o	o	-	-	o	-	o	o	o	o	o	o	9	28
	PortB	-	-	-	-	-	-	-	-	-	-	o	o	o	o	o	o	o	o	8	
	PortC	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	o	-	-	4	
	PortD	-	o	o	-	-	-	-	-	-	-	-	-	o	-	o	-	-	-	4	
	PortE	-	-	-	-	-	-	-	-	-	o	-	-	o	o	-	-	-	-	3	

Table 3-3 General Functional Specifications

Port		Pull-Up	Pull-Down	Open-Drain Output	Driving Capacity	Input
PortA	PA0-PA7, PA10-PA13	Support	Support	Support	Normal/High	CMOS/Schmitt
PortB	PB0-PB7, PB12-PB13	Support	Support	Support	Normal/High	CMOS/Schmitt
PortC	PC0-PC9, PC14-PC17	Support	Support	Support	Normal/High	CMOS/Schmitt
PortD	PD0-PD7, PD15-PD16	Support	Support	Support	Normal/High	CMOS/Schmitt
PortE	PE0-PE11	Support	Support	Support	Normal/High	CMOS/Schmitt

Note

Input voltage must not be higher than AVCC when used as an analog function.

3.3 Pin Function Description

Table 3-4 Pin Function Description

Categories	Functional Name	I/O	Description
Power	VCC	I	Power supply
	VSS	I	Power ground
	AVCC	I	Analog power
	VREFH	I	Analog reference voltage
System	NRST	I	Reset terminal, active low
LVD2	LVD2INP	I	LVD2 external input comparison voltage
Clock	XTAL_OUT	O	External main clock oscillator interface
	XTAL_IN	I	
	EXCLK	I	External main clock input
	XTAL32_OUT	O	External sub clock (32.768kHz) oscillator interface
	XTAL32_IN	I	
	MCO	O	Internal clock output
GPIO	Pxy (x=A-E y=0-17)	IO	General input output
EIRQ	EIRQx (x=0-7)	I	Maskable external interrupt
	NMI	I	Non-maskable external interrupt
Event Port	EVNTPxy (x=1-4 y=0-7)	IO	Event port input and output functions
SWD	SWCLK	I	Online debugging interface
	SWDIO	IO	
FCM	FCMREF	I	External reference clock input for clock frequency measurement
RTC	RTC_OUT	O	1Hz clock output
	RTC_CLKIN	I	External clock input
Timer2	TMR2_x_CLKA (x=1-2)	I	Counting clock port input
	TMR2_x_CLKB (x=1-2)	I	Counting clock port input
	TMR2_x_PWMA/TMR2_x_TRIGA (x=1-2)	IO	External event trigger input or PWM port output
	TMR2_x_PWMB/TMR2_x_TRIGB (x=1-2)	IO	External event trigger input or PWM port output
Timer4	TMR4_CLK	I	Counting clock port input
	TMR4_OUH	IO	PWM port U-phase output
	TMR4_OUL	IO	PWM port U-phase output
	TMR4_OVH	IO	PWM port V-phase output

Categories	Functional Name	I/O	Description
Timer4	TMR4_OVL	IO	PWM port V-phase output
	TMR4_OWH	IO	PWM port W-phase output
	TMR4_OWL	IO	PWM port W-phase output
	TMR4_ADSM	O	Special event output detection
	TMR4_PCT	O	PWM period output detection
TimerA	TMRA_TRIG	I	External event trigger input
	TMRA_CLKA	IO	Counting clock port input
	TMRA_CLKB	IO	Counting clock port input
	TMRA_PWMx (x=1-8)	IO	PWM port output
EMB	EMB_PORTx (x=0-3)	I	Port input control signal
USART	USARTx_TX (x=1-4)	O	Transmit data
	USARTx_RX (x=1-4)	I	Receiving data
	USARTx_CK (x=1-4)	IO	Communication clock
	USARTx_RTS/USARTx_DE (x=1-4)	O	Request transmiting signal/driver enable
	USARTx_CTS (x=1-4)	I	Clear transmiting signal
SPI	SPIx_MISO (x=1-2)	IO	Master input/slave output data transfer pin
	SPIx_MOSI (x=1-2)	IO	Master output/slave input data transfer pin
	SPIx_SCK (x=1-2)	IO	Transmission clock
	SPIx_NSS0 (x=1-2)	IO	Slave selection input/output pin
	SPIx_NSSy (x=1-2 y=1-3)	O	Slave selection output pin
I2C	I2C_SCL	IO	Clock line
	I2C_SDA	IO	Data line
MCAN	MCAN_TX	O	Transmit data
	MCAN_RX	I	Receiving data
CMP	VCOUT	O	Comparison result output
	CMP_INx (x=0-7)	I	CMP0 positive/negative analog input
ADC	ADTRG	I	ADC AD Convert External Startup Source
	ANIx (x=0-15)	I	ADC external analog input port
CTC	CTCREF	I	Reference clock input

3.4 Pin Instructions

Table 3-5 Pin Instruction

Pin Name	Usage Notes
VCC	Power Supply. Connect to 2.7V-5.5V and place a decoupling capacitor near the VSS pin (refer to "Electrical Specifications").
VSS	Source ground, connected to 0V.
AVCC	Analog Power Supply. Supply power to analog modules; connect to the same voltage as VCC (refer to "Electrical Specifications"). When not using an independent analog power supply, connect the pin to VCC and ensure it is not left floating.
VREFH	Analog Reference Voltage. Connect to AVCC when not in use and do not leave it floating. During power on and power down, it is necessary to ensure that VREFH ≤ AVCC or the driving capability of the VREFH power supply is less than 100mA.
NRST	Reset pin (NRST), active low. Resistance to VCC when not in use (pull-up).
Pxy (x=A to E y=0-17)	General pin. When used as an input function, the input voltage should not exceed VCC. When not in use, leave floating or connect a resistor to VCC (pull-up) or VSS (pull-down).

4 Electrical Specifications

4.1 Parameter Conditions

Unless otherwise specified, all voltages are based on VSS.

4.1.1 Minimum and Maximum Values

All Minimum Values and Maximum Values are measured under the worst conditions.

Data resulted from comprehensive evaluation, and/or guaranteed by design are indicated in the table footnotes, and they will not be tested on the production line.

4.1.2 Typical Values

Unless otherwise specified, typical data are given based on T_A=25℃ and VCC=5.0V. These data are only used for design guidance and have not been tested.

4.1.3 Typical Curve

Unless otherwise specified, all typical curves are untested and are for design reference only.

4.1.4 Load Capacitance

The left of Figure 4-1 : Pin Load Condition (Left) and Input Voltage Measurement (Right) displays the load conditions used to measure the pin parameters.

4.1.5 Pin Input Voltage

The right of Figure 4-1 : Pin Load Condition (Left) and Input Voltage Measurement (Right) displays the measurement method of the input voltage on the device pin.

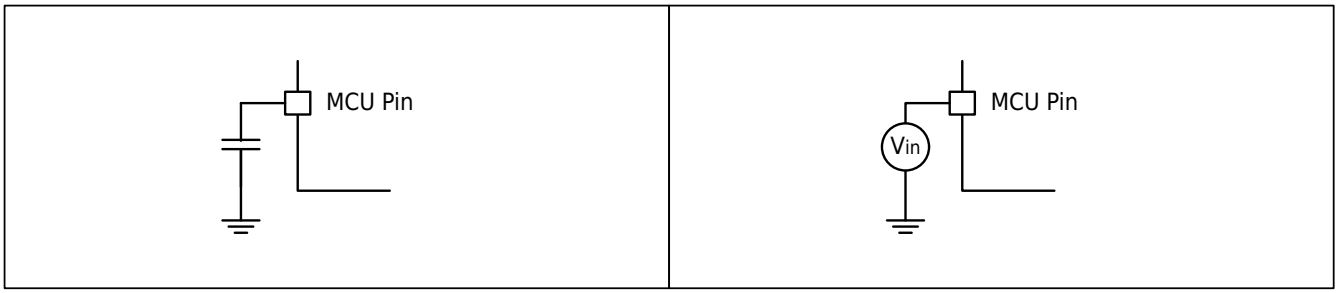


Figure 4-1 Pin Load Condition (Left) and Input Voltage Measurement (Right)

4.1.6 Power Scheme

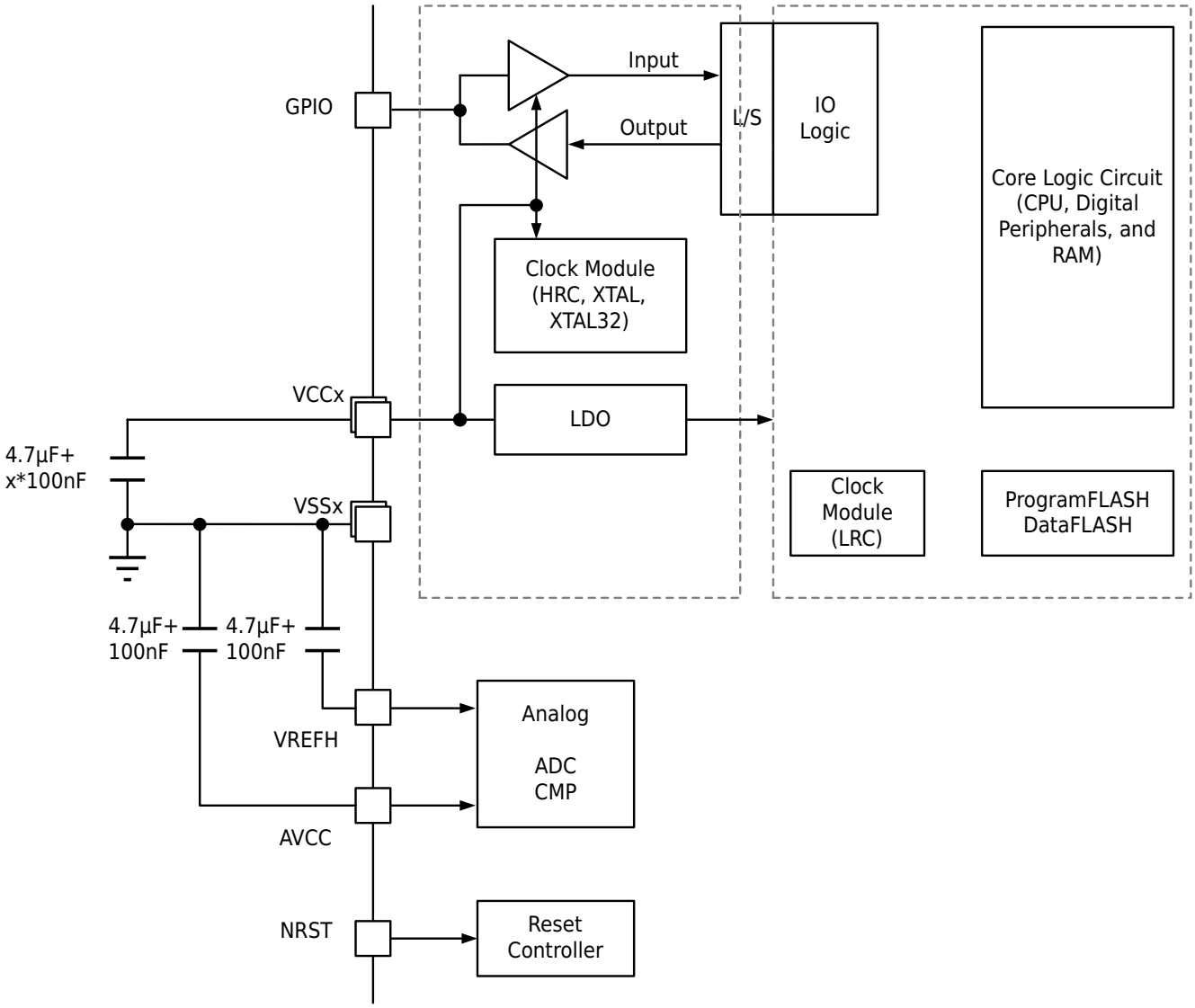


Figure 4-2 Power Scheme

Note

1. 4.7μF ceramic capacitor must be connected to the AVCC/VSS and VREFH/VSS pins.
2. 4.7μF ceramic capacitor must be connected to one of VCCx/VSSx pins.
3. Each power supply pair (e.g., VCCx/VSSx, AVCC/VSS...) must be decoupled using the filtered ceramic capacitors specified above. These capacitors must be placed as close as possible to—or directly beneath—the corresponding pins on the PCB to ensure proper device operation. It is not recommended to omit filtering capacitors for the purpose of reducing PCB size or cost, as this may result in abnormal device behavior.
4. It is recommended to use low-ESR ceramic capacitors (e.g., X7R type) for all filtering applications.

4.1.7 Current Consumption Measurement

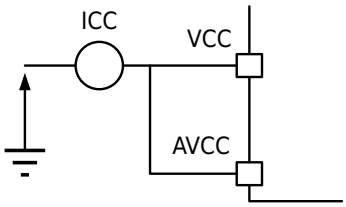


Figure 4-3 Current Consumption Measurement Solution

4.2 Absolute Maximum Ratings

If the load applied to the device exceeds the value given in the list of "Absolute Maximum Ratings", it may cause permanent damage to the device. These values are only rated stresses, and do not mean that the device functions normally under these conditions. Long-term operation at the maximum rating may affect the reliability of the device.

Table 4-1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{CC}-V_{SS}	External main power voltage (include VCC, AVCC, and VREFH)(1)	-0.3	5.8	V
V_{IN}	Input voltage on pin(2)	V_{SS}-0.8	5.8	V
$I_{INJPAD\_DC\_ABS}$	Injectable current of I/O pin	-3	3	mA
$I_{INJSUM\_DC\_ABS}$	Sum of absolute values of injection currents on all pins	-	30	mA
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human model)	Please refer to "Electrical Sensitivity"		-

Note

1. Within the allowable range, the VCC/AVCC/VREFH and VSS pins must always be connected to an external power supply.
2. The maximum values of $I_{INJPAD\_DC\_ABS}$, $I_{INJSUM\_DC\_ABS}$, $\sum I_{VCC}$, and $\sum I_{VSS}$ must always be observed.

Table 4-2 Current Characteristics

Symbol	Description	Max	Unit
$\sum I_{VCC}$	Total current to all VCC power wires (pull current) (1)	100	mA
$\sum I_{VSS}$	Total current from all VSS ground wires (sink current) (1)	-100	mA
I_{IO}	Output sink current of any I/O and control pins	20	mA
	Output pull current of any I/O and control pins	-20	mA
$\sum I_{IO}$	Total output sink current of all I/O and control pins(2)	100	mA
	Total output pull current of all I/O and control pins(2)	-100	mA

Note

1. Within the allowable range, the VCC and VSS pins must always be connected to an external power supply.
2. This current consumption must be properly distributed to all I/O and control pins. The total output current must not be sinked/pulled between two continuous power supply pins.

Table 4-3 Temperature Characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage Temperature Range	-55-+150	℃
T_{Jmax}	Maximum Junction Temperature	135	℃

4.3 Operating Conditions

4.3.1 General Operating Conditions

Table 4-4 General Operating Conditions(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{HCLK}	Internal AHB clock frequency	Running mode	-	-	64	MHz
V_{CC}	Standard operating voltage	-	2.7	-	5.5	V
V_{AVCC}	Analog operating voltage	-	2.7	-	5.5	V
V_{REFH}	Analog reference voltage		V_{AVCC}			V
V_{IN}	Pin input voltage	-	-0.3	-	V_{CC}+0.3	V
T_J	Junction temperature range	-	-40	-	135	℃
T_A	Working Temperature Range	-	-40	-	125	℃

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.2 Working Conditions at Power On and Power Down

Table 4-5 Working Conditions at Power On and Power Down(1)

Symbol	Parameters	Conditions	Min	Max	Unit
t_{VCC}	VCC rise time rate	-	20	20000	μs/V
	VCC fall time rate	LVD1ICGCR.LVDDIS=0b1	20	20000	μs/V
		LVD1ICGCR.LVDDIS=0b0	20	-	μs/V

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.3 Reset and Power Control Module Characteristics

Table 4-6 Reset and Power Control Module Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{LVD1}	LVD1 Monitoring Voltage(3)	LVD1LVLSEL[1:0]=0b00(rise)	-	4.45	4.70	V

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{LVD1}	LVD1 Monitoring Voltage[3]	LVD1LVLSEL[1:0]=0b00(fall)	4.10	4.30	-	V
		LVD1LVLSEL[1:0]=0b01(rise)[1]	-	3.96	-	V
		LVD1LVLSEL[1:0]=0b01(fall)[1]	-	3.85	-	V
		LVD1LVLSEL[1:0]=0b10(rise)[1]	-	3.27	-	V
		LVD1LVLSEL[1:0]=0b10(fall)[1]	-	3.17	-	V
		LVD1LVLSEL[1:0]=0b11(rise)	-	2.96	3.12	V
		LVD1LVLSEL[1:0]=0b11(fall)	2.74	2.87	-	V
V_{LVD2}	LVD2 Monitoring Voltage[3]	LVD2LVLSEL[3:0]=0b0000(rise)	-	4.08	4.32	V
		LVD2LVLSEL[3:0]=0b0000(fall)	3.78	3.96	-	V
		LVD2LVLSEL[3:0]=0b0001(rise)[1]	-	3.77	-	V
		LVD2LVLSEL[3:0]=0b0001(fall)[1]	-	3.67	-	V
		LVD2LVLSEL[3:0]=0b0010(rise)[1]	-	3.17	-	V
		LVD2LVLSEL[3:0]=0b0010(fall)[1]	-	3.07	-	V
		LVD2LVLSEL[3:0]=0b0011(rise)[1]	-	3.05	-	V
		LVD2LVLSEL[3:0]=0b0011(fall)[1]	-	2.96	-	V
		LVD2LVLSEL[3:0]=0b0100(rise)[1]	-	2.96	-	V
		LVD2LVLSEL[3:0]=0b0100(fall)[1]	-	2.87	-	V
		LVD2LVLSEL[3:0]=0b0101(rise)	-	2.83	3.00	V
		LVD2LVLSEL[3:0]=0b0101(fall)	2.62	2.75	-	V
		LVD2LVLSEL[3:0]=0b1110[5]	-	0.90	-	V
$V_{LVD1}hyst$[1]	Hysteresis of LVD1[4]	LVD1LVLSEL[1:0]=0b00	-	150	-	mV
		LVD1LVLSEL[1:0]=0b01	-	110	-	mV
		LVD1LVLSEL[1:0]=0b10	-	100	-	mV
		LVD1LVLSEL[1:0]=0b11	-	90	-	mV

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{LVD2}hyst$[1]	Hysteresis of LVD2[4]	LVD2LVLSEL[3:0]=0b0000	-	120	-	mV
		LVD2LVLSEL[3:0]=0b0001/0010	-	100	-	mV
		LVD2LVLSEL[3:0]=0b0011/0100	-	90	-	mV
		LVD2LVLSEL[3:0]=0b0101	-	80	-	mV
V_{POR}	Power On/Power Down Reset Threshold	Rising Edge VPOR	-	2.445	2.700	V
		Falling Edge VPDR	2.135	2.400	-	V
I_{RUSH}[1]	Surge Current When Voltage Regulator Powered On (POR)	-	-	-	300	mA
T_{NRST}[2]	NRST Reset Minimum Width	-	40	-	-	µs
T_{INRST}[2]	NRST Reset Release Time	-	300	1000	1400	µs
T_{RIPT}[2]	Internal Reset Time	-	300	1000	1400	µs
T_{RSTPOR}[2]	Power On Reset Release Time	-	-	4500	6600	µs

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. The monitoring voltage of LVD1 is the monitoring voltage when VCC voltage drops; when LVD2LVLSEL[3:0] is set to 0b1110, the LVD2 monitoring voltage is the monitoring voltage when the LVD2INP voltage drops, and when LVD2LVLSEL[3:0] is set to a value other than 0b1110, the LVD2 monitoring voltage is the monitoring voltage when the VCC voltage drops.
4. The hysteresis of LVD1/2 is the difference between the monitoring voltages when VCC rises and falls.
   LVD1 monitoring voltage when VCC rises =V_{LVD1}+V_{LVD1}hyst;
   LVD2 monitoring voltage when VCC rises =V_{LVD2}+V_{LVD2}hyst.
5. When LVD2LVLSEL[3:0]=0b1110, the comparison voltage is the external input comparison voltage of LVD2INP pin.

4.3.4 Supply Current Characteristics

Current consumption is affected by many parameters and factors, including operating voltage, ambient temperature, I/O pin load, device software configuration, operating frequency, I/O pin switching rate, program location in memory and running code.

Figure 4-3 : Current Consumption Measurement Solution describes the measurement method of current consumption. The measured values of current consumption in various modes described in this section are obtained by a set of test codes running in FLASH under laboratory conditions.

The specific conditions are as follows:

1. All I/O pins are set to input mode, with static values on V_{CC} or V_{SS} (no load).

2. The clock frequencies selected are f_{HCLK}=64MHz, f_{HCLK}=48MHz, and an ultra-low-speed mode of 32kHz.
3. The power consumption modes include the normal operating mode ICC_RUN, Sleep mode ICC_SLEEP,Stop mode ICC_STP, and Dhrystone operating mode ICC_DHRYSTONE.
4. For the ON/OFF status of peripheral clocks, please refer to the specific current test items.

Table 4-7 Normal Operating Mode with f_{HCLK}=64MHz Current Consumption

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=64MHz T_A=-40℃ V_{CC}=5.0V	-	10.1	-	mA
	While (1), all peripherals clock ON		-	17.7	-	mA
ICC_DHRY-STONE(1)	PREFETCH OFF		-	12.4	-	mA
	PREFETCH ON		-	12.6	-	mA
ICC_PERIPHER-AL(1)	PERIPHERAL ENABLE		-	18.2	-	mA
ICC_SLEEP	All peripherals clock OFF		-	5.0	-	mA
	All peripherals clock ON		-	12.7	-	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=64MHz T_A=25℃ V_{CC}=5.0V	-	10.2	-	mA
	While (1), all peripherals clock ON		-	17.8	-	mA
ICC_DHRY-STONE(1)	PREFETCH OFF		-	12.3	-	mA
	PREFETCH ON		-	12.4	-	mA
ICC_PERIPHER-AL(1)	PERIPHERAL ENABLE		-	18.3	-	mA
ICC_SLEEP	All peripherals clock OFF		-	5.2	-	mA
	All peripherals clock ON		-	12.8	-	mA
ICC_RUN(1)	While (1), all peripherals clock OFF	f_{HCLK}=64MHz T_A=105℃ V_{CC}=2.7-5.5V	-	-	11.3	mA
	While (1), all peripherals clock ON		-	-	21.6	mA
ICC_DHRY-STONE(1)	PREFETCH OFF		-	-	14.7	mA
	PREFETCH ON		-	-	14.9	mA
ICC_PERIPHER-AL(1)	PERIPHERAL ENABLE		-	-	22.7	mA
ICC_SLEEP(1)	All peripherals clock OFF		-	-	7.1	mA
	All peripherals clock ON		-	-	16.2	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=64MHz T_A=125℃ V_{CC}=2.7-5.5V	-	-	13.9	mA
	While (1), all peripherals clock ON		-	-	23.4	mA
ICC_DHRY-STONE(1)	PREFETCH OFF		-	-	17.2	mA
	PREFETCH ON		-	-	17.4	mA
ICC_PERIPHER-AL(1)	PERIPHERAL ENABLE		-	-	24.1	mA
ICC_SLEEP	All peripherals clock OFF		-	-	8.0	mA
	All peripherals clock ON		-	-	17.5	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-8 Normal Operating Mode with f_{HCLK}=48MHz Current Consumption

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=48MHz T_A=-40℃ V_{CC}=5.0V	-	7.8	-	mA
	While (1), all peripherals clock ON		-	13.6	-	mA
ICC_DHRY-STONE(1)	PREFETCH OFF		-	9.4	-	mA
	PREFETCH ON		-	9.5	-	mA
ICC_PERIPHER-AL(1)	PERIPHERAL ENABLE		-	14.2	-	mA
ICC_SLEEP	All peripherals clock OFF		-	4.0	-	mA
	All peripherals clock ON		-	9.8	-	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=48MHz T_A=25℃ V_{CC}=5.0V	-	7.8	-	mA
	While (1), all peripherals clock ON		-	13.6	-	mA
ICC_DHRY-STONE(1)	PREFETCH OFF		-	9.4	-	mA
	PREFETCH ON		-	9.5	-	mA
ICC_PERIPHER-AL(1)	PERIPHERAL ENABLE		-	14.2	-	mA
ICC_SLEEP	All peripherals clock OFF		-	4.1	-	mA
	All peripherals clock ON		-	9.9	-	mA
ICC_RUN(1)	While (1), all peripherals clock OFF	f_{HCLK}=48MHz T_A=105℃ V_{CC}=2.7-5.5V	-	-	9.8	mA
	While (1), all peripherals clock ON		-	-	16.9	mA
ICC_DHRY-STONE(1)	PREFETCH OFF		-	-	11.5	mA
	PREFETCH ON		-	-	11.7	mA
ICC_PERIPHER-AL(1)	PERIPHERAL ENABLE		-	-	17.9	mA
ICC_SLEEP(1)	All peripherals clock OFF		-	-	5.8	mA
	All peripherals clock ON		-	-	12.8	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=48MHz T_A=125℃ V_{CC}=2.7-5.5V	-	-	11.1	mA
	While (1), all peripherals clock ON		-	-	18.4	mA
ICC_DHRY-STONE(1)	PREFETCH OFF		-	-	13.5	mA
	PREFETCH ON		-	-	13.7	mA
ICC_PERIPHER-AL(1)	PERIPHERAL ENABLE		-	-	19.3	mA
ICC_SLEEP	All peripherals clock OFF		-	-	6.7	mA
	All peripherals clock ON		-	-	14.0	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-9 Normal Operating Mode with f_{HCLK}=32kHz Current Consumption

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=32kHz T_A=-40℃ V_{CC}=5.0V	-	0.02	-	mA
	While (1), all peripherals clock ON		-	0.60	-	mA
ICC_DHRY-STONE(1)	PREFETCH OFF		-	0.02	-	mA
	PREFETCH ON		-	0.02	-	mA
ICC_SLEEP	All peripherals clock OFF		-	0.02	-	mA
	All peripherals clock ON		-	0.60	-	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=32kHz T_A=25℃ V_{CC}=5.0V	-	0.03	-	mA
	While (1), all peripherals clock ON		-	0.610	-	mA
ICC_DHRY-STONE(1)	PREFETCH OFF		-	0.03	-	mA
	PREFETCH ON		-	0.03	-	mA
ICC_SLEEP	All peripherals clock OFF		-	0.03	-	mA
	All peripherals clock ON		-	0.60	-	mA
ICC_RUN(1)	While (1), all peripherals clock OFF	f_{HCLK}=32kHz T_A=105℃ V_{CC}=2.7-5.5V	-	-	0.70	mA
	While (1), all peripherals clock ON		-	-	1.50	mA
ICC_DHRY-STONE(1)	PREFETCH OFF		-	-	0.70	mA
	PREFETCH ON		-	-	0.70	mA
ICC_SLEEP(1)	All peripherals clock OFF		-	-	0.70	mA
	All peripherals clock ON		-	-	1.50	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=32kHz T_A=125℃ V_{CC}=2.7-5.5V	-	-	1.20	mA
	While (1), all peripherals clock ON		-	-	2.00	mA
ICC_DHRY-STONE(1)	PREFETCH OFF		-	-	1.15	mA
	PREFETCH ON		-	-	1.15	mA
ICC_SLEEP	All peripherals clock OFF		-	-	1.20	mA
	All peripherals clock ON		-	-	2.00	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-10 STOP Mode Current Consumption

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_STP	-	T_A=-40℃	-	12.3	-	μA
	-	T_A=25℃	-	19.5	33.6	μA
	-	T_A=105℃(1)	-	-	700	μA
	-	T_A=125℃	-	-	1125	μA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-11 Analog Module Current Consumption(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_MODULE	XTAL oscillation mode high drive 40MHz	T_A=25℃ AVCC=5.0V	-	4.80	-	mA
	Oscillation mode medium drive 32MHz		-	4.50	-	mA
	Oscillation mode low drive 8MHz		-	1.10	-	mA
	Oscillation mode ultra-low drive 4MHz		-	0.50	-	mA
	HRC (48MHz)		-	0.60	-	mA
	HRC (64MHz)		-	0.75	-	mA
	ADC		-	1.60	-	mA
	CMP		-	0.20	-	mA
	XTAL 32.768kHz		-	1.80	-	μA

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.5 Low Power Mode Wake-up Timing

Wake-up time is measured from the trigger of wake-up event to the first command executed by CPU:

- For Stop or Sleep mode: the wake-up event is WFE.
- The WKUP pin is used to wake up from Stop and Sleep modes. All time series are measured at ambient temperature VCC=5.0V.

Table 4-12 Low Power Mode Wake-up Time

Symbol	Parameters	Conditions	Typ	Max	Unit
T_{STOP1}	Wake up from Stop mode	System clock is HRC, and the program is executed on RAM	36	80	μs
T_{STOP2}	Wake up from Stop mode	System clock is HRC, and the program is executed on Flash	56	100	μs

Note

1. The measurement of wake-up time starts from the triggering of the wake-up event and ends when the application code reads its first instruction.

4.3.6 External Clock Source Characteristics

4.3.6.1 High-Speed External Clock Generated by External Source

In bypass mode, XTAL oscillator is disabled and the input pin is a standard I/O. The external clock signal must consider the static characteristics of the I/O.

Table 4-13 High-Speed External Clock Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{XTAL_EXT}(1)	User external clock source frequency	-	1	-	40	MHz

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{XTAL\_IN\_IH}$	XTAL_IN input pin high level voltage	-	$0.7*V_{CC}$	-	V_{CC}	V
$V_{XTAL\_IN\_IL}$	XTAL_IN input pin low level voltage	-	V_{SS}	-	$0.35*V_{CC}$	V
T_{rf}(2)(3)	External input clock rising time ($0.35*V_{CC}$ to $0.7*V_{CC}$) and falling time ($0.7*V_{CC}$ to $0.35*V_{CC}$)	f_{XTAL_EXT}: 1MHz to 20MHz	-	-	1.75	ns
		f_{XTAL_EXT}: 20.1MHz to 40MHz	-	-	1.46	ns
T_{width}(2)	Minimum width of the external input clock (high-level width, low-level width)	f_{XTAL_EXT}=8MHz	50	-	-	ns
		f_{XTAL_EXT}=16MHz	25	-	-	ns
		f_{XTAL_EXT}=20MHz	20	-	-	ns
		f_{XTAL_EXT}=32MHz	12.5	-	-	ns
		f_{XTAL_EXT}=40MHz	10	-	-	ns

Note

1. When the external input clock is used as the ADC reference clock, the maximum input frequency f_{XTAL_EXT} is 20MHz.
2. Guaranteed by design, not tested in production.
3. Input clock rising time ($0.2*V_{CC}$ to $0.8*V_{CC}$) and falling time ($0.8*V_{CC}$ to $0.2*V_{CC}$). For f_{XTAL_EXT}: 1MHz to 20MHz, the maximum T_{rf} is 3ns; for f_{XTAL_EXT}: 20.1MHz to 40MHz, the maximum T_{rf} is 2.5ns.

4.3.6.2 High-Speed External Clock Generated by Crystal Oscillator/Ceramic Resonator

The high-speed external (XTAL) clock can be generated by a crystal oscillator/ceramic resonant oscillator with a frequency of 4-40MHz. In application, the resonator and load capacitor must be as close as possible to the pin of oscillator, so as to minimize the output distortion and the stabilization time. For detailed information about resonator characteristics (frequency, package, accuracy, etc.), please consult the crystal resonator manufacturer.

Table 4-14 XTAL 4-40MHz Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{XTAL}(2)	Oscillator frequency	-	4	-	40	MHz
R_F(4)	Feedback resistance	-	-	500	-	kΩ

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
G_m (3)	G_m of crystal oscillator	35MHz-40MHz	15.9	-	-	mA/V
		30MHz-34.9MHz	9.5	-	-	mA/V
		25MHz-29.9MHz	8.6	-	-	mA/V
		20MHz-24.9MHz	8	-	-	mA/V
		16MHz-19.9MHz	5.3	-	-	mA/V
		12MHz-15.9MHz	4.3	-	-	mA/V
		4.1MHz-11.9MHz	3.6	-	-	mA/V
		4MHz	1.6	-	-	mA/V
$t_{SU(XTAL)}$ (1)(2)	Startup time	V_{CC} stable, crystal oscillator =8-40MHz	-	2.0	-	ms
		V_{CC} stable, crystal oscillator =4MHz	-	4.0	-	ms

Note

1. $t_{SU(XTAL)}$ is the oscillation starting time, that is, the time from the software enabling XTAL to the stable 8MHz oscillation frequency. This value is measured based on a standard crystal resonator, and may vary significantly depending on the crystal oscillator manufacturer.
2. Resulted from comprehensive evaluation, not tested in production.
3. Guaranteed by design, not tested in production.
4. When using an external feedback resistance, it is recommended that the resistance range of the external feedback resistor be between 200kΩ and 800kΩ. When the external feedback resistor used is greater than 800 kΩ, the internal feedback resistor needs to be enabled simultaneously.

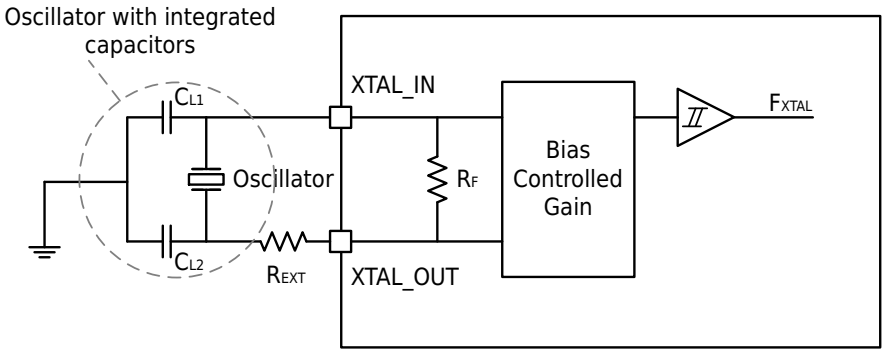


Figure 4-4 Typical application of 8MHz crystal oscillator

Note

- The value of R_{EXT} depends on the crystal oscillation characteristics.
- For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors designed for high-frequency applications, which can meet the requirements of crystal oscillator or resonator (see the figure above). C_{L1} and C_{L2} usually have the same size. $C_{L1}=C_{L2}=2*(C_L-C_S)$. C_S represents the total parasitic capacitance between the PCB and MCU pins (XTAL_IN, XTAL_OUT). C_L denotes the load capacitance of the crystal oscillator or ceramic resonator, please consult the crystal oscillator manufacturer for details.

4.3.6.3 Low-Speed External Clock Generated by Crystal Oscillator/Ceramic Resonator

The low-speed external clock can be generated by an oscillator composed of a crystal oscillator/ceramic resonator with a frequency of 32.768kHz. In application, the resonator and load capacitor must be as close as possible to the pin of oscillator, so as to minimize the output distortion and the stabilization time. For detailed information about resonator characteristics (frequency, package, accuracy, etc.), please consult the crystal resonator manufacturer.

Table 4-15 XTAL32 Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
F_{XTAL32}(1)	Frequency	-	-	32.768	-	kHz
R_F	Feedback resistance	-	-	19	-	MΩ
I_{CC_XTAL32}(1)	Power consumption	XTAL32DRV=0b0	-	1.6	-	μA
A_{XTAL32}(2)(3)	XTAL32 accuracy	-	-500	-	500	ppm
G_m(2)	Oscillator G_m	XTAL32DRV=0b0	5.6	-	-	μA/V
$T_{SUXTAL32}$(1)	Startup Time	Under V_{CC} steady state	-	2	-	s

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. This parameter depends on the resonator used in the application system.
4. $T_{SUXTAL32}$ is the oscillation starting time, that is, the time from the software enabling XTAL32 to the stable 32.768kHz oscillation frequency. This value is measured based on a standard crystal resonator, and may vary significantly depending on the crystal oscillator manufacturer.

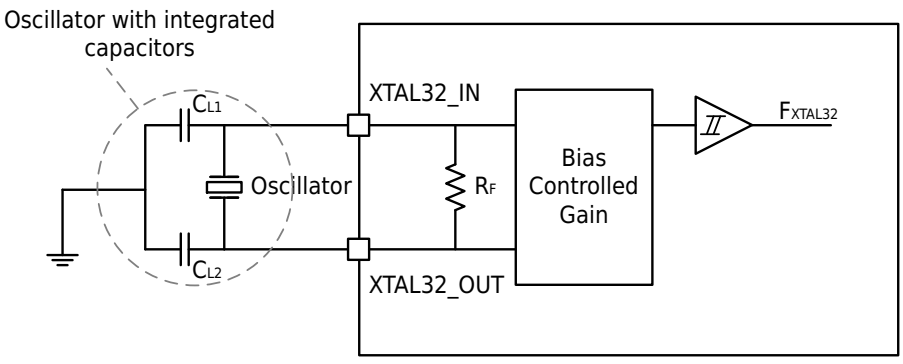


Figure 4-5 Typical application of 32.768kHz crystal oscillator

Note

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors (see the figure above). C_{L1} and C_{L2} usually have the same size, $C_{L1}=C_{L2}=2*(C_L-C_S)$. C_S represents the total parasitic capacitance between PCB and MCU pins (XTAL32_IN, XTAL32_OUT). If C_{L1} or C_{L2} is greater than 18pF, it is recommended to set XTAL32DRV=0b1 (high drive, typical power consumption increases by 0.4μA). C_L denotes the load capacitance of crystal resonator or ceramic resonator, please consult the crystal resonator manufacturer for details.

4.3.7 Internal Clock Source Characteristics

4.3.7.1 HRC

Table 4-16 HRC Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{HRC}	Frequency	Mode 1	-	48	-	MHz
		Mode 2	-	64	-	
	Frequency accuracy	T_A=25℃	-1	-	1	%
		T_A=-40-125℃	-2	-	2	%
$t_{st(HRC)}$	HRC oscillation stabilization time	-	-	-	30	μs

4.3.7.2 LRC

Table 4-17 LRC Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{LRC}	Frequency	-	27.853	32.768	37.683	kHz
$t_{st(LRC)}$	LRC oscillator stabilization time	-	-	-	100	μs
$I_{CC(LRC)}$(1)	LRC oscillator power consumption	-	-	300	-	nA

Note

1. Guaranteed by design, not tested in production.

4.3.8 Memory (Flash) Characteristics

When the device is delivered to the customer, the flash memory has been erased.

Table 4-18 Flash Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$I_{CC(Program-FLASH)}$	Supply current	Read mode, V_{CC}=2.7-5.5V	-	-	7	mA
		Programming mode, V_{CC}=2.7-5.5V	-	-	8	mA
		Block erase mode, V_{CC}=2.7-5.5V	-	-	2	mA
		Full erase mode, V_{CC}=2.7-5.5V	-	-	2	mA

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$I_{CC(DataFLASH/EDataFLASH)}$	Supply current	Read mode, V_{CC}=2.7-5.5V	-	-	5.5	mA
		Programming mode, V_{CC}=2.7-5.5V	-	-	4.5	mA
		Block erase mode, V_{CC}=2.7-5.5V	-	-	2	mA
		Full erase mode, V_{CC}=2.7-5.5V	-	-	2	mA

Table 4-19 Flash Programming Erase Time

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
T_{prog}	Word programming time	Single programming mode	24+2*t_{HCLK}	25+4*t_{HCLK}	26+6*t_{HCLK}	μs
	Word programming time	Continuous Programming Mode	6+2*t_{HCLK}	7+4*t_{HCLK}	8+6*t_{HCLK}	μs
	Half-Word programming time	Single programming mode	31+2*t_{HCLK}	32+4*t_{HCLK}	33+6*t_{HCLK}	μs
	Half-Word programming time	Continuous Programming Mode	13+2*t_{HCLK}	14+4*t_{HCLK}	15+6*t_{HCLK}	μs
	Byte programming time	Single programming mode	45+2*t_{HCLK}	46+4*t_{HCLK}	47+6*t_{HCLK}	μs
	Byte programming time	Continuous Programming Mode	27+2*t_{HCLK}	28+4*t_{HCLK}	29+6*t_{HCLK}	μs
T_{erase}	Block erase time	-	4.3+2*t_{HCLK}	4.5+4*t_{HCLK}	4.7+6*t_{HCLK}	ms
T_{mas}	Full erase time	-	29+2*t_{HCLK}	30+4*t_{HCLK}	31+6*t_{HCLK}	ms

Note

1. t_{HCLK} is 1 period of CPU clock.

Table 4-20 Flash Erase Write Times and Data Storage Period(1)

Symbol	Parameters	Conditions	Min	Unit
N_{end1}	Program, Block Erase times (ProgramFLASH)	T_A=25℃	25	kcycles
T_{ret1}	Data storage period (ProgramFLASH)	T_A=85℃, after 25 kcycles	10	Year
N_{end2}	Program, Block Erase times (DataFLASH/EDataFLASH)	T_A=25℃	100	kcycles
T_{ret2}	Data storage period (DataFLASH/EDataFLASH)	T_A=85℃, after 100 kcycles	10	Year

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.9 Electrical Sensitivity

Different tests (ESD, LU) are carried out on the chip by using specific measurement methods to determine its electrical sensitivity.

4.3.9.1 ESD Characteristics

Table 4-21 ESD Characteristics

Symbol	Parameters	Conditions		Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human model)	T_A=25℃, conforming to AEC-Q100-002		4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charging device model)	T_A=25℃, conforming to AEC-Q100-011	All pins except the corner pins	500	V
			Corner pins only	750	V

4.3.9.2 Static Latch-up Characteristics

Table 4-22 Static Latch-up Characteristics

Symbol	Parameters	Conditions	Max	Unit
I_{LU}	Static Latch-up	T_A=125℃, conforming to AEC-Q100-004	100	mA

4.3.10 I/O Port Characteristics

General-Purpose Input/Output Characteristics

Table 4-23 I/O Static Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{ILSCH}	Schmitt input low level	2.7≤V_{CC}<4	V_{SS}-0.3	-	0.3*V_{CC}	V
		4≤V_{CC}≤5.5	V_{SS}-0.3	-	0.35*V_{CC}	V
V_{IHSCH}	Schmitt input high level	2.7≤V_{CC}<4	0.7*V_{CC}	-	V_{CC}+0.3	V
		4≤V_{CC}≤5.5	0.65*V_{CC}	-	V_{CC}+0.3	V
V_{HYSSCH}(2)(4)	Schmitt input hysteresis	2.7≤V_{CC}≤5.5	0.06*V_{CC}	-	-	V
V_{ILTTL}	CMOS-compatible TTL input low level	2.7≤V_{CC}<4	V_{SS}-0.3	-	0.5	V
		4≤V_{CC}≤5.5	V_{SS}-0.3	-	0.8	V
V_{IHTTL}	CMOS-compatible TTL input high level	2.7≤V_{CC}≤4	2.0	-	V_{CC}+0.3	V
		4<V_{CC}≤5.5	2.2	-	V_{CC}+0.3	V
I_{LKG}	I/O input leakage current (Ports other than PB6 and PB7)	V_{SS}≤V_{IN}≤V_{CC}	-	-	±1000	nA
I_{LKG}	I/O input leakage current (PB6/PB7)	V_{SS}≤V_{IN}≤V_{CC}	-	-	±1500	nA
$I_{INJPAD\_DC\_OP}$(2)(3)(5)	Absolute value of the injected current on the I/O pin	2.7≤V_{CC}≤5.5	-	-	3	mA
$I_{INJSUM\_DC\_OP}$(2)(3)(5)	Sum of the absolute values of injected current on all pins	2.7≤V_{CC}≤5.5	-	-	30	mA
R_{PU}	Weak pull up equivalent resistance	V_{IN}=V_{SS}	20	45	100	kΩ

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
R_{PD}	Weak pull down equivalent resistance	$V_{IN}=V_{CC}$	20	45	100	kΩ
C_{IO}(1)	I/O pin capacitance	-	-	-	5	pF

Note

1. Guaranteed by design, not tested in production.
2. Resulted from comprehensive evaluation, not tested in production.
3. At the same time, the maximum values of V_{IN}, ΣI_{VCC}, and ΣI_{VSS} must always be observed.
4. The influence of adjacent port toggling is not considered.
5. When the current injected into a pin exceeds the chip's consumption current, the power supply itself must be able to handle this current. When the chip is not powered on, current injection into a pin may cause the chip's supply voltage to rise above 0V.

Output Drive Voltage

Table 4-24 Output Voltage Characteristics

Driver	Symbol	Parameters	Conditions		Min	Typ	Max	Unit
Normal drive	V_{OL}(1)	Low level output	$2.7\le V_{CC}<4$	I_{OL}=3.5mA	-	-	0.8	V
			$4\le V_{CC}\le 5.5$	I_{OL}=5mA	-	-	0.8	V
	V_{OH}(2)	High level output	$2.7\le V_{CC}<4$	I_{OH}=3.5mA	V_{CC}-0.8	-	-	V
			$4\le V_{CC}\le 5.5$	I_{OH}=5mA	V_{CC}-0.8	-	-	V
High drive	V_{OL}(1)	Low level output	$2.7\le V_{CC}<4$	I_{OL}=6mA	-	-	0.8	V
			$4\le V_{CC}\le 5.5$	I_{OL}=12mA	-	-	0.8	V
	V_{OH}(2)	High level output	$2.7\le V_{CC}<4$	I_{OH}=5mA	V_{CC}-0.8	-	-	V
			$4\le V_{CC}\le 5.5$	I_{OH}=10mA	V_{CC}-0.8	-	-	V

Note

1. The device's I_{IO} sinking current must always take into account the absolute maximum ratings specified in Table 4-2 : Current Characteristics. The sum of I_{IO} (I/O port and control pin) must always comply with Table 4-25 : Output Current Characteristics.
2. The device's I_{IO} pull current must always conform to the absolute maximum ratings specified in Table 4-2 : Current Characteristics. The sum of I_{IO} (I/O port and control pin) must always comply with Table 4-25 : Output Current Characteristics.

Output Current

Table 4-25 Output Current Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ΣI_{IO}(1)(2)(3)	Absolute value of the sum of output pull current on all I/O and control pins	2.7≤V_{CC}≤5.5	-	-	100	mA
	Absolute value of the sum of output sinking current on all I/O and control pins	2.7≤V_{CC}≤5.5	-	-	100	mA

Note

1. The total output source current and total output sink current must be correctly distributed within each power domain, and the sum of the total source current and total sink current must be ≤100mA.
2. Must always conform to the absolute maximum ratings specified in Table 4-2 : Current Characteristics.
3. Resulted from comprehensive evaluation, not tested in production.

Input/Output AC Characteristics

Table 4-26 I/O AC Characteristics

Driver	Symbol	Parameters	Conditions(1)	Min	Typ	Max	Unit
Normal drive	$f_{max(IO)out}$	Maximum Frequency(2)(3)	C_L=25pF, V_{CC}≥2.7V	-	-	12	MHz
			C_L=25pF, V_{CC}≥4.0V	-	-	20	MHz
			C_L=50pF, V_{CC}≥2.7V	-	-	10	MHz
			C_L=50pF, V_{CC}≥4.0V	-	-	16	MHz
	$t_{f(IO)out}$ $t_{r(IO)out}$	Rise/Fall Time(4)	C_L=25pF, V_{CC}≥2.7V	-	-	27	ns
			C_L=25pF, V_{CC}≥4.0V	-	-	16.6	ns
			C_L=50pF, V_{CC}≥2.7V	-	-	33	ns
			C_L=50pF, V_{CC}≥4.0V	-	-	20.8	ns
High drive	$f_{max(IO)out}$	Maximum Frequency(2)(3)	C_L=25pF, V_{CC}≥2.7V	-	-	20	MHz
			C_L=25pF, V_{CC}≥4.0V	-	-	32	MHz
			C_L=50pF, V_{CC}≥2.7V	-	-	12	MHz
			C_L=50pF, V_{CC}≥4.0V	-	-	20	MHz
	$t_{f(IO)out}$ $t_{r(IO)out}$	Rise/Fall Time(4)	C_L=25pF, V_{CC}≥2.7V	-	-	16.6	ns
			C_L=25pF, V_{CC}≥4.0V	-	-	10	ns
			C_L=50pF, V_{CC}≥2.7V	-	-	27	ns
			C_L=50pF, V_{CC}≥4.0V	-	-	16.6	ns

Note

1. Load capacitance C_L should take into account the parasitic capacitance of PCB.
2. Guaranteed by design, not tested in production. This value is for reference only, actual results may vary in user environments.
3. The maximum frequency is defined in the figure below.
4. Resulted from comprehensive evaluation, not tested in production. This value is for reference only, actual results may vary in user environments.

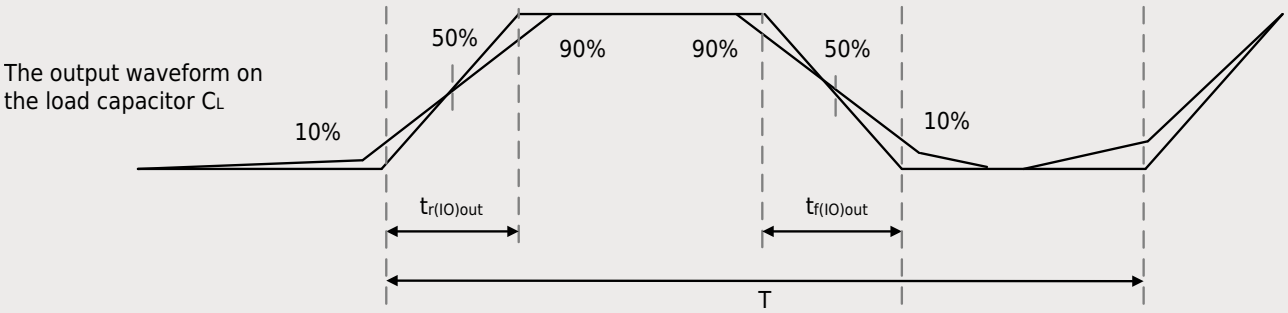


Figure 4-6 I/O AC Characteristics Definition

4.3.11 I2C Interface Characteristics

Table 4-27 I2C Characteristics(1)

Symbol	Parameters	Standard Mode (SM)		Fast Mode (FM)		Unit
		Min	Max	Min	Max	
f_{SCL}	SCL frequency	0	100	0	400	kHz
$t_{HD;STA}$	Start condition/restart condition hold time	4.0	-	0.6	-	μs
t_{LOW}	SCL low level	4.7	-	1.3	-	μs
t_{HIGH}	SCL high level	4	-	0.6	-	μs
$t_{SU;STA}$	Restart condition setup time	4.7	-	0.6	-	μs
$t_{HD;DAT}$	Data hold time	0	-	0	-	μs
$t_{SU;DAT}$	Data setup time	$50+t_{I2C\_REFCLK}$	-	$50+t_{I2C\_REFCLK}$	-	ns
t_R	SCL/SDA rise time	-	1000	20	300	ns
t_F	SCL/SDA fall time	-	300	6.5	300	ns
$t_{SU;STO}$	Stop condition setup time	4	-	0.6	-	μs
t_{BUF}	BUS idle time from stop condition to start condition	4.7	-	1.3	-	μs
C_b	Load capacitance	-	400	-	400	pF

Note

1. Resulted from comprehensive evaluation, not tested in production.

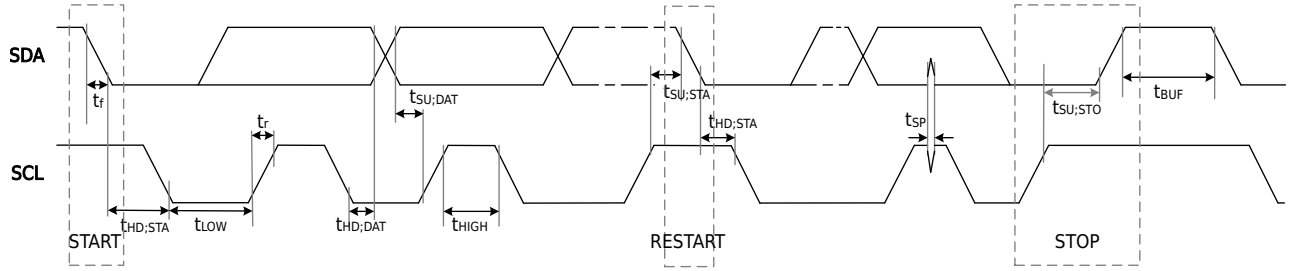


Figure 4-7 I2C Bus Timing Definition

4.3.12 SPI Interface Characteristics

Table 4-28 SPI Characteristics(1)

Symbol	Parameters	Conditions	Min	Max	Unit
t_{spcyc}	SCK clock period	Master mode, C=30pF	2	4096	T_{HCLK}
		Slave mode, C=30pF	8	4096	T_{HCLK}
t_{sckr}	SCK clock rising time	Master mode, C=30pF	-	20	ns
t_{sckf}	SCK clock falling time	Slave mode, C=30pF	-	1	μs
t_{su}	Data input setup time	Master mode, C=30pF	10	-	ns
		Slave mode, C=30pF	5	-	ns
t_h	Data input hold time	Master mode, C=30pF	T_{HCLK}	-	ns
		Slave mode, C=30pF	5	-	ns
t_{od}	Data output delay	Master mode, C=30pF	-	5	ns
		Slave mode, C=30pF	-	28	ns
t_{oh}	Data output hold time	Master mode, C=30pF	0	-	ns
		Slave mode, C=30pF	0	-	ns
t_{dr}	MOSI/MISO rising time	Master mode, C=30pF	-	20	ns
t_{df}	MOSI/MISO falling time	Slave mode, C=30pF	-	1	μs
t_{ssr}	SS rising time	Master mode, C=30pF	-	20	ns
t_{ssf}	SS falling time	Slave mode, C=30pF	-	1	μs

Note

1. Resulted from comprehensive evaluation, not tested in production.

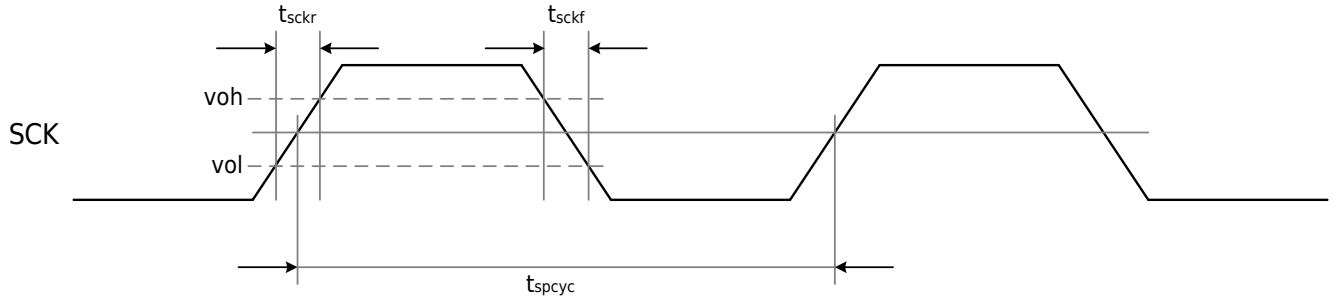


Figure 4-8 SPI Clock Definition

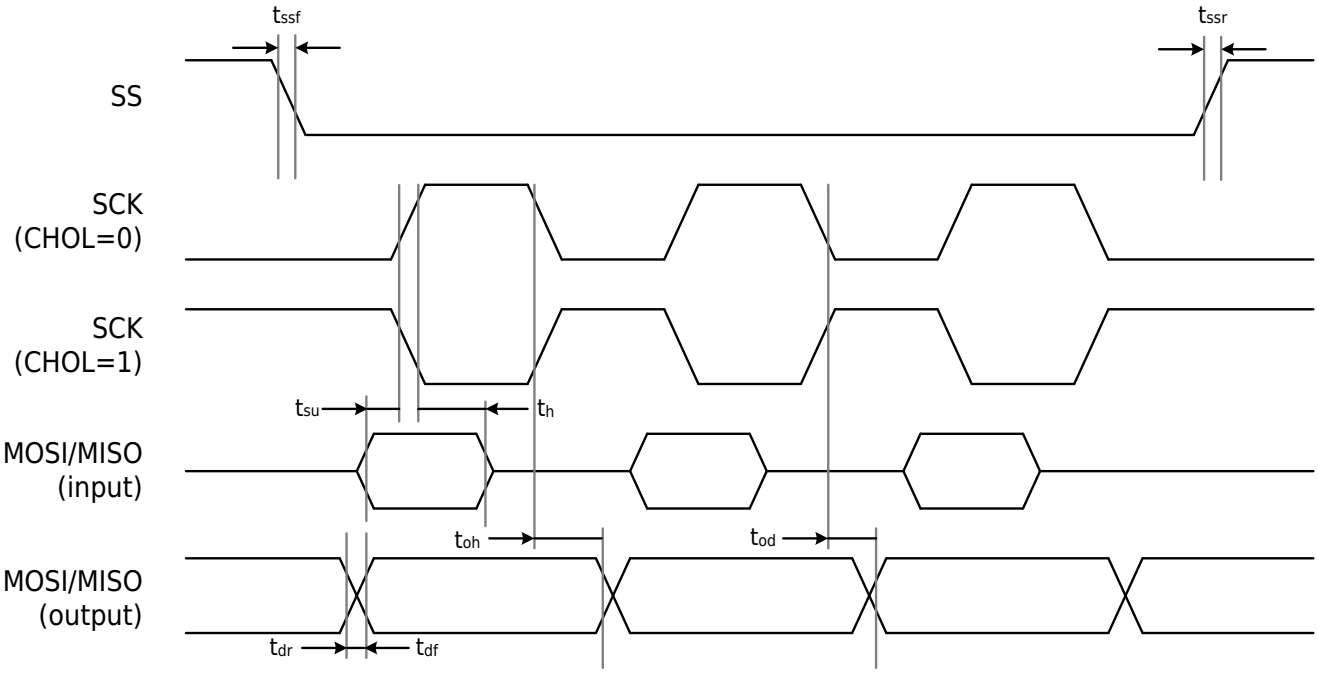


Figure 4-9 SPI Timing Definition

4.3.13 USART Interface Characteristics

Table 4-29 USART AC Timing(1)

Symbol	Parameters	Conditions	Min	Max	Unit
t_{cyc}	Input clock cycles	UART	4	-	t_{HCLK}
		Clock Synchronization Mode	6	-	
t_{CKw}	Input clock width	-	0.4	0.6	t_{cyc}
t_{CKr}	Input clock rise time	-	-	20	ns
t_{CKf}	Input clock fall time	-	-	20	ns
t_{TD}	Transmit delay time	Clock Synchronization Mode (Master)	-	10	ns
		Clock Synchronization Mode (Slave)	-	35	ns
t_{RDS}	Receive data setup time	Clock Synchronization Mode (Master)	35	-	ns
		Clock Synchronization Mode (Slave)	5	-	ns
t_{RDH}	Receive data hold time	Clock Synchronization Mode	5	-	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-30 USART Maximum Baud Rate(1)

Mode		Max Baud Rate
UART	Internal clock source	HCLK/8
	External clock source	HCLK/6
Clock Synchronization Mode	Internal clock source	4Mbps
	External clock source	6Mbps

Note

1. Resulted from comprehensive evaluation, not tested in production.

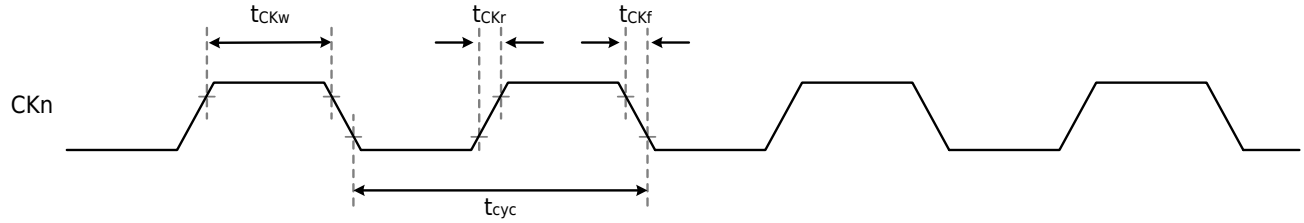


Figure 4-10 USART Clock Timing

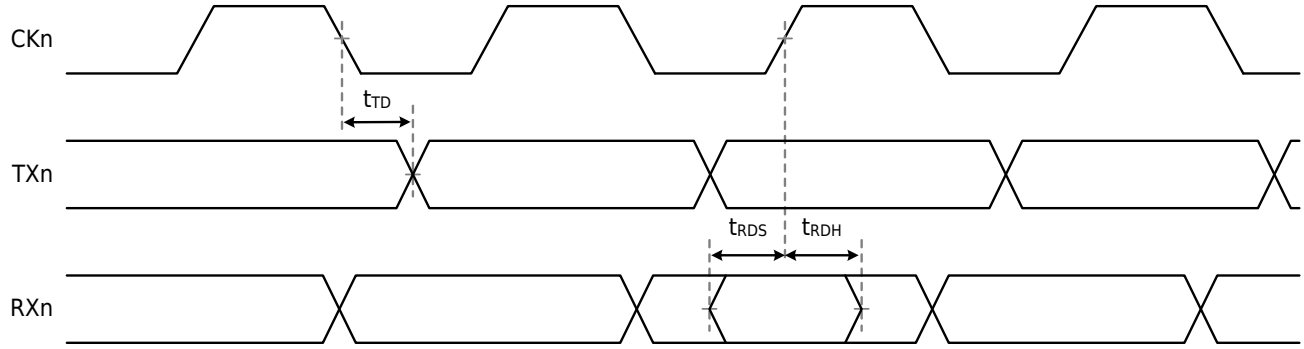


Figure 4-11 USART (CSI) Input and Output Timing

4.3.14 SWD Interface Characteristics

Table 4-31 SWD Interface Characteristics(1)

Symbol	Parameters	Min	Typ	Max	Unit
$t_{SWCLKcyc}$	SWCLK clock period	50	-	-	ns
t_{SWCLKH}	SWCLK clock high level	20	-	-	ns
t_{SWCLKL}	SWCLK clock low level	20	-	-	ns
t_{SWCLKr}	SWCLK clock rise time	-	-	5	ns
t_{SWCLKf}	SWLCK clock fall time	-	-	5	ns
t_{SWDIs}	SWDI setup time	8	-	-	ns
t_{SWDIh}	SWDI hold time	8	-	-	ns
t_{SWDOd}	SWDO data delay	2	-	40	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.

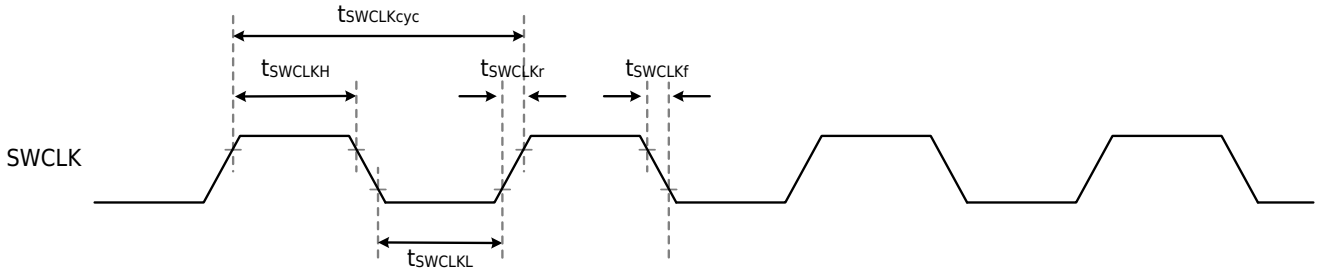


Figure 4-12 SWCLK Clock

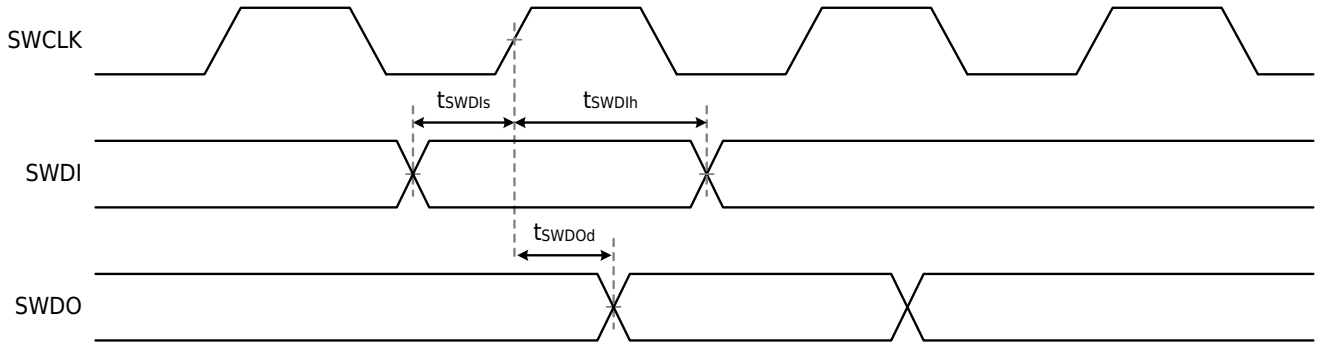


Figure 4-13 SWDIO Input and Output

4.3.15 12-bit ADC Characteristics

Table 4-32 ADC Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{AVCC}	ADC power supply	-	2.7	-	5.5	V
V_{REFH}	ADC reference voltage	-	V_{AVCC}			V
f_{ADC}	ADC conversion clock frequency	-	1	-	32	MHz
V_{AIN}	Conversion voltage range	-	V_{SSA}	-	V_{REFH}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
R_{ADC}	Sample switch resistance	See formula 1 for details.	-	-	11	kΩ
C_{ADC}	Sampling capacitor	-	-	4	7	pF
t_S	Sample time	f_{ADC}=32MHz	0.594	-	7.96	μs
			19	-	255	1/ f_{ADC}
t_{CONV}	Single channel total conversion time (Including sampling time, the calculation method is: sampling time Ts+ gradually approaching n-bit resolution +1)	f_{ADC}=32MHz 12-bit resolution	1	-	-	μs
			32	-	268	1/ f_{ADC}
		f_{ADC}=32MHz 10-bit resolution	0.94	-	-	μs
			30	-	266	1/ f_{ADC}

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
t_{CONV}	Single channel total conversion time (Including sampling time, the calculation method is: sampling time Ts+ gradually approaching n-bit resolution +1)	f_{ADC}=32MHz 8-bit resolution	0.88	-	-	μs
			28	-	264	1/ f_{ADC}
f_S	Sample rate f_{ADC}=32MHz	12-bit resolution single ADC	-	-	1	Msps
t_{ST}	Startup time	-	-	-	8	μs

Formula 1: RAIN Maximum Formula

$$R_{AIN} = \frac{k}{f_{ADC} * C_{ADC} * \ln\left(2^{N+2}\right)} - R_{ADC}$$

The above formula (Formula 1) is used to determine the maximum external impedance that makes the error less than 1/4LSB. Where N=12 (12-bit resolution) and k is the number of sampling periods defined in ADC_SSTR register.

Table 4-33 Static Accuracy

Symbol	Parameters	Conditions	Min	Max	Unit
E_T	Total Unadjusted Error	f_{ADC}=32MHz Input source impedance<1kΩ V_{AVCC}=2.7-5.5V T_A=-40℃/125℃	-8	8	LSB
E_O	Offset Error		-7.5	7.5	LSB
E_G	Gain Error		-7.5	7.5	LSB
E_D (4)	Differential Nonlinearity Error		-1	2	LSB
E_L	Integral Nonlinearity Error		-3	3	LSB

Table 4-34 Dynamic Accuracy(1)

Symbol	Parameters	Conditions	Min	Max	Unit
ENOB	Effective Number of Bits	f_{ADC} (Using crystal oscillator) Input signal frequency=2kHz V_{AVCC}=2.7-5.5V T_A=-40℃/125℃	10.5	-	Bits
SINAD	Signal-to-Noise and Distortion Ratio		62	-	dB
SNR	Signal-to-Noise Ratio		64	-	dB
THD	Total Harmonic Distortion		-	-65	dB

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. For packaging products featuring AVCC and VREFH double bonding, the ADC performance will experience a certain degree of degradation.
3. For input channels located near VCC/VSS, XTAL, or high-speed interfaces, the ADC performance will slightly decline.
4. No code loss will occur.

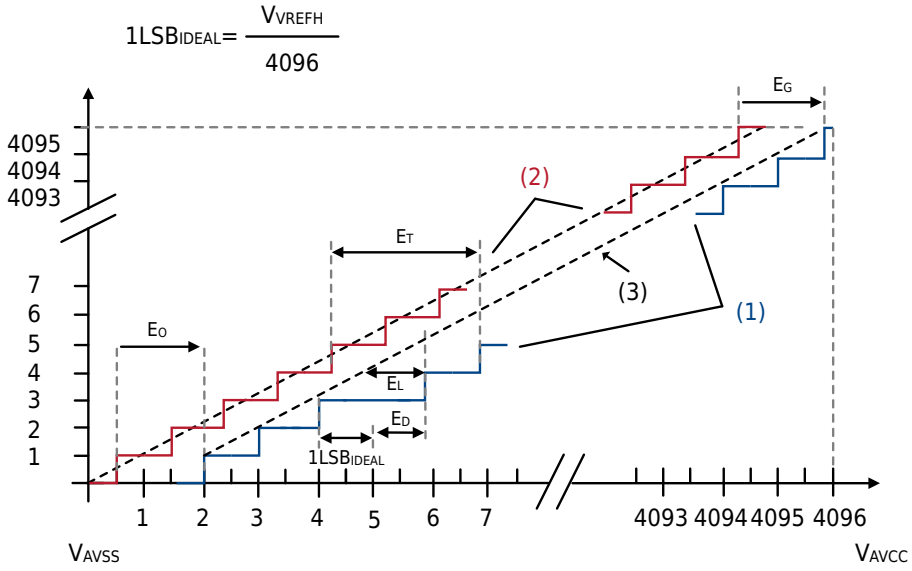


Figure 4-14 ADC Presision Characteristics

1. Examples of actual transmission curves.
2. Ideal transfer curve.
3. End point correlation line.
4. E_T = Total Unadjusted Error: Maximum deviation between actual and ideal transfer curves.
   E_O = Offset Error: Deviation between the first actual conversion and the first ideal conversion.
   E_G = Gain Error: Deviation between the last ideal conversion and the last actual conversion.
   E_D = Differential Nonlinearity Error: Maximum deviation between actual step and ideal value.
   E_L = Integral Nonlinearity Error: Maximum deviation between any actual conversion and the endpoint correlation line.

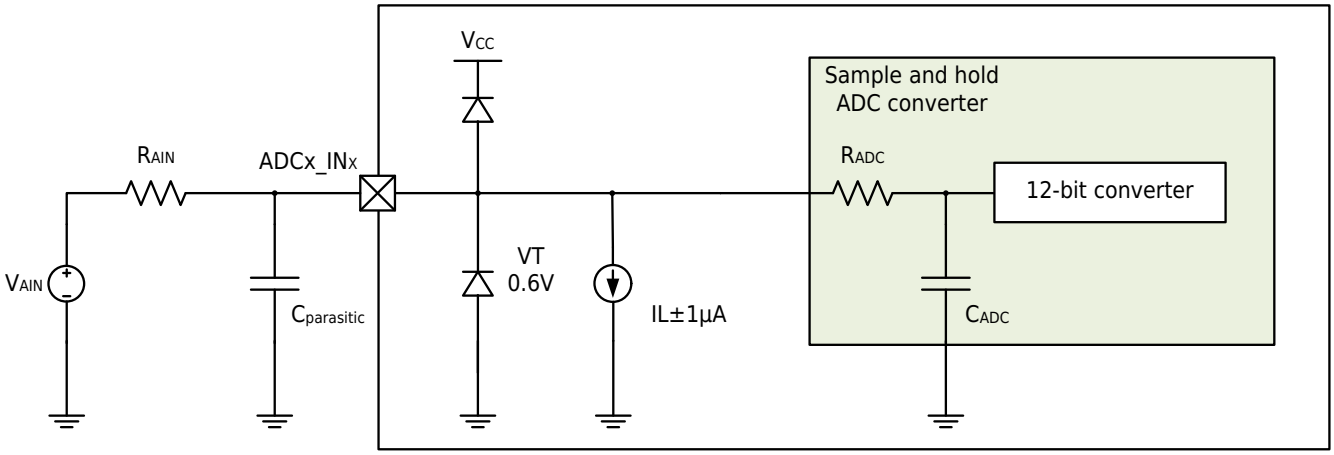


Figure 4-15 Typical connection using ADC

1. For information about R_{AIN}, R_{ADC}, and C_{ADC} values, refer to Table 4-32 : ADC Characteristics.
2. $C_{parasitic}$ indicates PCB capacitance (depending on the quality of soldering and PCB wiring) and bonding pad capacitance (about 5pF). Higher values of $C_{parasitic}$ result in less accurate conversions. To solve this problem, f_{ADC} should be reduced.

General PCB Design Guidelines

The power supply should be decoupled as shown in the following figure and the details depend on the connection of VREFH and AVCC and the number of AVCC pins. 0.1μF capacitor should be (high quality) ceramic capacitor. These capacitors should be as close to the chip as possible.

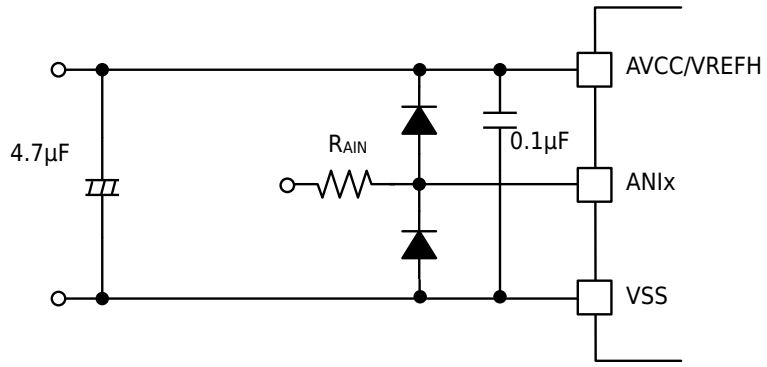


Figure 4-16 Example of Power Supply and Reference Supply Decoupling

1. For information about R_{AIN} values, refer to Table 4-32 : ADC Characteristics.

4.3.16 Comparator Characteristics

Table 4-35 Comparator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{AVCC} (2)	Analog Power Voltage	-	2.7	5.0	5.5	V
V_I (2)	Input Voltage Range	-	0	-	V_{AVCC}	V
T_{cmp} (1)	Compare Time	Comparator resolution voltage =100mV	-	100	150	ns
T_{set} (2)	Input Channel Switching Stabilization Time	Comparator resolution voltage =50mV	-	150	300	ns
T_{start} (1)	Start Time	-	-	-	3	μs

Note

1. Guaranteed by design, not tested in production.
2. Resulted from comprehensive evaluation, not tested in production.

4.3.17 DAC Characteristics

Table 4-36 DAC Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{AVCC}(1)	Analog Power Voltage	-	2.7	5.0	5.5	V
A_{ref}(1)	Reference power supply voltage (V_{REFH})	=V_{AVCC}	2.7	5.0	5.5	V
N	Resolution	-	-	8	-	bits
DNL	Differential nonlinear error (deviation between two consecutive codes -1LSB)	-	-1	-	1	LSB
INL	Integral nonlinear error (the difference between the value measured at code I and the value at code I on the line between code 0 and the last code 255)	-	-1	-	1	LSB
T_{st}(1)	Settling time (full scale: suitable for 8-bit input code conversion between the lowest input code and the highest input code when the DAC output reaches the final value of ±1/2LSB)	-	-	-	8	µs

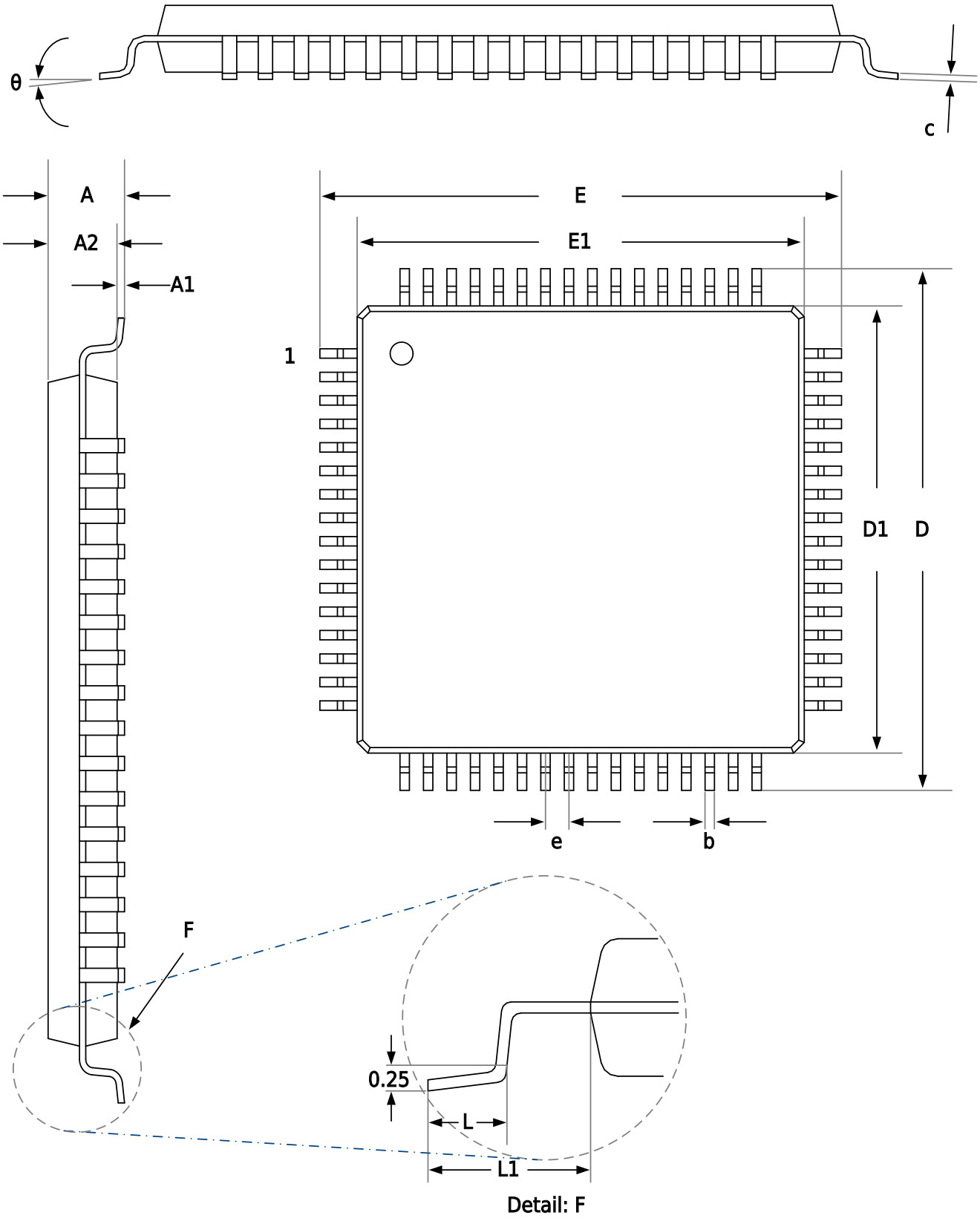
Note

1. Resulted from comprehensive evaluation, not tested in production.

5 Package Specifications

5.1 Package Dimensions

5.1.1 LQFP64 Package

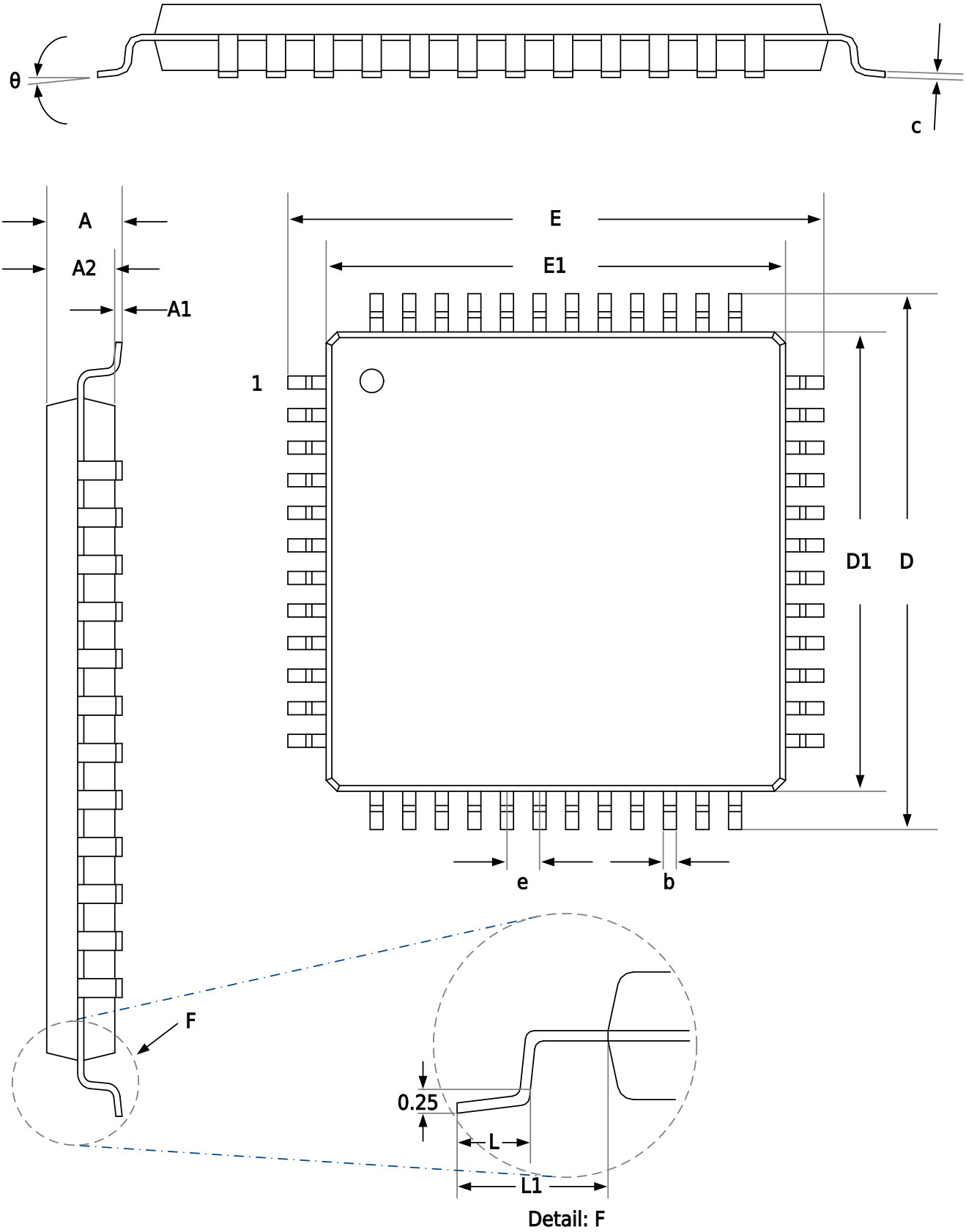


Symbol	10*10 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0°	--	7°

Note

Dimensions "D1" and "E1" do not include mold flash.

5.1.2 LQFP48 Package

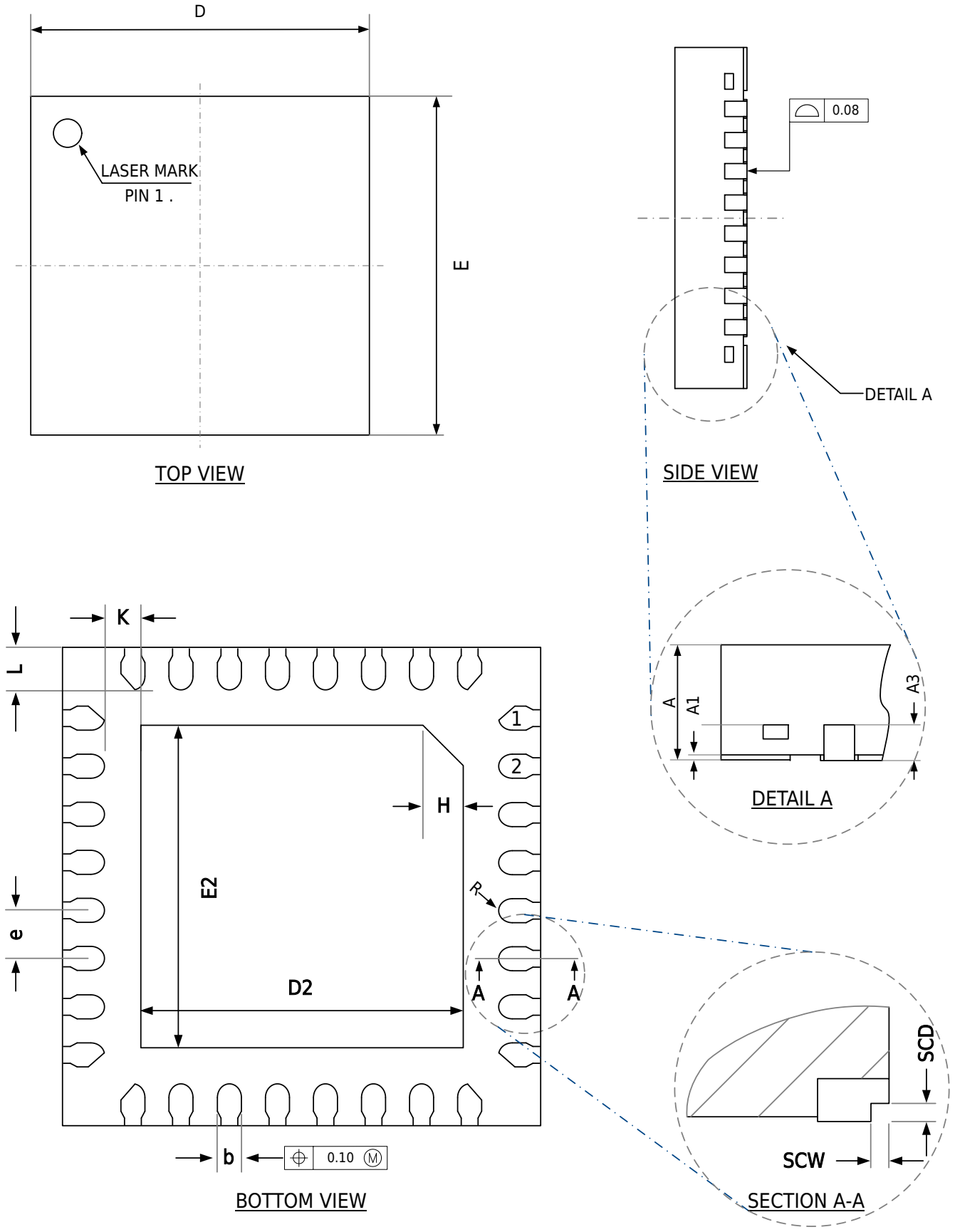


Symbol	7*7 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0	--	7°

Note

Dimensions "D1" and "E1" do not include mold flash.

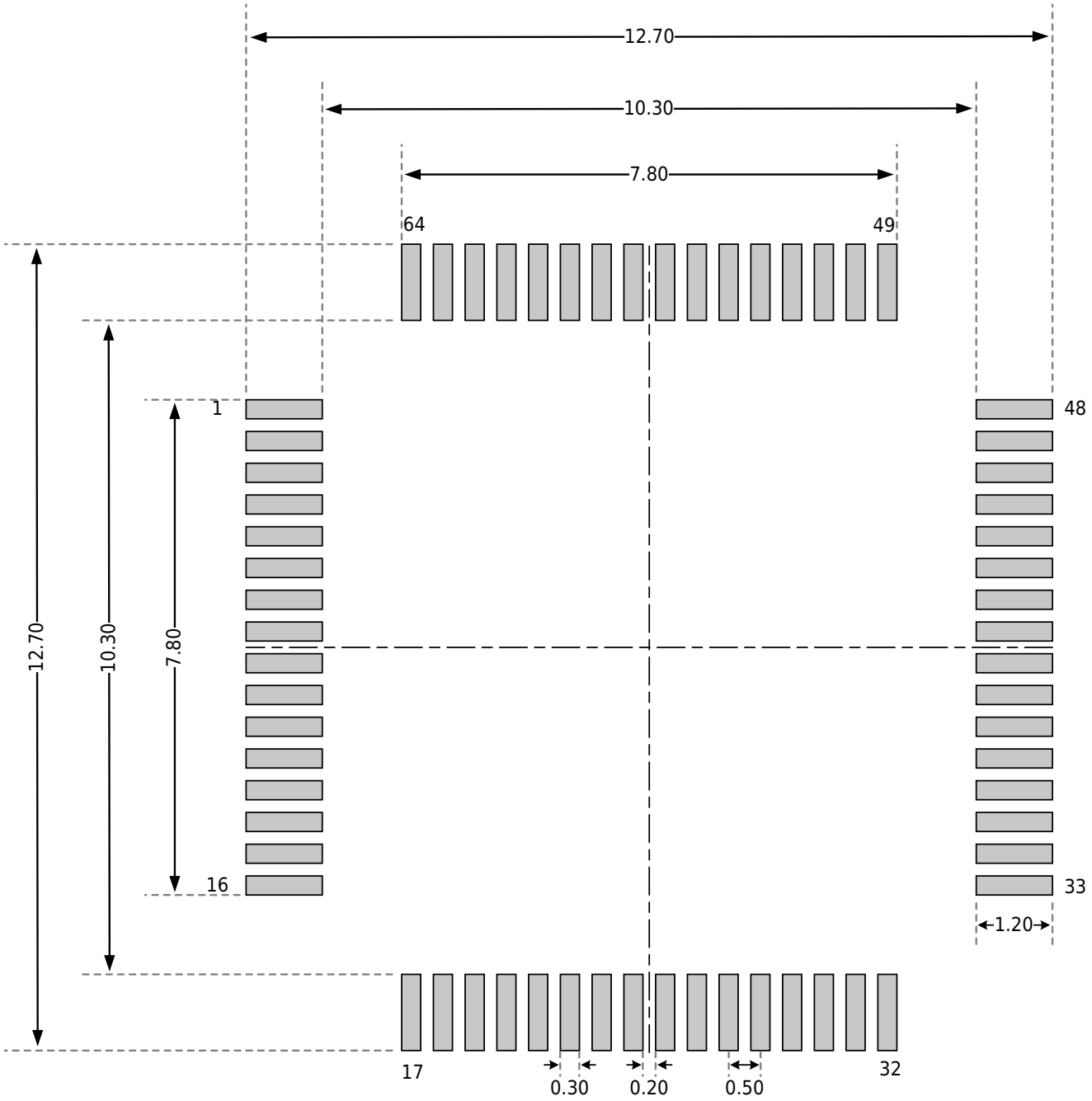
5.1.3 QFN32 Package



Symbol	5*5 Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.40	0.50	0.60
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.30	0.40	0.50
H		0.30REF	
K		0.35REF	
R	0.09	--	--
SCW	0.01	--	0.09
SCD	0.08	--	0.18

5.2 PCB Land Pattern

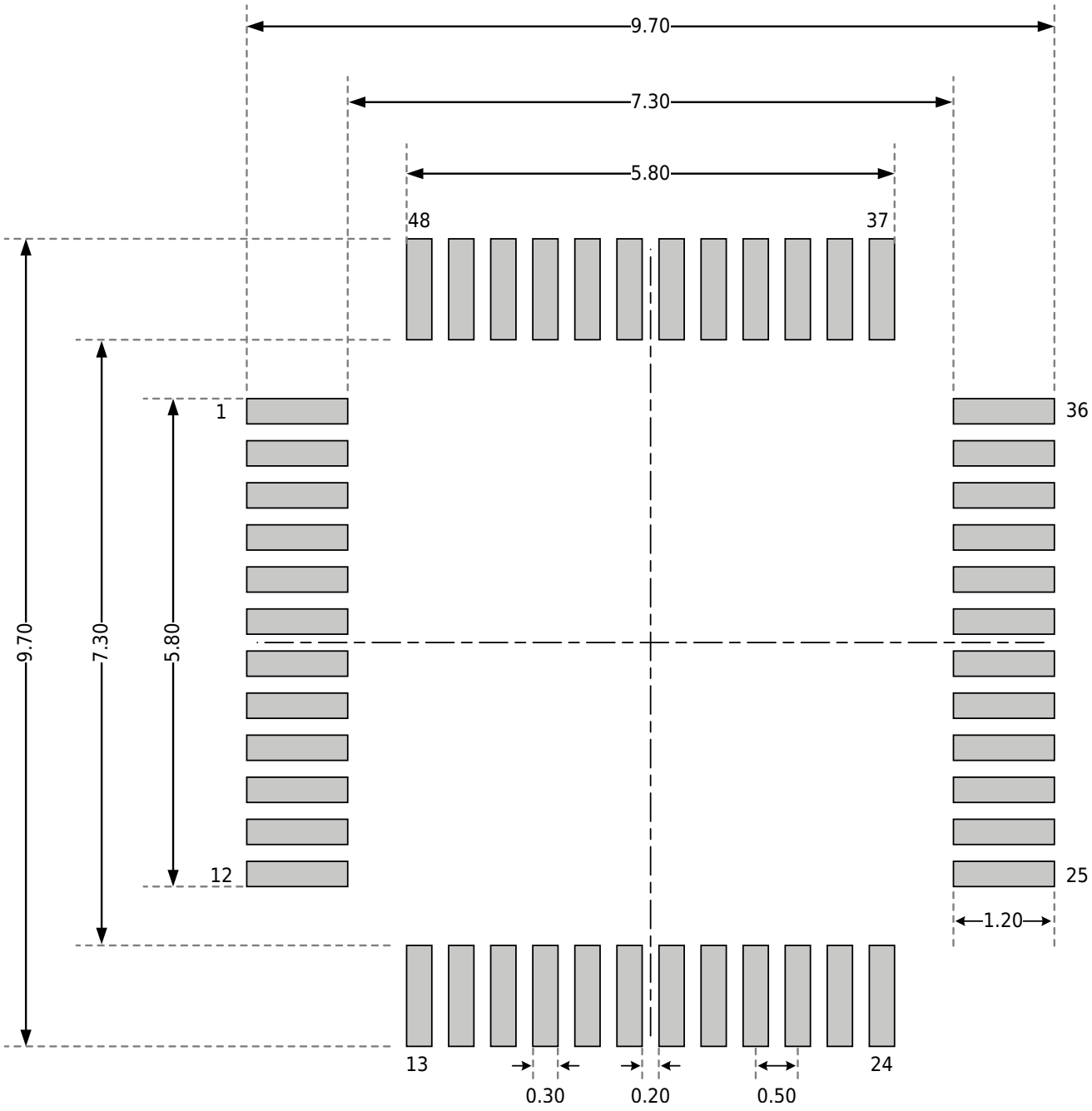
5.2.1 LQFP64 Package (10mm*10mm)



Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

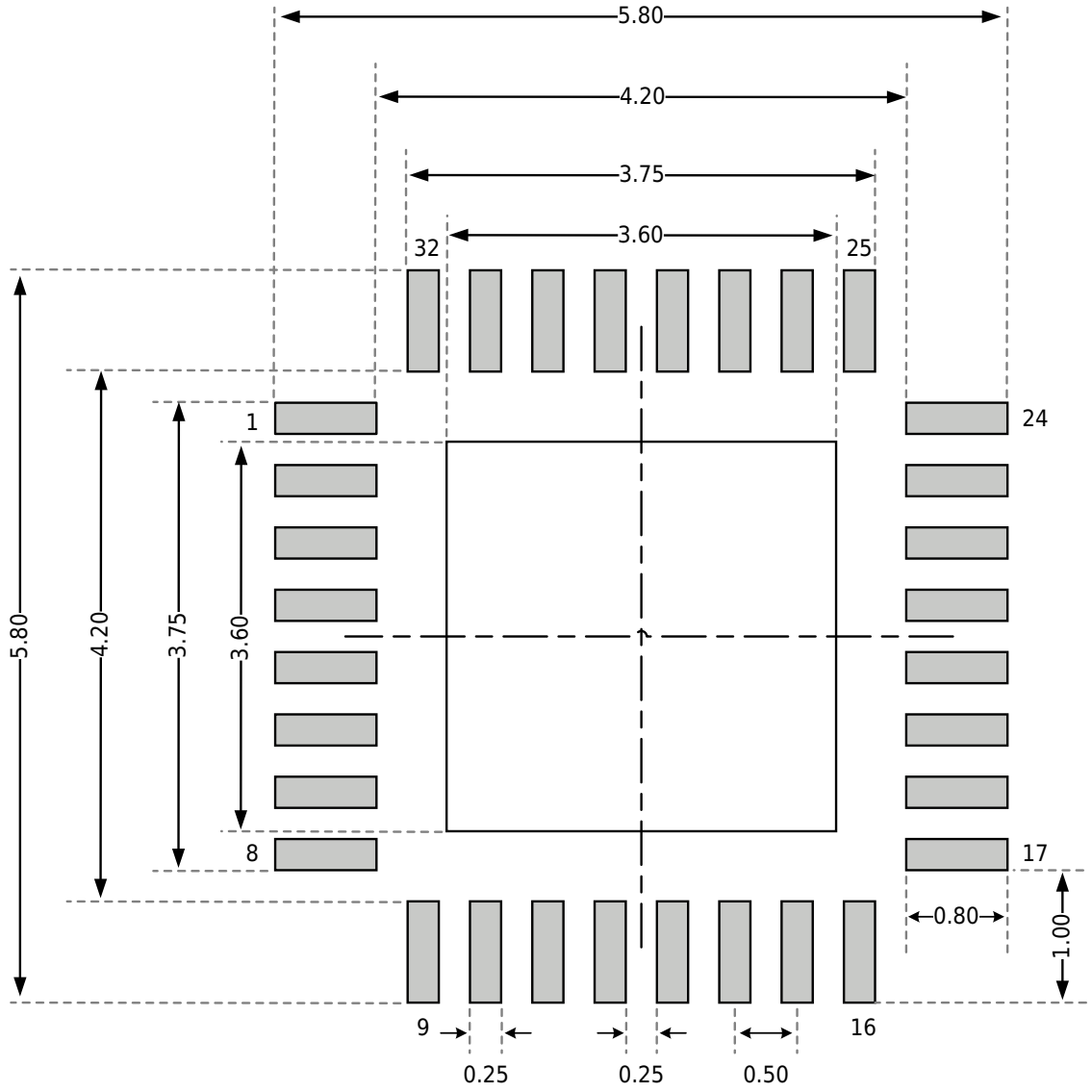
5.2.2 LQFP48 Package (7mm*7mm)



Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

5.2.3 QFN32 Package (5mm*5mm)



Note

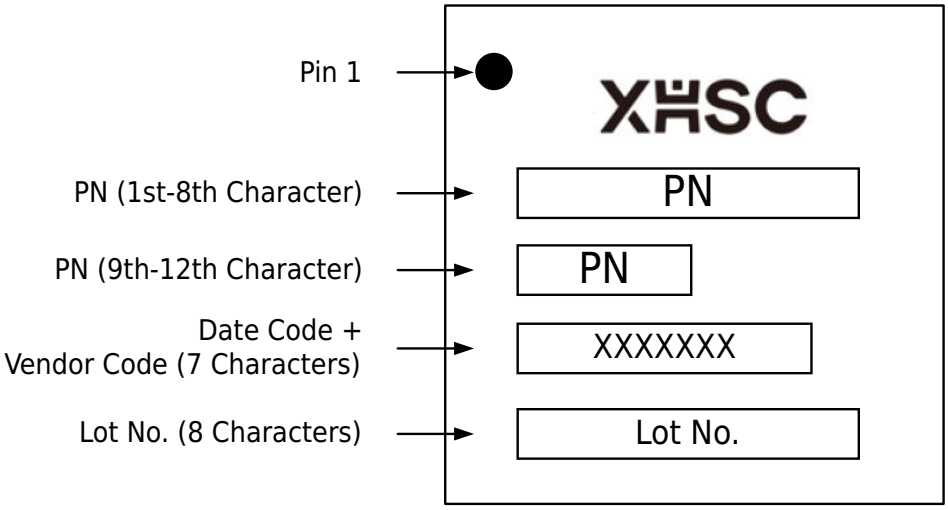
- Dimensions are in millimeters.
- Dimensions are for reference only.

5.3 Package Marking

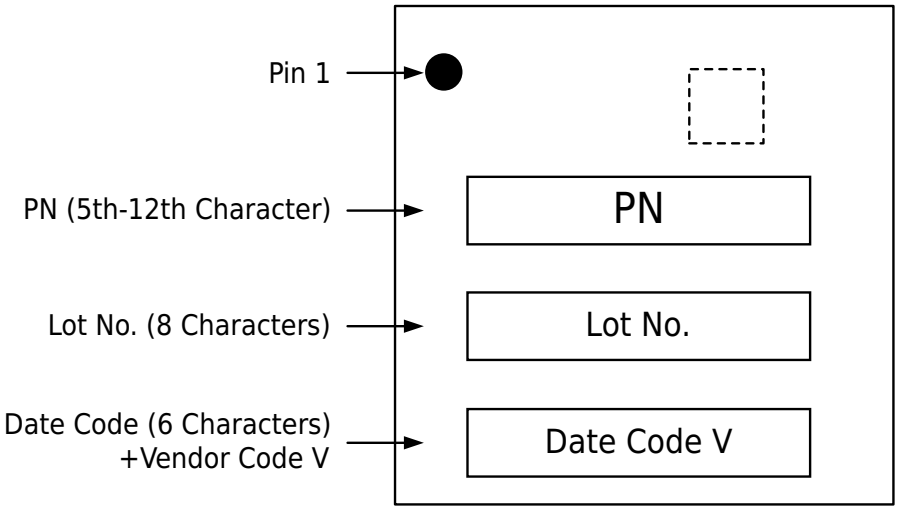
The location and information description of Pin1 on the front of each package are given below.

LQFP64 package (10mm*10mm)

LQFP48 package (7mm*7mm)



QFN32 package (5mm*5mm)



Note

The blank boxes in the above figure indicate optional marks related to production, which are not explained in this section.

5.4 Packaging Thermal Resistance Coefficient

When the packaged chip is working at the specified working environment temperature, the junction temperature T_j(℃) of the chip surface can be calculated according to the following formula:

$T_j = T_A + (P_D * \theta_{JA})$

- T_A refers to the working environment temperature when the packaged chip is working, the unit is ℃;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is ℃/W;

- P_D refers to total power dissipation, which is the sum of internal power consumption (P_{INT}) and I/O pin power consumption (P_{IO}), the unit is W.

  $P_D = P_{INT} + P_{IO}$

  - P_{INT}: Internal power consumption, calculated as the product of Icc and Vcc.
  - P_{IO}: I/O pin power consumption, calculated as: $P_{IO} = \Sigma(V_{OL} * I_{OL}) + \Sigma((V_{CC} - V_{OH}) * I_{OH})$

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable junction temperature T_{Jmax} of the chip.

Table 5-4 Thermal Resistance Coefficient Table For Each Package

Package Type and Dimensions	Thermal Resistance Parameters (θ_{JA})	Unit
LQFP64 10mm*10mm/0.5mm pitch	65±10%	℃/W
LQFP48 7mm*7mm/0.5mm pitch	75±10%	℃/W
QFN32 5mm*5mm/0.5mm pitch	52±10%	℃/W

6 Ordering Information

Part Number		HC32K118KCTJ-LQFP64	HC32K118JCTJ-LQ48	HC32K118FCUJ-QFN32	HC32K116KATJ-LQFP64	HC32K116JATJ-LQ48	HC32K116FAUJ-QFN32
GPIO		58	43	28	58	43	28
CPU	Core	Cortex-M0+	Cortex-M0+	Cortex-M0+	Cortex-M0+	Cortex-M0+	Cortex-M0+
	Frequency	64MHz	64MHz	64MHz	64MHz	64MHz	64MHz
Memory	ProgramFLASH	256KB with ECC	256KB with ECC	256KB with ECC	128KB with ECC	128KB with ECC	128KB with ECC
	DataFLASH	32KB with ECC	32KB with ECC	32KB with ECC	32KB with ECC	32KB with ECC	32KB with ECC
	EDataFLASH	2KB with ECC	2KB with ECC	2KB with ECC	2KB with ECC	2KB with ECC	2KB with ECC
	SRAM	32KB with ECC	32KB with ECC	32KB with ECC	32KB with ECC	32KB with ECC	32KB with ECC
Power Supply Voltages		2.7-5.5V	2.7-5.5V	2.7-5.5V	2.7-5.5V	2.7-5.5V	2.7-5.5V
Temp Range		-40~125℃	-40~125℃	-40~125℃	-40~125℃	-40~125℃	-40~125℃
DMA		4ch	4ch	4ch	4ch	4ch	4ch
TIMER	Timer0	1unit	1unit	1unit	1unit	1unit	1unit
	Timer2	2unit	2unit	2unit	2unit	2unit	2unit
	TimerA	1unit	1unit	1unit	1unit	1unit	1unit
	Timer4	1unit	1unit	1unit	1unit	1unit	1unit
RTC		1ch	1ch	1ch	1ch	1ch	1ch
SWDT		1ch	1ch	1ch	1ch	1ch	1ch
Connectivity	USART	4ch (2ch with LIN)	4ch (2ch with LIN)	4ch (2ch with LIN)	4ch (2ch with LIN)	4ch (2ch with LIN)	4ch (2ch with LIN)
	I2C	1ch	1ch	1ch	1ch	1ch	1ch
	SPI	2ch	2ch	2ch	2ch	2ch	2ch
	CAN FD	1ch	1ch	1ch	1ch	1ch	1ch
Analog	12-bit ADC	16ch	13ch	9ch	16ch	13ch	9ch
	CMP	1ch	1ch	1ch	1ch	1ch	1ch
LVD		2unit	2unit	2unit	2unit	2unit	2unit
CRC		√	√	√	√	√	√
CTC		1ch	1ch	1ch	1ch	1ch	1ch
Package (mm*mm)		LQFP64(10*10)	LQFP48(7*7)	QFN32(5*5)	LQFP64(10*10)	LQFP48(7*7)	QFN32(5*5)
Packing		Tray	Tray	Tape & Reel	Tray	Tray	Tape & Reel
Pitch		0.5mm	0.5mm	0.5mm	0.5mm	0.5mm	0.5mm
Thickness		1.6mm	1.6mm	0.8mm	1.6mm	1.6mm	0.8mm

Please contact the sales window for the latest mass production information before ordering.

Revision History

Revision/Date	Changes
Rev1.00 Nov. 14, 2025	First official release.