

HC32L021 Series

32-bit ARM[®] Cortex[®]-M0+ Microcontroller

Datasheet

Rev1.20
August 2026

Feature List

Support Features

- 48MHz Cortex-M0+ 32-bit CPU platform
- HC32L021 Series has a flexible power management system:
 - ▶ 0.65μA@3V DeepSleep mode: all clocks off, power-on reset active, IO state retention, IO interrupt active, all registers, RAM and CPU data save state power consumption
 - ▶ 45μA/MHz@3V@48MHz Operating Mode: CPU running, peripherals off, program running from Flash
- 64KB FLASH memory, with erase and write protection function, supports ISP, ICP, IAP, security protection level-4
- 6KB RAM memory
- GPIO: 17IO/20pin, 10IO/14pin
 - ▶ Selected IOs support input filtering
- Clock, Crystal
 - ▶ RC48M: 4/6/32/48MHz
 - ▶ RCL: 32.768/38.4kHz
 - ▶ XTL: 32.768kHz
 - ▶ Support external clock source input
- Timer/Counter
 - ▶ 2 CTIMs. Each CTIM can be configured either as one 16-bit General-Purpose Timer (GTIM) or as three 16-bit Basic Timers (BTIMs). In GTIM mode, it supports 4-channel capture/compare and 4-channel PWM output. In BTIM mode, each timer provides two toggle outputs
 - ▶ 1 advanced 16-bit timer (ATIM3) supporting 3-phase PWM outputs with dead-time insertion for complementary pairs
 - ▶ 1 Independent Watchdog, Internal Low-Speed Clock provides IWDG counting
 - ▶ 1 CTRIM module supporting ultra-low-power timing functions, enabling extended intervals up to 65536s with auto-wakeup capability, and featuring internal clock real-time calibration
 - ▶ 1 RTC calendar/counter module with up to 0.06ppm compensation accuracy
- ▶ 1 CM0+ integrated 24-bit SysTick timer
- Communication interface
 - ▶ 2-channel LPUART communication interface
 - ▶ 1-channel SPI standard communication interface
 - ▶ 1-channel I2C high-speed communication interface
- 1-way TRNG: 64-bit Random Number Generator
- Globally unique 10-byte ID number
- Integrate a high-speed and high-precision SAR ADC with a 12-bit 1Msps sampling
- 2 VCs, configurable with 64-step reference voltage ladder and 12 selectable filter levels
- Integrate a LVD supporting 16 programmable threshold levels, 12 configurable filter settings, and dual monitoring capability for both port voltages and power supply voltages
- SWD debugging solution provides a full-featured debugger
- Working conditions: -40-105°C, 1.8-5.5V
- Package: QFN20, TSSOP20, QFN14

Support Model

HC32L021C8PB-TSSOP20TR	HC32L021C8UB-ZFN20TR
HC32L021C8PB-TSSOP20	HC32L021B8UB-XFN14TR

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Preface

Number Format

- 0x prefix is used for hexadecimal numbers
- 0b prefix is used for binary numbers
- Numbers without prefix are in decimal representation

Security Statement

There may be potential security problems due to the use of a certain function or protocol, which need to be declared to remind users and avoid security risks.

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1 Product Overview

1.1 Product Lineup

Product Name

	HC	32	L	0	2	1	C	8	P	B
XiaoHua Semiconductor										
MCU Family										
32: 32-bit										
Product Type										
L: Ultra-low power										
MCU Platform										
0: Cortex-M0+										
MCU Specification Grade										
2: Low-end										
Feature Configuration										
1: Configuration 1										
Pins										
B: 14 Pin										
C: 20 Pin										
Program Capacity										
8: 64KB										
Package										
P: TSSOP										
U: QFN										
Temperature Grade										
B: -40-105°C, industrial level										

Model Function Comparison Table

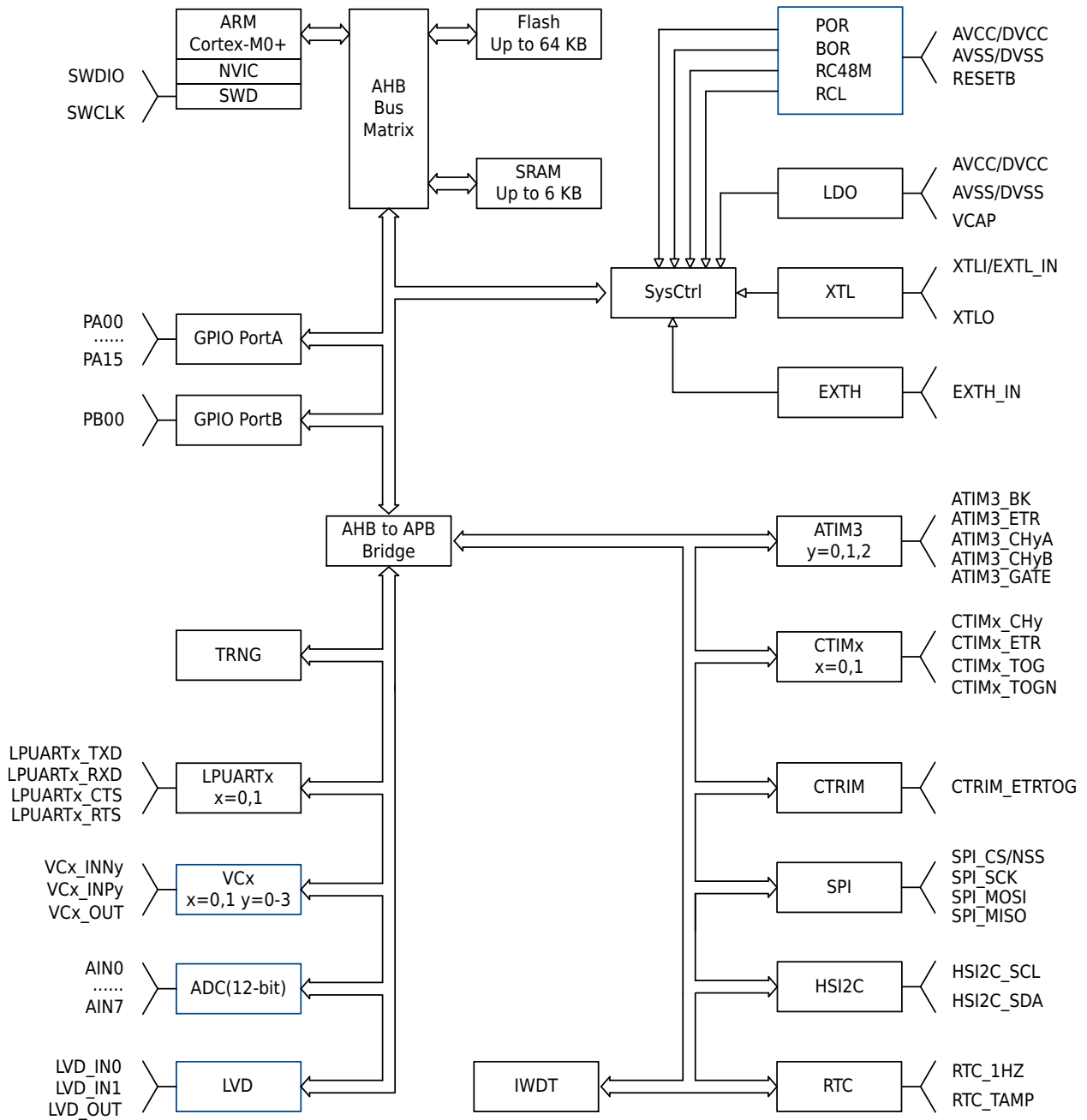
Product Name		HC32L021C8PB	HC32L021C8UB	HC32L021B8UB
Pins		20		14
GPIOs		16+1 ⁽¹⁾		9+1 ⁽¹⁾
CPU	Core	Cortex-M0+		
	Frequency	48MHz		
Memory	Flash	64KB		
	RAM	6KB		
Clock	RC48M	4/6/32/48MHz		
	RCL	32.768/38.4kHz		
	EXTH	4-24MHz		
	XTL	32.768kHz		-
Power Voltage Range		1.8-5.5V		
Single/dual Power Supply		Single power supply		
Temperature Range		-40-105°C		
Port Interrupt		17		10
Timer		General Timer CTIM0/1		General Timer CTIM0
		Advanced Timer ATIM3		
		Clock Calibration Timer CTRIM (supports low-power timer mode)		
RTC		1		
IWDT		1		
Connectivity		LPUART0/1		
		I2C (HS)		
		SPI		
ADC, 12-bit		8ch+2 (AVCC/3, VCAP)		7ch+2 (AVCC/3, VCAP)
VC		VC0/1		
LVD		1		No output
Flash Security Protection		Support		
TRNG		Support		
Debug Function		SWD debug/programming interface		
Unique Identification Code		Support (80bits)		
Package (mm*mm)		TSSOP20	QFN20 (3*3)	QFN14 (2*2)



Note

1. When the MCU is in the running state, the RESET pin can be reused as a GPIO input.

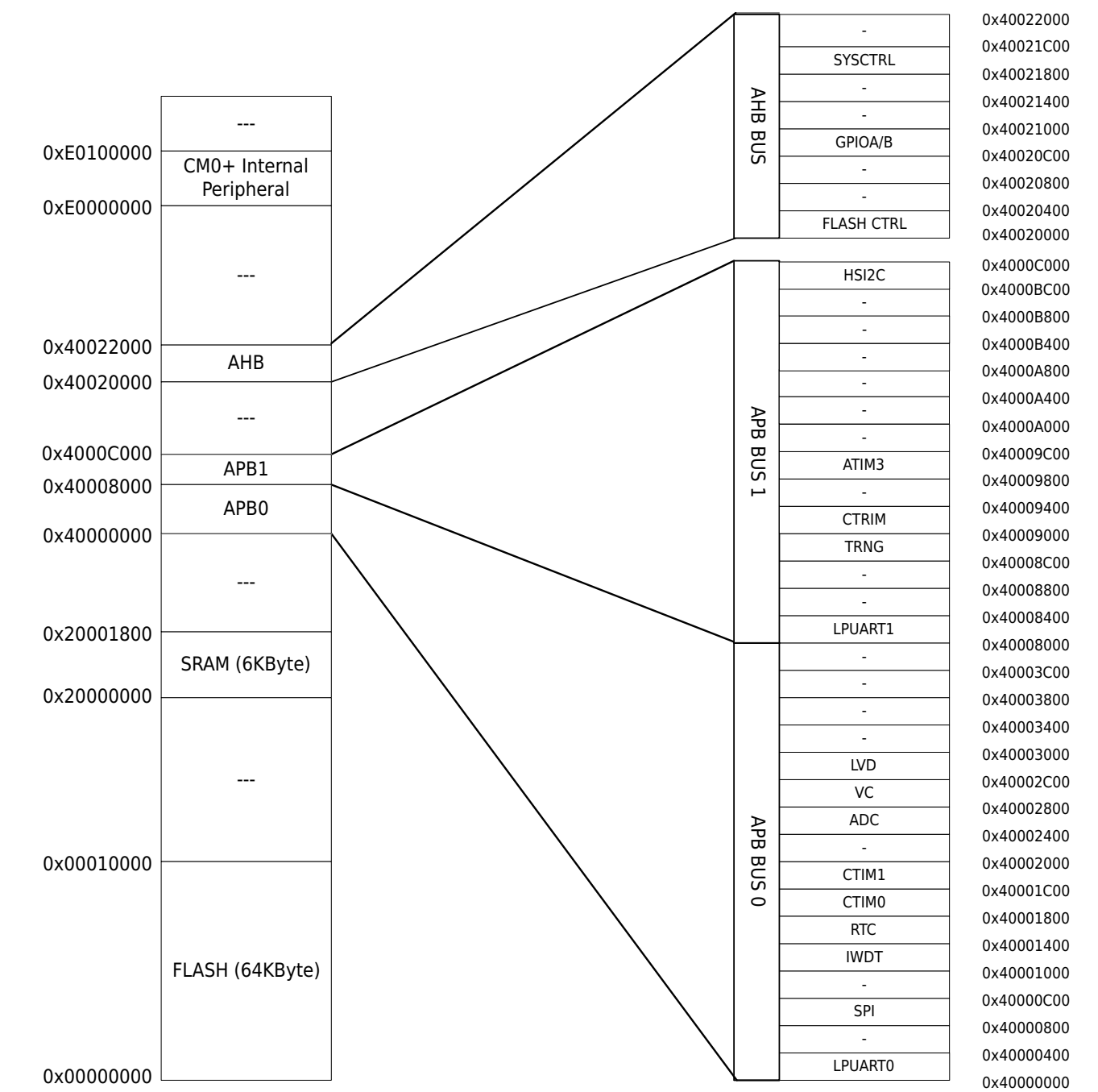
1.2 Functional Block Diagram



Note

Products in different packages support varying resources. For detailed specifications, please refer to [Model Function Comparison Table](#).

1.3 Memory Map



2 Functional Description

2.1 32-bit Cortex-M0+ Core

The ARM Cortex-M0+ processor is based on the Cortex-M0 and integrates a 32-bit RISC processor with a computing performance of 0.95 Dhrystone MIPS/MHz. It also incorporates multiple new designs, including improved debugging and tracing capabilities, reduced instructions per cycle (IPC) count, an enhanced two-stage pipeline for Flash access, and integrates energy-saving technologies. The Cortex-M0+ processor fully supports Keil & IAR debuggers.

The Cortex-M0+ includes a hardware debug circuit supporting the 2-pin SWD debug interface.

ARM Cortex-M0+ support features:

Instruction set	Thumb/Thumb-2
Assembly line	2-stage assembly line
Performance efficiency	2.46 CoreMark/MHz
Performance efficiency	0.95 DMIPS/MHz in Dhrystone
Interrupt	32 fast interrupts (For detailed interrupt specifications of this product, please refer to " NVIC ")
Interrupt priority	Configurable 4-level interrupt priority
Enhanced instruction	Multi-cycle 32-bit multiplier
Debugging	Serial-wire debug port, supports four break points and one watch point.

2.2 64KB FLASH

Built-in fully integrated FLASH controller, no need for external high voltage input, high voltage generated by the fully built-in circuit for programming. Supports ISP, IAP, ICP functions. Features 4-level security protection.

2.3 6KB RAM

RAM data is retained in any power mode.

2.4 Clock System

- A high-precision internal RC48M clock with configurable frequencies of 4/6/32/48MHz.
- An internal RCL clock with frequencies of 32.768/38.4kHz.
- An external high-speed clock source EXTH with a frequency range of 4-24MHz.
- An external 32.768kHz crystal oscillator XTL, primarily providing the RTC real-time clock.

2.5 Operating Mode

1. Active Mode: CPU running, peripheral functional modules running.
2. Sleep mode: CPU halted, peripheral functional modules running.
3. DeepSleep mode: CPU halted, high-speed clock modules disabled.

2.6 RTC

The RTC (Real-Time Clock) is a functional module supporting BCD data format, typically using a 32.768kHz crystal as its clock. It enables perpetual calendar functionality with configurable interrupt periods: month/day/hour/minute/second. 24/12 hour time mode, the hardware automatically corrects leap years. It features precision compensation, supporting either 0.96ppm or 0.06ppm precision. Software adjustments of +1/-1 are available for year/month/day/hour/minute/second, with a minimum adjustable precision of one second.

The RTC calendar recorder used to indicate time and date does not reset the register when the MCU is reset by external factors.

2.7 GPIO

It can provide up to 17 GPIO ports, some of which are multiplexed with analog ports. Each port is controlled by independent control register bits. Supports edge-triggered interrupts and level-triggered interrupts, and can wake up the MCU to working mode from various ultra-low power consumption modes. Supports bit set, bit clear, and bit set clear operations. Supports CMOS Push-Pull output, Open-Drain output. Built-in pull-up resistor, with Schmitt trigger function.

When PA02 and PA11 function as the HSI2C interface, they support level signal communication at different voltages, enabling low-voltage level recognition.

2.8 NVIC

The Cortex-M0+ processor integrates a Nested Vectored Interrupt Controller (NVIC) supporting up to 17 interrupt request (IRQ) inputs. With 4 interrupt priority levels, it can handle complex logic for real-time control and interrupt processing.

2.9 RESET

This product features 6 reset signal sources. Each reset signal can restart the CPU, reset most registers, and point the program counter (PC) to the starting address.

- Digital area power-on and power-off reset POR
- External Reset PAD, low level is reset signal
- IWDG reset
- LVD low voltage reset
- Cortex-M0+ SYSRESETREQ software reset
- Cortex-M0+ LOCKUP hardware reset

2.10 Timer

Name		Width	Prescaler	Count Direction	PWM	Capture	Complementary Output
ATIM3		16/32	1/2/4/8/16/32/64/256	Up count/ Count down/ Up and down count	6	6	3
CTIM0	GTIM0	16	1-32768	Up count	4	4	1
	BTIM0/1/2	16	1-32768	Up count	-	-	1/1/1

Name		Width	Prescaler	Count Direction	PWM	Capture	Complementary Output
CTIM1	GTIM1	16	1-32768	Up count	4	4	1
	BTIM3/4/5	16	1-32768	Up count	-	-	1/1/1
CTRIM		16	2-32768	Up count	-	-	-

The composite timer CTIM can be configured as a timer that supports 4-channel comparison capture function, or it can be configured as 3 basic timers. The basic timer is a timer with only timing and counting functions.

Advanced Timer includes timer ATIM3, supporting the following functions:

- PWM independent output, complementary output
- Capture input
- Pulse width measurement
- Quadrature encoder counting function
- Single pulse mode
- External counting function
- Dead-time control
- Braking control
- Edge alignment, symmetric center alignment and asymmetric center alignment PWM output

ATIM3 is a multi-channel general-purpose timer, capable of generating 3 sets of complementary PWM outputs or 6 independent PWM channels, with up to 6 input capture channels. With dead zone control function.

2.11 IWDG

The IWDG is a configurable 12-bit timer that provides a reset in case of MCU malfunction, with the internal RC10K clock input as the counter clock. In debug mode, it can be configured to pause or continue running; the IWDG can only be restarted by writing a specific sequence.

2.12 LPUART

2-channel Low-Power Universal Asynchronous Receiver/Transmitter (LPUART) that can operate in low-power mode.

Basic functions of LPUART:

- Configuration clock PCLK
- Transmission clock SCLK (SCLK can select XTL, RCL and PCLK)
- Support synchronous half-duplex, asynchronous full-duplex and single-wire half-duplex transmission.
- Programmable serial communication function
 - ▶ 2 character lengths: 8 bits, 9 bits
 - ▶ 3 check methods: no check, odd check, even check
 - ▶ 3 stop lengths: 1 bit, 1.5 bits, 2 bits
- Supports transmitting and receiving data in low power mode
- 16-bit baud rate counter
- Support hardware flow control (RTS, CTS)

- Support multi-machine communication and automatic address recognition

2.13 SPI

Basic features of SPI:

- Can be configured as master or slave, support multi-machine mode
- The maximum division factor in master mode is PCLK/2
- The maximum division factor in slave mode is PCLK/4
- Multiple communication modes: full-duplex, single-wire half-duplex, simplex
- 2 transmission orders: MSB first or LSB first
- Various data frame lengths: 4bits-16bits
- 2 NSS methods: hardware control, software control
- Configurable serial clock polarity and phase
- Support master mode delayed sampling

2.14 HSI2C

HSI2C supports:

- Supports standard mode, fast mode, fast enhanced mode, and high-speed mode.
- Hs-mode in slave mode.
- Supports multi-master, including synchronization and arbitration. Multi-master means any number of masters can be present. In addition, the master and slave roles can be changed during the transmission gap (after a STOP is sent).
- Supports 7-bit and 10-bit addressing.
- Supports software reset, START byte, and device ID (software support is also required).

HSI2C master supports:

- One word of command/transmit buffer (8-bit transmit data + 3-bit command), one word of receive buffer (8-bit receive data).
- The command buffer will wait for the I2C bus to be idle before starting the transmission.
- The command buffer can initialize (repeated) START and STOP conditions, as well as one or more master receive transmissions.
- The STOP condition can be generated from the command buffer or automatically when the transmit buffer is empty.
- Flexible receive data matching function can generate interrupts when data matching and/or discard unwanted data.
- Flags and optional interrupts to indicate Repeated START conditions, STOP conditions, arbitration loss, NACK, and command word errors.
- Supports configurable bus idle timeout and pin-stuck-low timeout.

HSI2C slave supports:

- Separate I2C slave registers to minimize software overhead for switching between master/slave.
- Supports SMBus alert address and broadcast address.
- Supports clock stretching.
- Supports transmit data register interrupt and receive data register interrupt.
- Software-controllable ACK or NACK, configurable ACK/NACK bit clock stretching. This is to avoid transmit buffer underrun and receive buffer overflow errors.

- Supports flags and interrupts for end of packet, STOP condition, or bit error detection.
- Support Ultra low power wake-up mode.

2.15 CTRIM

In calibration mode, this module automatically performs real-time calibration of the RC48M/RCL output frequency, making RC48M/RCL's accuracy immune to environmental variations. When the module works in timer mode, it has general timing function and can still work normally in DeepSleep mode.

2.16 Electronic Signature

Each chip has a unique 10-byte device identification number before leaving the factory, including wafer lot information, chip coordinate information, and so on.

2.17 TRNG

TRNG is a true random number generator, used to generate true random numbers.

2.18 ADC

A monotonic no missing code 12-bit successive approximation register analog-to-digital converter.

- 12-bit conversion accuracy
- 1Msps conversion speed
- Up to 10 input channels are supported, including 8 external pin inputs, 2 internal input channels (1/3 AVCC voltage, VCAP)
- 2 reference sources: AVCC voltage, EXVREF pins
- ADC voltage input range: 0-Vref
- Support SQR scan conversion
- Software can configure ADC conversion rate
- Support on-chip peripherals to automatically trigger ADC conversion, effectively reducing chip power consumption and improving real-time conversion

2.19 VC

Chip pin voltage monitoring/comparison circuit. Configurable positive/negative input channels: 4 external input channels; 2 internal input channels including 1-channel core voltage and 1-channel 64-step resistor divider voltage. Can generate asynchronous interrupts based on rising/falling edges to wake up the MCU from low-power modes. Configurable software anti-stake and window comparison functions. The PWM signal output from ATIM3 can serve as a blanking window signal to control the comparator output.

2.20 LVD

Detects chip supply voltage or pin voltage, supporting the following functions:

- 3 monitoring sources: DVCC, PA03, PA10
- 16-stage threshold voltage, 1.8-4.8V optional
- 3 interrupt triggering methods: high level/rising edge/falling edge
- 2 trigger results: reset and interrupt
- 12-stage filter configuration to prevent false triggering
- With hysteresis function, strong anti-interference

2.21 Embedded Debugging System

Embedded debugging solution, providing a full-featured real-time debugger, with standard mature Keil/IAR and other debugging and development softwares.

2.22 Programming Mode

Support programming modes: online programming and offline programming.

Support programming protocols: ISP protocol, SWD protocol.

Support programming interface: ISP protocol and SWD protocol share SWD port.

2.23 High Security

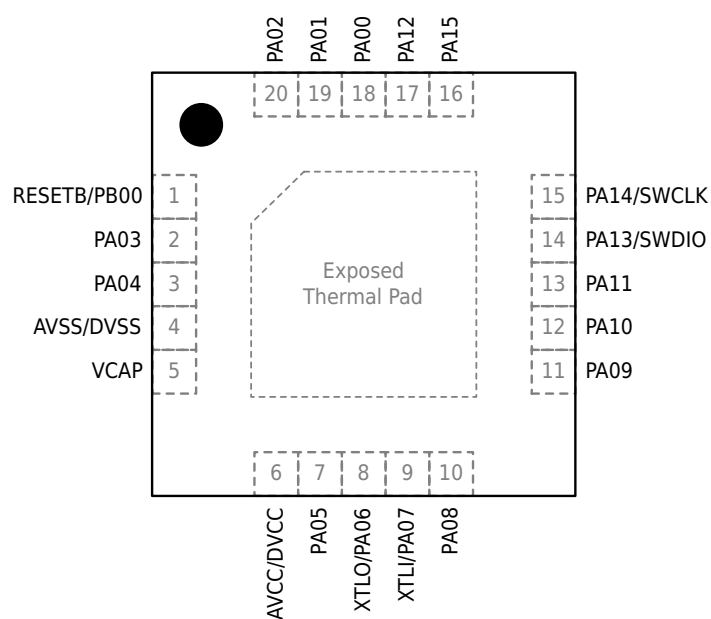
Encrypted embedded debugging solution, providing a full-featured real-time debugger.

3 Pin Definitions

3.1 Pinout

3.1.1 QFN20 Package

HC32L021C8UB-ZFN20TR

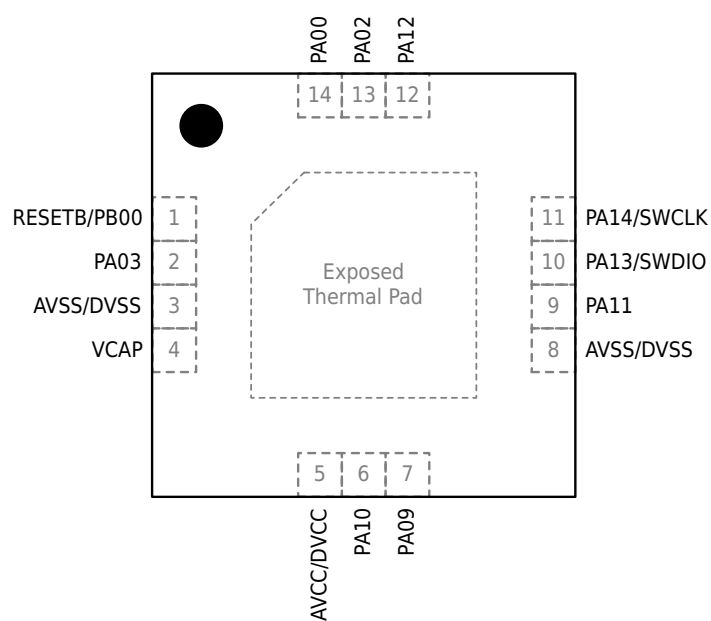


Note

- Exposed Thermal Pad needs to be connected to DVSS.

3.1.2 QFN14 Package

HC32L021B8UB-XFN14TR

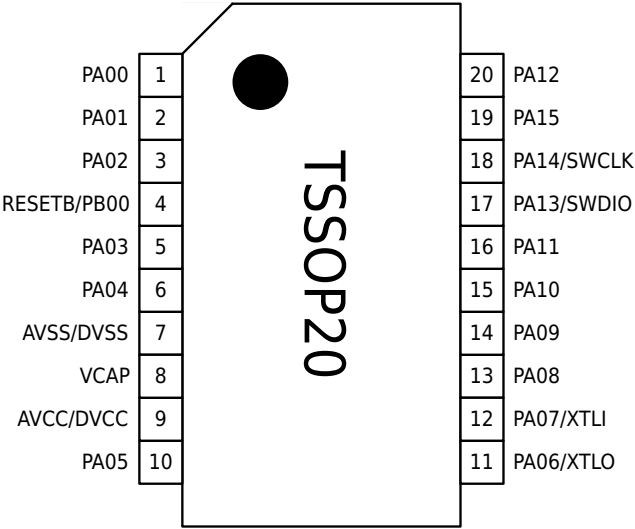


Note

Exposed Thermal Pad needs to be connected to DVSS.

3.1.3 TSSOP20 Package

HC32L021C8PB-TSSOP20/HC32L021C8PB-TSSOP20TR



3.2 Pin Function Description

TSSOP20	QFN20	QFN14	Name	Analog
1	18	14	PA00	AIN0/VC0_INN0/VC0_INP0
2	19	-	PA01	VC1_INN0/VC1_INP0
3	20	13	PA02	AIN1/EXVREF/VC0_INN1/VC0_INP1
4	1	1	RESETB/PB00	-
5	2	2	PA03	AIN2/VC1_INN1/VC1_INP1/LVD_IN0
6	3	-	PA04	-
7	4	3(8)	AVSS/DVSS	-
8	5	4	VCAP	-
9	6	5	AVCC/DVCC	-
10	7	-	PA05	AIN3
11	8	-	PA06	XTLO
12	9	-	PA07/EXTL_IN	XTLI
13	10	-	PA08	VC0_INN2/VC0_INP2
14	11	7	PA09	AIN4
15	12	6	PA10	AIN5/VC1_INN2/VC1_INP2/LVD_IN1
16	13	9	PA11/EXTH_IN	AIN6
17	14	10	PA13/SWDIO	-
18	15	11	PA14/SWCLK	-
19	16	-	PA15	VC0_INN3/VC0_INP3
20	17	12	PA12	AIN7/VC1_INN3/VC1_INP3

The digital function of each pin is controlled by the PSEL bit field, as detailed in the following table.

Table 3-2 Port Multiplexing Table

AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA00	CTIM1_CH0	LPUART1_TXD	-	-	ATIM3_CH0A	RTC_1HZ	ATIM3_GATE
PA01	LPUART1_TXD	-	-	RTC_TAMP	ATIM3_CH0B	SPI_MISO	HSI2C_SCL
PA02	LPUART1_RXD	ATIM3_CH2A	-	CTIM0_CH0	ATIM3_CH1A	SPI_MOSI	HSI2C_SDA
PA03	LPUART0_RXD	HSI2C_SDA	-	CTIM1_TOG	ATIM3_CH1B	SPI_SCK	-
PA04	LPUART0_TXD	HSI2C_SCL	-	CTIM1_TOGN	ATIM3_CH2A	SPI_CS	ATIM3_BK
PA05	CTIM1_CH3	SPI_CS	ATIM3_CH2B	-	RTC_1HZ	CTIM0_ETR	ATIM3_ETR
PA06	HSI2C_SDA	LPUART1_CTS	ATIM3_CH0B	-	SPI_SCK	LPUART0_RXD	LVD_OUT
PA07	HSI2C_SCL	LPUART1_RTS	CTIM1_ETR	-	SPI_CS	LPUART0_TXD	ATIM3_GATE
PA08	-	ATIM3_CH2B	-	CTIM0_CH0	SPI_MISO	LPUART1_TXD	IR_OUT
PA09	-	ATIM3_CH1B	-	CTIM0_CH1	SPI_MOSI	LPUART1_RXD	-
PA10	SPI_SCK	CTIM0_CH3	-	-	LPUART0_RXD	HSI2C_SDA	-
PA11	SPI_MOSI	ATIM3_CH0A	-	CTIM0_CH2	LPUART0_TXD	HSI2C_SCL	CTIM1_ETRTOG
PA12	SPI_CS	-	ATIM3_CH1A	CTIM0_CH1	LPUART1_RXD	-	LPUART0_RTS
PA13	SPI_MISO	-	ATIM3_CH2A	CTIM1_CH1	LPUART0_RXD	CTIM0_TOG	ATIM3_BK
PA14	CTIM1_ETRTOG	CTIM1_ETR	-	VC0_OUT	LPUART0_TXD	CTIM0_TOGN	TCLK_OUT
PA15	LPUART0_CTS	CTIM1_CH2	-	VC1_OUT	LPUART1_TXD	CTIM0_ETR	RTC_1HZ
PB00	-	-	-	-	CTIM0_ETR	ATIM3_ETR	ATIM3_BK

3.3 Module Signal Description

Table 3-3 Module Signal Description

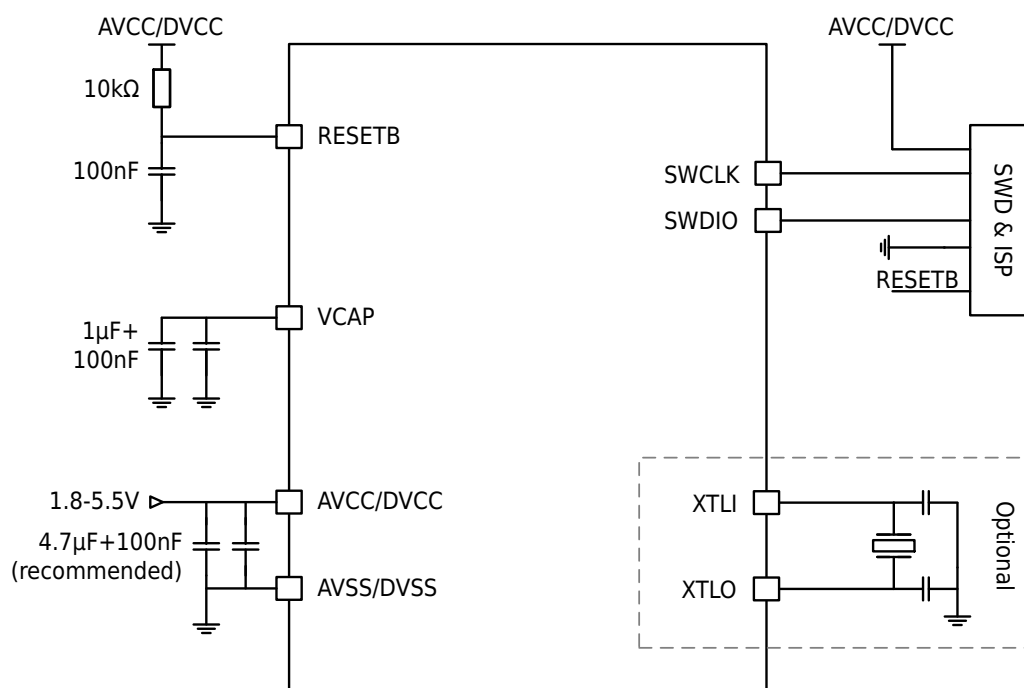
Modules	Pin Name	Description
Power supply	AVCC/DVCC	Power supply
	AVSS/DVSS	Ground
	VCAP	LDO core power supply output (only for internal circuit use, external voltage stabilization capacitor is required)
CLOCK	EXTH_IN	External high-speed clock input
	EXTL_IN	External low-speed clock input
	XTLO	External low-speed clock oscillator interface
	XTLI	External low-speed clock oscillator interface
ADC	AINx (x=0-7)	ADC input channel
	EXVREF	ADC external reference voltage
VC	VCx_INNy (x=0-1 y=0-3)	VC0/1 negative terminal input 0-3
	VCx_INPy (x=0-1 y=0-3)	VC0/1 positive terminal input 0-3
	VCx_OUT (x=0-1)	VC0/1 compare output
LVD	LVD_INx (x=0-1)	Voltage detection input
	LVD_OUT	Voltage detection output
LPUART	LPUARTx_TXD (x=0-1)	LPUART data transmitter
	LPUARTx_RXD (x=0-1)	LPUART data receiver
	LPUARTx_CTS (x=0-1)	LPUART transmit hardware flow control
	LPUARTx_RTS (x=0-1)	LPUART receive hardware flow control
CTRIM	CTRIM_ETR/TOG	CTRIM external sync signal/inverted output signal
SPI	SPI_MISO	SPI master input and slave output data signal
	SPI_MOSI	SPI master output and slave input data signal
	SPI_SCK	SPI clock signal
	SPI_CS	SPI chip selection
HSI2C	HSI2C_SDA	I2C data signal
	HSI2C_SCL	I2C clock signal
RTC	RTC_1HZ	RTC 1Hz output
	RTC_TAMP	RTC timestamp input
CTIM	CTIMx_CHy (x=0-1 y=0-3)	GTIM capture input comparison output/BTIM inverted output signal
	CTIMx_ETR (x=0-1)	External counting input signal of GTIM
	CTIMx_TOG/TOGN (x=0-1)	Inverted output signal of GTIM/BTIM

Modules	Pin Name	Description
ATIM3	ATIM3_CHyA (y=0-2)	Capture input and compare output A of ATIM3
	ATIM3_CHyB (y=0-2)	Capture input and compare output B of ATIM3
	ATIM3_ETR	External counting input signal of ATIM3
	ATIM3_BK	External brake input signal of ATIM3
	ATIM3_GATE	Gating signal of ATIM3

**Note**

The IO port is reset to the input high impedance stat, while the port states are maintained in Sleep mode and DeepSleep mode.

4 Typical Application Circuit Diagram



Notice

- Power supply requires external decoupling capacitors. For better anti-interference capability, it is preferable to route the power supply/ground lines through the decoupling capacitors first before connecting them to the chip.
- The crystal and load capacitors should be placed as close as possible to the oscillator pins of the chip.
- The VCAP decoupling capacitor should be placed as close as possible to the chip pin and kept as far away as possible from the crystal load capacitors.

5 Electrical Specifications

5.1 Parameter Conditions

Unless otherwise specified, all voltages are based on VSS.

5.1.1 Minimum and Maximum Values

All Minimum Values and Maximum Values are measured under the worst conditions.

Data resulted from comprehensive evaluation, and/or guaranteed by design are indicated in the table footnotes, and they will not be tested on the production line.

5.1.2 Typical Values

Unless otherwise specified, typical data are given based on $T_A=25^{\circ}\text{C}$ and $V_{CC}=3.3\text{V}$. These data are only used for design guidance and have not been tested.

5.2 Absolute Maximum Ratings

If the load applied to the device exceeds the value given in the list of "Absolute Maximum Ratings", it may cause permanent damage to the device. The maximum load given here is for reference, which does not mean that the functional operation of the device is correct under this condition. Operation of the device under the condition of maximum value for a long time will affect the reliability of the device.

Table 5-1 Voltage and Current Characteristics

Symbol	Parameters	Min	Max	Unit
VCC-VSS	External main supply voltage (including AVCC and DVCC) ⁽¹⁾	-0.3	6.0	V
V _{IN}	Input voltage on other pins ⁽²⁾	VSS-0.3	VCC+0.3	V
ΔVCCx	Voltage difference between different power supply pins	-	50	mV
VSSx-VSS	Voltage difference between different grounding pins	-	50	mV
V _{ESD} (HBM)	Electrostatic discharge voltage (Human model)	Refer to absolute maximum electrical parameters		V
I _{VCC}	Total current through DVCC/AVCC power line (supply current) ⁽¹⁾	-	100	mA
I _{VSS}	Total current through DVSS/AVSS ground wire (outflow current) ⁽¹⁾	-	100	mA
I _{IO}	Output sink current on any I/O and control pins	-	25	mA
	Output current on any I/O and control pins	-	-25	mA
I _{INJ(PIN)} ⁽²⁾⁽³⁾	Injection current of RESETB pin	-	±5	mA
	Injection current of the XTLL pin in XTL	-	±5	mA
	Injection current of other pins ⁽⁴⁾	-	±5	mA
ΣI _{INJ(PIN)} ⁽²⁾	Total injection current on all I/O and control pin ⁽⁴⁾	-	±25	mA

**Note**

1. All powers (DVCC, AVCC) and grounding (DVSS, AVSS) pins should always be connected to the power supply system within the external allowable range.
2. $I_{INJ(PIN)}$ should not exceed its limit, that is, ensure that V_{IN} does not exceed its maximum value. If V_{IN} cannot be guaranteed not to exceed its maximum value, it is also necessary to ensure that $I_{INJ(PIN)}$ does not exceed its maximum value externally. When $V_{IN} > VCC$, there is a forward injection current; When $V_{IN} < VSS$, there is a reverse injection current.
3. The reverse injection current will interfere with the simulation performance of the device.
4. When several I/O ports have injection currents at the same time, the maximum value of $\sum I_{INJ(PIN)}$ is the sum of the instantaneous absolute values of the forward injection current and the reverse injection current. This result is based on the features of the maximum value of $\sum I_{INJ(PIN)}$ at four I/O ports of the device.
5. The input voltage of IO with analog input channel of ADC should be between VSS and VCC; otherwise, the conversion accuracy of ADC will be affected.

Table 5-2 Temperature Characteristics

Symbol	Parameters	Value	Unit
T_{STG}	Storage temperature range	-65-+150	°C
T_{Jmax}	Maximum junction temperature	125	°C

5.3 Operating Conditions

5.3.1 General Operating Conditions

Table 5-3 General Operating Conditions

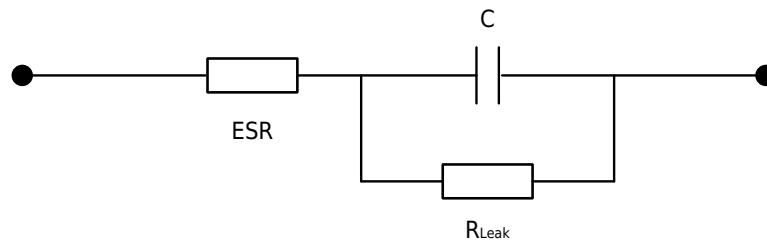
Symbol	Parameters	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK0}	Internal APB0 clock frequency	-	0	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	48	MHz
DVCC/ AVCC	Operating voltage ⁽¹⁾	-	1.8	5.5	V
T_A	Ambient temperature ⁽²⁾	-	-40	105	°C
T_J	Junction temperature range	-	-40	125	°C

**Note**

1. When using an ADC, see ADC Electrical Specifications.
2. $T_A(max)$ applies to $P_D(max)$. When $P_D < P_D(max)$, ambient temperature T_A may exceed $T_A(max)$ provided the junction temperature T_J does not exceed T_{Jmax} . For detailed specifications, refer to the [Packaging Thermal Resistance Coefficient](#).

5.3.2 VCAP External Capacitor

The stability of the main voltage regulator is achieved by connecting an external capacitor C_{EXT} to the VCAP pin. The specified values for C_{EXT} are detailed in the table below.

Figure 5-1 External Capacitor C_{EXT} **Note**

ESR stands for equivalent series resistance.

Table 5-4 VCAP Working Conditions

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$C_{EXT}^{(1)}$	External capacitance value	-	1	-	4.7	μF
ESR	External capacitor ESR	-	-	-	100	m Ω
VCAP ⁽¹⁾	LDO supply voltage	-	1.52	1.6	1.68	V

**Note**

1. Resulted from comprehensive evaluation, not tested in production.

5.3.3 Working Conditions at Power-On and Power-Down

Table 5-5 Working Conditions at Power-On and Power-Down⁽¹⁾

Symbol	Parameters	Conditions	Min	Max	Unit
S_{VCC_r}	VCC Rise Rate	-	0	1	V/ μs
S_{VCC_f}	VCC Fall Rate	-	0	0.05	V/ μs

**Note**

1. Resulted from comprehensive evaluation, not tested in production.

5.3.4 Embedded Reset and LVD Module Characteristics

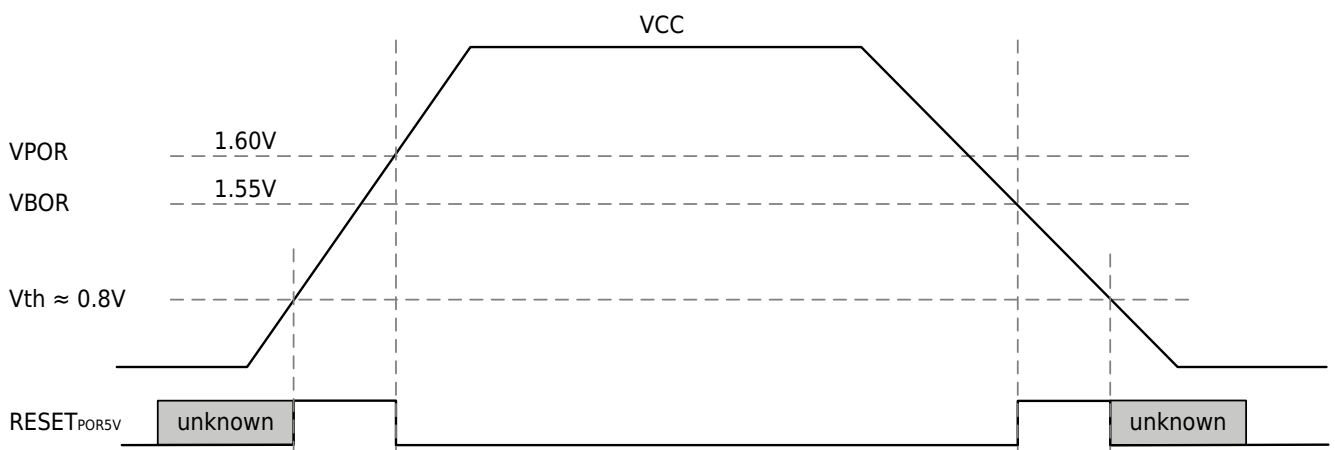


Figure 5-2 POR/Brown Out Schematic Diagram

Table 5-6 POR/Brown Out

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V _{POR}	POR release voltage (power on process)	-	1.50	1.60	1.70	V
V _{BOR}	BOR detection voltage (power down process)	-	1.40	1.55	1.65	V

Table 5-7 LVD Module Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V _{ex}	External input voltage range	-	0	-	VCC	V
V _{level}	Detection threshold	LVD_CR.VTDS=0b0000	1.70	1.80	1.90	V
		LVD_CR.VTDS=0b0001 ⁽¹⁾	1.90	2.00	2.10	V
		LVD_CR.VTDS=0b0010 ⁽¹⁾	2.10	2.20	2.30	V
		LVD_CR.VTDS=0b0011 ⁽¹⁾	2.30	2.40	2.50	V
		LVD_CR.VTDS=0b0100 ⁽¹⁾	2.50	2.60	2.70	V
		LVD_CR.VTDS=0b0101 ⁽¹⁾	2.70	2.80	2.90	V
		LVD_CR.VTDS=0b0110 ⁽¹⁾	2.90	3.00	3.10	V
		LVD_CR.VTDS=0b0111 ⁽¹⁾	3.10	3.20	3.30	V
		LVD_CR.VTDS=0b1000	3.30	3.40	3.50	V
		LVD_CR.VTDS=0b1001 ⁽¹⁾	3.45	3.60	3.75	V
		LVD_CR.VTDS=0b1010 ⁽¹⁾	3.65	3.80	3.95	V
		LVD_CR.VTDS=0b1011 ⁽¹⁾	3.85	4.00	4.15	V
		LVD_CR.VTDS=0b1100 ⁽¹⁾	4.05	4.20	4.35	V
		LVD_CR.VTDS=0b1101 ⁽¹⁾	4.25	4.40	4.55	V
		LVD_CR.VTDS=0b1110 ⁽¹⁾	4.45	4.60	4.75	V
		LVD_CR.VTDS=0b1111	4.65	4.80	4.95	V
I _{comp}	Power Consumption	-	-	0.20	-	μA
T _{response}	Response Time	Choose to detect the GPIO pin voltage, VCC=3.3V, LVD_CR.VTDS= 0b1000, the detection voltage changes from (V _{level} +100mV) to (V _{level} -100mV), and the change slope is $2 \times 10^5 \text{ V}/\mu\text{s}$	-	90	-	μs
T _{setup}	Settling time	Choose to detect the GPIO pin voltage, VCC=3.3V, LVD_CR.VTDS= 0b1000, the detection voltage is lower than V _{level} 100mV	-	400	-	μs
V _{hys}	Hysteresis voltage	-	-	60	-	mV

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
T_{filter}	Filter time	LVD_CR.DEBOUNCE_TIME=0b0000	-	0	-	μs
		LVD_CR.DEBOUNCE_TIME=0b0001	-	$2 \times T_{\text{LVD}}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b0010	-	$4 \times T_{\text{LVD}}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b0011	-	$8 \times T_{\text{LVD}}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b0100	-	$16 \times T_{\text{LVD}}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b0101	-	$32 \times T_{\text{LVD}}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b0110	-	$64 \times T_{\text{LVD}}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b0111	-	$128 \times T_{\text{LVD}}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b1000	-	$256 \times T_{\text{LVD}}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b1001	-	$512 \times T_{\text{LVD}}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b1010	-	$1024 \times T_{\text{LVD}}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b1011	-	$2048 \times T_{\text{LVD}}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b1100	-	$4096 \times T_{\text{LVD}}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b1101	-	$4096 \times T_{\text{LVD}}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b1110	-	$4096 \times T_{\text{LVD}}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b1111	-	$4096 \times T_{\text{LVD}}$	-	μs

**Note**

1. Resulted from comprehensive evaluation, not tested in production.
2. T_{LVD} represents the filter clock period, with the filter clock operating at approximately 256kHz.

5.3.5 Supply Current Characteristics

Current consumption is a comprehensive index of multiple parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin flip rate, and the location of the program in memory and the executed code, etc.

The MCU is in the following conditions:

- All I/O pins are in input mode and connected to a static level-VCC or VSS (no load).
- All peripherals are turned off, unless otherwise specified.
- The access time of the flash memory is adjusted to the frequency f_{HCLK} (0 wait cycle for 0-24MHz, 1 wait cycle for 24-48MHz)

Table 5-8 Operating Current Characteristics⁽³⁾

Symbol	Parameters	Conditions	Typ ⁽¹⁾			Unit
			25°C	85°C	105°C	
I_{DD} (Run in RAM)	All peripherals clock ON, Run while(1) in RAM	RC48M clock source	4M	405	-	μA
			6M	532	-	μA
			32M	2202	-	μA
			48M	3245	-	μA

Symbol	Parameters	Conditions		Typ ⁽¹⁾	Max ⁽²⁾		Unit
				25°C	85°C	105°C	
I _{DD} (Run in RAM)	All peripherals clock OFF, Run while(1) in RAM	RC48M clock source	4M	303	-	-	μA
			6M	379	-	-	μA
			32M	1400	-	-	μA
			48M	2010	-	-	μA
I _{DD} (Run CoreMark)	All peripherals clock OFF, Run CoreMark in Flash	RC48M clock source	4M	574	-	-	μA
			6M	738	-	-	μA
			32M	1758	-	-	μA
			48M	2473	-	-	μA
I _{DD} (Run mode)	All peripherals clock ON, Run while(1) in Flash	RC48M clock source	4M	712	912	932	μA
			6M	985	1250	1274	μA
			32M	2364	2922	2942	μA
			48M	3378	4158	4179	μA
	All peripherals clock OFF, Run while(1) in Flash	RC48M clock source	4M	610	789	809	μA
			6M	832	1064	1089	μA
			32M	1556	1940	1960	μA
			48M	2140	2656	2678	μA
I _{DD} (Sleep mode)	All peripherals clock ON	RC48M clock source	4M	335	433	442	μA
			6M	426	543	553	μA
			32M	1638	2012	2021	μA
			48M	2387	2919	2928	μA
	All peripherals clock OFF	RC48M clock source	4M	232	309	318	μA
			6M	272	357	367	μA
			32M	827	1032	1042	μA
			48M	1148	1422	1431	μA
I _{DD} (LP Run)	All peripherals clock ON, Run while(1) in Flash	32K clock source	RCL32K ⁽⁴⁾	80	109	123	μA
			XTL32K, Driver=2	76	106	122	μA
	All peripherals clock OFF, Run while(1) in Flash	32K clock source	RCL32K ⁽⁴⁾	79	108	122	μA
			XTL32K, Driver=2	75	103	120	μA
I _{DD} (LP Sleep)	All peripherals clock ON,	32K clock source	RCL32K ⁽⁴⁾	77	105	119	μA
			XTL32K, Driver=2	75	103	117	μA
	All peripherals clock OFF,	32K clock source	RCL32K ⁽⁴⁾	76	104	118	μA
			XTL32K, Driver=2	75	103	116	μA
I _{DD} (Deep-Sleep)	All peripherals clock OFF	NO CLK		0.65	3.60	7.70	μA
		RCL32K ⁽⁴⁾		0.92	4.30	8.40	μA
		XTL32K		1.39	4.70	8.80	μA
	Other peripherals clock OFF	RCL32K+IWD ⁽⁴⁾		1.02	4.40	8.60	μA
		RCL32K+LVD ⁽⁴⁾		1.06	4.70	8.70	μA
		RCL32K+IWD ⁽⁴⁾ +LVD ⁽⁴⁾		1.19	4.90	8.90	μA

**Note**

1. Unless otherwise specified, typical values are measured at $V_{CC}=3.3V$ and $V_{CAP}=1.6V$.
2. Unless otherwise specified, maximum values are measured across the full operating voltage range of V_{CC} with $V_{CAP}=1.6V$.
3. Resulted from comprehensive evaluation, not tested in production.
4. This data was measured under the condition of RCL@LPM. The typical value data in HPM mode is approximately $0.4\mu A$ higher than that in LPM mode.

5.3.6 Time to Wake-Up from Low-Power Mode

The wake-up time is measured during the wake-up phase of the RC48M oscillator. The clock source used when waking up depends on the current operating mode:

- Sleep mode: clock source is RC48M oscillator
- DeepSleep mode: clock source is RC48M oscillator

Table 5-9 Low-Power Mode Wake-Up Time

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$T_{WU}^{(1)}$	Sleep mode wake-up time	-	-	1.8	-	μs
	DeepSleep mode wake-up time	$F_{RC48M}=4MHz$	-	20.0	-	μs
		$F_{RC48M}=6MHz$	-	20.0	-	μs
		$F_{RC48M}=32MHz$	-	15.0	-	μs
		$F_{RC48M}=48MHz$	-	15.0	-	μs

**Note**

1. Guaranteed by design, not tested in production.
2. The wake-up time is measured from the start of the wake-up event to the user program reading the first instruction.

5.3.7 External Clock Source Characteristics

5.3.7.1 External Input High-Speed Clock

Table 5-10 External Input High-Speed Clock Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{EXTH}	User external clock frequency	-	4	8	24	MHz
V_{EXTHH}	Input pin high level voltage	-	$0.7V_{CC}$	-	V_{CC}	V
V_{EXTHL}	Input pin low level voltage	-	V_{SS}	-	$0.3V_{CC}$	V
$T_{r(EXTH)}$	Rising time	-	-	-	20	ns
$T_{f(EXTH)}$	Falling time	-	-	-	20	ns
$T_{w(EXTH)}$	Enter high or low time	-	16	-	-	ns
$C_{in(EXTH)}$	Input capacitance	-	-	5	-	pF

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Duty	Duty cycle	-	40	-	60	%
I_L	Input leakage current	-	-	-	± 1	μA

**Note**

1. Guaranteed by design, not tested in production.

5.3.7.2 External Input Low-Speed Clock

Table 5-11 External Input Low-Speed Clock⁽¹⁾

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{EXTL}	User external clock frequency	-	0	32.768	1000	kHz
V_{EXTLH}	Input pin high level voltage	-	0.7VCC	-	VCC	V
V_{EXTLL}	Input pin low level voltage	-	VSS	-	0.3VCC	V
$T_{r(EXTL)}$	Rising time	-	-	-	50	ns
$T_{f(EXTL)}$	Falling time	-	-	-	50	ns
$T_{w(EXTL)}$	Enter high or low time	-	450	-	-	ns
$C_{in(EXTL)}$	Input capacitance	-	-	5	-	pF
Duty	Duty cycle	-	30	-	70	%
I_L	Input leakage current	-	-	-	± 1	μA

**Note**

1. Guaranteed by design, not tested in production.

5.3.7.3 External Low-Speed Crystal XTL

The external low-speed crystal (XTL) can be generated using a 32.768kHz crystal/ceramic resonator oscillator. The information given in this section is based on typical external components and the results obtained through comprehensive characteristic evaluation. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and settling time at startup. For detailed parameters (frequency, package, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Table 5-12 External Low-Speed Crystal XTL Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
F_{CLK}	Oscillator frequency	-	-	32.768	-	kHz
ESR_{CLK}	Supported crystal ESR range	-	-	-	60	k Ω
$C_{Lx}^{(2)}$	Matching capacitance	Configure as required by the crystal manufacturer.	4	12	20	pF
DC_{ACLK}	Duty Cycle	-	30	50	70	%

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$I_{dd}^{(3)}$	Electrorheograph	XTL_CR[3:0]=0b1111	-	1330	-	nA
		XTL_CR[3:0]=0b1011	-	1230	-	
		XTL_CR[3:0]=0b0111	-	1140	-	
		XTL_CR[3:0]=0b0011	-	1050	-	
		XTL_CR[3:0]=0b1110	-	630	-	
		XTL_CR[3:0]=0b1010	-	580	-	
		XTL_CR[3:0]=0b0110	-	530	-	
		XTL_CR[3:0]=0b0010	-	490	-	
		XTL_CR[3:0]=0b1101	-	400	-	
		XTL_CR[3:0]=0b1001(Recommended value)	-	370	-	
		XTL_CR[3:0]=0b0101	-	350	-	
		XTL_CR[3:0]=0b0001	-	310	-	
		XTL_CR[3:0]=0b1100	-	290	-	
		XTL_CR[3:0]=0b1000	-	270	-	
		XTL_CR[3:0]=0b0100	-	250	-	
		XTL_CR[3:0]=0b0000	-	230	-	
g_m	Transconductance	XTL_CR[3:0]=0b1111	-	14.64	-	μS
		XTL_CR[3:0]=0b1011	-	13.17	-	
		XTL_CR[3:0]=0b0111	-	11.67	-	
		XTL_CR[3:0]=0b0011	-	10.15	-	
		XTL_CR[3:0]=0b1110	-	7.37	-	
		XTL_CR[3:0]=0b1010	-	6.62	-	
		XTL_CR[3:0]=0b0110	-	5.87	-	
		XTL_CR[3:0]=0b0010	-	5.10	-	
		XTL_CR[3:0]=0b1101	-	4.94	-	
		XTL_CR[3:0]=0b1001(Recommended value)	-	4.44	-	
		XTL_CR[3:0]=0b0101	-	3.93	-	
		XTL_CR[3:0]=0b0001	-	3.41	-	
		XTL_CR[3:0]=0b1100	-	3.72	-	
		XTL_CR[3:0]=0b1000	-	3.34	-	
		XTL_CR[3:0]=0b0100	-	2.95	-	
		XTL_CR[3:0]=0b0000	-	2.57	-	
$T_{start}^{(4)}$	Start time	ESR=30k Ω C_{Lx} =12pF XTL_CR[3:0]=0b1010	-	2000	-	ms

**Note**

1. Resulted from comprehensive evaluation, not tested in production.
2. C_{Lx} refers to the two pin matching capacitors C_{L1} and C_{L2} of the crystal. It is recommended to use high-quality ceramic capacitors, and select a crystal or resonator that meets the requirements. Usually C_{L1} and C_{L2} have the same parameters. When selecting C_{Lx} , one should take into account parameters such as the crystal oscillator's frequency and ESR, as well as the total parasitic capacitance to ground (C_p) from the PCB and MCU pins.

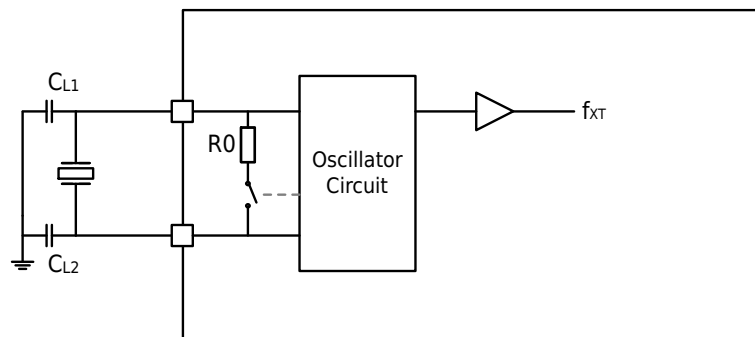
The C_{Lx} is recommended to be configured in accordance with the requirements of the crystal manufacturer's technical manual.

- If the crystal manufacturer gives *the value of the load capacitance* (C_L), the matching capacitance $C_{Lx} = 2 * C_L - C_p$.
- If the crystal manufacturer gives *the value of the matching capacitance*, the matching capacitance $C_{Lx} = \text{matching capacitance value} - C_p$.

In practical applications, if a larger C_{Lx} is selected, it is recommended to choose an appropriate current level setting.

Example:

- When the crystal manufacturer gives the load capacitance of the crystal as 8pF, considering the distributed capacitance between the PCB and MCU pins, it is recommended to choose a matching capacitor with a capacitance of 12pF.
 - When the crystal manufacturer gives the matching capacitance of the crystal as 12pF, considering the distributed capacitance between the PCB and MCU pins, it is recommended to choose a matching capacitor with a capacitance of 10pF or 8pF.
3. Choose a high-quality oscillator with a small ESR value, and you can optimize the current consumption by adjusting the `SYSCTRL_XTLCR[3:0]` setting value. Current consumption is proportional to the transconductance (g_m) provided by the circuit.
 4. T_{start} is the start-up time, which is the time from the software enabling XTL to start measuring until a stable 32768Hz oscillation is obtained. This value is measured using a standard crystal resonator with the settings `SYSCTRL_XTLCR[3:0]=0b1001` and `SYSCTRL_XTLCR[5:4]=0b10`. It may vary greatly depending on the crystal manufacturer and model.

**Note**

- The feedback resistance $R0$ has been integrated in the chip.

5.3.8 Internal Clock Source Characteristics

5.3.8.1 RC48M

Table 5-13 Internal High-Speed Clock RC48M Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
F_{CLK}	Oscillator frequency	-	4.0	4.0 6.0 32.0 48.0	48.0	MHz
TRIM ⁽¹⁾	User-adjustable frequency step size	-	-	0.12	-	%
Dev ⁽¹⁾	Oscillation frequency range under different temperatures and VCC conditions	$V_{CC}= 3.3V$ $T_A= 25^{\circ}C$	-0.3	-	0.3	%
		$V_{CC}= 1.8-5.5V$ $T_A= -40-105^{\circ}C$ $F_{CLK}= 4/6MHz$	-1.5	-	1.5	
		$V_{CC}= 1.8-5.5V$ $T_A= -40-105^{\circ}C$ $F_{CLK}= 32/48MHz$	-1.5	-	1.5	
I_{CLK}	Power consumption	$F_{CLK}= 4MHz$	-	60	-	μA
		$F_{CLK}= 6MHz$	-	66	-	
		$F_{CLK}= 32MHz$	-	176	-	
		$F_{CLK}= 48MHz$	-	220	-	
DC _{CLK} ⁽²⁾	Duty cycle	-	45	50	55	%
$t_{su}^{(2)}$	Startup time (from enable to clock output initiation)	$F_{CLK}= 4MHz$	-	8.8	20.1	μs
		$F_{CLK}= 6MHz$	-	8.5	19.8	
		$F_{CLK}= 32MHz$	-	4.7	12.9	
		$F_{CLK}= 48MHz$	-	4.7	12.8	



Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.

5.3.8.2 RCL

Table 5-14 Internal Low-Speed Clock RCL Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
F_{CLK}	Oscillator frequency@HPM	$V_{CC}=3.3V$ $T_A=25^{\circ}C$	38.2 32.5	38.4 32.768	38.6 33	kHz
TRIM ⁽¹⁾	User-adjustable frequency step size	-	-	0.5	-	%

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Dev ⁽¹⁾⁽²⁾	RCL oscillator accuracy@HPM	V _{CC} =1.8-5.5V T _A =-40-105°C	-2.5	-	2.5	%
	RCL oscillator accuracy@LPM		-15	-	15	%
T _{CLK}	Start time	-	-	150	-	μs
DC _{CLK} ⁽¹⁾	Duty Cycle	-	25	50	75	%

**Note**

1. Resulted from comprehensive evaluation, not tested in production.
2. The HPM or LPM mode can be selected through register configuration. For detailed information, please refer to the "RCL Control Register (RCL_CR)" register of "System Controller (SYSCTRL)" chapter in the "Reference Manual".

5.3.8.3 RC10K**Table 5-15 Internal Low-Speed Clock RC10K Characteristics**

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Dev ⁽¹⁾	Oscillator accuracy	V _{CC} =1.8-5.5V T _A =-40-105°C	-50	-	50	%
F _{CLK}	Oscillator frequency	V _{CC} <3.3V T _A =25°C	-	10	-	kHz

**Note**

1. Resulted from comprehensive evaluation, not tested in production.

5.3.8.4 RC256K**Table 5-16 Internal Low-Speed Clock RC256K Characteristics**

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
F _{CLK}	Oscillator frequency	V _{CC} =3.3V T _A =25°C	-	256	-	kHz
Dev ⁽¹⁾	RCL oscillator accuracy	V _{CC} =1.8-5.5V T _A =-40-105°C	-5.5	-	5.5	%
DC _{CLK} ⁽¹⁾	Duty cycle	-	40	-	60	%

**Note**

1. Resulted from comprehensive evaluation, not tested in production.

5.3.9 Flash Memory Characteristics

Table 5-17 Flash Memory Characteristics

Symbol	Parameters	Conditions		Min	Typ	Max	Unit
EC _{FLASH}	Program, Sector Erase times	T _A =-40℃ -105℃	Data Storage Period (RET _{FLASH}): 20 years, T _A =85℃	-	20000	-	time s
T _{b_prog}	Programming time (bytes)	-		22	-	30	μs
T _{w_prog}	Programming time (words)	-		40	-	52	μs
T _{p_erase}	Page erase time	-		2	-	3	ms
T _{m_erase}	Full chip erase time	-		30	-	40	ms

5.3.10 EMC Characteristics

5.3.10.1 EFT Characteristics

A chip reset can restore the system to normal operation.

Table 5-18 EFT Characteristics

Symbol	Level/Type
EFT to IO (IEC61000-4-4)	Class:4A
EFT to Power (IEC61000-4-4)	Class:4A

Design Reliable Software to Mitigate Noise-Related Issues

EMC evaluation and optimization at the device level is conducted in typical application environments (this testing was performed through sampling during comprehensive assessments using official evaluation boards). It should be noted that good EMC performance is closely related to user applications and specific software implementations.

Therefore, it is recommended that users implement EMC optimization in their software and conduct relevant EMC certification testing.

Software Recommendations

The software process must include control to deal with program runaway, such as:

- Corrupted program counter
- Unexpected reset
- Critical data is destroyed (control registers, etc.)

During the EFT test, interference that exceeds the application requirements can be directly applied to the chip power supply or IO. When an unexpected action is detected, the software part is strengthened to prevent unrecoverable errors.

5.3.10.2 ESD Characteristics

Using specific measurement methods, the chip is subjected to strength testing to determine its electrical sensitivity performance.

Table 5-19 ESD Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$VESD_{HBM}^{(1)}$	ESD @ Human Body Mode	$T_A=25^{\circ}C$, in line with ANSI/ESDA/JEDEC JS-001	-4	-	4	kV
$VESD_{CDM}^{(1)}$	ESD @ Charge Device Mode	$T_A=25^{\circ}C$, in line with ANSI/ESDA/JEDEC JS-002	-2	-	2	kV
$I_{latchup}^{(1)}$	Latch up current	$T_A=105^{\circ}C$, in line with JEDEC78	-400	-	400	mA

**Note**

1. Resulted from comprehensive evaluation, not tested in production.

5.3.11 I/O Port Characteristics

5.3.11.1 Output Characteristics-Port

Table 5-20 Port Output Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Max	Unit
V_{OH}	IO pin output high level	$I_{IO}=6mA$, $VCC=3.3V$	$VCC-0.3$	-	V
		$I_{IO}=12mA$, $VCC=3.3V$	$VCC-0.7$	-	V
V_{OL}	IO pin output low level	$I_{IO}=8mA$, $VCC=3.3V$	-	$VSS+0.3$	V
		$I_{IO}=16mA$, $VCC=3.3V$	-	$VSS+0.7$	V

**Note**

1. Resulted from comprehensive evaluation, not tested in production.
2. The device's I_{IO} current must always comply with the absolute maximum ratings specified in the [Table 5-1 : Voltage and Current Characteristics](#), and the sum of I_{IO} (I_{OH} and I_{OL} of I/O ports) must not exceed I_{VCC} .

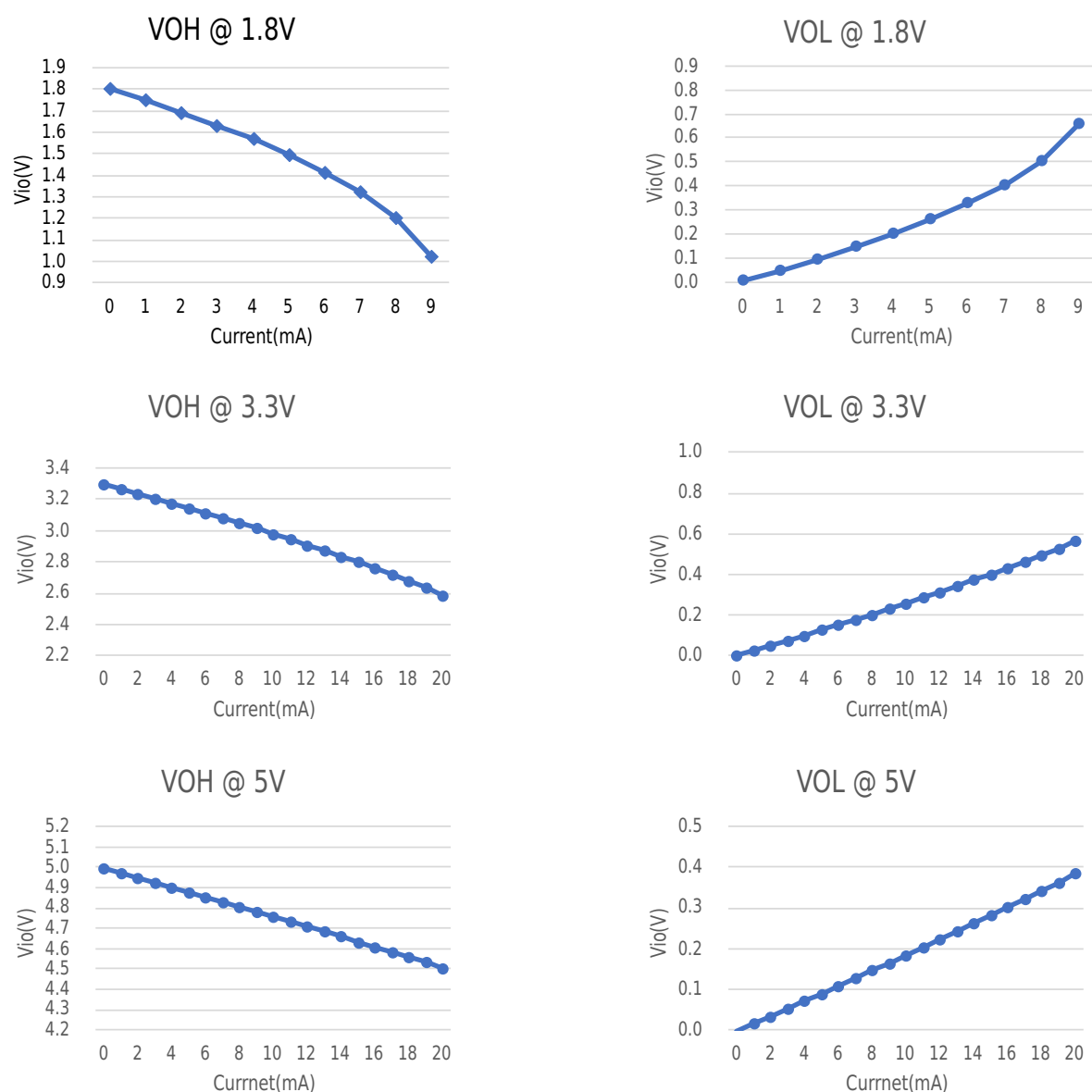


Figure 5-4 Output Port VOH/VOL Measured Curve (Typical Value)

5.3.11.2 Input Characteristics-PA/PB Port

Table 5-21 PA/PB Port Input Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{IH}^{(1)}$	Input high-level voltage	VCC=1.8V	0.7VCC	-	-	V
		VCC=3.3V	0.7VCC	-	-	V
		VCC=5.5V	0.7VCC	-	-	V
$V_{IL}^{(1)}$	Input low-level voltage	VCC=1.8V	-	-	0.3VCC	V
		VCC=3.3V	-	-	0.3VCC	V
		VCC=5.5V	-	-	0.3VCC	V

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{hys}	Input voltage hysteresis($V_{\text{IH}}-V_{\text{IL}}$)	$V_{\text{CC}}=1.8\text{V}$	-	0.3	-	V
		$V_{\text{CC}}=3.3\text{V}$	-	0.4	-	V
		$V_{\text{CC}}=5.5\text{V}$	-	0.6	-	V
R_{pullhigh}	Weak pull-up equivalent resistance	Weak pull-up enable $V_{\text{CC}}=3.3\text{V}$	-	60	-	k Ω
C_{input}	Input equivalent capacitance	-	-	5	-	pF

**Note**

1. Resulted from comprehensive evaluation, not tested in production.

Table 5-22 PA02/PA11 Input Level Low Voltage Recognition Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high-level voltage ⁽²⁾	-	0.7V _{CC}	-	-	V
V_{IL}	Input low-level voltage ⁽²⁾	-	-	-	0.3V _{CC}	V

**Note**

1. Guaranteed by design, not tested in production.
2. This level recognition feature is exclusively used for I2C communication and is unrelated to the input characteristics of GPIO ports.

5.3.11.3 Port Leakage Characteristics- PA/PB Port

Table 5-23 PA/PB Port Leakage Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$I_{\text{lk}}(\text{Px.y})$	Leakage current	$V_{(\text{Px.y})}^{(1)(2)}$	-	± 50	-	nA

**Note**

1. The port leakage is based on the corresponding port being connected to VSS or VCC.
2. The port must be configured as an input port.

5.3.12 RESETB Pin Characteristics

The RESETB pin input driver uses CMOS technology, which is connected with a pull-up resistor that cannot be disconnected.

Table 5-24 RESETB Pin Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{\text{IL}}(\text{RESETB})^{(1)}$	Input low-level voltage	-	-0.3	-	0.3V _{CC}	V
$V_{\text{IH}}(\text{RESETB})^{(1)}$	Input high-level voltage	-	0.7V _{CC}	-	V _{CC} +0.3	V
$V_{\text{hys}}(\text{RESETB})$	Schmitt trigger voltage hysteresis	-	-	400	-	mV

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistance	$V_{IN}=V_{SS}$	-	60	-	$k\Omega$
$T_{F(RESETB)}^{(1)}$	Filtered input pulse	-	-	-	1	μs
$T_{NF(RESETB)}^{(1)}$	Non-filtered input pulse	-	5	-	-	μs

**Note**

1. Guaranteed by design, not tested in production.

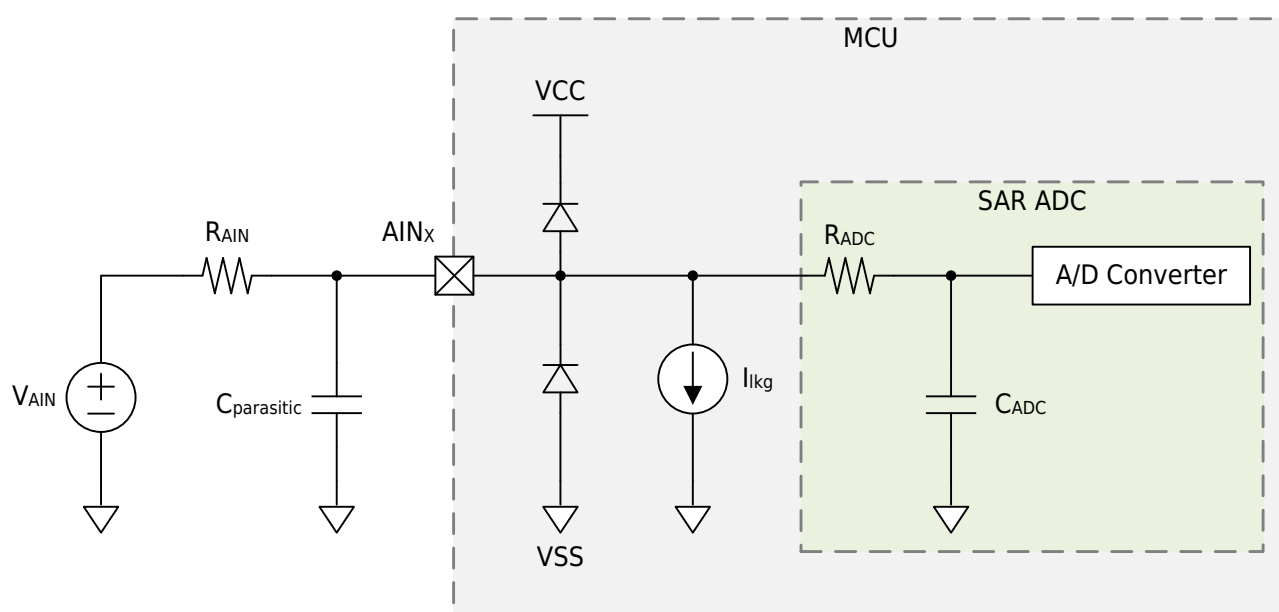
5.3.13 ADC Characteristics

Table 5-25 ADC Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
AVCC	Analog supply voltage	-	1.8	3.3	5.5	V
V_{AIN}	ADC input voltage range	Single-ended input mode	0	-	V_{REF+}	V
$V_{REF+}^{(1)}$	Positive reference voltage	-	1.5	-	AVCC	V
V_{REF-}	Negative reference voltage	-	-	AVSS	-	V
$DEV_{AVCC/3}^{(2)}$	AVCC/3 accuracy	-	-3	± 2	3	%
$I_{ADC}^{(1)}$	Operating current consumption	$f_s=1\text{Msps}$ $T_s=4/f_{ADCCLK}$	-	0.31	-	mA
$C_{ADC}^{(1)}$	ADC internal sampling capacitor	-	-	5	-	pF
$R_{ADC}^{(1)}$	ADC internal sampling resistor	-	-	1.5	-	$k\Omega$
$R_{AIN}^{(1)(4)}$	ADC external input impedance	-	-	-	1.5	$k\Omega$
$f_{ADCCLK}^{(1)}$	ADC clock frequency	$2.7V \leq AVCC \leq 5.5V$	0.3	-	24	MHz
		$2.4V \leq AVCC < 2.7V$	0.3	-	8	
		$1.8V \leq AVCC < 2.4V$	0.3	-	4	
$f_s^{(1)}$	Sampling rate	$2.7V \leq AVCC \leq 5.5V$	0.02	-	1	Msps
		$2.4V \leq AVCC < 2.7V$	0.02	-	0.5	
		$1.8V \leq AVCC < 2.4V$	0.02	-	0.25	
$T_{ADCSTART}$	Start time	-	-	-	10	μs
$T_s^{(3)}$	Sample time	-	2	4	127	$1/f_{ADCCLK}$
$T_{ADCCONV}$	Total conversion time (Including sampling time)	-	-	T_s+12	-	μs
$ENOB^{(2)}$	Effective bits	$2.7V \leq AVCC \leq 5.5V$	9.8	10.4	-	bits
$SNR^{(2)}$	signal to noise ratio	$f_s=1\text{Msps}$	60.0	64.8	-	dB

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
THD ⁽²⁾	Total Harmonic Distortion		-	-78.7	-71.5	dB
E _D ⁽²⁾	Differential non-linearity error		-1.0	-0.9/1.9	2.0	LSB
E _L ⁽²⁾	Integral non-linearity error		-4.0	-2.9/1.8	4.0	LSB
E _O ⁽²⁾	Offset Error		-	-1.0/10.1	-	LSB
E _G ⁽²⁾	Gain error		-	-1.7/3.0	-	LSB
E _T ⁽²⁾	Total unadjustable error		-	±11.0	-	LSB

1. Guaranteed by design, not tested in production.
2. Resulted from comprehensive evaluation, not tested in production.
3. The typical application of ADC is shown in the figure below:



In the diagram, I_{lkg} represents the I/O port leakage current. Refer to "[Port Leakage Characteristics-PA/PB Port](#)" for detailed parameters.

Under the condition of 0.5LSB sampling error accuracy requirement, the calculation formula of sampling time is as follows:

$$T_S = \frac{M}{f_{ADCLK}} \geq (R_{AIN} + R_{ADC}) \times C_{ADC} \times (N + 1) \times \ln(2)$$

Where N is the ADC resolution (12 bits), f_{ADCLK} is the ADC clock frequency (f_{PCLK} divided by the prescaler set in register ADC_CR0.CLKDIV), and M is the number of sampling cycles (sampling time occupies M ADC clock cycles, see register ADC_CR0.SAM for specific values).

The table below shows the relationship between ADC minimum sampling time T_S and external resistor R_{AIN} under typical operating conditions ($M=4$, with 0.5LSB sampling error). For other special external input impedance values, the corresponding minimum sampling time requirements can also be calculated through the sampling time calculation formula given above.

Table 5-26 Relationship Between ADC Minimum Sampling Time and External Resistance R_{AIN}

$R_{AIN} (\Omega)$	Minimum Sampling Time T_s (ns)
10	68.0
47	69.7
68	70.6
100	72.1
150	74.3
220	77.5
330	82.4
470	88.8
680	98.2
1000	112.6
1500	135.2
2200	166.7
3300	216.3
4700	279.3
6800	374.0
10000	518.1
15000	743.4

For the above typical applications, you should pay attention to:

- Minimize parasitic capacitance $C_{parasitic}$ at the ADC input port AIN_x , to make sure $C_{parasitic} \ll (1 + R_{ADC}/R_{AIN}) * C_{ADC}$. Otherwise, it may result in insufficient settling of the ADC input voltage and introduce conversion errors.
 - In addition to consider R_{AIN} value, if the internal resistance of signal source V_{AIN} is large, it also needs to be considered.
4. Based on evaluation at $T_j = 125^\circ\text{C}$, the error caused by leakage current must not exceed ± 2 LSB. This limit may be relaxed for lower temperatures. In practical applications, determining the maximum allowable external input impedance requires joint consideration of leakage current and sampling time (refer to the description above).

5.3.14 VC Characteristics

Table 5-27 VC Characteristics

Symbol	Parameters	Conditions		Min	Typ	Max	Unit
V _{in}	Input voltage range	-		0	-	5.5	V
V _{com}	Input common mode range	-		0.2	-	VCC-0.2	V
V _{offset}	Input offset	AVCC=3.3 V, T _A =25°C	BIAS=0b00	-	±15	-	mV
			BIAS=0b01	-	±15	-	mV
			BIAS=0b10	-	±10	-	mV

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{offset}	Input offset	BIAS=0b11	-	±5	-	mV
		AVCC=1.8-5.5V, T_A =-40-105°C	BIAS=0b00	±20	-	mV
			BIAS=0b01	±20	-	mV
			BIAS=0b10	±15	-	mV
			BIAS=0b11	±10	-	mV
I_{comp}	Comparator's current	VCx_CR0.BIAS=0b00 VCx_CR0.BIAS=0b01 VCx_CR0.BIAS=0b10 VCx_CR0.BIAS=0b11	-	0.3 1.2 10 20	-	μA
T_{response}	Comparator's response time when one input cross another	VCx_CR0.BIAS=0b00 VCx_CR0.BIAS=0b01 VCx_CR0.BIAS=0b10 VCx_CR0.BIAS=0b11	-	2500 1000 400 200	-	ns
T_{setup}	Comparator's setup time when ENABLE. Input signals unchanged.	VCx_CR0.BIAS=0b00 VCx_CR0.BIAS=0b01 VCx_CR0.BIAS=0b10 VCx_CR0.BIAS=0b11	-	10 2.5 0.7 0.35	-	μs
$V_{\text{hysteresis}}$	Comparator's hysteresis voltage	VCx_CR0.HYS=0b00 VCx_CR0.HYS=0b01 VCx_CR0.HYS=0b10 VCx_CR0.HYS=0b11	-	0 10 20 30	-	mV
$R_{\text{in}}^{(1)}$	allowable source resistance of the input signal	-	-	-	100	kΩ
$V_{\text{error_DAC}}$	Voltage error of DAC in VC	-	-	±25	-	mV
$T_{\text{setup_DAC}}$	Setup time of DAC in VC	-	-	25	-	μs
T_{filter}	Digital filter time	VCx_CR1.FLTTIME=0b000	-	0	-	μs
		VCx_CR1.FLTTIME=0b001	-	2* T_{VCx}	-	μs
		VCx_CR1.FLTTIME=0b010	-	4* T_{VCx}	-	μs
		VCx_CR1.FLTTIME=0b011	-	8* T_{VCx}	-	μs
		VCx_CR1.FLTTIME=0b100	-	16* T_{VCx}	-	μs
		VCx_CR1.FLTTIME=0b101	-	32* T_{VCx}	-	μs
		VCx_CR1.FLTTIME=0b110	-	64* T_{VCx}	-	μs
		VCx_CR1.FLTTIME=0b111	-	128* T_{VCx}	-	μs
		VCx_CR1.FLTTIME=0b1000	-	256* T_{VCx}	-	μs

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
T_{filter}	Digital filter time	VCx_CR1.FLTTIME=0b1001	-	$512 * T_{\text{VCx}}$	-	μs
		VCx_CR1.FLTTIME=0b1010	-	$1024 * T_{\text{VCx}}$	-	μs
		VCx_CR1.FLTTIME=0b1011	-	$2048 * T_{\text{VCx}}$	-	μs
		VCx_CR1.FLTTIME=0b1100	-	$4096 * T_{\text{VCx}}$	-	μs
		VCx_CR1.FLTTIME=0b1101	-	$4096 * T_{\text{VCx}}$	-	μs
		VCx_CR1.FLTTIME=0b1110	-	$4096 * T_{\text{VCx}}$	-	μs
		VCx_CR1.FLTTIME=0b1111	-	$4096 * T_{\text{VCx}}$	-	μs

**Note**

1. Guaranteed by design, not tested in production.
2. T_{VCx} represents the filter clock period, with VCx_CR1.FLTCLK selecting either the built-in RC oscillator (about 256kHz) or PCLK as the filter clock.

5.3.15 Timer Characteristics

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), see the table below.

Table 5-28 Advanced Timer (ATIM3) Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	-	1	-	t_{TIMCLK}
		$f_{\text{TIMCLK}}=48\text{MHz}$	20.8	-	ns
f_{ext}	External clock frequency	$f_{\text{TIMCLK}}=48\text{MHz}$	0	24	MHz
Res_{Tim}	Timer resolution		-	16	Bit
T_{counter}	When the internal clock is selected, the 16-bit counter clock cycle	-	1	65536	t_{TIMCLK}
		$f_{\text{TIMCLK}}=48\text{MHz}$	20.8	1365000	ns

**Note**

1. Guaranteed by design, not tested in production.

Table 5-29 Composite Timer (CTIM) Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	-	1	-	t_{TIMCLK}
		$f_{\text{TIMCLK}}=48\text{MHz}$	20.8	-	ns
f_{ext}	External clock frequency	$f_{\text{TIMCLK}}=48\text{MHz}$	0	24	MHz
Res_{Tim}	Timer resolution	-	-	16	Bit

Symbol	Parameters	Conditions	Min	Max	Unit
T_{counter}	When the internal clock is selected, the 16-bit counter	-	1	65536	t_{TIMCLK}
		$f_{\text{TIMCLK}}=48\text{MHz}$	20.8	1365000	ns

**Note**

1. Guaranteed by design, not tested in production.

Table 5-30 IWDTC Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Max	Unit
t_{res}	IWDTC overflow time	$f_{\text{WDTCCLK}}=10\text{kHz}$	0.4	209715.2	ms

**Note**

1. Guaranteed by design, not tested in production.

5.3.16 Communication Interface

5.3.16.1 I2C Characteristics

I2C interface features are as follows:

Table 5-31 I2C Interface Characteristics⁽¹⁾

Symbol	Parameters	Standard Mode (100k)		Fast Mode (400k)		Fast enhanced Mode (1M)		Unit
		Min	Max	Min	Max	Min	Max	
t_{LOW}	SCL clock low time	4.7	-	1.25	-	0.5	-	μs
t_{HIGH}	SCL clock high time	4.0	-	0.6	-	0.26	-	μs
$t_{\text{SU.DAT}}$	Data setup time	250	-	100	-	50	-	ns
$t_{\text{HD.DAT}}$	Data hold time	0	-	0	-	0	-	μs
$t_{\text{HD.STA}}$	(Repeated) START condition hold time	2.5	-	0.625	-	0.25	-	μs
$t_{\text{SU.STA}}$	Repeated START condition setup time	2.5	-	0.6	-	0.25	-	μs
$t_{\text{SU.STO}}$	STOP condition setup time	0.25	-	0.25	-	0.25	-	μs
t_{BUF}	Bus Idle (STOP condition to START condition)	4.7	-	1.3	-	0.5	-	μs

**Note**

1. Guaranteed by design, not tested in production.

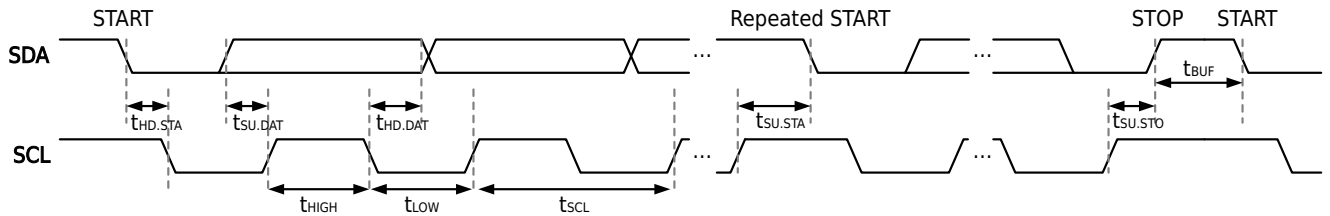


Figure 5-6 I2C Interface Timing

5.3.16.2 SPI Characteristics

Table 5-32 SPI Interface Characteristics⁽¹⁾⁽²⁾

Symbol	Parameters	Conditions	Min	Max	Unit
$t_{c(SCK)}$	Serial clock period ⁽³⁾	Master transmit mode $f_{PCLK}=48MHz$	41.6	-	ns
		Master receiving mode (Master delayed sam- pling disabled) $f_{PCLK}=48MHz$	166	-	ns
		Master receiving mode (Master delayed sam- pling enabled) $f_{PCLK}=48MHz$	83.3	-	ns
		Slave transmit mode (Master delayed sam- pling disabled) $f_{PCLK}=48MHz$	166	-	ns
		Slave transmit mode (Master delayed sam- pling enabled) $f_{PCLK}=48MHz$	83.3	-	ns
		Slave receiving mode $f_{PCLK}=48MHz$	83.3	-	ns
$t_{w(SCKH)}$	High level time of seri- al clock	Master mode	$0.45 \times t_{c(SCK)}$	-	ns
		Slave mode	$0.45 \times t_{c(SCK)}$	-	ns
$t_{w(SCKL)}$	Low level time of serial clock	Master mode	$0.45 \times t_{c(SCK)}$	-	ns
		Slave mode	$0.45 \times t_{c(SCK)}$	-	ns
$t_{su(SSN)}$	Setup time selected by slave	Slave Mode	$0.45 \times t_{c(SCK)}$	-	ns
$t_{h(SSN)}$	Hold time selected by slave	Slave Mode	$0.45 \times t_{c(SCK)}$	-	ns
$t_{v(MO)}$	Effective time of mas- ter data output	-	-	3	ns
$t_{h(MO)}$	Hold time of master data output	-	0	-	ns
$t_{v(SO)}$	Effective time of slave data output	-	-	$20 + 1.5 \times T_{PCLK}$	ns

Symbol	Parameters	Conditions	Min	Max	Unit
$t_{h(SO)}$	Hold time of slave data output	-	$14+0.5 \times T_{PCLK}$	-	ns
$t_{su(MI)}$	Setup time of master data input	-	20	-	ns
$t_{h(MI)}$	Hold time of master data input	-	2	-	ns
$t_{su(SI)}$	Setup time of slave data input	-	0	-	ns
$t_{h(SI)}$	Hold time of slave data input	-	$2+1.5 \times T_{PCLK}$	-	ns

**Note**

1. Guaranteed by design, not tested in production.
2. The data is provided under the condition of $V_{CC}=3.0V$.
3. The maximum frequency division factor of the master mode is $PCLK/2$, and the The maximum frequency division factor of slave mode is $PCLK/4$.

The waveform and timing parameters of the SPI interface signal are as follows:

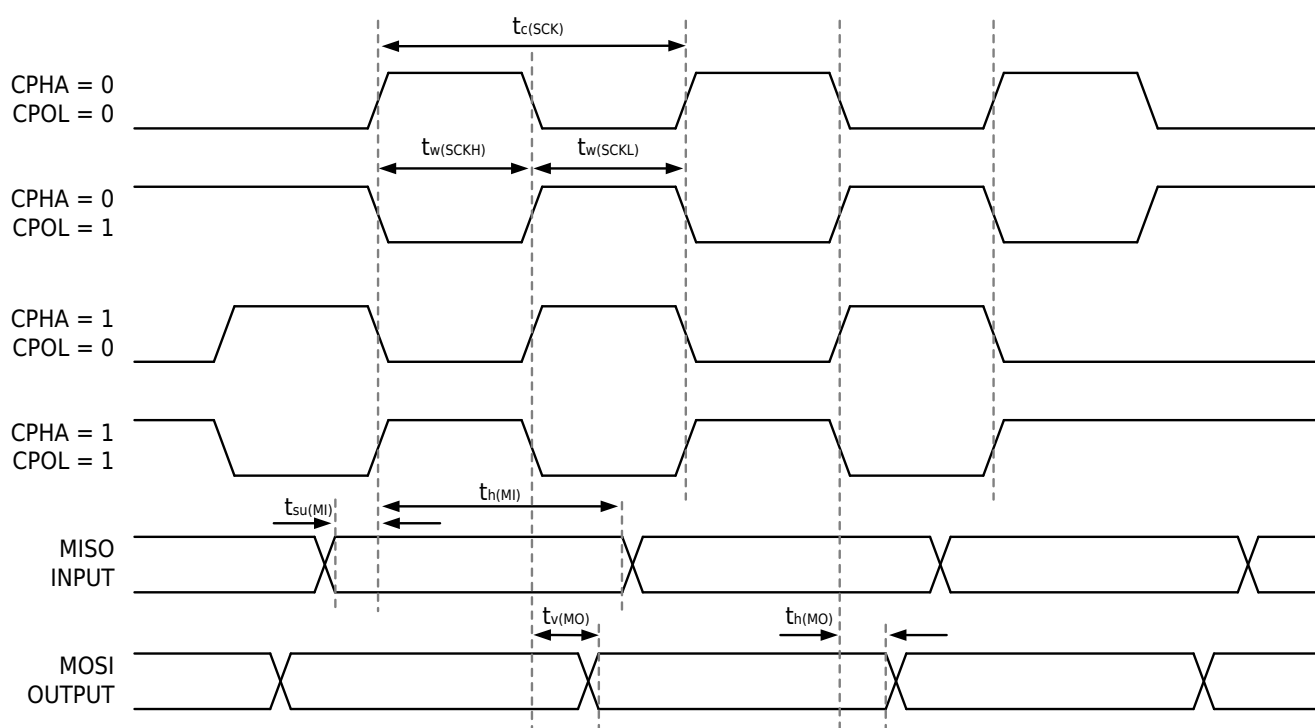


Figure 5-7 SPI Timing Diagram (Master Mode)

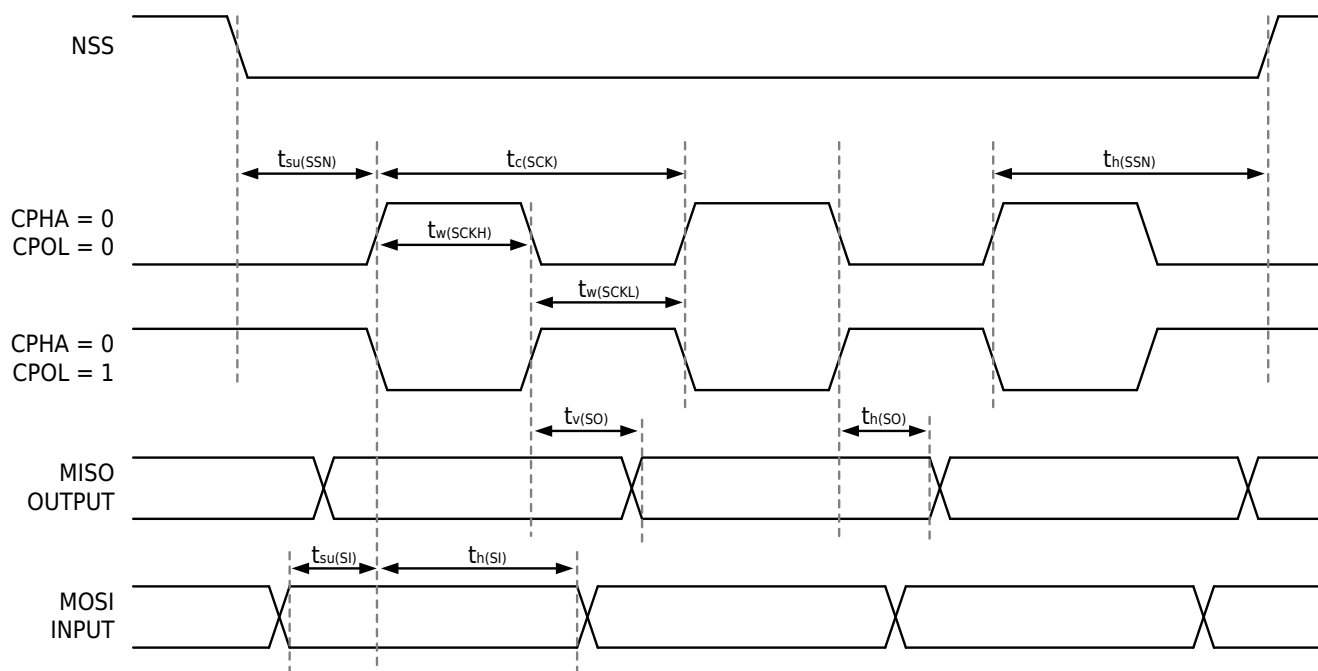


Figure 5-8 SPI Timing Diagram (Slave Mode CPHA=0)

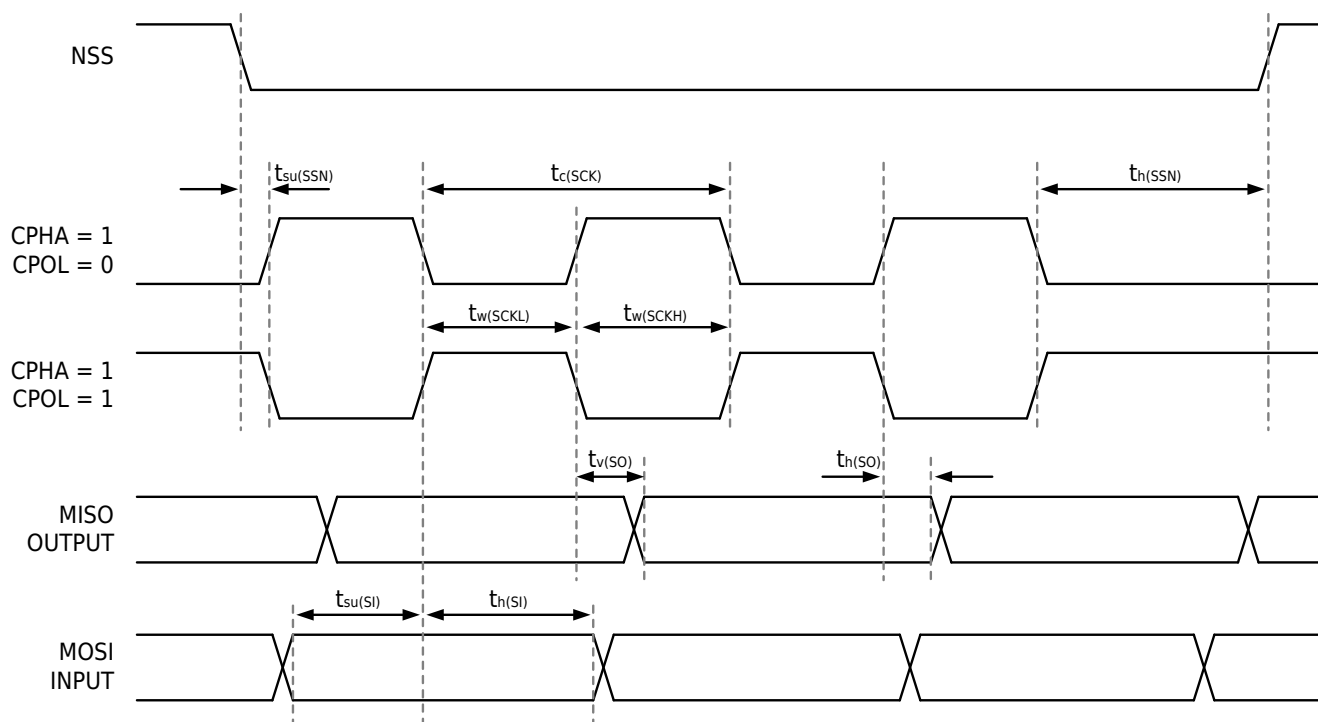
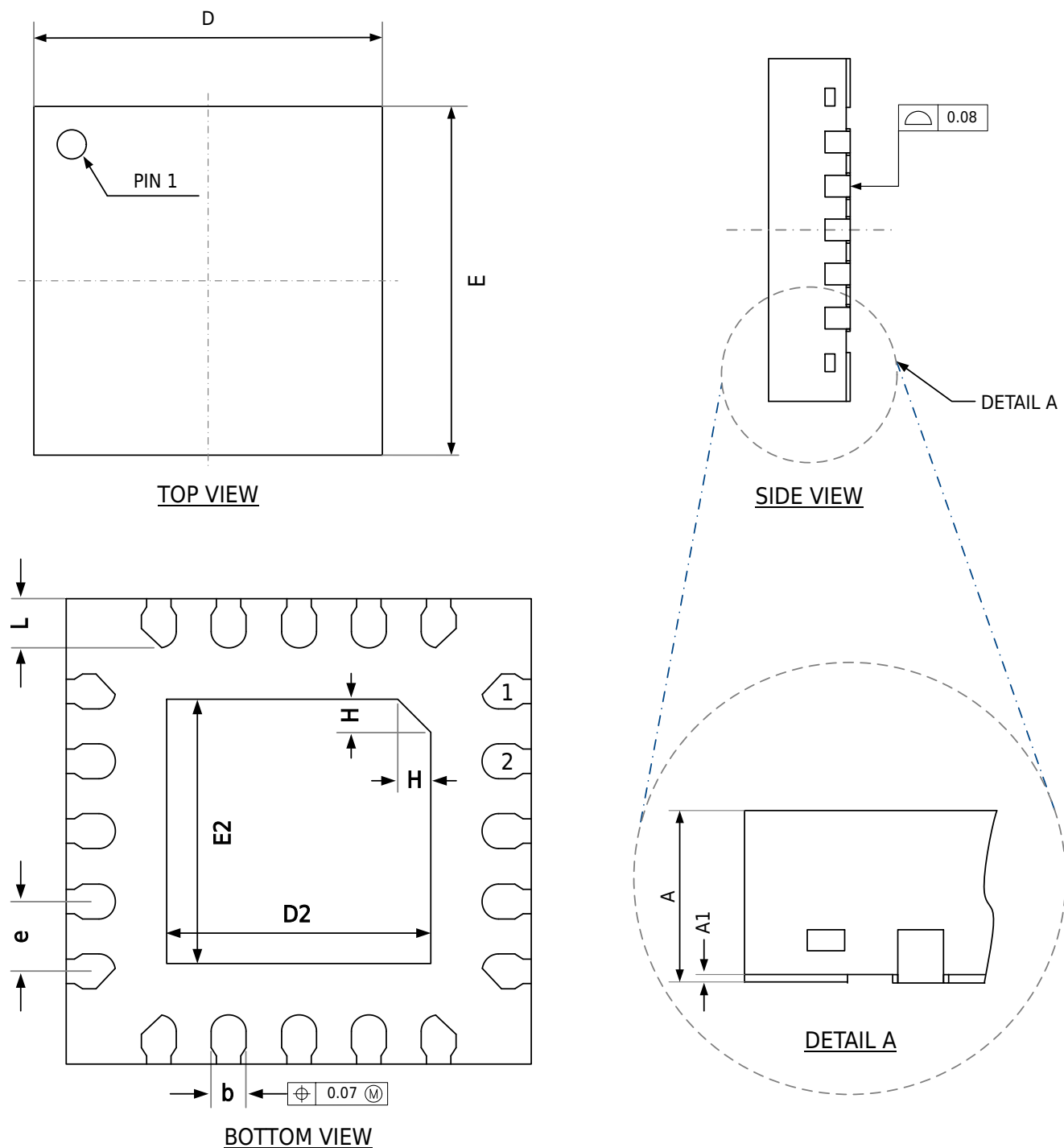


Figure 5-9 SPI Timing Diagram (Slave Mode CPHA=1)

6 Package Specifications

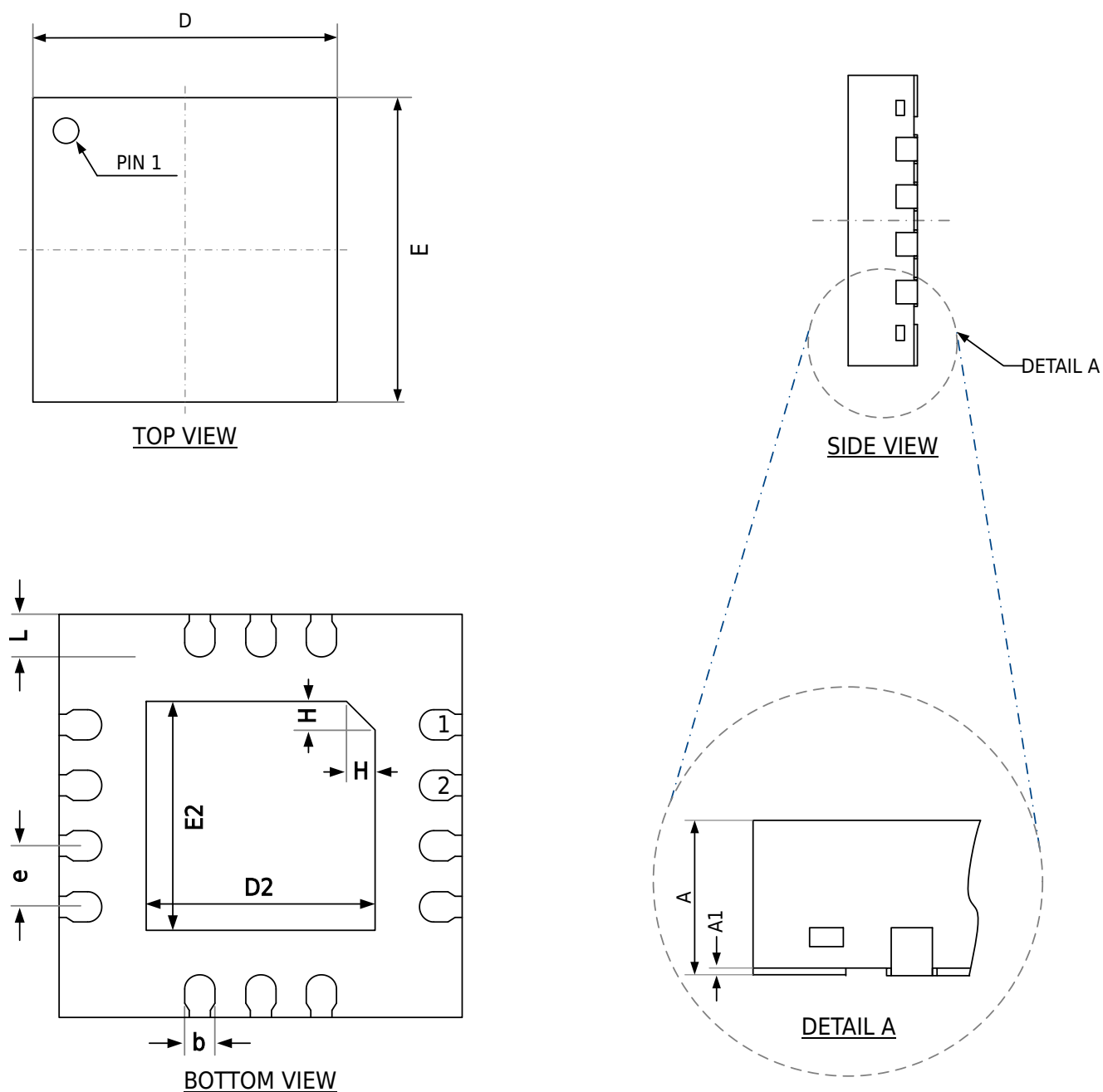
6.1 Package Dimensions

6.1.1 QFN20 Package



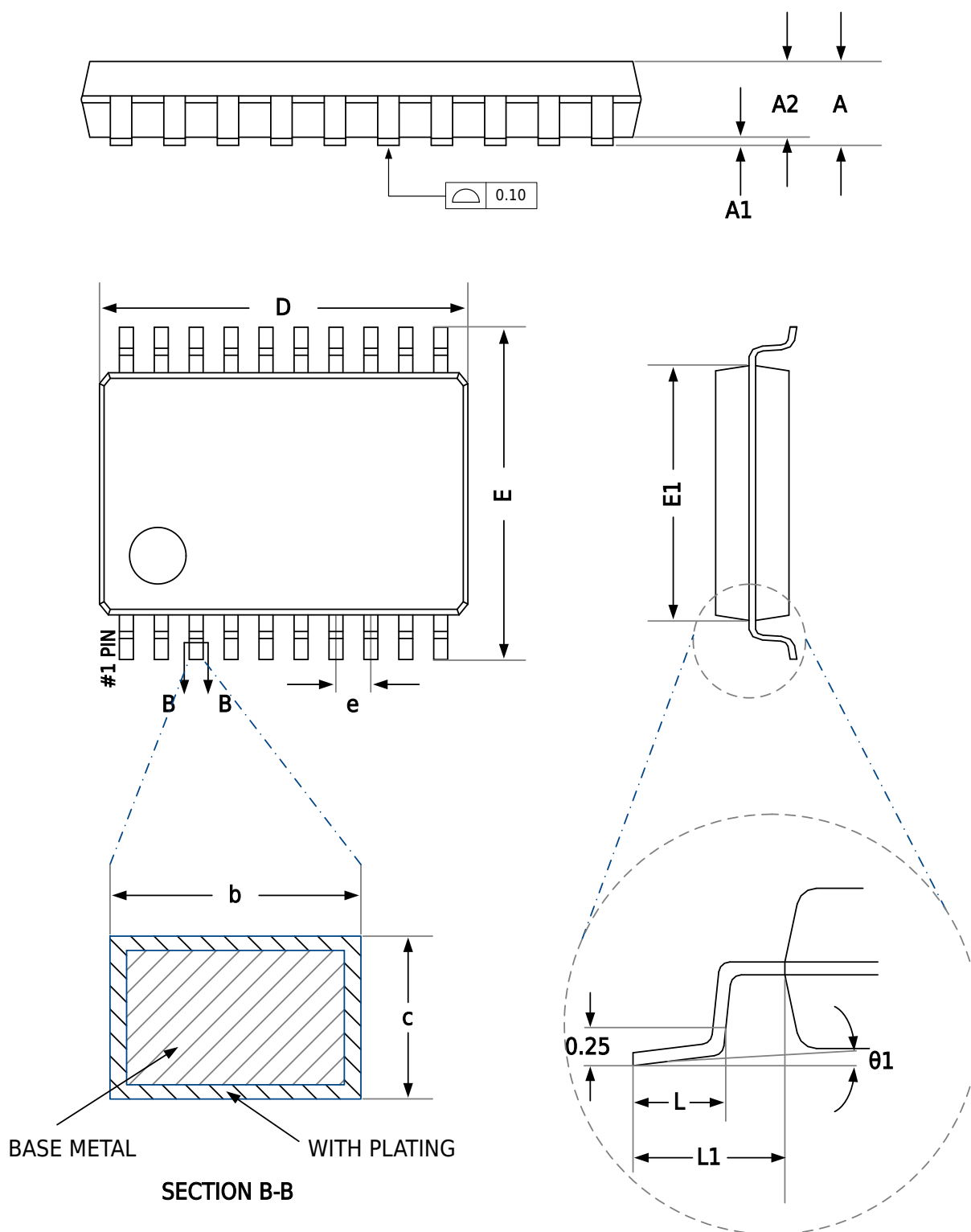
Symbol	3*3 Millimeter		
	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
D	2.90	3.00	3.10
D2	1.60	1.70	1.80
E	2.90	3.00	3.10
E2	1.60	1.70	1.80
e	0.40BSC		
L	0.25	--	0.40
H	0.25REF		

6.1.2 QFN14 Package



Symbol	2*2 Millimeter		
	Min	Nom	Max
A	0.40	0.45	0.50
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
D	1.95	2.00	2.05
D2	1.15	1.20	1.25
E	1.95	2.00	2.05
E2	1.15	1.20	1.25
e	0.35BSC		
L	0.15	0.20	0.25
H	0.20REF		

6.1.3 TSSOP20 Package



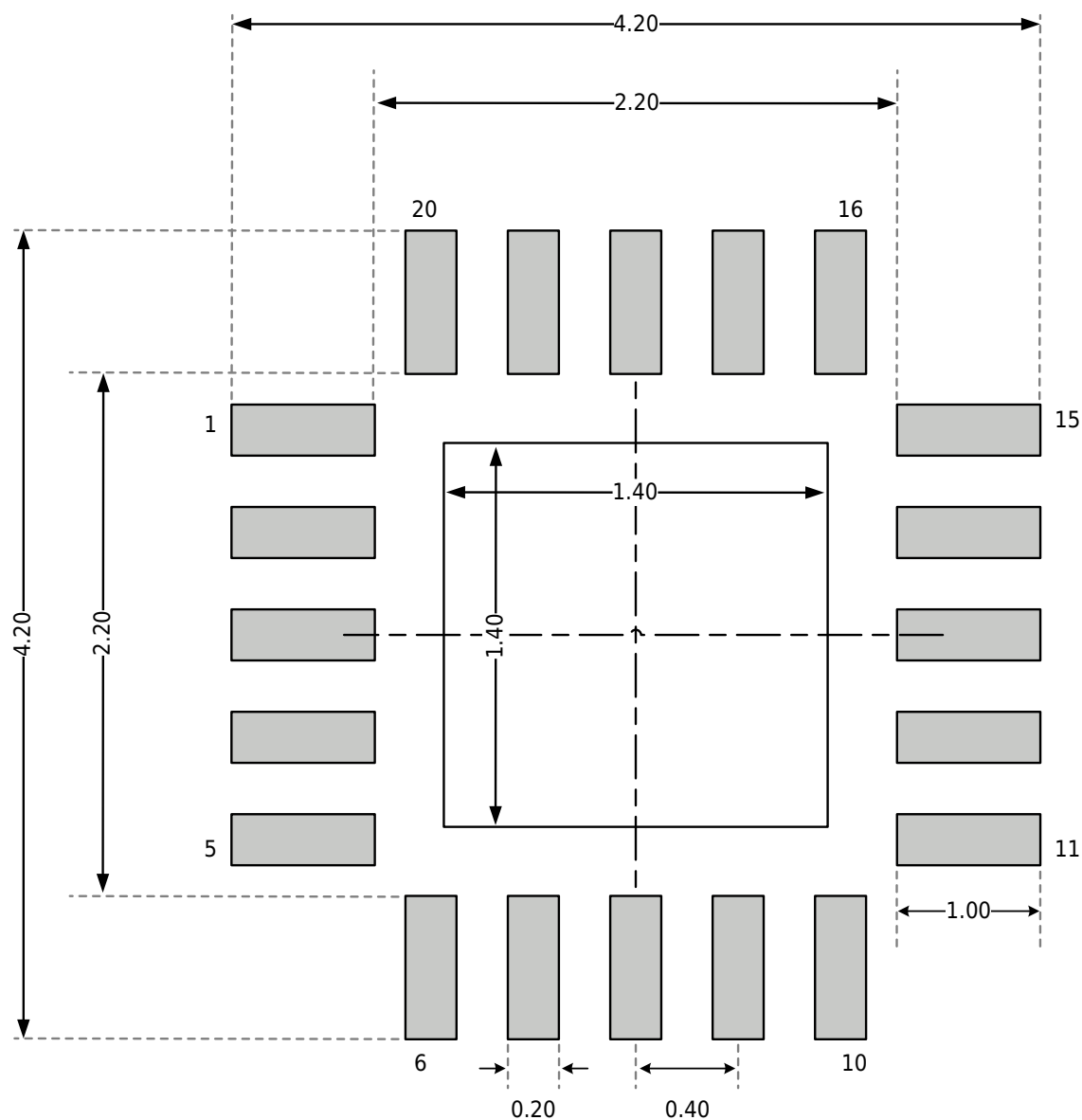
Symbol	Millimeter		
	Min	Nom	Max
A	--	--	1.20
A1	0.05	--	0.15
A2	0.90	1.00	1.05
b	0.20	--	0.28
c	0.10	--	0.19
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ1	0°	--	8°

**Note**

Dimensions "D1" and "E1" do not include mold flash.

6.2 PCB Land Pattern

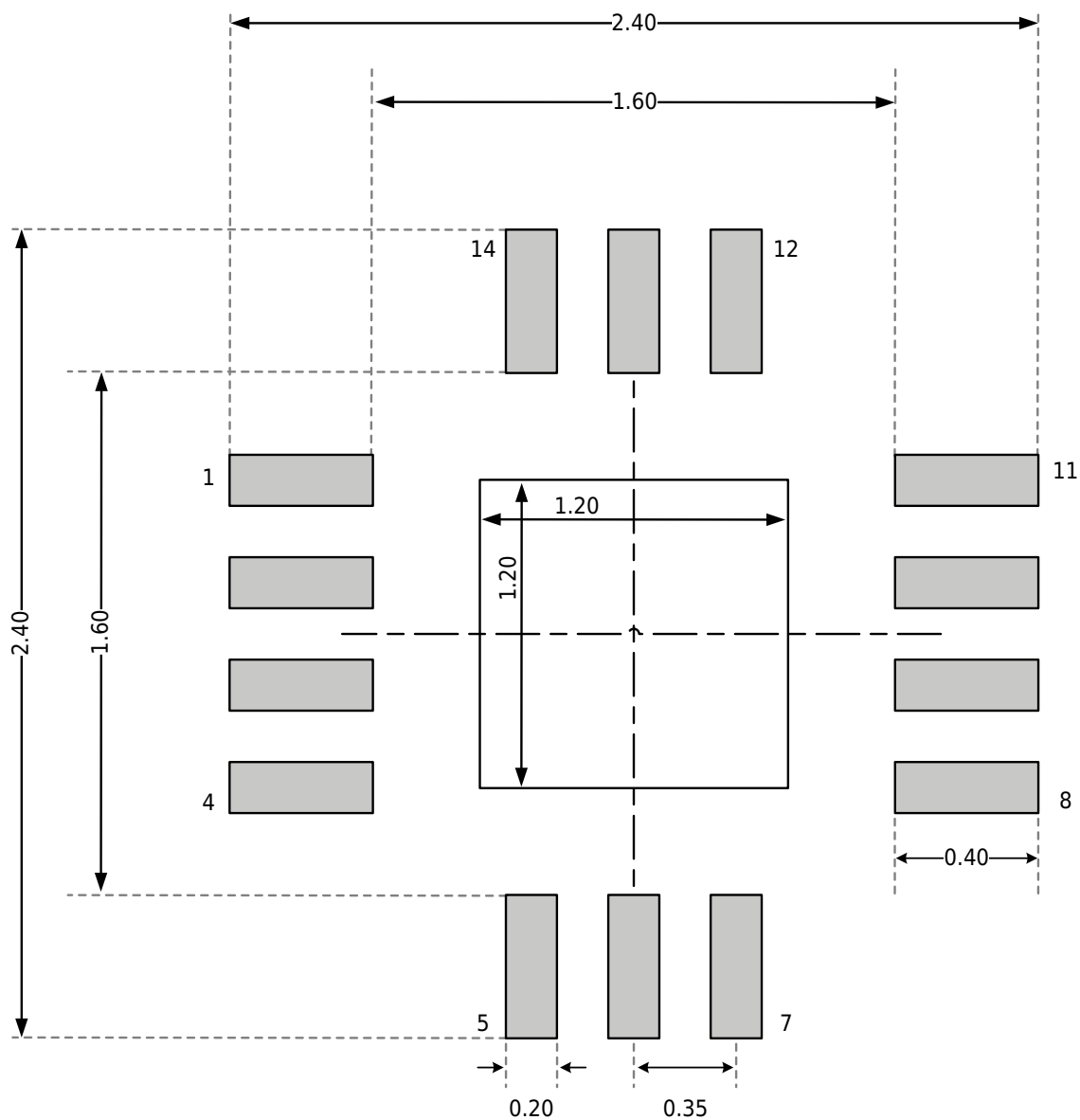
6.2.1 QFN20 Package (3mm*3mm)



Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

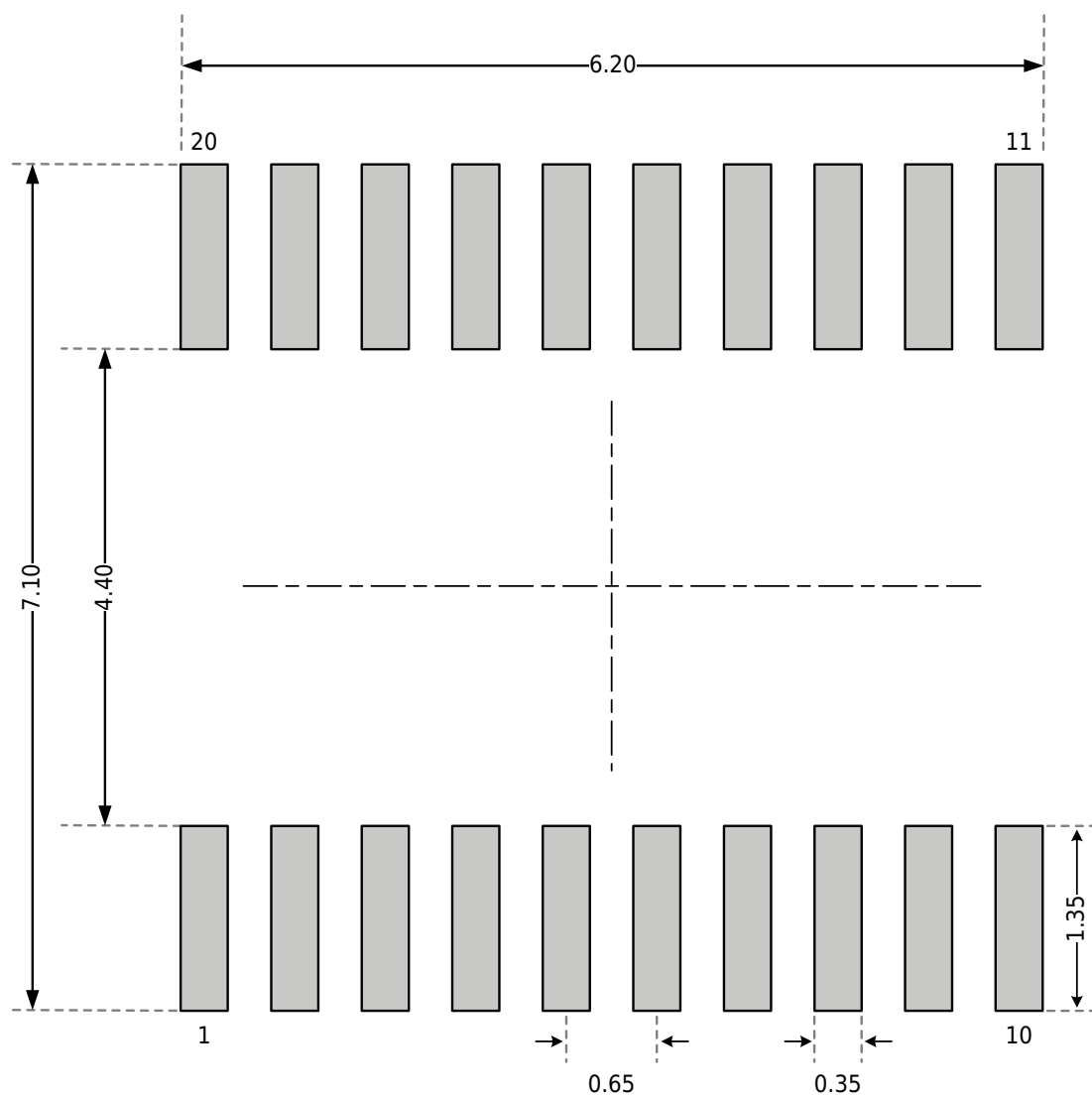
6.2.2 QFN14 Package (2mm*2mm)



Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

6.2.3 TSSOP20 Package

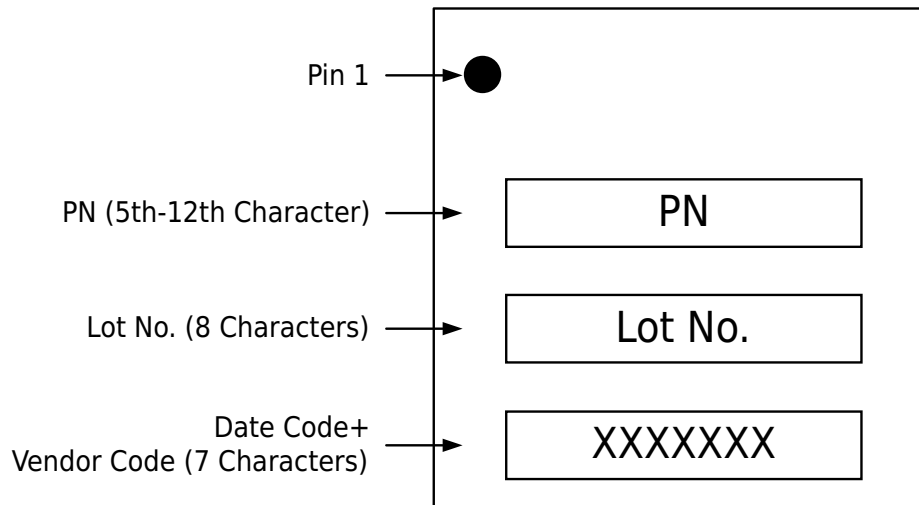
**Note**

- Dimensions are in millimeters.
- Dimensions are for reference only.

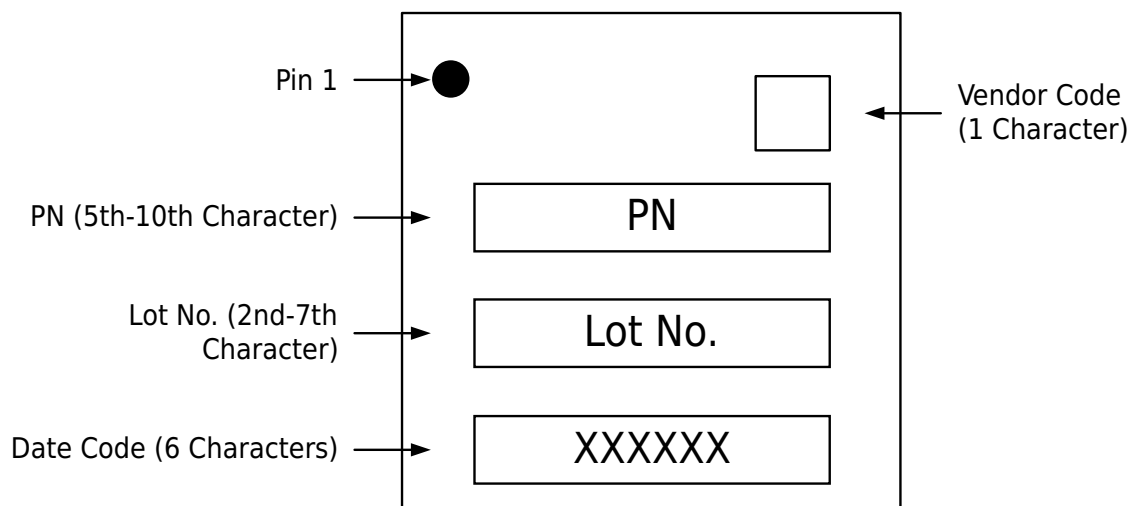
6.3 Package Marking

The location and information description of Pin1 on the front of each package are given below.

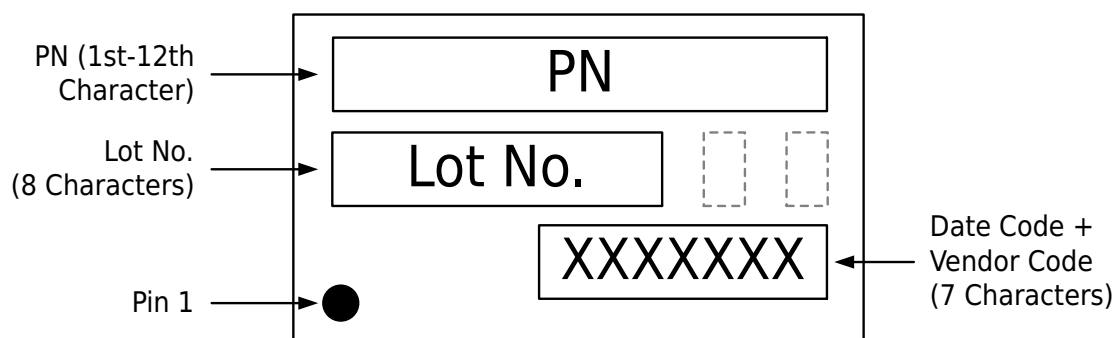
QFN20 package (3mm*3mm)



QFN14 Package (2mm*2mm)



TSSOP20 package



Note

The blank boxes in the above figure indicate optional marks related to production, which are not explained in this section.

6.4 Packaging Thermal Resistance Coefficient

When the packaged chip is working at the specified working environment temperature, the junction temperature T_j (°C) of the chip surface can be calculated according to the following formula:

$$T_j = T_A + (P_D * \theta_{JA})$$

- T_A refers to the working environment temperature when the packaged chip is working, the unit is °C;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is °C/W;
- P_D refers to total power dissipation, which is the sum of internal power consumption (P_{INT}) and I/O pin power consumption (P_{IO}), the unit is W.

$$P_D = P_{INT} + P_{IO}$$

► P_{INT} : Internal power consumption, calculated as the product of I_{VCC} and V_{CC} .

► P_{IO} : I/O pin power consumption, calculated as: $P_{IO} = \Sigma(V_{OL} * I_{OL}) + \Sigma((V_{CC} - V_{OH}) * I_{OH})$

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable junction temperature T_{jmax} of the chip.

Table 6-4 Thermal Resistance Coefficient Reference Table For Each Package

Package Type and Dimensions	Thermal Resistance Parameters (θ_{JA})	Unit
QFN20 3mm*3mm/0.4mm pitch	70±10%	°C/W
QFN14 2mm*2mm/0.35mm pitch	70±10%	°C/W
TSSOP20	91±10%	°C/W

7 Ordering Information

Part Number	HC32L021C8PB-TSSOP20	HC32L021C8PB-TSSOP20TR	HC32L021C8UB-ZFN20TR	HC32L021B8UB-XFN14TR
GPIO	16+1	16+1	16+1	9+1
Core	Cortex-M0+	Cortex-M0+	Cortex-M0+	Cortex-M0+
Frequency	48MHz	48MHz	48MHz	48MHz
Flash	64KB	64KB	64KB	64KB
RAM	6KB	6KB	6KB	6KB
Power Supply Voltages	1.8-5.5V	1.8-5.5V	1.8-5.5V	1.8-5.5V
Temp Range	-40-105°C	-40-105°C	-40-105°C	-40-105°C
Basic Timer	[6] ⁽¹⁾	[6] ⁽¹⁾	[6] ⁽¹⁾	[3] ⁽¹⁾
General Timer	2	2	2	1
Advanced Timer	1	1	1	1
LPTimer	1	1	1	1
RTC	1	1	1	1
IWDT	1	1	1	1
LPUART	2	2	2	2
HSI2C	1	1	1	1
SPI	1	1	1	1
12-bit ADC	1*8ch	1*8ch	1*8ch	1*7ch
Vcomp	2	2	2	2
LVD	√	√	√	√
TRNG	1	1	1	1
Package (mm*mm)	TSSOP20 (6.5*6.4)	TSSOP20 (6.5*6.4)	QFN20 (3*3)	QFN14 (2*2)
Pins	20	20	20	14
Packing	Tube	Tape & Reel	Tape & Reel	Tape & Reel
Pitch	0.65mm	0.65mm	0.4mm	0.35mm
Thickness	1.2mm	1.2mm	0.55mm	0.45mm



Note

1. This module is time-division multiplexed with the General Timer.

Please contact the sales window for the latest mass production information before ordering.

Revision History

Revision/Date	Changes
Rev1.20 Aug. 28, 2026	1. Typical Application Circuit Diagram: the decoupling capacitor description is optimized. 2. Electrical Specifications: In the "Absolute Maximum Ratings" chapter, the voltage and current tables is combined; In the "Supply Current Characteristics" chapter, the I_{DD} (Run mode) parameter data at 85°C condition is changed from "3100" to "2656"; In the "Flash Memory Characteristics" chapter, delete the 100K data incorrectly added in EC_{FLASH} parameter; 3. Package Specifications: In the "PCB Land Pattern" chapter, the redundant data is removed; the pad pin width of QFN14 is changed from "0.30" to "0.20".
Rev1.11 Feb. 12, 2026	1. Electrical Specifications: In the "Time to Wake-Up from Low-Power Mode" chapter, the typical wake-up time from low-power mode for 4MHz/6MHz deep sleep is revised from "15.0" to "20.0"; In the "RCL" chapter, a subscript 2 is added to the Dev parameter, and a new description regarding "selecting HPM or LPM mode through register configuration" is included; In the "RC10K" chapter, the parameter V is removed; In the "Flash Memory Characteristics" chapter, the data of EC_{FLASH} parameters have been optimized and updated based on new conditions; In the "I/O Port Characteristics" chapter, the subsection "Port External Input Sampling Requirements" is deleted; In the "I/O Port Characteristics - Input Characteristics" chapter, a new feature for low-voltage level recognition is added; In the "ADC Characteristics" chapter, the value of the f_s parameter is revised from "1.5" to "1"; In the "Timer Characteristics" chapter, the time units in the timer table are unified to "ns", and an additional line of time data is added to the $T_{counter}$ parameter in the CTIM characteristics table. 2. Package Specifications: In the "Package Dimensions" chapter, the A3, K of QFN package have been removed; In the "QFN20 Package" chapter, the max value of L is modified to "0.40", the value of H is modified to "0.25REF".
Rev1.10 Nov. 21, 2025	1. Product Overview: In the "Product Lineup" chapter, the ADC channel in model function comparison table is revised from "7ch+1" to "7ch+2". 2. Pin Definitions: Add P and N designations to the functional pins of VC. 3. Electrical Specifications: In the "Absolute Maximum Ratings" chapter, the symbol "T_j" representing temperature characteristics is revised to "T_{jmax}"; In the "Working Conditions at Power-On and Power-Down" chapter, the maximum values for the VCC rising rate have been changed from "5" to "1", the maximum values for the VCC falling rate have been changed from "5" to "0.05"; In the "Built-in Reset and LVD Module Characteristics" chapter, the V_{level} maximum and minimum values are optimized; In the "Supply Current Characteristics" chapter, current data for I_{DD}(LP Run), I_{DD}(LP Sleep), and I_{DD}(DeepSleep) is refreshed; In the "External Clock Source Characteristics-XTL" chapter, additional data has been added for the conditions of I_{dd} and g_m with the new criterion $XTL_CR[3:0]=0bxx0x$, and the recommended value has been changed from "$XTL_CR[3:0]=0b1010$" to "$XTL_CR[3:0]=0b1001$". The description of C_{Lx} is changed to "Matching ca-

Revision/Date	Changes
Rev1.10 Nov. 21, 2025	capitance", and change the minimum value to "4pF". Meanwhile, optimize the annotation description; In the "Internal Clock Source Characteristics" chapter, the "RC256K" section is added; In the "Internal Clock Source Characteristics - RC48M" chapter, data under the conditions of "VCC = 3.3V, TA = 25°C" are newly added for the Dev parameter, and the data under the condition of "FCLK = 4/6MHz" is revised from "± 2.0" to "± 1.5"; In the "Internal Clock Source Characteristics - RCL" chapter, the data of Dev parameter is revised from "TBD" to "-2.5" (Min) and "2.5"(Max), the Dev@LPM data is added; In the "ADC Characteristics" chapter, the minimum value "-3" and maximum value "3" are added for the $DEV_{AVCC/3}$ parameter, the superscript 3 of the R_{AIN} parameter is removed, and its maximum value is revised from "15" to "1.5", the maximum value of the f_{ADCCLK} parameter under the condition of "$2.7V \leq AVCC \leq 5.5V$" is revised from "16" to "24", the maximum value of the f_s parameter under the condition of "$2.7V \leq AVCC \leq 5.5V$" is revised from "1" to "1.5", a superscript 3 is added to the T_s parameter, the maximum and minimum values of the ENOB/SNR/THD/E_D/E_L parameters are revised from TBD data to specific values, the schematic in Note 3 is modified, the formula is optimized to represent sampling time, and the content descriptions in Note 3 and Note 4 are optimized; In the "VC Characteristics" chapter, the typical value of the V_{offset} parameter under the condition of "$AVCC = 1.8-5.5V, T_A = -40-105^\circ C$" is reduced by 5mV. 4. Package Specifications: In the "PCB Land Pattern" chapter, the QFN14 pad width is changed from "0.30mm" to "0.20mm", and the pin pitch is modified from "0.05mm" to "0.15mm".
Rev1.00 Apr. 14, 2025	First official release.