

HC32L12x Series

32-bit ARM[®] Cortex[®]-M0+ Microcontroller

Datasheet

Rev1.20
August 2026

Feature List

Support Features

- 48MHz Cortex-M0+ 32-bit CPU platform
- HC32L12x Series has a flexible power management system, ultra-low power performance Standby:
 - ▶ 0.65μA@3V DeepSleep mode: all clocks off, power-on reset active, IO state retention, IO interrupt active, all registers, RAM and CPU data save state power consumption
 - ▶ 27μA/MHz@3V@48MHz Sleep mode: CPU halted, peripherals off, main clock running
 - ▶ 51μA/MHz@3V@48MHz Operating Mode: CPU running, peripherals off, program running from Flash
- Maximum 128KB Flash memory, with erase and write protection function, support ISP, ICP, IAP
- Maximum 16KB RAM memory with parity check to enhance system stability
- GPIO: 56IO/64PIN, 40IO/48PIN, 26IO/32PIN, 20IO/24PIN
- Clock, Crystal
 - ▶ XTH: 8-32MHz
 - ▶ XTL: 32.768kHz
 - ▶ RCH: 4/6/32/48MHz
 - ◆ Accuracy up to 0.3% @25°C
 - ▶ RCL: 32.768/38.4kHz
 - ◆ Accuracy up to 0.5% @25°C
 - ▶ Hardware supports internal and external clock calibration and monitoring
- Timer/Counter
 - ▶ 3 1-channel complementary output general-purpose 16-bit timers
 - ▶ 1 3-channel complementary output general-purpose 16-bit timer
 - ▶ 2 low-power 16-bit timers, support cascading and PWM output
 - ▶ 1 programmable watchdog, built-in dedicated 10kHz oscillator to provide IWDG counting
 - ▶ 1 7-bit programmable window watchdog
- Communication interface
 - ▶ Up to 2-channel USART standard communication interface
 - ▶ Up to 3-channel LPUART low power communication interface, can work in DeepSleep mode
 - ▶ Up to 2-channel SPI standard communication interface
 - ▶ 2-channel I2C standard communication interface
 - ▶ 1-channel I2C high-speed communication interface
- Buzzer frequency generator supports complementary output
- Hardware perpetual calendar RTC
- Hardware CRC16/CRC32 module
- AES-128/192/256 hardware coprocessor
- TRNG
- 2-channel DMAC
- 4*40/6*38/8*36 LCD driver
- Globally unique 10-byte ID number
- Up to 2Msps sampling 12-bit high-speed SAR ADC, built-in Input follower, can measure signals with high output impedance
- Integrated 2-channel VC with 6-bit Resistor divider and programmable comparison reference
- Integrated LVD, can be configured with 16-step comparison voltage, can monitor port voltage and power supply voltage
- SWD debugging solution provides a full-featured debugger
- Working conditions: -40-105°C, 1.8-5.5V
- Package: LQFP64/48, QFN48/32/24

Support Model

HC32L126KATB-LQFP64	HC32L126KATB-LQ64
HC32L126JATB-LQ48	HC32L121JAUB-ZFN48TR
HC32L121FAUB-QFN32TR	-
HC32L121DAUB-UFN24TR	-

Statement

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Preface

Number Format

- 0x prefix is used for hexadecimal numbers
- 0b prefix is used for binary numbers
- Numbers without prefix are in decimal representation

Security Statement

There may be potential security problems due to the use of a certain function or protocol, which need to be declared to remind users and avoid security risks.

Contents

Feature List.....	ii
Preface.....	iv
1 Product Overview.....	8
1.1 Product Lineup.....	8
1.2 Functional Block Diagram.....	10
1.3 Memory Map.....	11
2 Functional Description.....	12
2.1 32-bit Cortex-M0+ Core.....	12
2.2 128KB FLASH.....	12
2.3 16KB RAM.....	12
2.4 Clock System.....	12
2.5 Operating Mode.....	12
2.6 RTC.....	13
2.7 GPIO.....	13
2.8 NVIC.....	13
2.9 RESET.....	13
2.10 DMAC.....	13
2.11 Timer.....	14
2.12 WDT.....	15
2.13 USART.....	15
2.14 LPUART.....	16
2.15 SPI.....	16
2.16 I2C.....	17
2.17 HSI2C.....	17
2.18 Buzzer.....	18
2.19 CTRIM.....	18
2.20 Electronic Signature.....	18
2.21 CRC.....	18
2.22 AES.....	18
2.23 TRNG.....	18
2.24 ADC.....	18
2.25 VC.....	19
2.26 LVD.....	19
2.27 LCD.....	19
2.28 Embedded Debugging System.....	20
2.29 Programming Mode.....	20
2.30 High Security.....	20
3 Pin Definitions.....	21
3.1 Pinout.....	21
3.1.1 LQFP64 Package.....	21
3.1.2 LQFP48 Package.....	22
3.1.3 QFN48 Package.....	23

3.1.4 QFN32 Package.....	24
3.1.5 QFN24 Package.....	25
3.2 Pin Function Description.....	26
3.3 Module Signal Description.....	31
4 Typical Application Circuit Diagram.....	33
5 Electrical Specifications.....	34
5.1 Parameter Conditions.....	34
5.1.1 Minimum and Maximum Values.....	34
5.1.2 Typical Values.....	34
5.2 Absolute Maximum Ratings.....	34
5.3 Operating Conditions.....	35
5.3.1 General Operating Conditions.....	35
5.3.2 VCAP External Capacitor.....	36
5.3.3 Working Conditions at Power-On and Power-Down.....	36
5.3.4 Embedded Reset and LVD Module Characteristics.....	37
5.3.5 Built-In Reference Voltage.....	39
5.3.6 Supply Current Characteristics.....	39
5.3.7 Time to Wake-Up from Low-Power Mode.....	41
5.3.8 External Clock Source Characteristics.....	42
5.3.9 Internal Clock Source Characteristics.....	47
5.3.10 Memory Characteristics.....	50
5.3.11 ESD Characteristics.....	50
5.3.12 I/O Port Characteristics.....	50
5.3.13 RESETB Pin Characteristics.....	53
5.3.14 ADC Characteristics.....	53
5.3.15 Temperature Sensor Characteristics.....	59
5.3.16 VC Characteristics.....	60
5.3.17 LCD Controller.....	62
5.3.18 TIM Timer Characteristics.....	63
5.3.19 Communication Interface.....	64
6 Package Specifications.....	68
6.1 Package Dimensions.....	68
6.1.1 LQFP64 Package.....	68
6.1.2 LQFP48 Package.....	70
6.1.3 QFN48 Package.....	72
6.1.4 QFN32 Package.....	74
6.1.5 QFN24 Package.....	76
6.2 PCB Land Pattern.....	78
6.2.1 LQFP64 Package (10mm*10mm).....	78
6.2.2 LQFP64 Package (7mm*7mm).....	79
6.2.3 LQFP48 Package (7mm*7mm).....	80
6.2.4 QFN48 Package (5mm*5mm).....	81
6.2.5 QFN32 Package (4mm*4mm).....	82
6.2.6 QFN24 Package (3mm*3mm).....	83
6.3 Package Marking.....	84

6.4 Packaging Thermal Resistance Coefficient.....	84
7 Ordering Information.....	86
Revision History	87

1 Product Overview

1.1 Product Lineup

Product Name

	HC	32	L	1	2	6	K	A	T	B
XiaoHua Semiconductor										
MCU Family 32: 32-bit										
Product Type L: Ultra-low power										
MCU Platform 1: Cortex-M0+										
MCU Specification Grade 2: Low-end										
Feature Configuration 1: Configuration 1 6: Configuration 6										
Pins K: 64 Pin J: 48 Pin F: 32 Pin D: 24 Pin										
Program Capacity A: 128KB										
Package T: LQFP U: QFN										
Temperature Grade B: -40-105°C, industrial level										

Model Function Comparison Table

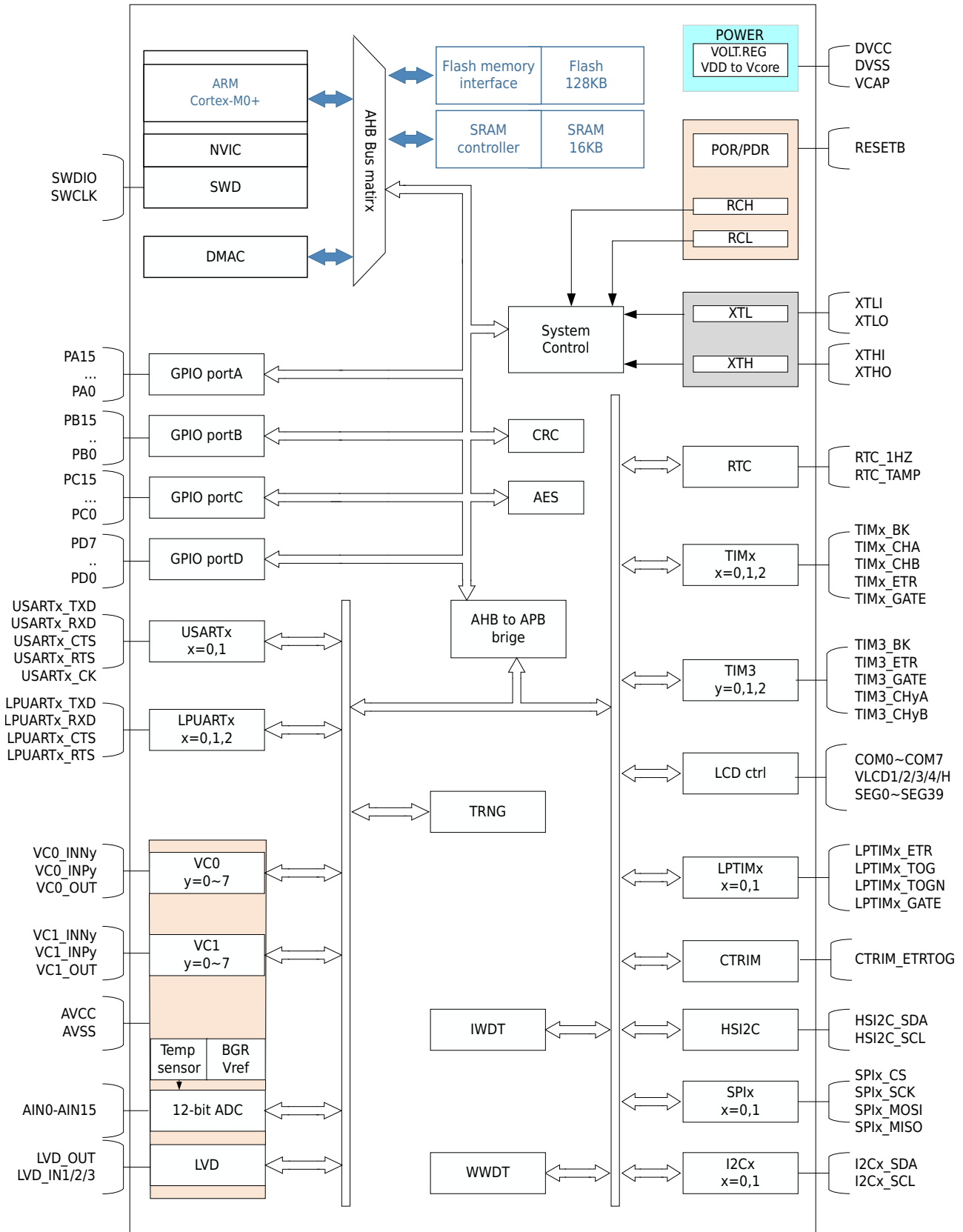
Product Name		HC32L126KATB	HC32L126JATB	HC32L121JAUB	HC32L121FAUB	HC32L121DAUB
Pins		64	48		32	24
GPIOs		56	40		26	20
CPU	Core	Cortex-M0+				
	Frequency	48MHz				
Memory	Flash	128KB				
	RAM	16KB				
Clock	RCH	4/6/32/48MHz				
	RCL	32.768/38.4kHz				
	XTH	8-32MHz				
	XTL	32.768kHz				
Power Voltage Range		1.8-5.5V				
Single/dual Power Supply		Single power supply				
Temperature Range		-40-105℃				
DMA Controller		2ch				
Timer	General Timer	TIM0/1/2/3				TIM0/1/2/3 ⁽²⁾
	Low Power Timer	LPTIM0/1				LPTIM0/1 ⁽³⁾
RTC		1				
Watchdog Timer		IWDT*1/WWDT*1				
Connectivity		USART0/1				USART0/1 ⁽⁴⁾
		LPUART0/1/2			LPUART0/2 ⁽¹⁾	
		I2C0/1				
		I2C (HS)				
		SPI0/1			SPI0	
ADC, 12-bit		16ch	10ch		7ch	6ch
VC		2				
LCD		4*40/6*38/8*36	4*26	-		
LVD		1				
CTRIM		Support				
Flash Security Protection		Support				
RAM Parity		Support				
CRC		Support				
TRNG		Support				
AES		Support				
Debug Function		SWD debug interface				
Unique Identification Code		Support				
Package (mm*mm)		LQFP64 (10*10) LQFP64 (7*7)	LQFP48 (7*7)	QFN48 (5*5)	QFN32 (4*4)	QFN24(3*3)



Note

1. QFN32 and QFN24 package lacks CTS/RTS function pin for LPUART2.
2. QFN24 package lacks CH1B function pin for TIM3.
3. QFN24 package lacks TOG function pin for LPTIM1.
4. QFN24 package lacks CTS function pin for USART1.

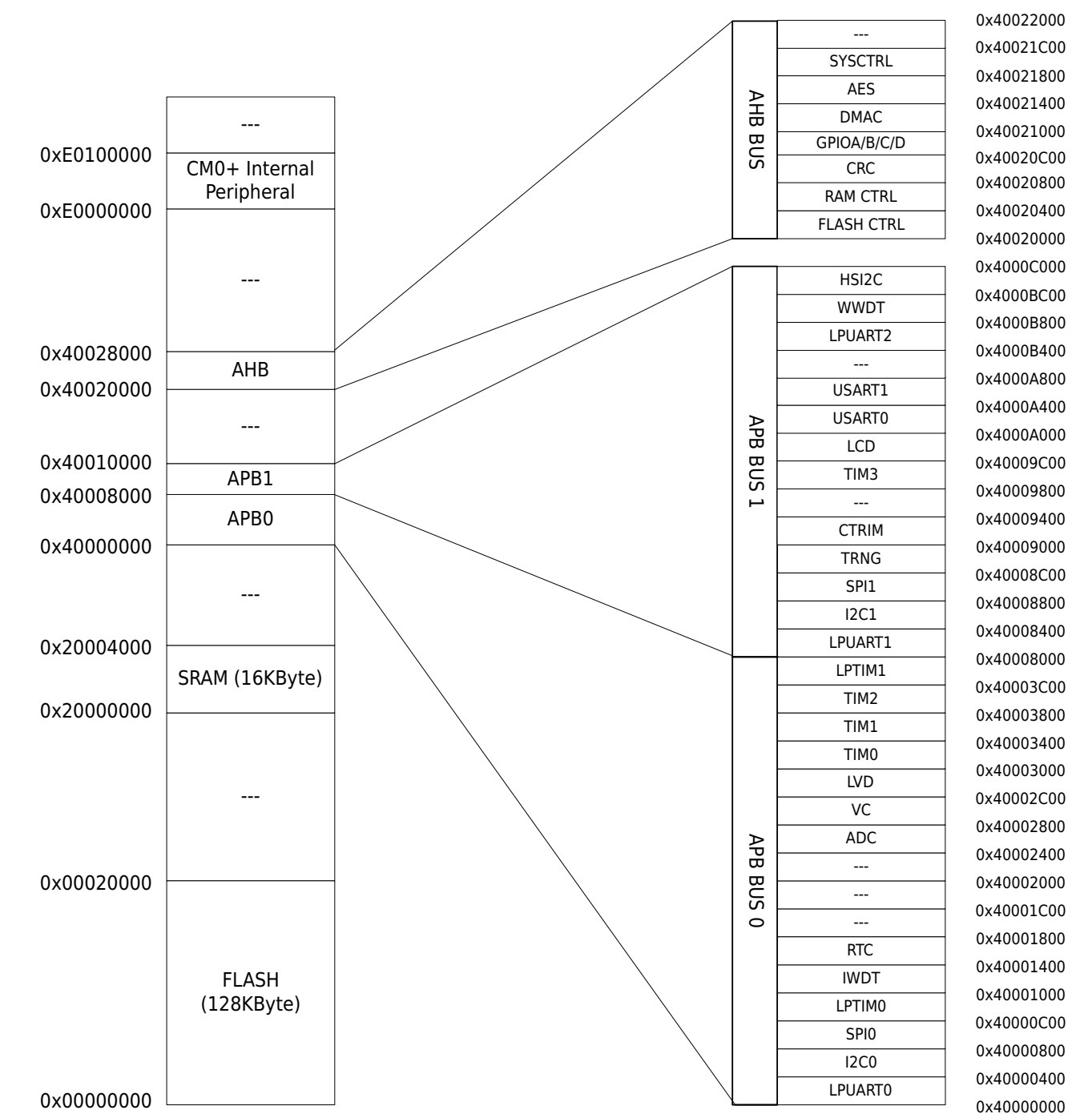
1.2 Functional Block Diagram



Note

Products in different packages support varying resources. For detailed specifications, please refer to [Model Function Comparison Table](#).

1.3 Memory Map



2 Functional Description

2.1 32-bit Cortex-M0+ Core

The ARM Cortex-M0+ processor is based on the Cortex-M0 and integrates a 32-bit RISC processor with a computing performance of 0.95 Dhrystone MIPS/MHz. It also incorporates multiple new designs, including improved debugging and tracing capabilities, reduced instructions per cycle (IPC) count, an enhanced two-stage pipeline for Flash access, and integrates energy-saving technologies. The Cortex-M0+ processor fully supports Keil & IAR debuggers.

The Cortex-M0+ includes a hardware debug circuit supporting the 2-pin SWD debug interface.

ARM Cortex-M0+ support features:

Instruction set	Thumb/Thumb-2
Assembly line	2-stage assembly line
Performance efficiency	2.46 CoreMark/MHz
Performance efficiency	0.95 DMIPS/MHz in Dhrystone
Interrupt	32 fast interrupts
Interrupt priority	Configurable 4-level interrupt priority
Enhanced instruction	Single-cycle 32-bit multiplier
Debugging	Serial-wire debug port, supports four break points and two watch points.

2.2 128KB FLASH

Built-in fully integrated FLASH controller, no need for external high voltage input, high voltage generated by the fully built-in circuit for programming. Supports ISP, IAP, ICP functions.

2.3 16KB RAM

According to different ultra-low power modes selected by customers, RAM data will be retained. With hardware parity bit, in case the data is accidentally damaged, when the data is read, the hardware circuit will immediately generate an interrupt to ensure the reliability of the system.

2.4 Clock System

- A high-precision internal RCH clock with configurable frequencies of 4/6/32/48MHz.
- An internal RCL clock with frequencies of 32.768/38.4kHz.
- An external crystal oscillator XTH with a frequency range of 8-32MHz.
- An external 32.768kHz crystal oscillator XTL, primarily providing the RTC real-time clock.

2.5 Operating Mode

1. Active Mode: CPU running, peripheral functional modules running.
2. Sleep mode: CPU halted, peripheral functional modules running.
3. DeepSleep mode: CPU halted, high-speed clock modules disabled.

2.6 RTC

The RTC (Real-Time Clock) is a functional module supporting BCD data format, typically using a 32.768kHz crystal as its clock. It enables perpetual calendar functionality with configurable interrupt periods: month/day/hour/minute/second. 24/12 hour time mode, the hardware automatically corrects leap years. It features precision compensation, supporting either 0.96ppm or 0.06ppm precision. Precision compensation can be performed using either the internal or external temperature sensor. Software adjustments of +1/-1 are available for year/month/day/hour/minute/second, with a minimum adjustable precision of one second.

The RTC calendar recorder used to indicate time and date does not reset the register when the MCU is reset by external factors.

2.7 GPIO

It can provide up to 56 GPIO ports, some of which are multiplexed with analog ports. Each port is controlled by independent control register bits and supports FAST IO. Supports edge-triggered interrupts and level-triggered interrupts, and can wake up the MCU to working mode from various ultra-low power consumption modes. Supports bit set, bit clear, and bit set clear operations. Supports CMOS Push-Pull output, Open-Drain output. Built-in pull-up resistor, pull-down resistor, with Schmitt trigger input filter function. The output drive capability is configurable, and the maximum current drive capability is 16mA. All general-purpose IOs can support external asynchronous interrupts.

Some ports feature digital input filtering.

When ports are multiplexed as HSI2C interfaces, they support level signal communication at different voltages, enabling low-voltage level recognition.

2.8 NVIC

The Cortex-M0+ processor integrates a Nested Vectored Interrupt Controller (NVIC) supporting up to 32 interrupt request (IRQ) inputs. With 4 interrupt priority levels, it can handle complex logic for real-time control and interrupt processing.

2.9 RESET

This product features 7 reset signal sources. Each reset signal can restart the CPU, reset most registers, and point the program counter (PC) to the starting address.

- Digital area power-on and power-off reset POR
- External Reset PAD, low level is reset signal
- WWDT reset
- IWDT reset
- LVD low voltage reset
- Cortex-M0+ SYSRESETREQ software reset
- Cortex-M0+ LOCKUP hardware reset

2.10 DMAC

The DMAC (Direct Memory Access Controller) function block can transmit data at high speed without passing through the CPU. Using DMAC can improve system performance.

- The DMAC is equipped with an independent bus, so even when the CPU bus is used, the DMAC can also perform transfer operations.

- Composed of 2 channels, capable of performing 2 independent DMA transfers.
- The transmission destination address, transmission source address, transmission data size, transmission request source, and transmission mode can be set, and the transmission operation start of each channel, the forced termination of transmission and the suspension of transmission can be controlled.
- It can control the start, forcibly terminate and pause of batch transmission of all channels.
- When multiple channels are operated at the same time, a fixed method or a cyclic method can be used to select the priority of the operating channel.
- Supports hardware DMA transfer using peripheral interrupt signals.
- Comply with system bus (AHB) and support 32-bit address space (4GB).

2.11 Timer

Name	Width	Prescaler	Count Direction	PWM	Capture	Complementary Output
TIM0	16/32	1/2/4/8/16/32/64/256	Up count/ Count down/ Up and down count	2	2	1
TIM1	16/32	1/2/4/8/16/32/64/256	Up count/ Count down/ Up and down count	2	2	1
TIM2	16/32	1/2/4/8/16/32/64/256	Up count/ Count down/ Up and down count	2	2	1
TIM3	16/32	1/2/4/8/16/32/64/256	Up count/ Count down/ Up and down count	6	6	3
LPTIM0	16	1/2/4/8/16/32/64/128/256/512/1024/2048/4096/8192/16384/32768	Up count	1	No	No
LPTIM1	16	1/2/4/8/16/32/64/128/256/512/1024/2048/4096/8192/16384/32768	Up count	1	No	No

General timer includes four timers: TIM0/1/2/3, supporting the following functions:

- PWM independent output, complementary output
- Capture input
- Pulse width measurement
- Quadrature encoder counting function
- Single pulse mode
- External counting function
- DMA trigger
- Dead-time control

- Braking control
- Cycle-by-cycle current limiting
- Edge alignment, symmetric center alignment and asymmetric center alignment PWM output

TIM0/1/2 have exactly the same function. TIM0/1/2 is a synchronous timer/counter, which can be used as a 16-bit timer/counter with automatic reloading function, or as a 32-bit timer/counter without reloading function. Each timer of TIM0/1/2 has 2 channels of capture and comparison function, which can generate 2 channels of independent PWM output or 1 group of complementary PWM outputs. With dead zone control function.

TIM3 is a multi-channel general-purpose timer with all functions of TIM0/1/2, capable of generating 3 sets of complementary PWM outputs or 6 independent PWM channels, with up to 6 input capture channels. With dead zone control function.

The low-power timer LPTIM is an asynchronous 16-bit timer/counter that can continue timing/counting via the internal low-speed RC oscillator, external low-speed crystal oscillator, or ETR external input even after the system clock is turned off. Wake up the system in low-power mode through interrupts. Supports PWM pulse output.

2.12 WDT

The IWDG (Independent Watch Dog Timer) is a configurable 12-bit timer that provides a reset in case of MCU malfunction, with the internal RC10K clock input as the counter clock. In debug mode and DeepSleep mode, it can be configured to pause or continue running; the IWDG can only be restarted by writing a specific sequence.

WWDT is a 7-bit timer. When external interference or unforeseen logic conditions cause the application program to deviate from the normal running sequence, WWDT can detect such software failures and generate interrupts or resets.

2.13 USART

2-channel Universal Synchronous Asynchronous Receiver/Transmitter.

Basic functions of USART:

- 2 baud rate generation methods: integer frequency division, decimal frequency division
- Built-in multifunctional timer/counter, supporting functions such as receive timeout
- Support DMA continuous communication
- Asynchronous serial port features
 - ▶ Transfer data asynchronously
 - ▶ 2 frame lengths: 8 bits, 9 bits
 - ▶ Frame check: odd check, even check, no check
 - ▶ 2 stop bits: 1 bit, 2 bits
 - ▶ Support hardware flow control (CTS/RTS)
 - ▶ Support single-wire half-duplex communication
 - ▶ Support baud rate automatic detection
 - ▶ Support for multiprocessor communication
- Synchronous serial port features
 - ▶ Transfer data synchronously
 - ▶ The data length is fixed at 8 bits

- ▶ Support hardware flow control (CTS/RTS)
- ▶ 2 communication clock sources: internal clock source, external clock source
- Smart card interface features
 - ▶ Communication protocol: ISO/IEC7816-3
 - ▶ 8 ETU lengths: 16-512
 - ▶ Support hardware error detection and retransmission
 - ▶ Support master interface
- Infrared communication features
 - ▶ Support 3/16 no carrier mode
 - ▶ Support 38K carrier modulation mode, adjustable duty cycle, configurable modulation level
- LIN features
 - ▶ Support synchronous interval transmission and detection
 - ▶ Support synchronous segment transmission and baud rate automatic detection

2.14 LPUART

3-channel Low-Power Universal Asynchronous Receiver/Transmitter (LPUART) that can operate in low-power mode.

Basic functions of LPUART:

- Configuration clock PCLK
- Transmission clock SCLK (SCLK can select XTL, RCL and PCLK)
- Support synchronous half-duplex, asynchronous full-duplex and single-wire half-duplex transmission.
- Programmable serial communication function
 - ▶ 2 character lengths: 8 bits, 9 bits
 - ▶ 3 check methods: no check, odd check, even check
 - ▶ 3 stop lengths: 1 bit, 1.5 bits, 2 bits
- Supports transmitting and receiving data in low power mode
- 16-bit baud rate counter
- Support hardware flow control (RTS, CTS)
- Support multi-machine communication and automatic address recognition
- Support data transfer via DMA

2.15 SPI

2-channel Serial Peripheral Interface(SPI).

Basic features of SPI:

- Can be configured as master or slave, support multi-machine mode
- The maximum division factor in master mode is PCLK/2
- The maximum division factor in slave mode is PCLK/4
- Multiple communication modes: full-duplex, single-wire half-duplex, simplex
- 2 transmission orders: MSB first or LSB first
- Various data frame lengths: 4bits-16bits
- 2 NSS methods: hardware control, software control
- Configurable serial clock polarity and phase

- Support DMA
- Support master mode delayed sampling

2.16 I2C

2-channel I2C, using serial synchronous clock, can realize data transmission between devices at different rates.

Basic features of I2C:

- Support 4 working modes of master sending/receiving and slave sending/receiving
- Support 3 operating rates: Standard (100kbps)/Fast (400kbps)/Fast enhanced (1Mbps)
- Support 7-bit addressing function
- Support noise filtering function
- Support 3 slave addresses
- Support broadcast address
- Support interrupt status query function

2.17 HSI2C

1-way enhanced channel supports independent Master and Slave mode operation.

HSI2C supports:

- Supports standard mode, fast mode, fast enhanced mode, and high-speed mode.
- Hs-mode in slave mode.
- Supports multi-master, including synchronization and arbitration. Multi-master means any number of masters can be present. In addition, the master and slave roles can be changed during the transmission gap (after a STOP is sent).
- Supports 7-bit and 10-bit addressing.
- Supports software reset, START byte, and device ID (software support is also required).
- Supports DMA transmission and reception.

HSI2C master supports:

- One word of command/transmit buffer (8-bit transmit data + 3-bit command), one word of receive buffer (8-bit receive data).
- The command buffer will wait for the I2C bus to be idle before starting the transmission.
- The command buffer can initialize (repeated) START and STOP conditions, as well as one or more master receive transmissions.
- The STOP condition can be generated from the command buffer or automatically when the transmit buffer is empty.
- Flexible receive data matching function can generate interrupts when data matching and/or discard unwanted data.
- Flags and optional interrupts to indicate Repeated START conditions, STOP conditions, arbitration loss, NACK, and command word errors.
- Supports configurable bus idle timeout and pin-stuck-low timeout.

HSI2C slave supports:

- Separate I2C slave registers to minimize software overhead for switching between master/slave.
- Supports SMBus alert address and broadcast address.
- Supports clock stretching.

- Supports transmit data register interrupt and receive data register interrupt.
- Software-controllable ACK or NACK, configurable ACK/NACK bit clock stretching. This is to avoid transmit buffer underrun and receive buffer overflow errors.
- Supports flags and interrupts for end of packet, STOP condition, or bit error detection.
- Support Ultra low power wake-up mode.

2.18 Buzzer

Four general-purpose timers and two low-power timers function multiplexing output to provide programmable driving frequency for Buzzer. The buzzer port can provide 16mA sink current, complementary output, no additional transistor is needed.

2.19 CTRIM

In calibration mode, this module automatically performs real-time calibration of the RCH/RCL output frequency, making RCH/RCL's accuracy immune to environmental variations. When the module works in timer mode, it has general timing function and can still work normally in DeepSleep mode.

2.20 Electronic Signature

Each chip has a unique 10-byte device identification number before leaving the factory, including wafer lot information, chip coordinate information, and so on.

2.21 CRC

CRC16 conforms to the polynomial given in ISO/IEC13239: $x^{16} + x^{12} + x^5 + 1$.

CRC32 conforms to the polynomial given in ISO/IEC13239: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$.

Support algorithms: CRC16/CCITT, CRC16/CCITT-FALSE, CRC16/XMODE, CRC16/X25, CRC32, CRC32/MPEG-2.

2.22 AES

Advanced Encryption Standard (AES) is a new data encryption standard officially announced by the National Institute of Standards and Technology (NIST) on November 26, 2001. The block size of AES is fixed at 128 bits, while the key length supports 128/192/256 bits.

2.23 TRNG

TRNG is a true random number generator, used to generate true random numbers.

2.24 ADC

A monotonic no missing code 12-bit successive approximation register analog-to-digital converter.

- 12-bit conversion accuracy
- A maximum of 2Msps conversion speed
- Up to 19 input channels are supported, including 16 external pin inputs, 1 internal temperature sensor voltage channel, 1 channel of 1/3 AVCC voltage, and 1 channel of internal 1.2V reference voltage VREF1P2
- 4 reference sources: AVCC voltage, EXVREF pins, internal 1.5V reference voltage, internal 2.5V reference voltage
- ADC voltage input range: 0-Vref

- Built-in signal follower, which can convert high-impedance signals
- Multiple conversion modes: single conversion, SQR scan conversion, and JQR scan conversion
- Software can configure ADC conversion rate
- Support on-chip peripherals to automatically trigger ADC conversion, effectively reducing chip power consumption and improving real-time conversion
- ADC conversion results are continuously accumulated
- Input channel voltage threshold monitoring

2.25 VC

Built-in 2-channel Analog Voltage Comparator (VC), chip pin voltage monitoring/comparison circuit. 8 configurable positive external input channels, 5 configurable negative external input channels; 3 internal negative input channels including 1-channel internal temperature sensor voltage, 1-channel VCore voltage, and 1-channel 64-step resistor divider voltage. The VC output can be used by TIM0/1/2/3 and LPTIM. Can generate asynchronous interrupts based on rising/falling edges to wake up the MCU from low-power modes. Configurable software anti-shake function. Configurable blanking window function.

2.26 LVD

Detects chip supply voltage or pin voltage, supporting the following functions:

- 4 monitoring sources
- 16-stage threshold voltage, 1.8-4.8V optional
- 8 trigger conditions, combinations of high level, rising edge and falling edge
- 2 trigger results: reset and interrupt
- 12-stage filter configuration to prevent false triggering
- With hysteresis function, strong anti-interference

2.27 LCD

The LCD controller is a digital controller/driver designed for monochrome passive liquid crystal display (LCD), featuring up to 8 common terminals (COM) to drive 160 (4x40), 228 (6x38) or 288 (8x36) LCD pixel elements. Can choose either capacitor voltage divider or resistor voltage divider, support internal resistor divider. The internal resistor divider can adjust the contrast. Support DMA hardware data transfer.

Basic features of LCD:

- Highly flexible frame rate control
- Support static, 1/2, 1/3, 1/4, 1/6 and 1/8 duty cycle
- Support 1/2, 1/3, 1/4 offset
- LCD data RAM with up to 16 registers
- The contrast of LCD can be configured through software
- Three drive waveform generation methods
 - ▶ Internal resistor divider, external resistor divider, external capacitor divider method
 - ▶ The power consumption of the internal resistor divider method can be configured through software to match the capacitive charge required by the LCD panel
- Support low power mode: LCD controller can display in Active, Sleep, DeepSleep mode
- Configurable frame interrupt
- Support LCD blinking function and configurable multiple blinking frequencies

- The unused LCD segments and common pins can be configured as digital or analog functions
- Support dead zone insertion

2.28 Embedded Debugging System

Embedded debugging solution, providing a full-featured real-time debugger, with standard mature Keil/IAR and other debugging and development softwares.

2.29 Programming Mode

Support programming modes: online programming and offline programming.

Support programming protocols: ISP protocol, SWD protocol.

Support programming interface: ISP protocol and SWD protocol share SWD port.

- When the package of this MCU has a BOOT pin:
 - ▶ When the BOOT0 (PD03) pin is at high level during power-on or LVD/RESET pin resets, the chip operates in ISP programming mode, and the Flash can be programmed through the ISP protocol.
 - ▶ When the BOOT0 (PD03) pin is at low level during power-on or LVD/RESET pin resets, the chip waits for several hundred microseconds time window to receive ISP programming command. If programming command is received, it operates in ISP programming mode; otherwise, it enters user mode, the chip executes the program code in the Flash, and the Flash can be programmed through the SWD protocol.
- When the package of this MCU does not have a BOOT pin:
 - ▶ After power-on or LVD/RESET pin resets, if the chip receives ISP programming command within the several hundred microseconds time window, the chip will operate in ISP programming mode, and the Flash can be programmed through the ISP protocol.
 - ▶ After power-on or LVD/RESET pin resets, if the chip does not receive ISP programming command within the several hundred microseconds time window, the chip will operate in user mode, the chip executes the program code in the Flash, and the Flash can be programmed through the SWD protocol.

2.30 High Security

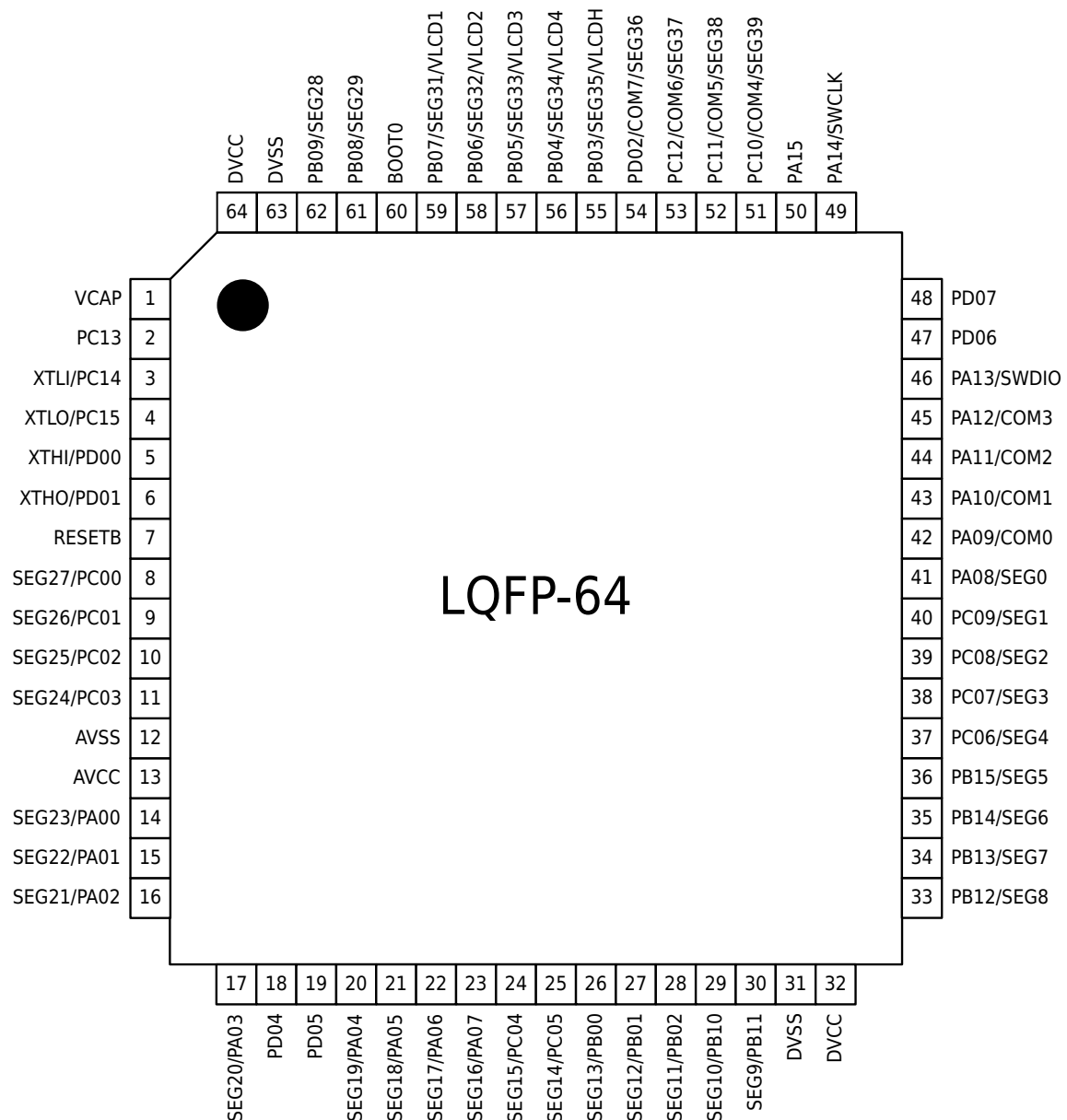
Encrypted embedded debugging solution, providing a full-featured real-time debugger.

3 Pin Definitions

3.1 Pinout

3.1.1 LQFP64 Package

HC32L126KATB-LQFP64, HC32L126KATB-LQ64

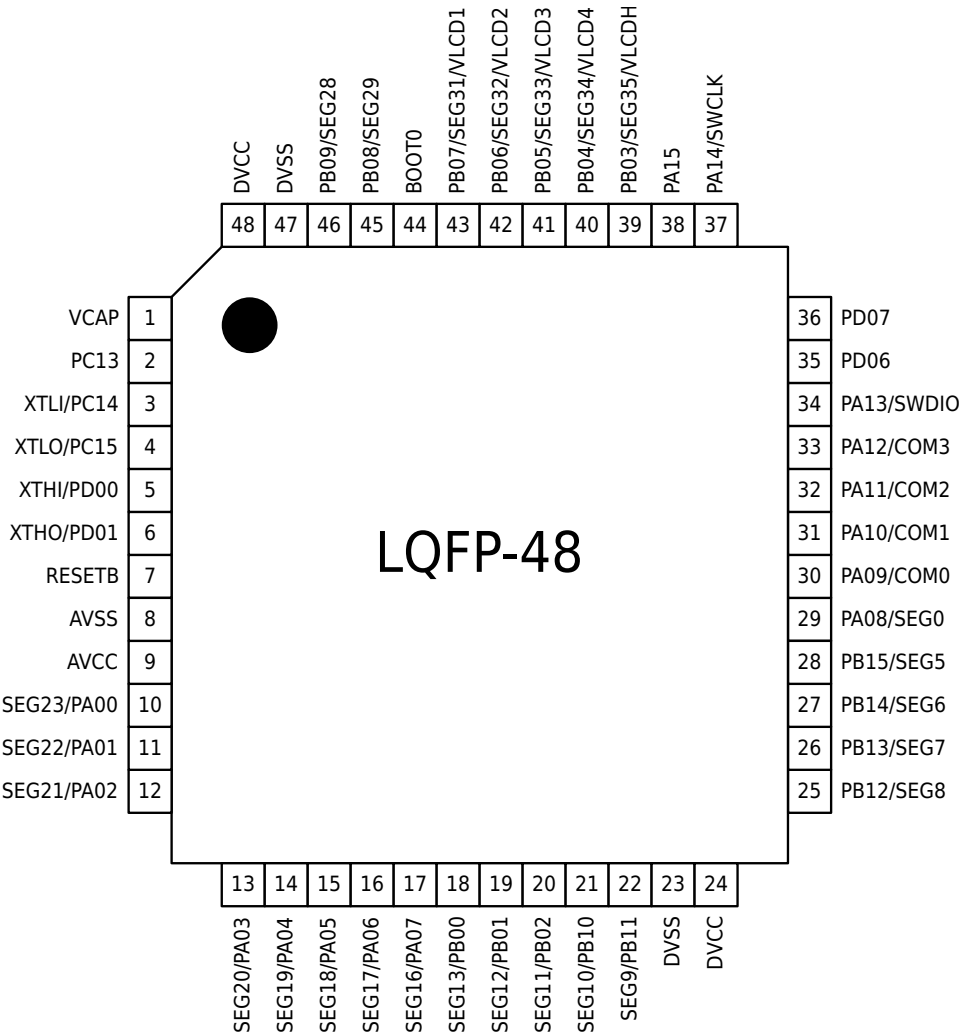


Note

- For details on the IOs not brought out by this package, please refer to [Pin Function Description](#).
- BOOT0 pin is used to control FLASH programming, see [Module Signal Description](#).

3.1.2 LQFP48 Package

HC32L126JATB-LQ48

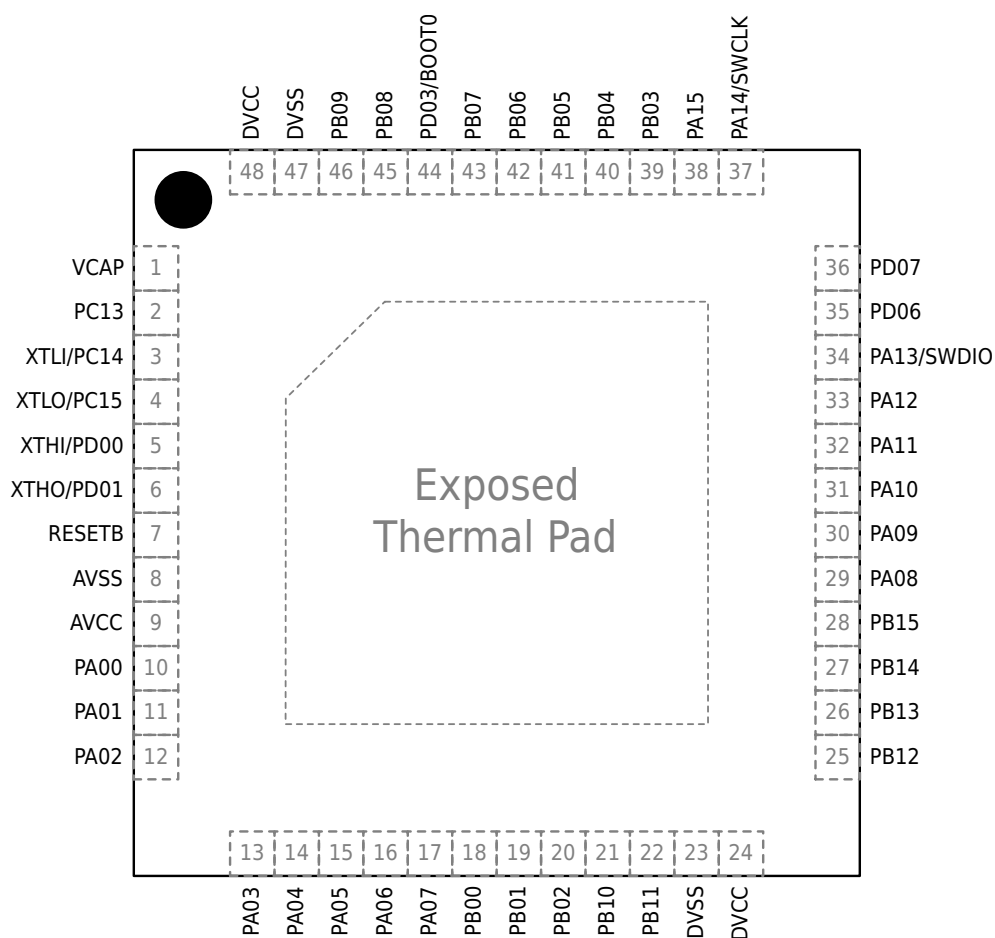


Note

- For details on the IOs not brought out by this package, please refer to [Pin Function Description](#).
- BOOT0 pin is used to control FLASH programming, see [Module Signal Description](#).

3.1.3 QFN48 Package

HC32L121JAUB-ZFN48TR

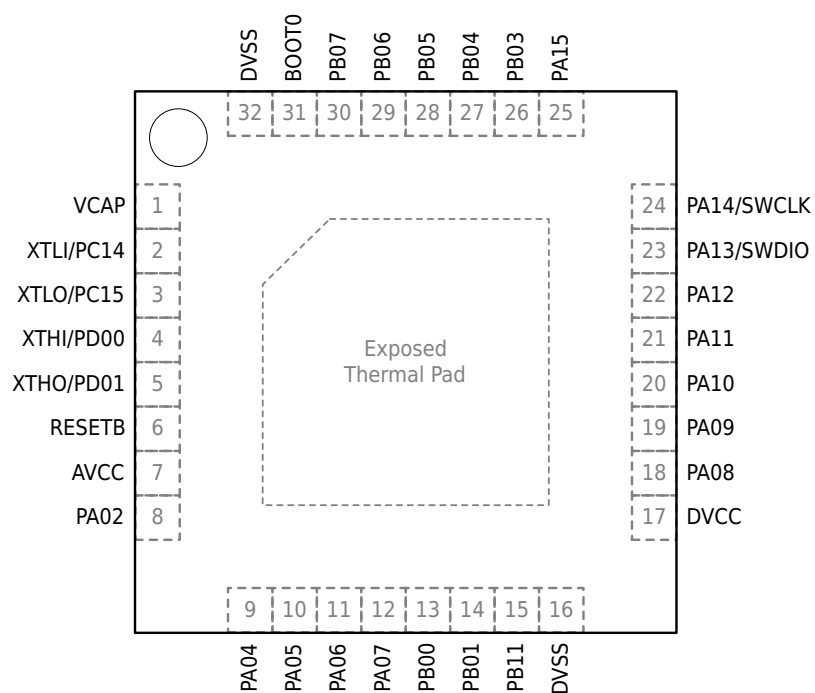


Note

- Exposed Thermal Pad needs to be connected to DVSS.
- For details on the IOs not brought out by this package, please refer to [Pin Function Description](#).
- BOOT0 pin is used to control FLASH programming, see [Module Signal Description](#).

3.1.4 QFN32 Package

HC32L121FAUB-QFN32TR

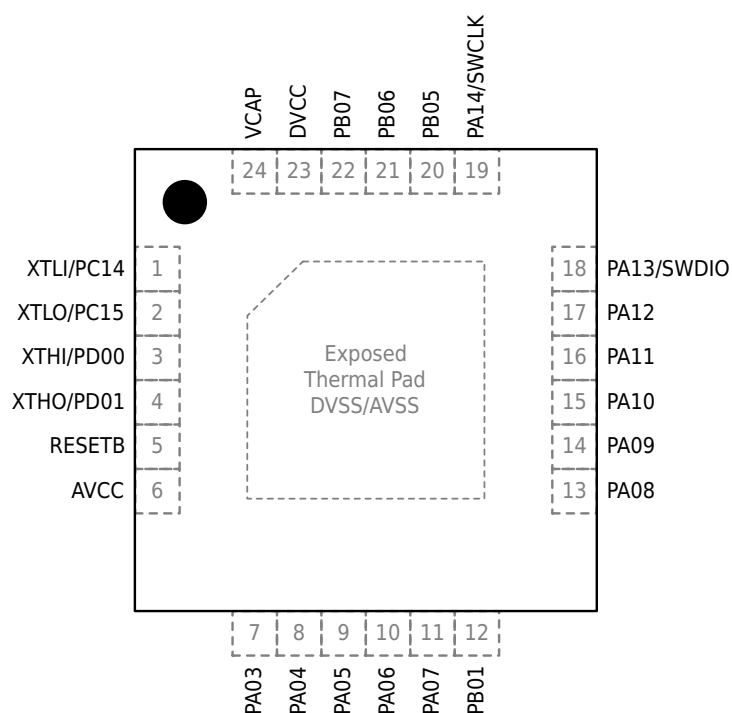


Note

- Exposed Thermal Pad needs to be connected to DVSS.
- For details on the IOs not brought out by this package, please refer to [Pin Function Description](#).
- BOOT0 pin is used to control FLASH programming, see [Module Signal Description](#).

3.1.5 QFN24 Package

HC32L121DAUB-UFN24TR



Note

- Exposed Thermal Pad must be connected to DVSS/AVSS.
- For details on the IOs not brought out by this package, please refer to [Pin Function Description](#).
- This package has no BOOT pin. For details, please refer to [Programming Mode](#).

3.2 Pin Function Description

LQFP64	LQFP48	QFN48	QFN32	QFN24	Name	Analog
1	1	1	1	24	VCAP	-
2	2	2			PC13	LVD_IN1
3	3	3	2	1	PC14	XTLI
4	4	4	3	2	PC15	XTLO
5	5	5	4	3	PD00	XTHI
6	6	6	5	4	PD01	XTHO
7	7	7	6	5	RESETB	-
8					PC00	AIN10 SEG27
9					PC01	AIN11 SEG26
10					PC02	AIN12 SEG25
11					PC03	AIN13 SEG24
12	8	8			AVSS	-
13	9	9	7	6	AVCC	-
14	10	10			PA00	AIN0 VC0_INN0 SEG23
15	11	11			PA01	AIN1 VC0_INP0 VC1_INP0 SEG22
16	12	12	8		PA02	AIN2 VC1_INN0 SEG21
17	13	13		7	PA03	AIN3 VC0_INP1 VC1_INP1 SEG20
18					PD04	-
19					PD05	-
20	14	14	9	8	PA04	AIN4 VC0_INN1 VC1_INN1 SEG19
21	15	15	10	9	PA05	AIN5 VC0_INN2 VC2_INN2 SEG18
22	16	16	11	10	PA06	AIN6 VC0_INP2 VC1_INP2 SEG17
23	17	17	12	11	PA07	AIN7 VC0_INP3 VC1_INP3 SEG16

LQFP64	LQFP48	QFN48	QFN32	QFN24	Name	Analog
24					PC04	AIN14 SEG15
25					PC05	AIN15 SEG14
26	18	18	13		PB00	AIN8 SEG13
27	19	19	14	12	PB01	AIN9/EXVREF VC0_INN3 SEG12
28	20	20			PB02	SEG11
29	21	21			PB10	SEG10
30	22	22	15		PB11	SEG9
31	23	23	16		DVSS	-
32	24	24	17		DVCC	-
33	25	25			PB12	SEG8
34	26	26			PB13	SEG7
35	27	27			PB14	SEG6
36	28	28			PB15	SEG5
37					PC06	SEG4
38					PC07	SEG3
39					PC08	SEG2
40					PC09	SEG1
41	29	29	18	13	PA08	SEG0
42	30	30	19	14	PA09	COM0
43	31	31	20	15	PA10	COM1
44	32	32	21	16	PA11	COM2
45	33	33	22	17	PA12	COM3
46	34	34	23	18	PA13/SWDIO	-
47	35	35			PD06	-
48	36	36			PD07	-
49	37	37	24	19	PA14/SWCLK	-
50	38	38	25		PA15	-
51					PC10	COM4/SEG39
52					PC11	COM5/SEG38
53					PC12	COM6/SEG37
54					PD02	COM7/SEG36
55	39	39	26		PB03	VC1_INN3 SEG35/VLCDH
56	40	40	27		PB04	VC0_INP4 VC1_INP4 SEG34/VLCD4
57	41	41	28	20	PB05	VC0_INP5 VC1_INP5 SEG33/VLCD3
58	42	42	29	21	PB06	VC0_INP6 VC1_INP6 SEG32/VLCD2

LQFP64	LQFP48	QFN48	QFN32	QFN24	Name	Analog
59	43	43	30	22	PB07	VC0_INP7 VC1_INP7 LVD_IN3 SEG31/VLCD1
60	44	44	31		BOOT0/PD03	SEG30
61	45	45			PB08	LVD_IN2 SEG29
62	46	46			PB09	SEG28
63	47	47	32		DVSS	-
64	48	48		23	DVCC	-

The digital function of each pin is controlled by the PSEL bit field, as detailed in the following table.

Table 3-2 Port Multiplexing Table

AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA00	USART1_CTS	LPUART1_TXD	TIM0_ETR	VC0_OUT	TIM1_CHA	TIM3_ETR	TIM0_CHA
PA01	USART1_RTS	LPUART1_RXD	TIM0_CHB	TIM1_ETR	TIM1_CHB	HCLK_OUT	SPI1_MOSI
PA02	USART1_TXD	TIM0_CHA	VC1_OUT	TIM1_CHA	TIM2_CHA	PCLK_OUT	SPI1_MISO
PA03	USART1_RXD	TIM0_GATE	TIM1_CHB	TIM2_CHB	SPI1_CS	TIM3_CH1A	-
PA04	SPI0_CS	USART1_TXD	LPUART1_RTS	TIM2_ETR	-	LVD_OUT	TIM3_CH2B
PA05	SPI0_SCK	TIM0_ETR	LPUART1_CTS	TIM0_CHA	USART1_RTS	XTL_OUT	XTH_OUT
PA06	SPI0_MISO	LPTIM0_TOG	TIM3_BK	TIM1_CHA	VC0_OUT	TIM3_GATE	LPUART0_CTS
PA07	SPI0_MOSI	LPTIM0_TOGN	HCLK_OUT	TIM3_CH0B	TIM2_CHA	VC1_OUT	LPUART0_RXD
PA08	USART0_TXD	TIM3_CH0A	CTRM_ETRTOG	LPTIM1_ETR	TIM1_GATE	-	TIM3_BK
PA09	USART0_TXD	TIM3_CH1A	TIM0_BK	I2C0_SCL	LPUART0_TXD	HCLK_OUT	TIM3_CH0A
PA10	USART0_RXD	TIM3_CH2A	TIM2_BK	I2C0_SDA	TIM2_GATE	PCLK_OUT	TIM0_CHB
PA11	USART0_CTS	TIM3_GATE	I2C1_SCL	HSI2C_SCL	VC0_OUT	SPI0_MISO	CTRM_ETRTOG
PA12	USART0_RTS	TIM3_ETR	I2C1_SDA	HSI2C_SDA	VC1_OUT	SPI0_MOSI	-
PA13	IR_OUT	USART0_RXD	LVD_OUT	TIM3_ETR	RTC_1HZ	I2C1_SDA	USART1_SCK
PA14	USART1_TXD	USART0_TXD	TIM3_CH2A	LVD_OUT	RCH_OUT	RCL_OUT	I2C1_SCL
PA15	SPI0_CS	USART1_RXD	LPUART1_RTS	TIM0_ETR	TIM0_CHA	TIM3_CH1A	USART0_SCK
PB00	-	TIM3_CH1B	LPUART0_TXD	LPTIM1_TOG	RCH_OUT	RCL_OUT	-
PB01	-	PCLK_OUT	TIM3_CH2B	-	LPUART0_RTS	LPTIM1_ETR	TCLK_OUT
PB02	LPTIM0_TOG	-	LPUART1_TXD	-	TIM1_BK	TIM0_BK	TIM2_BK
PB03	SPI0_SCK	TIM0_CHB	TIM1_GATE	TIM3_CH0A	LPTIM0_GATE	XTL_OUT	XTH_OUT
PB04	SPI0_MISO	-	TIM2_BK	USART0_CTS	TIM2_GATE	TIM3_CH0B	LPTIM0_ETR
PB05	SPI0_MOSI	HSI2C_SCL	TIM1_BK	-	LPTIM0_GATE	-	USART0_RTS
PB06	I2C0_SCL	USART0_TXD	TIM1_CHB	TIM0_CHA	LPTIM0_ETR	TIM3_CH0A	LPTIM0_TOG
PB07	I2C0_SDA	USART0_RXD	TIM2_CHB	LPUART1_CTS	TIM0_CHB	LPTIM0_TOGN	-
PB08	I2C0_SCL	TIM1_CHA	USART1_SCK	TIM2_CHA	TIM0_GATE	TIM3_CH2A	USART0_TXD
PB09	I2C0_SDA	IR_OUT	SPI1_CS	TIM2_CHA	HSI2C_SDA	TIM2_CHB	USART0_RXD
PB10	I2C1_SCL	SPI1_SCK	TIM1_CHA	LPUART0_TXD	TIM3_CH1A	LPUART1_RTS	USART1_RTS
PB11	I2C1_SDA	TIM1_CHB	LPUART0_RXD	TIM2_GATE	-	LPUART1_CTS	USART1_CTS

AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB12	SPI1_CS	TIM3_BK	LPUART0_TXD	TIM0_BK	USART0_SCK	LPUART0_RTS	-
PB13	SPI1_SCK	I2C1_SCL	TIM3_CH0B	LPUART0_CTS	TIM1_CHA	TIM1_GATE	-
PB14	SPI1_MISO	I2C1_SDA	TIM3_CH1B	TIM0_CHA	RTC_1HZ	LPUART0_RTS	TIM1_BK
PB15	SPI1_MOSI	TIM3_CH2B	TIM0_CHB	TIM0_GATE	-	-	LPUART1_RXD
PC00	LPTIM0_GATE	-	USART1_CTS	HSI2C_SCL	-	-	-
PC01	LPTIM0_TOG	-	USART1_RTS	HSI2C_SDA	-	-	-
PC02	SPI1_MISO	LPTIM0_TOGN	-	-	-	-	-
PC03	SPI1_MOSI	LPTIM0_ETR	LPTIM0_TOGN	-	-	-	-
PC04	LPUART0_TXD	TIM2_ETR	IR_OUT	-	-	-	-
PC05	LPUART0_RXD	-	-	-	-	-	-
PC06	-	-	TIM2_CHA	LPTIM1_GATE	-	LPUART2_RXD	-
PC07	-	-	TIM2_CHB	LPTIM1_ETR	-	LPUART2_TXD	-
PC08	-	-	TIM2_ETR	LPTIM1_TOG	-	LPUART2_CTS	-
PC09	-	-	TIM1_ETR	LPTIM1_TOGN	-	LPUART2_RTS	-
PC10	LPUART1_TXD	LPUART0_TXD	-	-	-	-	-
PC11	LPUART1_RXD	LPUART0_RXD	-	-	-	-	-
PC12	LPUART0_TXD	LPUART1_TXD	-	-	-	-	-
PC13	RTC_TAMP	RTC_1HZ	TIM3_CH1B	-	-	-	-
PC14	-	USART0_SCK	-	LPTIM1_TOGN	-	-	-
PC15	-	USART1_SCK	-	LPTIM1_GATE	-	-	-
PD00	I2C0_SDA	CTRM_ETRTOG	USART1_TXD	-	-	LPUART2_RXD	-
PD01	I2C0_SCL	-	USART1_RXD	-	-	LPUART2_TXD	-
PD02	-	LPUART0_RTS	TIM1_ETR	HSI2C_SCL	-	-	-
PD03	-	-	-	-	-	-	-
PD04	-	-	LPTIM1_TOGN	-	-	-	-
PD05	USART0_SCK	-	LPTIM1_TOG	HSI2C_SDA	-	-	-
PD06	I2C1_SCL	LPUART1_CTS	USART0_CTS	LPTIM1_GATE	-	LPUART2_CTS	-
PD07	I2C1_SDA	LPUART1_RTS	USART0_RTS	LPTIM1_TOGN	-	LPUART2_RTS	-

3.3 Module Signal Description

Table 3-3 Module Signal Description

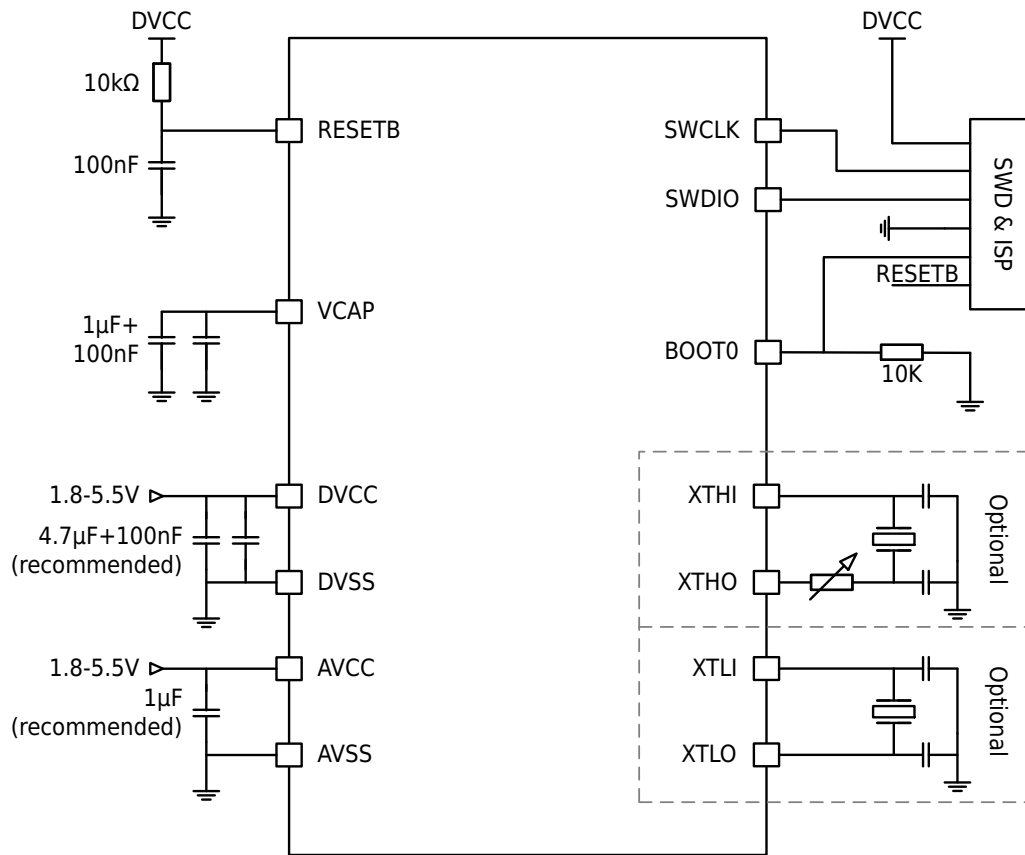
Modules	Pin Name	Description
Power supply	DVCC	Digital power supply
	AVCC	Analog power
	DVSS	Digital ground
	AVSS	Analog ground
	VCAP	LDO core power supply output (only for internal circuit use, external voltage stabilization capacitor is required)
ISP	BOOT0	When reset, the BOOT0 (PD03) pin is high level, the chip works in ISP programming mode, and Flash can be programmed through ISP protocol When reset, the BOOT0 (PD03) pin is low level, the chip waits for several hundred microseconds time window to receive ISP programming command. If programming command is received, it operates in ISP programming mode; otherwise, it enters user mode, the chip executes the program code in the Flash, and the Flash can be programmed through the SWD protocol
ADC	AINx (x=0-15)	ADC input channel
	EXVREF	ADC external reference voltage
VC	VCx_INNy (x=0-1 y=0-7)	VC0/1 negative terminal input
	VCx_INPy (x=0-1 y=0-7)	VC0/1 positive terminal input
	VCx_OUT (x=0-1)	VC0/1 compare output
LVD	LVD_INx (x=1-3)	Voltage detection input
	LVD_OUT	Voltage detection output
LCD	COMx (x=0-7)	LCD common output
	SEgy (y=0-39)	LCD segment output
	VLCDx (x=1-4, H)	External resistance mode, external capacitor mode uses pins
USART	USARTx_TXD (x=0-1)	USART data transmitter
	USARTx_RXD (x=0-1)	USART data receiver
	USARTx_CTS (x=0-1)	USART transmit hardware flow control
	USARTx_RTS (x=0-1)	USART receive hardware flow control
	USARTx_SCK (x=0-1)	USART clock input and output
LPUART	LPUARTx_TXD (x=0-2)	LPUART data transmitter
	LPUARTx_RXD (x=0-2)	LPUART data receiver
	LPUARTx_CTS (x=0-2)	LPUART transmit hardware flow control
	LPUARTx_RTS (x=0-2)	LPUART receive hardware flow control

Modules	Pin Name	Description
CTRIM	CTRIM_ETRTOG	CTRIM external sync signal/inverted output signal
SPI	SPIx_MISO (x=0-1)	SPI master input and slave output data signal
	SPIx_MOSI (x=0-1)	SPI master output and slave input data signal
	SPIx_SCK (x=0-1)	SPI clock signal
	SPIx_CS (x=0-1)	SPI chip selection
I2C	I2Cx_SDA(x=0-1)	I2C data signal
	I2Cx_SCL(x=0-1)	I2C clock signal
HSI2C	HSI2C_SDA	HSI2C data signal
	HSI2C_SCL	HSI2C clock signal
RTC	RTC_1HZ	RTC 1Hz output
	RTC_TAMP	RTC timestamp input
TIM0-2	TIMx_CHA (x=0-2)	Capture input and compare output A of TIM
	TIMx_CHB (x=0-2)	Capture input and compare output B of TIM
	TIMx_ETR (x=0-2)	External counting input signal of TIM
	TIMx_BK(x=0-2)	External brake input signal of TIM
	TIMx_GATE (x=0-2)	Gating signal of TIM
TIM3	TIM3_CHyA (y=0-2)	Capture input and compare output A of TIM3
	TIM3_CHyB (y=0-2)	Capture input and compare output B of TIM3
	TIM3_ETR	External counting input signal of TIM3
	TIM3_BK	External brake input signal of TIM3
	TIM3_GATE	Gating signal of TIM3
LPTIM	LPTIMx_TOG (x=0-1)	Toggle/PWM output signal of LPTimer
	LPTIMx_TOGN (x=0-1)	Toggle/PWM output inverted signal of LPTimer
	LPTIMx_ETR (x=0-1)	External count input signal of LPTimer
	LPTIMx_GATE (x=0-1)	Gating signal of LPTimer

**Note**

The IO port is reset to the input high impedance stat, while the port states are maintained in Sleep mode and DeepSleep mode.

4 Typical Application Circuit Diagram



Notice

- AVCC and DVCC voltage must be the same.
- Power supply for each group requires external decoupling capacitors. For better anti-interference capability, it is preferable to route the power supply/ground lines through the decoupling capacitors first before connecting them to the chip.
- The crystal and load capacitors should be placed as close as possible to the oscillator pins of the chip.
- The VCAP decoupling capacitor should be placed as close as possible to the chip pin and kept as far away as possible from the crystal load capacitors.
- For packages without a BOOT pin, ignore the BOOT0 line diagram.

5 Electrical Specifications

5.1 Parameter Conditions

Unless otherwise specified, all voltages are based on VSS.

5.1.1 Minimum and Maximum Values

All Minimum Values and Maximum Values are measured under the worst conditions.

Data resulted from comprehensive evaluation, and/or guaranteed by design are indicated in the table footnotes, and they will not be tested on the production line.

5.1.2 Typical Values

Unless otherwise specified, typical data are given based on $T_A=25^{\circ}\text{C}$ and $V_{CC}=3.3\text{V}$. These data are only used for design guidance and have not been tested.

5.2 Absolute Maximum Ratings

If the load applied to the device exceeds the value given in the list of "Absolute Maximum Ratings", it may cause permanent damage to the device. The maximum load given here is for reference, which does not mean that the functional operation of the device is correct under this condition. Operation of the device under the condition of maximum value for a long time will affect the reliability of the device.

Table 5-1 Voltage and Current Characteristics

Symbol	Parameters	Min	Max	Unit
VCC-VSS	External main supply voltage (including AVCC and DVCC) ⁽¹⁾	-0.3	6.0	V
V _{IN}	Input voltage at other pins ⁽²⁾⁽⁵⁾	VSS-0.3	VCC+0.3	V
ΔVCCx	Voltage difference between different power supply pins	-	50	mV
VSSx-VSS	Voltage difference between different grounding pins	-	50	mV
I _{VCC}	Total current through DVCC/AVCC power line (supply current) ⁽¹⁾	-	100	mA
I _{VSS}	Total current through DVSS/AVSS ground wire (outflow current) ⁽¹⁾	-	100	mA
I _{IO}	Output sink current on any I/O and control pins	-	25	mA
	Output current on any I/O and control pins	-	-25	mA
I _{INJ(PIN)} ⁽²⁾⁽³⁾	Injection current of RESETB pin	-	±5	mA
	Injection current of XTH pin of XTH and XTL pin of XTL	-	±5	mA
	Injection current of other pins ⁽⁴⁾	-	±5	mA
ΣI _{INJ(PIN)} ⁽²⁾	Total injection current on all I/O and control pin ⁽⁴⁾	-	±25	mA

**Note**

1. All power supply (DVCC, AVCC) and grounding (DVSS, AVSS) pins should always be connected to the power supply system within the external allowable range.
2. $I_{INJ(PIN)}$ should not exceed its limit, that is, ensure that V_{IN} does not exceed its maximum value. If V_{IN} cannot be guaranteed not to exceed its maximum value, it is also necessary to ensure that $I_{INJ(PIN)}$ does not exceed its maximum value externally. When $V_{IN} > VCC$, there is a forward injection current; When $V_{IN} < VSS$, there is a reverse injection current.
3. The reverse injection current will interfere with the simulation performance of the device.
4. When several I/O ports have injection currents at the same time, the maximum value of $\sum I_{INJ(PIN)}$ is the sum of the instantaneous absolute values of the forward injection current and the reverse injection current. This result is based on the features of the maximum value of $\sum I_{INJ(PIN)}$ at four I/O ports of the device.
5. The input voltage of IO with analog input channel of ADC should be between VSS and VCC; otherwise, the conversion accuracy of ADC will be affected.

Table 5-2 Temperature features

Symbol	Parameters	Value	Unit
T_{STG}	Storage temperature range	-65-+150	°C
T_{Jmax}	Maximum Junction Temperature	125	°C

5.3 Operating Conditions

5.3.1 General Operating Conditions

Table 5-3 General Operating Conditions

Symbol	Parameters	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK0}	Internal APB0 clock frequency	-	0	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	48	MHz
DVCC	Digital operating voltage	-	1.8	5.5	V
AVCC ⁽¹⁾	Analog operating voltage	Must be the same as DVCC ⁽²⁾	1.8	5.5	V
T_A	Ambient temperature	-	-40	105	°C
T_J	Junction temperature range	-	-40	125	°C

**Note**

1. When using an ADC, see ADC Electrical Specifications.
2. It is recommended to use the same power supply for DVCC and AVCC, allowing a maximum of 300mV difference between DVCC and AVCC during power-up and normal operation.

5.3.2 VCAP External Capacitor

The stability of the main voltage regulator is achieved by connecting an external capacitor C_{EXT} to the VCAP pin. The specified values for C_{EXT} are detailed in the table below.

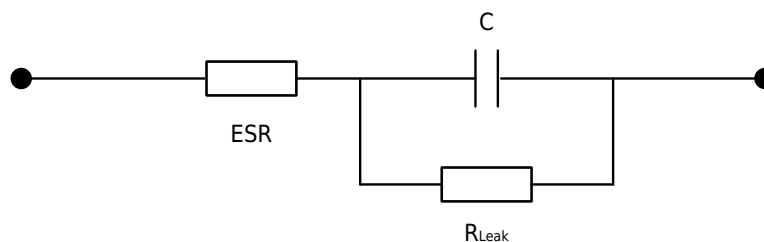


Figure 5-1 External Capacitor C_{EXT}



Note

ESR represents the equivalent series resistance.

Table 5-4 VCAP Working Conditions

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$C_{EXT}^{(1)}$	External capacitance value	-	1	-	4.7	μF
ESR ⁽²⁾	External capacitor ESR	-	-	-	100	m Ω
VCAP ⁽¹⁾	LDO supply voltage	-	1.42	1.5	1.58	V



Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.

5.3.3 Working Conditions at Power-On and Power-Down

Table 5-5 Working Conditions at Power-On and Power-Down⁽¹⁾

Symbol	Parameters	Conditions	Min	Max	Unit
S_{VCC_r}	VCC rise rate	-	0	1	V/ μs
S_{VCC_f}	VCC fall rate	-	0	0.05	V/ μs



Note

1. Resulted from comprehensive evaluation, not tested in production.

5.3.4 Embedded Reset and LVD Module Characteristics

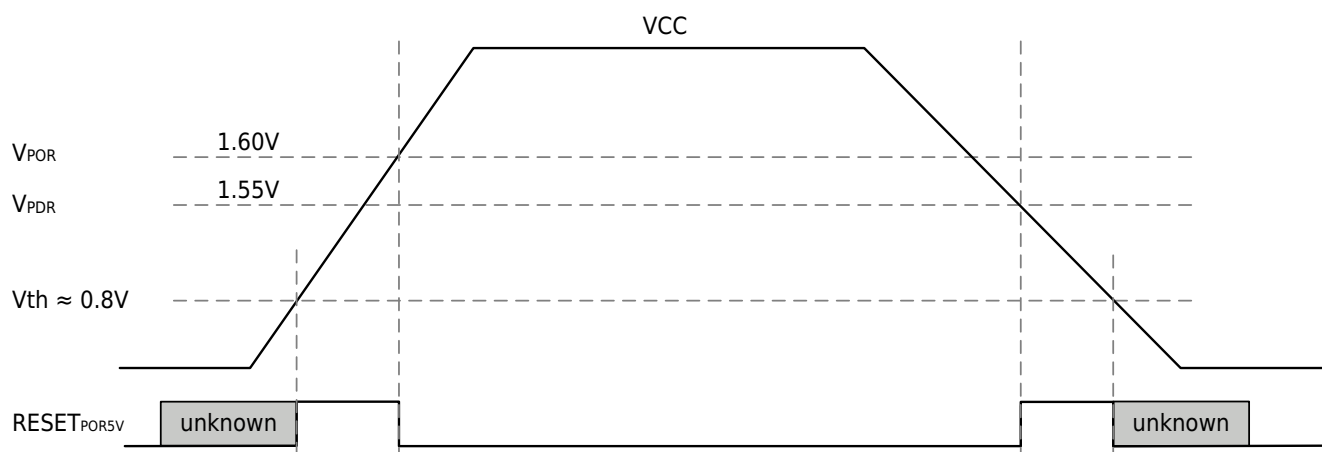


Figure 5-2 POR/PDR Schematic Diagram

Table 5-6 POR/PDR

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V _{POR}	POR release voltage (power on process)	-	1.50	1.60	1.70	V
V _{PDR}	PDR detection voltage (power down process)	-	1.40	1.55	1.65	V

Table 5-7 LVD mode features

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V _{ex}	External input voltage range	-	0	-	VCC	V
V _{level}	Detection threshold	LVD_CR.VTDS=0b0000	1.70	1.80	1.90	V
		LVD_CR.VTDS=0b0001 ⁽¹⁾	1.90	2.00	2.10	V
		LVD_CR.VTDS=0b0010 ⁽¹⁾	2.10	2.20	2.30	V
		LVD_CR.VTDS=0b0011 ⁽¹⁾	2.30	2.40	2.50	V
		LVD_CR.VTDS=0b0100 ⁽¹⁾	2.50	2.60	2.70	V
		LVD_CR.VTDS=0b0101 ⁽¹⁾	2.70	2.80	2.90	V
		LVD_CR.VTDS=0b0110 ⁽¹⁾	2.90	3.00	3.10	V
		LVD_CR.VTDS=0b0111 ⁽¹⁾	3.10	3.20	3.30	V
		LVD_CR.VTDS=0b1000	3.30	3.40	3.50	V
		LVD_CR.VTDS=0b1001 ⁽¹⁾	3.45	3.60	3.75	V
		LVD_CR.VTDS=0b1010 ⁽¹⁾	3.65	3.80	3.95	V
		LVD_CR.VTDS=0b1011 ⁽¹⁾	3.85	4.00	4.15	V
		LVD_CR.VTDS=0b1100 ⁽¹⁾	4.05	4.20	4.35	V
		LVD_CR.VTDS=0b1101 ⁽¹⁾	4.25	4.40	4.55	V
		LVD_CR.VTDS=0b1110 ⁽¹⁾	4.45	4.60	4.75	V

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{level}	Detection threshold	LVD_CR.VTDS=0b1111	4.65	4.80	4.95	V
I_{comp}	Power consumption	-	-	0.20	-	μA
$T_{response}$	Response time	Choose to detect the GPIO pin voltage, VCC=3.3V, LVD_CR.VTDS= 0b1000, the detection voltage changes from ($V_{level}+100mV$) to ($V_{level}-100mV$), and the change slope is $2 \times 10^5 V/\mu s$	-	90	-	μs
T_{setup}	Settling time	Choose to detect the GPIO pin voltage, VCC=3.3V, LVD_CR.VTDS= 0b1000, the detection voltage is lower than $V_{level} 100mV$	-	400	600	μs
V_{hys}	Hysteresis voltage	-	-	60	-	mV
T_{filter}	Filter time	LVD_CR.DEBOUNCE_TIME=0b0000	-	0	-	μs
		LVD_CR.DEBOUNCE_TIME=0b0001	-	$2 * T_{LVD}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b0010	-	$4 * T_{LVD}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b0011	-	$8 * T_{LVD}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b0100	-	$16 * T_{LVD}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b0101	-	$32 * T_{LVD}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b0110	-	$64 * T_{LVD}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b0111	-	$128 * T_{LVD}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b1000	-	$256 * T_{LVD}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b1001	-	$512 * T_{LVD}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b1010	-	$1024 * T_{LVD}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b1011	-	$2048 * T_{LVD}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b1100	-	$4096 * T_{LVD}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b1101	-	$4096 * T_{LVD}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b1110	-	$4096 * T_{LVD}$	-	μs
		LVD_CR.DEBOUNCE_TIME=0b1111	-	$4096 * T_{LVD}$	-	μs

**Note**

1. Resulted from comprehensive evaluation, not tested in production.
2. T_{LVD} represents the filter clock period, with the filter clock approximately 256kHz.

5.3.5 Built-In Reference Voltage

Table 5-8 Built-In Reference Voltage

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{REF25}^{(2)}$	Internal 2.5V reference voltage	$V_{CC}=3.3V$ $T_A=25^{\circ}C$	2.480	2.5	2.520	V
		$V_{CC}=2.8-5.5V$ $T_A=-40-105^{\circ}C$	2.455 ⁽¹⁾	2.5	2.545 ⁽¹⁾	V
V_{REF15}	Internal 1.5V reference voltage	$V_{CC}=3.3V$ $T_A=25^{\circ}C$	1.488	1.5	1.512	V
		$V_{CC}=1.8-5.5V$ $T_A=-40-105^{\circ}C$	1.473 ⁽¹⁾	1.5	1.527 ⁽¹⁾	V
$T_{Coeff}^{(3)}$	Temperature coefficient of internal 1.5/2.5V reference voltage	$T_A=-40-105^{\circ}C$	-	-	120	ppm/ $^{\circ}C$
$T_{stable(BGR)}^{(3)}$	BGR voltage stability time	-	-	30	-	μs
$T_{stable(REFBUF)}^{(3)}$	Internal reference voltage buffer settling time	-	-	-	1	μs
$I_{REFBUF}^{(3)}$	Internal reference voltage buffer current consumption	-	-	460	-	μA



Note

1. Resulted from comprehensive evaluation, not tested in production.
2. The 2.5V range can only be selected when the power supply voltage exceeds 2.8V, otherwise it may cause system malfunction.
3. Guaranteed by design, not tested in production.

5.3.6 Supply Current Characteristics

Current consumption is a comprehensive index of multiple parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin flip rate, and the location of the program in memory and the executed code, etc.

The MCU is in the following conditions:

- All I/O pins are in input mode and connected to a static level-VCC or VSS (no load).
- All peripherals are turned off, unless otherwise specified.
- The access time of the flash memory is adjusted to the frequency f_{HCLK} (0 wait cycle for 0-24MHz, 1 wait cycle for 24-48MHz)
- When peripherals is used: $f_{PCLK0}=f_{HCLK}$, $f_{PCLK1}=f_{HCLK}$.

Table 5-9 Operating Current Characteristics⁽³⁾

Symbol	Parameters	Conditions		Typ ⁽¹⁾	Max ⁽²⁾	Unit
				25°C	105°C	
I _{DD} (Run in RAM)	All peripherals clock ON, Run while(1) in RAM	RCH clock source	4M	865.6	-	μA
			6M	1209.1	-	μA
			32M	3604.5	-	μA
			48M	5246.3	-	μA
		XTH clock source	24M	3290.1	-	μA
	All peripherals clock OFF, Run while(1) in RAM	RCH clock source	4M	638.9	-	μA
			6M	868.8	-	μA
			32M	1783.9	-	μA
			48M	2519.8	-	μA
		XTH clock source	24M	1924.3	-	μA
I _{DD} (Run CoreMark)	All peripherals clock OFF, Run CoreMark in Flash	RCH clock source	4M	805.2	-	μA
			6M	1085.6	-	μA
			32M	2335.9	-	μA
			48M	3336.9	-	μA
		XTH clock source	24M	2529.6	-	μA
I _{DD} (Run mode)	All peripherals clock ON, Run while(1) in Flash	RCH clock source	4M	863.0	1129.4	μA
			6M	1204.9	1584.2	μA
			32M	3545.4	4354.2	μA
			48M	5157.8	6314.5	μA
		XTH clock source	24M	3230.5	4297.3	μA
	All peripherals clock OFF, Run while(1) in Flash	RCH clock source	4M	636.4	857.9	μA
			6M	864.7	1174.6	μA
			32M	1725.7	2155.4	μA
			48M	2432.9	3017.9	μA
		XTH clock source	24M	1866.0	2655.1	μA
I _{DD} (Sleep mode)	All peripherals clock ON	RCH clock source	4M	473.1	612.1	μA
			6M	633.0	806.5	μA
			32M	2748.8	3379.1	μA
			48M	4024.9	4931.8	μA
		XTH clock source	24M	2455.2	3343.7	μA
	All peripherals clock OFF	RCH clock source	4M	245.6	335.9	μA
			6M	291.8	391.8	μA
			32M	924.0	1165.3	μA
			48M	1291.6	1612.7	μA
		XTH clock source	24M	1087.0	1681.9	μA
I _{DD} (LP Run)	All peripherals clock ON, Run while(1) in Flash	32K clock source	RCL32K	95.8	136.2	μA
			XTL32K, Driver=2	96.3	136.2	μA
	All peripherals clock OFF, Run while(1) in Flash	32K clock source	RCL32K	93.9	133.8	μA
			XTL32K, Driver=2	94.5	134.8	μA
I _{DD} (LP Sleep)	All peripherals clock ON,	32K clock source	RCL32K	84.0	119.8	μA
			XTL32K, Driver=2	84.5	119.0	μA
	All peripherals clock OFF,	32K clock source	RCL32K	82.1	117.5	μA
			XTL32K, Driver=2	82.6	116.8	μA

Symbol	Parameters	Conditions	Typ ⁽¹⁾	Max ⁽²⁾	Unit
			25°C	105°C	
I _{DD} (Deep-Sleep)	All peripherals clock OFF	NO CLK	0.65	8.4	μA
		RCL32K	0.95	8.7	μA
		XTL32K	1.50	9.5	μA
	Other peripherals clock OFF	NO CLK+IWDT	0.70	8.4	μA
		RCL32K+RTC	0.95	8.8	μA
		RCL32K+LPUART	1.00	8.9	μA
		RCL32K+LPTimer	1.00	8.8	μA
		XTL32K+RTC	1.50	9.5	μA
		XTL32K+LPUART	1.51	9.6	μA
		XTL32K+LPTimer	1.50	9.5	μA
		XTL32K+RTC+IWDT+LVD	1.81	10.2	μA

**Note**

1. Unless otherwise specified, typical values are measured at V_{CC}=3.3V and V_{CAP}=1.5V.
2. Unless otherwise specified, maximum values are measured across the full operating voltage range of V_{CC} with V_{CAP}=1.5V.
3. Resulted from comprehensive evaluation, not tested in production.

5.3.7 Time to Wake-Up from Low-Power Mode

The wake-up time is measured during the wake-up phase of the RCH oscillator. The clock source used when waking up depends on the current operating mode:

- Sleep mode: clock source is RCH oscillator
- DeepSleep mode: clock source is RCH oscillator

Table 5-10 Wake-Up Time Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
T _{wu} ⁽¹⁾	Sleep mode Wake-up Time	-	-	1.8	-	μs
	DeepSleep mode wake-up time	F _{RCH} =4MHz	-	13	-	μs
		F _{RCH} =6MHz	-	13	-	μs
		F _{RCH} =32MHz	-	7	-	μs
		F _{RCH} =48MHz	-	7	-	μs

**Note**

1. Guaranteed by design, not tested in production.
2. The wake-up time is measured from the start of the wake-up event to the user program reading the first instruction.

5.3.8 External Clock Source Characteristics

5.3.8.1 External Input High-Speed Clock

Table 5-11 External Input High-Speed Clock Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{EXTH}	User External clock frequency	-	-	8	32	MHz
V_{EXTHH}	Input pin high level voltage	-	0.7VCC	-	VCC	V
V_{EXTHL}	Input pin low level voltage	-	VSS	-	0.3VCC	V
$T_{\text{r(EXTH)}}$	Rise time	-	-	-	20	ns
$T_{\text{f(EXTH)}}$	Falling time	-	-	-	20	ns
$T_{\text{w(EXTH)}}$	Enter high or low time	-	16	-	-	ns
$C_{\text{in(EXTH)}}$	Input Capacitance	-	-	5	-	pF
Duty	Duty cycle	-	40	-	60	%
I_{L}	Input leakage current	-	-	-	±1	μA



Note

1. Guaranteed by design, not tested in production.

5.3.8.2 External Input Low-Speed Clock

Table 5-12 External Input Low-Speed Clock Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{EXTL}	User External clock frequency	-	-	32.768	1000	kHz
V_{EXTLH}	Input pin high level voltage	-	0.7VCC	-	VCC	V
V_{EXTLL}	Input Pin Low Voltage	-	VSS	-	0.3VCC	V
$T_{\text{r(EXTL)}}$	Rise time	-	-	-	50	ns
$T_{\text{f(EXTL)}}$	Falling time	-	-	-	50	ns
$T_{\text{w(EXTL)}}$	Enter high or low time	-	450	-	-	ns
$C_{\text{in(EXTL)}}$	Input Capacitance	-	-	5	-	pF
Duty	Duty cycle	-	30	-	70	%
I_{L}	Input leakage current	-	-	-	±1	μA



Note

1. Guaranteed by design, not tested in production.

5.3.8.3 External High-Speed Crystal XTH

The external high-speed crystal (XTH) can be generated using a 8-32MHz crystal/ceramic resonator oscillator. The information given in this section is based on the results obtained through comprehensive

characteristic evaluation using the typical external components listed in the table below. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and settling time at startup. For detailed parameters (frequency, package, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Table 5-13 External High-Speed Crystal XTH Characteristics⁽¹⁾⁽²⁾

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
F_{CLK}	Oscillator frequency	-	8	-	32	MHz
ESR_{CLK}	Supported crystal oscillator ESR range	32MHz	-	-	60	Ω
		24MHz	-	-	90	
		16MHz	-	-	120	
		8MHz	-	-	150	
$C_{Lx}^{(3)}$	Matching Capacitance	Configure as required by the crystal manufacturer.	4	12	20	pF
Duty	Duty cycle	-	40	50	60	%
$I_{dd}^{(4)}$	Electrorheograph	XTH_CR[3:0]=0b1111	-	1630	-	μA
		XTH_CR[3:0]=0b1110	-	1020	-	
		XTH_CR[3:0]=0b1010	-	650	-	
		XTH_CR[3:0]=0b0110	-	500	-	
		XTH_CR[3:0]=0b0010	-	280	-	
g_m	Transconductance	XTH_CR[3:0]=0b1111	-	11.3	-	mA/V
		XTH_CR[3:0]=0b1110(32MHz, 24MHz recommended value)	-	6.35	-	
		XTH_CR[3:0]=0b1101	-	4.44	-	
		XTH_CR[3:0]=0b1100	-	3.42	-	
		XTH_CR[3:0]=0b1011	-	7.12	-	
		XTH_CR[3:0]=0b1010(16MHz recommended value)	-	4.00	-	
		XTH_CR[3:0]=0b1001	-	2.79	-	
		XTH_CR[3:0]=0b1000	-	2.15	-	
		XTH_CR[3:0]=0b0111	-	5.44	-	
		XTH_CR[3:0]=0b0110(12MHz recommended value)	-	3.06	-	
		XTH_CR[3:0]=0b0101	-	2.14	-	
		XTH_CR[3:0]=0b0100	-	1.65	-	
		XTH_CR[3:0]=0b0011	-	2.51	-	
		XTH_CR[3:0]=0b0010(8MHz recommended value)	-	1.41	-	
		XTH_CR[3:0]=0b0001	-	1.00	-	
		XTH_CR[3:0]=0b0000	-	0.76	-	

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$T_{\text{start}}^{(5)}$	Start time	32MHz, $C_{Lx}=16\text{pF}$ @ $XTH_CR[3:0]=0b1110$	-	500	-	μs
		8MHz, $C_{Lx}=16\text{pF}$ @ $XTH_CR[3:0]=0b0010$	-	1.5	-	ms

**Note**

1. The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.
2. Resulted from comprehensive evaluation, not tested in production.
3. C_{Lx} refers to the two pin matching capacitors C_{L1} and C_{L2} of the crystal. It is recommended to use high-quality ceramic capacitors, and select a crystal or resonator that meets the requirements. Usually C_{L1} and C_{L2} have the same parameters. When selecting C_{Lx} , one should take into account parameters such as the crystal oscillator's frequency and ESR, as well as the total parasitic capacitance to ground (C_p) from the PCB and MCU pins.

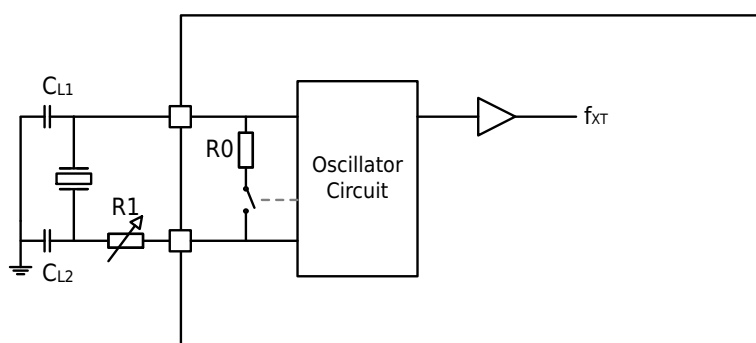
The C_{Lx} is recommended to be configured in accordance with the requirements of the crystal manufacturer's technical manual.

- If the crystal manufacturer gives *the value of the load capacitance* (C_L), the matching capacitance $C_{Lx} = 2 * C_L - C_p$.
- If the crystal manufacturer gives *the value of the matching capacitance*, the matching capacitance $C_{Lx} = \text{matching capacitance value} - C_p$.

In practical applications, if a larger C_{Lx} is selected, it is recommended to choose an appropriate current level setting.

Example:

- When the crystal manufacturer gives the load capacitance of the crystal as 8pF, considering the distributed capacitance between the PCB and MCU pins, it is recommended to choose a matching capacitor with a capacitance of 12pF.
 - When the crystal manufacturer gives the matching capacitance of the crystal as 12pF, considering the distributed capacitance between the PCB and MCU pins, it is recommended to choose a matching capacitor with a capacitance of 10pF or 8pF.
4. Current varies with frequency and drive capability selection. Higher frequencies result in stronger drive capability but greater current consumption.
 5. T_{start} represents the startup time, measured from when software enables XTH until a stable output clock signal is obtained. This value is measured using a standard crystal resonator with the $XTH_CR[5:4]=0b10$ setting. It may vary greatly depending on the crystal manufacturer and model.



**Note**

- The feedback resistance R0 has been integrated in the chip.
- The damping resistance R1 is optional, and the value of the resistance depends on the default is 0Ω.

5.3.8.4 External Low-Speed Crystal XTL

The external low-speed crystal (XTL) can be generated using a 32.768kHz crystal/ceramic resonator oscillator. The information given in this section is based on typical external components and the results obtained through comprehensive characteristic evaluation. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and settling time at startup. For detailed parameters (frequency, package, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Table 5-14 External Low-Speed Crystal XTL Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
F_{CLK}	Oscillator frequency	-	-	32.768	-	kHz
ESR_{CLK}	Supported crystal oscillator ESR range	-	-	-	60	kΩ
$C_{Lx}^{(2)}$	Matching capacitance	Configure as required by the crystal manufacturer.	4	12	20	pF
DC_{ACLK}	Duty cycle	-	30	50	70	%
$I_{dd}^{(3)}$	Electrorheograph	XTL_CR[3:0]=0b1111	-	1330	-	nA
		XTL_CR[3:0]=0b1011	-	1230	-	
		XTL_CR[3:0]=0b0111	-	1140	-	
		XTL_CR[3:0]=0b0011	-	1050	-	
		XTL_CR[3:0]=0b1110	-	630	-	
		XTL_CR[3:0]=0b1010	-	580	-	
		XTL_CR[3:0]=0b0110	-	530	-	
		XTL_CR[3:0]=0b0010	-	490	-	
		XTL_CR[3:0]=0b1101	-	400	-	
		XTL_CR[3:0]=0b1001(Recommended value)	-	370	-	
		XTL_CR[3:0]=0b0101	-	350	-	
		XTL_CR[3:0]=0b0001	-	310	-	
		XTL_CR[3:0]=0b1100	-	290	-	
		XTL_CR[3:0]=0b1000	-	270	-	
		XTL_CR[3:0]=0b0100	-	250	-	
		XTL_CR[3:0]=0b0000	-	230	-	
g_m	Transconductance	XTL_CR[3:0]=0b1111	-	14.64	-	μA/V
		XTL_CR[3:0]=0b1011	-	13.17	-	
		XTL_CR[3:0]=0b0111	-	11.67	-	
		XTL_CR[3:0]=0b0011	-	10.15	-	

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
g_m	Transconductance	$XTL_CR[3:0]=0b1110$	-	7.37	-	$\mu A/V$
		$XTL_CR[3:0]=0b1010$	-	6.62	-	
		$XTL_CR[3:0]=0b0110$	-	5.87	-	
		$XTL_CR[3:0]=0b0010$	-	5.10	-	
		$XTL_CR[3:0]=0b1101$	-	4.94	-	
		$XTL_CR[3:0]=0b1001$ (Recommended value)	-	4.44	-	
		$XTL_CR[3:0]=0b0101$	-	3.93	-	
		$XTL_CR[3:0]=0b0001$	-	3.41	-	
		$XTL_CR[3:0]=0b1100$	-	3.72	-	
		$XTL_CR[3:0]=0b1000$	-	3.34	-	
		$XTL_CR[3:0]=0b0100$	-	2.95	-	
		$XTL_CR[3:0]=0b0000$	-	2.57	-	
$T_{start}^{(4)}$	Start time	ESR=30k Ω $C_{Lx}=12pF$ $XTL_CR[3:0]=0b1001$	-	2000	-	ms

**Note**

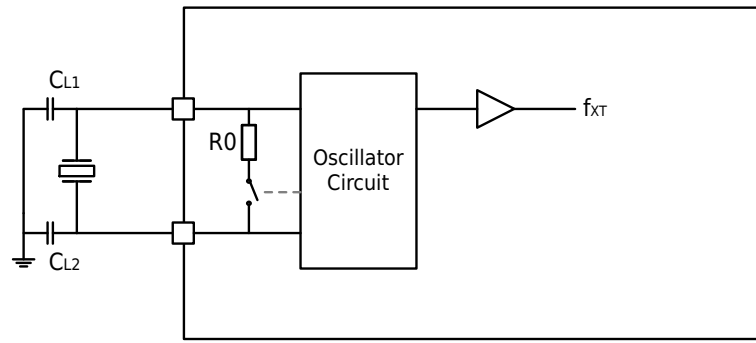
1. Resulted from comprehensive evaluation, not tested in production.
2. C_{Lx} refers to the two pin matching capacitors C_{L1} and C_{L2} of the crystal. It is recommended to use high-quality ceramic capacitors, and select a crystal or resonator that meets the requirements. Usually C_{L1} and C_{L2} have the same parameters. When selecting C_{Lx} , one should take into account parameters such as the crystal oscillator's frequency and ESR, as well as the total parasitic capacitance to ground (C_p) from the PCB and MCU pins.

The C_{Lx} is recommended to be configured in accordance with the requirements of the crystal manufacturer's technical manual.

- If the crystal manufacturer gives *the value of the load capacitance* (C_L), the matching capacitance $C_{Lx} = 2 * C_L - C_p$.
- If the crystal manufacturer gives *the value of the matching capacitance*, the matching capacitance $C_{Lx} = \text{matching capacitance value} - C_p$.

In practical applications, if a larger C_{Lx} is selected, it is recommended to choose an appropriate current level setting.

3. Choose a high-quality oscillator with a small ESR value, and you can optimize the current consumption by adjusting $XTL_CR[3:0]$ setting value. Current consumption is proportional to the transconductance (g_m) provided by the circuit.
4. T_{start} represents the startup time, measured from when software enables XTL until a stable output clock signal is obtained. This value is measured using a standard crystal resonator with the settings $XTL_CR[3:0]=0b1001$ and $XTL_CR[5:4]=0b11$. It may vary greatly depending on the crystal manufacturer and model.

**Note**

- The feedback resistance $R0$ has been integrated in the chip.

5.3.9 Internal Clock Source Characteristics

5.3.9.1 RCH

Table 5-15 Internal High-Speed Clock RCH Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
F_{CLK}	Oscillator frequency	-	4.0	4.0 6.0 32.0 48.0	48.0	MHz
TRIM ⁽¹⁾	User-adjustable frequency step size	-	-	0.12	-	%
Dev ⁽¹⁾	Oscillation frequency range under different temperatures and VCC conditions	$V_{CC}=1.8-5.5V$ $T_A=-40-105^{\circ}C$	-1.5	-	1.5	%
		$V_{CC}=1.8-5.5V$ $T_A=-20-75^{\circ}C$	-1.0	-	1.0	%
		$V_{CC}=3.3V$ $T_A=25^{\circ}C$	-0.3	-	0.3	%
$I_{CLK}^{(2)}$	Power consumption	$F_{CLK}=4MHz$	-	60	-	μA
		$F_{CLK}=6MHz$	-	66	-	μA
		$F_{CLK}=32MHz$	-	177	-	μA
		$F_{CLK}=48MHz$	-	222	-	μA
$DC_{CLK}^{(2)}$	Duty cycle	-	45	50	55	%
$t_{su}^{(2)}$	Startup time (from enable to clock output initiation)	$F_{CLK}=4MHz$	-	8.8	20.1	μs
		$F_{CLK}=6MHz$	-	8.5	19.8	μs
		$F_{CLK}=32MHz$	-	4.7	12.9	μs
		$F_{CLK}=48MHz$	-	4.7	12.8	μs

**Note**

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.

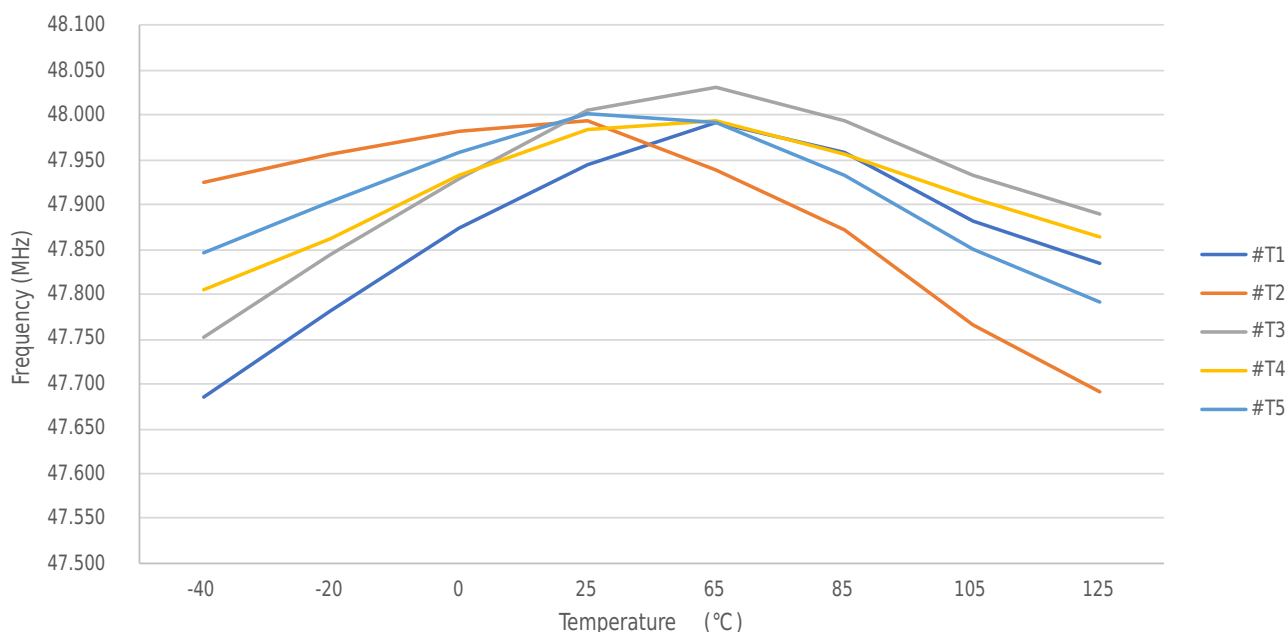


Figure 5-5 RCH Clock Frequency Variation Curve ($F_{CLK}=48\text{MHz}$, $V_{CC}=3.3\text{V}$)

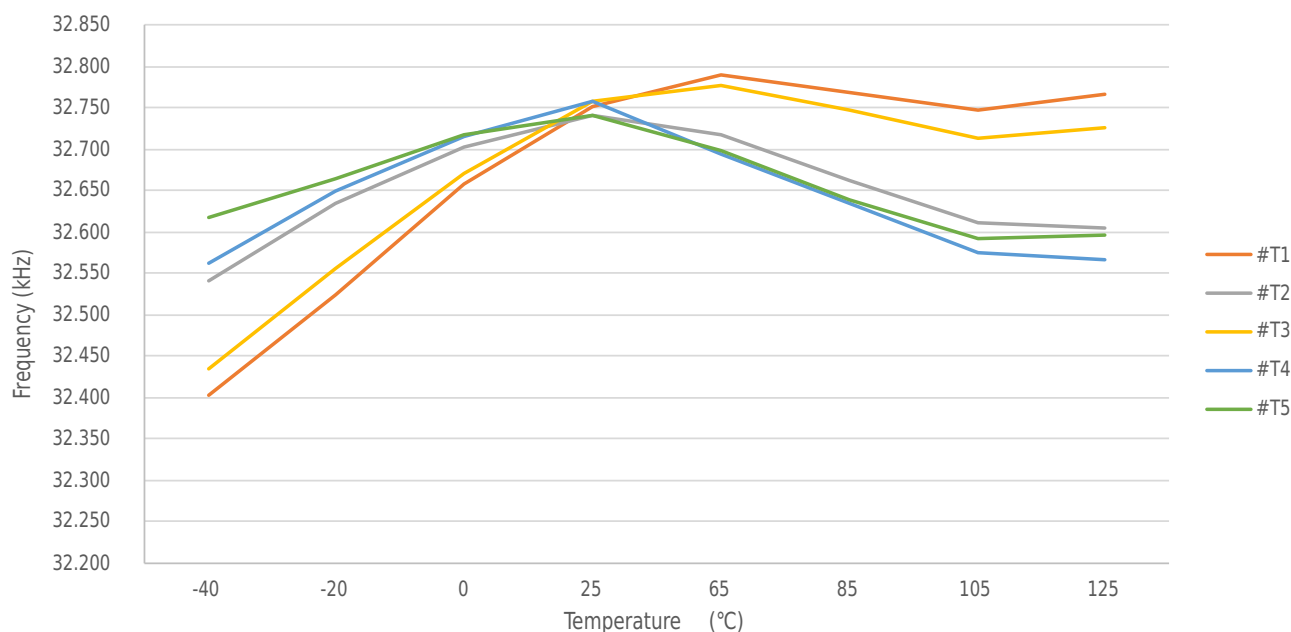
5.3.9.2 RCL

Table 5-16 Internal Low-Speed Clock RCL Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$F_{CLK}^{(1)}$	Oscillator frequency	$V_{CC}=3.3\text{V}$ $T_A=25^\circ\text{C}$	-	38.4 32.768	-	kHz
TRIM ⁽²⁾	User-adjustable frequency step size	-	-	0.5	-	%
Dev ⁽²⁾⁽³⁾	RCL oscillator accuracy@HPM	$V_{CC}=1.8\text{-}5.5\text{V}$ $T_A=-40\text{-}105^\circ\text{C}$	-2.5	-	2.5	%
	RCL oscillator accuracy@LPM		-10	-	10	%
$T_{CLK}^{(2)}$	Start time	-	-	150	-	μs
$DC_{CLK}^{(2)}$	Duty cycle	-	25	-	75	%

**Note**

1. RCL has two frequency points: 38.4 kHz and 32.768 kHz.
2. Resulted from comprehensive evaluation, not tested in production.
3. The HPM or LPM mode can be selected through register configuration. For detailed information, please refer to the "RCL Control Register (RCL_CR)" register of "System Controller (SYSCTRL)" chapter in the "Reference Manual".

Figure 5-6 RCL@HPM Mode Clock Frequency Variation Curve ($F_{CLK}=32.768\text{kHz}$, $V_{CC}=3.3\text{V}$)

5.3.9.3 RC10K

Table 5-17 Internal Low-Speed Clock RC10K Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Dev ⁽¹⁾	Oscillator accuracy	$V_{CC}=1.8\text{-}5.5\text{V}$ $T_A=-20\text{-}50^\circ\text{C}$	-50	-	80	%
F_{CLK}	Oscillator frequency	$V_{CC}<3.3\text{V}$ $T_A=25^\circ\text{C}$	-	10	-	kHz



Note

1. Resulted from comprehensive evaluation, not tested in production.

5.3.9.4 RC256K

Table 5-18 Internal Low-Speed Clock RC256K Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
F_{CLK}	Oscillator frequency	$V_{CC}=3.3\text{V}$ $T_A=25^\circ\text{C}$	-	256	-	kHz
Dev ⁽¹⁾	Oscillator accuracy	$V_{CC}=1.8\text{-}5.5\text{V}$ $T_A=-40\text{-}105^\circ\text{C}$	-5.5	-	5.5	%
DC _{CLK} ⁽¹⁾	Duty cycle	-	40	-	60	%



Note

1. Resulted from comprehensive evaluation, not tested in production.

5.3.10 Memory Characteristics

Table 5-19 Memory Characteristics

Symbol	Parameters	Conditions		Min	Typ	Max	Unit
EC _{FLASH}	Program, Sector Erase times	T _A =-40°C -105°C	Data Storage Period (RET _{FLASH}): 10 years, T _A =85°C	-	100000	-	time s
			Data Storage Period (RET _{FLASH}): 20 years, T _A =85°C	20000	-	-	time s
T _{b_prog}	Programming time (bytes)	-		22	-	30	μs
T _{w_prog}	Programming time (words)	-		40	-	52	μs
T _{p_erase}	Page erase time	-		2	-	3	ms
T _{m_erase}	Full chip erase time	-		30	-	40	ms

5.3.11 ESD Characteristics

Using specific measurement methods, the chip is subjected to strength testing to determine its electrical sensitivity performance.

Table 5-20 ESD Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
VESD _{HBM}	ESD@Human body model	T _A =25℃, in line with AN-SI/ESDA/JEDEC JS-001	-6	-	6	kV
VESD _{CDM}	ESD@charged device model	T _A =25℃, in line with AN-SI/ESDA/JEDEC JS-002	-1.5	-	1.5	kV
I _{latchup}	Latch current	T _A =105℃, in line with JESD78	-200	-	200	mA



Note

1. Resulted from comprehensive evaluation, not tested in production.

5.3.12 I/O Port Characteristics

5.3.12.1 Output Characteristics-Port

Table 5-21 Port Output Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Max	Unit
V _{OH}	IO pin output high level (low drive)	I _{IO} =3mA, VCC=3.3V	VCC-0.3	-	V
		I _{IO} =6mA, VCC=3.3V	VCC-0.7	-	V
V _{OL}	IO pin output low level (low drive)	I _{IO} =4mA, VCC=3.3V	-	VSS+0.3	V
		I _{IO} =8mA, VCC=3.3V	-	VSS+0.7	V

Symbol	Parameters	Conditions	Min	Max	Unit
V_{OH}	IO pin output high level (strong drive)	$I_{IO}=6\text{mA}$, $V_{CC}=3.3\text{V}$	$V_{CC}-0.3$	-	V
		$I_{IO}=12\text{mA}$, $V_{CC}=3.3\text{V}$	$V_{CC}-0.7$	-	V
V_{OL}	IO pin output low level (strong drive)	$I_{IO}=8\text{mA}$, $V_{CC}=3.3\text{V}$	-	$V_{SS}+0.3$	V
		$I_{IO}=16\text{mA}$, $V_{CC}=3.3\text{V}$	-	$V_{SS}+0.7$	V

**Note**

1. Resulted from comprehensive evaluation, not tested in production.
2. The device's I_{IO} current must always comply with the absolute maximum ratings specified in the [Table 5-1 : Voltage and Current Characteristics](#), and the sum of I_{IO} (I_{OH} and I_{OL} of I/O ports) must not exceed I_{VCC} .

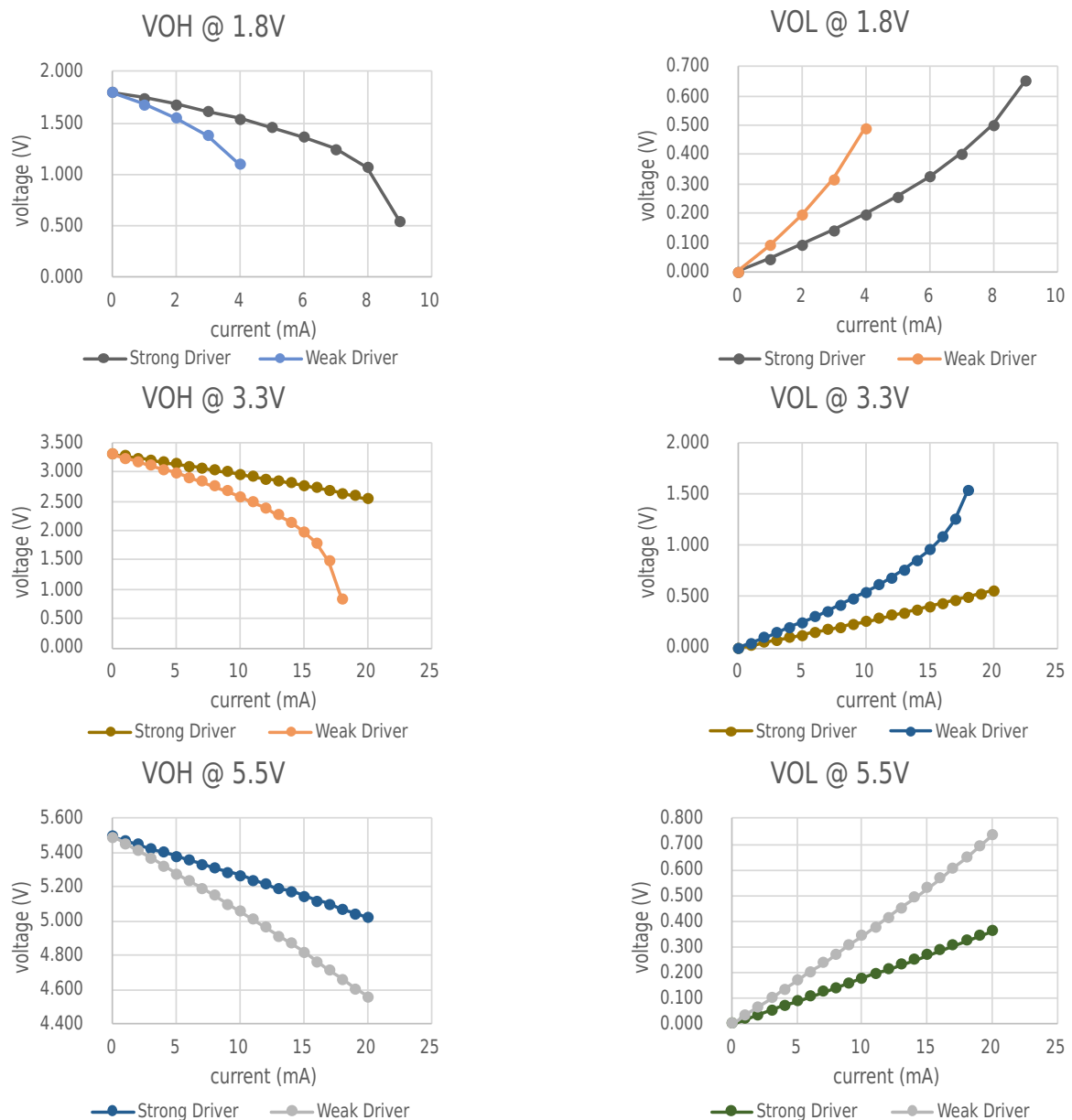


Figure 5-7 Measured VOH/VOL Output Port Curves (Typical Values)

5.3.12.2 Input Characteristics-PA/PB/PC/PD Port

Table 5-22 Port Input Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high-level voltage	-	0.7VCC	-	-	V
V_{IL}	Input low-level voltage	-	-	-	0.3VCC	V
V_{hys}	Schmitt trigger input voltage hysteresis($V_{IH}-V_{IL}$)	VCC=1.8V	-	0.3	-	V
		VCC=3.3V	-	0.4	-	V
		VCC=5.5V	-	0.6	-	V
$R_{pullhigh}$	Weak pull-up equivalent resistance	Weak pull-up enable VCC=3.3V	-	60	-	k Ω
$R_{pulllow}$	Weak pull-down equivalent resistance	Weak pull-down enable VCC=3.3V	-	60	-	k Ω
C_{input}	Input equivalent capacitance	-	-	5	-	pF

**Note**

1. Resulted from comprehensive evaluation, not tested in production.

Table 5-23 PA12/PA11/PB09/PB05/PC01/PC00/PD05/PD02 Input Level Low Voltage Recognition Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high-level voltage ⁽²⁾	-	0.7VCAP	-	-	V
V_{IL}	Input low-level voltage ⁽²⁾	-	-	-	0.3VCAP	V

**Note**

1. Guaranteed by design, not tested in production.
2. This level recognition feature is exclusively used for I2C communication and is unrelated to the input characteristics of GPIO ports.

5.3.12.3 Port External Input Sampling Requirements-Timer Gate/Timer Clock

Table 5-24 Port External Input Sampling Requirements

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$t_{(cap)}$	Timer capture timing	Timer capture pulse width	-	0.5	-	μ s
$t_{(clk)}^{(1)}$	Timer clock frequency applied to pin	Timer external clock input $f_{HCLK}=4\text{MHz}$	-	-	PCLK/2	MHz

**Note**

1. Resulted from comprehensive evaluation, not tested in production.

5.3.12.4 Port Leakage Characteristics-PA/PB/PC/PD Port

Table 5-25 Port Leakage Characteristics⁽¹⁾⁽²⁾

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$I_{lkg}(P_{x,y})$	Leakage current	$V_{(P_{x,y})}$	-	± 50	-	nA



Note

1. The port leakage is based on the corresponding port being connected to VSS or VCC.
2. The port must be configured as an input port.

5.3.13 RESETB Pin Characteristics

The RESETB pin input driver uses CMOS technology, which is connected with a pull-up resistor that cannot be disconnected.

Table 5-26 RESETB Pin Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{IL}(\text{RESETB})$	Input low-level voltage	-	-0.3	-	0.3VCC	V
$V_{IH}(\text{RESETB})$	Input high-level voltage	-	0.7VCC	-	VCC+0.3	V
$V_{hys}(\text{RESETB})$	Schmitt trigger voltage hysteresis	-	-	0.1VCC	-	mV
R_{PU}	Weak pull-up equivalent resistance	$V_{IN}=V_{SS}$	-	60	-	k Ω
$T_F(\text{RESETB})$	Filtered input pulse	-	-	-	1	μ s
$T_{NF}(\text{RESETB})$	Non-filtered input pulse	-	5	-	-	μ s



Note

1. Guaranteed by design, not tested in production.

5.3.14 ADC Characteristics

Table 5-27 ADC Characteristics

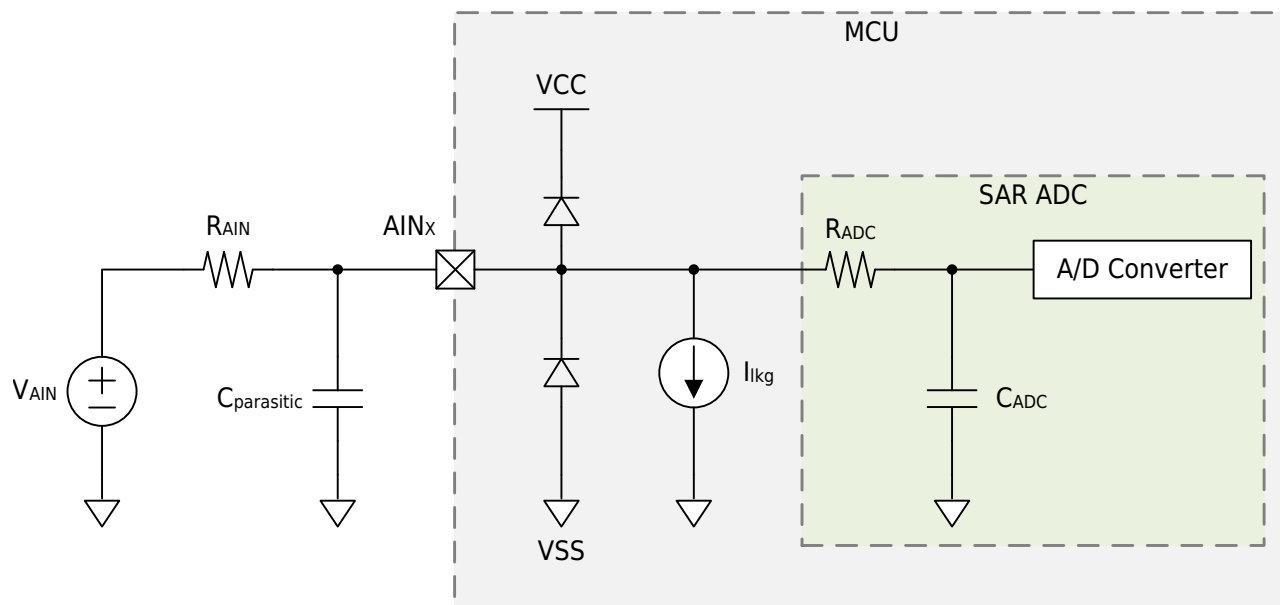
Symbol	Parameters	Conditions	Min	Typ	Max	Unit
AVCC	Analog supply voltage	-	1.8	3.3	5.5	V
V_{AIN}	ADC Input Voltage Range	Single-ended input mode	0	-	V_{REF+}	V
$V_{REF+}^{(1)}$	Positive reference voltage	-	1.5	-	AVCC	V
V_{REF-}	Negative reference voltage	-	-	AVSS	-	V
$DEV_{AVCC/3}^{(2)}$	AVCC/3 accuracy	-	-3.5	± 2	3.5	%
$V_{BUF}^{(1)}$	External input voltage range for which both the input buffer and ADC can guarantee accuracy	$(AVCC-0.2V) < V_{REF+}$	0.2	-	AVCC-0.2	V
		$(AVCC-0.2V) \geq V_{REF+}$	0.2	-	V_{REF+}	V

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{OSBUF}^{(2)}$	Input equivalent offset voltage of the input buffer	Input voltage within the range specified by V_{BUF}	-12	-	12	mV
$I_{ADC}^{(1)}$	Operating Current Consumption	$V_{REF+}=AVCC/EXVREF$ $f_s=1\text{Msps}$	-	0.24	-	mA
		$V_{REF+}=AVCC/EXVREF$ $f_s=2\text{Msps}$	-	0.40	-	mA
$I_{BUF}^{(1)}$	Input buffer current consumption	-	-	0.49	-	mA
$C_{ADC}^{(1)}$	ADC internal sampling capacitor	-	-	5	-	pF
$C_{BUF}^{(1)}$	Input Capacitance of Buffer Amplifier	-	-	1	-	pF
$R_{ADC}^{(1)}$	ADC internal sampling resistor	Not use input Buffer Amplifier	-	1.5	-	k Ω
		Use input Buffer Amplifier	-	4.5	-	k Ω
$R_{AIN}^{(1)(5)}$	ADC external input impedance	Not use input Buffer Amplifier $T_j=125^\circ\text{C}$	-	-	1.5	k Ω
		Use input Buffer Amplifier $T_j=125^\circ\text{C}$	-	-	10	k Ω
$f_{ADCCLK}^{(1)}$	ADC clock frequency	$2.7\text{V}\leq AVCC\leq 5.5\text{V}$ $V_{REF+}=AVCC/EXVREF$	0.3	-	32	MHz
		$2.4\text{V}\leq AVCC<2.7\text{V}$ $V_{REF+}=AVCC/EXVREF$	0.3	-	8	
		$1.8\text{V}\leq AVCC<2.4\text{V}$ $V_{REF+}=AVCC/EXVREF$	0.3	-	4	
		$V_{REF+}=\text{built-in } 1.5\text{V}/2.5\text{V}$	0.3	-	4	
$f_s^{(1)}$	Sampling rate	$2.7\text{V}\leq AVCC\leq 5.5\text{V}$ $V_{REF+}=AVCC/EXVREF$ Select sampling channel AIN0 Not use input Buffer Amplifier	0.02	-	2	Msps
		$2.7\text{V}\leq AVCC\leq 5.5\text{V}$ $V_{REF+}=AVCC/EXVREF$ Select sampling channel other than AIN0 Not use input Buffer Amplifier	0.02	-	1	

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$f_s^{(1)}$	Sampling rate	$2.4V \leq AVCC < 2.7V$ $V_{REF+} = AVCC/EXVREF$ Not use input Buffer Amplifier	0.02	-	0.5	MSPS
		$1.8V \leq AVCC < 2.4V$ $V_{REF+} = AVCC/EXVREF$ Not use input Buffer Amplifier	0.02	-	0.25	
		$2.8V \leq AVCC \leq 5.5V$ $V_{REF+} = \text{built-in } 2.5V$ Not use input Buffer Amplifier	0.02	-	0.25	
		$1.8V \leq AVCC \leq 5.5V$ $V_{REF+} = \text{built-in } 1.5V$ Not use input Buffer Amplifier	0.02	-	0.25	
		$2.7V \leq AVCC \leq 5.5V$ $V_{REF+} = AVCC/EXVREF$ Use input Buffer Amplifier	0.02	-	0.57	
		$2.4V \leq AVCC < 2.7V$ $V_{REF+} = AVCC/EXVREF$ Use input Buffer Amplifier	0.02	-	0.40	
		$1.8V \leq AVCC < 2.4V$ $V_{REF+} = AVCC/EXVREF$ Use input Buffer Amplifier	0.02	-	0.25	
		$2.8V \leq AVCC \leq 5.5V$ $V_{REF+} = \text{built-in } 2.5V$ Use input Buffer Amplifier	0.02	-	0.25	
		$1.8V \leq AVCC \leq 5.5V$ $V_{REF+} = \text{built-in } 1.5V$ Use input Buffer Amplifier	0.02	-	0.25	
$T_{ADCCONV}^{(1)}$	Start time	-	-	-	10	μs
$T_s^{(3)(4)}$	Sample Time	-	2	4	127	$1/f_{ADCC}$
$T_{ADCCONV}$	Total conversion time (including sampling time)	-	-	$T_s + 12$	-	
$T_{SETBUF}^{(1)}$	Output Voltage Setting Time of Voltage Buffer	Input signal is an internal signal	2.0	-	-	μs
		Input signal is an external signal	1.0	-	-	μs

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ENOB ⁽²⁾	Effective bits	$V_{REF+}=AVCC/EXVREF$ $f_s=2\text{Msps}$	10.5	11.1	-	bits
		$V_{REF+}=AVCC/EXVREF$ $f_s=1\text{Msps}$	10.6	11.2	-	
		$V_{REF+}=\text{built-in } 1.5\text{V}/2.5\text{V}$ $f_s=250\text{ksps}$	9.5	10.0	-	
SNR ⁽²⁾	Signal to noise ratio	$V_{REF+}=AVCC/EXVREF$ $f_s=2\text{Msps}$	67.5	69.7	-	dB
		$V_{REF+}=AVCC/EXVREF$ $f_s=1\text{Msps}$	67.6	70.2	-	
		$V_{REF+}=\text{built-in } 1.5\text{V}/2.5\text{V}$ $f_s=250\text{ksps}$	59.5	62.1	-	
THD ⁽²⁾	Total harmonic distortion	$V_{REF+}=AVCC/EXVREF$ $f_s=2\text{Msps}$	-75.0	-76.2	-	dB
		$V_{REF+}=AVCC/EXVREF$ $f_s=1\text{Msps}$	-75.0	-76.0	-	
		$V_{REF+}=\text{built-in } 1.5\text{V}/2.5\text{V}$ $f_s=250\text{ksps}$	-75.0	-76.4	-	
$E_D^{(2)}$	Differential non-linearity error	$V_{REF+}=AVCC/EXVREF$ $f_s=1\text{Msps}$	-0.9	± 0.5	1.5	LSB
$E_L^{(2)}$	Integral non-linearity error		-2.5	± 1.5	2.5	
$E_O^{(2)}$	Offset error		-	± 2.5	-	
$E_G^{(2)}$	Gain error		-	± 1.5	-	
$E_T^{(2)}$	Total unadjustable error		-	± 3.3	-	

1. Guaranteed by design, not tested in production.
2. Resulted from comprehensive evaluation, not tested in production.
3. When **NOT** use input Buffer Amplifier, the typical application of ADC is shown in the figure below:



In the diagram, I_{lkg} represents the I/O port leakage current. Refer to "[Port Leakage Characteristics-PA/PB/PC/PD Port](#)" for detailed parameters.

Under the condition of 0.5LSB sampling error accuracy requirement, the calculation formula of sampling time is as follows:

$$T_S = \frac{M}{f_{ADCCLK}} \geq (R_{AIN} + R_{ADC}) \times C_{ADC} \times (N + 1) \times \ln(2)$$

Where N is the ADC resolution (12 bits), f_{ADCCLK} is the ADC clock frequency (f_{PCLK} divided by the prescaler set in register ADC_CR0.CLKDIV), and M is the number of sampling cycles (sampling time occupies M ADC clock cycles - see register ADC_CR0.SAM for specific values).

The table below shows the relationship between ADC minimum sampling time T_S and external resistor R_{AIN} under typical operating conditions (with 0.5LSB sampling error). For other special external input impedance values, the corresponding minimum sampling time requirements can also be calculated through the sampling time calculation formula given above.

Table 5-28 Relationship Between ADC Minimum Sampling Time and External Input Impedance R_{AIN} (Not use input Buffer Amplifier)

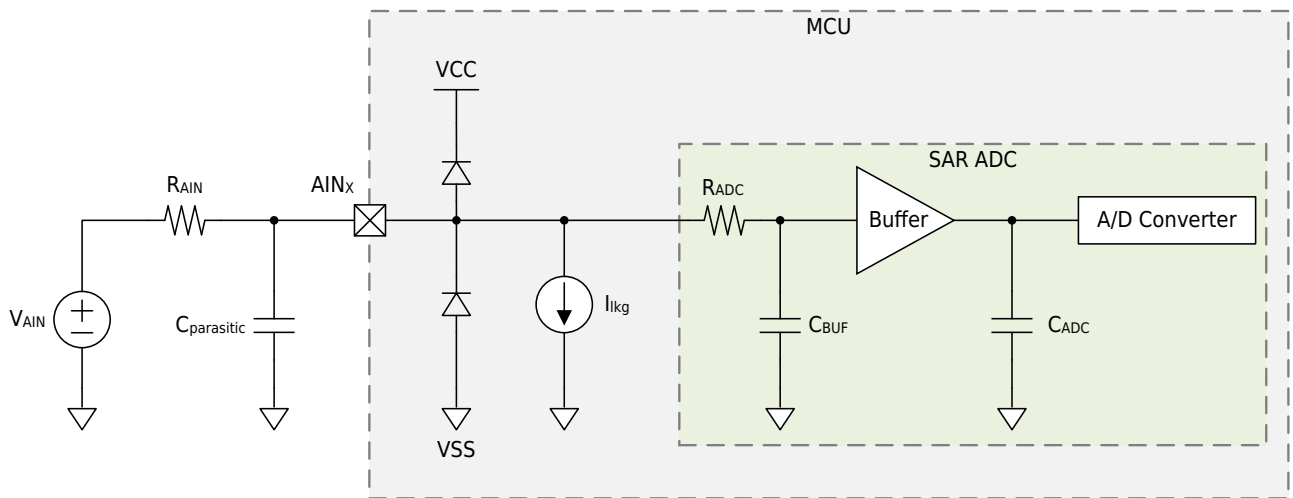
R_{AIN} (Ω)	Minimum Sampling Time T_S (ns)	R_{AIN} (Ω)	Minimum Sampling Time T_S (ns)
10	68	2200	167
47	70	3300	216
68	71	4700	279
100	72	6800	374
150	74	10000	518
220	77	15000	743
330	82	22000	1059
470	89	47000	2185
680	98	68000	3131
1000	113	100000	4573

R_{AIN} (Ω)	Minimum Sampling Time T_S (ns)	R_{AIN} (Ω)	Minimum Sampling Time T_S (ns)
1500	135		

For the above typical applications, you should pay attention to:

- Minimize parasitic capacitance $C_{parasitic}$ at the ADC input port AIN_x , to make sure $C_{parasitic} \ll (1 + R_{ADC}/R_{AIN}) * C_{ADC}$. Otherwise, it may result in insufficient settling of the ADC input voltage and introduce conversion errors.
- In addition to consider R_{AIN} value, if the internal resistance of signal source V_{AIN} is large, it also needs to be considered.

4. When use input Buffer Amplifier, the typical application of ADC is shown in the figure below:



In the diagram, I_{lkg} represents the I/O port leakage current. Refer to "[Port Leakage Characteristics-PA/PB/PC/PD Port](#)" for detailed parameters.

Under the condition of 0.5LSB sampling error accuracy requirement, the calculation formula of sampling time is as follows:

$$T_S = \frac{M}{f_{ADCCLK}} \geq (R_{AIN} + R_{ADC}) \times C_{BUF} \times (N + 1) \times \ln(2) + T_{SETBUF}$$

Where N is the ADC resolution (12 bits), f_{ADCCLK} is the ADC clock frequency (f_{PCLK} divided by the prescaler set in register `ADC_CR0.CLKDIV`), and M is the number of sampling cycles (sampling time occupies M ADC clock cycles - see register `ADC_CR0.SAM` for specific values). In this case, it is necessary to consider the voltage settling times at both the input and output terminals of the input voltage buffer simultaneously.

The table below shows the relationship between ADC minimum sampling time T_S and external resistor R_{AIN} under typical operating conditions (with 0.5LSB sampling error). For other special external input impedance values, the corresponding minimum sampling time requirements can also be calculated through the sampling time calculation formula given above.

Table 5-29 Relationship Between ADC Minimum Sampling Time and External Input Impedance R_{AIN} (Use input Buffer Amplifier)

R_{AIN} (Ω)	Minimum Sampling Time T_S (ns)	R_{AIN} (Ω)	Minimum Sampling Time T_S (ns)
10	1014	2200	1033
47	1014	3300	1043

$R_{AIN} (\Omega)$	Minimum Sampling Time T_s (ns)	$R_{AIN} (\Omega)$	Minimum Sampling Time T_s (ns)
68	1014	4700	1056
100	1014	6800	1075
150	1015	10000	1104
220	1015	15000	1149
330	1016	22000	1212
470	1018	47000	1437
680	1020	68000	1626
1000	1023	100000	1915
1500	1027		

For the above typical applications, you should pay attention to:

- Minimize parasitic capacitance $C_{parasitic}$ at the ADC input port AIN_x , to make sure $C_{parasitic} \ll (1 + R_{ADC}/R_{AIN}) * C_{BUF}$. Otherwise, it may result in insufficient settling of the ADC input voltage and introduce conversion errors.
 - In addition to consider R_{AIN} value, if the internal resistance of signal source V_{AIN} is large, it also needs to be considered.
5. Based on evaluation at $T_j = 125^\circ\text{C}$, the error caused by leakage current must not exceed ± 2 LSB. This limit may be relaxed for lower temperatures. In practical applications, determining the maximum allowable external input impedance requires joint consideration of leakage current and sampling time (refer to the two descriptions above).

5.3.15 Temperature Sensor Characteristics

When the measurement channel of the ADC selects the output voltage of the temperature sensor, the current chip temperature (Junction Temperature T_j) can be calculated through the output result of the ADC and the calibration value stored in the Flash memory.

Table 5-30 Temperature Sensor Parameters

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Temp Range	Operating junction temperature range for the temperature sensor	-	-40	-	125	$^\circ\text{C}$
$\Delta T_{linearity}^{(1)}$	Linearity error	-	-	± 3	-	$^\circ\text{C}$
$K^{(1)}$	Output the average value of the curve's slope	-	-	0.0798	-	$^\circ\text{C}/V$
$\Delta T_{error}^{(1)(2)}$	Temperature detection error	$T_A = -40\sim 105^\circ\text{C}$	-	± 6	-	$^\circ\text{C}$
$T_{start}^{(1)}$	Output stabilization time of temperature sensor	-	-	18	-	μs

**Note**

1. Guaranteed by design, not tested in production.
2. The deviation between the temperature calculated based on the calibration value at room temperature and the average slope of the output curve (refer to the "Reference Manual" for detailed calculation method) and the actual junction temperature.

5.3.16 VC Characteristics**Table 5-31 VC Characteristics**

Symbol	Parameters	Conditions		Min	Typ	Max	Unit
V _{in}	Positive/Negative channel single-ended input voltage range	-		0	-	5.5	V
V _{com}	Positive/Negative channel common-mode voltage range	-		0.1	-	VCC-0.1	V
V _{offset}	Offset voltage (Load offset trimcode from flash)	AVCC=3.3 V, T _A =25°C	BIAS=0b00	-	±15	-	mV
			BIAS=0b01	-	±15	-	mV
			BIAS=0b10	-	±10	-	mV
			BIAS=0b11	-	±5	-	mV
		AVCC=1.8-5.5V, T _A =-40-105°C	BIAS=0b00	-	±20	-	mV
			BIAS=0b01	-	±20	-	mV
			BIAS=0b10	-	±15	-	mV
			BIAS=0b11	-	±10	-	mV
I _{comp}	Current Consumption	VCx_CR0.BIAS=0b00 VCx_CR0.BIAS=0b01 VCx_CR0.BIAS=0b10 VCx_CR0.BIAS=0b11		-	0.3 1.2 10 20	-	μA
T _{response}	Response time (from change in positive/negative input voltage relationship to valid output)	VCx_CR0.BIAS=0b00 VCx_CR0.BIAS=0b01 VCx_CR0.BIAS=0b10 VCx_CR0.BIAS=0b11		-	2500 1000 400 200	-	ns
T _{setup}	Startup time (from enable to valid output)	VCx_CR0.BIAS=0b00 VCx_CR0.BIAS=0b01 VCx_CR0.BIAS=0b10 VCx_CR0.BIAS=0b11		-	10 2.5 0.7 0.35	-	μs
V _{hysteresis}	Hysteresis Voltage	VCx_CR0.HYS=0b00 VCx_CR0.HYS=0b01 VCx_CR0.HYS=0b10 VCx_CR0.HYS=0b11		-	0 10 20 30	-	mV
R _{in} ⁽¹⁾	Supported input signal impedance range	-		-	-	100	kΩ
V _{VDAC_off}	Built-in DAC voltage error	-		-	±25	-	mV

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
T_{VDAC_setup}	Settling time for the comparator's built-in DAC output voltage after enabling	-	-	5	-	μs
T_{filter}	Comparator result digital filter time	CR1.FLTTIME=0b0000	-	0	-	μs
		CR1.FLTTIME=0b0001	-	$2 \cdot T_{VCx}$	-	μs
		CR1.FLTTIME=0b0010	-	$4 \cdot T_{VCx}$	-	μs
		CR1.FLTTIME=0b0011	-	$8 \cdot T_{VCx}$	-	μs
		CR1.FLTTIME=0b0100	-	$16 \cdot T_{VCx}$	-	μs
		CR1.FLTTIME=0b0101	-	$32 \cdot T_{VCx}$	-	μs
		CR1.FLTTIME=0b0110	-	$64 \cdot T_{VCx}$	-	μs
		CR1.FLTTIME=0b0111	-	$128 \cdot T_{VCx}$	-	μs
		CR1.FLTTIME=0b1000	-	$256 \cdot T_{VCx}$	-	μs
		CR1.FLTTIME=0b1001	-	$512 \cdot T_{VCx}$	-	μs
		CR1.FLTTIME=0b1010	-	$1024 \cdot T_{VCx}$	-	μs
		CR1.FLTTIME=0b1011	-	$2048 \cdot T_{VCx}$	-	μs
		CR1.FLTTIME=0b1100	-	$4096 \cdot T_{VCx}$	-	μs
		CR1.FLTTIME=0b1101	-	$4096 \cdot T_{VCx}$	-	μs
		CR1.FLTTIME=0b1110	-	$4096 \cdot T_{VCx}$	-	μs
		CR1.FLTTIME=0b1111	-	$4096 \cdot T_{VCx}$	-	μs

**Note**

1. Guaranteed by design, not tested in production.
2. T_{VCx} represents the filter clock period, with $VCx_CR1.FLTCLK$ selecting either the built-in RC oscillator (about 256kHz) or PCLK as the filter clock.

5.3.17 LCD Controller

Table 5-32 LCD Controller Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$I_{LCD}^{(1)}$	Working current	VCC=3.3V, internal resistance mode (high-power consumption)	-	10	-	μA
		VCC=3.3V, internal resistance mode (medium-power consumption)	-	9.2	-	μA
		VCC=3.3V, internal resistance mode (low-power consumption)	-	0.55	-	μA
		VCC=3.3V, internal resistor mode (low-power consumption), 1/2 Bias, buffer enabled, acceleration pulse disabled	-	0.7	-	μA
		VCC=3.3V, internal resistor mode (low-power consumption), 1/3 Bias, buffer enabled, acceleration pulse disabled	-	0.85	-	μA
		VCC=3.3V, internal resistor mode (low-power consumption), 1/4 Bias, buffer enabled, acceleration pulse disabled	-	1	-	μA
		VCC=3.3V, internal resistor mode (high-power consumption), 1/3 Bias, buffer disabled, acceleration pulse enabled with $4/f_{in_clk}$	-	17	-	μA
		VCC=3.3V, external capacitance mode, 1/3 Bias, buffer disabled, acceleration pulse disabled	-	<1	-	μA
		VCC=3.3V, external resistor mode, 1/3 Bias, buffer disabled, acceleration pulse disabled	-	Determined by external resistor	-	μA
V_{LCDH}	LCD adjustable maximum voltage	-	-	VCC	-	V
V_{LCD34}	LCD 3/4 voltage	-	-	$3/4 V_{LCDH}$	-	V
V_{LCD23}	LCD 2/3 voltage	-	-	$2/3 V_{LCDH}$	-	V
V_{LCD12}	LCD 1/2 voltage	-	-	$1/2 V_{LCDH}$	-	V
V_{LCD13}	LCD 1/3 voltage	-	-	$1/3 V_{LCDH}$	-	V
V_{LCD14}	LCD 1/4 voltage	-	-	$1/4 V_{LCDH}$	-	V

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{LCD0}	LCD minimum voltage	-	-	0	-	V
ΔV_{XX}	LCD voltage deviation	$T_A = -40-105^{\circ}\text{C}$	-	± 35	-	mV

**Note**

1. The power consumption data was measured without an LCD screen attached, exclusively isolating the power draw of the LCD driver circuit itself and excluding contributions from GPIO or other system components.

5.3.18 TIM Timer Characteristics

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), see the table below.

Table 5-33 General Timer Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	-	1	-	t_{TIMCLK}
		$f_{TIMCLK}=48\text{MHz}$	0.0208	-	μs
f_{ext}	External clock frequency	-	0	$f_{TIMCLK}/2$	MHz
		$f_{TIMCLK}=48\text{MHz}$	0	24	MHz
Res_{Tim}	Timer resolution	-	-	16	Bit
		Mode 0 free counting	-	32	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle	-	1	65536	t_{TIMCLK}
		$f_{TIMCLK}=48\text{MHz}$	0.0208	-	μs

**Note**

1. Guaranteed by design, not tested in production.

Table 5-34 Low-Power Timer Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	-	1	-	t_{TIMCLK}
		$f_{TIMCLK}=48\text{MHz}$	0.0208	-	μs
f_{ext}	External clock frequency	-	0	$f_{TIMCLK}/2$	MHz
		$f_{TIMCLK}=48\text{MHz}$	0	24	MHz
Res_{Tim}	Timer resolution	-	-	16	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle	-	1	65536	t_{TIMCLK}
		$f_{TIMCLK}=48\text{MHz}$	0.0208	1363	μs

**Note**

1. Guaranteed by design, not tested in production.

Table 5-35 IWDTC Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Max	Unit
t_{res}	IWDTC overflow time	$f_{WDTCLK}=10kHz$	0.4	209715.2	ms

**Note**

1. Guaranteed by design, not tested in production.

5.3.19 Communication Interface

5.3.19.1 HSI2C/I2C Characteristics

HSI2C/I2C interface features are as follows:

Table 5-36 HSI2C/I2C Interface Characteristics⁽¹⁾

Symbol	Parameters	Standard Mode (100k)		Fast Mode (400k)		Fast enhanced Mode (1M)		Unit
		Min	Max	Min	Max	Min	Max	
t_{LOW}	SCL clock low time	4.7	-	1.25	-	0.5	-	μs
t_{HIGH}	SCL clock high time	4.0	-	0.6	-	0.26	-	μs
$t_{SU.DAT}$	Data setup time	250	-	100	-	50	-	ns
$t_{HD.DAT}$	Data hold time	0	-	0	-	0	-	μs
$t_{HD.STA}$	(Repeated) START condition hold time	2.5	-	0.625	-	0.25	-	μs
$t_{SU.STA}$	Repeated START condition setup time	2.5	-	0.6	-	0.25	-	μs
$t_{SU.STO}$	STOP condition setup time	0.25	-	0.25	-	0.25	-	μs
t_{BUF}	Bus Idle (STOP condition to START condition)	4.7	-	1.3	-	0.5	-	μs

**Note**

1. Guaranteed by design, not tested in production.

Table 5-37 HSI2C Characteristics-HS mode⁽¹⁾

Symbol	Parameters	Conditions	Min	Max	Unit
t_{LOW}	SCL clock low time	-	160	-	ns
t_{HIGH}	SCL clock high time	-	60	-	ns
$t_{SU.DAT}$	Data setup time	-	10	-	ns
$t_{HD.DAT}$	Data hold time	-	0	70	ns
$t_{HD.STA}$	(Repeated) START condition hold time	-	160	-	ns
$t_{SU.STA}$	Repeated START condition setup time	-	160	-	ns
$t_{SU.STO}$	STOP condition setup time	-	160	-	ns

Symbol	Parameters	Conditions	Min	Max	Unit
t_{BUF}	Bus Idle (STOP condition to START condition)	-	0.5	-	μs

**Note**

1. Guaranteed by design, not tested in production.

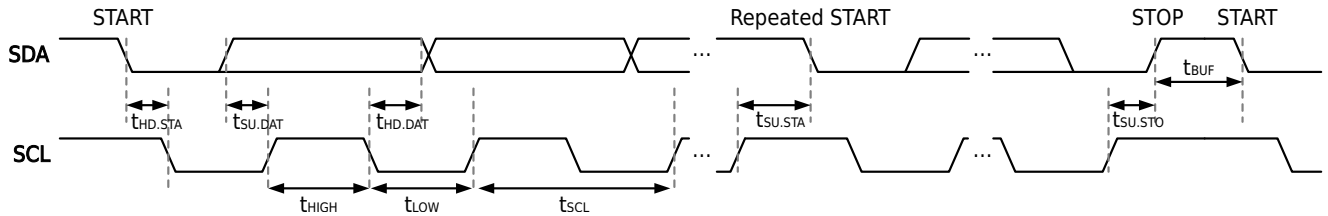


Figure 5-11 HSI2C/I2C Interface Timing

5.3.19.2 SPI Characteristics

Table 5-38 SPI Interface Characteristics⁽¹⁾⁽²⁾

Symbol	Parameters	Conditions	Min	Max	Unit
$t_{c(SCK)}$	Serial clock period ⁽³⁾	Master transmit mode $f_{PCLK}=48MHz$	41.6	-	ns
		Master receiving mode (Master delayed sampling disabled) $f_{PCLK}=48MHz$	166	-	ns
		Master receiving mode (Master delayed sampling enabled) $f_{PCLK}=48MHz$	83.3	-	ns
		Slave transmit mode (Master delayed sampling disabled) $f_{PCLK}=48MHz$	166	-	ns
		Slave transmit mode (Master delayed sampling enabled) $f_{PCLK}=48MHz$	83.3	-	ns
		Slave receiving mode $f_{PCLK}=48MHz$	83.3	-	ns
$t_{w(SCKH)}$	High level time of serial clock	Master mode	$0.45 \times t_{c(SCK)}$	-	ns
		Slave mode	$0.45 \times t_{c(SCK)}$	-	ns
$t_{w(SCKL)}$	Low level time of serial clock	Master mode	$0.45 \times t_{c(SCK)}$	-	ns
		Slave mode	$0.45 \times t_{c(SCK)}$	-	ns
$t_{su(SSN)}$	Setup time selected by slave	Slave Mode	$0.45 \times t_{c(SCK)}$	-	ns

Symbol	Parameters	Conditions	Min	Max	Unit
$t_{h(SSN)}$	Hold time selected by slave	Slave Mode	$0.45 \times t_{c(SCK)}$	-	ns
$t_{v(MO)}$	Effective time of master data output	-	-	3	ns
$t_{h(MO)}$	Hold time of master data output	-	0	-	ns
$t_{v(SO)}$	Effective time of slave data output	-	-	$20 + 1.5 \times T_{PCLK}$	ns
$t_{h(SO)}$	Hold time of slave data output	-	$14 + 0.5 \times T_{PCLK}$	-	ns
$t_{su(MI)}$	Setup time of master data input	-	20	-	ns
$t_{h(MI)}$	Hold time of master data input	-	2	-	ns
$t_{su(SI)}$	Setup time of slave data input	-	0	-	ns
$t_{h(SI)}$	Hold time of slave data input	-	$2 + 1.5 \times T_{PCLK}$	-	ns

**Note**

1. Guaranteed by design, not tested in production.
2. The data is provided under the condition of $V_{CC}=3.0V$.
3. The maximum frequency division factor of the master mode is $PCLK/2$, and the The maximum frequency division factor of slave mode is $PCLK/4$.

The waveform and timing parameters of the SPI interface signal are as follows:

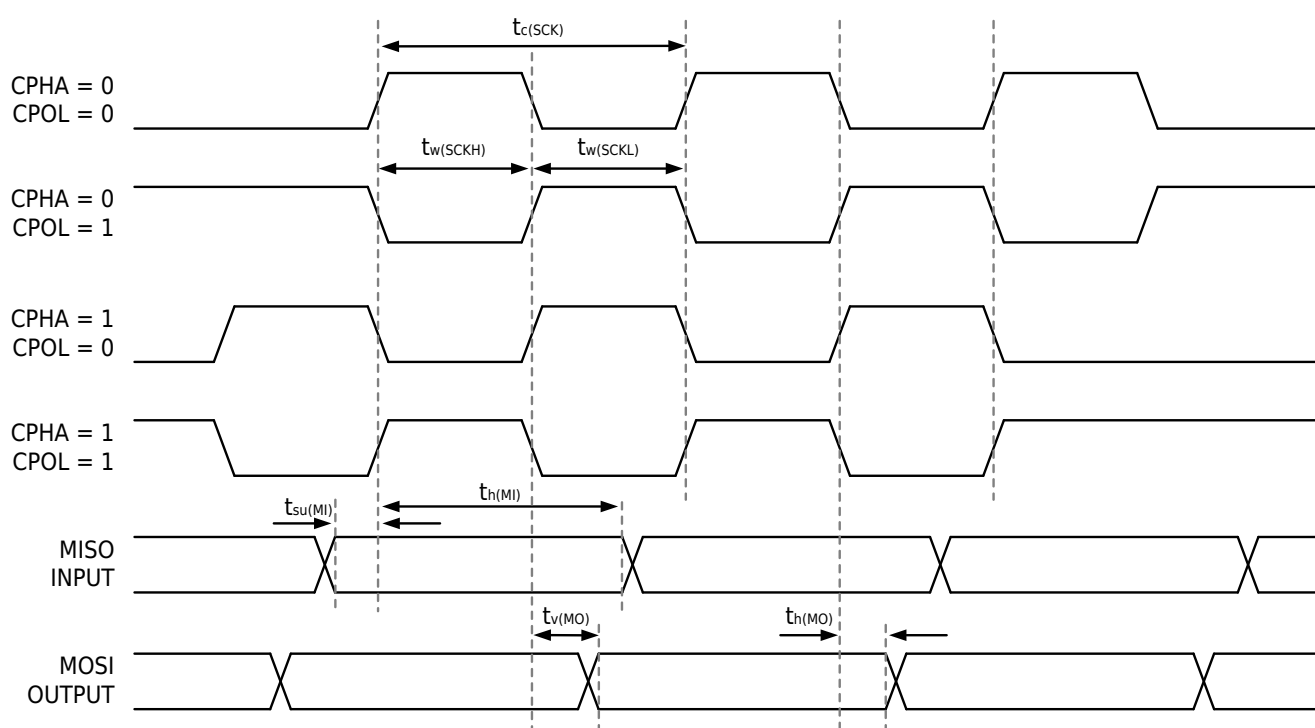


Figure 5-12 SPI Timing Diagram (Master Mode)

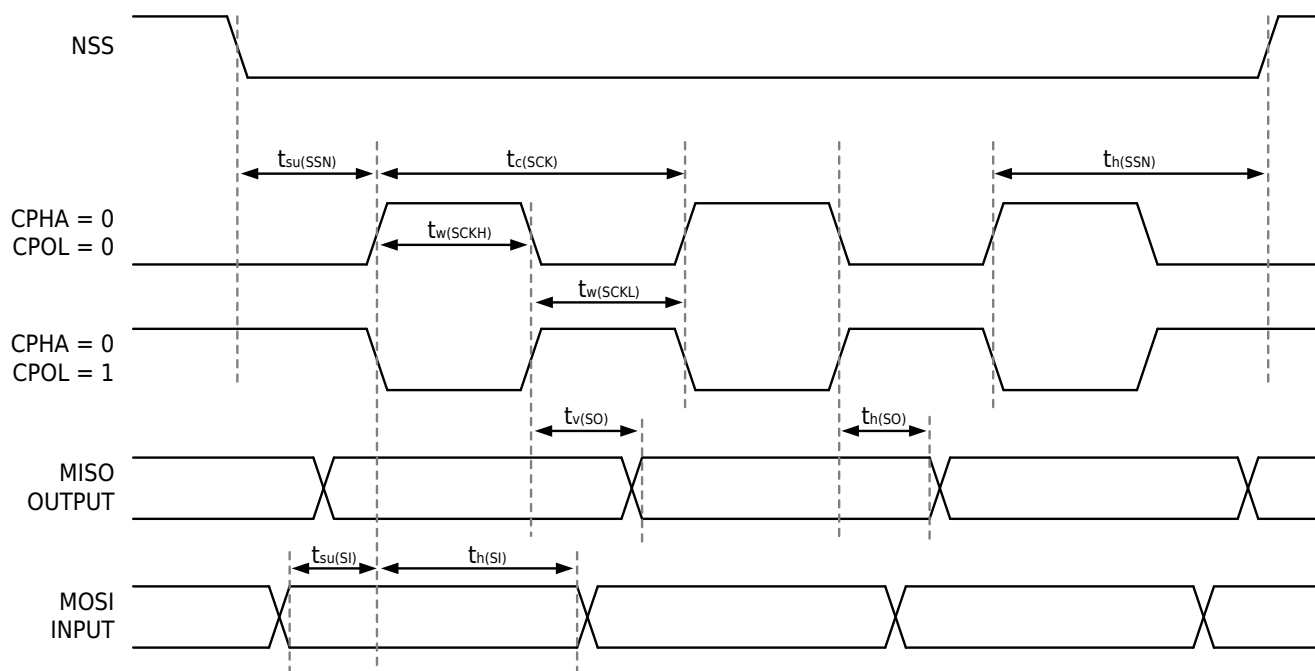


Figure 5-13 SPI Timing Diagram (Slave Mode CPHA=0)

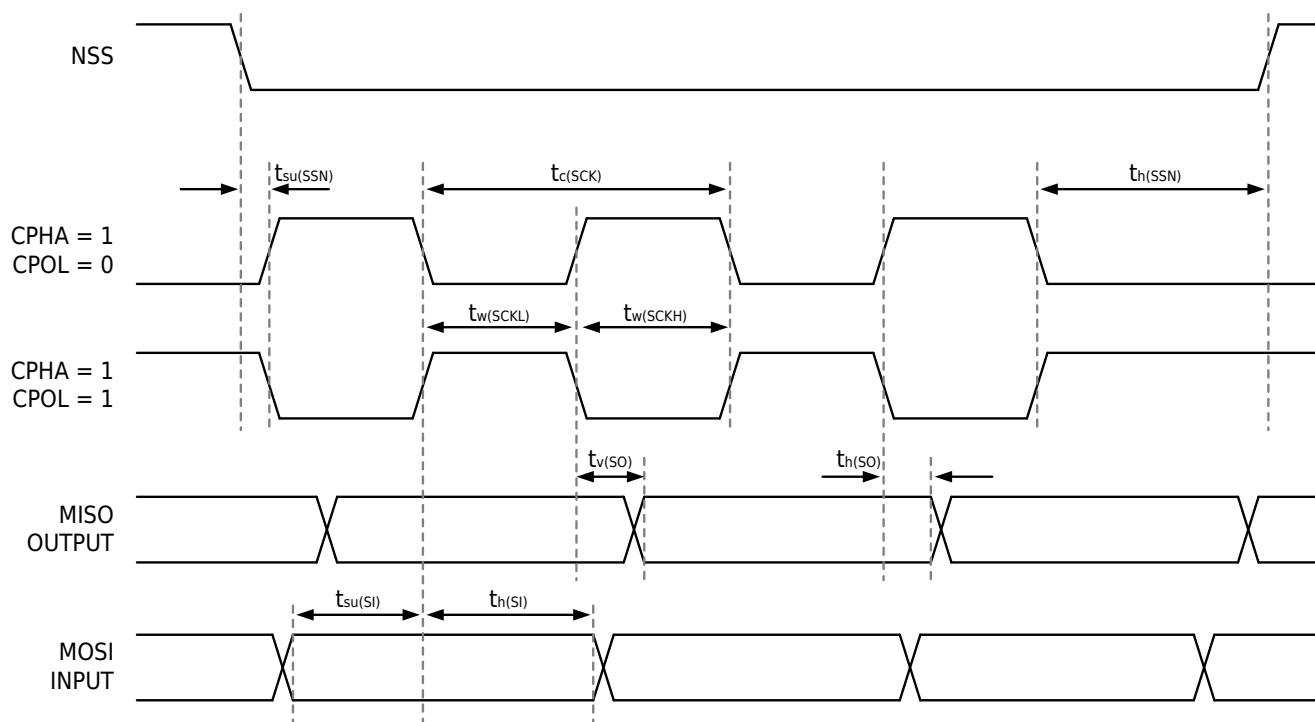
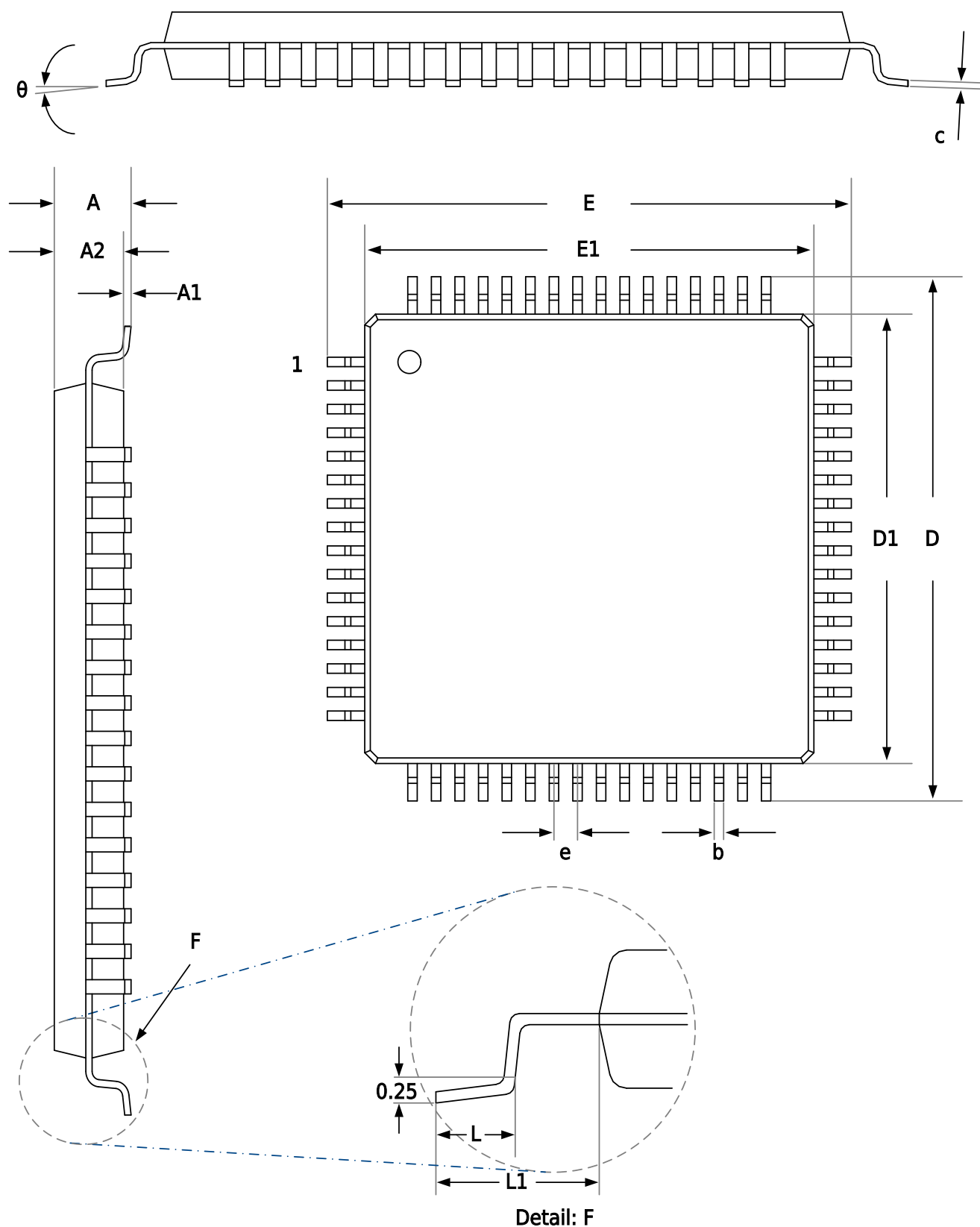


Figure 5-14 SPI Timing Diagram (Slave Mode CPHA=1)

6 Package Specifications

6.1 Package Dimensions

6.1.1 LQFP64 Package

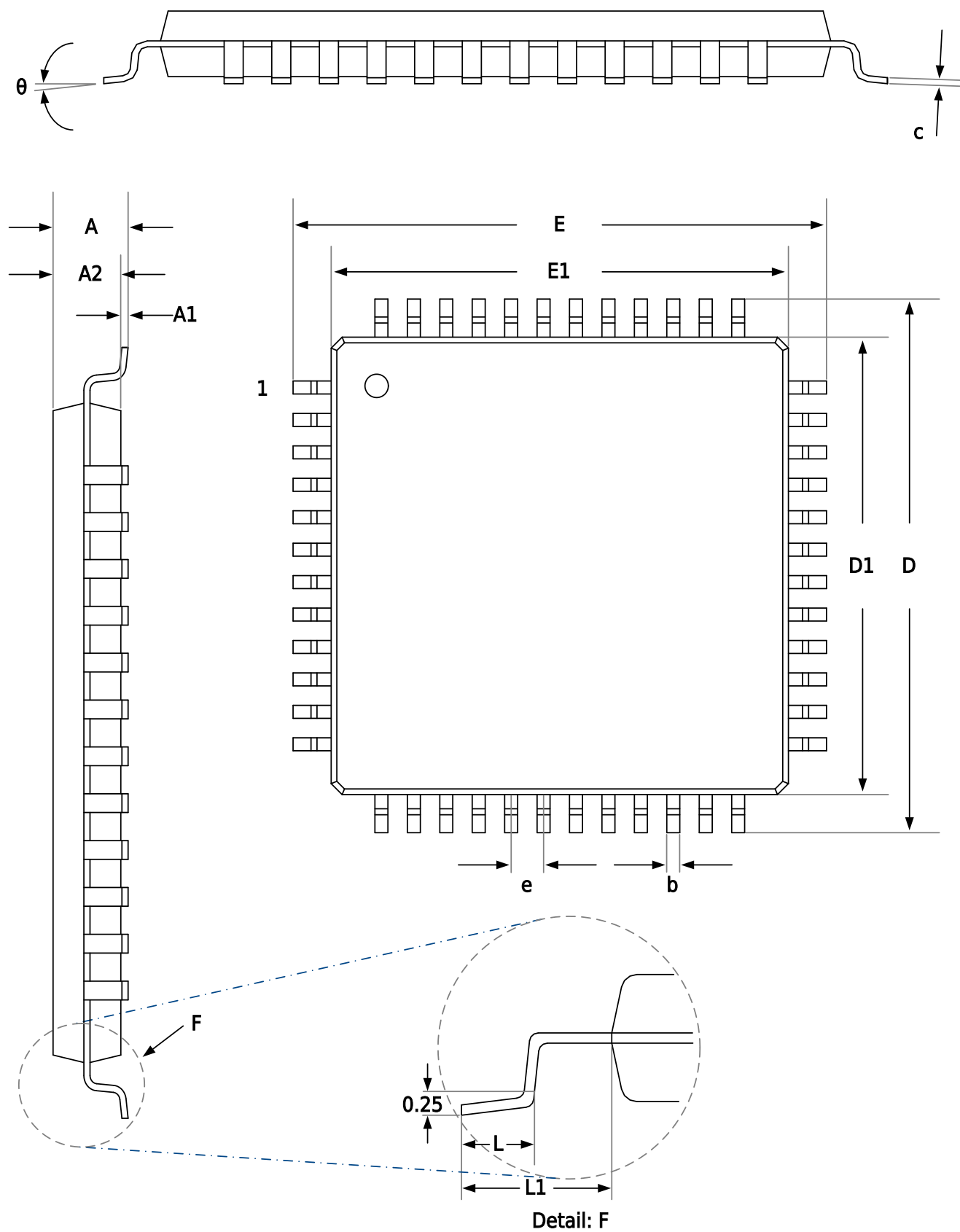


Symbol	10*10 Millimeter			7*7 Millimeter		
	Min	Nom	Max	Min	Nom	Max
A	--	--	1.60	--	--	1.60
A1	0.05	--	0.15	0.05	--	0.15
A2	1.35	1.40	1.45	1.35	1.40	1.45
b	0.17	0.22	0.27	0.16	0.20	0.25
c	0.09	--	0.20	0.09	--	0.20
D	11.80	12.00	12.20	8.80	9.00	9.20
D1	9.90	10.00	10.10	6.90	7.00	7.10
E	11.80	12.00	12.20	8.80	9.00	9.20
E1	9.90	10.00	10.10	6.90	7.00	7.10
e	0.50BSC			0.40BSC		
L	0.45	--	0.75	0.45	--	0.75
L1	1.00REF			1.00REF		
θ	0°	--	7°	0°	--	7°

**Note**

Dimensions "D1" and "E1" do not include mold flash.

6.1.2 LQFP48 Package

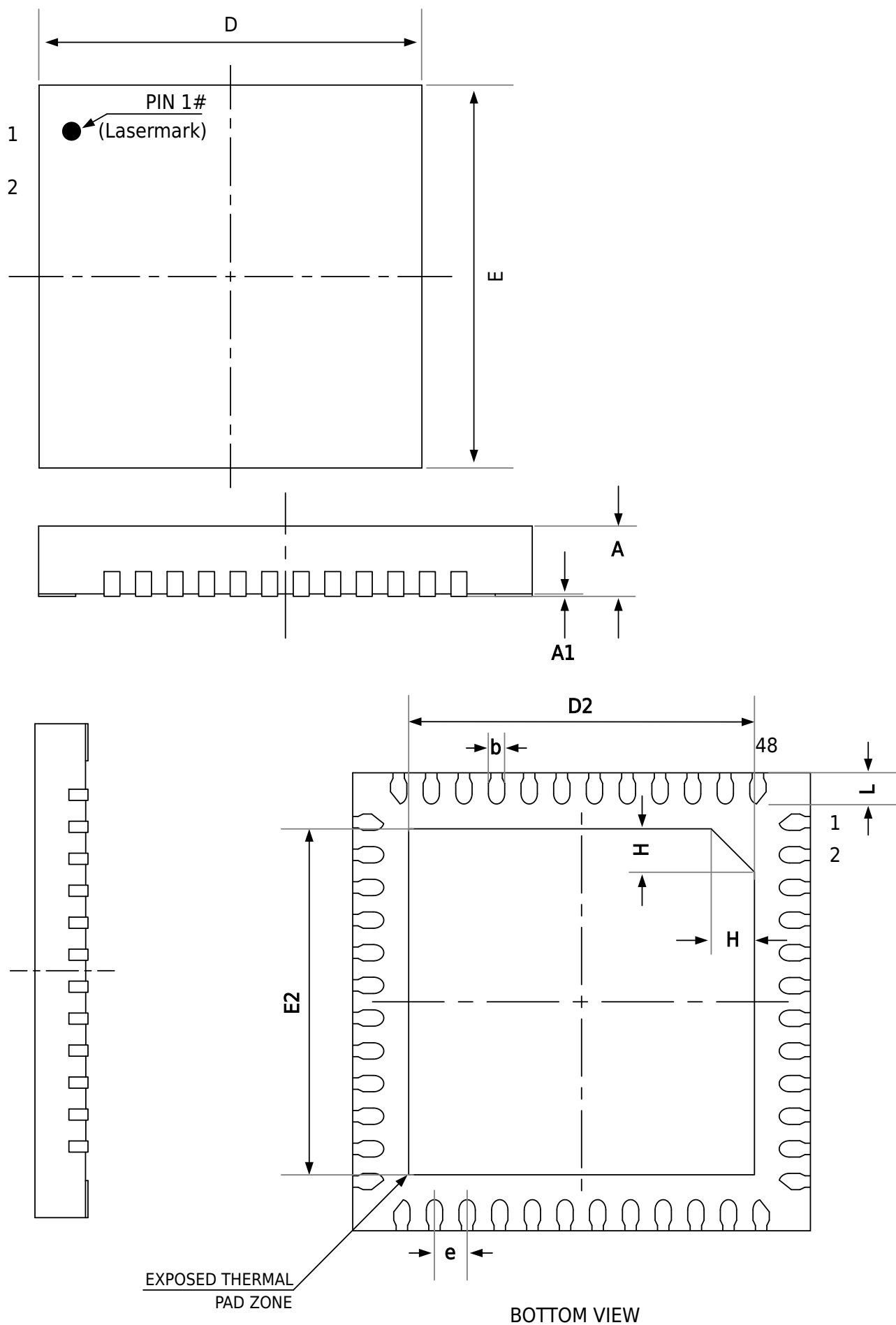


Symbol	7*7 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0	--	7°

**Note**

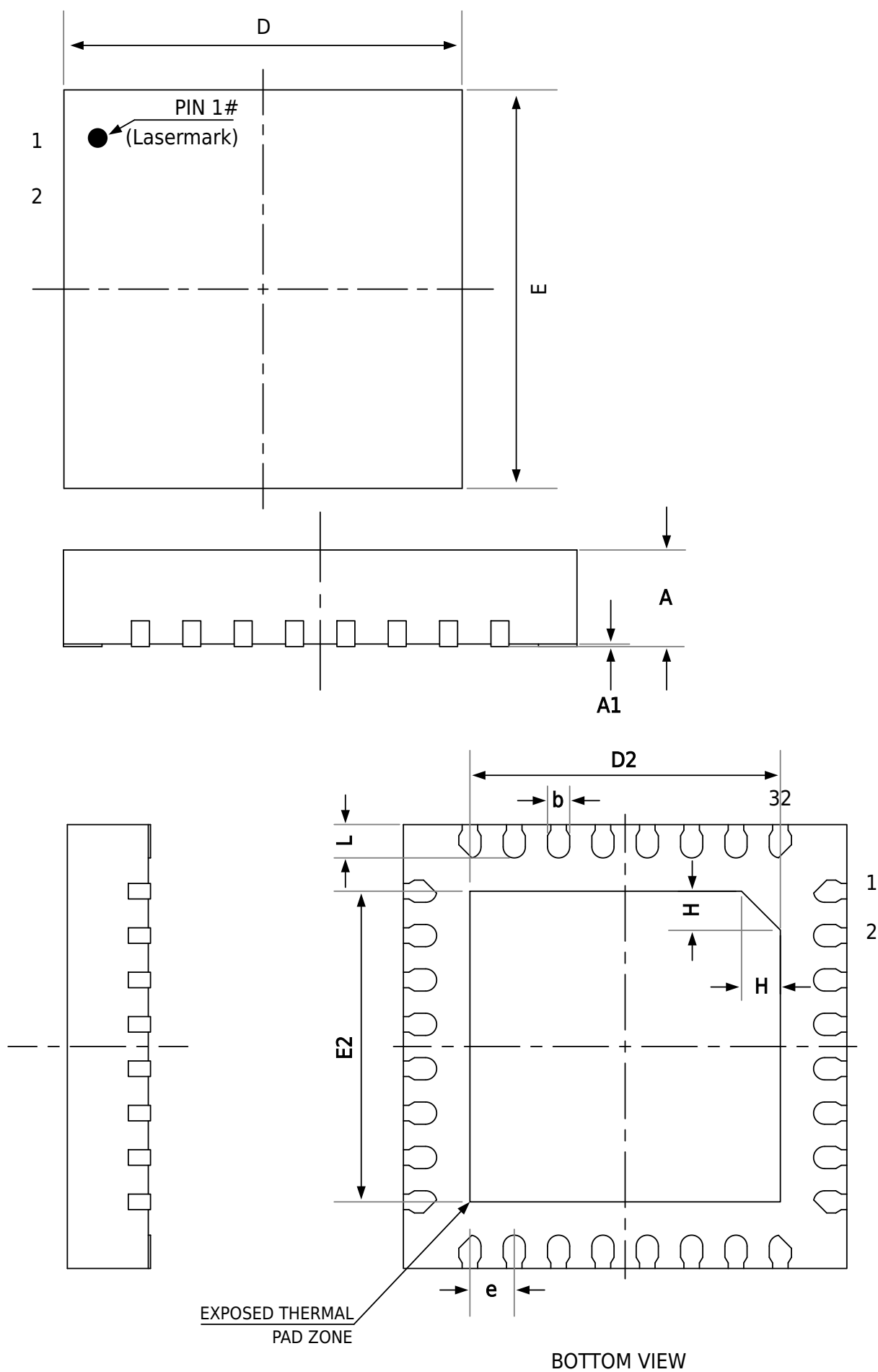
Dimensions "D1" and "E1" do not include mold flash.

6.1.3 QFN48 Package



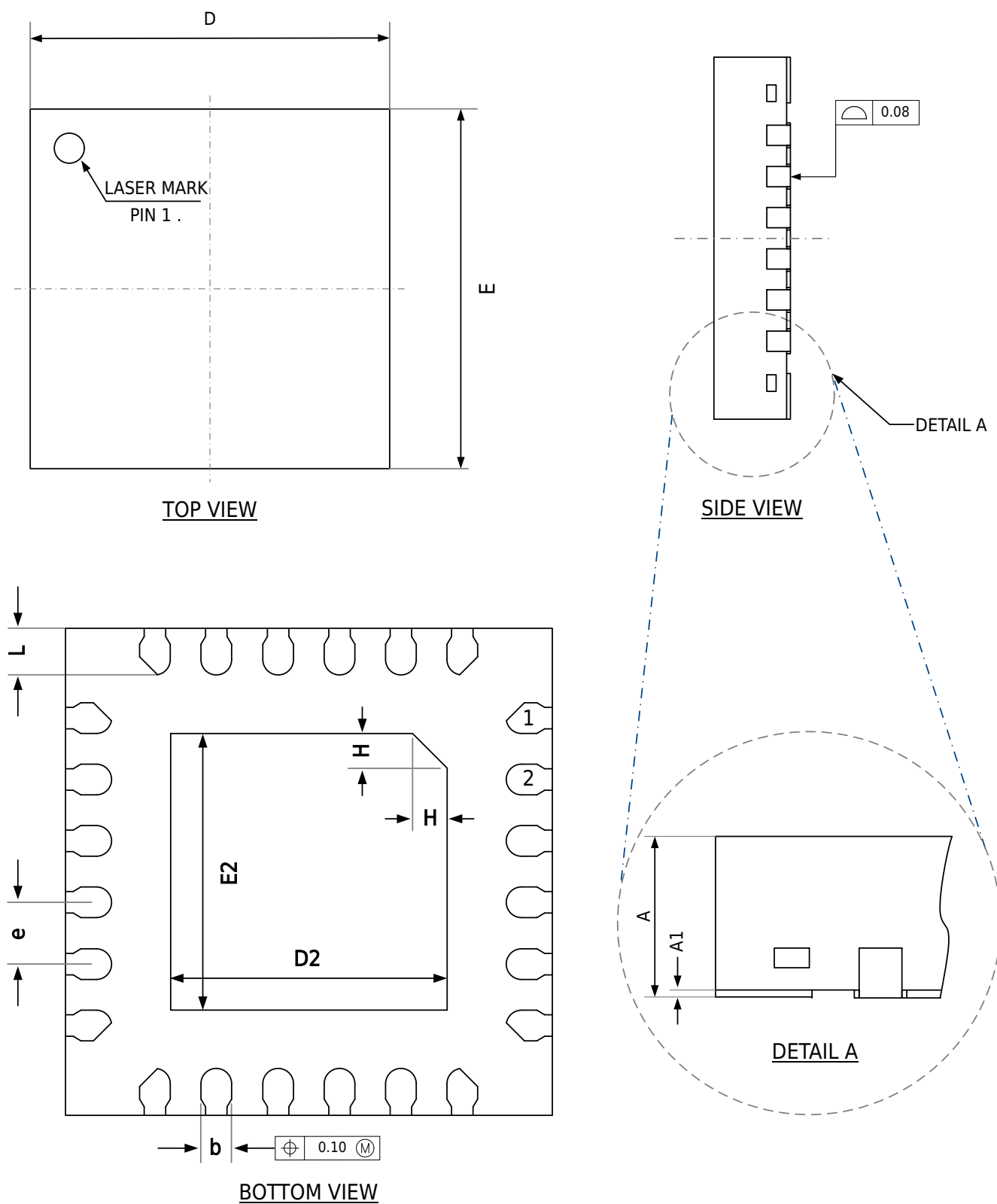
Symbol	5*5 Millimeter		
	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
b	0.13	0.18	0.23
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
e	0.35BSC		
L	0.30	0.35	0.40
H	0.30REF		

6.1.4 QFN32 Package



Symbol	4*4 Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
e	0.40BSC		
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
L	0.30	0.40	0.50
H	0.30REF		

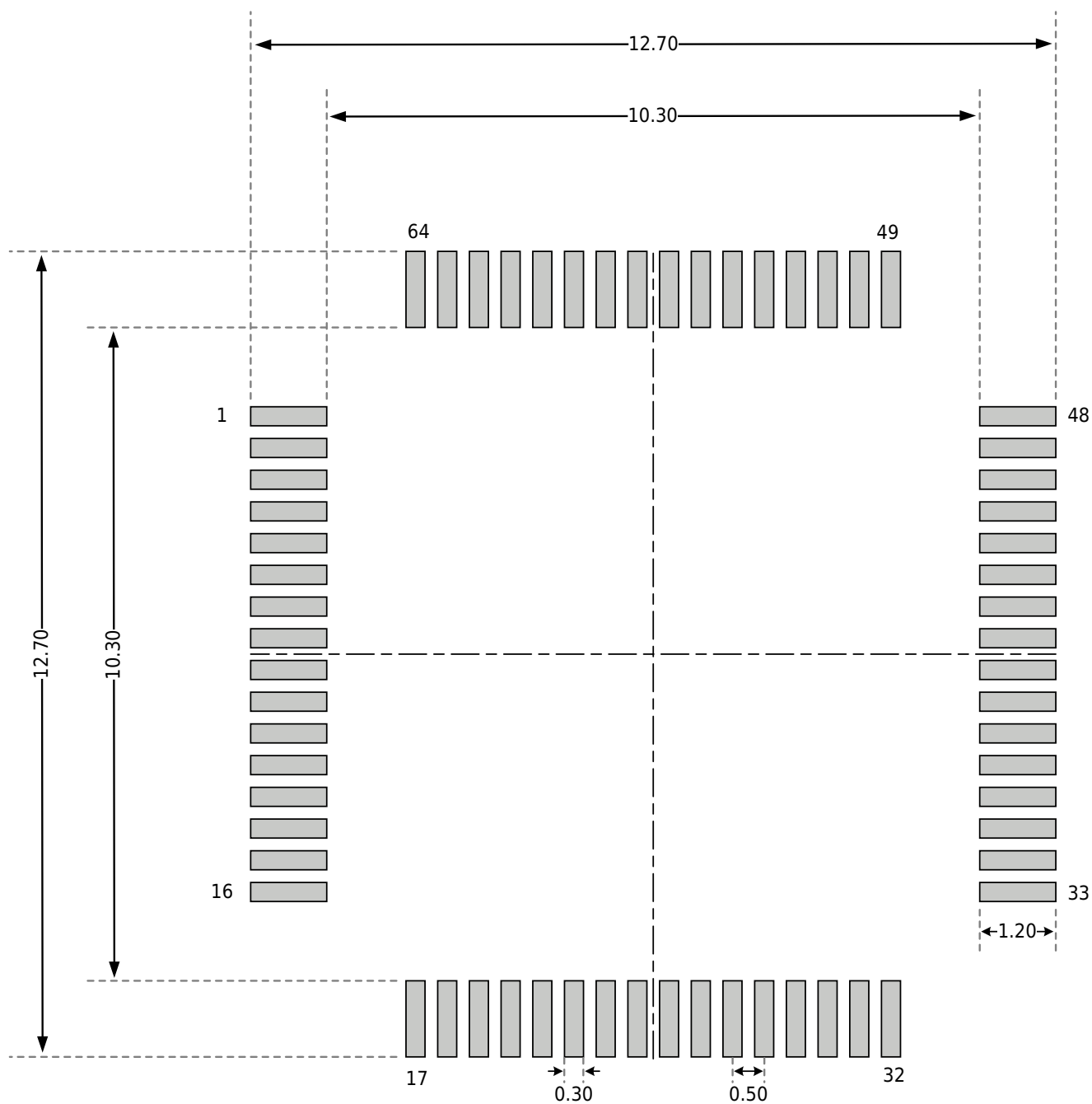
6.1.5 QFN24 Package



Symbol	3*3 Millimeter		
	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
b	0.10	0.15	0.20
D	2.90	3.00	3.10
D2	1.90	2.05	2.23
E	2.90	3.00	3.10
E2	1.90	2.05	2.23
e	0.30	0.35	0.40
L	0.15	0.21	0.27
H	0.25REF		

6.2 PCB Land Pattern

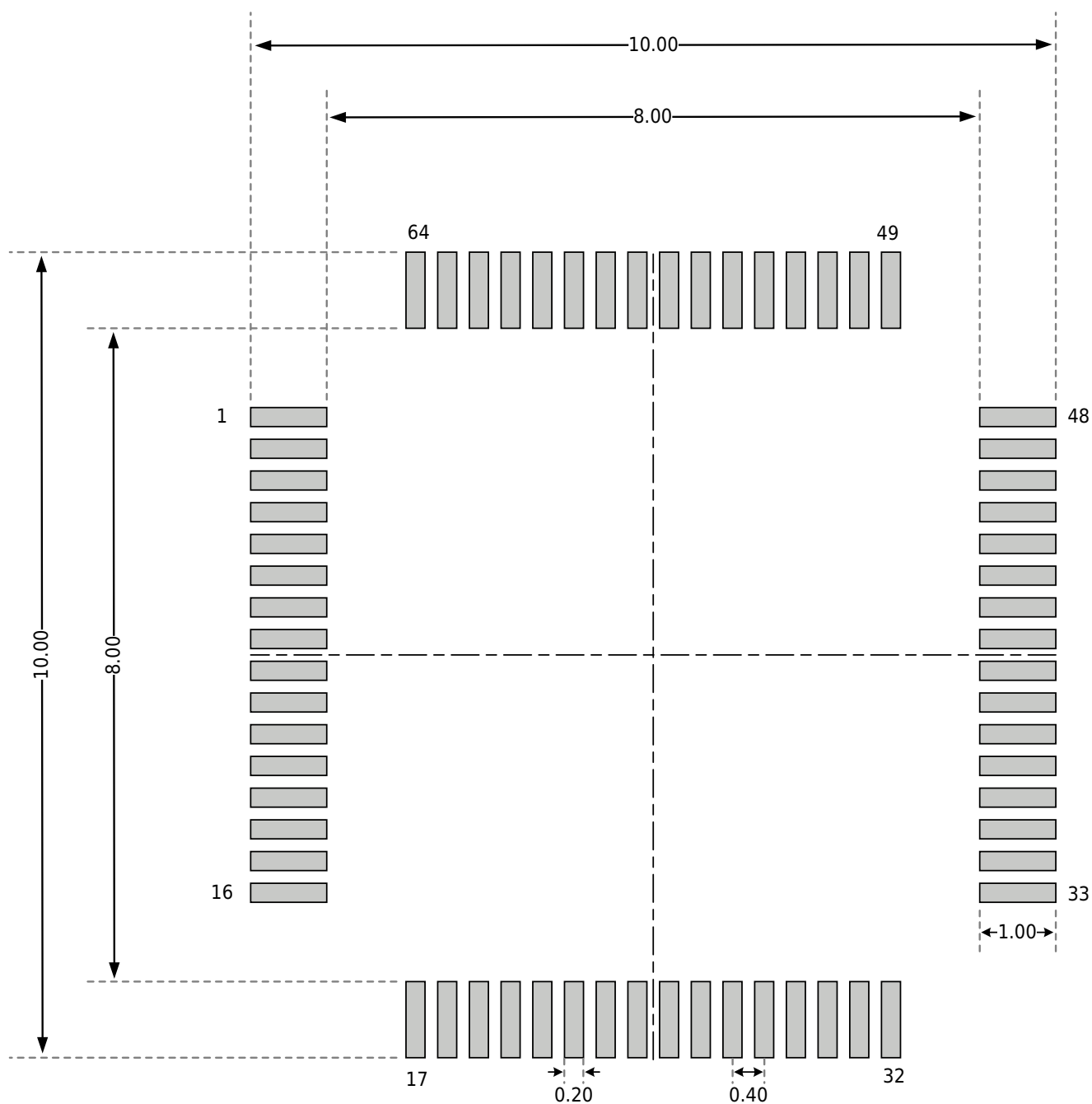
6.2.1 LQFP64 Package (10mm*10mm)



Note

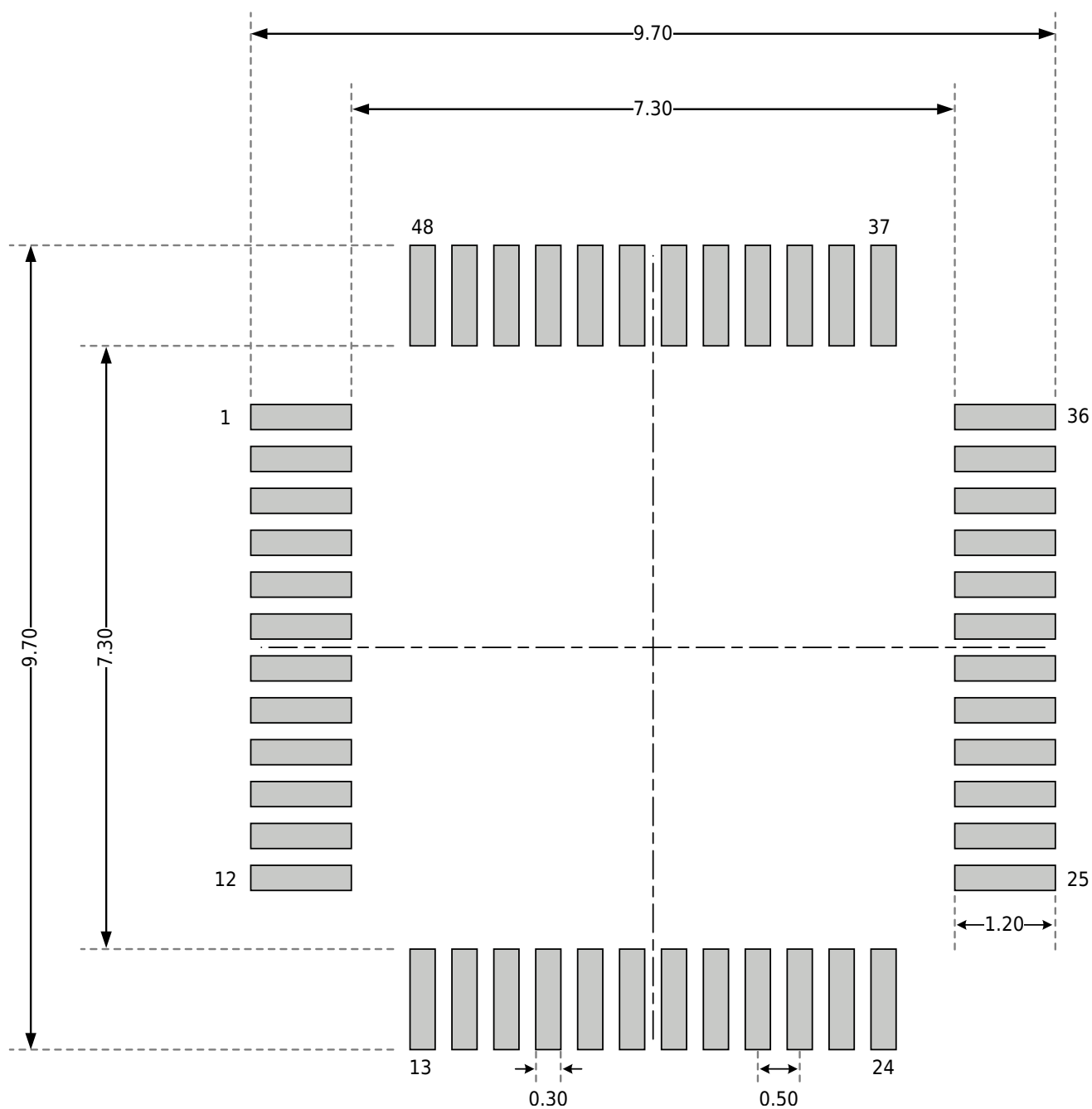
- Dimensions are in millimeters.
- Dimensions are for reference only.

6.2.2 LQFP64 Package (7mm*7mm)

**Note**

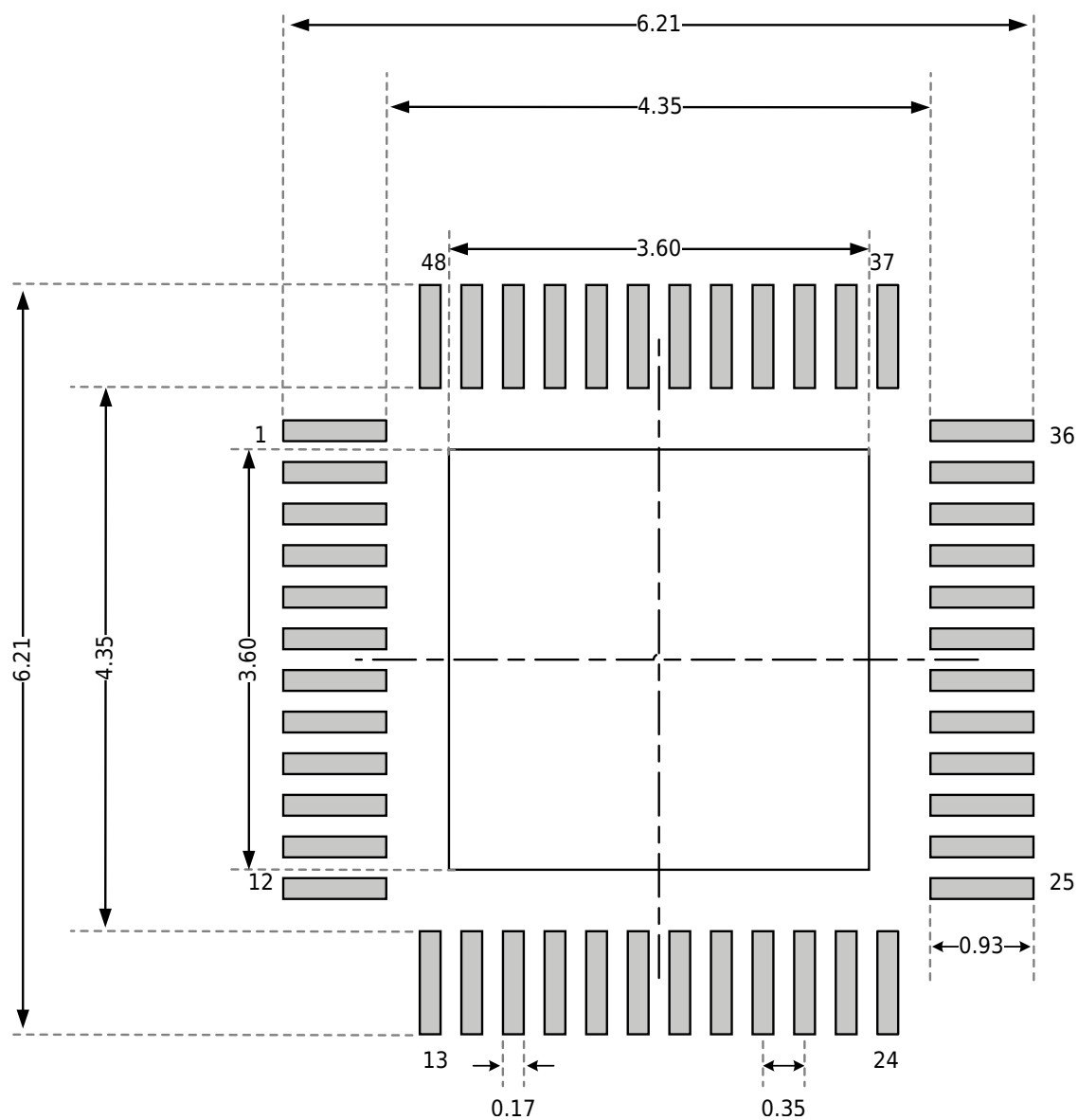
- Dimensions are in millimeters.
- Dimensions are for reference only.

6.2.3 LQFP48 Package (7mm*7mm)

**Note**

- Dimensions are in millimeters.
- Dimensions are for reference only.

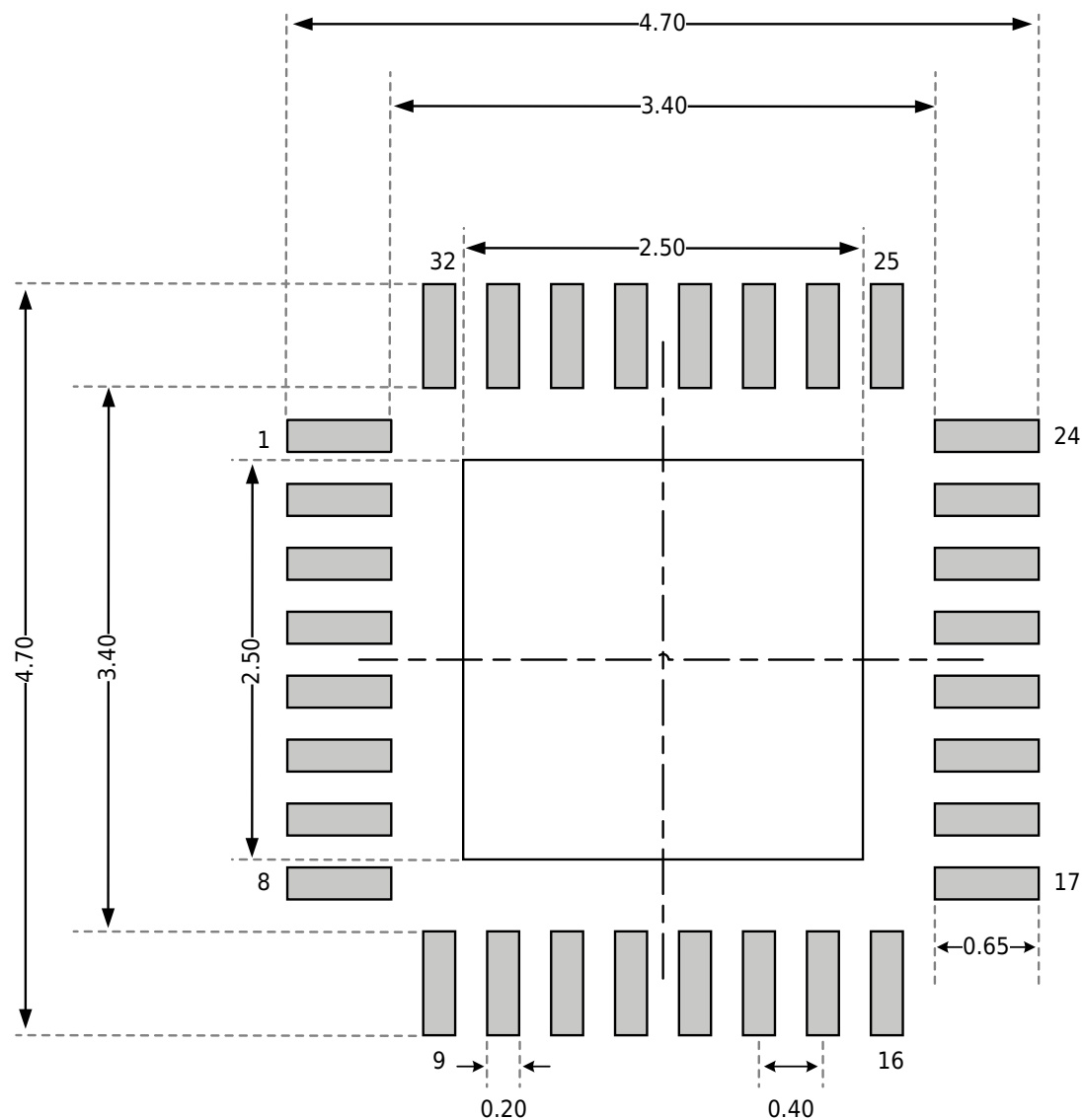
6.2.4 QFN48 Package (5mm*5mm)



Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

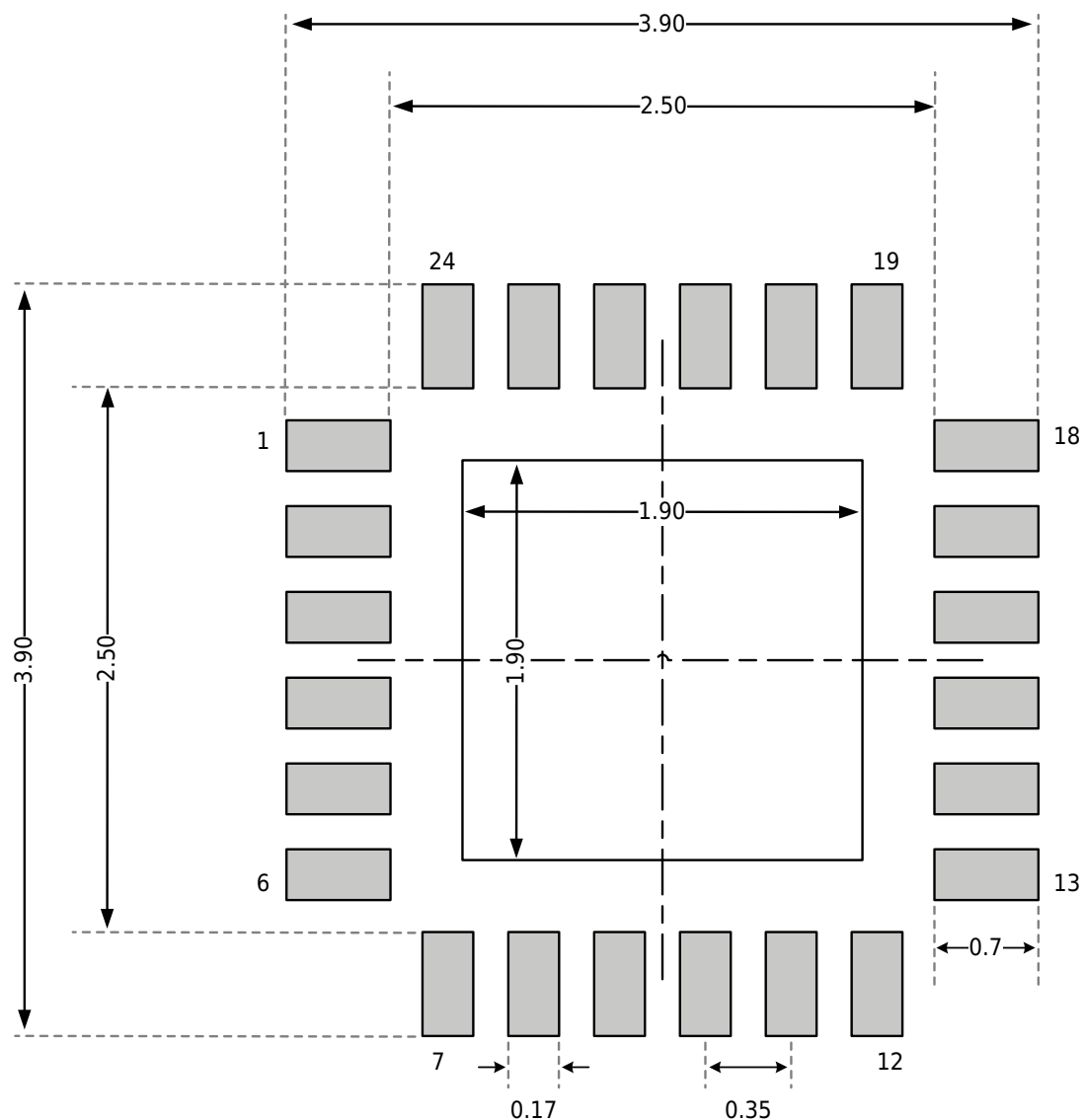
6.2.5 QFN32 Package (4mm*4mm)



Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

6.2.6 QFN24 Package (3mm*3mm)



Note

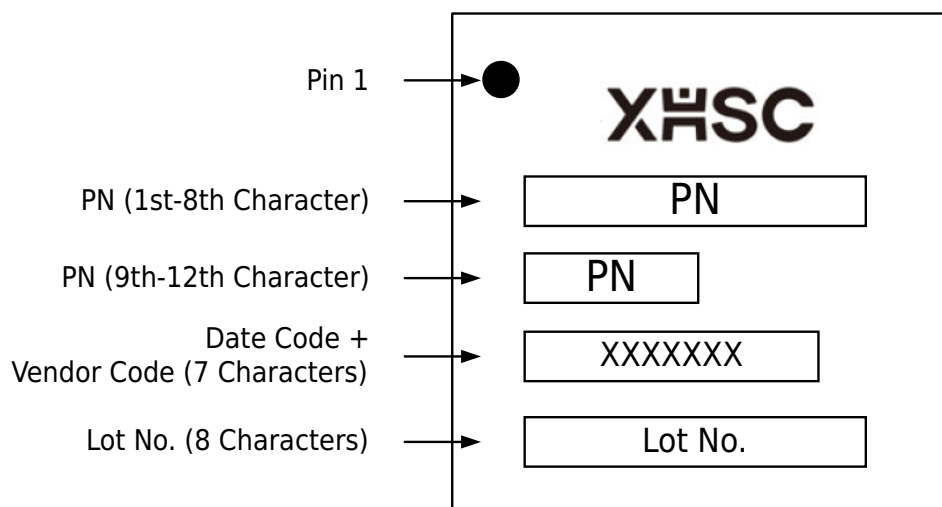
- Dimensions are in millimeters.
- Dimensions are for reference only.

6.3 Package Marking

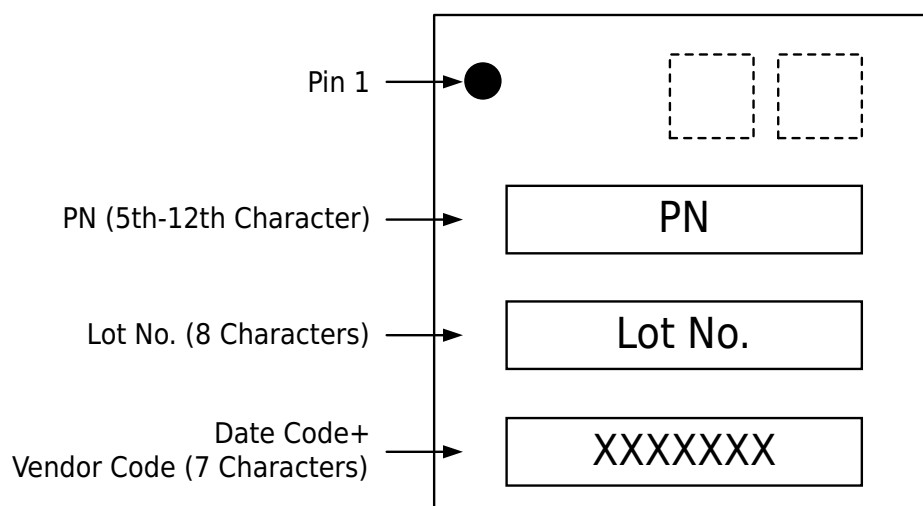
The location and information description of Pin1 on the front of each package are given below.

LQFP64 package (10mm*10mm)/LQFP64 package (7mm*7mm)

LQFP48 package (7mm*7mm)



QFN48 package (5mm*5mm)/QFN32 package (4mm*4mm)/QFN24 package (3mm*3mm)



Note

The blank boxes in the above figure indicate optional marks related to production, which are not explained in this section.

6.4 Packaging Thermal Resistance Coefficient

When the packaged chip is working at the specified working environment temperature, the junction temperature $T_j(^{\circ}\text{C})$ of the chip surface can be calculated according to the following formula:

$$T_j = T_A + (P_D * \theta_{JA})$$

- T_A refers to the working environment temperature when the packaged chip is working, the unit is $^{\circ}\text{C}$;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is $^{\circ}\text{C}/\text{W}$;

- P_D refers to total power dissipation, which is the sum of internal power consumption (P_{INT}) and I/O pin power consumption (P_{IO}), the unit is W.

$$P_D = P_{INT} + P_{IO}$$

► P_{INT} : Internal power consumption, calculated as the product of I_{VCC} and V_{CC} .

► P_{IO} : I/O pin power consumption, calculated as: $P_{IO} = \Sigma(V_{OL} * I_{OL}) + \Sigma((V_{CC} - V_{OH}) * I_{OH})$

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable junction temperature T_{jmax} of the chip.

Table 6-6 Thermal Resistance Coefficient Reference Table For Each Package

Package Type and Dimensions	Thermal Resistance Parameters (θ_{JA})	Unit
LQFP64 10mm*10mm/0.5mm pitch	65±10%	°C/W
LQFP64 7mm*7mm/0.4mm pitch	75±10%	°C/W
LQFP48 7mm*7mm/0.5mm pitch	75±10%	°C/W
QFN48 5mm*5mm/0.35mm pitch	42±10%	°C/W
QFN32 4mm*4mm/0.4mm pitch	53±10%	°C/W
QFN24 3mm*3mm/0.35mm pitch	70 ± 10%	°C/W

7 Ordering Information

Part Number	HC32L126KATB-LQFP64	HC32L126KATB-LQ64	HC32L126JATB-LQ48	HC32L121JAUB-ZFN48TR	HC32L121FAUB-QFN32TR	HC32L121DAUB-UFN24TR
GPIO	56	56	40	40	26	20
Core	Cortex-M0+	Cortex-M0+	Cortex-M0+	Cortex-M0+	Cortex-M0+	Cortex-M0+
Frequency	48MHz	48MHz	48MHz	48MHz	48MHz	48MHz
Flash	128KB	128KB	128KB	128KB	128KB	128KB
RAM	16KB	16KB	16KB	16KB	16KB	16KB
Power Supply Voltages	1.8-5.5V	1.8-5.5V	1.8-5.5V	1.8-5.5V	1.8-5.5V	1.8-5.5V
Temp Range	-40-105°C	-40-105°C	-40-105°C	-40-105°C	-40-105°C	-40-105°C
DMA	1*2ch	1*2ch	1*2ch	1*2ch	1*2ch	1*2ch
LPTimer	2	2	2	2	2	2
General Timer	4	4	4	4	4	4
RTC	1	1	1	1	1	1
IWDT	1	1	1	1	1	1
WWDT	1	1	1	1	1	1
LPUART	3	3	3	3	1	1
USART	2	2	2	2	2	1
LIN	√	√	√	√	√	√
ISO7816	√	√	√	√	√	√
I2C	3	3	3	3	3	3
SPI	2	2	2	2	1	1
12-bit ADC	1*16ch	1*16ch	1*10ch	1*10ch	1*7ch	1*6ch
VC	2	2	2	2	2	2
LCD	4*40/6*38/8*36	4*40/6*38/8*36	4*26	-	-	-
LVD	1	1	1	1	1	1
CRC	1	1	1	1	1	1
AES	1	1	1	1	1	1
TRNG	1	1	1	1	1	1
Package (mm*mm)	LQFP64(10*10)	LQFP64(7*7)	LQFP48(7*7)	QFN48(5*5)	QFN32(4*4)	QFN24(3*3)
Packing	Tray	Tray	Tray	Tray	Tape & Reel	Tape & Reel
Pitch	0.5mm	0.4mm	0.5mm	0.35mm	0.4mm	0.35mm
Thickness	1.4mm	1.4mm	1.4mm	0.55mm	0.75mm	0.55mm

Please contact the sales window for the latest mass production information before ordering.

Revision History

Revision/Date	Changes
Rev1.20 Aug. 28, 2026	1. Typical Application Circuit Diagram: the decoupling capacitor description is optimized. 2. Electrical Specifications: In the "Absolute Maximum Ratings" chapter, the voltage and current tables is combined; In the "I/O Port Characteristics - Input Characteristics" chapter, the "Input Level Low Voltage Recognition Characteristics" table is added; In the "ADC Characteristics" chapter, the data of Buffer function is added. 3. Package Specifications: In the "PCB Land Pattern" section, the redundant data is removed;
Rev1.10 Feb. 12, 2026	1. Added QFN24 product: HC32L121DAUB-UFN24TR, modified product support descriptions in relevant chapters. 2. Functional Description: In the "Programming Mode" chapter, the BOOT pin related programming descriptions are optimized. 3. Pin Definitions: In the "Module Signal Description" chapter, the description of TIMx_BK signal is added. 4. Typical Application Circuit Diagram: the note of BOOT pin is added. 5. Electrical Specifications: In the "General Operating Conditions" chapter, the descriptions related to power dissipation have been removed, the subscript of "T_A" and its related annotation explanations have been removed; In the "Working Conditions at Power-On and Power-Down" chapter, the maximum value of the S_{VCC_f} parameter changed from 1 to 0.05; The "Time to Wake-Up from Low-Power Mode" chapter is added; In the "External High-Speed Crystal XTH" chapter, the I_{dd} data was refreshed, and the typical value of the T_{start} parameter changed from "2" to "1.5"; In the "External Low-Speed Crystal XTL" chapter, the minimum value of C_{Lx} is changed to "4pF". Meanwhile, optimize the annotation description; In the "RCH" chapter, the Dev data condition removed frequency information; In the "RCL" chapter, the typical value of the TRIM parameter changed from "0.35" to "0.5", the maximum and minimum values of the Dev parameter @HPM changed from "2, -3.5" to "2.5, -2.5", the typical value of the T_{CLK} parameter changed from "120" to "150", and the maximum and minimum values of the DC_{CLK} parameter changed from "70, 30" to "75, 25"; In the "Memory Characteristics" chapter, the EC_{FLASH} parameters have been optimized based on new conditions; In the "ADC Characteristics" chapter, the maximum value of the E_D parameter changed from "0.9" to "1.5", and the maximum value of the E_L parameter changed from "1.5" to "2.5"; In the "Temperature Sensor Characteristics" chapter, the typical value of the $\Delta T_{linearity}$ parameter changed from "± 5" to "± 3", and the ΔT_{error} parameter is added; In the "LCD Controller" chapter, the typical values for the high and low power consumption in the internal resistance model of the I_{LCD} parameters have been corrected, three sets of conditional data were added, and the typical value of the ΔV_{xx} parameter changed from "± 25" to "± 35".

Revision/Date	Changes
Rev1.10 Feb. 12, 2026	6. Package Specifications: In the "Package Dimensions" chapter, the A2, A3, c of QFN package have been removed; In the "QFN48 Package" chapter, the value of H (original "h") is modified to "0.30REF"; In the "QFN32 Package" chapter, the min value of L is modified to "0.30", the max and min value of D2/E2 is modified to "2.80, 2.60", the value of H (original "h") is modified to "0.30REF".
Rev1.01 Sep. 12, 2025	1. Functional Description: In the "ADC" chapter, the description is changed from "Up to 18 input channels are supported" to "Up to 19 input channels are supported", the description "1 internal temperature sensor voltage channel" is added. 2. Electrical Specifications: The chapter "Temperature Sensor Characteristics" is added.
Rev1.00 Sep. 9, 2025	First official release.