

HC32L18x Series

32-bit ARM[®] Cortex[®]-M0+ Microcontroller

Datasheet

Rev1.30
August 2026

Feature List

Support Features

- 48MHz Cortex-M0+ 32-bit CPU platform
- HC32L18x Series has a flexible power management system, ultra-low power performance:
 - ▶ 0.8μA@3V DeepSleep mode: all clocks off, power-on reset active, IO state retention, IO interrupt active, all registers, RAM and CPU data save state power consumption
 - ▶ 1.5μA @3V DeepSleep mode + RTC working
 - ▶ 23μA/MHz@3V@48MHz Sleep mode: CPU halted, peripherals off, main clock is running
 - ▶ 52μA/MHz@3V@48MHz Operating Mode: CPU running, peripherals off, program running from Flash
 - ▶ 10μs ultra-low power consumption wake-up time makes mode switching more flexible and efficient, and system response more agile
- Maximum 256KB Flash memory, with erase and write protection function, supports ISP, ICP, IAP
- Maximum 32KB RAM memory with parity check to enhance system stability
- GPIO: 72 IO/80 PIN, 56 IO/64 PIN, 40 IO/48 PIN, 26 IO/32 PIN
- Clock, Crystal
 - ▶ XTH: 8-32MHz
 - ▶ XTL: 32.768kHz
 - ▶ RCH: 4/8/16/22.12/24MHz
 - ▶ RC48M: 4/6/32/48MHz
 - ▶ RCL: 32.768/38.4kHz
 - ▶ PLL: 8-48MHz
 - ▶ Hardware supports internal and external clock calibration and monitoring
- Timer/Counter
 - ▶ Three 1-channel complementary output general-purpose 16-bit timers
 - ▶ One 3-channel complementary output general-purpose 16-bit timer
 - ▶ Two low-power 16-bit timers, support cascading
 - ▶ One ultra-low-power pulse counter PCNT, with automatic timing wake-up function in low-power mode, the maximum timing is 1024 seconds
- ▶ Three high-performance 16-bit timers/counters, support PWM complementary, dead zone protection function
- ▶ One programmable 16-bit timer PCA, support 5-channel capture and compare, 5-channel PWM output
- ▶ One 20-bit programmable watchdog circuit, built-in dedicated 10kHz oscillator to provide WDT counting
- ▶ One 7-bit programmable window watchdog
- Communication interface
 - ▶ Up to 4-channel UART standard communication interface
 - ▶ Up to 2-channel LPUART low power communication interface, can work in DeepSleep mode
 - ▶ Up to 2-channel SPI standard communication interface
 - ▶ 2-channel I2C standard communication interface
- Buzzer frequency generator supports complementary output
- Hardware perpetual calendar RTC
- Hardware CRC16/CRC32 module
- AES-128/192/256 hardware coprocessor
- TRNG
- 2-channel DMAC
- 4*47/6*45/8*43 LCD driver
- Globally unique 10-byte ID number
- 12-bit 1Msps sampling high-speed SAR and ADC, built-in Input follower, can measure signals with high output impedance
- 12-bit 500ksps DAC
- Integrate a multifunctional operational amplifier, which can be used as the output buffer of DAC
- Integrated 3-channel voltage comparators with 6-bit Resistor divider and programmable comparison reference
- Integrated low voltage detector, can be configured with 16-step comparison voltage, can monitor port voltage and power supply voltage

- SWD debugging solution provides a full-featured debugger
- Operating conditions: -40-85°C, 1.8-5.5V
- Package: LQFP80/64/48/32

Support Model

HC32L186MCTH-LQFP80	HC32L186MATH-LQFP80
HC32L186KCTH-LQFP64	HC32L186KATH-LQFP64
HC32L180JCTH-LQ48	HC32L180JATH-LQ48
HC32L180FCTH-LQ32	HC32L180FATH-LQ32

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Preface

Number Format

- 0x prefix is used for hexadecimal numbers
- 0b prefix is used for binary numbers
- Numbers without prefix are in decimal representation

Security Statement

There may be potential security problems due to the use of a certain function or protocol, which need to be declared to remind users and avoid security risks.

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1 Product Overview

1.1 Product Lineup

Product Name

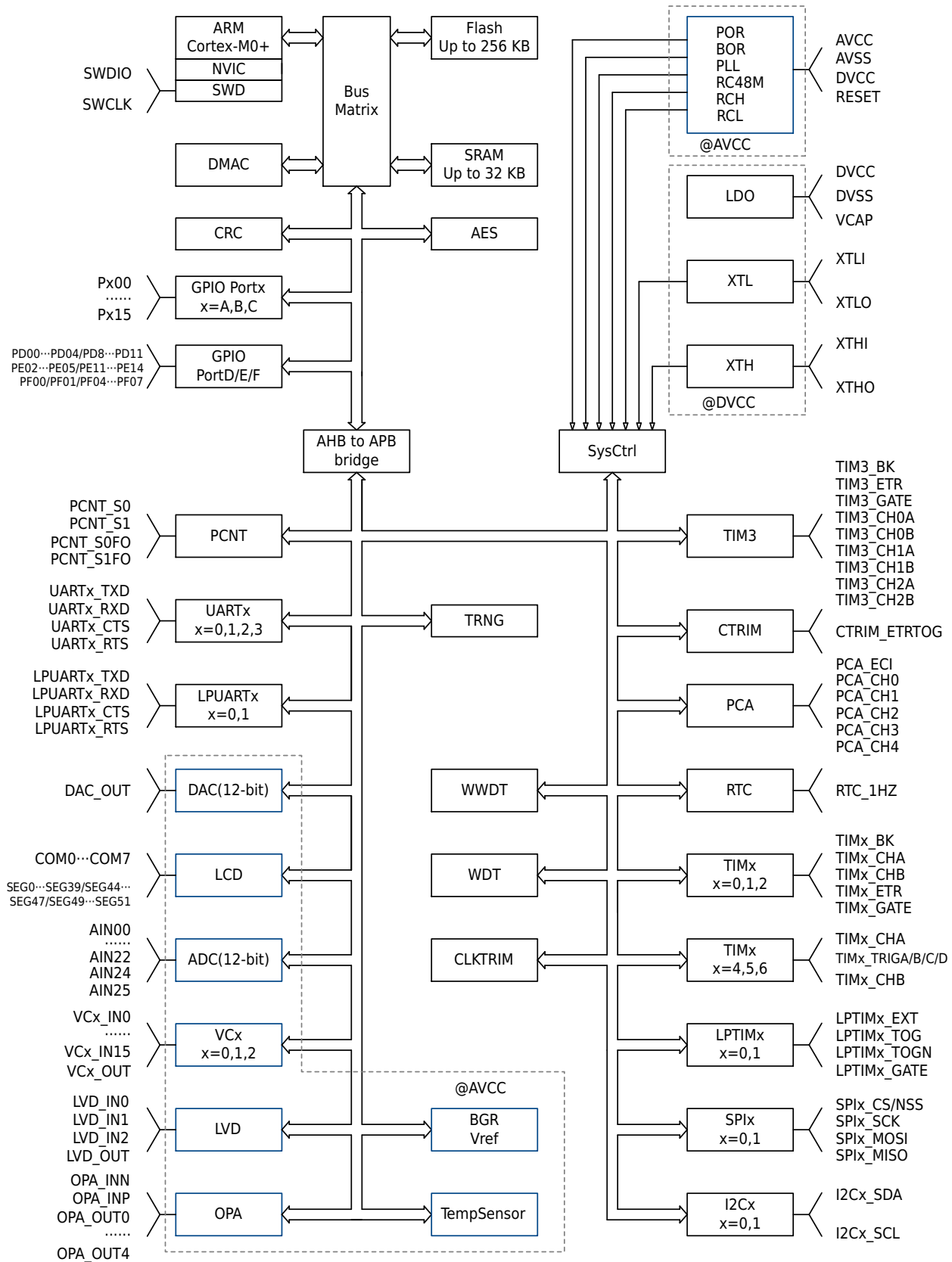
	HC	32	L	1	8	6	M	C	T	H
XiaoHua Semiconductor										
MCU Family										
32: 32-bit										
Product Type										
L: Ultra-low power										
MCU Platform										
1: Cortex-M0+										
MCU Specification Grade										
8: Top Configuration										
Feature Configuration										
0: Configuration 0										
6: Configuration 6										
Pins										
M: 80 Pin										
K: 64 Pin										
J: 48 Pin										
F: 32 Pin										
Program Capacity										
C: 256KB										
A: 128KB										
Package										
T: LQFP										
Temperature Grade										
H: -40-85 °C, enhanced industrial level										

Model Function Comparison Table

Product Name		HC32L186MCTH	HC32L186KCTH	HC32L180JCTH	HC32L180FCTH
Pins		80	64	48	32
GPIOs		72	56	40	26
CPU	Core	Cortex-M0+			
	Frequency	48MHz			
Memory	Flash	256KB			
	RAM	32KB			
Clock	RCH	4/8/16/22.12/24MHz			
	RC48M	4/6/32/48MHz			
	RCL	32.768/38.4kHz			
	PLL	8-48MHz			
	XTH	8-32MHz			
	XTL	32.768kHz			
Power Voltage Range		1.8-5.5V			
Single/dual Power Supply		Single power supply			
Temperature Range		-40-85°C			
Port Interrupt		72	56	40	26
DMA Controller		2ch			
Timer		General Timer TIM0/1/2/3 Advanced Timer TIM4/5/6 Low Power Timer LPTIM0/1			
RTC		1			
Watchdog Timer		IWDT *1 WWDT *1			
PCNT		1			
Connectivity		UART0/1/2/3 LPUART0/1 I2C0/1 SPI0/1	UART0/1 LPUART0/1 I2C0/1 SPI0/1	UART0/1 LPUART1 I2C0/1 SPI0	
ADC, 12-bit		25ch	23ch	17ch	10ch
DAC, 12-bit		1			
OPA		1		-	
VC		VC0/1/2			
LCD		4*47/6*45/8*43	4*40/6*38/8*36	-	-
LVD		1			
Buzzer		Support			
Flash Security Protection		Support			
RAM Parity		Support			
CRC		Support			
TRNG		Support			
AES		Support			
CLKTRIM/CTRIM		Support			
Debug Function		SWD debug interface			
Unique Identification Code		Support			
Package (mm*mm)		LQFP80 (12*12)	LQFP64 (10*10)	LQFP48 (7*7)	LQFP32 (7*7)

Product Name		HC32L186MATH	HC32L186KATH	HC32L180JATH	HC32L180FATH
Pins		80	64	48	32
GPIOs		72	56	40	26
CPU	Core	Cortex-M0+			
	Frequency	48MHz			
Memory	Flash	128KB			
	RAM	32KB			
Clock	RCH	4/8/16/22.12/24MHz			
	RC48M	4/6/32/48MHz			
	RCL	32.768/38.4kHz			
	PLL	8-48MHz			
	XTH	8-32MHz			
	XTL	32.768kHz			
Power Voltage Range		1.8-5.5V			
Single/dual Power Supply		Single power supply			
Temperature Range		-40-85℃			
Port Interrupt		72	56	40	26
DMA Controller		2ch			
Timer		General Timer TIM0/1/2/3 Advanced Timer TIM4/5/6 Low Power Timer LPTIM0/1			
RTC		1			
Watchdog Timer		IWDT *1 WWDT *1			
PCNT		1			
Connectivity		UART0/1/2/3 LPUART0/1 I2C0/1 SPI0/1	UART0/1 LPUART0/1 I2C0/1 SPI0/1	UART0/1 LPUART1 I2C0/1 SPI0	
ADC, 12-bit		25ch	23ch	17ch	10ch
DAC, 12-bit		1			
OPA		1	-		
VC		VC0/1/2			
LCD		4*47/6*45/8*43	4*40/6*38/8*36	-	-
LVD		1			
Buzzer		Support			
Flash Security Protection		Support			
RAM Parity		Support			
CRC		Support			
TRNG		Support			
AES		Support			
CLKTRIM/CTRIM		Support			
Debug Function		SWD debug interface			
Unique Identification Code		Support			
Package (mm*mm)		LQFP80 (12*12)	LQFP64 (10*10)	LQFP48 (7*7)	LQFP32 (7*7)

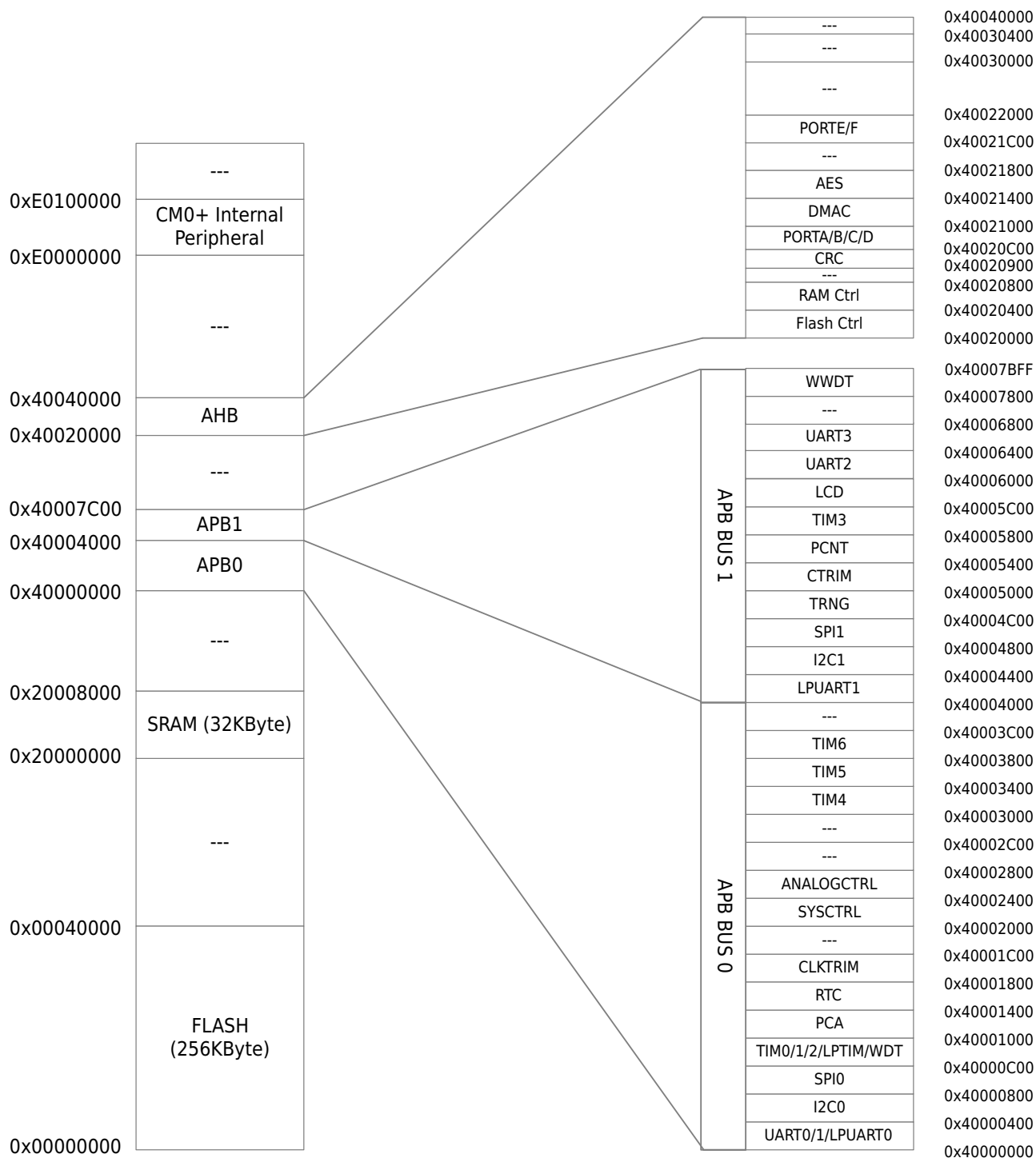
1.2 Functional Block Diagram



Note

Products in different packages support varying resources. For detailed specifications, please refer to [Model Function Comparison Table](#).

1.3 Memory Map



Note

PORTA/B/C/D and PORTE/F modules use two separate address spaces.

Products in different packages support varying FLASH and SRAM sizes. Pay attention to the address space ranges during use. For details, refer to the [Model Function Comparison Table](#).

2 Functional Description

2.1 32-bit Cortex-M0+ Core

The ARM Cortex-M0+ processor is based on the Cortex-M0 and integrates a 32-bit RISC processor with a computing performance of 0.95 Dhrystone MIPS/MHz. It also incorporates multiple new designs, including improved debugging and tracing capabilities, reduced instructions per cycle (IPC) count, an enhanced two-stage pipeline for Flash access, and integrates energy-saving technologies. The Cortex-M0+ processor fully supports Keil & IAR debuggers.

The Cortex-M0+ includes a hardware debug circuit supporting the 2-pin SWD debug interface.

ARM Cortex-M0+ support features:

Instruction set	Thumb/Thumb-2
Assembly line	2-stage assembly line
Performance efficiency	2.46 CoreMark/MHz
Performance efficiency	0.95 DMIPS/MHz in Dhrystone
Interrupt	32 fast interrupts
Interrupt priority	Configurable 4-level interrupt priority
Enhanced instruction	Single-cycle 32-bit multiplier
Debugging	Serial-wire debug port, supports four break points and two watch points.

2.2 256KB/128KB FLASH

Built-in fully integrated FLASH controller, no need for external high voltage input, high voltage generated by the fully built-in circuit for programming. Supports ISP, IAP, ICP functions.

2.3 32KB RAM

According to different ultra-low power modes selected by customers, RAM data will be retained. With hardware parity bit, in case the data is accidentally damaged, when the data is read, the hardware circuit will immediately generate an interrupt to ensure the reliability of the system.

2.4 Clock System

- An internal configurable RCH clock with selectable frequencies of 4/8/16/22.12/24MHz.
- A high-precision internal RC48M clock with configurable frequencies of 4/6/32/48MHz.
- An internal RCL clock with frequencies of 32.768/38.4kHz.
- An external crystal oscillator XTH with a frequency range of 8-32MHz.
- An external 32.768kHz crystal oscillator XTL, primarily providing the RTC real-time clock.
- A PLL with an output frequency range of 8-48MHz.

2.5 Operating Mode

1. Active Mode: CPU running, peripheral functional modules running.
2. Sleep mode: CPU halted, peripheral functional modules running.
3. DeepSleep mode: CPU halted, high-speed clock modules disabled.

2.6 RTC

The RTC (Real-Time Clock) is a functional module supporting BCD data format, typically using a 32.768kHz crystal as its clock. It enables perpetual calendar functionality with configurable interrupt periods: month/day/hour/minute/second. 24/12 hour time mode, the hardware automatically corrects leap years. It features precision compensation, with maximum accuracy of 0.96ppm. Precision compensation can be performed using either the internal or external temperature sensor. Software adjustments of +1/-1 are available for year/month/day/hour/minute/second, with a minimum adjustable precision of one second.

The RTC calendar recorder used to indicate time and date does not reset the register when the MCU is reset by external factors.

2.7 GPIO

It can provide up to 72 GPIO ports, some of which are multiplexed with analog ports. Each port is controlled by independent control register bits and supports FAST IO. Supports edge-triggered interrupts and level-triggered interrupts, and can wake up the MCU to working mode from various ultra-low power consumption modes. Supports bit set, bit clear, and bit set clear operations. Supports CMOS Push-Pull output, Open-Drain output. Built-in pull-up resistor, pull-down resistor, with Schmitt trigger input filter function. The output drive capability is configurable, and the maximum current drive capability is 16mA. All general-purpose IOs can support external asynchronous interrupts.

2.8 NVIC

The Cortex-M0+ processor integrates a Nested Vectored Interrupt Controller (NVIC) supporting up to 32 interrupt request (IRQ) inputs. With 4 interrupt priority levels, it can handle complex logic for real-time control and interrupt processing.

2.9 RESET

This product features 8 reset signal sources. Each reset signal can restart the CPU, reset most registers, and point the program counter (PC) to the starting address.

- Digital area power-on and power-off reset POR
- External Reset PAD, low level is reset signal
- WWDT reset
- WDT reset
- PCA reset
- LVD low voltage reset
- Cortex-M0+ SYSRESETREQ software reset
- Cortex-M0+ LOCKUP hardware reset

2.10 DMAC

The DMAC (Direct Memory Access Controller) function block can transmit data at high speed without passing through the CPU. Using DMAC can improve system performance.

- The DMAC is equipped with an independent bus, so even when the CPU bus is used, the DMAC can also perform transfer operations.
- Composed of 2 channels, capable of performing 2 independent DMA transfers.

- The transmission destination address, transmission source address, transmission data size, transmission request source, and transmission mode can be set, and the transmission operation start of each channel, the forced termination of transmission and the suspension of transmission can be controlled.
- It can control the start, forcibly terminate and pause of batch transmission of all channels.
- When multiple channels are operated at the same time, a fixed method or a cyclic method can be used to select the priority of the operating channel.
- Supports hardware DMA transfer using peripheral interrupt signals.
- Comply with system bus (AHB) and support 32-bit address space (4GB).

2.11 Timer

Name	Width	Prescaler	Count Direction	PWM	Capture	Complementary Output
TIM0	16/32	1/2/4/8/16/32/64/256	Up count/ Count down/ Up and down count	2	2	1
TIM1	16/32	1/2/4/8/16/32/64/256	Up count/ Count down/ Up and down count	2	2	1
TIM2	16/32	1/2/4/8/16/32/64/256	Up count/ Count down/ Up and down count	2	2	1
TIM3	16/32	1/2/4/8/16/32/64/256	Up count/ Count down/ Up and down count	6	6	3
LPTIM0	16	1/2/4/8/16/32/64/256	Up count	No	No	No
LPTIM1	16	1/2/4/8/16/32/64/256	Up count	No	No	No
PCA	16	2/4/8/16/32	Up count	5	5	No
TIM4	16	1/2/4/8/16/64/256/1024	Up count/ Count down/ Up and down count	2	2	1
TIM5	16	1/2/4/8/16/64/256/1024	Up count/ Count down/ Up and down count	2	2	1
TIM6	16	1/2/4/8/16/64/256/1024	Up count/ Count down/ Up and down count	2	2	1

General timer includes four timers: TIM0/1/2/3, supporting the following functions:

- PWM independent output, complementary output
- Capture input
- Pulse width measurement
- Quadrature encoder counting function
- Single pulse mode

- External counting function
- DMA trigger
- Dead-time control
- Braking control
- Cycle-by-cycle current limiting
- Edge alignment, symmetric center alignment and asymmetric center alignment PWM output

TIM0/1/2 have exactly the same function. TIM0/1/2 is a synchronous timer/counter, which can be used as a 16-bit timer/counter with automatic reloading function, or as a 32-bit timer/counter without reloading function. Each timer of TIM0/1/2 has 2 channels of capture and comparison function, which can generate 2 channels of independent PWM output or 1 group of complementary PWM outputs. With dead zone control function.

TIM3 is a multi-channel general-purpose timer with all functions of TIM0/1/2, capable of generating 3 sets of complementary PWM outputs or 6 independent PWM channels, with up to 6 input capture channels. With dead zone control function.

The low-power timer LPTIM is an asynchronous 16-bit timer/counter that can continue timing/counting via the internal low-speed RC oscillator or external low-speed crystal oscillator even when the system clock is disabled. Wake up the system in low-power mode through interrupts.

The PCA (Programmable Counter Array) supports up to five 16-bit capture/compare modules. The timer/counter can be used as a common clock count/event counter capture/compare function. Each module of the PCA can be independently programmed to provide input capture, output compare, or pulse width modulation. In addition, module 4 has an additional watchdog timer mode.

Advanced Timer contains three timers TIM4/5/6. TIM4/5/6 are high-performance counters with identical functions, capable of generating various clock waveforms through counting. One timer can produce either a complementary pair of PWM outputs or two independent PWM channels, and can capture external inputs for pulse width or period measurement.

The basic functions and features of the Advanced Timer are shown in the table below:

Table 2-3 Advanced Timer Basic Features

Basic Features	Description
Waveform mode	Sawtooth wave, triangle wave
Basic function	Up/down counting direction
	Software synchronization
	Hardware Synchronization
	Cache function
	Capture input
	Pulse width/period measurement
	External input counting
	Quadrature encoding count
	General PWM output
	Dead-time control
	Protection mechanism

Basic Features	Description
Basic function	AOS associated action
Interrupt type	Count comparison match interrupt
	Count period match interrupt
	Dead-time error interrupt
	Same high same low interrupt

2.12 PCNT

The PCNT (Pulse Counter) module is used to count external pulses and supports single-channel and dual-channel (quadrature code and non-interleaved code) pulses. It can count in low-power Sleep mode without software involvement.

Pulse counter characteristics:

- Supports 16-bit counter supporting reload function
- Single-channel pulse counting
- Dual channel non-intersecting pulse counting
- Dual channel quadrature pulse counting without missing codes
- Up/Down counting overflow interrupt
- Pulse timeout interrupt
- Four decoding error interrupt, non-intermittent pulse mode
- One direction change interrupt, quadrature pulse mode
- Multi-stage pulse width filtering
- Configurable input pulse polarity
- Support low-power consumption mode counting
- Support waking up MCU in low power mode
- Support any pulse edge spacing not less than one count clock cycle
- With automatic timing wake-up function in low-power consumption mode, the maximum timing is 1024 seconds

2.13 WDT

The WDT (Watch Dog Timer) is a configurable 20-bit timer that provides a reset in case of MCU malfunction, with a built-in 10kHz low-speed clock input as the counter clock. In debug mode, it can be configured to pause or continue running; the WDT can only be restarted by writing a specific sequence.

WWDT is a 7-bit timer. When external interference or unforeseen logic conditions cause the application program to deviate from the normal running sequence, WWDT can detect such software failures and generate interrupts or resets.

2.14 UART

4-channel Universal Asynchronous Receiver/Transmitter, UART0-UART3.

Basic functions of UART:

- Support synchronous half-duplex, asynchronous full-duplex and single-line half-duplex transmission.
- Programmable serial communication function

- ▶ 2 character lengths: 8 bits, 9 bits
- ▶ 3 check methods: no check, odd check, even check
- ▶ 3 stop lengths: 1 bit, 2 bits, 1.5 bits
- 16-bit baud rate counter
- Support hardware flow control (RTS, CTS)
- Support multi-machine communication and automatic address recognition
- Support data transfer via DMA

2.15 LPUART

2-channel Low-Power Universal Asynchronous Receiver/Transmitter (LPUART) that can operate in low-power mode.

Basic functions of LPUART:

- Configuration clock PCLK
- Transmission clock SCLK (SCLK can select XTL, RCL and PCLK)
- Support synchronous half-duplex, asynchronous full-duplex and single-wire half-duplex transmission.
- Programmable serial communication function
 - ▶ 2 character lengths: 8 bits, 9 bits
 - ▶ 3 check methods: no check, odd check, even check
 - ▶ 3 stop lengths: 1 bit, 1.5 bits, 2 bits
- Supports transmitting and receiving data in low power mode
- 16-bit baud rate counter
- Support hardware flow control (RTS, CTS)
- Support multi-machine communication and automatic address recognition
- Support data transfer via DMA

2.16 SPI

2-channel Serial Peripheral Interface(SPI).

Basic features of SPI:

- Support SPI master mode, SPI slave mode
- Support standard four-wire full-duplex communication
- Support configuration of serial clock polarity and phase
- The maximum division factor in master mode is $PCLK/2$
- The maximum division factor in slave mode is $PCLK/4$
- Set the frame length to 8 bits
- Support DMA hardware transmission handshake

2.17 I2C

2-channel I2C, using serial synchronous clock, can realize data transmission between devices at different rates.

Basic features of I2C:

- Support 4 working modes of master sending/receiving and slave sending/receiving
- Support 3 operating rates: Standard (100kbps)/Fast (400kbps)/Fast enhanced (1Mbps)
- Support 7-bit addressing function

- Support noise filtering function
- Support 3 slave addresses
- Support broadcast address
- Support interrupt status query function

2.18 Buzzer

Four general-purpose timers and two low-power timers function multiplexing output to provide programmable driving frequency for Buzzer. The buzzer port can provide 16mA sink current, complementary output, no additional transistor is needed.

2.19 CLKTRIM

The built-in Clock Calibration Circuit Module (CLKTRIM) can calibrate the internal RC clock using an external precise crystal oscillator clock, and can also use the internal RC clock to verify whether the external crystal oscillator clock is functioning properly.

Basic features of clock calibration:

- Calibration mode
- Monitoring mode
- 32-bit reference clock counter can be loaded with initial value
- 32-bit clock counter to be calibrated with configurable overflow value
- 6 reference clock sources
- 5 clock sources to be calibrated
- Support interrupt mode

2.20 CTRIM

In calibration mode, this module automatically performs real-time calibration of the RCH/RC48M/RCL output frequency, making RCH/RC48M/RCL's accuracy immune to environmental variations. When the module works in timer mode, it has general timing function and can still work normally in DeepSleep mode.

2.21 Electronic Signature

Each chip has a unique 10-byte device identification number before leaving the factory, including wafer lot information, chip coordinate information, and so on. The UID addresses are: 0x00101E94-0x00101E9D.

2.22 CRC

CRC16 conforms to the polynomial given in ISO/IEC13239: $x^{16} + x^{12} + x^5 + 1$.

CRC32 conforms to the polynomial given in ISO/IEC13239: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$.

2.23 AES

Advanced Encryption Standard (AES) is a new data encryption standard officially announced by the National Institute of Standards and Technology (NIST) on November 26, 2001. The block size of AES is fixed at 128 bits, while the key length supports 128/192/256 bits.

2.24 TRNG

TRNG is a true random number generator, used to generate true random numbers.

2.25 ADC

A monotonic no missing code 12-bit successive approximation register analog-to-digital converter achieves a sampling rate of 1 Msps when operating with a 24MHz ADC clock. The reference voltage can be selected from the on-chip precision voltage (1.5V or 2.5V) or from an external input or power supply voltage.

- 12-bit conversion accuracy
- 1Msps conversion speed
- Up to 28 input channels are supported, including 25 external pin inputs, 1 internal temperature sensor voltage, 1 1/3 AVCC voltage, 1 DAC internal output
- 4 reference sources: AVCC voltage, EXVREF pins, internal 1.5V reference voltage, internal 2.5V reference voltage
- ADC voltage input range: 0-Vref
- Built-in signal follower, which can convert high-impedance signals
- Multiple conversion modes: single conversion, SQR scan continuous conversion, JQR scan conversion, continuous conversion accumulation
- Software can configure ADC conversion rate
- Support on-chip peripherals to automatically trigger ADC conversion, effectively reducing chip power consumption and improving real-time conversion
- Input channel voltage threshold monitoring

2.26 DAC

1-channel 12-bit 500ksps Digital-to-Analog Converter (DAC) can perform digital-to-analog conversion.

2.27 VC

Built-in 3-channel Analog Voltage Comparator (VC), chip pin voltage monitoring/comparison circuit. 16 configurable positive external input channels (including DAC output voltage), 11 configurable negative external input channels (including DAC output voltage); 4 internal negative input channels, including 1-channel internal temperature sensor voltage, 1-channel ADC reference voltage, 1-channel 64-step resistor divider voltage, and 1 VCAP voltage. The VC output can be used for capture, gating, and external counting clock functions by TIM0/1/2/3, LPTIM, and PCA. Can generate asynchronous interrupts based on rising/falling edges to wake up the MCU from low-power modes. Configurable software anti-shake function.

2.28 LVD

Detects chip supply voltage or pin voltage, supporting the following functions:

- 4 monitoring sources: AVCC, PC13, PB08, PB07
- 16-stage threshold voltage, 1.8-3.3V optional
- 8 trigger conditions, combinations of high level, rising edge and falling edge
- 2 trigger results: reset and interrupt
- 8-stage filter configuration to prevent false triggering
- With hysteresis function, strong anti-interference

2.29 OPA

The Operational Amplifier (OPA) can be flexibly configured for simple filter and voltage follower applications. It can be used as a DAC output buffer or configured as an operational amplifier.

2.30 LCD

The LCD controller is a digital controller/driver designed for monochrome passive liquid crystal display (LCD), featuring up to 8 common terminals (COM) to drive 188 (4x47), 270 (6x45) or 344 (8x43) LCD pixel elements. Can choose either capacitor voltage divider or resistor voltage divider, support internal resistor divider. The internal resistor divider can adjust the contrast. Support DMA hardware data transfer.

Basic features of LCD:

- Highly flexible frame rate control
- Support static, 1/2, 1/3, 1/4, 1/6 and 1/8 duty cycle
- Support 1/2, 1/3 offset
- LCD data RAM with up to 16 registers
- The contrast of LCD can be configured through software
- Three drive waveform generation methods
 - ▶ Internal resistor divider, external resistor divider, external capacitor divider method
 - ▶ The power consumption of the internal resistor divider method can be configured through software to match the capacitive charge required by the LCD panel
- Support low power mode: LCD controller can display in Active, Sleep, DeepSleep mode
- Configurable frame interrupt
- Support LCD blinking function and configurable multiple blinking frequencies
- The unused LCD segments and common pins can be configured as digital or analog functions

2.31 Embedded Debugging System

Embedded debugging solution, providing a full-featured real-time debugger, with standard mature Keil/IAR and other debugging and development softwares. Support four hard breakpoints and multiple soft breakpoints.

2.32 Programming Mode

Support programming modes: online programming and offline programming.

Support programming protocols: ISP protocol, SWD protocol.

Support programming interface: ISP protocol and SWD protocol share SWD port.

When reset, the BOOT0 (PF11) pin is high level, the chip works in ISP programming mode, and Flash can be programmed through ISP protocol.

When reset, the BOOT0 (PF11) pin is low level, the chip works in user mode, the chip executes the program code in the Flash, and the Flash can be programmed through the SWD protocol.

2.33 High Security

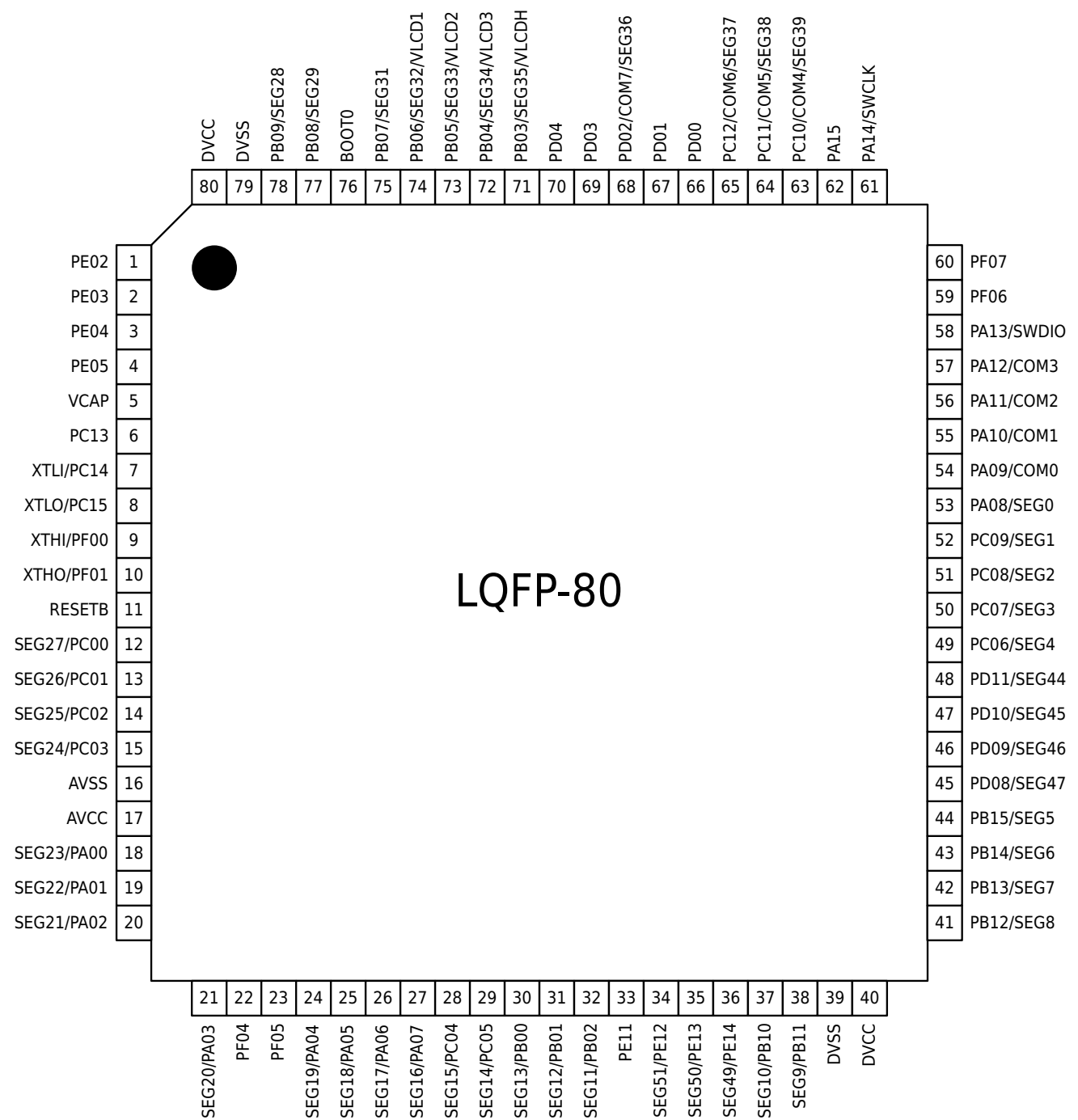
Encrypted embedded debugging solution, providing a full-featured real-time debugger.

3 Pin Definitions

3.1 Pinout

3.1.1 LQFP80 Package

HC32L186MCTH-LQFP80, HC32L186MATH-LQFP80

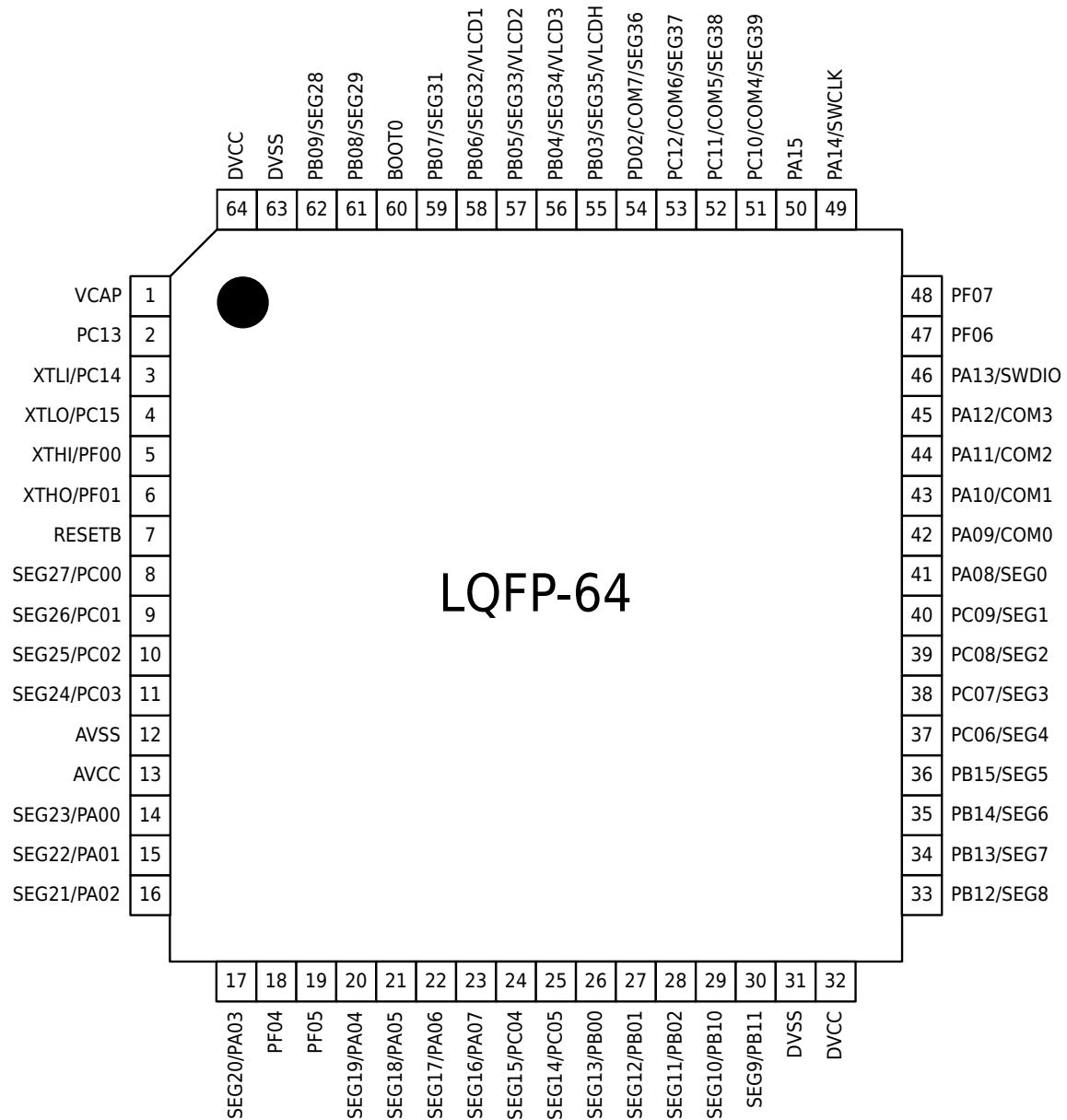


 **Note**

● BOOT0 pin is used to control FLASH programming, see [Module Signal Description](#).

3.1.2 LQFP64 Package

HC32L186KCTH-LQFP64, HC32L186KATH-LQFP64

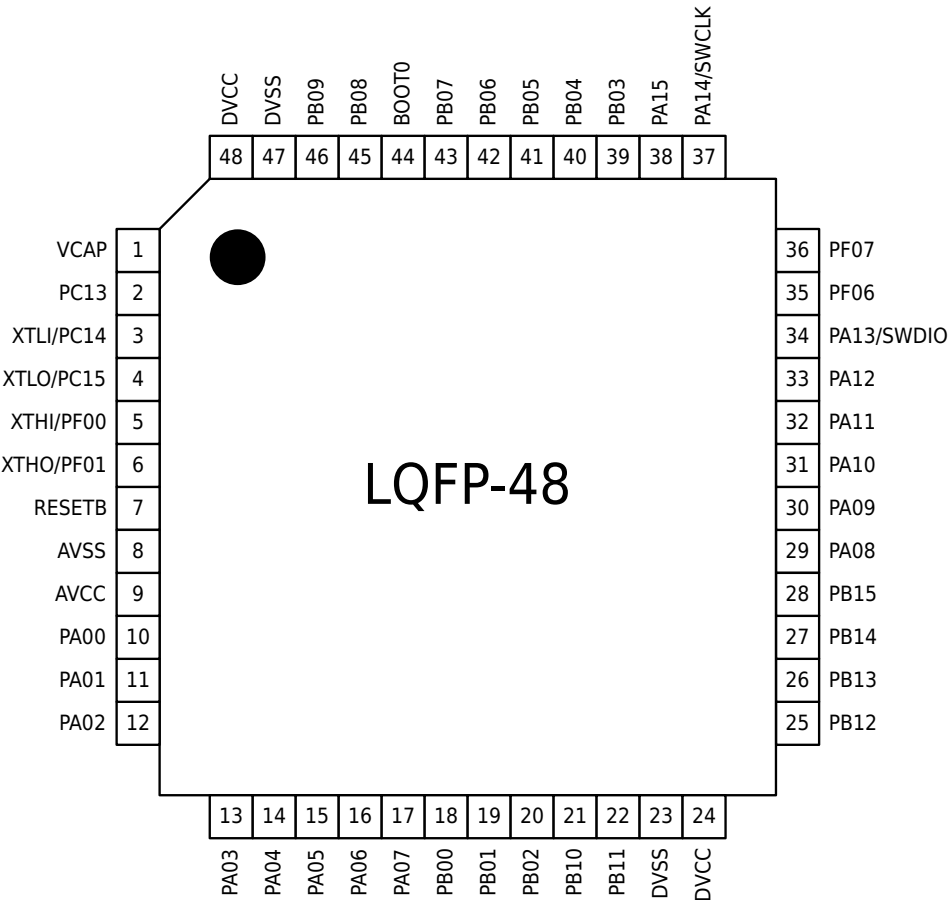


Note

- For details on the IOs not brought out by this package, please refer to [Pin Function Description](#).
- BOOT0 pin is used to control FLASH programming, see [Module Signal Description](#).

3.1.3 LQFP48 Package

HC32L180JCTH-LQ48, HC32L180JATH-LQ48

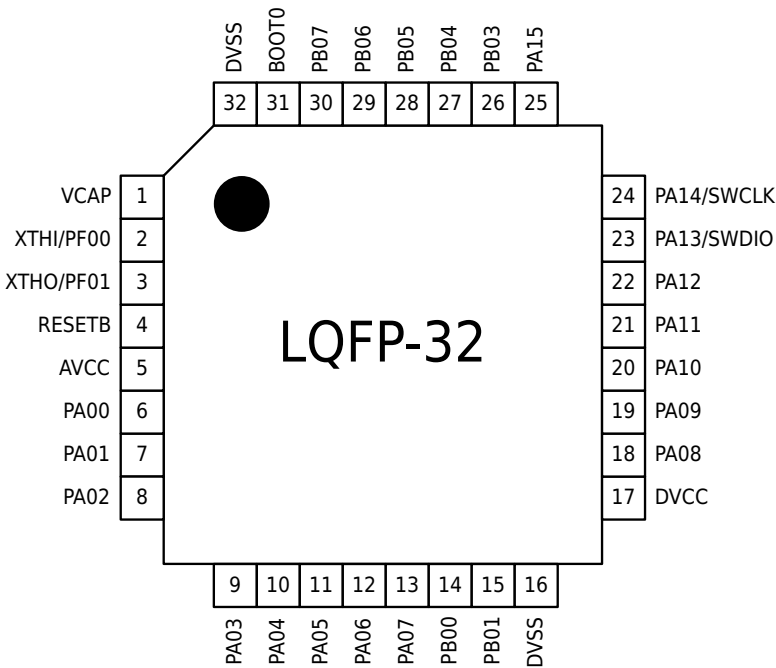


Note

- For details on the IOs not brought out by this package, please refer to [Pin Function Description](#).
- BOOT0 pin is used to control FLASH programming, see [Module Signal Description](#).

3.1.4 LQFP32 Package

HC32L180FCTH-LQ32, HC32L180FATH-LQ32



Note

- For details on the IOs not brought out by this package, please refer to [Pin Function Description](#).
- BOOT0 pin is used to control FLASH programming, see [Module Signal Description](#).

3.2 Pin Function Description

LQFP80	LQFP64	LQFP48	LQFP32	Name	Analog
1				PE02	-
2				PE03	-
3				PE04	-
4				PE05	-
5	1	1	1	VCAP	-
6	2	2		PC13	LVD_IN0
7	3	3		PC14	XTLI
8	4	4		PC15	XTLO
9	5	5	2	PF00	XTHI
10	6	6	3	PF01	XTHO
11	7	7	4	RESETB	-
12	8			PC00	AIN10 VC0_INP0 VC1_INN0 SEG27
13	9			PC01	AIN11 VC0_INP1 VC1_INN1 SEG26
14	10			PC02	AIN12 VC0_INP2 VC1_INN2 SEG25
15	11			PC03	AIN13 VC0_INP3 VC1_INN3 SEG24
16	12	8		AVSS	-
17	13	9	5	AVCC	-
18	14	10	6	PA00	AIN0 VC0_INP4 VC0_INN0 VC1_INP0 VC1_INN4 SEG23
19	15	11	7	PA01	AIN1 VC0_INP5 VC0_INN1 VC1_INP1 VC1_INN5 SEG22
20	16	12	8	PA02	AIN2 VC0_INP6 VC0_INN2 VC1_INP2 SEG21

LQFP80	LQFP64	LQFP48	LQFP32	Name	Analog
21	17	13	9	PA03	AIN3 VC0_INP7 VC0_INN3 VC1_INP3 SEG20
22	18			PF04	-
23	19			PF05	-
24	20	14	10	PA04	AIN4 VC0_INP8 VC0_INN4 VC1_INP4 DAC_OUT OPA_OUT0 SEG19
25	21	15	11	PA05	AIN5 VC0_INP9 VC0_INN5 VC1_INP5 VC2_INP0 VC2_INN0 OPA_OUT1 SEG18
26	22	16	12	PA06	AIN6 VC0_INP10 VC0_INN6 OPA_OUT2 SEG17
27	23	17	13	PA07	AIN7 VC0_INP11 VC0_INN7 OPA_OUT3 SEG16
28	24			PC04	AIN14 VC0_INN8 OPA_OUT4 SEG15
29	25			PC05	AIN15 VC0_INN9 OPA_INN SEG14
30	26	18	14	PB00	AIN8 VC1_INN6 OPA_INP SEG13
31	27	19	15	PB01	AIN9/EXVREF VC1_INP6 VC1_INN7 VC2_INP1 VC2_INN1 SEG12
32	28	20		PB02	AIN16 VC1_INP7 VC1_INN8 SEG11

LQFP80	LQFP64	LQFP48	LQFP32	Name	Analog
33				PE11	VC2_INP4 VC2_INN2
34				PE12	SEG51
35				PE13	AIN25 VC2_INP5 SEG50
36				PE14	AIN24 VC2_INP6 SEG49
37	29	21		PB10	AIN17 VC1_INP8 SEG10
38	30	22		PB11	AIN18 VC2_INP8 VC2_INN4 SEG9
39	31	23	16	DVSS	-
40	32	24	17	DVCC	-
41	33	25		PB12	AIN19 VC1_INP9 SEG8
42	34	26		PB13	AIN20 VC1_INP10 SEG7
43	35	27		PB14	AIN21 VC1_INP11 VC2_INP9 VC2_INN5 SEG6
44	36	28		PB15	AIN22 SEG5
45				PD08	SEG47
46				PD09	VC2_INP10 SEG46
47				PD10	VC2_INP11 VC2_INN6 SEG45
48				PD11	VC2_INP12 VC2_INN7 SEG44
49	37			PC06	SEG4
50	38			PC07	VC2_INP13 VC2_INN8 SEG3
51	39			PC08	SEG2
52	40			PC09	SEG1
53	41	29	18	PA08	SEG0
54	42	30	19	PA09	COM0
55	43	31	20	PA10	COM1
56	44	32	21	PA11	COM2
57	45	33	22	PA12	COM3

LQFP80	LQFP64	LQFP48	LQFP32	Name	Analog
58	46	34	23	PA13/SWDIO	-
59	47	35		PF06	-
60	48	36		PF07	-
61	49	37	24	PA14/SWCLK	-
62	50	38	25	PA15	-
63	51			PC10	COM4/SEG39
64	52			PC11	COM5/SEG38
65	53			PC12	COM6/SEG37
66				PD00	-
67				PD01	-
68	54			PD02	COM7/SEG36
69				PD03	-
70				PD04	-
71	55	39	26	PB03	VC1_INN9 SEG35/VLCDH
72	56	40	27	PB04	VC0_INP12 VC1_INP12 SEG34/VLCD3
73	57	41	28	PB05	VC0_INP13 SEG33/VLCD2
74	58	42	29	PB06	VC0_INP14 VC1_INP14 SEG32/VLCD1
75	59	43	30	PB07	VC1_INP15 LVD_IN2 SEG31
76	60	44	31	BOOT0/PF11	SEG30
77	61	45		PB08	LVD_IN1 SEG29
78	62	46		PB09	SEG28
79	63	47	32	DVSS	-
80	64	48		DVCC	-

The digital function of each pin is controlled by the PSEL bit field, as detailed in the following table.

Table 3-2 Port Multiplexing Table

AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA00	UART1_CTS	LPUART1_TXD	TIM0_ETR	VC0_OUT	TIM1_CHA	TIM3_ETR	TIM0_CHA
PA01	UART1_RTS	LPUART1_RXD	TIM0_CHB	TIM1_ETR	TIM1_CHB	HCLK_OUT	SPI1_MOSI
PA02	UART1_TXD	TIM0_CHA	VC1_OUT	TIM1_CHA	TIM2_CHA	PCLK_OUT	SPI1_MISO
PA03	UART1_RXD	TIM0_GATE	TIM1_CHB	TIM2_CHB	SPI1_CS	TIM3_CH1A	TIM5_CHA
PA04	SPI0_CS	UART1_TXD	PCA_CH4	TIM2_ETR	TIM5_CHA	LVD_OUT	TIM3_CH2B
PA05	SPI0_SCK	TIM0_ETR	PCA_ECI	TIM0_CHA	TIM5_CHB	XTL_OUT	XTH_OUT
PA06	SPI0_MISO	PCA_CH0	TIM3_BK	TIM1_CHA	VC0_OUT	TIM3_GATE	LPUART0_CTS
PA07	SPI0_MOSI	PCA_CH1	HCLK_OUT	TIM3_CH0B	TIM2_CHA	VC1_OUT	TIM4_CHB
PA08	UART0_TXD	TIM3_CH0A	CTRM_ETRTOG	-	TIM1_GATE	TIM4_CHA	TIM3_BK
PA09	UART0_TXD	TIM3_CH1A	TIM0_BK	I2C0_SCL	-	HCLK_OUT	TIM5_CHA
PA10	UART0_RXD	TIM3_CH2A	TIM2_BK	I2C0_SDA	TIM2_GATE	PCLK_OUT	TIM6_CHA
PA11	UART0_CTS	TIM3_GATE	I2C1_SCL	-	VC0_OUT	SPI0_MISO	TIM4_CHB
PA12	UART0_RTS	TIM3_ETR	I2C1_SDA	-	VC1_OUT	SPI0_MOSI	PCNT_S0
PA13	IR_OUT	UART0_RXD	LVD_OUT	TIM3_ETR	RTC_1HZ	PCNT_S1	VC2_OUT
PA14	UART1_TXD	UART0_TXD	TIM3_CH2A	LVD_OUT	RCH_OUT	RCL_OUT	PLL_OUT
PA15	SPI0_CS	UART1_RXD	LPUART1_RTS	TIM0_ETR	TIM0_CHA	TIM3_CH1A	-
PB00	PCA_CH2	TIM3_CH1B	LPUART0_TXD	TIM5_CHB	RCH_OUT	RCL_OUT	PLL_OUT
PB01	PCA_CH3	PCLK_OUT	TIM3_CH2B	TIM6_CHB	LPUART0_RTS	VC2_OUT	TCLK_OUT
PB02	LPTIM0_TOG	PCA_ECI	LPUART1_TXD	TIM4_CHA	TIM1_BK	TIM0_BK	TIM2_BK
PB03	SPI0_SCK	TIM0_CHB	TIM1_GATE	TIM3_CH0A	LPTIM0_GATE	XTL_OUT	XTH_OUT
PB04	SPI0_MISO	PCA_CH0	TIM2_BK	UART0_CTS	TIM2_GATE	TIM3_CH0B	LPTIM0_ETR
PB05	SPI0_MOSI	-	TIM1_BK	PCA_CH1	LPTIM0_GATE	PCNT_S0	UART0_RTS
PB06	I2C0_SCL	UART0_TXD	TIM1_CHB	TIM0_CHA	LPTIM0_ETR	TIM3_CH0A	LPTIM0_TOG
PB07	I2C0_SDA	UART0_RXD	TIM2_CHB	LPUART1_CTS	TIM0_CHB	LPTIM0_TOGN	PCNT_S1
PB08	I2C0_SCL	TIM1_CHA	-	TIM2_CHA	TIM0_GATE	TIM3_CH2A	UART0_TXD
PB09	I2C0_SDA	IR_OUT	SPI1_CS	TIM2_CHA	-	TIM2_CHB	UART0_RXD
PB10	I2C1_SCL	SPI1_SCK	TIM1_CHA	LPUART0_TXD	TIM3_CH1A	LPUART1_RTS	UART1_RTS
PB11	I2C1_SDA	TIM1_CHB	LPUART0_RXD	TIM2_GATE	TIM6_CHA	LPUART1_CTS	UART1_CTS

AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB12	SPI1_CS	TIM3_BK	LPUART0_TXD	TIM0_BK	-	LPUART0_RTS	TIM6_CHA
PB13	SPI1_SCK	I2C1_SCL	TIM3_CH0B	LPUART0_CTS	TIM1_CHA	TIM1_GATE	TIM6_CHB
PB14	SPI1_MISO	I2C1_SDA	TIM3_CH1B	TIM0_CHA	RTC_1HZ	LPUART0_RTS	TIM1_BK
PB15	SPI1_MOSI	TIM3_CH2B	TIM0_CHB	TIM0_GATE	-	-	LPUART1_RXD
PC00	LPTIM0_GATE	PCNT_S0	UART1_CTS	UART2_RTS	-	-	-
PC01	LPTIM0_TOG	TIM5_CHB	UART1_RTS	PCNT_S0FO	-	UART2_CTS	-
PC02	SPI1_MISO	LPTIM0_TOGN	PCNT_S1	UART2_RXD	-	-	-
PC03	SPI1_MOSI	LPTIM0_ETR	LPTIM0_TOGN	PCNT_S1FO	UART2_TXD	-	-
PC04	LPUART0_TXD	TIM2_ETR	IR_OUT	VC2_OUT	-	-	-
PC05	LPUART0_RXD	TIM6_CHB	PCA_CH4	-	-	-	-
PC06	PCA_CH0	TIM4_CHA	TIM2_CHA	LPTIM1_GATE	-	UART3_RXD	-
PC07	PCA_CH1	TIM5_CHA	TIM2_CHB	LPTIM1_ETR	-	UART3_TXD	-
PC08	PCA_CH2	TIM6_CHA	TIM2_ETR	LPTIM1_TOG	-	UART3_CTS	-
PC09	PCA_CH3	TIM4_CHB	TIM1_ETR	LPTIM1_TOGN	-	UART3_RTS	-
PC10	LPUART1_TXD	LPUART0_TXD	PCA_CH2	-	-	-	-
PC11	LPUART1_RXD	LPUART0_RXD	PCA_CH3	PCNT_S0FO	-	-	-
PC12	LPUART0_TXD	LPUART1_TXD	PCA_CH4	PCNT_S1FO	-	-	-
PC13	-	RTC_1HZ	TIM3_CH1B	-	-	-	-
PC14	-	-	-	-	-	-	-
PC15	-	-	-	-	-	-	-
PD00	-	SPI1_CS	-	-	-	-	-
PD01	-	SPI1_SCK	-	-	-	-	-
PD02	PCA_ECI	LPUART0_RTS	TIM1_ETR	-	-	-	-
PD03	UART1_CTS	SPI1_MISO	LPTIM1_TOG	-	-	-	-
PD04	UART1_RTS	SPI1_MOSI	LPTIM1_TOGN	-	-	-	-
PD08	LPUART0_TXD	-	-	-	-	-	-
PD09	LPUART0_RXD	-	-	-	-	-	-
PD10	LPUART0_TXD	-	-	-	-	-	-
PD11	LPUART0_CTS	-	-	-	-	-	-
PE02	PCA_ECI	-	-	-	-	-	-
PE03	PCA_CH0	-	-	-	-	-	-

AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PE04	PCA_CH1	-	-	-	-	-	-
PE05	PCA_CH2	-	-	-	-	-	-
PE11	TIM3_CH1A	-	-	-	-	-	-
PE12	TIM3_CH2B	SPI0_CS	UART3_CTS	-	-	-	-
PE13	TIM3_CH2A	SPI0_SCK	UART3_RTS	-	-	-	-
PE14	TIM3_CH0B	SPI0_MISO	UART3_RXD	-	-	-	-
PF00	I2C0_SDA	CTRM_ETRTOG	UART1_TXD	-	-	-	-
PF01	I2C0_SCL	TIM4_CHB	UART1_RXD	-	-	-	-
PF04	-	-	-	-	-	-	-
PF05	-	-	-	-	-	-	-
PF06	I2C1_SCL	LPUART1_CTS	UART0_CTS	-	-	-	-
PF07	I2C1_SDA	LPUART1_RTS	UART0_RTS	-	-	-	-
PF11	-	-	-	-	-	-	-

3.3 Module Signal Description

Table 3-3 Module Signal Description

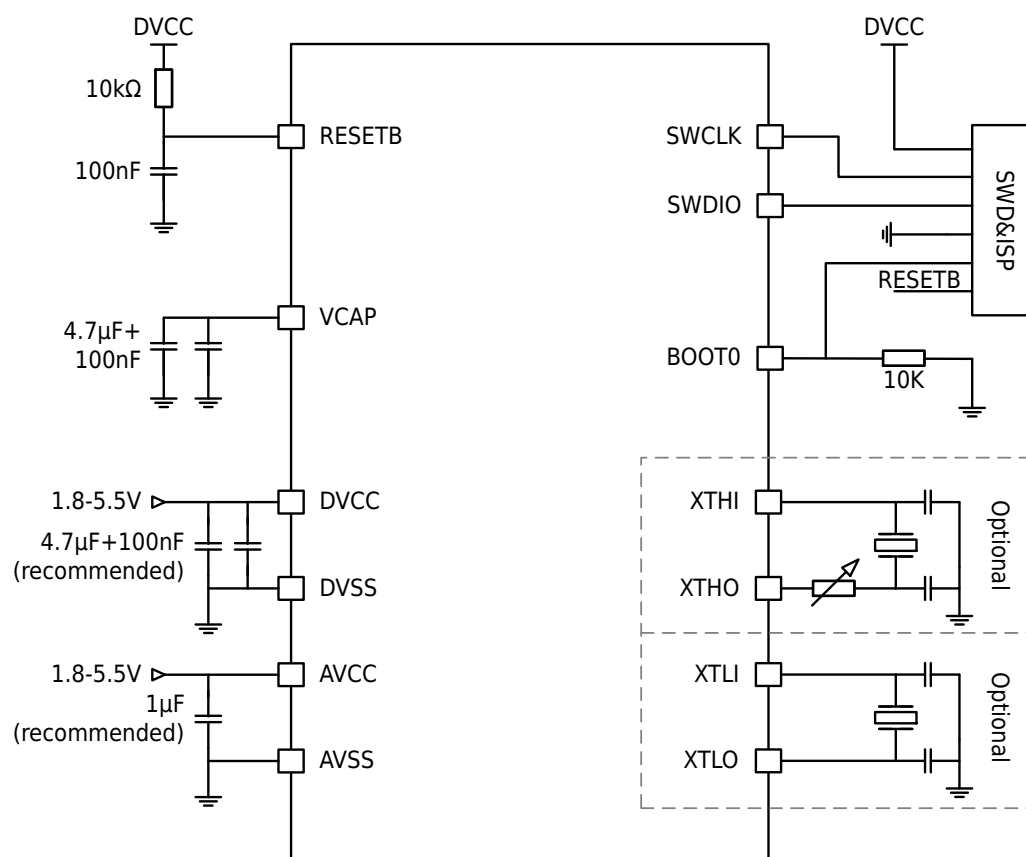
Modules	Pin Name	Description
Power supply	DVCC	Digital power supply
	AVCC	Analog power
	DVSS	Digital ground
	AVSS	Analog ground
	VCAP	LDO core power supply output (only for internal circuit use, external voltage stabilization capacitor is required)
ISP	BOOT0	When reset, the BOOT0 (PF11) pin is high level, the chip works in ISP programming mode, and Flash can be programmed through ISP protocol When reset, the BOOT0 (PF11) pin is low level, the chip works in user mode, the chip executes the program code in the Flash, and the Flash can be programmed through the SWD protocol
ADC	AINx (x=0-22, 24-25)	ADC input channel
	EXVREF	ADC external reference voltage
VC	VCx_INNy (x=0-1 y=0-9)	VC0/1 negative terminal input
	VC2_INNy (y=0-8)	VC2 negative terminal input
	VC0_INPy (y=0-14)	VC0 positive terminal input
	VC1_INPy (y=0-12, 14, 15)	VC1 positive terminal input
	VC2_INPy (y=0-13)	VC2 positive terminal input
	VCx_OUT (x=0-2)	VCx compare output
LVD	LVD_INx (x=0-2)	Voltage detection input
	LVD_OUT	Voltage detection output
OPA	OPA_INN	OPA negative terminal input
	OPA_INP	OPA positive terminal input
	OPA_OUTx (x=0-4)	OPA output
LCD	COMx (x=0-7)	LCD common output
	SEgy (y=0-39, 44-47, 49-51)	LCD segment output
	VLCDx (x=1-3, H)	External resistance mode, external capacitor mode uses pins
UART	UARTx_TXD (x=0-3)	UART data transmitter
	UARTx_RXD (x=0-3)	UART data receiver
	UARTx_CTS (x=0-3)	UART transmit hardware flow control
	UARTx_RTS (x=0-3)	UART receive hardware flow control

Modules	Pin Name	Description
LPUART	LPUARTx_TXD (x=0-1)	LPUART data transmitter
	LPUARTx_RXD (x=0-1)	LPUART data receiver
	LPUARTx_CTS (x=0-1)	LPUART transmit hardware flow control
	LPUARTx_RTS (x=0-1)	LPUART receive hardware flow control
SPI	SPIx_MISO (x=0-1)	SPI master input and slave output data signal
	SPIx_MOSI (x=0-1)	SPI master output and slave input data signal
	SPIx_SCK (x=0-1)	SPI clock signal
	SPIx_CS (x=0-1)	SPI chip selection
I2C	I2Cx_SDA (x=0-1)	I2C data signal
	I2Cx_SCL (x=0-1)	I2C clock signal
TIM0-2	TIMx_CHA (x=0-2)	Timer capture input compare output A
	TIMx_CHB (x=0-2)	Timer capture input compare output B
	TIMx_ETR (x=0-2)	Timer external count input signal
	TIMx_GATE (x=0-2)	Timer gate signal
TIM3	TIM3_CHyA (y=0-2)	Timer capture input compare output A
	TIM3_CHyB (y=0-2)	Timer capture input compare output B
	TIM3_ETR	Timer external count input signal
	TIM3_GATE	Timer gate signal
LPTIM	LPTIMx_TOG (x=0-1)	Inverted output signal of LPTimer
	LPTIMx_TOGN (x=0-1)	Toggle output inverted signal of LPTimer
	LPTIMx_ETR (x=0-1)	External count input signal of LPTimer
	LPTIMx_GATE (x=0-1)	Gating signal of LPTimer
PCA	PCA_ECI	External clock input signal
	PCA_CHx (x=0-4)	Capture input/compare output/PWM output 0-4
PCNT	PCNT_Sx (x=0-1)	PCNT Pulse Counting Input 0-1
	PCNT_SxFO (x=0-1)	The shaped pulse signals of S0-S1 can be used for debugging and observation
Advanced timer	TIMx_CHA (x=4-6)	Advanced Timer 4-6 compare output/capture input A
	TIMx_CHB (x=4-6)	Advanced Timer 4-6 compare output/capture input B

**Note**

The IO port is reset to the input high impedance state, while the port states are maintained in Sleep mode and DeepSleep mode.

4 Typical Application Circuit Diagram



Notice

- AVCC and DVCC voltage must be the same.
- Power supply for each group requires external decoupling capacitors. For better anti-interference capability, it is preferable to route the power supply/ground lines through the decoupling capacitors first before connecting them to the chip.

5 Electrical Specifications

5.1 Parameter Conditions

Unless otherwise specified, all voltages are based on VSS.

5.1.1 Minimum and Maximum Values

All Minimum Values and Maximum Values are measured under the worst conditions.

Data resulted from comprehensive evaluation, and/or guaranteed by design are indicated in the table footnotes, and they will not be tested on the production line.

5.1.2 Typical Values

Unless otherwise specified, typical data are given based on $T_A=25^{\circ}\text{C}$ and $V_{CC}=3.3\text{V}$. These data are only used for design guidance and have not been tested.

5.2 Absolute Maximum Ratings

If the load applied to the device exceeds the value given in the list of "Absolute Maximum Ratings", it may cause permanent damage to the device. The maximum load given here is for reference, which does not mean that the functional operation of the device is correct under this condition. Operation of the device under the condition of maximum value for a long time will affect the reliability of the device.

Table 5-1 Voltage and Current Characteristics

Symbol	Parameters	Min	Max	Unit
VCC-VSS	External main supply voltage (including AVCC and DVCC) ⁽¹⁾	-0.3	6.0	V
V _{IN}	Input voltage at other pins ⁽²⁾⁽⁵⁾	VSS-0.3	VCC+0.3	V
ΔVCCx	Voltage difference between different power supply pins	-	50	mV
VSSx-VSS	Voltage difference between different grounding pins	-	50	mV
I _{VCC}	Total current through DVCC/AVCC power line (supply current) ⁽¹⁾	-	100	mA
I _{VSS}	Total current through DVSS/AVSS ground wire (outflow current) ⁽¹⁾	-	100	mA
I _{IO}	Output sink current on any I/O and control pins	-	25	mA
	Output current on any I/O and control pins	-	-25	mA
I _{INJ(PIN)} ⁽²⁾⁽³⁾	Injection current of RESETB pin	-	±5	mA
	Injection current of XTH pin of XTH and XTL pin of XTL.	-	±5	mA
	Injection current of other pins ⁽⁴⁾	-	±5	mA
ΣI _{INJ(PIN)} ⁽²⁾	Total injection current on all I/O and control pin ⁽⁴⁾	-	±25	mA

**Note**

1. All power supply (DVCC, AVCC) and grounding (DVSS, AVSS) pins should always be connected to the power supply system within the external allowable range.
2. $I_{INJ(PIN)}$ should not exceed its limit, that is, ensure that V_{IN} does not exceed its maximum value. If V_{IN} cannot be guaranteed not to exceed its maximum value, it is also necessary to ensure that $I_{INJ(PIN)}$ does not exceed its maximum value externally. When $V_{IN} > VCC$, there is a forward injection current; When $V_{IN} < VSS$, there is a reverse injection current.
3. The reverse injection current will interfere with the simulation performance of the device.
4. When several I/O ports have injection currents at the same time, the maximum value of $\sum I_{INJ(PIN)}$ is the sum of the instantaneous absolute values of the forward injection current and the reverse injection current. This result is based on the features of the maximum value of $\sum I_{INJ(PIN)}$ at four I/O ports of the device.
5. The input voltage of IO with analog input channel of ADC should be between VSS and VCC; otherwise, the conversion accuracy of ADC will be affected.

Table 5-2 Temperature Characteristics

Symbol	Parameters	Value	Unit
T_{STG}	Storage temperature range	-65-+150	°C
T_{Jmax}	Maximum Junction Temperature	105	°C

5.3 Operating Conditions

5.3.1 General Operating Conditions

Table 5-3 General Operating Conditions

Symbol	Parameters	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK0}	Internal APB0 clock frequency	-	0	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	48	MHz
DVCC	Digital operating voltage	-	1.8	5.5	V
AVCC ⁽¹⁾	Analog operating voltage	Must be the same as DVCC ⁽²⁾	1.8	5.5	V
T_A	Ambient temperature ⁽³⁾	Maximum power consumption	-40	85	°C
		Low power consumption ⁽⁴⁾	-40	105	°C
T_J	Junction temperature range	-	-40	105	°C

**Note**

1. When using an ADC, see ADC Electrical Specifications.
2. It is recommended to use the same power supply for DVCC and AVCC, allowing a maximum of 300mV difference between DVCC and AVCC during power-up and normal operation.
3. $T_A(\text{max})$ is suitable for $P_D(\text{max})$. When $P_D < P_D(\text{max})$, ambient temperature T_A may exceed $T_A(\text{max})$ provided junction temperature T_J does not exceed $T_{J(\text{max})}$. Refer to [Packaging Thermal Resistance Coefficient](#) for details.
4. In a state of lower power consumption, as long as T_J does not exceed $T_{J(\text{max})}$, T_A can be extended to this range.

5.3.2 VCAP External Capacitor

Main regulator stability is achieved by connecting external capacitor C_{EXT} to the VCAP pin. The specified values for C_{EXT} are detailed in the following table.

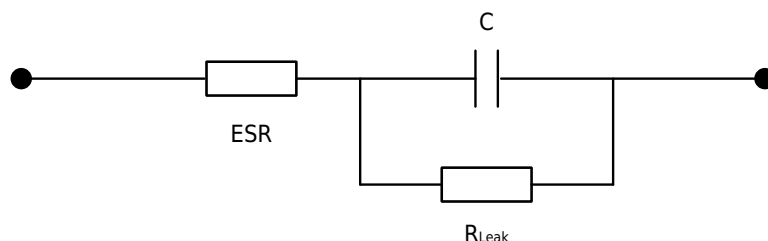


Figure 5-1 External Capacitor C_{EXT}

**Note**

ESR stands for Equivalent Series Resistance.

Table 5-4 VCAP Working Conditions

Symbol	Parameters	Conditions	Min	Max	Unit
$C_{\text{EXT}}^{(1)}$	External capacitance value	-	2.2	10	μF
ESR	External capacitor ESR	-	-	100	$\text{m}\Omega$

**Note**

1. Resulted from comprehensive evaluation, not tested in production.

5.3.3 Working Conditions at Power-on and Power-down

Table 5-5 Working Conditions at Power-On and Power-Down⁽¹⁾

Symbol	Parameters	Conditions	Min	Max	Unit
S_{VCC_r}	VCC rise rate	-	0	5	$\text{V}/\mu\text{s}$
S_{VCC_f}	VCC fall rate	-	0	5	$\text{V}/\mu\text{s}$

**Note**

1. Resulted from comprehensive evaluation, not tested in production.

5.3.4 Embedded Reset and LVD Module Characteristics

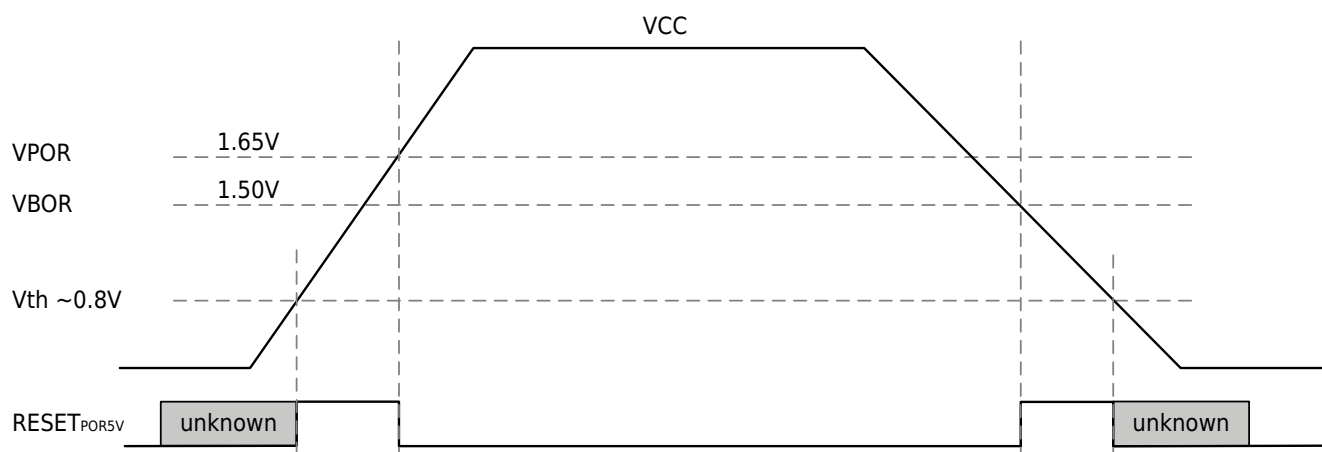


Figure 5-2 POR/Brown Out Schematic Diagram

Table 5-6 POR/Brown Out⁽¹⁾

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
VPOR	POR release voltage (power on process)	-	1.49	1.65	1.75	V
VBOR	BOR detection voltage (power down process)	-	1.45	1.50	1.55	V



Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 5-7 LVD Module Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	unit
V _{ex}	External input voltage range	-	0	-	VCC	V
V _{level}	Detection threshold	LVD_CR.VTDS=0b0000	1.70	1.80	1.90	V
		LVD_CR.VTDS=0b0001 ⁽¹⁾	1.80	1.90	2.00	
		LVD_CR.VTDS=0b0010 ⁽¹⁾	1.90	2.00	2.10	
		LVD_CR.VTDS=0b0011 ⁽¹⁾	2.00	2.10	2.20	
		LVD_CR.VTDS=0b0100 ⁽¹⁾	2.10	2.20	2.30	
		LVD_CR.VTDS=0b0101 ⁽¹⁾	2.20	2.30	2.40	
		LVD_CR.VTDS=0b0110 ⁽¹⁾	2.30	2.40	2.55	
		LVD_CR.VTDS=0b0111 ⁽¹⁾	2.35	2.50	2.65	
		LVD_CR.VTDS=0b1000	2.45	2.60	2.75	
		LVD_CR.VTDS=0b1001 ⁽¹⁾	2.55	2.70	2.85	
		LVD_CR.VTDS=0b1010 ⁽¹⁾	2.65	2.80	2.95	
		LVD_CR.VTDS=0b1011 ⁽¹⁾	2.75	2.90	3.05	
		LVD_CR.VTDS=0b1100 ⁽¹⁾	2.85	3.00	3.15	

Symbol	Parameters	Conditions	Min	Typ	Max	unit
V_{level}	Detection threshold	LVD_CR.VTDS=0b1101 ⁽¹⁾	2.95	3.10	3.25	V
		LVD_CR.VTDS=0b1110 ⁽¹⁾	3.05	3.20	3.35	
		LVD_CR.VTDS=0b1111	3.15	3.30	3.45	
I_{comp}	Power consumption	-	-	0.12	-	μA
$T_{response}$	Response time	Choose to detect the GPIO pin voltage, VCC=3.3V, LVD_CR.VTDS= 0b1000, the detection voltage changes from ($V_{level}+100mV$) to ($V_{level}-100mV$), and the change slope is $2 \times 10^5 V/\mu s$	-	90	-	μs
T_{setup}	Settling time	Choose to detect the GPIO pin voltage, VCC=3.3V, LVD_CR.VTDS= 0b1000, the detection voltage is lower than $V_{level}-100mV$	-	400	-	μs
V_{hys}	Hysteresis voltage	-	-	40	-	mV
T_{filter}	Filter time	LVD_debounce=0b000	-	7	-	μs
		LVD_debounce=0b001	-	14	-	
		LVD_debounce=0b010	-	28	-	
		LVD_debounce=0b011	-	112	-	
		LVD_debounce=0b100	-	450	-	
		LVD_debounce=0b101	-	1800	-	
		LVD_debounce=0b110	-	7200	-	
		LVD_debounce=0b111	-	28800	-	

**Note**

1. Resulted from comprehensive evaluation, not tested in production.

5.3.5 Built-In Reference Voltage

Table 5-8 Built-In Reference Voltage

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{REF25}^{(2)}$	Internal 2.5V Reference Voltage	$V_{CC}=3.3V$ $T_A=25^{\circ}C$	2.475	2.5	2.525	V
$V_{REF25}^{(1)(2)}$	Internal 2.5V Reference Voltage	$V_{CC}=2.8-5.5V$ $T_A=-40-85^{\circ}C$	2.455	2.5	2.545	V
V_{REF15}	Internal 1.5V Reference Voltage	$V_{CC}=3.3V$ $T_A=25^{\circ}C$	1.485	1.5	1.515	V
$V_{REF15}^{(1)}$	Internal 1.5V Reference Voltage	$V_{CC}=1.8-5.5V$ $T_A=-40-85^{\circ}C$	1.473	1.5	1.527	V

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$T_{\text{Coeff}}^{(3)}$	Internal 2.5V 1.5V temperature coefficient	$T_A = -40-85^{\circ}\text{C}$	-	-	120	ppm/ $^{\circ}\text{C}$
$T_{\text{stable(BGR)}}$	BGR stable time	$V_{\text{CC}} = 3.3\text{V}$ $T_A = 25^{\circ}\text{C}$	-	20	-	μs

**Note**

1. Resulted from comprehensive evaluation, not tested in production.
2. The 2.5V range can only be selected when the power supply voltage exceeds 2.8V, otherwise it may cause system malfunction.
3. Guaranteed by design, not tested in production.

5.3.6 Supply Current Characteristics

Current consumption is a comprehensive index of multiple parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin flip rate, and the location of the program in memory and the executed code, etc.

The MCU is in the following conditions:

- All I/O pins are in input mode and connected to a static level-VCC or VSS (no load).
- All peripherals are turned off, unless otherwise specified.
- The access time of the flash memory is adjusted to the frequency f_{HCLK} (0 wait cycle for 0-24MHz, 1 wait cycle for 24-48MHz)
- When peripherals is used: $f_{\text{PCLK0}} = f_{\text{HCLK}}$, $f_{\text{PCLK1}} = f_{\text{HCLK}}$.

Table 5-9 Operating Current Characteristics

Symbol	Parameters	Conditions			Typ ⁽¹⁾⁽³⁾	Max ⁽²⁾⁽³⁾	Unit
I_{DD} (Run in RAM)	All peripherals clock ON, Run while(1) in RAM	$V_{\text{CAP}} = 1.5\text{V}$ $V_{\text{CC}} = 3.3\text{V}$ $T_A = 25^{\circ}\text{C}$	RCH clock source	4M	701.6	-	μA
				8M	1264	-	
				16M	2352.1	-	
				22.12M	3215.6	-	
				24M Flash Wait=0	3465.3	-	
			RC48M clock source	4M	707.6	-	
				6M	976.5	-	
				32M Flash Wait=1	6687.4	-	
				48M Flash Wait=1	6715.6	-	
			PLL RCH4M to xxM clock source	32M Flash Wait=1	4915.8	-	
				48M Flash Wait=1	7272.8	-	
	All peripherals clock OFF, Run while(1) in RAM	$V_{\text{CAP}} = 1.5\text{V}$ $V_{\text{CC}} = 3.3\text{V}$ $T_A = 25^{\circ}\text{C}$	RCH clock source	4M	402.2	-	μA
				8M	665	-	
				16M	1159.6	-	
				22.12M	1552.2	-	

Symbol	Parameters	Conditions			Typ ⁽¹⁾⁽³⁾	Max ⁽²⁾⁽³⁾	Unit
I _{DD} (Run in RAM)	All peripherals clock OFF, Run while(1) in RAM			24M Flash Wait=0	1664.8	-	μA
				RC48M clock source	4M	406.4	
					6M	527.2	
					32M Flash Wait=1	3118.1	
					48M Flash Wait=1	3130.8	
				PLL RCH4M to xxM clock source	32M Flash Wait=1	2531.5	
					48M Flash Wait=1	3701.8	
I _{DD} (Run CoreMark)	All peripherals clock OFF, Run CoreMark in Flash	V _{CAP} =1.5V V _{CC} =3.3V T _A =2xC	RCH clock source	4M	846	-	μA
				8M	1369	-	
				16M	1732	-	
				22.12M	2248	-	
				24M Flash Wait=0	2409	-	
			RC48M clock source	4M	847	-	
				6M	1157	-	
				32M Flash Wait=1	2479	-	
				48M Flash Wait=1	3558	-	
			PLL RCH4M to xxM clock source	16M	2016	-	
				24M Flash Wait=0	2767	-	
				32M Flash Wait=1	2772	-	
				48M Flash Wait=1	3958	-	
I _{DD} (Sleep mode)	All peripherals clock ON	V _{CAP} =1.5V V _{CC} =1.8-5.5 V T _A =-40-85°C	RCH clock source	4M	508.4	646	μA
				8M	901.5	1127	
				16M	1652.4	2045	
				22.12M	2250.7	2779	
				24M Flash Wait=0	2422.3	2990	
			RC48M clock source	4M	513.4	641	
				6M	698.8	867	
				32M Flash Wait=1	4623.9	5757	
				48M Flash Wait=1	4643.1	5787	
			PLL RCH4M to xxM clock source	32M Flash Wait=1	3539.3	4362	
				48M Flash Wait=1	5194.7	6412	

Symbol	Parameters	Conditions			Typ ⁽¹⁾⁽³⁾	Max ⁽²⁾⁽³⁾	Unit
I _{DD} (Sleep mode)	All peripherals clock OFF	V _{CAP} =1.5V V _{CC} =1.8-5.5 V T _A =-40-85°C	RCH clock source	4M	208.1	285	μA
				8M	300.7	399	
				16M	456.3	588	
				22.12M	589.1	754	
				24M Flash Wait=0	622.4	795	
			RC48M clock source	4M	210.5	284	
				6M	247.1	327	
				32M Flash Wait=1	1055.3	1302	
				48M Flash Wait=1	1059	1301	
			PLL RCH12M to xxM clock source	32M Flash Wait=1	1155	1444	
				48M Flash Wait=1	1634.2	2039	
I _{DD} (Run mode)	All peripherals clock ON, Run while(1) in Flash	V _{CAP} =1.5V V _{CC} =1.8-5.5 V T _A =-40-85°C	RCH clock source	4M	940	1215	μA
				8M	1748.1	2240	
				16M	2314.9	2870	
				22.12M	3126.3	3869	
				24M Flash Wait=0	3360.5	4155	
			RC48M clock source	4M	947.6	1204	
				6M	1336.4	1698	
				32M Flash Wait=1	5997	7409	
				48M Flash Wait=1	6022.2	7450	
			PLL RCH4M to xxM clock source	32M Flash Wait=1	4496.4	5513	
				48M Flash Wait=1	6571.9	8057	
	All peripherals clock OFF, Run while(1) in Flash	V _{CAP} =1.5V V _{CC} =1.8-5.5 V T _A =-40-85°C	RCH clock source	4M	640.1	855	μA
				8M	1148.5	1523	
				16M	1122.4	1442	
				22.12M	1466.6	1874	
				24M Flash Wait=0	1564.5	1995	
			RC48M clock source	4M	645.8	847	
				6M	886.4	1165	
				32M Flash Wait=1	2440	3009	
				48M Flash Wait=1	2450	3060	
			PLL RCH12M to xxM clock source	32M Flash Wait=1	2116.8	2651	
				48M Flash Wait=1	3018.2	3770	

Symbol	Parameters	Conditions			Typ ⁽¹⁾⁽³⁾	Max ⁽²⁾⁽³⁾	Unit	
I _{DD} (LP Run)	All peripherals clock ON, Run while(1) in Flash	V _{CAP} =1.5V V _{CC} =1.8-5.5 V T _A =-40-85°C	RCL clock source ⁽⁴⁾	-	112.2	158	μA	
			XTL clock source ⁽⁴⁾	Driver=2	111.8	157		
	All peripherals clock OFF, Run while(1) in Flash		RCL clock source ⁽⁴⁾	-	109.4	155		
			XTL clock source ⁽⁴⁾	Driver=2	109.4	154		
I _{DD} (LP Sleep)	All peripherals clock ON, Run while(1) in Flash	V _{CAP} =1.5V V _{CC} =1.8-5.5 V T _A =-40-85°C	RCL clock source ⁽⁴⁾	-	84.9	121	μA	
			XTL clock source ⁽⁴⁾	Driver=2	84.9	120		
	All peripherals clock OFF,		RCL clock source ⁽⁴⁾	-	82	117		
			XTL clock source ⁽⁴⁾	Driver=2	82.4	117		
I _{DD} (Deep- Sleep)	All peripherals clock OFF	V _{CAP} =1.5V V _{CC} =1.8-5.5 V T _A =-40-85°C	-	NO CLK	0.8	10.8	μA	
	All peripherals clock OFF		-	RCL ⁽⁴⁾	1.2	11		
	All peripherals clock OFF		-	XTL ⁽⁴⁾	1.5	11.2		
	Other peripherals clock OFF		-	RCL ⁽⁴⁾ +WDT	1.3	11.1		
	Other peripherals clock OFF		-	RCL ⁽⁴⁾ +LVD	1.3	11.1		
	Other peripherals clock OFF		-	RCL ⁽⁴⁾ +RTC	1.3	11.1		
	Other peripherals clock OFF		-	RCL ⁽⁴⁾ +LPT	1.3	11.1		
	Other peripherals clock OFF		-	RCL ⁽⁴⁾ +WDT +LVD	1.4	11.2		
	Other peripherals clock OFF		-	XTL ⁽⁴⁾ +WDT	1.5	11.3		
	Other peripherals clock OFF		-	XTL ⁽⁴⁾ +LVD	1.5	11.3		
	Other peripherals clock OFF		-	XTL ⁽⁴⁾ +RTC	1.5	11.3		
	Other peripherals clock OFF		-	XTL ⁽⁴⁾ +LPT	1.5	11.3		
	Other peripherals clock OFF		-	XTL ⁽⁴⁾ +WDT +LVD	1.6	11.4		

**Note**

1. If there are no other specified conditions, the value of the Typ is 25°C & V_{CC}=3.3V measured.
2. If there are no other specified conditions, the value of Max is the maximum value in the range of V_{CC}=1.8-5.5V & Temperature=-40-85°C.
3. Resulted from comprehensive evaluation, not tested in production.
4. RCL and XTL clock testing uses a frequency of 32.768kHz.

5.3.7 Time to Wake-Up from Low-Power Mode

The wake-up time is measured during the wake-up phase of the RCH oscillator. The clock source used when waking up depends on the current operating mode:

- Sleep mode: clock source is RCH oscillator
- DeepSleep mode: clock source is RCH oscillator

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$T_{wu}^{(1)}$	Sleep mode wake-up time	-	-	1.8	-	μs
	DeepSleep mode wake-up time	$F_{RCH}=4MHz$	-	13.0	-	μs
		$F_{RCH}=8MHz$	-	10.5	-	μs
		$F_{RCH}=16MHz$	-	9.4	-	μs
		$F_{RCH}=24MHz$	-	10.3	-	μs



Note

1. Guaranteed by design, not tested in production.
2. The wake-up time is measured from the start of the wake-up event to the user program reading the first instruction.

5.3.8 External Clock Source Characteristics

5.3.8.1 External Input High-Speed Clock

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{XTH_ext}	User external clock frequency ⁽¹⁾	-	0	8	32	MHz
V_{XTHH}	Input pin high level voltage ⁽¹⁾	-	0.7VCC	-	VCC	V
V_{XTHL}	Input pin low level voltage ⁽¹⁾	-	VSS	-	0.3VCC	V
$T_{r(XTH)}$	Rise time ⁽¹⁾	-	-	-	20	ns
$T_{f(XTH)}$	Falling time ⁽¹⁾	-	-	-	20	ns
$T_{w(XTH)}$	Enter high or low time ⁽¹⁾	-	16	-	-	ns
$C_{in(XTH)}$	Input capacitive reactance ⁽¹⁾	-	-	5	-	pF
Duty	Duty Cycle ⁽¹⁾	-	40	-	60	%
I_L	Input Leakage Current ⁽¹⁾	-	-	-	± 1	μA



Note

1. Guaranteed by design, not tested in production.

5.3.8.2 External Input Low-Speed Clock

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$f_{\text{XTL_ext}}$	User external clock frequency ⁽¹⁾	-	0	32.768	1000	kHz
V_{XTLH}	Input pin high level voltage ⁽¹⁾	-	0.7VCC	-	VCC	V
V_{XTLL}	Input pin low level voltage ⁽¹⁾	-	VSS	-	0.3VCC	V
$T_{\text{r(XTL)}}$	Rise time ⁽¹⁾	-	-	-	50	ns
$T_{\text{f(XTL)}}$	Falling time ⁽¹⁾	-	-	-	50	ns
$T_{\text{w(XTL)}}$	Enter high or low time ⁽¹⁾	-	450	-	-	ns
$C_{\text{in(XTL)}}$	Input capacitive reactance ⁽¹⁾	-	-	5	-	pF
Duty	Duty cycle ⁽¹⁾	-	30	-	70	%
I_{L}	Input leakage current ⁽¹⁾	-	-	-	±1	μA



Note

1. Guaranteed by design, not tested in production.

5.3.8.3 External High-Speed Crystal XTH

The external high-speed crystal (XTH) can be generated using a 8-32MHz crystal/ceramic resonator oscillator. The information given in this section is based on the results obtained through comprehensive characteristic evaluation using the typical external components listed in the table below. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and settling time at startup. For detailed parameters (frequency, package, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Table 5-13 External High-Speed Crystal XTH Characteristics⁽¹⁾⁽²⁾

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
F_{CLK}	oscillator frequency	-	8	-	32	MHz
ESR_{CLK}	Supported crystal oscillator ESR range	32MHz	-	-	60	Ω
		24MHz	-	-	80	
		16MHz	-	-	100	
		8MHz	-	-	120	
$C_{\text{LX}}^{(3)}$	Matching Capacitance	Configure as required by the crystal manufacturer.	4	12	20	pF
Duty	Duty cycle	-	40	50	60	%

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$I_{dd}^{(4)}$	electrorheograph	XTH_CR[3:0]=0b1111	-	1000	-	μA
		XTH_CR[3:0]=0b1110	-	600	-	
		XTH_CR[3:0]=0b1010	-	370	-	
		XTH_CR[3:0]=0b0110	-	300	-	
		XTH_CR[3:0]=0b0010	-	160	-	
g_m	Transconductance	XTH_CR[3:0]=0b1111	-	11.75	-	mS
		XTH_CR[3:0]=0b1110 (32MHz, 24MHz recommended value)	-	6.34	-	
		XTH_CR[3:0]=0b1101	-	4.38	-	
		XTH_CR[3:0]=0b1100	-	3.38	-	
		XTH_CR[3:0]=0b1011	-	7.41	-	
		XTH_CR[3:0]=0b1010 (16MHz recommended value)	-	4.01	-	
		XTH_CR[3:0]=0b1001	-	2.77	-	
		XTH_CR[3:0]=0b1000	-	2.14	-	
		XTH_CR[3:0]=0b0111	-	5.59	-	
		XTH_CR[3:0]=0b0110 (12MHz recommended value)	-	3.01	-	
		XTH_CR[3:0]=0b0101	-	2.08	-	
		XTH_CR[3:0]=0b0100	-	1.60	-	
		XTH_CR[3:0]=0b0011	-	2.50	-	
		XTH_CR[3:0]=0b0010 (8MHz recommended value)	-	1.30	-	
		XTH_CR[3:0]=0b0001	-	0.93	-	
		XTH_CR[3:0]=0b0000	-	0.72	-	
$T_{start}^{(5)}$	Start time	32MHz, $C_{Lx}=16pF$ @ XTH_CR[3:0]=0b1110	-	500	-	μs
		8MHz, $C_{Lx}=16pF$ @ XTH_CR[3:0]=0b0010	-	2	-	ms

**Note**

1. The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.
2. Resulted from comprehensive evaluation, not tested in production.
3. C_{Lx} refers to the two pin matching capacitors C_{L1} and C_{L2} of the crystal. It is recommended to use high-quality ceramic capacitors, and select a crystal or resonator that meets the requirements. Usually C_{L1} and C_{L2} have the same parameters. When selecting C_{Lx} , one should take into account parameters such as the crystal oscillator's frequency and ESR, as well as the total parasitic capacitance to ground (C_p) from the PCB and MCU pins.

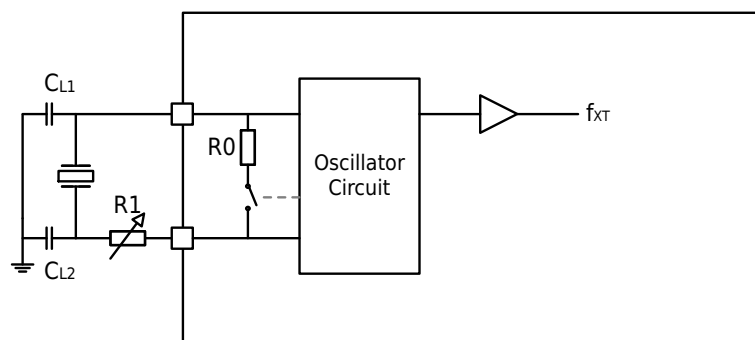
The C_{Lx} is recommended to be configured in accordance with the requirements of the crystal manufacturer's technical manual.

- If the crystal manufacturer gives *the value of the load capacitance* (C_L), the matching capacitance $C_{Lx} = 2 * C_L - C_p$.
- If the crystal manufacturer gives *the value of the matching capacitance*, the matching capacitance $C_{Lx} = \text{matching capacitance value} - C_p$.

In practical applications, if a larger C_{Lx} is selected, it is recommended to choose an appropriate current level setting.

Example:

- When the crystal manufacturer gives the load capacitance of the crystal as 8pF, considering the distributed capacitance between the PCB and MCU pins, it is recommended to choose a matching capacitor with a capacitance of 12pF.
 - When the crystal manufacturer gives the matching capacitance of the crystal as 12pF, considering the distributed capacitance between the PCB and MCU pins, it is recommended to choose a matching capacitor with a capacitance of 10pF or 8pF.
4. Current varies with frequency and drive capability. Higher frequencies result in stronger drive capability but greater current consumption.
 5. T_{start} is the start-up time, which is the time from the software enabling XTH to start measuring until a stable 32MHz/8MHz oscillation is obtained. This value is measured using a standard crystal resonator with the $XTH_CR[5:4] = 0b10$ setting. It may vary greatly depending on the crystal manufacturer and model.

**Note**

- The feedback resistance $R0$ has been integrated in the chip.
- The damping resistance $R1$ is optional, and the value of the resistance depends on crystal characteristic, the default is 0Ω .

5.3.8.4 External Low-Speed Crystal XTL

The external low-speed crystal (XTL) can be generated using a 32.768kHz crystal/ceramic resonator oscillator. The information given in this section is based on typical external components and the results obtained through comprehensive characteristic evaluation. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and settling time at startup. For detailed parameters (frequency, package, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Table 5-14 External Low-Speed Crystal XTL Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
F_{CLK}	Oscillator frequency	-	-	32.768	-	kHz
ESR_{CLK}	Supported crystal oscillator ESR range	-	-	-	60	k Ω
$C_{Lx}^{(2)}$	Matching capacitance	Configure as required by the crystal manufacturer.	4	12	20	pF
DC_{ACLK}	Duty cycle	-	30	50	70	%
$I_{dd}^{(3)}$	electrorheograph	XTL_CR[3:0]=0b1111	-	1330	-	nA
		XTL_CR[3:0]=0b1011	-	1230	-	
		XTL_CR[3:0]=0b0111	-	1140	-	
		XTL_CR[3:0]=0b0011	-	1050	-	
		XTL_CR[3:0]=0b1110	-	630	-	
		XTL_CR[3:0]=0b1010 (Recommended value)	-	580	-	
		XTL_CR[3:0]=0b0110	-	530	-	
		XTL_CR[3:0]=0b0010	-	490	-	
g_m	Transconductance	XTL_CR[3:0]=0b1111	-	14.64	-	μS
		XTL_CR[3:0]=0b1011	-	13.17	-	
		XTL_CR[3:0]=0b0111	-	11.67	-	
		XTL_CR[3:0]=0b0011	-	10.15	-	
		XTL_CR[3:0]=0b1110	-	7.37	-	
		XTL_CR[3:0]=0b1010 (Recommended value)	-	6.62	-	
		XTL_CR[3:0]=0b0110	-	5.87	-	
		XTL_CR[3:0]=0b0010	-	5.10	-	
$T_{start}^{(4)}$	Start time	ESR=30k Ω C_{Lx} =12pF XTL_CR[3:0]=0b1010	-	2000	-	ms

**Note**

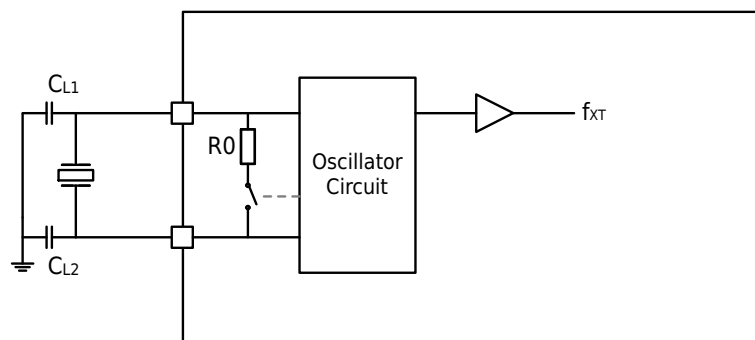
1. Resulted from comprehensive evaluation, not tested in production.
2. C_{Lx} refers to the two pin matching capacitors C_{L1} and C_{L2} of the crystal. It is recommended to use high-quality ceramic capacitors, and select a crystal or resonator that meets the requirements. Usually C_{L1} and C_{L2} have the same parameters. When selecting C_{Lx} , one should take into account parameters such as the crystal oscillator's frequency and ESR, as well as the total parasitic capacitance to ground (C_p) from the PCB and MCU pins.

The C_{Lx} is recommended to be configured in accordance with the requirements of the crystal manufacturer's technical manual.

- If the crystal manufacturer gives *the value of the load capacitance* (C_L), the matching capacitance $C_{Lx} = 2 * C_L - C_p$.
- If the crystal manufacturer gives *the value of the matching capacitance*, the matching capacitance $C_{Lx} = \text{matching capacitance value} - C_p$.

In practical applications, if a larger C_{Lx} is selected, it is recommended to choose an appropriate current level setting.

3. Choose a high-quality oscillator with a small ESR value, and you can optimize the current consumption by adjusting $XTL_CR[3:0]$ setting value. Current consumption is proportional to the transconductance (g_m) provided by the circuit.
4. T_{start} is the start-up time, which is the time from the software enabling XTL to start measuring until a stable 32768Hz oscillation is obtained. This value is measured using a standard crystal resonator with the settings $XTL_CR[3:0]=0b1010$ and $XTL_CR[5:4]=0b11$. It may vary greatly depending on the crystal manufacturer and model.

**Note**

- The feedback resistance $R0$ has been integrated in the chip.

5.3.9 Internal Clock Source Characteristics

5.3.9.1 RC48M

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Dev ₄₈	RC48M oscillator accuracy	User trimming step for given VCC and T _A conditions	-	0.2	-	%
		V _{CC} = 1.8-5.5V T _A = -40-85°C F _{CLK48} = 4/6MHz	-2.0 ⁽¹⁾	-	+2.0 ⁽¹⁾	
		V _{CC} = 1.8-5.5V T _A = -20-75°C F _{CLK48} = 4/6MHz	-1.5 ⁽¹⁾	-	+1.5 ⁽¹⁾	
		V _{CC} = 1.8-5.5V T _A = -40-85°C F _{CLK48} = 32/48MHz	-1.5 ⁽¹⁾	-	+1.5 ⁽¹⁾	
		V _{CC} = 1.8-5.5V T _A = -20-75°C F _{CLK48} = 32/48MHz	-1.0 ⁽¹⁾	-	+1.0 ⁽¹⁾	
F _{CLK48}	Oscillator frequency	-	4.0	4.0 6.0 32.0 48.0	48.0	MHz
I _{CLK48}	Power consumption	F _{CLK48} = 4MHz	-	54	-	μA
		F _{CLK48} = 6MHz	-	60	-	
		F _{CLK48} = 32MHz	-	181	-	
		F _{CLK48} = 48MHz	-	235	-	
DC _{CLK48} ⁽²⁾	Duty cycle	-	45	50	55	%
t _{su48}	Startup time (from enable to clock output initiation)	F _{CLK48} = 4MHz	-	18.2	-	μs
		F _{CLK48} = 6MHz	-	16.6	-	
		F _{CLK48} = 32MHz	-	10.9	-	
		F _{CLK48} = 48MHz	-	10.4	-	



Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.

5.3.9.2 RCH

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Dev	RCH oscillator accuracy	User trimming step for given VCC and T _A conditions	-	0.25	-	%
		V _{CC} =1.8-5.5V T _A =-40-85°C	-4.5 ⁽¹⁾	-	+3.0 ⁽¹⁾	%
F _{CLK}	Oscillator frequency	-	4.0	4.0 8.0 16.0 22.12 24.0	24.0	MHz
I _{CLK}	Power consumption	F _{MCLK} =4MHz	-	80	-	μA
		F _{MCLK} =8MHz	-	100	-	μA
		F _{MCLK} =16MHz	-	120	-	μA
		F _{MCLK} =24MHz	-	140	-	μA
DC _{CLK} ⁽¹⁾	Duty cycle	-	45	50	55	%



Note

1. Resulted from comprehensive evaluation, not tested in production.

5.3.9.3 RCL

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Dev	RCL oscillator accuracy	User trimming step for given VCC and T _A conditions	-	0.5	-	%
		V _{CC} =1.8-5.5V T _A =-40-85°C	-5.0 ⁽¹⁾	-	+3.0 ⁽¹⁾	%
F _{CLK}	Oscillator frequency	V _{CC} =3.3V T _A =25°C	38.2 32.5	38.4 32.768	38.6 33	kHz
T _{CLK}	Start time	-	-	150	-	μs
DC _{CLK} ⁽¹⁾	Duty cycle	-	25	50	75	%



Note

1. Resulted from comprehensive evaluation, not tested in production.

5.3.9.4 RC10K

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V	Operation voltage	-	1.8	-	5.5	V
Dev ⁽¹⁾	Oscillator accuracy	V _{CC} =1.8-5.5V T _A =-20-50°C	-50	-	50	%

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
F_{CLK}	Oscillator frequency	$V_{CC}=3.3V$ $T_A=25^{\circ}C$	-	10	-	kHz

**Note**

1. Resulted from comprehensive evaluation, not tested in production.

5.3.10 PLL Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$F_{in}^{(1)}$	Input clock	-	4	4	24	MHz
Duty_in ⁽¹⁾	Input clock duty cycle	-	40	-	60	%
F_{out}	Output frequency	-	8	-	48	MHz
Duty_out ⁽¹⁾	Output Duty Cycle	-	48%	-	52%	-
Tlock ⁽¹⁾	Lock Time	Input frequency 4MHz	-	100	200	μs
Iconsum	Power consumption	Output frequency 48MHz	-	450	-	μA

**Note**

1. Resulted from comprehensive evaluation, not tested in production.

5.3.11 Memory Characteristics

Symbol	Parameters	Conditions		Min	Typ	Max	Unit
EC _{FLASH}	Program, Sector Erase times	T _A =-40°C -105°C	Data Storage Period (RET _{FLASH}): 10 years, T _A =85°C	-	100000	-	time s
			Data Storage Period (RET _{FLASH}): 20 years, T _A =85°C	20000	-	-	time s
T _{b_prog}	Programming time (bytes)	-		22	-	30	μs
T _{w_prog}	Programming time (words)	-		40	-	52	μs
T _{p_erase}	Page Erase time	-		2	-	3	ms
T _{m_erase}	Full chip erase time	-		30	-	40	ms

5.3.12 I/O Port Characteristics

5.3.12.1 Output Characteristics-Port

Table 5-21 Port Output Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Max	Unit
V_{OH}	IO pin outputs high level (weak driver)	$I_{IO}=3mA$, $VCC=3.3V$	$VCC-0.3$	-	V
		$I_{IO}=6mA$, $VCC=3.3V$	$VCC-0.7$	-	V
V_{OL}	IO pin outputs low level (weak driver)	$I_{IO}=4mA$, $VCC=3.3V$	-	$VSS+0.3$	V
		$I_{IO}=8mA$, $VCC=3.3V$	-	$VSS+0.7$	V
V_{OHD}	IO pin outputs high level (strong driver)	$I_{IO}=6mA$, $VCC=3.3V$	$VCC-0.3$	-	V
		$I_{IO}=12mA$, $VCC=3.3V$	$VCC-0.7$	-	V
V_{OLD}	IO pin outputs low level (strong driver)	$I_{IO}=8mA$, $VCC=3.3V$	-	$VSS+0.3$	V
		$I_{IO}=16mA$, $VCC=3.3V$	-	$VSS+0.7$	V



Note

1. Resulted from comprehensive evaluation, not tested in production.
2. The device's I_{IO} current must always comply with the absolute maximum ratings specified in [Table 5-1 : Voltage and Current Characteristics](#), and the sum of I_{IO} (I_{OH} and I_{OL} of I/O ports) must not exceed I_{VCC} .

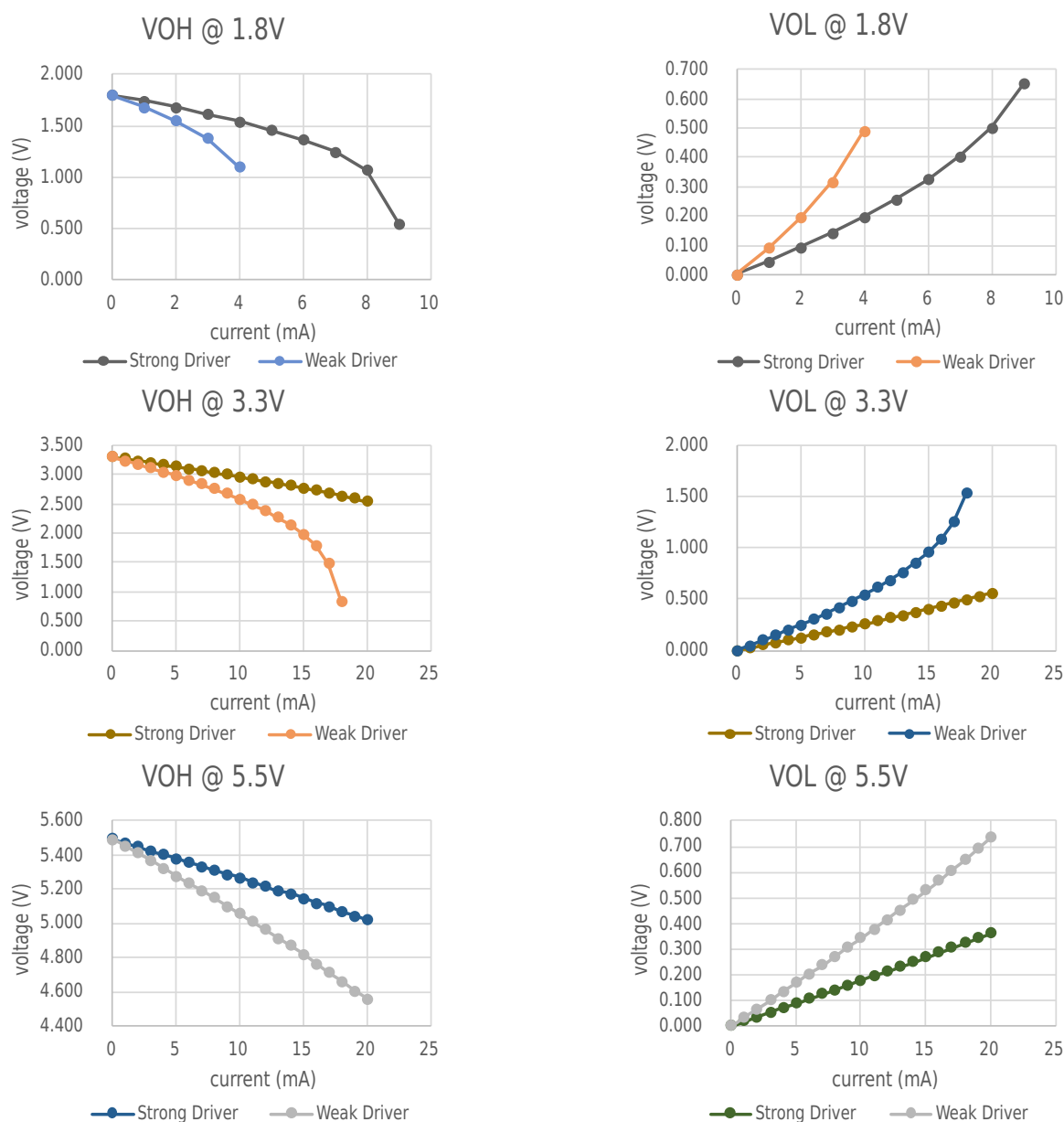


Figure 5-5 Output port VOH/VOL measured curve (typical value)

5.3.12.2 Input Characteristics-PA/PB/PC/PD/PE/PF Port

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{IH}^{(1)}$	Positive-going input threshold voltage	VCC=1.8V	0.7VCC	-	-	V
		VCC=3.3V	0.7VCC	-	-	V
		VCC=5.5V	0.7VCC	-	-	V
$V_{IL}^{(1)}$	Negative-going input threshold voltage	VCC=1.8V	-	-	0.3VCC	V
		VCC=3.3V	-	-	0.3VCC	V
		VCC=5.5V	-	-	0.3VCC	V
V_{hys}	Input voltage hysteresis ($V_{IH}-V_{IL}$)	VCC=1.8V	-	0.3	-	V
		VCC=3.3V	-	0.4	-	V
		VCC=5.5V	-	0.6	-	V

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$R_{pullhigh}$	Pullup resistor	Pullup enabled VCC=3.3V	-	80	-	k Ω
$R_{pulllow}$	Pulldown resistor	Pulldown enabled VCC=3.3V	-	40	-	k Ω
C_{input}	Input capacitance	-	-	5	-	pF

**Note**

1. Resulted from comprehensive evaluation, not tested in production.

5.3.12.3 Port External Input Sampling Requirements-Timer Gate/Timer Clock

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$t_{(cap)}$	Timer capture timing	Timer capture pulse width	-	0.5	-	μ s
$t_{(clk)}^{(1)}$	Timer clock frequency applied to pin	Timer external clock input $f_{HCLK}=4\text{MHz}$	-	-	PCLK/2	MHz
$t_{(pca)}^{(1)}$	PCA clock frequency applied to pin	PCA external clock input $f_{HCLK}=4\text{MHz}$	-	-	PCLK/8	MHz

**Note**

1. Resulted from comprehensive evaluation, not tested in production.

5.3.12.4 Port Leakage Characteristics- PA/PB/PC/PD/PE/PF Port

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$I_{lkg(Px.y)}$	Leakage current	$V_{(Px.y)}^{(1)(2)}$	-	± 50	-	nA

**Note**

1. The port leakage is based on the corresponding port being connected to VSS or VCC.
2. The port must be configured as an input port.

5.3.13 RESETB Pin Characteristics

The RESETB pin input driver uses CMOS technology, which is connected with a pull-up resistor that cannot be disconnected.

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{IL(RESETB)}^{(1)}$	Input Low-level voltage	-	-0.3	-	0.3VCC	V
$V_{IH(RESETB)}^{(1)}$	Input high-level voltage	-	0.7VCC	-	VCC+0.3	V
$V_{hys(RESETB)}$	Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistance	$V_{IN}=V_{SS}$	-	80	-	k Ω

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$T_{F(RESETB)}^{(1)}$	Filtered input pulse	-	-	-	2	μs
$T_{NF(RESETB)}^{(1)}$	Non-filtered input pulse	-	10	-	-	μs

**Note**

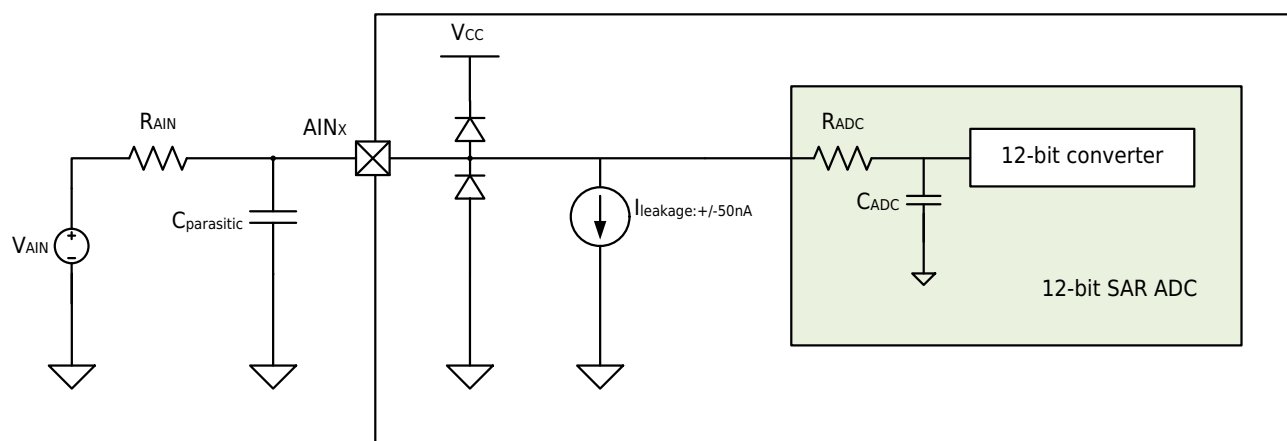
1. Guaranteed by design, not tested in production.

5.3.14 ADC Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{ADCIN}	Input voltage range	Single ended	0	-	V_{REF+}	V
$V_{REF+}^{(1)}$	Positive reference voltage	-	1.5	-	AVCC	V
V_{REF-}	Negative reference voltage	-	-	AVSS	-	V
$DEV_{AVCC/3}$	AVCC/3 accuracy	-	-	± 3	-	%
$V_{INBUF}^{(1)}$	Input voltage range of the input buffer within which the accuracy is guaranteed	$(AVCC-0.1V) < V_{REF+}$	0.1	-	AVCC-0.1	V
		$(AVCC-0.1V) \geq V_{REF+}$	0.1	-	V_{REF+}	
$I_{ADC}^{(1)}$	Active current	reference generator on, input buffer on, $f_s=200ksps$	-	1.77	-	mA
		reference generator on, input buffer on, $f_s=1Msps$	-	2.10	-	
		reference generator off, input buffer off, $f_s=1Msps$	-	0.71	-	
$C_{ADCIN}^{(1)}$	ADC input capacitance	-	-	16	-	pF
$R_{ADC}^{(1)}$	ADC sampling switch impedance	-	-	1.5	-	k Ω
$R_{AIN}^{(1)(3)}$	ADC external input resistor	-	-	-	100	k Ω
$f_{ADCCLK}^{(1)}$	ADC clock frequency	Range 1: $1.8V \leq AVCC \leq 2.4V$	0.2	-	4.8	MHz
		Range 2: $2.4V \leq AVCC \leq 2.7V$	0.2	-	12	
		Range 3: $AVCC \geq 2.7V$	0.2	-	24 ⁽⁴⁾	

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$f_s^{(1)}$	Sampling rate	Range 3, $V_{REF+}=AVCC$	-	-	1	Msps
		Range 3, $V_{REF+}=EX-VREF$ (PB01)	-	-	0.9	
		Range 2, $V_{REF+}=AVCC/EXVREF$ (PB01)	-	-	0.5	
		Range 1, $V_{REF+}=AVCC/EXVREF$ (PB01)/internal 1.5V/internal 2.5V	-	-	0.2 ⁽⁵⁾	
$T_{ADCSTART}$	Startup time of reference generator and ADC core	-	-	20	-	μs
T_s	Sampling time	-	4	-	12	1/ f_{ADCCLK}
$T_{ADCCONV}$	Conversion time	-	-	T_s+16	-	
$ENOB^{(1)}$	Effective bits	$V_{REF+}=AVCC=3.3V$, $T_A=25^\circ C$, $f_s=1Msps$	9.9	10.7	-	bits
		$V_{REF+}=internal\ 1.5V$, $AVCC=3.3V$, $T_A=25^\circ C$, $f_s=200ksps$	9.1	9.8	-	
$SNR^{(1)}$	Signal to noise ratio	$V_{REF+}=AVCC=3.3V$, $T_A=25^\circ C$, $f_s=1Msps$	63.1	67.3	-	dB
		$V_{REF+}=internal\ 1.5V$, $AVCC=3.3V$, $T_A=25^\circ C$, $f_s=200ksps$	56.9	60.6	-	
$DNL^{(2)}$	Differential non-linearity	$V_{REF+}=AVCC=3.3V$, $T_A=25^\circ C$, $f_s=500ksps$	-1	-0.9/+1.3	+1.8	LSB
$INL^{(2)}$	Integral non-linearity		-3.3	-2.2/+2.2	+3.3	
$E_o^{(1)}$	Offset error		-	-1.2/+3.5	-	
$E_g^{(1)}$	Gain error		-	-2.0/+3.4	-	
$E_T^{(1)}$	Total unadjusted error		-	± 5.4	-	

1. Guaranteed by design, not tested in production.
2. Resulted from comprehensive evaluation, not tested in production.
3. The typical application of ADC is shown in the figure below:



Under the condition of 0.5LSB sampling error accuracy requirement, the calculation formula of external input impedance is as follows:

$$R_{AIN} \leq \frac{T_s}{C_{ADC} * (N+1) * \ln(2)} - R_{ADC} = \frac{M}{f_{ADCCLK} * C_{ADC} * (N+1) * \ln(2)} - R_{ADC}$$

where T_s is the sampling time, N is the ADC bit number 12, f_{ADCCLK} is the ADC clock frequency, and M is the number of sampling cycles (the sampling time occupies M ADC clock cycles).

Register ADC_CR0[3:2] can set the relationship between f_{ADCCLK} and PCLK frequency, as shown in the following table:

Table 5-27 ADC Clock Frequency f_{ADCCLK} and PCLK Division Ratio Relationship

ADC_CR0[3:2]	f_{PCLK}/f_{ADCCLK}
0b00	1
0b01	2
0b10	4
0b11	8

Register ADC_CR0[13:12] can set the number of sampling periods M , as shown in the following table:

Table 5-28 ADC Sampling Period Number M

ADC_CR0[13:12]	M
0b00	4
0b01	6
0b10	8
0b11	12

The table below shows the relationship between ADC minimum sampling time T_s and external resistor R_{AIN} under typical operating conditions ($M=12$, with 0.5LSB sampling error). For other special external input impedance values, the corresponding minimum sampling time requirements can also be calculated through the external input impedance calculation formula given above.

Table 5-29 Relationship Between ADC Minimum Sampling Time T_s and External Resistance R_{AIN}

$R_{AIN} (\Omega)$	Minimum Sampling Time T_s (ns)
10	218
47	223

$R_{AIN} (\Omega)$	Minimum Sampling Time T_s (ns)
68	226
100	231
150	238
220	248
330	264
470	284
680	314
1000	360
1500	433
2200	533
3300	692
4700	894
6800	1197
10000	1658
15000	2379

For the above typical applications, you should pay attention to:

- Minimize parasitic capacitance $C_{parasitic}$ at the ADC input pin AIN_x .
 - In addition to consider R_{AIN} value, if the internal resistance of signal source V_{AIN} is large, it also needs to be considered.
4. For voltage range 3, if $V_{REF+} = EXVREF$ (PB01), the ADC's maximum clock frequency must be reduced to 20MHz to ensure performance.
 5. For voltage range 1, if $V_{REF+} =$ internal 2.5V, the minimum allowed AVCC voltage is 2.8V instead of 1.8V.

5.3.15 Temperature Sensor Characteristics

When the measurement channel of the ADC selects the output voltage of the temperature sensor, the current chip temperature can be calculated through the output result of the ADC and the calibration value stored in the Flash memory.

Table 5-30 Temperature Sensor Parameters

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Temp Range	Operating junction temperature range for the temperature sensor	-	-40	-	105	°C
Δ Terror	Temperature Error	-	-	± 5	-	°C

5.3.16 VC Characteristics

Symbol	Parameters	Conditions		Min	Typ	Max	Unit
V _{in}	Input voltage range	-		0	-	5.5	V
V _{com}	Input common mode range	-		0.2	-	VCC-0.2	V
V _{offset}	Input offset	0.8V≤V _{com} ≤ (AVCC-0.8V)	VCx_BIAS_SEL=0b00	-	±20	-	mV
			VCx_BIAS_SEL=0b01	-	±20	-	
			VCx_BIAS_SEL=0b10	-	±10	-	
			VCx_BIAS_SEL=0b11	-	±10	-	
		0.2V≤V _{com} ≤0.8V or (AVCC-0.8V)≤V _{com} ≤ (AVCC-0.2V)	VCx_BIAS_SEL=0b00	-	±33	-	
			VCx_BIAS_SEL=0b01	-	±32	-	
			VCx_BIAS_SEL=0b10	-	±26	-	
			VCx_BIAS_SEL=0b11	-	±25	-	
I _{comp}	Comparator's current	VCx_BIAS_SEL=0b00 VCx_BIAS_SEL=0b01 VCx_BIAS_SEL=0b10 VCx_BIAS_SEL=0b11	-	0.23 0.46 9.1 18.2	-	μA	
T _{response}	Comparator's response time when one input cross another	VCx_BIAS_SEL=0b00 VCx_BIAS_SEL=0b01 VCx_BIAS_SEL=0b10 VCx_BIAS_SEL=0b11	-	2500 1400 120 80	-	ns	
T _{setup}	Comparator's setup time when ENABLE. Input signals un- changed.	-	-	360	-	ns	
V _{hysteresis}	Comparator's hystere- sis voltage	VCx_HYS_SEL=0b00 VCx_HYS_SEL=0b01 VCx_HYS_SEL=0b10 VCx_HYS_SEL=0b11	-	0 10 20 30	-	mV	
R _{in} ⁽¹⁾	Allowable source resist- ance of the input signal	VCx_HYS_SEL=0b00 VCx_HYS_SEL=0b01/0b 10/0b11	-	-	100k 400	Ω	
V _{off_DAC}	Comparator's inner DAC's offset	-	-	±40	-	mV	

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
T_{warmup}	The waiting time after enabling the BGR	internal 1.5V/2.5V reference voltage	-	40	-	μs
		the temperature sensor is needed or $\text{VCx_BIAS_SEL}=0\text{b}10/0\text{b}11$	-	20	-	
T_{filter}	Digital filter time	$\text{VCx_CR}[11:9]=0\text{b}000$ $\text{VCx_CR}[11:9]=0\text{b}001$ $\text{VCx_CR}[11:9]=0\text{b}010$ $\text{VCx_CR}[11:9]=0\text{b}011$ $\text{VCx_CR}[11:9]=0\text{b}100$ $\text{VCx_CR}[11:9]=0\text{b}101$ $\text{VCx_CR}[11:9]=0\text{b}110$ $\text{VCx_CR}[11:9]=0\text{b}111$	-	7 14 28 112 450 1800 7200 28800	-	μs

**Note**

1. Guaranteed by design, not tested in production.

5.3.17 OPA Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{in}	Input voltage	-	0.2	-	$\text{AVCC}-0.2$	V
$V_{\text{o}}^{(1)}$	Output voltage	-	0.2	-	$\text{AVCC}-0.2$	V
$I_{\text{o}}^{(1)}$	Output current	-	-	-	0.3	mA
$R_{\text{L}}^{(1)}$	Load resistance	-	5	-	-	k Ω
$T_{\text{start}}^{(2)}$	Initialization time	$V_{\text{ip}}=\text{AVCC}/2+50\text{mV}$, $V_{\text{in}}=\text{AVCC}/2-50\text{mV}$ $I_{\text{load}}=300\mu\text{A}$, $\text{CL}=50\text{pF}$	-	1	-	μs
V_{os}	Input offset voltage	$V_{\text{in}}=\text{AVCC}/2$, $V_{\text{o}}=\text{AVCC}/2$ $I_{\text{load}}=300\mu\text{A}$, $R_{\text{s}}=50\Omega$	-	± 6	-	mV
GBW	Unity gain bandwidth	$V_{\text{in}}=\text{AVCC}/2$, $V_{\text{o}}=\text{AVCC}/2$ $I_{\text{load}}=300\mu\text{A}$, $\text{CL}=50\text{pF}$	-	6.5	-	MHz
SR	Slew rate	$I_{\text{load}}=300\mu\text{A}$, $\text{CL}=50\text{pF}$	-	6	-	V/ μs

**Note**

1. Guaranteed by design, not tested in production.
2. Need to set $\text{BGR_CR}[0]=0\text{b}1$ at the same time.

5.3.18 LCD Controller

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$I_{LCD}^{(1)}$	Working current	VCC=3.3V, internal resistance mode (high-power consumption)	-	10	-	μA
		VCC=3.3V, internal resistance mode (medium-power consumption)	-	7	-	μA
		VCC=3.3V, internal resistance mode (low-power consumption)	-	3.5	-	μA
V_{LCDH}	LCD adjustable maximum voltage	-	-	-	VCC	V
V_{LCD3}	LCD maximum voltage	-	-	-	V_{LCDH}	V
V_{LCD2}	LCD 2/3 voltage	-	-	-	$2/3 V_{LCDH}$	V
V_{LCD1}	LCD 1/3 voltage	-	-	-	$1/3 V_{LCDH}$	V
V_{LCD0}	LCD minimum voltage	-	0	-	-	V
ΔV_{XX}	LCD voltage deviation	$T_A = -40-85^{\circ}C$	-	$\pm 5\%$	-	-



Note

1. The power consumption data was measured without an LCD screen attached, exclusively isolating the power draw of the LCD driver circuit itself and excluding contributions from GPIO or other system components.

5.3.19 DAC Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{REF+}^{(1)}$	Positive reference voltage	-	1.5	-	AVCC	V
V_{REF-}	Negative reference voltage	-	-	AVSS	-	V
$V_{DACOUT}^{(1)}$	Output voltage range	DAC buffer off (bypass buffer)	0	-	V_{REF+}	V
		DAC buffer on	0.2	-	$V_{REF+}-0.2$	
I_{DAC}	Active current	$V_{REF+} = AVCC/EXVREF$ (PB01)	-	9	-	μA
		$V_{REF+} = \text{internal } 1.5V/2.5V$	-	510	-	
R_O	Output resistance	DAC buffer off (bypass buffer)	-	100	-	k Ω
$SR_{DAC}^{(1)}$	Sample rate	-	-	-	500	ksps

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$t_{\text{DACCONV}}^{(1)}$	Conversion time, variation of the input code = 1 LSB	Settling error $\leq 0.5 \times \text{LSB}$, $CL \leq 10\text{pF}$, DAC buffer off (bypass buffer)	2	-	-	μs
		Settling error $\leq 0.5 \times \text{LSB}$, $CL \leq 50\text{pF}$, DAC buffer on	2	-	-	
$t_{\text{DACSETTLE}}$	Setting time, transition between the lowest and the highest input codes	Settling error $\leq 0.5 \times \text{LSB}$, $CL \leq 10\text{pF}$, DAC buffer off (bypass buffer)	-	9	-	μs
		Settling error $\leq 0.5 \times \text{LSB}$, $CL \leq 50\text{pF}$, DAC buffer on	-	3	-	
SNR_{DAC}	Signal to noise ratio	DAC buffer on, $R_L \geq 5\text{k}\Omega$	-	62	-	dB
SNDR_{DAC}	Signal to noise and distortion ratio		-	59	-	dB
SFDR_{DAC}	Spurious free dynamic range		-	67	-	dB
$E_o^{(2)}$	Offset error at code 0x000	DAC buffer off (bypass buffer), no R_L , $\text{AVCC} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$	-3.5	-2.5/+0.5	+1.4	LSB
$E_g^{(2)}$	Gain error at code 0xFFFF		-7.0	-3.5/+1.4	+3.1	LSB
$\text{DNL}_{\text{DAC}}^{(2)}$	Differential non-linearity		-1.5	-1.2/+0.7	+1.0	LSB
$\text{INL}_{\text{DAC}}^{(2)}$	Integral non-linearity		-2.3	-1.8/+8.4	+10.1	LSB

**Note**

1. Guaranteed by design, not tested in production.
2. Resulted from comprehensive evaluation, not tested in production.

5.3.20 TIM Timer Characteristics

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), see the table below.

Table 5-35 Advanced Timer (ADVTIM) Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	-	1	-	t_{TIMCLK}
		$f_{\text{TIMCLK}} = 48\text{MHz}$	20.8	-	ns
f_{ext}	External clock frequency	-	0	$f_{\text{TIMCLK}}/2$	MHz
		$f_{\text{TIMCLK}} = 48\text{MHz}$	0	24	MHz
Res_{Tim}	Timer resolution	-	-	16	Bit

Symbol	Parameters	Conditions	Min	Max	Unit
T_{counter}	When the internal clock is selected, the 16-bit counter clock cycle	-	1	65536	t_{TIMCLK}
		$f_{\text{TIMCLK}}=48\text{MHz}$	0.0208	1363	μs

**Note**

1. Guaranteed by design, not tested in production.

Table 5-36 General Timer Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	-	1	-	t_{TIMCLK}
		$f_{\text{TIMCLK}}=48\text{MHz}$	20.8	-	ns
f_{ext}	External clock frequency	-	0	$f_{\text{TIMCLK}}/2$	MHz
		$f_{\text{TIMCLK}}=48\text{MHz}$	0	24	MHz
Res_{Tim}	Timer resolution	-	-	16	Bit
		Mode 0 free counting	-	32	Bit
T_{counter}	When the internal clock is selected, the 16-bit counter clock cycle	-	1	65536	t_{TIMCLK}
		$f_{\text{TIMCLK}}=48\text{MHz}$	0.0208	-	μs

**Note**

1. Guaranteed by design, not tested in production.

Table 5-37 PCA Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	-	1	-	t_{TIMCLK}
		$f_{\text{TIMCLK}}=48\text{MHz}$	20.8	-	ns
f_{ext}	External clock frequency	-	0	$f_{\text{TIMCLK}}/8$	MHz
		$f_{\text{TIMCLK}}=48\text{MHz}$	0	6	MHz
Res_{Tim}	Timer resolution	-	-	16	Bit
T_{counter}	When the internal clock is selected, the 16-bit counter clock cycle	-	1	65536	t_{TIMCLK}
		$f_{\text{TIMCLK}}=48\text{MHz}$	0.0208	1363	μs

**Note**

1. Guaranteed by design, not tested in production.

Table 5-38 Low-Power Timer Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	-	1	-	t_{TIMCLK}
		$f_{\text{TIMCLK}}=48\text{MHz}$	20.8	-	ns

Symbol	Parameters	Conditions	Min	Max	Unit
f_{ext}	External clock frequency	-	0	$f_{\text{TIMCLK}/2}$	MHz
		$f_{\text{TIMCLK}}=48\text{MHz}$	0	24	MHz
Res_{Tim}	Timer resolution	-	-	16	Bit
T_{counter}	When the internal clock is selected, the 16-bit counter clock cycle	-	1	65536	t_{TIMCLK}
		$f_{\text{TIMCLK}}=48\text{MHz}$	0.0208	1363	μs

**Note**

1. Guaranteed by design, not tested in production.

Table 5-39 WDT Characteristics⁽¹⁾

Symbol	Parameters	Conditions	Min	Max	Unit
t_{res}	WDT overflow time	$f_{\text{WDTCLK}}=10\text{kHz}$	1.6	52400	ms

**Note**

1. Guaranteed by design, not tested in production.

5.3.21 Communication Interface

5.3.21.1 I2C Characteristics

I2C interface characteristics are as follows:

Table 5-40 I2C Interface Characteristics⁽¹⁾

Symbol	Parameters	Standard Mode (100k)		Fast Mode (400k)		Fast enhanced Mode (1M)		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCLL}	SCL clock low time	4.7	-	1.25	-	0.5	-	μs
t_{SCLH}	SCL clock high time	4.0	-	0.6	-	0.26	-	μs
$t_{\text{SU.SDA}}$	SDA establishment time	250	-	100	-	50	-	ns
$t_{\text{HD.SDA}}$	SDA hold time	0	-	0	-	0	-	μs
$t_{\text{HD.STA}}$	Start condition hold time	2.5	-	0.625	-	0.25	-	μs
$t_{\text{SU.STA}}$	Repeated start condition establishment time	2.5	-	0.6	-	0.25	-	μs
$t_{\text{SU.STO}}$	Stop condition setup time	0.25	-	0.25	-	0.25	-	μs
t_{BUF}	Bus idle (stop condition to start condition)	4.7	-	1.3	-	0.5	-	μs

**Note**

1. Guaranteed by design, not tested in production.

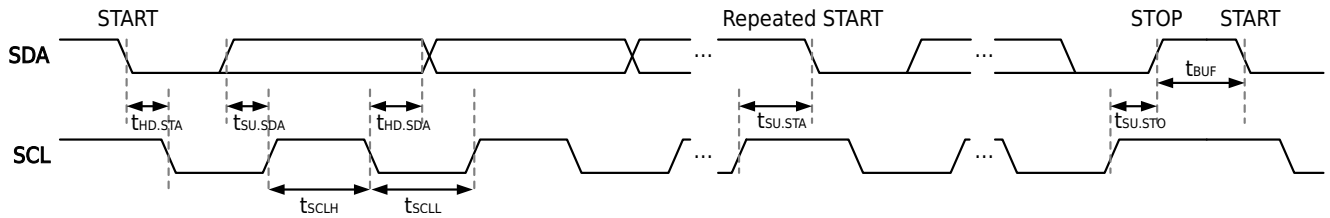


Figure 5-7 I2C Interface Timing

5.3.21.2 SPI Characteristics

Table 5-41 SPI Interface Characteristics⁽¹⁾⁽²⁾

Symbol	Parameters	Conditions	Min	Max	Unit
$t_{c(SCK)}$	Serial clock period ⁽³⁾	Master transmit mode $f_{PCLK}=32\text{MHz}$	62.5	-	ns
		Master receiving mode $f_{PCLK}=48\text{MHz}$	160	-	ns
		Slave transmit mode $f_{PCLK}=48\text{MHz}$	160	-	ns
		Slave receiving mode $f_{PCLK}=48\text{MHz}$	84	-	ns
$t_{w(SCKH)}$	High level time of serial clock	Master mode	$0.45 \times t_{c(SCK)}$	-	ns
		Slave mode	$0.45 \times t_{c(SCK)}$	-	ns
$t_{w(SCKL)}$	Low level time of serial clock	Master mode	$0.45 \times t_{c(SCK)}$	-	ns
		Slave mode	$0.45 \times t_{c(SCK)}$	-	ns
$t_{su(SSN)}$	Setup time selected by slave	Slave mode	$0.45 \times t_{c(SCK)}$	-	ns
$t_{h(SSN)}$	Hold time selected by slave	Slave mode	$0.45 \times t_{c(SCK)}$	-	ns
$t_{v(MO)}$	Effective time of Master data output	-	-	3	ns
$t_{h(MO)}$	Hold time of Master data output	-	2	-	ns
$t_{v(SO)}$	Effective time of slave data output	-	-	$20 + 1.5 \times T_{PCLK}$	ns
$t_{h(SO)}$	Hold time of slave data output	-	$10 + 0.5 \times T_{PCLK}$	-	ns
$t_{su(MI)}$	Setup time of Master data input	-	10	-	ns
$t_{h(MI)}$	Hold time of Master data input	-	2	-	ns
$t_{su(SI)}$	Setup time of slave data input	-	10	-	ns
$t_{h(SI)}$	Hold time of slave data input	-	2	-	ns

**Note**

1. Guaranteed by design, not tested in production.
2. The data is provided under the condition of $V_{CC}=3.0V$.
3. The maximum frequency division factor of the master mode is $PCLK/2$, and the The maximum frequency division factor of slave mode is $PCLK/4$.

The waveform and timing parameters of the SPI interface signal are as follows:

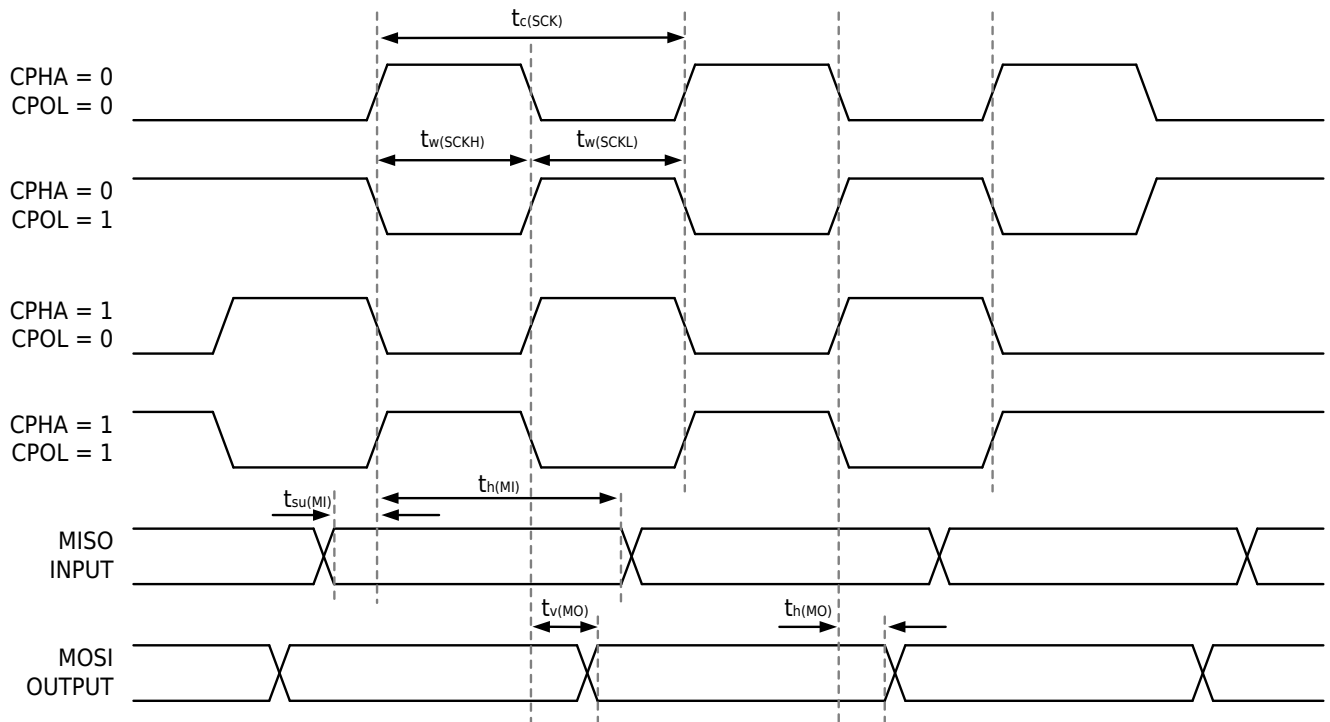


Figure 5-8 SPI Timing Diagram (Master Mode)

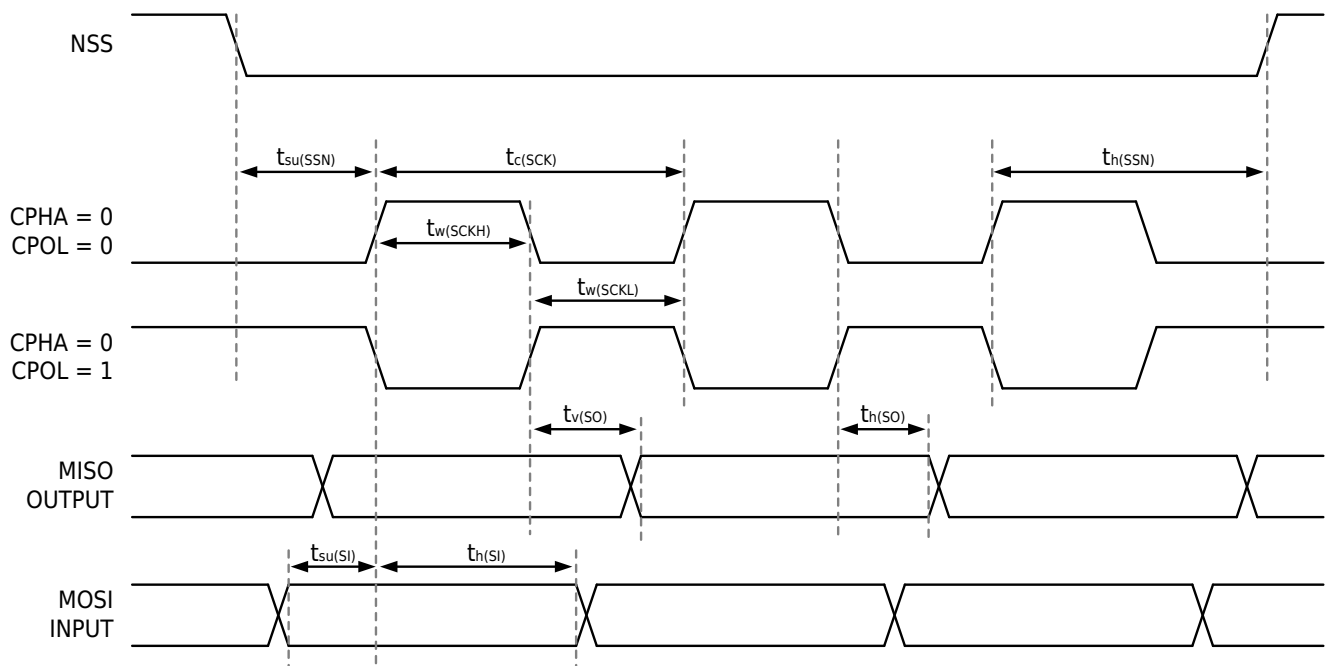


Figure 5-9 SPI Timing Diagram (Slave Mode CPHA=0)

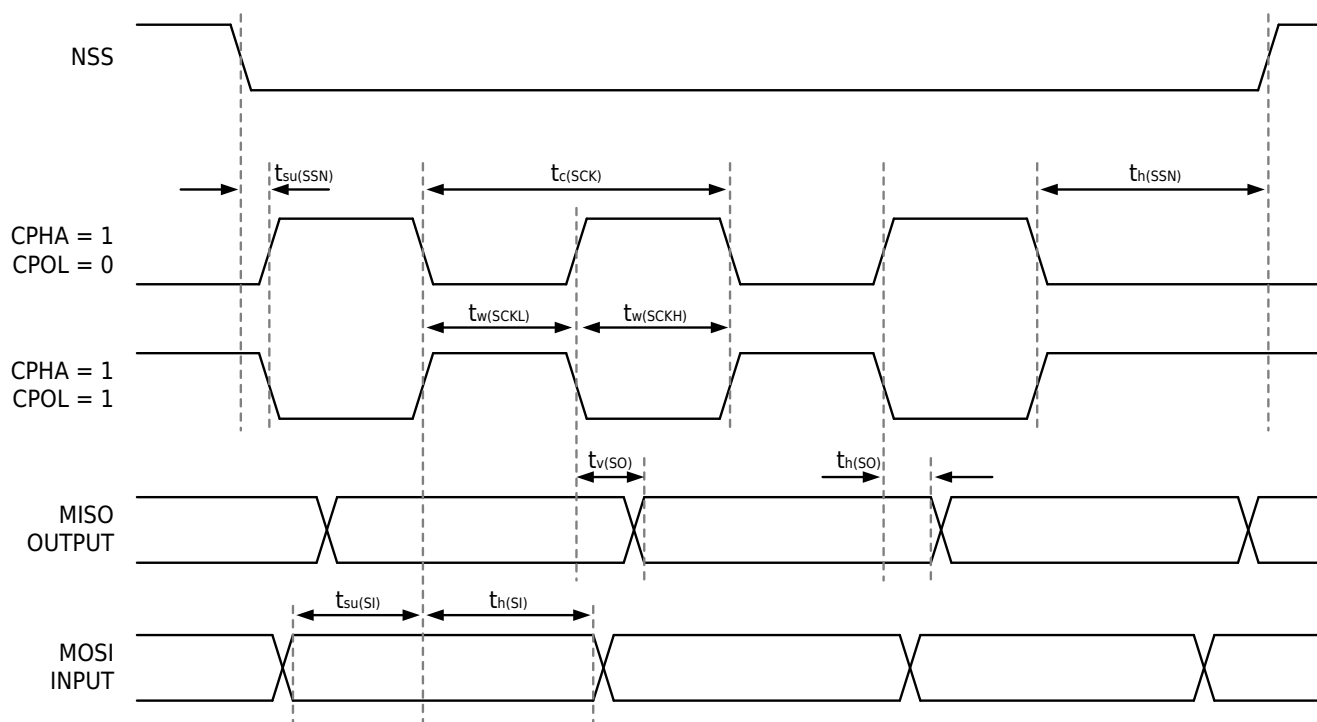
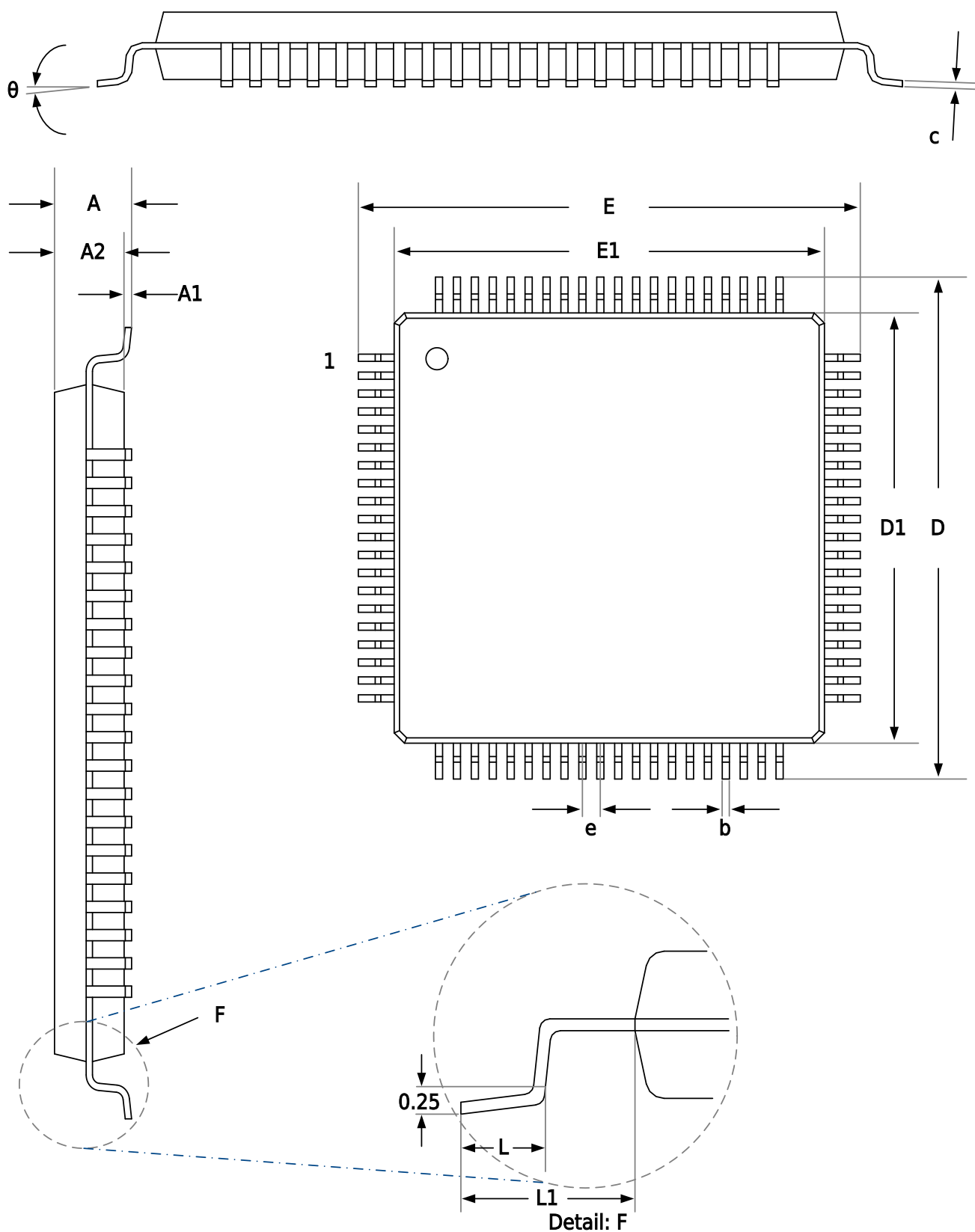


Figure 5-10 SPI Timing Diagram (Slave Mode CPHA=1)

6 Package Specifications

6.1 Package Dimensions

6.1.1 LQFP80 Package

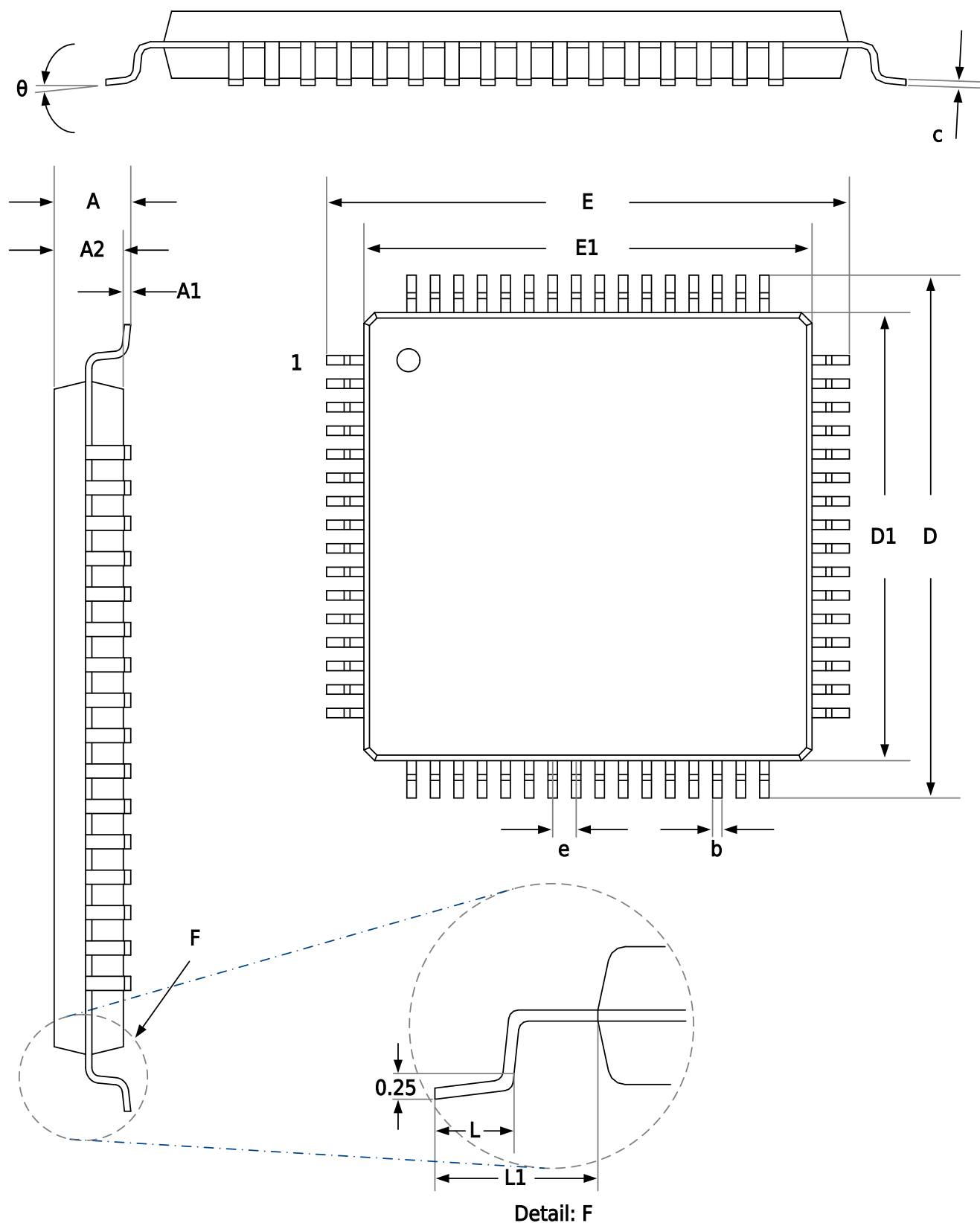


Symbol	12*12 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	--	7°

**Note**

Dimensions "D1" and "E1" do not include mold flash.

6.1.2 LQFP64 Package

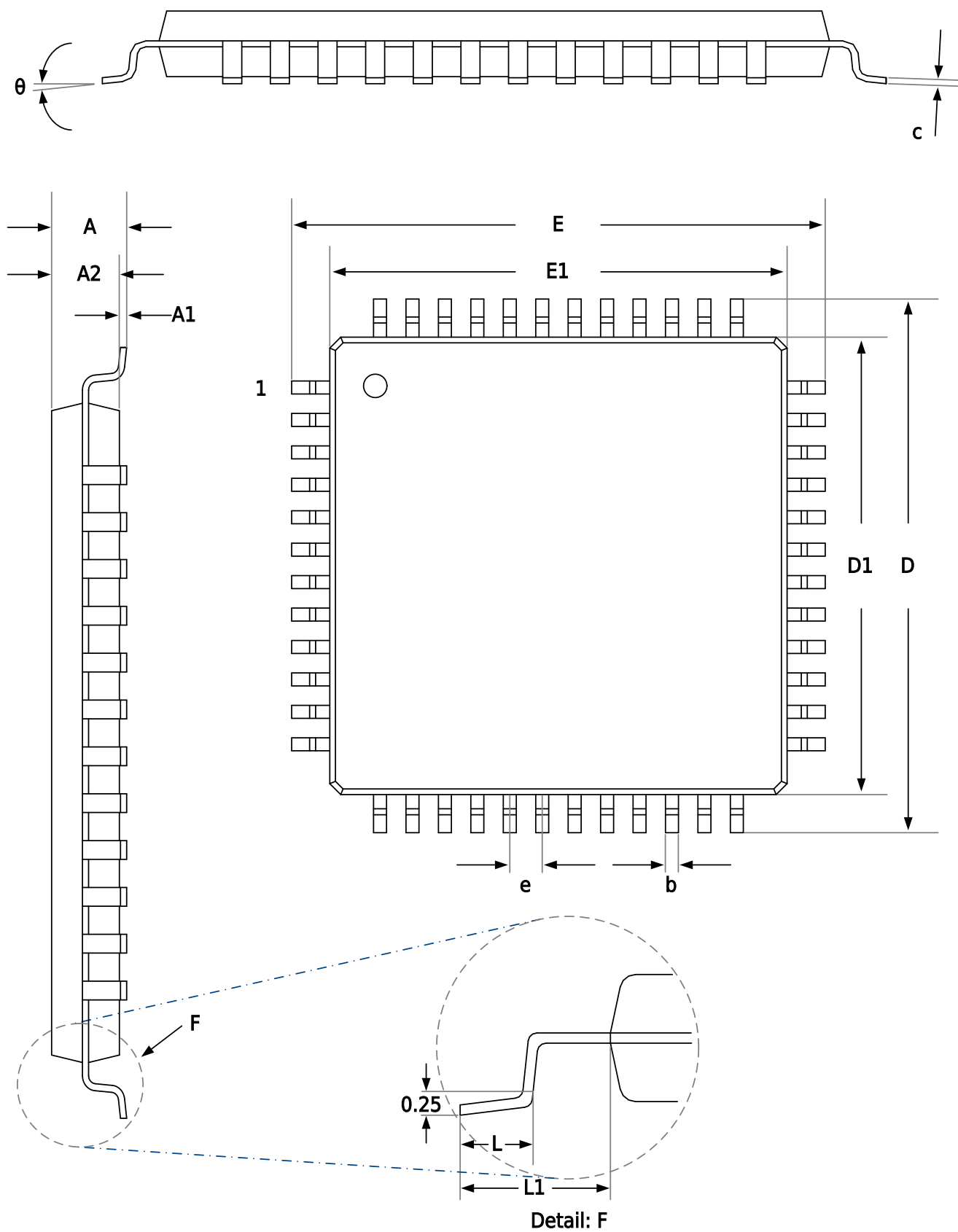


Symbol	10*10 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0°	--	7°

**Note**

Dimensions "D1" and "E1" do not include mold flash.

6.1.3 LQFP48 Package

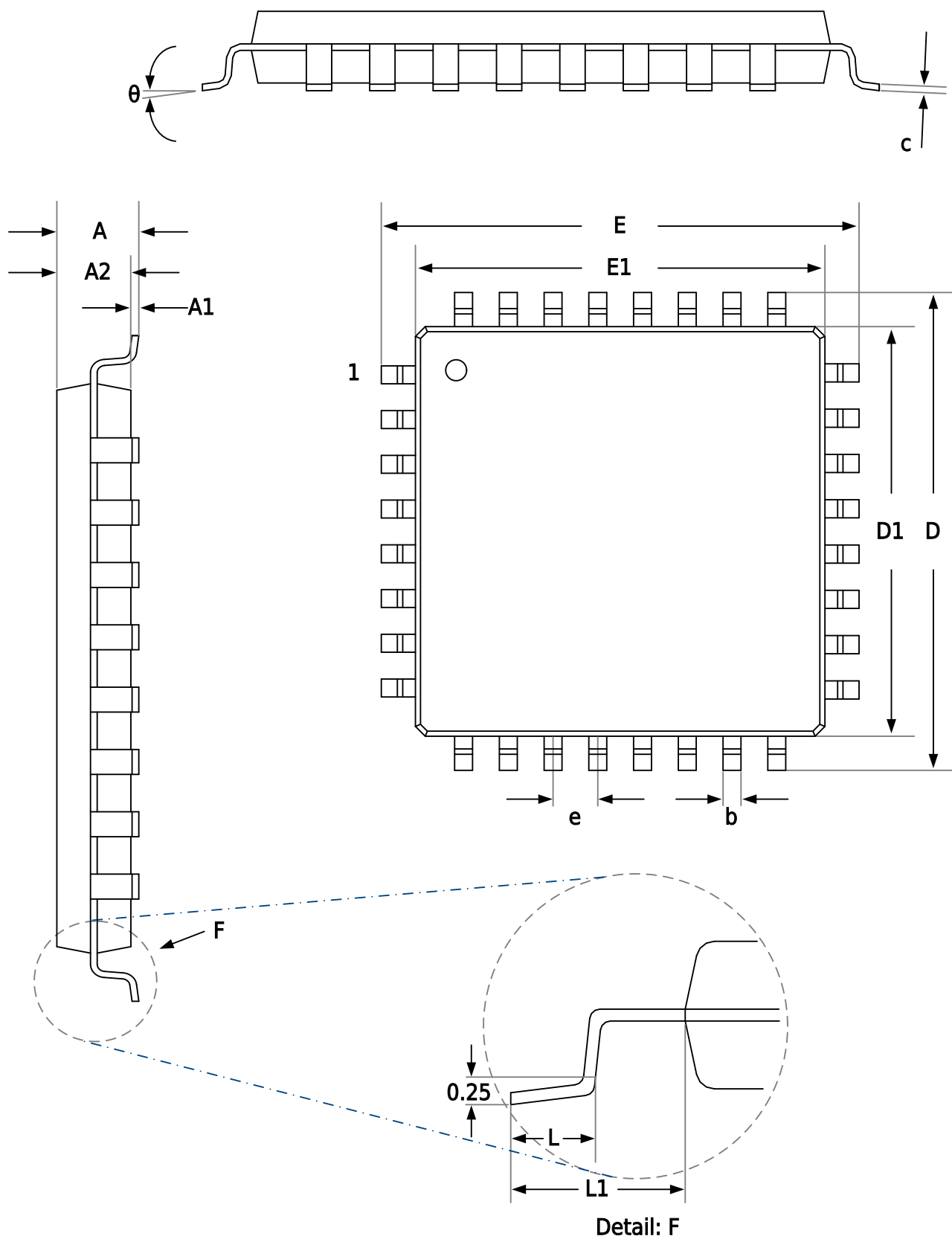


Symbol	7*7 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0	--	7°

**Note**

Dimensions "D1" and "E1" do not include mold flash.

6.1.4 LQFP32 Package



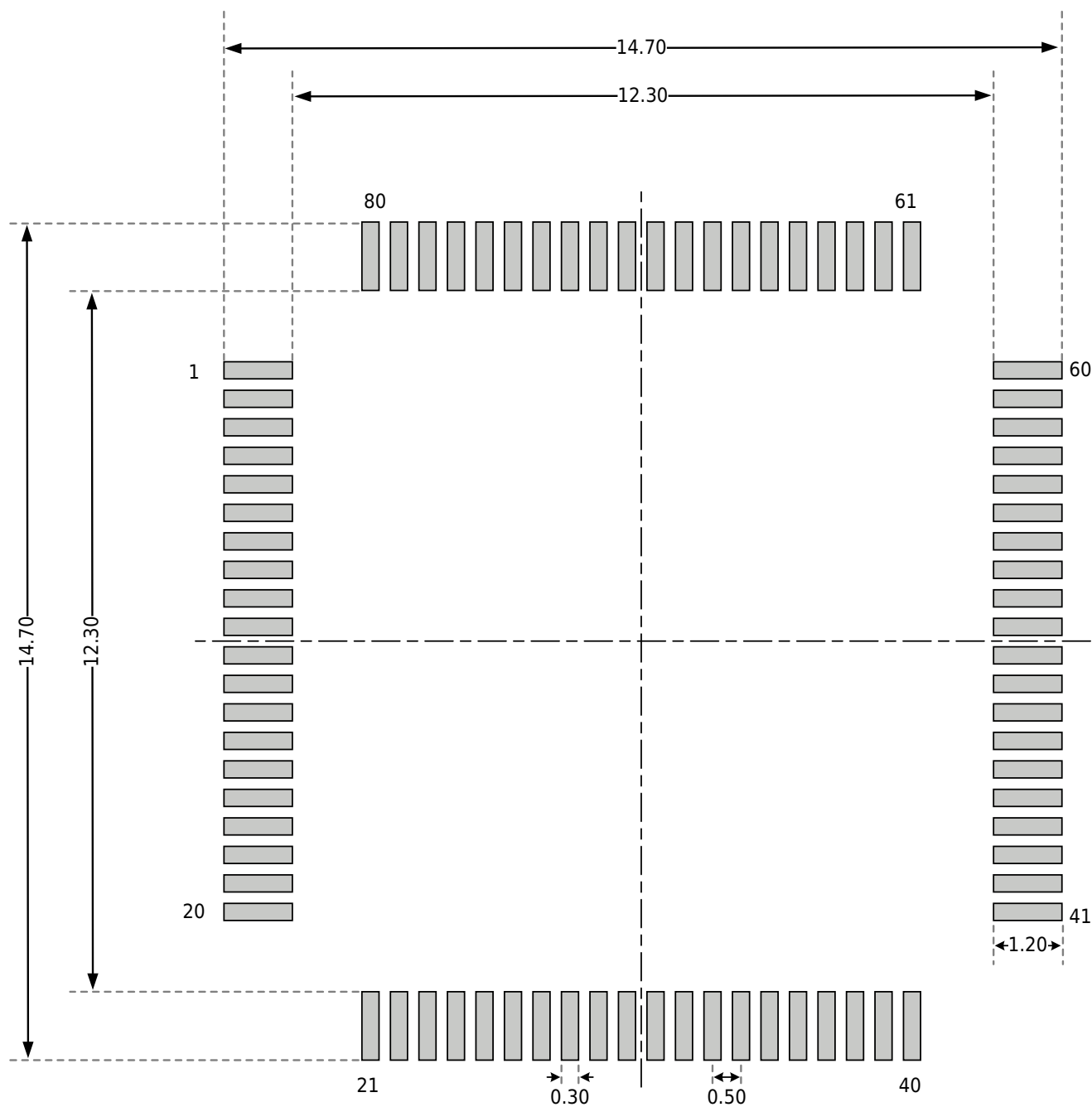
Symbol	7*7 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	--	0.45
c	0.09	--	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.80BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0	--	7°

**Note**

Dimensions "D1" and "E1" do not include mold flash.

6.2 PCB Land Pattern

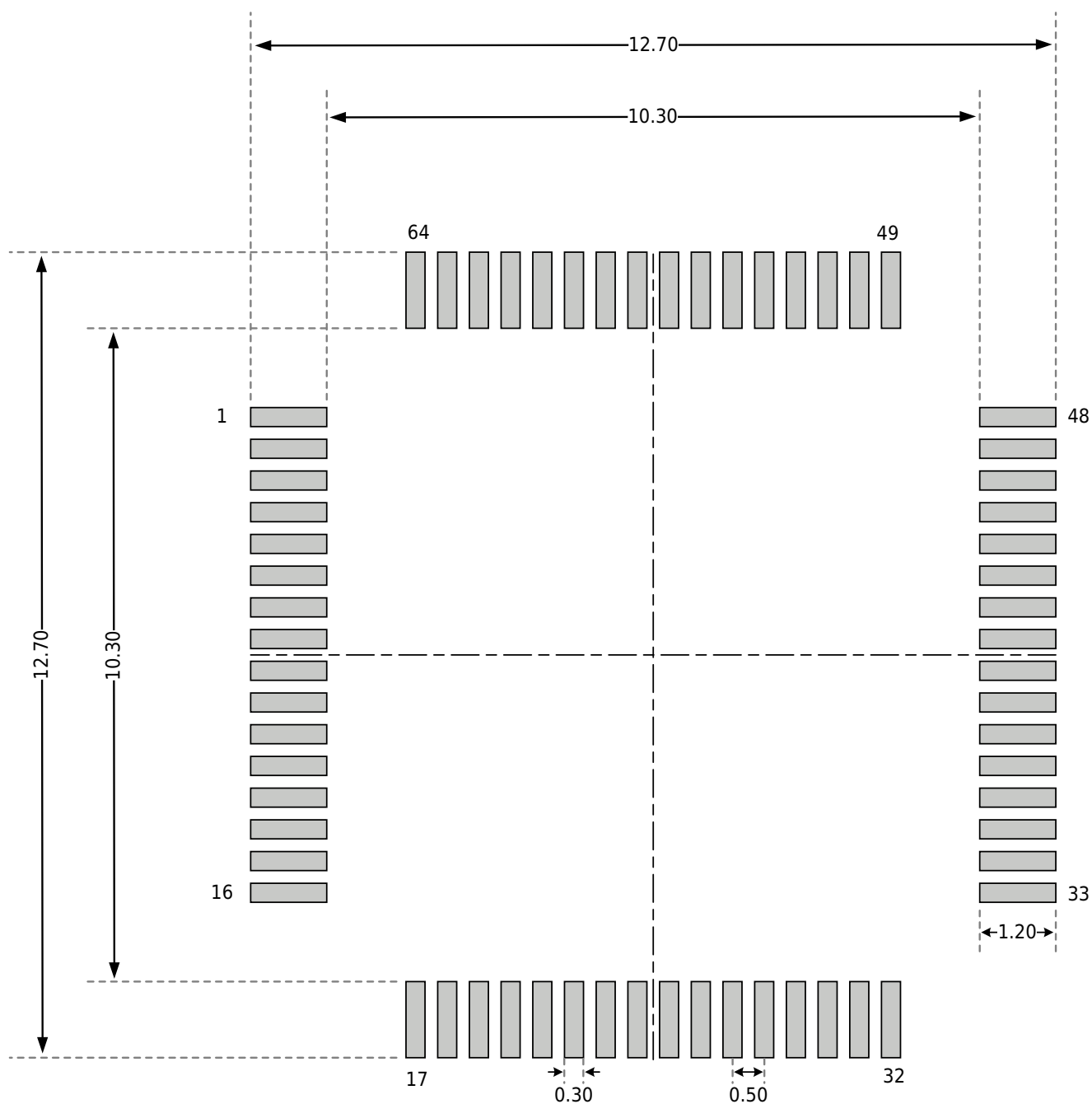
6.2.1 LQFP80 Package (12mm*12mm)



Note

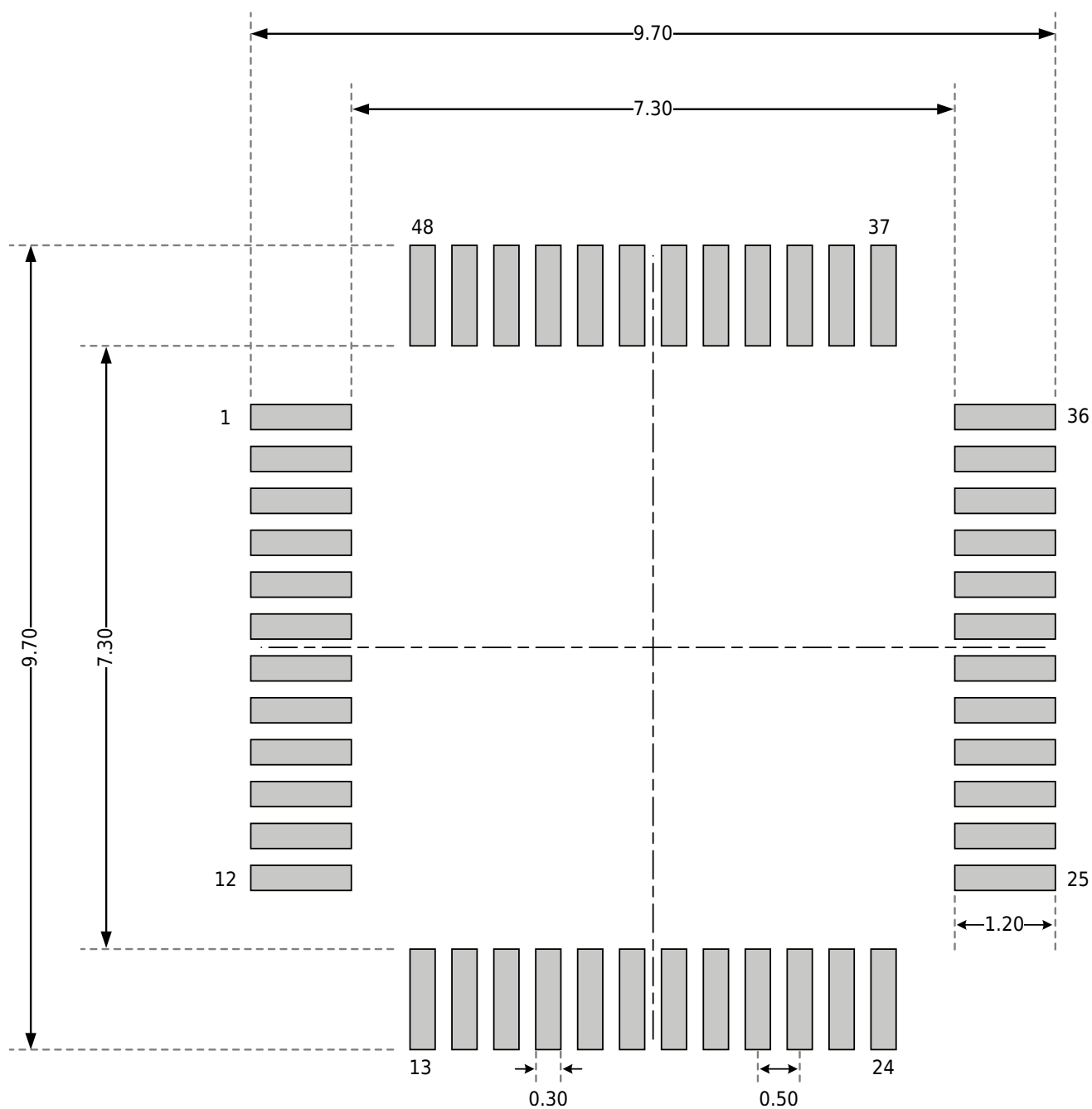
- Dimensions are in millimeters.
- Dimensions are for reference only.

6.2.2 LQFP64 Package (10mm*10mm)

**Note**

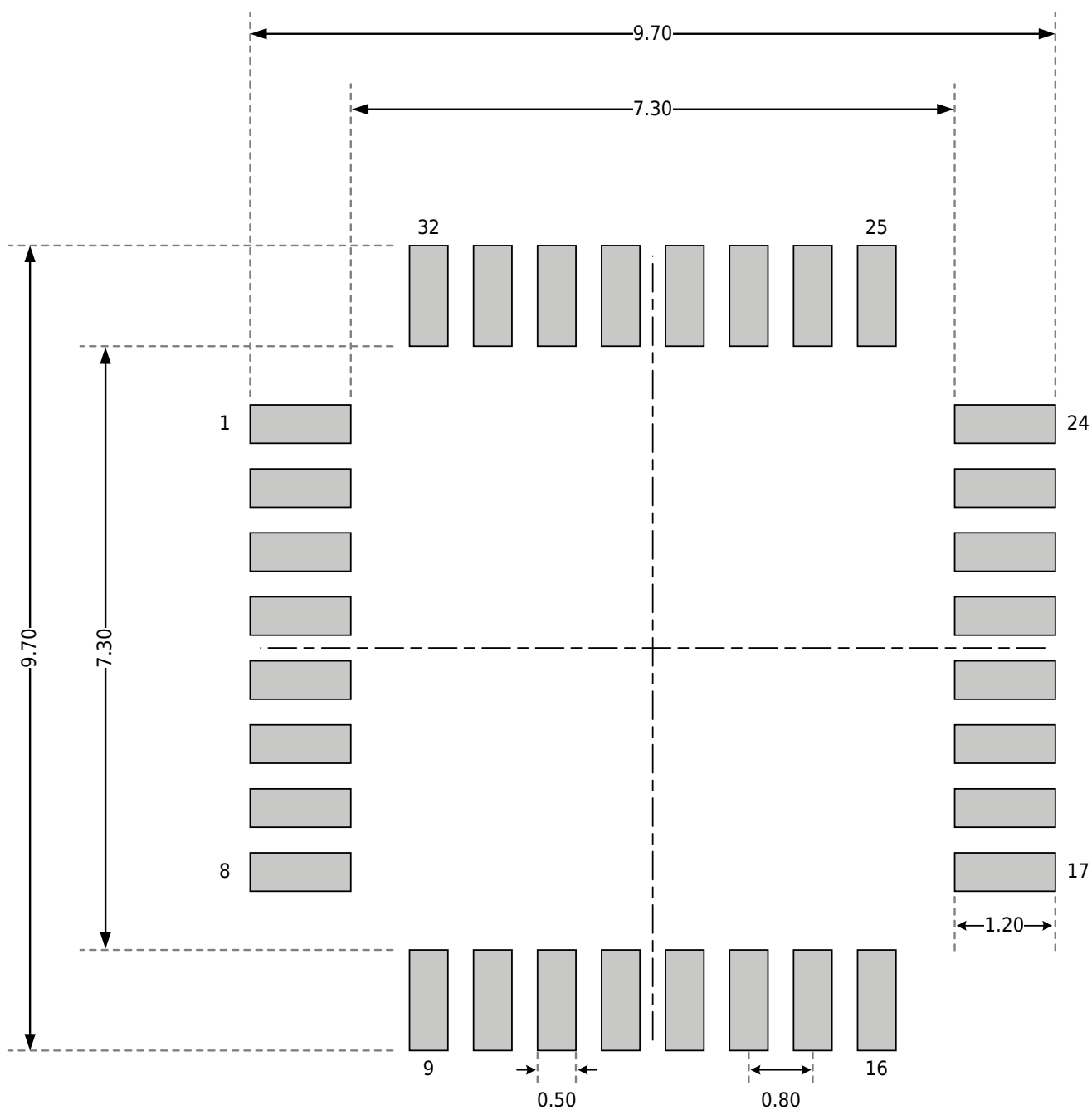
- Dimensions are in millimeters.
- Dimensions are for reference only.

6.2.3 LQFP48 Package (7mm*7mm)

**Note**

- Dimensions are in millimeters.
- Dimensions are for reference only.

6.2.4 LQFP32 Package (7mm*7mm)



Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

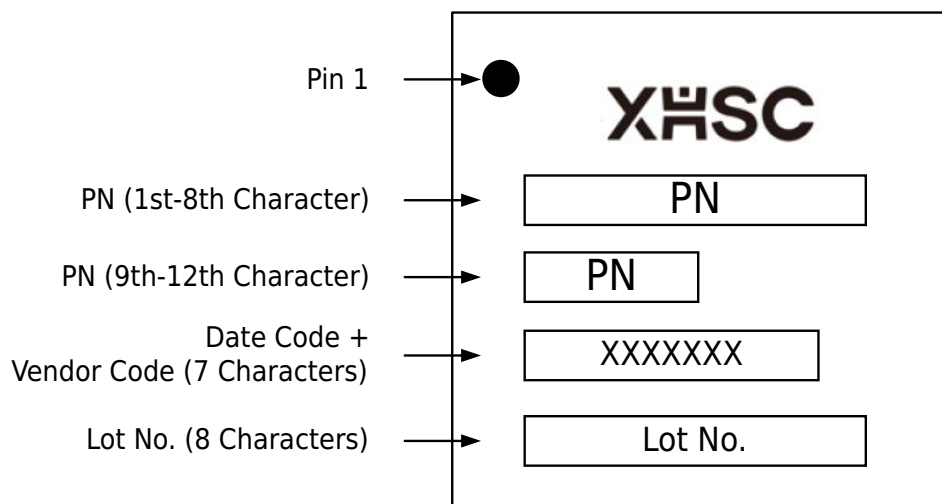
6.3 Package Marking

The location and information description of Pin1 on the front of each package are given below.

LQFP80 package (12mm*12mm)

LQFP64 package (10mm*10mm)

LQFP48 package (7mm*7mm)/LQFP32 package (7mm*7mm)



6.4 Packaging Thermal Resistance Coefficient

When the packaged chip is working at the specified working environment temperature, the junction temperature T_j (°C) of the chip surface can be calculated according to the following formula:

$$T_j = T_A + (P_D * \theta_{JA})$$

- T_A refers to the working environment temperature when the packaged chip is working, the unit is °C;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is °C/W;
- P_D refers to total power dissipation, which is the sum of internal power consumption (P_{INT}) and I/O pin power consumption (P_{IO}), the unit is W.

$$P_D = P_{INT} + P_{IO}$$

► P_{INT} : Internal power consumption, calculated as the product of I_{VCC} and V_{CC} .

► P_{IO} : I/O pin power consumption, calculated as: $P_{IO} = \Sigma(V_{OL} * I_{OL}) + \Sigma((V_{CC} - V_{OH}) * I_{OH})$

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable junction temperature T_{jmax} of the chip.

Table 6-5 Thermal Resistance Coefficient Reference Table For Each Package

Package Type and Dimensions	Thermal Resistance Parameters (θ_{JA})	Unit
LQFP80 12mm*12mm/0.5mm pitch	55±10%	°C/W
LQFP64 10mm*10mm/0.5mm pitch	65±10%	°C/W
LQFP48 7mm*7mm/0.5mm pitch	75±10%	°C/W
LQFP32 7mm*7mm/0.8mm pitch	80±10%	°C/W

7 Ordering Information

Part Number		HC32L186MCTH-LQFP80	HC32L186KCTH-LQFP64	HC32L180JCTH-LQ48	HC32L180FCTH-LQ32	HC32L186MATH-LQFP80	HC32L186KATH-LQFP64	HC32L180JATH-LQ48	HC32L180FATH-LQ32
I/O		72	56	40	26	72	56	40	26
CPU	Core	Cortex-M0+	Cortex-M0+	Cortex-M0+	Cortex-M0+	Cortex-M0+	Cortex-M0+	Cortex-M0+	Cortex-M0+
	Frequency	48MHz	48MHz	48MHz	48MHz	48MHz	48MHz	48MHz	48MHz
Memory	Flash	256KB	256KB	256KB	256KB	128KB	128KB	128KB	128KB
	RAM	32KB	32KB	32KB	32KB	32KB	32KB	32KB	32KB
Power Supply Voltages		1.8-5.5V	1.8-5.5V	1.8-5.5V	1.8-5.5V	1.8-5.5V	1.8-5.5V	1.8-5.5V	1.8-5.5V
Temp Range		-40-85°C	-40-85°C	-40-85°C	-40-85°C	-40-85°C	-40-85°C	-40-85°C	-40-85°C
DMAC		2ch	2ch	2ch	2ch	2ch	2ch	2ch	2ch
TIMER	General Timer	4	4	4	4	4	4	4	4
	Advanced Timer	3	3	3	3	3	3	3	3
	LPTimer	2	2	2	2	2	2	2	2
RTC		1	1	1	1	1	1	1	1
WDT		1	1	1	1	1	1	1	1
WWDT		1	1	1	1	1	1	1	1
Connectivity	UART	4	4	2	2	4	4	2	2
	LPUART	2	2	2	1	2	2	2	1
	I2C	2	2	2	2	2	2	2	2
	SPI	2	2	2	1	2	2	2	1
Analog	12-bit ADC	25ch	23ch	17ch	10ch	25ch	23ch	17ch	10ch
	12-bit DAC	1ch	1ch	1ch	1ch	1ch	1ch	1ch	1ch
	OPA	1	1	-	-	1	1	-	-
	VC	3	3	3	3	3	3	3	3
Display	LCD	4*47/6*45/8*43	4*40/6*38/8*36	-	-	4*47/6*45/8*43	4*40/6*38/8*36	-	-
LVD		1	1	1	1	1	1	1	1
CRC		√	√	√	√	√	√	√	√
Security	AES	√	√	√	√	√	√	√	√
Package (mm*mm)		LQFP80(12*12)	LQFP64(10*10)	LQFP48(7*7)	LQFP32(7*7)	LQFP80(12*12)	LQFP64(10*10)	LQFP48(7*7)	LQFP32(7*7)
Packing		Tray	Tray	Tray	Tray	Tray	Tray	Tray	Tray
Pitch		0.5mm	0.5mm	0.5mm	0.8mm	0.5mm	0.5mm	0.5mm	0.8mm

Please contact the sales window for the latest mass production information before ordering.

Revision History

Revision/Date	Changes
Rev1.30 Aug. 28, 2026	1. Typical Application Circuit Diagram: the decoupling capacitor description is optimized. 2. Electrical Specifications: In the "Absolute Maximum Ratings" chapter, the voltage and current tables is combined; 3. Package Specifications: In the "PCB Land Pattern" section, the redundant data is removed;
Rev1.20 Feb. 12, 2026	1. Electrical Specifications: In the "Absolute Maximum Ratings" chapter, the symbol "T_j" representing temperature characteristics is revised to "T_{jmax}"; In the "Supply Current Characteristics" chapter, the XTL condition is modified from "Driver=1" to "Driver=2"; In the "External High-Speed Crystal XTH" chapter, the description of C_{Lx} is changed to "Matching capacitance". Meanwhile, optimize the annotation description; In the "External Low-Speed Crystal XTL" chapter, the description of C_{Lx} is changed to "Matching capacitance", and change the minimum value to "4pF". Meanwhile, optimize the annotation description; In the "Memory Characteristics" chapter, the data of EC_{FLASH} parameters have been optimized based on new conditions;
Rev1.03 May 12, 2025	1. Pin Definitions: The "Module Signal Description" labels have been updated to align with the "Pin Function Description". 2. Electrical Specifications: In the "Memory Characteristics" chapter, the EC_{FLASH} parameter name has been revised to "Erase/Write Cycles (Sector Erase)", with the minimum value changed to "100"; In the "ADC Characteristics" chapter, the unit of $T_{ADCCONV}$ has been adjusted to align with T_S; In the "Operating Conditions-Communication Interface-SPI Characteristics" chapter, parameters such as serial clock cycle, slave data output valid time, and slave data output hold time have been adjusted, table notes have been added: "Data is provided under $V_{CC}=3.0V$ conditions", "Maximum divider coefficient is $PCLK/2$ in master mode and $PCLK/4$ in slave mode". 3. Package Specifications: In the "Package Dimensions" chapter, the eB marking and SECTION B-B have been removed.
Rev1.02 Jan. 6, 2025	1. Feature List: Under ultra-low power performance, "Sleep mode power consumption" has been revised from "2.0μA@3V DeepSleep mode+RTC operation" to "1.5μA@3V DeepSleep mode + RTC operation". 2. Electrical Specifications: The definitions of maximum/minimum values and typical parameter values in the "Parameter Conditions" chapter have been optimized; All data sources in this chapter have been adjusted according to the latest specifications; In the "Operating Conditions-VC Characteristics" chapter, the typical values of the $T_{response}$ parameter have been revised from "250, 140" to "2500, 1400"; In the "RESETB Pin Characteristics" chapter, the units for $V_{F(RESETB)}$ and $V_{NF(RESETB)}$ have been changed from "ns" to "μs". 3. Package Specifications: in the "Packaging Thermal Resistance Coefficient" chapter, the description of P_D is adjusted to make it more practical.

Revision/Date	Changes
Rev1.02 Jan. 6, 2025	4. Ordering Information: Adding main frequency and core details.
Rev1.01 May 17, 2024	Added: 1. Add the PF11 port to the port multiplexing table in the "Pin Function Description" chapter of the "Pin Definitions" chapter. Modified: 1. In the "Feature List" chapter, under ultra-low power performance, the Sleep mode power consumption has been revised from "30μA/MHz@3V@24MHz" to "23μA/MHz@3V@48MHz". 2. In the "Electrical Specifications-Parameter Conditions" chapter, the character "δ" has been revised to "σ" in the descriptive content. 3. In the "Electrical Specifications-Absolute Maximum Ratings" voltage characteristics table, the maximum value of the VCC-VSS parameter has been revised from "5.5" to "6.0". 4. In the "Electrical Specifications-Operating Conditions-Supply Current Characteristics" chapter, the current data for I_{DD} (DeepSleep) has been revised. 5. In the "Electrical Specifications-Operating Conditions-Internal Clock Source Characteristics-RC10K" chapter, the minimum value of the Dev parameter has been revised from "50" to "-50". Delete: 1. In the "Pin Function Description" under "Pin Definitions" chapter, the VC0_INN10 description has been removed from the ANALOG in PB00.
Rev1.00 Apr. 22, 2024	First official release.