XIAOHUA SEMICONDUCTOR

HC32M458 Series

32-bit ARM® Cortex®-M4 Microcontroller

Datasheet

Rev1.00

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Feature List

ARM Cortex-M4 32-bit MCU+FPU, 250DMIPS, 512KB Code Flash, 8KB Data Flash, 64KB SRAM, 11Timers, 2ADCs, 2DACs, 2CMPs, 2OPAs, 4UARTs, 2SPIs, 1I2C

- ARMv7-M architecture, 32-bit Cortex-M4 CPU, integrated FPU, DSP supporting SIMD instructions, and CoreSight standard debug unit.
  The highest operating frequency 200MHz can reach 250DMIPS or 680Coremarks computing performance
- Built-in memory
  - Up to 512KB Code Flash memory with ECC
  - 8KB Data flash
  - 64KB single-cycle access high-speed SRAM with ECC
- Power, clock, reset management
  - System power supply (V_{CC}): 2.7-5.5V
  - 5 independent clock sources: XTAL (4-25MHz); HRC (12MHz), clock accuracy ±1%; MRC (8MHz); LRC (32.768kHz); PLL
  - 13 reset sources: including POR, PVD1R/ PVD2R, NRST, etc. Each with an independent flag
- Low-power operation
  - Peripheral functions can be independently disabled or enabled
  - 2 low power modes: Sleep mode, Stop mode
- Peripheral operation support system significantly reduces CPU processing load
  - 2-channel DMAC
  - 1 math acceleration unit (MAU)
  - Supports action on signal (AOS) for peripheral events
- High-performance analog
  - 2 independent 12-bit 2.5Msps ADCs
  - 2 independent 8-bit DACs (output only used for CMP negative reference voltage input)
  - 2 independent voltage comparators (CMP)
  - 2 independent operational amplifiers (OPA)
- Timers
  - 2 16-bit Timer4s, supporting 3-phase complementary PWM output with dead time and brake
  - 5 16-bit TimerAs, including 4 TimerAs for 6ch PWM, EMB, and phase shift functions, and 1 TimerA for 6ch PWM, EMB, and capture functions
  - 2 16-bit Timer0s (basic timers)
  - 2 WDTs (including WDT and SWDT)
- Up to 52 GPIOs
- Up to 7 communication interfaces
  - 4 USARTs, supporting ISO7816-3, LIN protocol
  - 2 SPIs
  - 1 I2C, supporting SMBus
- Other functions: CRC16/32, TRNG
- Package form: LQFP64

Support Model

HC32M458KETI-LQFP64	HC32M458KCTI-LQFP64

Statement

Precautions

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Preface

Number Format

- 0x prefix is used for hexadecimal numbers
- 0b prefix is used for binary numbers
- Numbers without prefix are in decimal representation

Security Statement

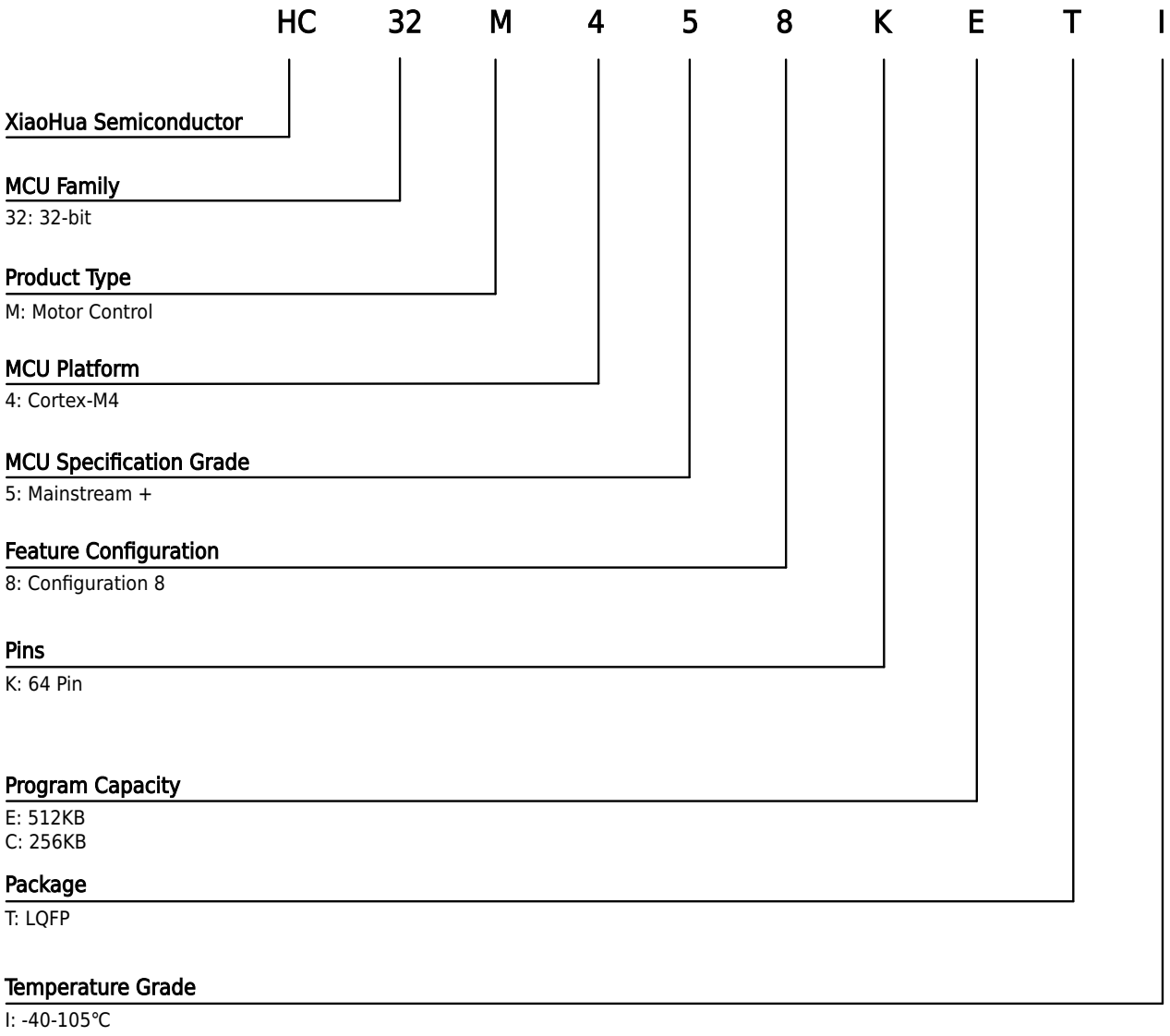
There may be potential security problems due to the use of a certain function or protocol, which need to be declared to remind users and avoid security risks.

Contents

1 Product Overview

1.1 Product Lineup

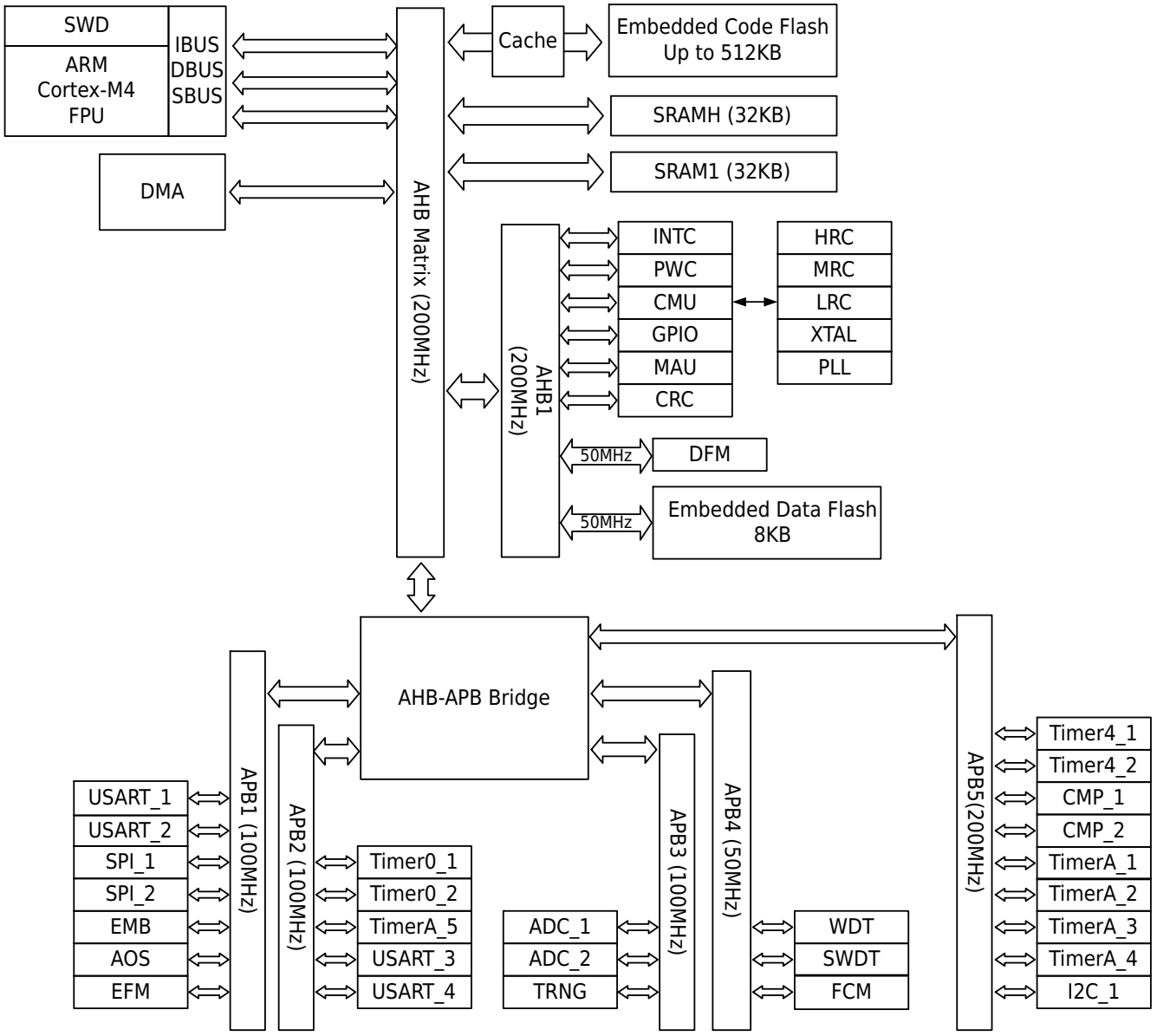
Product Name



Model Function Comparison Table

Product Name		HC32M458KCTI	HC32M458KETI
Pins		64	
GPIOs		52	
CPU	Core	Cortex-M4	
	Frequency	200MHz	
Storage Space	Code Flash (w/i ECC)	256KB	512KB
	Data Flash	8KB	
	SRAM (w/i ECC)	64KB	
Clock	HRC	12MHz	
	MRC	8MHz	
	LRC	32.768kHz	
	XTAL	4-25MHz	
Supply Voltage Range		2.7-5.5V	
Temperature Range		-40-105℃	
External Port Interrupt		EIRQ * 8	
DMA Controller		1unit * 2ch	
Timer and Counter	Timer0	2unit	
	TimerA	5unit	
	Timer4	2unit	
	WDT	1ch	
	SWDT	1ch	
Connectivity	USART	4ch	
	I2C	1ch	
	SPI	2ch	
Analog	12-bit ADC	2unit, 17ch	
	8-bit DAC	2ch (Only used for CMP negative input reference voltage)	
	CMP	2ch	
	OPA	2ch	
	PVD	√	
Security	TRNG	√	
Co-processing	MAU	√	
CRC		√	
FCM		√	
Debugging Interface	SWD	√	
Package		LQFP	

1.2 Functional Block Diagram



Note

Products in different packages support varying resources. For detailed specifications, please refer to Model Function Comparison Table.

2 Functional Description

2.1 CPU

HC32M458 Series integrates embedded ARM® Cortex-M4 with FPU 32-bit simplified command CPU, which realizes less pins and low power consumption, and provides excellent computing performance and rapid interrupt response capability. The on-chip integrated storage capacity can give full play to the excellent command efficiency of ARM® Cortex-M4. The CPU supports DSP command, which can realize efficient signal processing operations and complex algorithms. Single-point precision FPU (Floating Point Unit) can avoid command saturation and speed up software development.

2.2 BUS

The main system consists of a 32-bit multi-layer AHB bus matrix, enabling the interconnection of the following host buses and slave buses:

- Host bus
  - Cortex-M4 core CPU-I bus, CPU-D bus, CPU-S bus
  - System DMA bus
- Slave bus
  - Code Flash ICODE bus
  - Code Flash DCODE bus
  - Code Flash MCODE bus (The bus for accessing Code Flash by components other than the CPU on the host)
  - System SRAMH (SRAMH 32KB) bus
  - System SRAM (SRAM1 32KB) bus
  - APB1 peripheral bus (AOS/EFM/EMB/SPI/USART)
  - APB2 peripheral bus (USART/Timer0/TimerA)
  - APB3 peripheral bus (ADC/TRNG)
  - APB4 peripheral bus (FCM/WDT/SWDT)
  - APB5 peripheral bus (Timer4/TimerA/CMP/I2C)
  - AHB1 peripheral bus (DFM/Data Flash/INTC/GPIO/DMA/CMU/PWC/MAU/CRC)

With the bus matrix, efficient concurrent access from host buses to slave buses can be achieved.

2.3 RMU

The chip is configured with 13 reset modes:

- Power-on Reset (POR)
- NRST Pin Reset (NRST)
- Brown-out Reset (BOR)
- Programmable Voltage Detection 1 Reset (PVD1R)
- Programmable Voltage Detection 2 Reset (PVD2R)
- Watchdog Reset (WDTR)
- Special Watchdog Reset (SWDTR)
- Software Reset (SRST)

- RAM ECC Reset (RAMECCR)
- FLASH ECC Reset (FLASHECCR)
- Clock Frequency Error Reset (CKFER)
- XTAL Error Reset (XTALER)
- Cortex-M4 Lockup Reset (LKUPR)

2.4 CMU

The clock control unit provides a series of clock functions with different frequencies, including: an external high-speed oscillator, one PLL clock, an internal high-speed oscillator, an internal medium-speed oscillator, an internal low-speed oscillator, a clock prescaler, clock multiplexing, and clock gating circuit.

The clock control unit also provides a clock frequency measurement function. The clock frequency measurement circuit (FCM) monitors and measures the measurement target clock using the measurement reference clock. An interrupt or reset occurs when the setting range is exceeded.

AHB, APB, and Cortex-M4 clocks are derived from the System Clock. The maximum operating clock frequency of the System Clock can reach 200MHz, with 5 selectable clock sources:

1. External High-speed Oscillator (XTAL)
2. PLL Clock (PLL)
3. Internal High-speed Oscillator (HRC)
4. Internal Medium-speed Oscillator (MRC)
5. Internal Low-speed Oscillator (LRC)

For each clock source, it can be individually turned on and off when not in use to reduce power consumption. SWDT uses the internal low-speed oscillator as its counting clock source.

2.5 PWC

Power controller is used to control the supply, switching and detection in run modes and low power modes. The power controller consists of a power consumption control logic (PWCL), a power supply voltage detection unit (PVD).

The operating voltage (VCC) of the chip is 2.7V to 5.5V. The voltage regulator (LDO) supplies power to the VDD domain. The chip provides two low-power modes: SLEEP mode and STOP mode through the power consumption control logic (PWCL).

The power voltage detection unit (PVD) provides functions such as power on reset (POR), power down reset (PDR), brown out reset (BOR), programmable voltage detection 1 (PVD1), programmable voltage detection 2 (PVD2). Among them, POR, PDR, and BOR control the chip reset action by detecting the VCC voltage. PVD1 detects the VCC voltage and resets or interrupts the chip according to the register settings. PVD2 detects VCC voltage or external input detection voltage, and generates reset or interrupt according to register selection.

The analog blocks are equipped with dedicated supply pins for improved analog performance.

2.6 ICG

After the chip's reset is released, the hardware circuit reads data from FLASH addresses 0x00080000-0x00080017 and loads it into the Initialization Configuration (ICG) register. Addresses 0x00080014-0x00080017 is reserved for future functions. Users can modify the ICG register by programming or erasing the corresponding FLASH addresses of the sectors. Addresses 0x00080018-0x0008001F are the data security protection enable region. The register reset value is determined by FLASH data.

2.7 EFM

This system contains a 512KBytes capacity Code Flash memory, divided into 512 sectors, each with a capacity of 1KByte.

The controller performs read, program, erase, and full erase operations on the Code Flash memory via the ICODE, DCODE, and MCODE buses; code execution is accelerated through a cache mechanism. This controller also supports erase/write protection for the Code Flash memory and write protection for control registers.

Code Flash Main Features:

- Two independent cache areas: ICODE bus cache space 1KBytes (64x128-bit); DCODE bus cache space 128Bytes (8x128-bit)
- Supports prefetching
- Data ECC function for security protection, can correct 1-bit error, detect 2-bit error
- Supports proprietary code read protection (PCROP) function
- Supports Code Flash data CRC check function
- Support data security protection
- Provides 16Byte product name information

2.8 DFM

The system contains a 8KBytes capacity Data Flash memory, divided into 64 sectors, each with a capacity of 128Bytes.

Data Flash is only used for storing user data and cannot be used for storing program instructions.

The controller supports erase, programming, and read operations on the Data Flash memory. This controller also supports write protection for the Data Flash memory and write protection for control registers.

Data Flash Main Features:

- 8KB capacity: 128Byte/sector, total 64 sectors
- Supports sector erase and full chip erase
- Supports 8-bit/16-bit write operations and continuous write operations
- Supports 8-bit/16-bit data read operations
- Illegal access causes system to enter Hard Fault:
  - Fetching instructions from Data Flash for execution
  - Data Flash receives 32-bit (Word) read/write requests
  - Accessing Data Flash when it is in low-power mode
  - Accessing Data Flash when it is in erase/program state
- Each sector has 2-bit erase/program protection control bits to improve reliability
- Supports low-power mode

2.9 SRAM

This product has 64KB system SRAM (SRAMH/SRAM1).

Each SRAM can be accessed as a byte, half-word (16 bits), or full-word (32 bits). All SRAM read and write operations can be performed at the fastest CPU speed (200MHz) with 0 wait period (i.e., in 1 clock cycle).

SRAM1 and SRAMH feature ECC (Error Checking and Correcting) check. The ECC check is a single-error-correcting, double-error-detecting (SECDED) code, meaning it can correct a single-bit error and detect a double-bit error. When an ECC check error occurs while reading SRAM data, an SRAM ECC check reset or NMI interrupt will be triggered.

2.10 GPIO

Main features of GPIO:

- Each port group has 16 I/O pins, which may be less than 16 depending on actual configuration
- Supports pull-up and pull-down input
- Supports push-pull, open-drain output mode
- Supports combinations of high/low drive strength and fast/slow slew rate modes
- Supports free switching between CMOS/Schmitt input modes
- Supports for external interrupt input
- Supports I/O pin peripheral function multiplexing, one I/O pin can have up to 29 optional multiplexing functions
- Individual I/O pins can be programmed independently
- Each I/O pin can select 2 functions to be enabled at the same time (does not support 2 output functions to be enabled at the same time)

2.11 INTC

The Interrupt Controller (INTC) selects interrupt events to be sent to the CPU to generate interrupts (maskable interrupts and non-maskable interrupts); selects interrupt events to wake up the CPU from low power consumption mode (WFI and WFE); selects interrupt events to wake up the system from low power consumption mode (Sleep mode and Stop mode); and controls external interrupts and software interrupts.

The main features of INTC are as follows:

1. Maskable interrupts: INTC is equipped with 142 interrupt events, which are processed and sent to NVIC as interrupt requests (IRQ). It supports 79 IRQs, each IRQ corresponds to one or more interrupt events.

   Note

   For more instructions on exception and NVIC programming, please refer to the "Arm Cortex-M4 Processor Technical Reference Manual".

2. Programmable priority of NVIC: 16 programmable priorities (4-bit interrupt priority register is used).
3. Non-maskable interrupts: Multiple system interrupt event requests can be independently selected as non-maskable interrupts, and each interrupt event is equipped with independent enable, flag and flag clear registers.
4. Equipped with 8 external pin interrupt events.
5. Equipped with multiple interrupt events, please refer to the "Interrupt Event List" in the "Interrupt Controller (INTC)" chapter of "Reference Manual" for the specific number.
6. Equipped with 32 software interrupt events.
7. Interrupt wakes up system Sleep mode and Stop mode.

2.12 AOS

The Automatic Operation System (AOS) is used to achieve coordination between peripherals without the assistance of the CPU. It utilizes events generated by peripherals as AOS sources, such as timer comparison matches, timer counting overflow, various states of the sending and receiving data of the communication module (idle, receive data full, transmit data end, transmit data empty), ADC conversion end events, etc., to trigger actions of other peripherals. The triggered peripheral actions are referred to as AOS targets.

Users can select one or more AOS sources to trigger the same AOS target based on their needs.

Main features of AOS:

The AOS has multiple trigger sources, please refer to the "AOS Source Events" in the "Automatic Operation System (AOS)" chapter of "Reference Manual". Unless specifically restricted, each AOS target can select one or more of these as trigger sources. When multiple trigger sources are required, two common trigger sources can be selected through the common trigger source selection registers 1 and 2, which are shared by all AOS targets. Thus, for an AOS target, up to 3 trigger sources can be selected, and any of these can trigger the AOS target action when an event occurs.

Triggering can be done by hardware from peripheral circuits or by software through register writes.

The peripherals and their quantities that can serve as AOS targets are as follows:

- 3 DMA trigger targets
- 6 ADC trigger targets for ADC sequence triggering

2.13 DMA

DMA is used to transfer data between memory and peripheral function modules, enabling data exchange between memories, between memory and peripheral function modules, and between peripheral function modules without CPU involvement.

Main features of DMA:

- The DMA bus is independent of the CPU bus and transmits data according to the AMBA AHB-Lite bus protocol
- With 1 DMA control units, a total of 2 independent channels, which can independently operate different DMA transfer functions
- The start source of each channel is configured through an independent trigger source selection register
- 1 block per request
- The data block is a minimum of one data and can be up to 1024 data
- The width of each data item can be configured as 8-bit, 16-bit, or 32-bit
- It can be configured for 1-65535 transfers or infinite transfers
- The source address and destination address can be independently configured as fixed, incrementing, decrementing, repeated jump, or specified offset jump
- 3 types of interrupts can be generated: block transfer completed interrupt, transfer completed interrupt, and transfer error interrupt. Each interrupt can be configured to be masked or unmasked. Among them, block transfer completed and transfer completed can be used as event outputs, serving as trigger sources for other peripheral modules
- Support chain transfer function, enabling the transfer of multiple data blocks in a single request
- Support channel reset triggered by external events

- Support software-triggered start of transfer and software-triggered channel reset
- When not in use, it can be set to stop state to reduce power consumption

2.14 CMP

Voltage Comparator (hereinafter referred to as CMP) is a peripheral module that compares two analog voltages and outputs the comparison result. This product is equipped with 2 comparison channels: CMP1 and CMP2.

CMP Main features:

- 2 comparison channels can independently perform normal comparison
- The combination of CMP1 and CMP2 can implement the window comparison function
- Each comparison channel's positive and negative voltage inputs have multiple input sources (IO, DAC) to choose from
- Hysteresis voltage is configurable
- A noise filter can filter the comparator output, with 7 sampling clocks to choose from
- Timer PWM can be used for comparator blanking window control
- Interrupts can be generated at the edges of comparison result changes, other peripherals can be triggered, and STOP mode can be woken up
- Compare results can be monitored through registers and output to the external pin VCOUT
- Compare results can be used for EMB control events

2.15 ADC

The 12-bit ADC is an analog-to-digital converter that adopts the successive approximation method. This MCU is equipped with 2 ADC units, a maximum of 16 channels, which can convert analog signals from external pins and inside the chip. Analog input channels can be arbitrarily combined into a sequence for single scan or continuous scan conversion. Supports continuous multiple conversions on any specified channel and averaging of the conversion results. The ADC block also includes an analog watchdog function that monitors the conversion results of any specified channel to detect if they exceed user-set ranges.

The main features of the ADC are as follows:

- High Performance
  - 12-bit resolution
  - The clock source of the ADC sampling conversion clock ADCLK is PCLK4 (set by the CMU_ADCKSEL register)
  - Sampling Rate: 2.5Msps (ADCLK=80MHz, 12-bit, 18 sampling cycles, 14 conversion cycles)
  - Independent programming of channel sampling time is supported
  - Each channel has an independent data register and physical channel register
  - Data registers can be configured for left/right alignment
  - Continuous multiple conversion averaging function
  - Oversampling function
  - Analog watchdog to monitor conversion results
  - The ADC module can be set to stop when not in use
- Analog Input Channel
  - Total of 17 external analog inputs

  - 1 internal analog signal: internal reference voltage 0.8V
- Conversion Start Conditions
  - Software setup conversion started
  - Peripheral synchronously trigger the conversion to start
  - External pin trigger the conversion to start
- Conversion Mode
  - Each unit has 3 scan sequences A, B, C, optionally specifying a single or multiple channels
  - Sequence A single scan
  - Sequence A continuous scan
  - Dual sequence scan, with sequences A and B independently selecting trigger sources, and sequence B having higher priority than A
  - Triple sequence scan, with sequences A, B, and C independently selecting trigger sources, sequence C having higher priority than B, and sequence B having higher priority than A.
- Interrupt and Event Signal Output
  - Sequence A scan end interrupt and event ADC_EOCA
  - Sequence B scan end interrupt and event ADC_EOCB
  - Sequence C scan end interrupt and event ADC_EOCC
  - Analog watchdog 0 compare interrupt and event ADC_CMP0
  - Analog watchdog 1 compare interrupt and event ADC_CMP1
  - All the event outputs mentioned above can start DMA

2.16 Timer4

The General Control Timer 4 is a timer module designed for three-phase motor control, offering a variety of solutions for different three-phase motor control applications. It supports both triangular and sawtooth waveform modes, enabling the generation of various PWM waveforms. It also features buffer functionality and supports EMB control. 2 unit of Timer4 is carried in this product family.

The following table outlines the basic functions and features of Timer4.

Table 2-1 Basic Functions and Features of Timer4

Waveform mode	Sawtooth wave, triangle wave
Basic function	Up/Down-counting direction
	Buffer function
	General PWM output
	General compare match event
	Overflow/Underflow/Reload count match event
	Special compare match event
	Software-synchronized counter start
	EMB control

Interrupt type	General compare match interrupt
	Count period match interrupt
	Reload count match interrupt
	Special compare match interrupt

2.17 EMB

The emergency brake module is a function module that generates contorl events output to the timer when certain conditions are met to stop the timer or change the PWM signal output to the external motor. The following factors are used to generate control events:

- External port input level change
- Level of Timer4 PWM output port occurs in phase (same high or same low)
- Voltage comparator comparison results
- System error occurred
- Write register software control

2.18 TimerA

The General Timer A (TimerA) is a timer with a 16-bit counting width and 6-channel PWM output. The timer supports two waveform modes, triangle wave and sawtooth wave, and can generate various PWM waveforms (single-side aligned PWM, double-side symmetrical PWM, multiphase interleaved output PWM); supports synchronous start of counter; the compare reference value register supports buffer function; supports cascading between units to achieve 32-bit counting; supports 2-phase quadrature encoding count and 3-phase quadrature encoding count; supports PWM output control via EMB event reception. This product series is equipped with 5 TimerA units, each unit has 6 channels of PWM output. The 5 units can achieve a maximum of 30 channels of PWM output in total.

The basic functions and features of TimerA are shown in the table below:

Table 2-2 Basic Functions and Features of TimerA

Waveform mode	Sawtooth wave, triangular wave
Basic function	Up/Down-counting direction
	Synchronous startup counter
	Reference value buffer function
	Period buffer function
	32-bit cascading count
	Quadrature encoding count
	6 PWM output
	Multiphase interleaved PWM output
	General compare match event output
	Special compare match event output
	PWM output control via EMB event reception

Interrupt type	Compare match interrupt
	Period match interrupt

2.19 Timer0

General Timer 0 (Timer0) is a basic timer that can realize synchronous counting and asynchronous counting. The timer contains two channels (CH-A and CH-B) that can generate compare match events and count overflow events during counting. This event can trigger an interrupt and can be used to trigger other module actions. This series of products is equipped with 2 units of Timer0.

2.20 WDT/SWDT

This product has two watchdog counters: one is a dedicated watchdog counter (SWDT) with an internal RC (32kHz) as its count clock source, and the other is a general-purpose watchdog counter (WDT) with PCLK3 as its count clock source. Both the dedicated watchdog and the general-purpose watchdog are 16-bit down counters used to monitor software faults caused by external interference or unforeseen logic conditions that cause the application to deviate from normal operation.

Both watchdogs support the window function. The window interval can be preset before the count starts, and when the count value is within the window interval, the counter can be refreshed and the count restarted.

Table 2-3 Basic Features of Watchdog Timer

Count Clock	● SWDT: 1/16/32/64/128/256/2048 division of SWDTCLK ● WDT: 4/64/128/256/512/1024/2048/8192 division of PCLK3
Maximum Overflow Time	● SWDT: 1.16 hours (SWDTCLK=32kHz) ● WDT: 10.7 seconds (PCLK3=50MHz)
Counting Mode	Decrement count
Window Function	Can set window interval, define the allowable interval of refresh action
Startup Mode	1. Hardware startup 2. Software startup
Stop Condition	1. Resetting 2. Underflow, refresh error occurs and then restart: ● In hardware startup mode, it starts automatically after a reset or interrupt request is output ● In software startup mode, set refresh register again
Interrupt/Reset Conditions	1. Count underflow 2. Refresh error

2.21 USART

This product is equipped with 4 units of Universal Synchronous Asynchronous Receiver/Transmitter (USART) modules, which can flexibly exchange full-duplex data with external devices; the USART equipped in this product supports universal asynchronous serial communication interface (UART) , clock synchronous communication interface, and LIN communication interface. Support modem operation

(CTS/RTS operation), multiprocessor operation, DE function, receive timeout function. USART1 supports the STOP mode wake-up function via the RX line.

The specific function allocation is as follows:

Function	Support Module			
	USART1	USART2	USART3	USART4
UART	✓	✓	✓	✓
Multiprocessor Communication	✓	✓	✓	✓
Clock Synchronization Communication	✓	✓	✓	✓
Wake-up from STOP Mode via RX Line	✓	-	-	-
Fractional Baud Rate	✓	✓	✓	✓
LIN	✓	✓	✓	✓
UART Receive Timeout Function	✓	✓	✓	✓
RS485 Driver Enable	✓	✓	✓	✓
Automatic Baud Rate Detection	✓	✓	✓	✓

2.22 I2C

I2C (Inter-Integrated Circuit) used as an interface between the microcontroller and the I2C serial bus. Provide multi-master mode function, which can control the protocol and arbitration of all I2C buses. Standard mode and fast mode are supported. SMBus is also supported.

Main features of I2C:

- I2C bus mode and SMBUS bus mode are optional. Master mode and slave mode are optional. Automatically ensure various preparation times, hold times, and bus idle times corresponding to the transfer rate
- Standard mode up to 100kbps, fast mode up to 400kbps
- The start condition, restart condition, and stop condition are automatically generated, and the start condition, restart condition, and stop condition of the bus can be detected
- Supports up to 128 slave mode addresses. Supports 7-bit address format and 10-bit address format. Broadcast call address, SMBus host address, SMBus device default address, SMBus alarm address can be detected
- Answer bits can be automatically determined when sent. Answer bits can be automatically sent when reception
- Handshake function
- Arbitration function
- Timeout function, can detect SCL clock stop for a long time
- SCL input and SDA input have built-in digital filters that are programmable to filter
- Communication error, receive data full, send data empty, one frame send end, address match unanimously interrupt
- 2-stage transmit FIFO and 2-stage receive FIFO

2.23 SPI

This product is equipped with 2-channel serial peripheral interface SPI, supports high-speed full-duplex serial synchronous transmission, and facilitates data exchange with peripheral devices. Users can set the range of 3/4-wire, master/slave and baud rate as as required.

Table 2-5 SPI Main Features

Essentials	Description
Serial Communication Function	● Supporting 4-wire SPI mode and 3-wire clock synchronization mode ● Supports full-duplex synchronous communication mode, transmit-only communication mode, and slave receive-only communication mode ● Polarity and phase of adjustable communication clock SCK
Data Format	● Selectable data shift order: MSB start/LSB start ● Selectable data width: 4/5/6/7/8/9/10/11/12/13/14/15/16/20/24/32 bits ● A maximum of 4 frames width of 32-bit data can be transmitted or received at a single time
Baud Rate	● The baud rate can be adjusted by the built-in special baud rate generator in master mode. The baud rate ranges from 2 to 256 frequency division of PCLK1. ● Maximum baud rate allowed in slave mode is 6 frequency division of PCLK1
Data Buffer	● With 16-byte data buffer ● Supports double buffering
Error Monitoring	● Mode fault error monitoring ● Data overload error monitoring ● Data underload error monitoring ● Parity error monitoring
Chip Selection Signal Control	● Each channel is configured with 4 chip-selected signal line ● The relative timing relationship between the chip select signal and the communication clock can be adjusted ● The inactive time of the chip select signal between two consecutive communications can be adjusted ● Polarity adjustable
Transmission Control in Master Mode	● Start transmission by writing data to the data register ● Communication auto suspend function
Interrupt	● Receive buffer is full ● Transmit buffer is empty ● SPI error (mode/overload/underload/parity) ● SPI vacant ● Transmit complete (event source only)

Essentials	Description
Low Power Control	• Configurable module stop
Other Functions	• SPI initialization function

2.24 CRC

CRC supports 11 kinds of polynomial counting, which are CRC16/CCITT, CRC16/CCITT-FALSE, CRC16/XMODE, CRC16/IBM, CRC16/MAXIM, CRC16/USB, CRC16/MODBUS, CRC16/X25, CRC32, CRC32/MPEG-2 and CRC64.

2.25 MAU

The Math Arithmetical Unit (MAU) is a hardware-accelerated computing module that includes three types of operations: square root, sine, and arctangent. It supports square root, sine, and arctangent operations for fixed-point numbers. The sine function supports an operation precision of $360°/2^{12}$.

2.26 TRNG

TRNG is a random number generator based on continuous analog noise, providing 64-bit random numbers.

2.27 DBGC

This MCU's core is Cortex-M4, which includes hardware for advanced debugging functions. Using these debugging functions, the core can be stopped when fetching instructions (instruction breakpoint) or accessing data (data breakpoint). When the core is stopped, the internal state of the core and the external state of the system can be queried. After the query completes, the kernel and system are restored and program execution is restored.

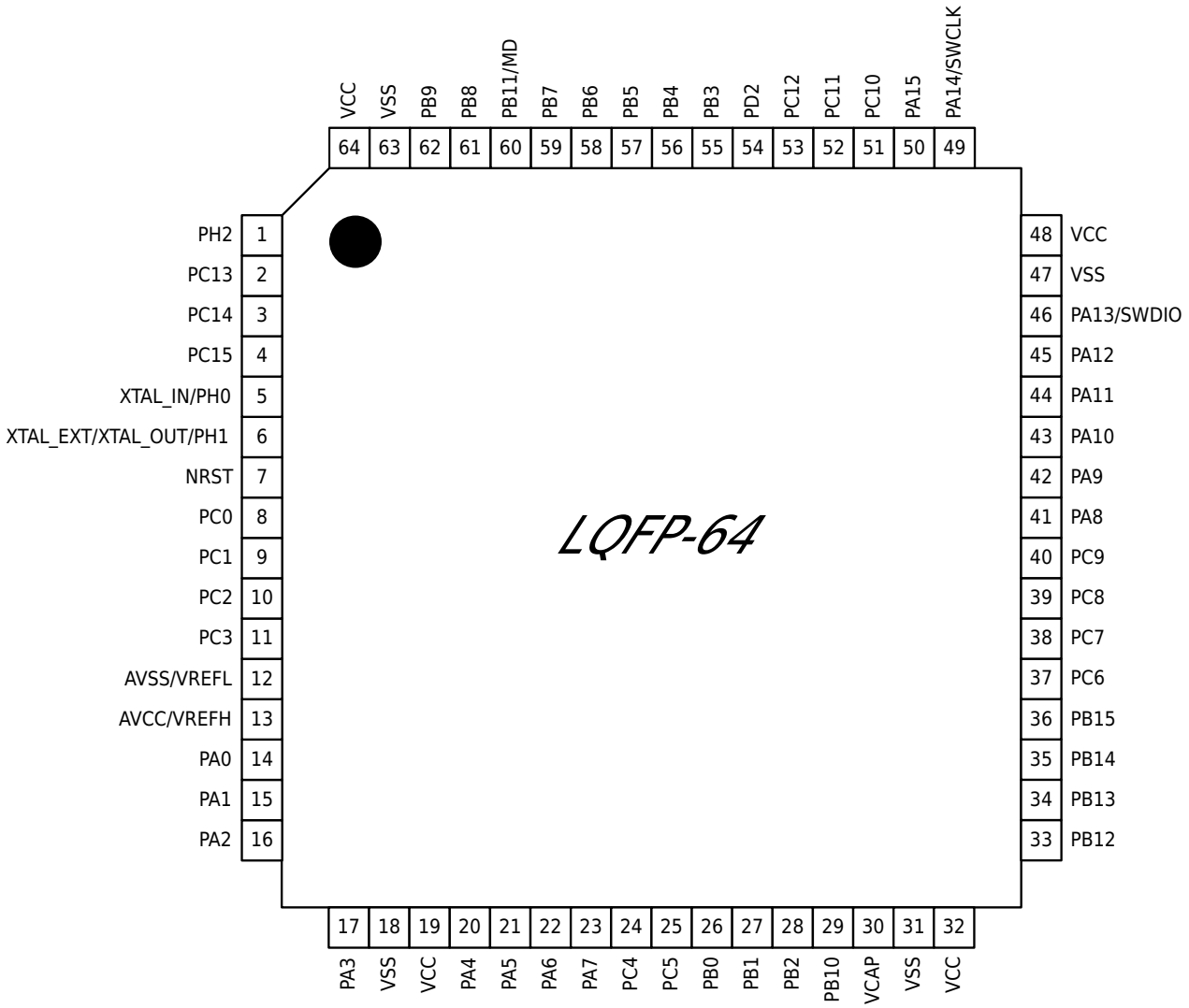
Debugging interface supported:

- Serial debug trace interface SWD

3 Pin Definitions

3.1 Pinout

3.1.1 LQFP64 Package



3.2 Pin Function Table

LQFP64	Pin Name	Analog	EIRQ	SWD	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10~31	Func
					GPO	other	TMR4, VCOUT	TMR4, TMRA	TMRA	TMRA	EMB, TMRA	USART, SPI	USART	TMR4, TMRA		Group
1	PH2		EIRQ2			FCMREF	TMR4_2_CLK	TMRA_4_TRIG	TMRA_4_PWM5	TMRA_3_TRIG	EMB_IN4	USART4_CK	USART1_CTS			FG2
2	PC13		EIRQ5				VCOUT2	TMR4_1_ADSM	TMRA_4_PWM6	TMRA_2_PWM2/ TMRA_2_CLKB		USART3_CK	USART1_RTS			FG2
3	PC14		EIRQ6				TMR4_1_OVH		TMRA_4_PWM5		EMB_IN2		USART2_CTS			
4	PC15		EIRQ7				TMR4_1_OWH	TMR4_1_CLK	TMRA_4_PWM6				USART2_RTS			
5	PH0	XTAL_IN	EIRQ0							TMRA_5_PWM3						
6	PH1	XTAL_EXT/ XTAL_OUT	EIRQ1				TMR4_1_CLK			TMRA_5_PWM4						
7	NRST															
8	PC0	ADC12_IN10+ CMP1_INP7+ CMP2_INP7	EIRQ0				TMR4_1_PCT		TMRA_2_PWM5							FG1
9	PC1	ADC12_IN11	EIRQ1				TMR4_1_ADSM		TMRA_2_PWM6							FG1
10	PC2	ADC1_IN12	EIRQ2						TMRA_2_PWM3		EMB_IN3					FG1
11	PC3	ADC1_IN13+ CMP1_INM2	EIRQ3			MCO			TMRA_2_PWM4							FG1
12	AVSS/ VREFL															
13	AVCC/ VREFH															
14	PA0	ADC1_IN0+ CMP1_INP1	EIRQ0			TMR4_1_OVH	TMR4_2_OUH		TMRA_2_PWM1/ TMRA_2_CLKA	TMRA_1_PWM1/ TMRA_1_CLKA	TMRA_2_TRIG	SPI1_NSS1	USART3_CTS			FG1
15	PA1	ADC1_IN1+ CMP1_INP2	EIRQ1				TMR4_2_OUL		TMRA_2_PWM2/ TMRA_2_CLKB	TMRA_3_TRIG		SPI1_NSS2	USART4_CTS			FG1
16	PA2	ADC1_IN2+ CMP1_INP3	EIRQ2				TMR4_2_OVH		TMRA_2_PWM3	TMRA_5_PWM1/ TMRA_5_CLKA		SPI1_NSS3	USART4_CTS			FG1
17	PA3	ADC1_IN3+ CMP1_INP4+ CMP2_INP4	EIRQ3				TMR4_2_OVL		TMRA_2_PWM4	TMRA_5_PWM2/ TMRA_5_CLKB		USART2_CK	USART3_RTS	TMRA_2_PWM1/ TMRA_2_CLKA		FG1
18	VSS															
19	VCC															
20	PA4	ADC12_IN4+ CMP2_INP1+ CMP1_INP8	EIRQ4			TMR4_1_OWH	TMR4_2_OWH			TMRA_3_PWM5		USART2_CK				FG1
21	PA5	ADC12_IN5+ CMP2_INP2	EIRQ5				TMR4_2_OWL		TMRA_2_PWM1/ TMRA_2_CLKA	TMRA_3_PWM6	TMRA_2_TRIG	SPI1_NSS1				FG1
22	PA6	ADC12_IN6+ CMP2_INP3+ OPA1O	EIRQ6				TMR4_2_ADSM	TMR4_1_PCT		TMRA_3_PWM1/ TMRA_3_CLKA	EMB_IN2	SPI1_NSS2				FG1
23	PA7	ADC12_IN7+ CMP12_INM1	EIRQ7				TMR4_1_OUL		TMRA_1_PWM5	TMRA_3_PWM2/ TMRA_3_CLKB	EMB_IN3	SPI1_NSS3				FG1
24	PC4	ADC1_IN14+ CMP2_INM2	EIRQ4				TMR4_2_OUH			TMRA_3_PWM5		USART1_CK				FG1
25	PC5	ADC1_IN15+ CMP1_INM3	EIRQ5				TMR4_2_OUL			TMRA_3_PWM6						FG1
26	PB0	ADC12_IN8+ CMP1_INP5	EIRQ0				TMR4_1_OVL		TMRA_1_PWM6	TMRA_3_PWM3		USART4_CK				FG1
27	PB1	ADC12_IN9+ CMP1_INP6+ CMP2_INP6+ OPA2O	EIRQ1				TMR4_1_OWL		TMRA_1_PWM1/ TMRA_1_CLKA	TMRA_3_PWM4	TMRA_4_PWM4					FG1
28	PB2	PVD2EXINP	EIRQ2			VCOUT	TMR4_1_PCT		TMRA_1_PWM2/ TMRA_1_CLKB	TMRA_5_PWM2/ TMRA_5_CLKB	EMB_IN1					FG1
29	PB10	ADC2_IN12	EIRQ2			ADTRG2	TMR4_2_OVH		TMRA_2_PWM3	TMRA_5_PWM4	TMRA_1_PWM3					FG2
30	VCAP															
31	VSS															
32	VCC															
33	PB12	OPA1P	EIRQ4			VCOUT1	TMR4_2_OVL		TMRA_1_PWM3	TMRA_5_TRIG	EMB_IN2		USART2_CTS			FG2
34	PB13	OPA1N	EIRQ5			VCOUT2	TMR4_1_OUL		TMRA_1_PWM5	TMRA_4_PWM1/ TMRA_4_CLKA	TMRA_3_PWM1/ TMRA_3_CLKA		USART2_RTS			FG2

LQFP64	Pin Name	Analog	EIRQ	SWD	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10~31	Func
					GPO	other	TMR4, VCOUT	TMR4, TMRA	TMRA	TMRA	EMB, TMRA	USART, SPI	USART	TMR4, TMRA		Group
35	PB14	OPA2P	EIRQ6			VCOUT1	TMR4_1_OVL		TMRA_1_PWM6	TMRA_4_PWM2/ TMRA_4_CLKB	TMRA_3_PWM2/ TMRA_3_CLKB		USART1_CTS			FG2
36	PB15	OPA2N	EIRQ7				TMR4_1_OWL	TMRA_1_PWM2/ TMRA_1_CLKB	TMRA_1_PWM4		EMB_IN4	USART3_CK	USART1_RTS			FG2
37	PC6		EIRQ6				TMR4_2_ADSM	TMR4_1_CLK	TMRA_3_PWM1/ TMRA_3_CLKA	TMRA_5_PWM4						FG2
38	PC7		EIRQ7				TMR4_2_CLK	TMR4_1_OVH	TMRA_3_PWM2/ TMRA_3_CLKB	TMRA_5_PWM3						FG2
39	PC8		EIRQ0				TMR4_2_OWH	TMR4_1_OVL	TMRA_3_PWM3	TMRA_5_PWM6		USART3_CK				FG2
40	PC9		EIRQ1			MCO	TMR4_2_OWL	TMR4_1_OUL	TMRA_3_PWM4	TMRA_5_PWM5						FG1
41	PA8	CMP2_INM3	EIRQ0			MCO	TMR4_1_OUH		TMRA_1_PWM1/ TMRA_1_CLKA	TMRA_2_PWM1/ TMRA_2_CLKA		USART1_CK				FG1
42	PA9	CMP2_INP5	EIRQ1				TMR4_1_OVH		TMRA_1_PWM2/ TMRA_1_CLKB							FG1
43	PA10	CMP2_INP8	EIRQ2				TMR4_1_OWH	TMR4_2_CLK	TMRA_1_PWM3	TMRA_5_TRIG		USART1_CK				FG1
44	PA11		EIRQ3				TMR4_1_CLK		TMRA_1_PWM4	TMRA_5_PWM1/ TMRA_5_CLKA	EMB_IN1	USART2_CK	USART3_RTS			FG1
45	PA12		EIRQ4			TMR4_1_ADSM	TMR4_1_OWL	TMR4_2_PCT	TMRA_1_TRIG		TMRA_2_TRIG	USART1_CK	USART3_CTS	TMR4_2_OWL		FG1
46	PA13		EIRQ5	SWDIO			TMR4_2_ADSM	TMRA_5_TRIG	TMRA_2_PWM5			SPI2_NSS1				FG1
47	VSS															
48	VCC															
49	PA14		EIRQ6	SWCLK			TMR4_2_PCT		TMRA_2_PWM6		TMRA_4_TRIG	SPI2_NSS2				FG1
50	PA15		EIRQ7						TMRA_2_PWM1/ TMRA_2_CLKA		TMRA_2_TRIG	SPI2_NSS3				FG1
51	PC10		EIRQ2				TMR4_1_OUH		TMRA_2_PWM5	TMRA_5_PWM1/ TMRA_5_CLKA						FG1
52	PC11		EIRQ3				TMR4_1_OVH		TMRA_2_PWM6	TMRA_5_PWM2/ TMRA_5_CLKB						FG1
53	PC12		EIRQ4				TMR4_1_OWH	TMR4_2_PCT	TMRA_4_TRIG	TMRA_5_PWM3						FG1
54	PD2		EIRQ2					TMR4_2_OVH	TMRA_2_PWM4							FG1
55	PB3		EIRQ3			FCMREF	TMR4_2_CLK		TMRA_2_PWM2/ TMRA_2_CLKB							FG2
56	PB4		EIRQ4				TMR4_2_OWL		TMRA_3_PWM1/ TMRA_3_CLKA							FG2
57	PB5		EIRQ5			ADTRG1	TMR4_2_OWH	TMRA_1_PWM2/ TMRA_1_CLKB	TMRA_3_PWM2/ TMRA_3_CLKB	TMRA_3_TRIG	TMRA_4_TRIG	USART4_CK				FG2
58	PB6		EIRQ6			ADTRG2	TMR4_2_OVL		TMRA_4_PWM1/ TMRA_4_CLKA							FG2
59	PB7		EIRQ7			ADTRG1	TMR4_2_OVH		TMRA_4_PWM2/ TMRA_4_CLKB					TMRA_4_PWM1/ TMRA_4_CLKA		FG2
60	PB11/MD															
61	PB8		EIRQ0				TMR4_2_OUL		TMRA_4_PWM3			USART3_CK				FG2
62	PB9		EIRQ1				TMR4_2_OUH	TMR4_1_ADSM	TMRA_4_PWM4		EMB_IN4	SPI2_NSS1				FG2
63	VSS															
64	VCC															

Func32-63 are primarily serial communication functions (including USART, SPI, I2C), divided into 2 Function Groups (FG1, FG2). Detailed correspondence is shown in the following table.

Table 3-2 Func32-63 Table

	Func32	Func33	Func34	Func35	Func36	Func37	Func38	Func39	Func40	Func41	Func42	Func43	Func44	Func45	Func46	Func47
FG1	USART1_TX	USART1_RX	USART1_RTS	USART1_CTS	USART2_TX	USART2_RX	USART2_RTS	USART2_CTS	SPI1_MOSI	SPI1_MISO	SPI1_NSS0	SPI1_SCK	SPI2_MOSI	SPI2_MISO	SPI2_NSS0	SPI2_SCK
FG2	USART3_TX	USART3_RX	USART3_RTS	USART3_CTS	USART4_TX	USART4_RX	USART4_RTS	USART4_CTS	-	-	-	-	SPI1_MOSI	SPI1_MISO	SPI1_NSS0	SPI1_SCK
	Func48	**Func49**	**Func50**	**Func51**	**Func52**	**Func53**	**Func54**	**Func55**	**Func56**	**Func57**	**Func58**	**Func59**	**Func60**	**Func61**	**Func62**	**Func63**
FG1	I2C_SDA	I2C_SCL	-	-	USART3_TX	USART3_RX	-	-	-	-	-	-	-	-	-	-
FG2	I2C_SDA	I2C_SCL	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Table 3-3 Port Configuration

Package	Port Group	Bits																Pin Count Total	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
LQFP64	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	52
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	-	-	-	-	-	-	-	-	-	-	-	-	-	o	-	-	1	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	3	

Table 3-4 General Functional Specifications

Port		Pull-Up/Pull-Down	Open-Drain Output	Driving Capacity
PortA	PA0-PA15	Support	Support	Low-drive slow-speed, Low-drive high-speed, High-drive slow-speed, High-drive high-speed
PortB	PB0-PB15	Support	Support	Low-drive slow-speed, Low-drive high-speed, High-drive slow-speed, High-drive high-speed
PortC	PC0-PC15	Support	Support	Low-drive slow-speed, Low-drive high-speed, High-drive slow-speed, High-drive high-speed
PortD	PD2	Support	Support	Low-drive slow-speed, Low-drive high-speed, High-drive slow-speed, High-drive high-speed
PortH	PH0-PH2	Support	Support	Low-drive slow-speed, Low-drive high-speed, High-drive slow-speed, High-drive high-speed

Note

Input voltage must not be higher than VREFH/AVCC when used as an analog function.

3.3 Pin Function Description

Table 3-5 Pin Function Description

Categories	Functional Name	I/O	Description
Power	VCC	I	Power supply
	VSS	I	Power ground
	VCAP	IO	Core voltage
	AVCC/VREFH	I	Analog power supply/analog reference voltage
	AVSS/VREFL	I	Analog power ground/analog reference voltage
System	NRST	I	Reset terminal, active low
	MD	I	Mode terminal
PVD	PVD2EXINP	I	PVD2 external input comparison voltage
Clock	XTAL_IN	I	External main clock oscillator interface
	XTAL_EXT/XTAL_OUT	IO	XTAL_EXT external clock input/external main clock oscillator interface
	MCO	O	Internal clock output
GPIO	GPIOxy (x=A to D, H y=0-15)	IO	General input output
EIRQ	EIRQx (x=0-7)	I	Maskable external interrupt
SWD	SWCLK	I	Online debugging interface
	SWDIO	IO	
FCM	FCMREF	I	External reference clock input for clock frequency measurement
Timer4	TMR4_<t>_CLK (<t>=1-2)	I	Counting clock port input
	TMR4_<t>_OUH (<t>=1-2)	IO	PWM port U-phase output
	TMR4_<t>_OUL (<t>=1-2)	IO	PWM port U-phase output
	TMR4_<t>_OVH (<t>=1-2)	IO	PWM port V-phase output
	TMR4_<t>_OVL (<t>=1-2)	IO	PWM port V-phase output
	TMR4_<t>_OWH (<t>=1-2)	IO	PWM port W-phase output
	TMR4_<t>_OWL (<t>=1-2)	IO	PWM port W-phase output
	TMR4_<t>_ADSM (<t>=1-2)	O	Special event output monitoring
	TMR4_<t>_PCT (<t>=1-2)	O	PWM periodic output monitoring

Categories	Functional Name	I/O	Description
TimerA	TMRA_<t>_TRIG (<t>=1-5)	I	External event trigger input
	TMRA_<t>_PWM1/CLKA (<t>=1-5)	IO	External event trigger input or PWM port output or count clock port input
	TMRA_<t>_PWM2/CLKB (<t>=1-5)	IO	External event trigger input or PWM port output or count clock port input
	TMRA_<t>_PWMm (<t>=1-5 m=3-6)	IO	External Event Trigger Input or PWM Port Output
EMB	EMB_INx (x=1-4)	I	Port input control signal
USART	USARTx_TX (x=1-4)	IO	Transmit data
	USARTx_RX (x=1-4)	IO	Receiving data
	USARTx_CK (x=1-4)	IO	Communication clock
	USARTx_RTS (x=1-4)	O	Request transmiting signal
	USARTx_CTS (x=1-4)	I	Clear transmiting signal
SPI	SPIx_MISO (x=1-2)	IO	Master input/slave output data transfer pin
	SPIx_MOSI (x=1-2)	IO	Master output/slave input data transfer pin
	SPIx_SCK (x=1-2)	IO	Transmission clock
	SPIx_NSS0 (x=1-2)	IO	Slave selection input/output pin
	SPIx_NSSy (x=1-2 y=1-3)	O	Slave selection output pin
I2C	I2C_SCL	IO	Clock line
	I2C_SDA	IO	Data line
CMP	VCOUT1	O	CMP1 result output
	VCOUT2	O	CMP2 result output
	VCOUT	O	CMP1-2 result OR output
	CMPx_INPy (x=1-2 y=1-8)	I	CMPx positive analog input
	CMPx_INM2 (x=1-2)	I	CMPx negative analog input
	CMP12_INM1	I	CMP1-2 negative analog input
ADC	ADTRG1	I	ADC1 AD conversion external start source
	ADTRG2	I	ADC2 AD conversion external start source
	ADC12_INx (x=4-11)	I	ADC1-2 shared external analog input port
	ADC1_INx (x=0-3, 12-15)	I	ADC1 external analog input port
	ADC2_IN12	I	ADC2 external analog input port

3.4 Pin Instructions

Table 3-6 Pin Instruction

Pin Name	Usage Notes
VCC	Power Supply. Connect to 2.7V-5.5V and place a decoupling capacitor near the VSS pin (refer to "Electrical Specifications").
VSS	Source ground, connected to 0V.
VCAP	Core Voltage. Place a capacitor near the VSS pin to stabilize the core voltage (refer to "Electrical Specifications").
AVCC/VREFH	Analog Power Supply. Supply power to analog modules; connect to the same voltage as VCC (refer to "Electrical Specifications"). When not using an independent analog power supply, connect the pin to VCC and ensure it is not left floating.
AVSS/VREFL	Analog Power Ground. Supply ground to analog modules; connect to the same voltage as VSS (refer to "Electrical Specifications"). When not using an independent analog power supply, connect the pin to VSS and ensure it is not left floating.
PB11/MD	Mode input. When NRST is released (changing from low level to high level), this pin must be fixed at low level. Recommended to connect a resistor (4.7kΩ) to VSS (pull-down).
NRST	Reset pin (NRST), active low. Resistance to VCC when not in use (pull-up).
Pxy (x=A to D, H y=0-15)	General pin. When used as an input function, the input voltage should not exceed VCC. When used as an analog input, the analog voltage should not exceed VREFH/AVCC. When not in use, leave floating or connect a resistor to VCC (pull-up) or VSS (pull-down).

4 Electrical Specifications

4.1 Parameter Conditions

Unless otherwise specified, all voltages are based on VSS.

4.1.1 Minimum and Maximum Values

All Minimum Values and Maximum Values are measured under the worst conditions.

Data resulted from comprehensive evaluation, and/or guaranteed by design are indicated in the table footnotes, and they will not be tested on the production line.

4.1.2 Typical Values

Unless otherwise specified, typical data are given based on T_A=25℃ and VCC=5.0V. These data are only used for design guidance and have not been tested.

4.1.3 Typical Curve

Unless otherwise specified, all typical curves are untested and are for design reference only.

4.1.4 Load Capacitance

The left of Figure 4-1 : Pin Load Condition (Left) and Input Voltage Measurement (Right) displays the load conditions used to measure the pin parameters.

4.1.5 Pin Input Voltage

The right of Figure 4-1 : Pin Load Condition (Left) and Input Voltage Measurement (Right) displays the measurement method of the input voltage on the device pin.

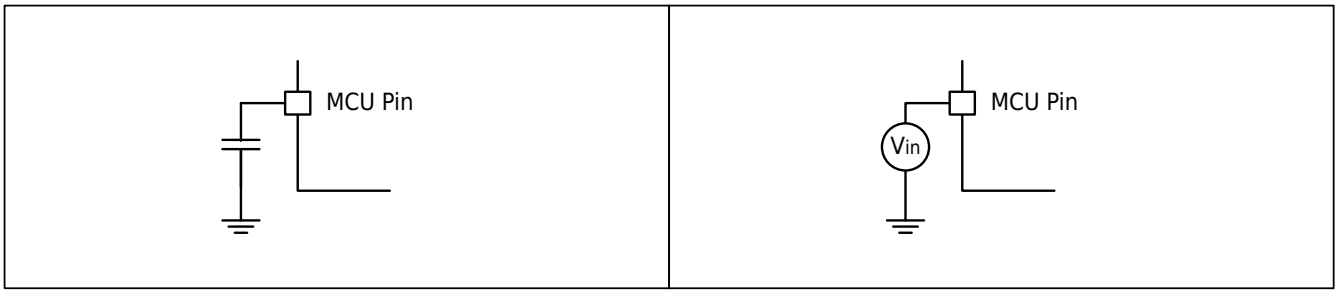


Figure 4-1 Pin Load Condition (Left) and Input Voltage Measurement (Right)

4.1.6 Power Scheme

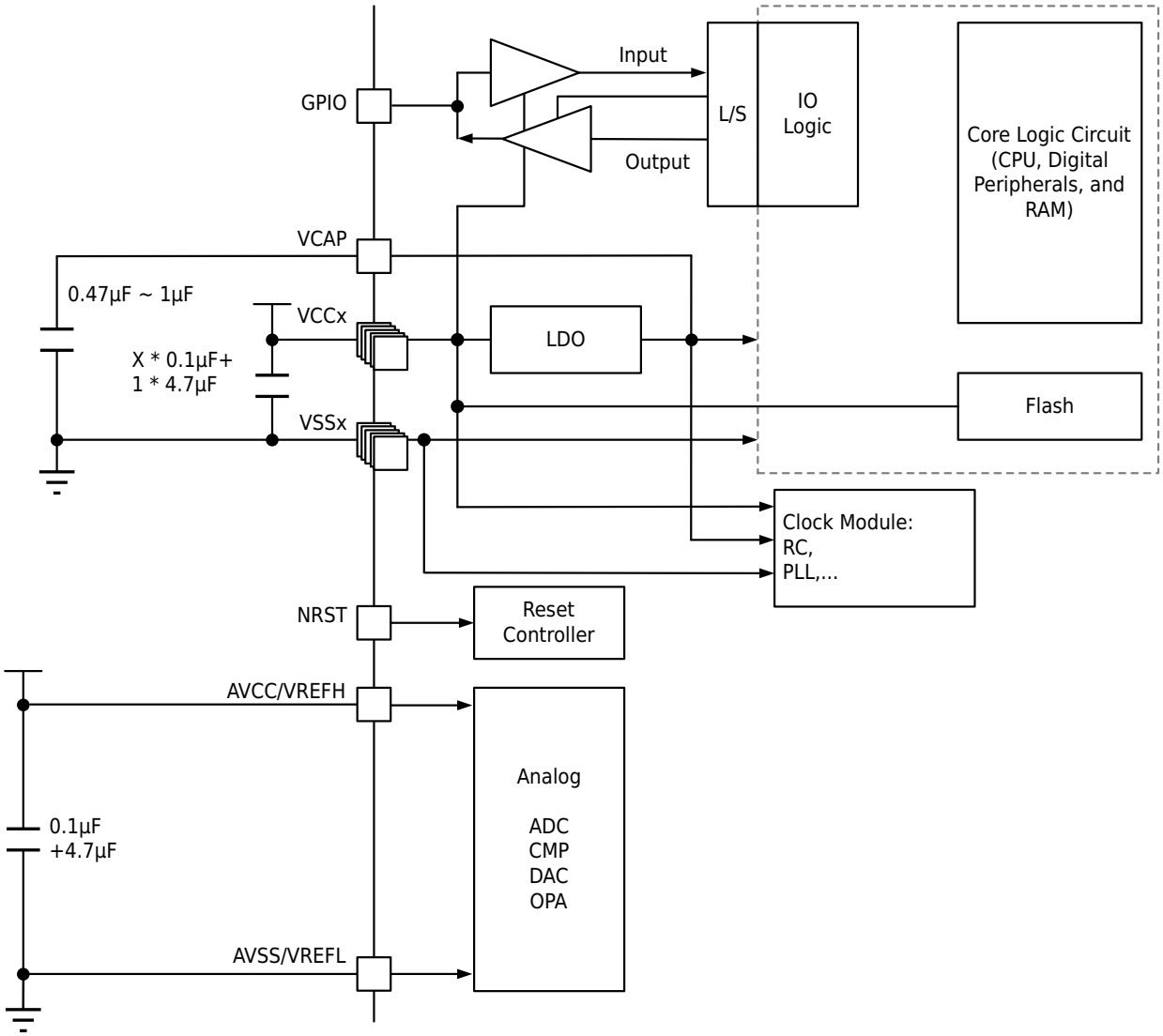


Figure 4-2 Power Scheme

Note

1. 4.7μF ceramic capacitor must be connected to one of VCC pins.
2. AVSS=VSS.
3. Each power supply pair (e.g. VCC/VSS, AVCC/AVSS...) must be decoupled with the above-mentioned filter ceramic capacitors. These capacitors must be as close as possible to or below that of the appropriate pins under the PCB to ensure the normal operation of the device. It is not recommended to remove the filter capacitor to reduce the size or cost of PCB, which may lead to abnormal operation of the device.

4.1.7 Current Consumption Measurement

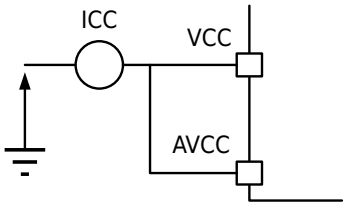


Figure 4-3 Current Consumption Measurement Solution

4.2 Absolute Maximum Ratings

Loads applied to the device that exceed the values listed in the Absolute Maximum Ratings list may cause permanent damage to the device. Here are only the maximum loads that the device can withstand. It is not implied that the functional operation of the device in such conditions is incorrect. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1 Voltage and Current Characteristics

Symbol	Description	Min	Max	Unit
V_{CC}-V_{SS}	External main power voltage (including AVCC, VCC)(1)	-0.3	5.8	V
V_{IN}	Input voltage of other pins(2)	0.3	V_{CC}+0.3	V
|VSSx-VSS|	Voltage difference between different ground pins	-	50	mV
$\sum I_{VCC}$	Total current flowing into all VCC_X power wires (pull current) (1)	-	100	mA
$\sum I_{VSS}$	Total current flowing out all VSS_X ground wires (sink current) (1)	-	-100	mA
I_{VCC}	Maximum current flowing into each VCC_X power wire (pull current)(1)	-	60	mA
I_{VSS}	Maximum current flowing out each VSS_X ground wire (sink current)(1)	-	-60	mA
I_{IO}	Output sink current on any I/O and control pins	-	20	mA
	Output pull current on any I/O and control pins	-	-20	mA
$\sum I_{IO}$	Total output sink current on all I/O and control pins(3)	-	60	mA
	Total output pull current on all I/O and control pins(3)	-	-60	mA

Note

1. Within the permissible range, all main power supply pins (VCC, AVCC) and ground pins (VSS, AVSS) must always be connected to external power sources, and they must be powered on simultaneously. Otherwise, normal operation of the chip cannot be guaranteed.
2. The maximum value for V_{IN} must always be conformed.
3. This total output current must be properly distributed across all power domains. The total output current must not be sinked/pulled between two consecutive power pins.

Table 4-2 Temperature Characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage Temperature Range	-65-+150	℃
T_{Jmax}	Maximum Junction Temperature	125	℃

4.3 Operating Conditions

4.3.1 General Operating Conditions

Table 4-3 General Operating Conditions

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	-	200	MHz
V_{CC}(1)	Standard operating voltage	-	2.7	-	5.5	V
V_{AVCC}(1)	Analog operating voltage	-	2.7	-	5.5	V
T_J(1)	Junction temperature range	-	-40	-	125	℃
T_A(1)	Operating temperature range	-	-40	-	105	℃

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.2 Working Conditions at Power On and Power Down

Table 4-4 Working Conditions at Power On and Power Down

Symbol	Parameters	Conditions	Min	Max	Unit
t_{VCC}(1)(2)	VCC rise time rate	-	20	20000	μs/V
	VCC fall time rate	BORDIS=0b1	20	20000	
		BORDIS=0b0	20	-	

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. VCC and AVCC must be powered on and off simulataneously.

4.3.3 Reset and Power Control Module Characteristics

Table 4-5 Reset and Power Control Module Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{BOR}(1)	BOR monitoring voltage(3)	ICG1.BOR_LEV=0b01	2.65	2.80	2.95	V
		ICG1.BOR_LEV=0b10	3.40	3.55	3.70	V
		ICG1.BOR_LEV=0b11	3.70	3.85	4.00	V
V_{PVD1}(1)	PVD1 monitoring voltage(3)	PVD1LVL=0b0010	2.65	2.80	2.95	V
		PVD1LVL=0b0011	2.80	2.95	3.10	V
		PVD1LVL=0b0100	2.95	3.10	3.25	V
		PVD1LVL=0b0101	3.10	3.25	3.40	V
		PVD1LVL=0b0110	3.25	3.40	3.55	V
		PVD1LVL=0b0111	3.40	3.55	3.70	V
		PVD1LVL=0b1000	3.55	3.70	3.85	V

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{PVD1}[1]	PVD1 monitoring voltage[3]	PVD1LVL=0b1001	3.70	3.85	4.00	V
		PVD1LVL=0b1010	3.85	4.00	4.15	V
		PVD1LVL=0b1011	4.00	4.15	4.30	V
		PVD1LVL=0b1100	4.15	4.30	4.45	V
		PVD1LVL=0b1101	4.30	4.45	4.60	V
		PVD1LVL=0b1110	4.45	4.60	4.75	V
		PVD1LVL=0b1111	4.60	4.75	4.90	V
V_{PVD2}[1]	PVD2 monitoring voltage[3][5]	PVD2LVL=0b0010	2.65	2.80	2.95	V
		PVD2LVL=0b0011	2.80	2.95	3.10	V
		PVD2LVL=0b0100	2.95	3.10	3.25	V
		PVD2LVL=0b0101	3.10	3.25	3.40	V
		PVD2LVL=0b0110	3.25	3.40	3.55	V
		PVD2LVL=0b0111	3.40	3.55	3.70	V
		PVD2LVL=0b1000	3.55	3.70	3.85	V
		PVD2LVL=0b1001	3.70	3.85	4.00	V
		PVD2LVL=0b1010	3.85	4.00	4.15	V
		PVD2LVL=0b1011	4.00	4.15	4.30	V
		PVD2LVL=0b1100	4.15	4.30	4.45	V
		PVD2LVL=0b1101	4.30	4.45	4.60	V
		PVD2LVL=0b1110	4.45	4.60	4.75	V
		PVD2LVL=0b1111	4.60	4.75	4.90	V
$V_{BOR}hyst$[1]	BOR hysteresis[4]	-	-	60	-	mV
$V_{PVD}hyst$[1]	PVD1/2 hysteresis[4]	-	-	60	-	mV
V_{POR}	Power-on reset threshold	Rising edge VPOR	2.37	2.55	2.68	V
		Falling edge VPDR	2.32	2.50	2.63	V
I_{RUSH}[1]	Regulator inrush current at power-on (POR)	-	-	100	150	mA
T_{NRST}[1]	NRST reset minimum pulse width	-	10	-	-	µs
T_{PVDST}[2]	PVD startup time	-	-	-	50	µs
T_{IPVD1}[2]	PVD1 reset removal time	-	-	380	-	µs
T_{IPVD2}[2]	PVD2 reset removal time	-	-	380	-	µs
T_{INRST}[2]	NRST reset removal time	-	-	380	-	µs
T_{RIPT}[2]	Internal reset time	-	-	380	-	µs
T_{RSTBOR}[2]	BOR reset removal time	-	-	380	-	µs
T_{RSTPOR}[2]	Power-on reset removal time	-	-	2500	3000	µs

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. The BOR monitoring voltage is the monitoring voltage when the VCC voltage is falling; the PVD1 monitoring voltage is the monitoring voltage when the VCC voltage is falling; the PVD2 monitoring voltage is the monitoring voltage when the VCC voltage is falling or when the PVD2EXINP voltage is falling.
4. The hysteresis for BOR and PVD1/2 is the difference between the monitoring voltage when VCC or PVD2EXINP is rising and the monitoring voltage when it is falling.

   BOR monitoring voltage when VCC is rising = V_{BOR} + V_{BOR}hyst;

   PVD1 monitoring voltage when VCC is rising = V_{PVD1} + V_{PVD}hyst;

   PVD2 monitoring voltage when VCC or PVD2EXINP is rising = V_{PVD2} + V_{PVD}hyst.
5. PVD2 supports external voltage PVD2EXINP monitoring function, and the PVD2EXINP voltage must be less than the chip supply voltage.

4.3.4 Supply Current Characteristics

Current consumption is affected by many parameters and factors, including operating voltage, ambient temperature, I/O pin load, device software configuration, operating frequency, I/O pin switching rate, program location in memory and running code.

Figure 4-3 : Current Consumption Measurement Solution describes the measurement method of current consumption. The measured values of current consumption in various modes described in this section are obtained by a set of test codes running in FLASH under laboratory conditions.

The specific conditions are as follows:

1. All I/O pins are in high impedance mode (no load).
2. Clock frequencies selected are f_{HCLK}=200MHz, 25MHz, and 8MHz.
3. Power modes are categorized as: Normal Operating Mode ICC_RUN, Sleep Mode ICC_SLEEP, Stop Mode ICC_STP, and Dhrystone Operating Mode ICC_DHRYSTONE.
4. Please refer to the specific current condition description for peripheral clock ON/OFF.
5. The PLL is enabled at f_{HCLK}=200MHz.

Table 4-6 f_{HCLK}=200MHz Current Consumption(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=200MHz T_A=-40℃ V_{CC}=5.0V	-	17.3	-	mA
	While (1), all peripherals clock ON		-	26.7	-	mA
ICC_DHRYSTONE	CACHE OFF		-	26.6	-	mA
	CACHE ON		-	33.1	-	mA
ICC_SLEEP	All peripherals clock OFF		-	9.4	-	mA
	All peripherals clock ON		-	18.8	-	mA

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=200MHz T_A=25℃ V_{CC}=5.0V	-	17.6	-	mA
	While (1), all peripherals clock ON		-	27.1	-	mA
ICC_DHRYSTONE	CACHE OFF		-	27.2	-	mA
	CACHE ON		-	33.7	-	mA
ICC_SLEEP	All peripherals clock OFF		-	9.6	-	mA
	All peripherals clock ON		-	19.2	-	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=200MHz T_A=85℃ V_{CC}=2.7-5.5V	-	-	28.7	mA
	While (1), all peripherals clock ON		-	-	40.0	mA
ICC_DHRYSTONE	CACHE OFF		-	-	40.0	mA
	CACHE ON		-	-	48.0	mA
ICC_SLEEP	All peripherals clock OFF		-	-	18.9	mA
	All peripherals clock ON		-	-	30.8	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=200MHz T_A=105℃ V_{CC}=2.7-5.5V	-	-	30.0	mA
	While (1), all peripherals clock ON		-	-	41.6	mA
ICC_DHRYSTONE	CACHE OFF		-	-	41.8	mA
	CACHE ON		-	-	49.8	mA
ICC_SLEEP	All peripherals clock OFF		-	-	20.6	mA
	All peripherals clock ON		-	-	32.3	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-7 f_{HCLK}=25MHz Current Consumption(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=25MHz T_A=-40℃ V_{CC}=5.0V	-	3.3	-	mA
	While (1), all peripherals clock ON		-	5.4	-	mA
ICC_DHRYSTONE	CACHE OFF		-	5.6	-	mA
ICC_SLEEP	All peripherals clock OFF		-	2.2	-	mA
	All peripherals clock ON		-	4.3	-	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=25MHz T_A=25℃ V_{CC}=5.0V	-	3.4	-	mA
	While (1), all peripherals clock ON		-	5.6	-	mA
ICC_DHRYSTONE	CACHE OFF		-	5.9	-	mA
ICC_SLEEP	All peripherals clock OFF		-	2.3	-	mA
	All peripherals clock ON		-	4.5	-	mA

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=25MHz T_A=85℃ V_{CC}=2.7-5.5V	-	-	11.6	mA
	While (1), all peripherals clock ON		-	-	14.3	mA
ICC_DHRYSTONE	CACHE OFF		-	-	14.8	mA
ICC_SLEEP	All peripherals clock OFF		-	-	9.7	mA
	All peripherals clock ON		-	-	12.9	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=25MHz T_A=105℃ V_{CC}=2.7-5.5V	-	-	13.2	mA
	While (1), all peripherals clock ON		-	-	16.1	mA
ICC_DHRYSTONE	CACHE OFF		-	-	16.5	mA
ICC_SLEEP	All peripherals clock OFF		-	-	11.9	mA
	All peripherals clock ON		-	-	14.8	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-8 f_{HCLK}=8MHz Current Consumption

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=8MHz T_A=-40℃ V_{CC}=5.0V	-	1.7	-	mA
	While (1), all peripherals clock ON		-	2.8	-	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	2.8	-	mA
ICC_SLEEP	All peripherals clock OFF		-	1.4	-	mA
	All peripherals clock ON		-	2.4	-	mA
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=8MHz T_A=25℃ V_{CC}=5.0V	-	1.8	-	mA
	While (1), all peripherals clock ON		-	3.0	-	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	3.0	-	mA
ICC_SLEEP	All peripherals clock OFF		-	1.5	-	mA
	All peripherals clock ON		-	2.6	-	mA
ICC_RUN(1)	While (1), all peripherals clock OFF	f_{HCLK}=8MHz T_A=85℃ V_{CC}=2.7-5.5V	-	-	8.9	mA
	While (1), all peripherals clock ON		-	-	10.5	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	-	10.6	mA
ICC_SLEEP(1)	All peripherals clock OFF		-	-	7.8	mA
	All peripherals clock ON		-	-	10	mA

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_RUN	While (1), all peripherals clock OFF	f_{HCLK}=8MHz T_A=105℃ V_{CC}=2.7-5.5V	-	-	11.3	mA
	While (1), all peripherals clock ON		-	-	12.9	mA
ICC_DHRY-STONE(1)	CACHE OFF		-	-	13.0	mA
ICC_SLEEP	All peripherals clock OFF		-	-	10.8	mA
	All peripherals clock ON		-	-	12.5	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-9 Low Power Mode Current Consumption(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_STP (Stop Mode)	-	T_A=-40℃ V_{CC}=5.0V	-	88	-	μA
	-	T_A=25℃ V_{CC}=5.0V	-	160	-	μA
	-	T_A=85℃ V_{CC}=2.7-5.5V	-	-	4.9	mA
	-	T_A=105℃ V_{CC}=2.7-5.5V	-	-	9.0	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-10 Analog Module Current Consumption(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ICC_MODULE	XTAL oscillation mode high drive 24MHz	T_A=25℃ V_{CC}=V_{AVCC}=5.0V	-	1.26	-	mA
	Oscillation mode ultra-low drive 4MHz		-	0.23	-	mA
	HRC		-	0.25	-	mA
	PLL (VCO=480MHz)		-	1.48	-	mA
	ADC		-	1.66	-	mA
	DAC		-	0.19	-	mA
	CMP		-	0.14	-	mA
	OPA		-	1.2	-	mA

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.5 Low Power Mode Wake-up Timing

The wake-up time is measured from the trigger of the wake-up event to the first command executed by the CPU:

- For Stop or Sleep mode: the wake-up event is WFE.

- All timing is measured at ambient temperature and V_{CC}=5.0V.

Table 4-11 Low-power Mode Wake-up Time(1)

Symbol	Parameters	Conditions	Typical	Maximum	Unit
T_{STOP}	Wake-up from Stop mode	The system clock is MRC	123	135	μs

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.6 External Clock Source Characteristics

4.3.6.1 High-Speed External Clock Generated by External Source

In bypass mode, XTAL oscillator is disabled and the input pin is a standard I/O. The external clock signal must consider the static characteristics of the I/O.

Table 4-12 High-Speed External Clock Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{XTAL_EXT}	User external clock source frequency	-	1(1)	-	25	MHz
V_{IH_XTAL}(1)	XTAL_EXT input pin high-level voltage	-	0.7*V_{CC}	-	V_{CC}	V
V_{IL_XTAL}(1)	XTAL_EXT input pin low-level voltage	-	V_{SS}	-	0.3*V_{CC}	V
$t_{r(XTAL)}$(1) $t_{f(XTAL)}$(1)	XTAL_EXT rising or falling time	-	-	-	20	ns
$Duty_{(XTAL)}$(1)	Duty cycle	-	40	-	60	%

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.6.2 High-Speed External Clock Generated by Crystal Oscillator/Ceramic Resonator

The high-speed external (XTAL) clock can be generated by a crystal oscillator/ceramic resonant oscillator with a frequency of 4-25MHz. In application, the resonator and load capacitor must be as close as possible to the pin of oscillator, so as to minimize the output distortion and the stabilization time. For detailed information about resonator characteristics (frequency, package, accuracy, etc.), please consult the crystal resonator manufacturer.

Table 4-13 XTAL 4-25 MHz Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{XTAL_IN}(1)	Oscillator frequency	-	4	-	25	MHz
R_F	Feedback resistance	-	-	0.43	-	MΩ
G_m(2)	G_m of crystal oscillator	XTALDRV=0b00, FREQSEL=0b00	0.234	0.347	0.494	mA/V
		XTALDRV=0b00, FREQSEL=0b01	0.465	0.696	0.992	

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
G_m (2)	G_m of crystal oscillator	XTALDRV=0b00, FREQSEL=0b10	1.295	1.944	2.767	mA/V
		XTALDRV=0b00, FREQSEL=0b11	2.071	3.12	4.445	
		XTALDRV=0b01, FREQSEL=0b00	0.301	0.444	0.63	
		XTALDRV=0b01, FREQSEL=0b01	0.599	0.89	1.264	
		XTALDRV=0b01, FREQSEL=0b10	1.672	2.488	3.527	
		XTALDRV=0b01, FREQSEL=0b11	2.673	3.989	5.661	
		XTALDRV=0b10, FREQSEL=0b00	0.437	0.641	0.906	
		XTALDRV=0b10, FREQSEL=0b01	0.871	1.286	1.819	
		XTALDRV=0b10, FREQSEL=0b10	2.438	3.597	5.079	
		XTALDRV=0b10, FREQSEL=0b11	3.897	5.762	8.147	
		XTALDRV=0b11, FREQSEL=0b00	0.791	1.129	1.57	
		XTALDRV=0b11, FREQSEL=0b01	1.581	2.263	3.148	
		XTALDRV=0b11, FREQSEL=0b10	4.433	6.343	8.81	
		XTALDRV=0b11, FREQSEL=0b11	7.08	10.14	14.1	
$t_{SU(XTAL)}$ (1)(3) (4)	Startup time	V_{CC} stable, crystal=25 MHz	-	2	-	ms
		V_{CC} stable, crystal=4 MHz	-	4	-	ms

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. This parameter depends on the resonator used in the application system.
4. $t_{SU(XTAL)}$ is the oscillation starting time, that is, the time from the software enabling XTAL to the stable oscillation frequency. This value is measured based on a standard crystal resonator, and may vary significantly depending on the crystal oscillator manufacturer.

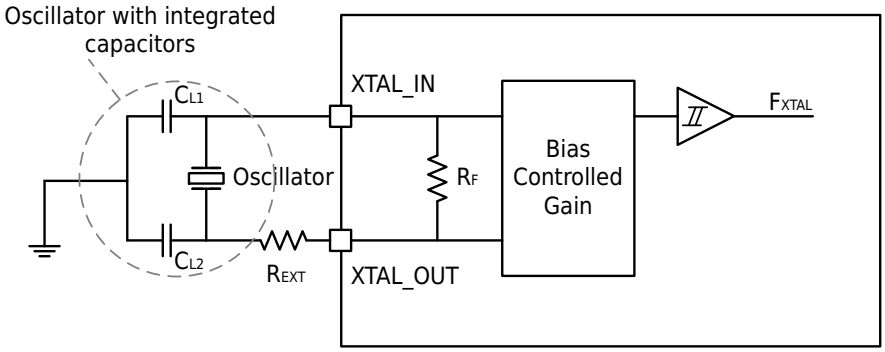


Figure 4-4 Typical Application with an 8 MHz Crystal Oscillator

Note

- For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors designed for high-frequency applications, which can meet the requirements of crystal oscillator or resonator (see the figure above). C_{L1} and C_{L2} usually have the same size. $C_{L1}=C_{L2}=2 \times C_L - C_P$. C_P is the total parasitic capacitance to ground of the PCB and the MCU pins (XTAL_IN, XTAL_OUT). C_L denotes the load capacitance of the crystal oscillator or ceramic resonator, please consult the crystal oscillator manufacturer for details.
- The value of R_{EXT} depends on the crystal oscillation characteristics.

4.3.7 Internal Clock Source Characteristics

4.3.7.1 HRC

Table 4-14 HRC Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{HRC}	Frequency(2)	-	-	12	-	MHz
	Frequency accuracy(1)	T_A=-40-105℃	-1	-	1	%
		T_A=25℃	-0.5	-	0.5	%
$t_{st(HRC)}$(2)	HRC oscillator stabilization time	-	-	8	-	μs

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.

4.3.7.2 MRC

Table 4-15 MRC Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{MRC}	Frequency	-	7.2	8	8.8	MHz
$t_{st(MRC)}$	MRC oscillator stabilization time	-	-	-	15	μs

4.3.7.3 LRC

Table 4-16 LRC Oscillator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{LRC}	Frequency	-	32.1	32.768	33.5	kHz
$t_{st(LRC)}$	LRC oscillator stabilization time	-	-	-	150	μs

4.3.8 PLL Characteristics

Table 4-17 System PLL (PLL) Key Performance Indicators

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}(2)	Input clock of PLL phase detector (PFD)	-	4	-	12.5	MHz

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_{PLL_OUT}(1)	Output clock of PLL multiplier	-	10	-	250	MHz
f_{VCO_OUT}	PLL voltage controlled oscillator (VCO) output	-	320	-	500	MHz
$Jitter_{PLL}$(1)	Periodic jitter	The PLL PFD input clock is 8MHz, and the system clock is 200MHz	-	±300	-	ps
t_{LOCK}(1)	PLL lock time	-	-	80	120	µs

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. It is recommended to use a higher input clock to obtain jittering characteristics.

4.3.9 Memory (Flash) Characteristics

The Flash memory is delivered to the customer in an erased state.

Table 4-18 Flash Characteristics(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
I_{VCC}	Supply Current	Read mode (Code Flash), V_{CC}=2.7-5.5V	-	-	8	mA
		Read mode (Data Flash), V_{CC}=2.7-5.5V	-	-	3	mA
		Programming mode (Code Flash), V_{CC}=2.7-5.5V	-	-	4	mA
		Programming mode (Data Flash), V_{CC}=2.7-5.5V	-	0.8	1.6	mA
		Block erase mode (Code Flash), V_{CC}=2.7-5.5V	-	-	2	mA
		Block erase mode (Data Flash), V_{CC}=2.7-5.5V	-	0.6	1	mA
		Mass erase mode (Code Flash), V_{CC}=2.7-5.5V	-	-	2	mA
		Mass erase mode (Data Flash), V_{CC}=2.7-5.5V	-	0.6	1	mA

Note

1. Guaranteed by design, not tested in production.

Table 4-19 Flash Programming and Erase Time(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
T_{prog}	8-byte Programming Time (Code Flash)	Single programming mode	-	41	-	µs
	8-byte Programming Time (Code Flash)	Continuous programming mode	-	18	-	µs

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
T_{prog}	1-byte Programming Time (Data Flash)	Single programming mode	-	111	-	µs
	1-byte Programming Time (Data Flash)	Continuous programming mode	-	10	-	µs
	2-byte Programming Time (Data Flash)	Single programming mode	-	121	-	µs
	2-byte Programming Time (Data Flash)	Continuous programming mode	-	20	-	µs
T_{erase}	Block Erase Time (Code Flash)	-	-	2.6	-	ms
	Block Erase Time (Data Flash)	-	-	2.6	-	ms
T_{mas}	Mass Erase Time (Code Flash)	-	-	38	-	ms
	Mass Erase Time (Data Flash)	-	-	36	-	ms

Note

1. Guaranteed by design, not tested in production.

Table 4-20 Flash Erase Write Times and Data Storage Period(1)

Symbol	Parameters	Conditions	Min	Typ	Unit
N_{END}	Program, Block Erase Cycles (Code Flash)	T_A=-40℃~105℃	-	100000	Cycles
	Program, Block Erase Cycles (Data Flash)	T_A=-40℃~105℃	-	1000000	Cycles
T_{RET}	Data Storage Period (Code Flash)	20 kcycles at T_A=85℃	10	-	Year
	Data Storage Period (Data Flash)	100 kcycles at T_A=85℃	10	-	Year

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.10 I/O Port Characteristics

General-Purpose Input/Output Characteristics

Table 4-21 I/O Static Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{IL_SCH}	Schmitt Input Low Level	Except NRST pin	-	-	$0.3V_{CC}$	V
		NRST pin	-	-	$0.2V_{CC}$	V
V_{IH_SCH}	Schmitt Input High Level	Except NRST pin	$0.7V_{CC}$	-	-	V
		NRST pin	$0.8V_{CC}$	-	-	V
V_{HYS}(1)	Schmitt Input Hysteresis	-	$0.1V_{CC}$	-	-	V

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{IL_CMOS}	CMOS Input Low Voltage	-	-	-	$0.3V_{CC}$	V
V_{IH_CMOS}	CMOS Input High Voltage	-	$0.7V_{CC}$	-	-	V
V_{IL_TTL}	TTL Input Low Voltage (CMOS Compatible)	$2.7≤V_{CC}≤3.63$	-	-	0.8	V
V_{IH_TTL}	TTL Input High Voltage (CMOS Compatible)	$2.7≤V_{CC}≤3.63$	2.2	-	-	V
I_{LKG}	I/O Input Leakage Current	$V_{SS}≤V_{IN}≤V_{CC}$	-	-	1	μA
R_{PU}	Weak Pull-up Equivalent Resistance	$V_{IN}=V_{SS}$ $2.7≤V_{CC}≤5.5$	20	55	100	kΩ
R_{PD}	Weak Pull-down Equivalent Resistance	$V_{IN}=V_{CC}$ $2.7≤V_{CC}≤5.5$	20	55	100	kΩ
C_{IO}(2)	I/O Pin Capacitance	-	-	5	-	pF

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.

Output Current

The GPIO can provide a maximum source or sink current of ±20mA.

Output Voltage

Table 4-22 Output Voltage Characteristics

Driver	Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Weak Drive DRV=0b0x	V_{OL}(1)	Low level output	I_{IO}=±4mA $2.7≤V_{CC}≤5.5$	-	-	0.55	V
	V_{OH}(2)	High level output		V_{CC}-0.55	-	-	V
	V_{OL}(1)	Low level output	I_{IO}=±8mA $4≤V_{CC}≤5.5$	-	-	0.65	V
	V_{OH}(2)	High level output		V_{CC}-0.65	-	-	V
Strong Drive DRV=0b1x	V_{OL}(1)	Low level output	I_{IO}=±8mA $2.7≤V_{CC}≤5.5$	-	-	0.55	V
	V_{OH}(2)	High level output		V_{CC}-0.55	-	-	V
	V_{OL}(1)	Low level output	I_{IO}=±16mA $4≤V_{CC}≤5.5$	-	-	0.65	V
	V_{OH}(2)	High level output		V_{CC}-0.65	-	-	V
	V_{OL}(1)	Low level output	I_{IO}=±20mA $2.97≤V_{CC}≤5.5$	-	-	1.3	V
	V_{OH}(2)	High level output		V_{CC}-1.3	-	-	V

Note

1. The device's I_{IO} sinking current must always conform to the absolute maximum ratings specified in Table 4-1 : Voltage and Current Characteristics. The sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The device's I_{IO} pull current must always conform to the absolute maximum ratings specified in Table 4-1 : Voltage and Current Characteristics. The total I_{IO} (I/O ports and control pins) must not exceed I_{VCC}.

Output AC Characteristics

Table 4-23 I/O AC Characteristics (Except PA6 and PB1)(1)

Drive Setting	Symbol	Parameters	Conditions(3)	Min	Typ	Max	Unit
DRV=0b00 Weak Drive Slow Slew	$f_{max(IO)out}$(2)	Maximum Frequency	C_L=25pF, V_{CC}≥2.7V	-	-	20	MHz
			C_L=25pF, V_{CC}≥4.5V	-	-	25	MHz
	$t_{f(IO)out}$ $t_{r(IO)out}$(1)	Rise/Fall Time	C_L=25pF, V_{CC}≥2.7V	-	-	16	ns
			C_L=25pF, V_{CC}≥4.5V	-	-	13.3	ns
DRV=0b01 Weak Drive Fast Slew	$f_{max(IO)out}$(2)	Maximum Frequency	C_L=25pF, V_{CC}≥2.7V	-	-	25	MHz
			C_L=25pF, V_{CC}≥4.5V	-	-	30	MHz
	$t_{f(IO)out}$ $t_{r(IO)out}$(1)	Rise/Fall Time	C_L=25pF, V_{CC}≥2.7V	-	-	13.3	ns
			C_L=25pF, V_{CC}≥4.5V	-	-	11.1	ns
DRV=0b10 Strong Drive Slow Slew	$f_{max(IO)out}$(2)	Maximum Frequency	C_L=25pF, V_{CC}≥2.7V	-	-	30	MHz
			C_L=25pF, V_{CC}≥4.5V	-	-	50	MHz
	$t_{f(IO)out}$ $t_{r(IO)out}$(1)	Rise/Fall Time	C_L=25pF, V_{CC}≥2.7V	-	-	8.3	ns
			C_L=25pF, V_{CC}≥4.5V	-	-	6.6	ns
DRV=0b11 Strong Drive Fast Slew	$f_{max(IO)out}$(2)	Maximum Frequency	C_L=25pF, V_{CC}≥2.7V	-	-	50	MHz
	$t_{f(IO)out}$ $t_{r(IO)out}$(1)	Rise/Fall Time	C_L=25pF, V_{CC}≥2.7V	-	-	6.6	ns

Table 4-24 I/O AC Characteristics (PA6 and PB1)(1)

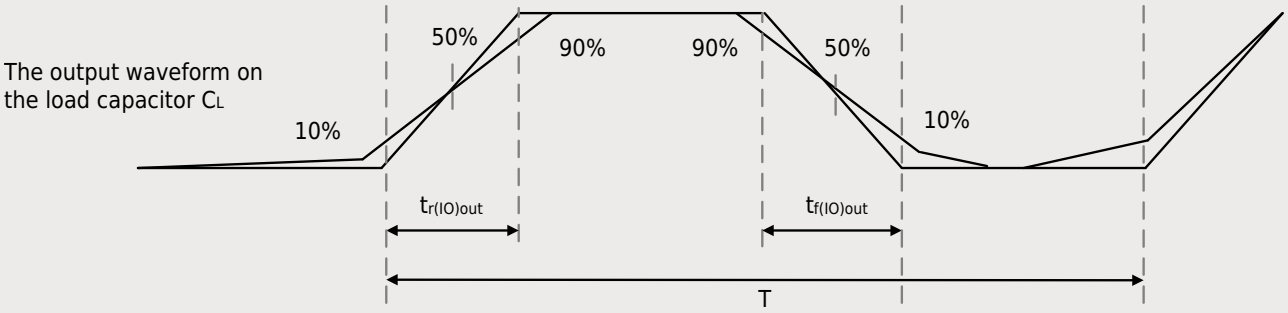
Drive Setting	Symbol	Parameters	Conditions(3)	Min	Typ	Max	Unit
DRV=0b0x Weak Drive	$f_{max(IO)out}$(2)	Maximum Frequency	C_L=25pF, V_{CC}≥2.7V $t_{f(IO)}/t_{r(IO)}$=(10%~90%)*V_{CC}	-	-	10	MHz
			C_L=25pF, V_{CC}≥2.7V $t_{f(IO)}/t_{r(IO)}$=(20%~80%)*V_{CC}	-	-	15	MHz
	$t_{f(IO)out}$ $t_{r(IO)out}$(1)	Rise/Fall Time	C_L=25pF, V_{CC}≥2.7V $t_{f(IO)}/t_{r(IO)}$=(10%~90%)*V_{CC}	-	-	33	ns
			C_L=25pF, V_{CC}≥2.7V $t_{f(IO)}/t_{r(IO)}$=(20%~80%)*V_{CC}	-	-	22	ns

Drive Setting	Symbol	Parameters	Conditions(3)	Min	Typ	Max	Unit
DRV=0b10 Strong Drive Slow Slew	$f_{max(IO)out}$(2)	Maximum Frequency	C_L=25pF, V_{CC}≥2.7V $t_{f(IO)}/t_{r(IO)}$=(10%~90%)*V_{CC}	-	-	15	MHz
			C_L=25pF, V_{CC}≥2.7V $t_{f(IO)}/t_{r(IO)}$=(20%~80%)*V_{CC}	-	-	30	MHz
	$t_{f(IO)out}$ $t_{r(IO)out}$(1)	Rise/Fall Time	C_L=25pF, V_{CC}≥2.7V $t_{f(IO)}/t_{r(IO)}$=(10%~90%)*V_{CC}	-	-	22	ns
			C_L=25pF, V_{CC}≥2.7V $t_{f(IO)}/t_{r(IO)}$=(20%~80%)*V_{CC}	-	-	8.3	ns
DRV=0b11 Strong Drive Fast Slew	$f_{max(IO)out}$(2)	Maximum Frequency	C_L=25pF, V_{CC}≥2.7V $t_{f(IO)}/t_{r(IO)}$=(10%~90%)*V_{CC}	-	-	15	MHz
			C_L=25pF, V_{CC}≥2.7V $t_{f(IO)}/t_{r(IO)}$=(20%~80%)*V_{CC}	-	-	50	MHz
	$t_{f(IO)out}$ $t_{r(IO)out}$(1)	Rise/Fall Time	C_L=25pF, V_{CC}≥2.7V $t_{f(IO)}/t_{r(IO)}$=(10%~90%)*V_{CC}	-	-	22	ns
			C_L=25pF, V_{CC}≥2.7V $t_{f(IO)}/t_{r(IO)}$=(20%~80%)*V_{CC}	-	-	6.6	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production. The maximum frequency is defined in the figure below.
3. The load capacitance C_L must take into account the capacitance of the PCB and the MCU pins (the pin-to-board capacitance can be roughly estimated as 10pF).

Figure 4-5 I/O AC Characteristics Definition



Maximum frequency condition (t_r + t_f) ≤ (2/3)T and Duty cycle= 50% ± 5%
C_L is indicated in the "Conditions" column of the "I/O AC Characteristics" table)

4.3.11 I2C Interface Characteristics

Table 4-25 I2C Electrical Specifications

Symbol	Parameter	Standard Mode (SM)		Fast Mode (FM)		Unit
		Min	Max	Min	Max	
f_{SCL}(1)	SCL Frequency	0	100	0	400	kHz
$t_{HD;STA}$(1)	START Condition/Repeated START Condition Hold	4.0	-	0.6	-	μs
t_{LOW}(1)	SCL Low Level	4.7	-	1.3	-	μs
t_{HIGH}(1)	SCL High Level	4	-	0.6	-	μs
$t_{SU;STA}$(1)	Repeated Start Condition Setup	4.7	-	0.6	-	μs
$t_{HD;DAT}$	Data Hold	0	-	0	-	μs
$t_{SU;DAT}$	Data Setup	$30+t_{I2C\_REFCLK}$(2)	-	$30+t_{I2C\_REFCLK}$(2)	-	ns
t_R(1)	SCL/SDA Rising Time	-	1000	-	300	ns
t_F(1)	SCL/SDA Falling Time	-	300	-	300	ns
$t_{SU;STO}$(1)	STOP Condition Setup	4	-	0.6	-	μs
t_{BUF}(1)	Bus Free Time between STOP and START Conditions	4.7	-	1.3	-	μs
t_{SP}	Pulse Width of Spikes which must be Suppressed	-	-	0	Input filter(3)	ns
C_b(1)	Load Capacitance	-	400	-	400	pF

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. The t_{I2C_REFCLK}, i.e., the I2C reference clock period, is determined by the I2C_CCR.FREQ bit.
3. Spikes on the bus must be suppressed by the input filter, and the filtering capability is set by I2C_FLTR.

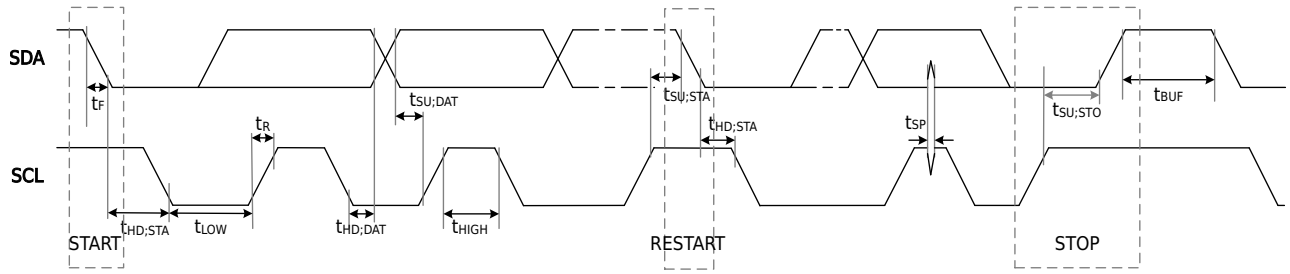


Figure 4-7 I2C Bus Timing Definition

4.3.12 SPI Interface Characteristics

Table 4-26 SPI Electrical Specifications

Symbol	Parameters	Conditions	Min	Max	Unit
t_w(SCKH)(1)	SCK high-level time	Master mode(4)	T_{PCLK1}-1(5)	T_{PCLK1}+1(5)	ns
		Slave mode(4)	3*T_{PCLK1}-1(5)	3*T_{PCLK1}+1(5)	ns
t_w(SCKL)(1)	SCK low-level time	Master mode(4)	T_{PCLK1}-1(5)	T_{PCLK1}+1(5)	ns
		Slave mode(4)	3*T_{PCLK1}-1(5)	3*T_{PCLK1}+1(5)	ns
t_{su}(SI)	Data input setup time	Slave mode	4	-	ns
t_h(SI)	Data input hold time	Slave mode	3	-	ns
t_v(SO)	Data output valid time	Slave mode	-	26	ns
t_{su}(MI)	Data input setup time	Master mode	9	-	ns
t_h(MI)	Data input hold time	Master mode	T_{PCLK1}(5)	-	ns
t_{su}(SS)(1)	SS setup time	Slave mode	6*T_{PCLK1}(5)	-	ns
		Master mode	-10+N*T_{SCK}(2)(5)	-	ns
t_h(SS)(1)	SS hold time	Slave mode	6*T_{PCLK1}(5)	-	ns
		Master mode	-10+N*T_{SCK}(3)(5)	-	ns
t_v(MO)	Data output valid time	Master mode	-	9	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. N=1-8, determined by register SPI_CFG1.MSSI.
3. N=1-8, determined by register SPI_CFG1.MSSDL.
4. The values of t_w(SCKH) and t_w(SCKL) are determined by SPI_CFG2.MBR. The values listed in the table are for SPI_CFG2.MBR=0.
5. T_{PCLK1} refers to 1 period of clock PCLK1, and T_{SCK} refers to 1 period of SPI communication clock.

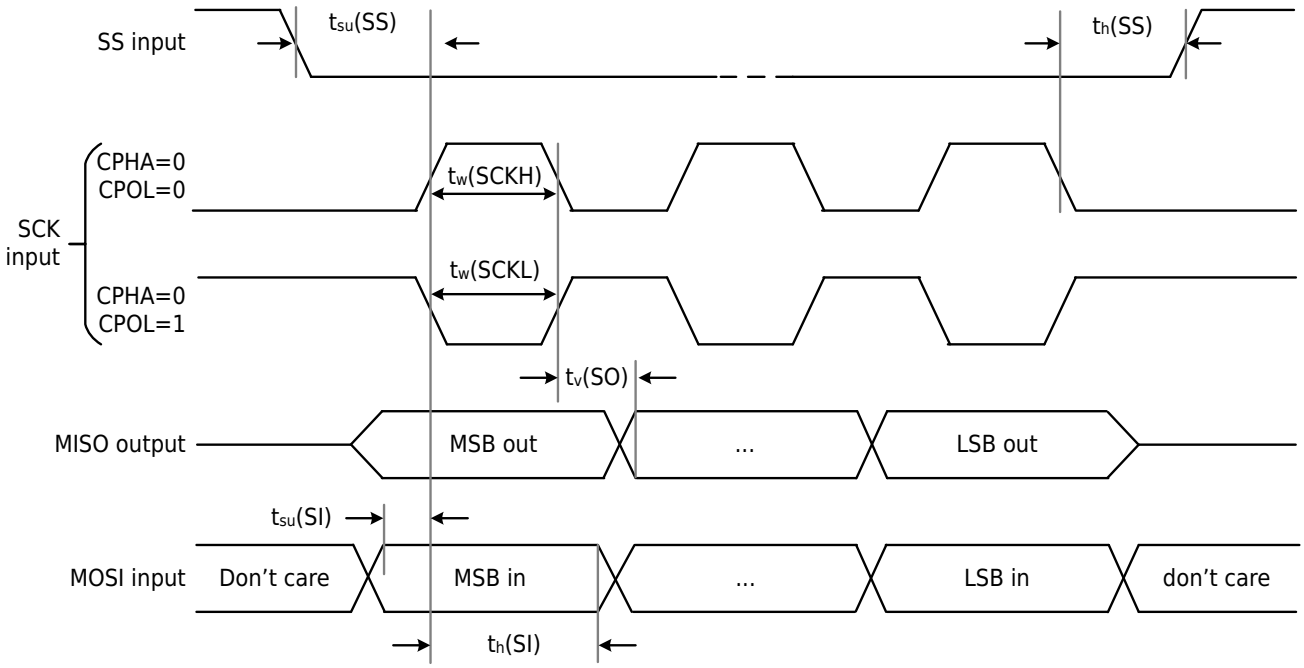


Figure 4-8 SPI Timing Definition (Slave mode, CPHA=0)

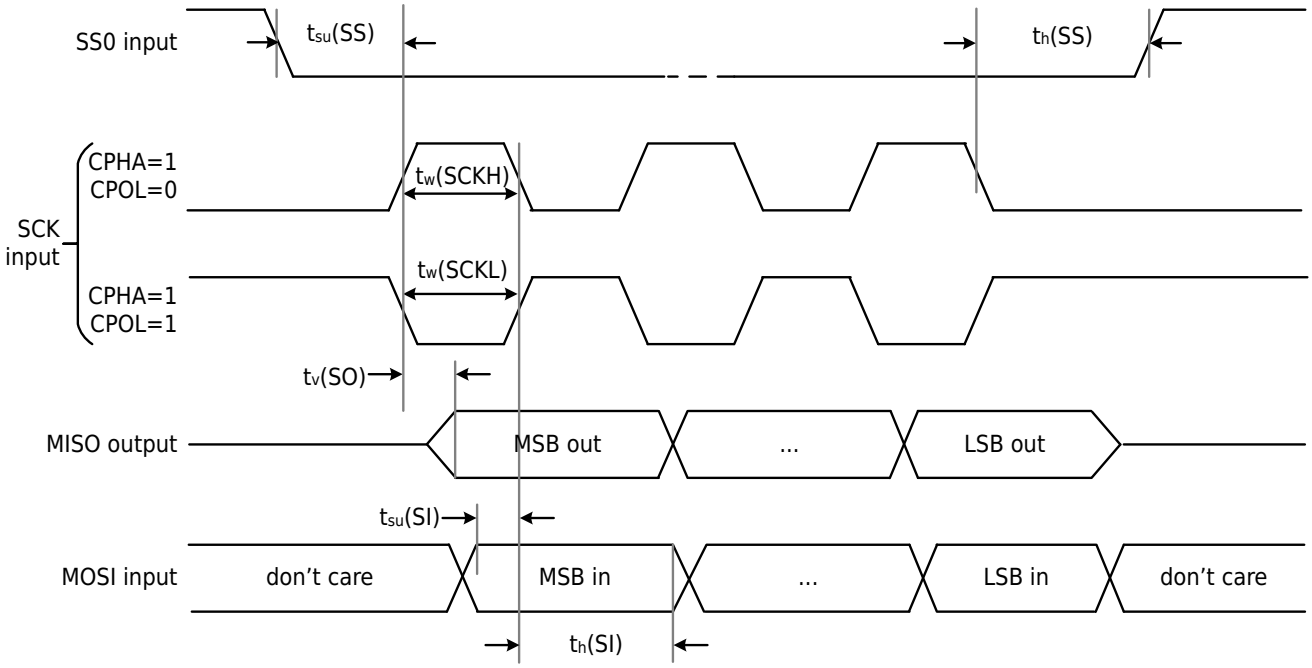


Figure 4-9 SPI Timing Definition (Slave mode, CPHA=1)

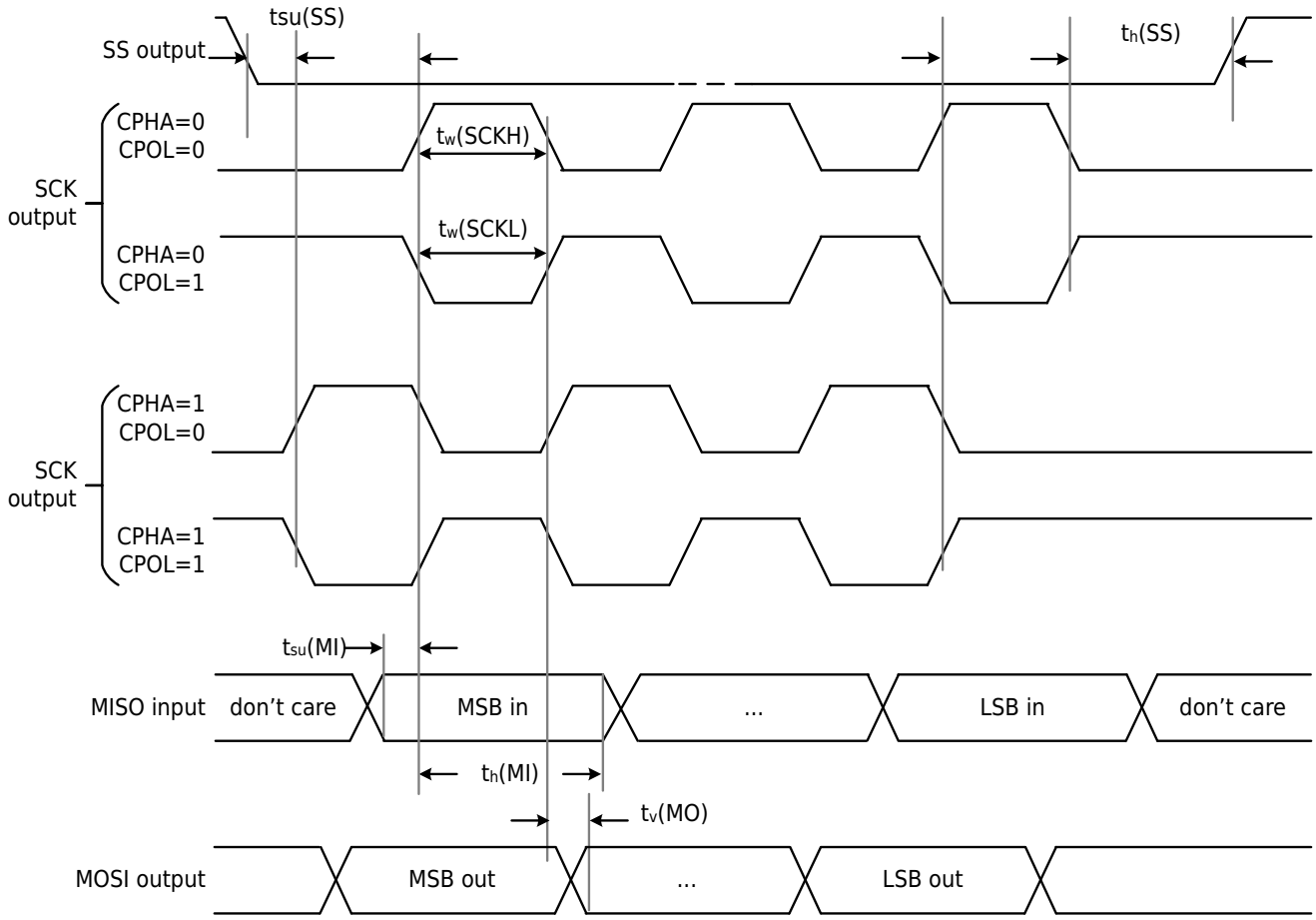


Figure 4-10 SPI Timing Definition (Master mode)

4.3.13 USART Interface Characteristics

Table 4-27 USART AC Timing[1]

Symbol	Parameters	Conditions	Min	Max	Unit
t_{cyc}	Input clock cycles	UART	4	-	t_{PCLK1}
		Clock Synchronization Mode	6	-	
t_{CKw}	Input clock width	-	0.4	0.6	t_{cyc}
t_{CKr}	Input clock rise time	-	-	5	ns
t_{CKf}	Input clock fall time	-	-	5	ns
t_{TD}	Transmimission delay time	Clock Synchronization Mode	-	30	ns
t_{RDS}	Received data setup time	Clock Synchronization Mode	17	-	ns
t_{RDH}	Received data hold time	Clock Synchronization Mode	5	-	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-28 USART Maximum Baud Rate

Mode		Max Baud Rate
UART	Internal clock source	PCLK1/8
	External clock source	PCLK1/32
Clock sync mode		8.0 Mbps

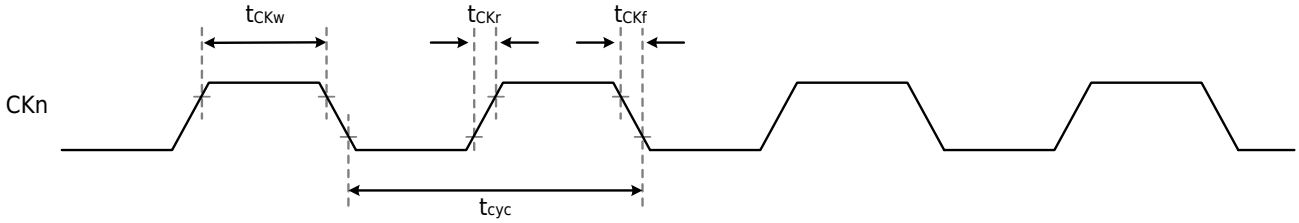


Figure 4-11 USART Clock Timing

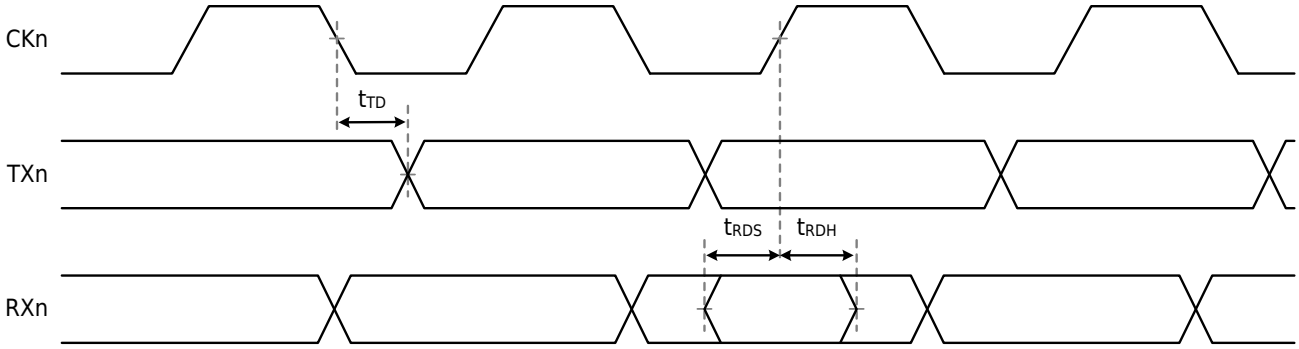


Figure 4-12 USART (CSI) Input/Output Timing

Note

The value of n in the diagram ranges from 1 to 4.

4.3.14 SWD Interface Characteristics

Table 4-29 SWD Interface Characteristics

Symbol	Parameters	Min	Typ	Max	Unit
$t_{SWCLKcyc}$ (1)	SWCLK clock cycle	50	-	-	ns
t_{SWCLKH} (1)	SWCLK clock high level	15	-	-	ns
t_{SWCLKL} (1)	SWCLK clock low level	15	-	-	ns
t_{SWCLKr} (1)	SWCLK clock rise time	-	-	5	ns
t_{SWCLKf} (1)	SWCLK clock fall time	-	-	5	ns
t_{SWDIs}	SWDI setup time	10	-	-	ns
t_{SWDIh}	SWDI hold time	10	-	-	ns
t_{SWDOd}	SWDO data delay	-	-	28	ns

Note

1. Resulted from comprehensive evaluation, not tested in production.

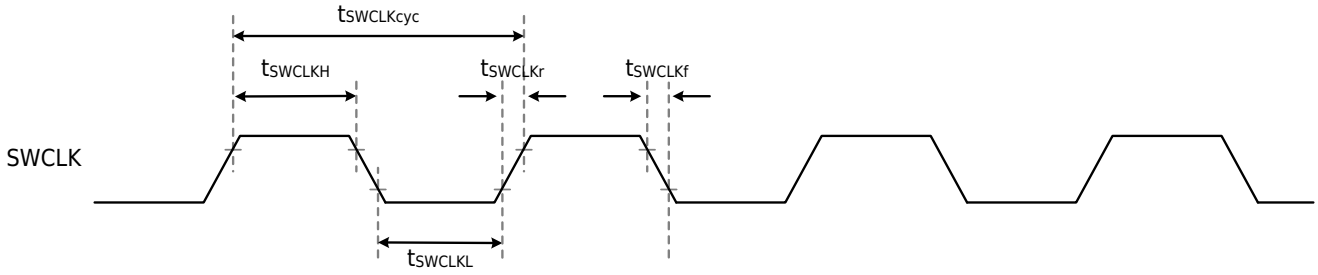


Figure 4-13 SWCLK Clock

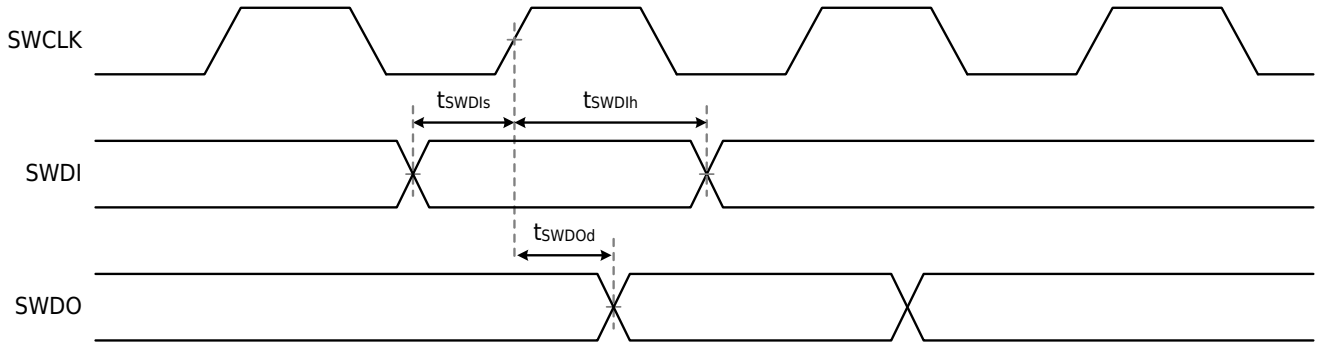


Figure 4-14 SWDIO Input/Output

4.3.15 12-bit ADC Characteristics

Table 4-30 ADC Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{AVCC/VREFH}$ (2)	Power Supply	-	2.7	-	5.5	V
f_{ADC} (2)	ADC Conversion Clock Frequency	4.5V≤V_{AVCC}≤5.5V	-	-	80	MHz
		2.7V≤V_{AVCC}<4.5V	-	-	67	MHz
V_{AIN} (2)	Conversion Voltage Range	-	V_{AVSS}	-	$V_{AVCC/VREFH}$	V
R_{AIN} (1)	External Input Impedance	-	-	-	50	kΩ
R_{ADC} (1)	Sampling Switch Resistance	-	-	1.5	-	kΩ
C_{ADC} (1)	Internal Sample and Hold Capacitance	-	-	5.1	-	pF
t_S (1)	Sampling Time	f_{ADC}=67MHz	12	-	255	1/f_{ADC}
		f_{ADC}=80MHz	18	-	255	1/f_{ADC}
t_{CONV} (1)	Single Channel Total Conversion Time (Includes sampling time, calculated as: Sampling Time Ts + 14)	f_{ADC}=80MHz	0.400	-	-	µs
			32	-	269	1/f_{ADC}
		f_{ADC}=67MHz	0.400	-	-	µs
			26	-	269	1/f_{ADC}

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
f_S(1)	Sampling Rate	f_{ADC}=80MHz	-	-	2.5	Msps
		f_{ADC}=67MHz	-	-	2.5	Msps
t_{ST}(1)	Startup Time	-	-	-	5	μs

Note

1. Guaranteed by design, not tested in production.
2. Resulted from comprehensive evaluation, not tested in production.

Formula 1: RAIN Maximum Value Formula

$$R_{AIN} = \frac{k}{f_{ADC} * C_{ADC} * \ln\left(2^{N+2}\right)} - R_{ADC}$$

The above formula (Formula 1) is used to determine the maximum external impedance that makes the error less than 1/4LSB. Where, N=12 (12-bit resolution), and k is the number of sampling periods defined in the ADC_SSTR register.

Table 4-31 Input Channel Static Accuracy @ f_{ADC}=80MHz(1)

Symbol	Parameters	Conditions	Min	Max	Unit
E_T	Total Unadjustable Error	f_{ADC}=80MHz VREFH as reference V_{AVCC}=4.5V/5.5V T_A=-40℃/125℃	-10	10	LSB
E_O	Offset Error		-8	8	LSB
E_G	Gain Error		-10	10	LSB
E_D	Differential Nonlinearity Error		-1	3	LSB
E_L	Integral Nonlinearity Error		-4	4	LSB

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-32 Output Channel Dynamic Accuracy @ f_{ADC}=80MHz(1)

Symbol	Parameters	Conditions	Min	Max	Unit
ENOB	Effective Number of Bits	f_{ADC}=80MHz Input signal frequency=2kHz Input source impedance=0Ω V_{AVCC}=4.5V/5.5V T_A=-40℃/125℃	10	-	Bits
SINAD	Signal-to-noise and Distortion Ratio		63.4	-	dB
SNR	Signal-to-noise Ratio		64	-	dB
THD	Total Harmonic Distortion		-	-70	dB

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-33 Input Channel Static Accuracy@f_{ADC}=67MHz(1)

Symbol	Parameters	Conditions	Min	Max	Unit
E_T	Total Unadjustable Error	f_{ADC}=67MHz VREFH for reference V_{AVCC}=2.7V/5.5V T_A=-40℃/125℃	-10	10	LSB
E_O	Offset Error		-8	8	LSB
E_G	Gain Error		-10	10	LSB
E_D	Differential Nonlinearity Error		-1	3	LSB
E_L	Integral Nonlinearity Error		-4	4	LSB

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 4-34 Input Channel Dynamic Accuracy @ f_{ADC}=67MHz(1)

Symbol	Parameters	Conditions	Min	Max	Unit
ENOB	Effective Number of Bits	f_{ADC}=67MHz Input signal frequency=2kHz Input source impedance=0Ω V_{AVCC}=2.7V/5.5V T_A=-40℃/125℃	10	-	Bits
SINAD	Signal-to-noise and Distortion Ratio		63.4	-	dB
SNR	Signal-to-noise Ratio		64	-	dB
THD	Total Harmonic Distortion		-	-70	dB

Note

1. Resulted from comprehensive evaluation, not tested in production.

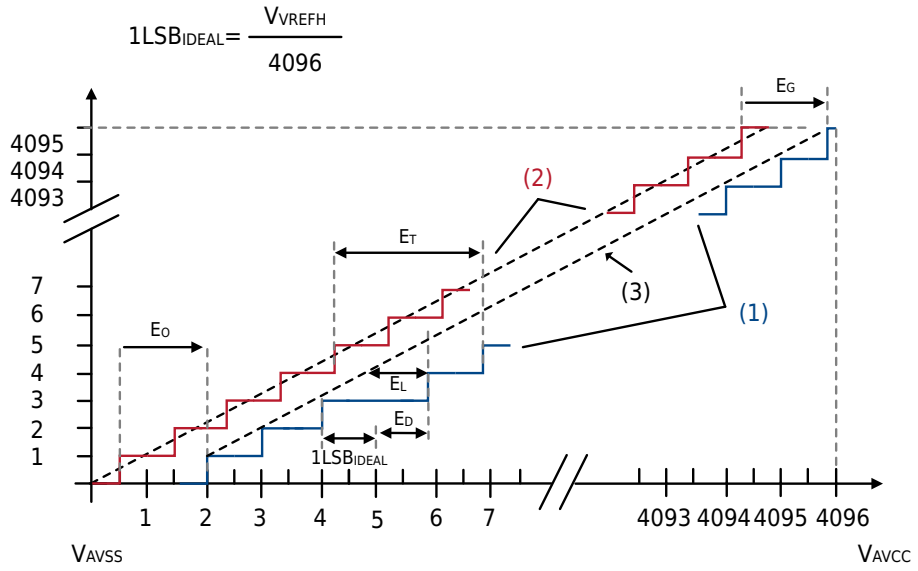


Figure 4-15 ADC Accuracy Characteristics

1. Example of actual transfer curve.
2. Ideal transfer curve.

3. Endpoint correlation line.
4. E_T = Total Unadjusted Error: Maximum deviation between actual and ideal transfer curves.
   E_O = Offset Error: Deviation between the first actual conversion and the first ideal conversion.
   E_G = Gain Error: Deviation between the last ideal conversion and the last actual conversion.
   E_D = Differential Nonlinearity Error: Maximum deviation between actual step and ideal value.
   E_L = Integral Nonlinearity Error: Maximum deviation between any actual conversion and the endpoint correlation line.

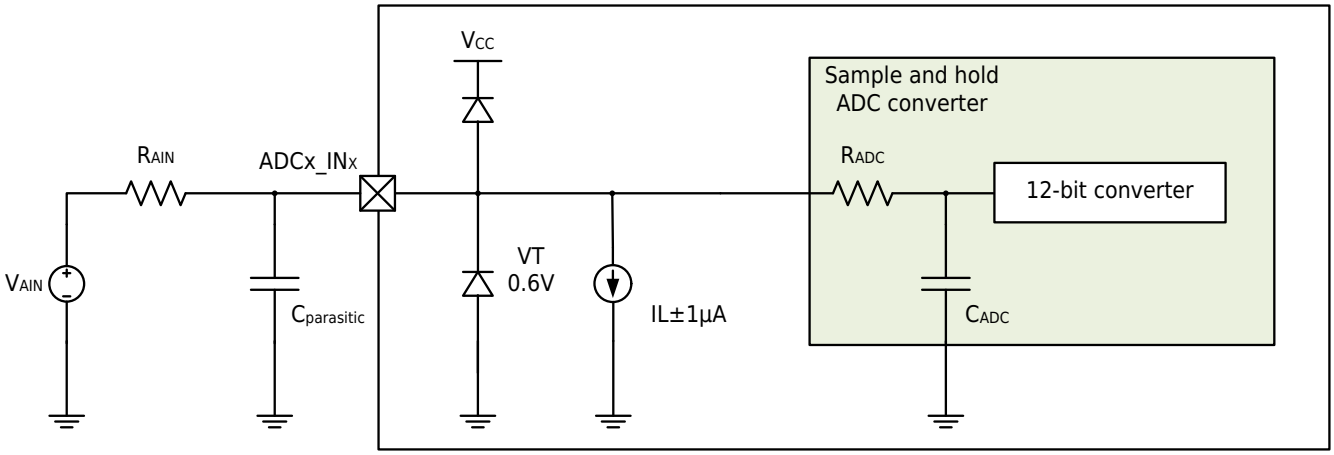


Figure 4-16 Typical Connection Using ADC

1. For information on R_{AIN}, R_{ADC}, and C_{ADC} values, refer to Table 4-30 : ADC Characteristics.
2. $C_{parasitic}$ indicates PCB capacitance (depending on the quality of soldering and PCB wiring) and bonding pad capacitance (about 5pF). Higher values of $C_{parasitic}$ result in less accurate conversions. To solve this problem, f_{ADC} should be reduced.

General PCB Design Guidelines

The power supply should be decoupled as shown in the figure below. The 0.1μF capacitor should be a (high-quality) ceramic capacitor. These capacitors should be placed as close to the chip as possible.

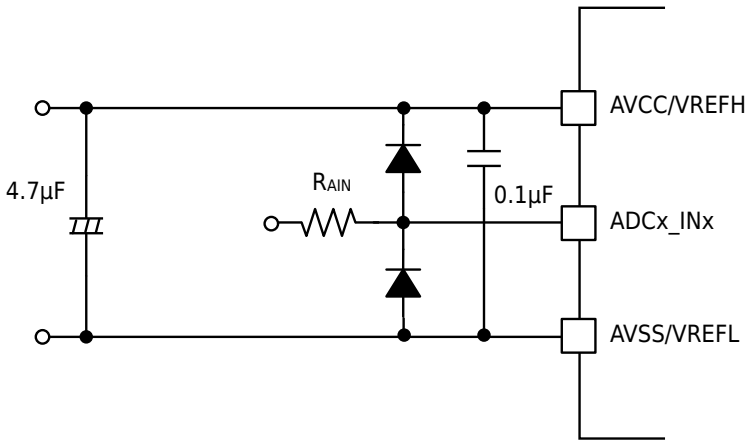


Figure 4-17 Example of Power Supply and Reference Supply Decoupling

1. For information on R_{AIN} values, refer to Table 4-30 : ADC Characteristics.

4.3.16 8-bit DAC Characteristics

Table 4-35 8-bit DAC Characteristics with Output Disabled

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{AVCC}(2)	Analog Power Voltage	-	2.7	5.0	5.5	V
AO(2)	Output Voltage Range	Reference voltage is AVCC	0	-	V_{AVCC}-1LSB	V
DNL(2)	Differential Non-linearity Error (deviation between two consecutive codes)	-	-	-	±1	LSB
TUE(2)	Total Unadjustable Error	Reference voltage is AVCC	-	-	±1	LSB
T_{up}	Startup Time	-	-	-	1	μs
T_{dacst}(1)	Setup Time (applies to 8-bit input code transition from lowest to highest input code, until DAC output reaches final value ±0.5LSB)	-	-	-	1	μs

Note

1. Guaranteed by design, not tested in production.
2. Resulted from comprehensive evaluation, not tested in production.

4.3.17 Comparator Characteristics

Table 4-36 Comparator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{AVCC}(2)	Analog Power Voltage	-	2.7	5.0	5.5	V
V_I(2)	Input Voltage Range	-	0	-	V_{AVCC}	V
V_{offset}(2)	Input Offset Voltage	-	-	10	-	mV
T_{cmp}(1)	Comparison Time	Comparator resolution voltage = 100mV	-	-	150	ns
T_{set}(2)	Stabilization Time for Input Channel Switching	-	-	100	250	ns

Note

1. Guaranteed by design, not tested in production.
2. Resulted from comprehensive evaluation, not tested in production.

4.3.18 OPA Characteristics

Table 4-37 OPA Features

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{AVCC}(2)	Analog power voltage	-	2.7	5.0	5.5	V

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
I_{CMR}(1)	Input common mode range	-	0	-	V_{AVCC}-1.2	V
V_{OUT}(1)	Output voltage range	-	0.2	-	V_{AVCC}-0.2	V
V_{OS}(2)	Input offset voltage	T_J=-40-125℃ V_{AVCC}=2.7-5.5V	-3.5	-	3.5	mV
C_{LOAD}(2)	Output load capacitance	-	-	-	50	pF
R_{LOAD}(2)	Output load resistance	-	10K	-	-	Ω
SR(1)	Slew rate	rising/falling	-	10	-	V/us
GBW(1)	Unity gain bandwidth	-	-	13	-	MHz
G_{DC}(1)	DC gain	-	-	100	-	dB
CMRR(1)	Common mode rejection ratio	V_{IN}=0.2V-V_{AVCC}-1.2	-	100	-	dB
PSRR(1)	Power supply rejection ratio	V_{IN}=0.2V-V_{AVCC}-1.2	-	75	-	dB
T_{set}(2)	Setup time	-	-	-	5	µs
I_{LOAD}(2)	Output current	V_{AVCC}=5.0V V_{OUT}=1V or V_{AVCC}-1V OPAxP-OPAxN=100mV	30	-	-	mA

Note

1. Guaranteed by design, not tested in production.
2. Resulted from comprehensive evaluation, not tested in production.

4.3.19 EIRQ Filter Characteristics

Table 4-38 EIRQ Filter Characteristics(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
W_{F_EIRQ}	EIRQ input filter width	INTC_EIRQCR.NOCSEL=0b00	0.5	-	1.0	µs
		INTC_EIRQCR.NOCSEL=0b01	1.0	-	2.0	µs
		INTC_EIRQCR.NOCSEL=0b10	2.0	-	4.0	µs
		INTC_EIRQCR.NOCSEL=0b11	4.0	-	8.0	µs

Note

1. Resulted from comprehensive evaluation, not tested in production.

4.3.20 RX Filter Characteristics in USART1 STOP Mode

Table 4-39 RX Filter Characteristics in USART1 STOP Mode(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
W_{F_USART1}	USART1 input filter width	USART1_NFC.USART1_NFS=0b00	0.5	-	1.0	μs
		USART1_NFC.USART1_NFS=0b01	1.0	-	2.0	μs
		USART1_NFC.USART1_NFS=0b10	2.0	-	4.0	μs
		USART1_NFC.USART1_NFS=0b11	4.0	-	8.0	μs

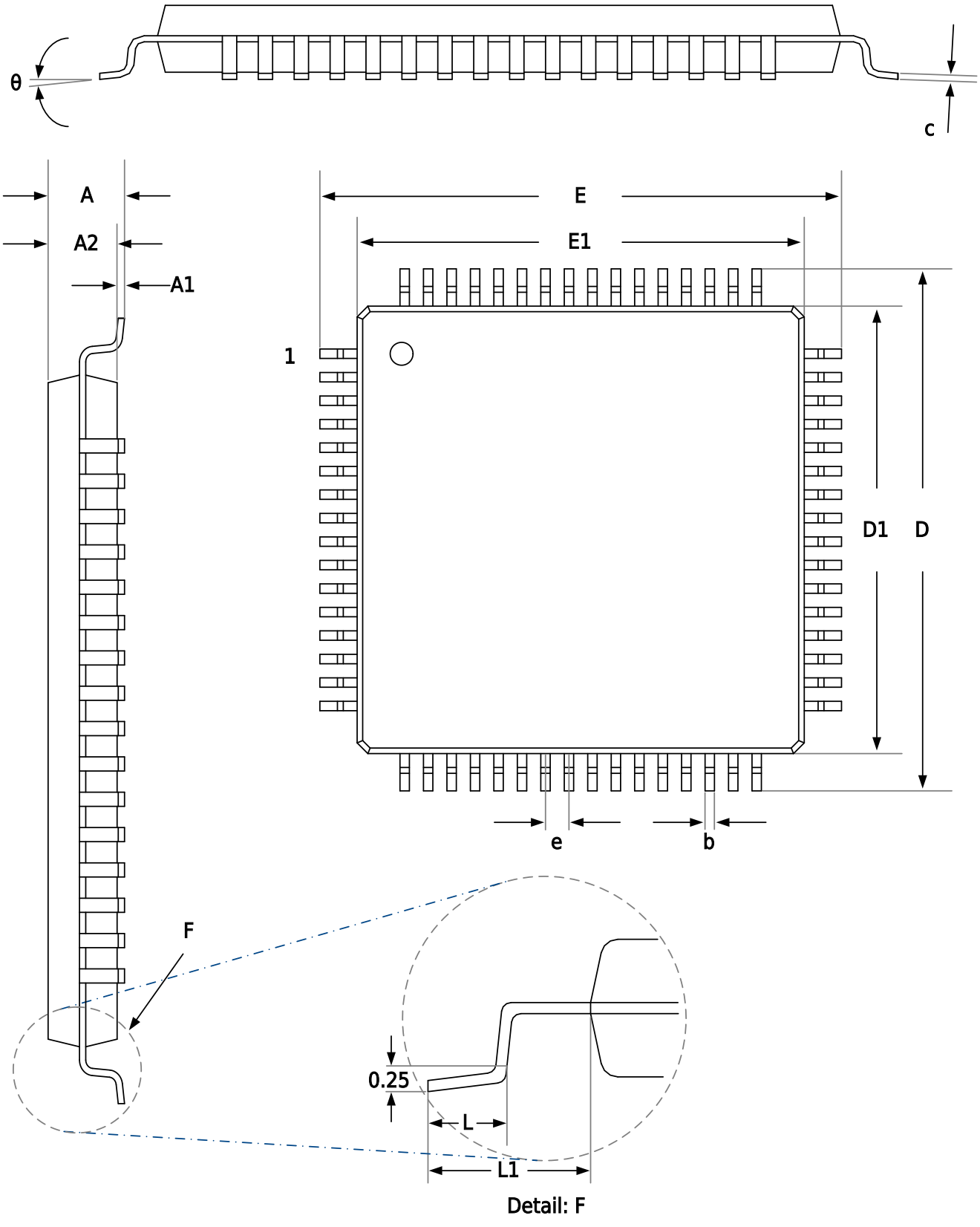
Note

1. Resulted from comprehensive evaluation, not tested in production.

5 Package Specifications

5.1 Package Dimensions

5.1.1 LQFP64 Package



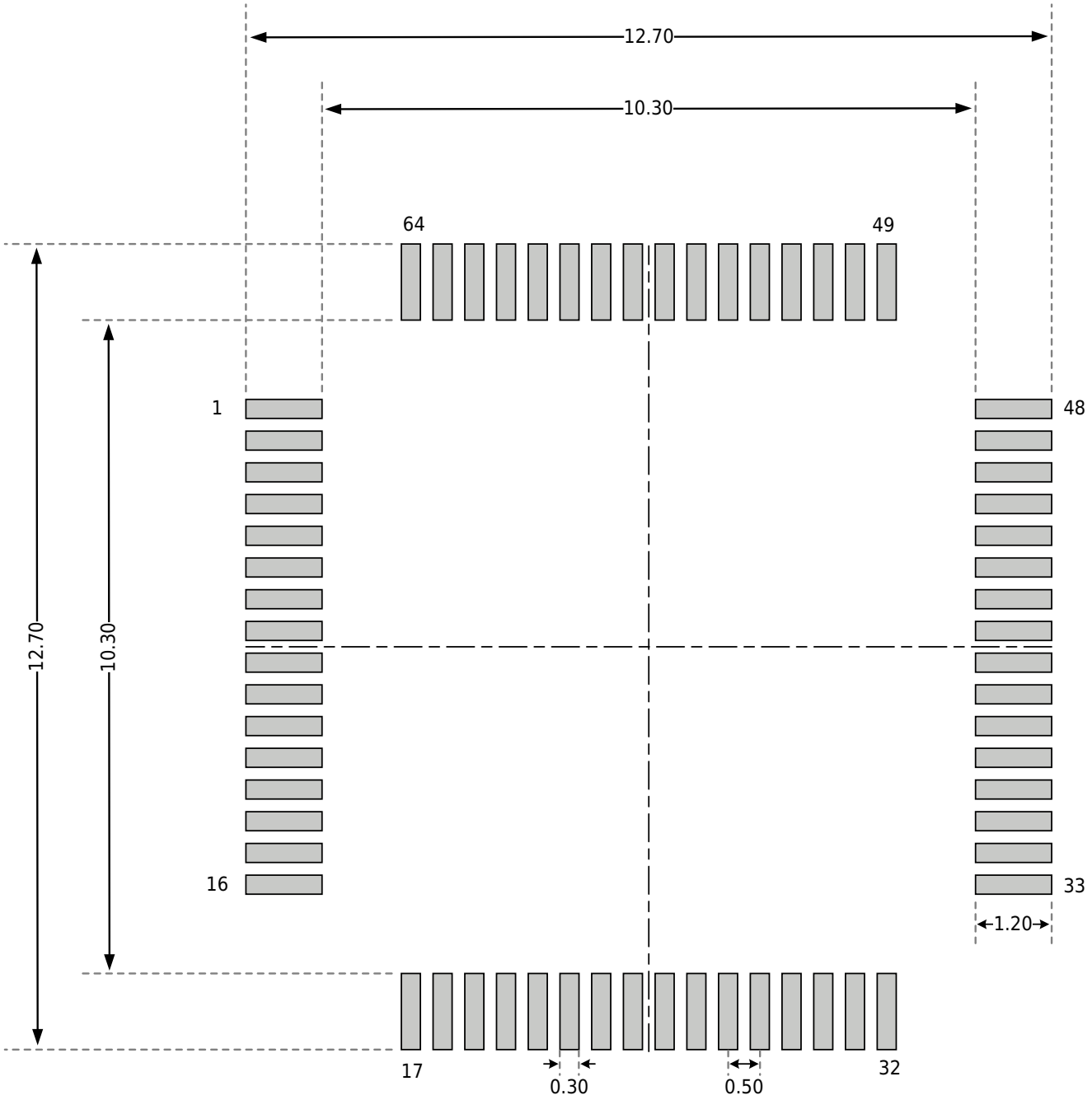
Symbol	10*10 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0°	--	7°

Note

Dimensions "D1" and "E1" do not include mold flash.

5.2 PCB Land Pattern

5.2.1 LQFP64 Package (10mm*10mm)



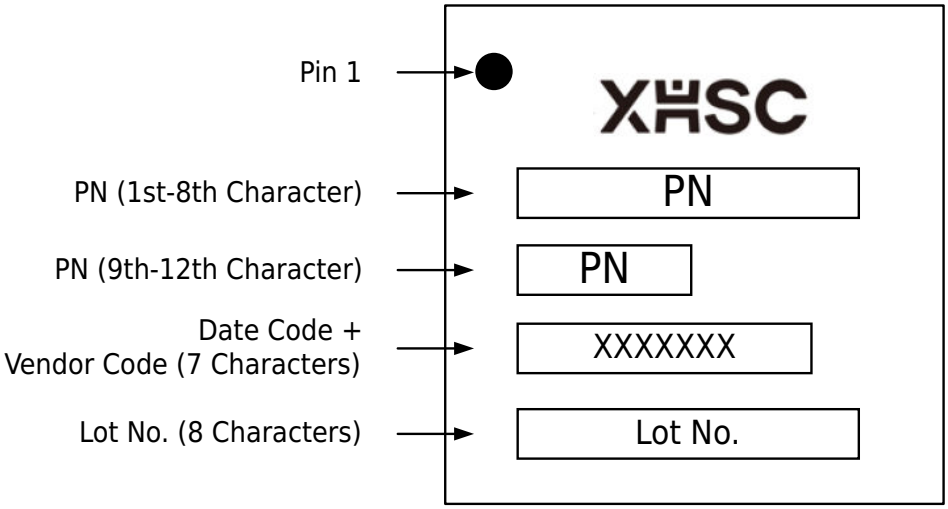
Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

5.3 Package Marking

The location and information description of Pin1 on the front of each package are given below.

LQFP64 package (10mm*10mm)



5.4 Packaging Thermal Resistance Coefficient

When the packaged chip is working at the specified working environment temperature, the junction temperature T_j(℃) of the chip surface can be calculated according to the following formula:

$T_j = T_A + (P_D * \theta_{JA})$

- T_A refers to the working environment temperature when the packaged chip is working, the unit is ℃;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is ℃/W;
- P_D refers to total power dissipation, which is the sum of internal power consumption (P_{INT}) and I/O pin power consumption (P_{IO}), the unit is W.

  $P_D = P_{INT} + P_{IO}$

  - P_{INT}: Internal power consumption, calculated as the product of Icc and Vcc.
  - P_{IO}: I/O pin power consumption, calculated as: $P_{IO} = \Sigma(V_{OL} * I_{OL}) + \Sigma((V_{CC} - V_{OH}) * I_{OH})$

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable junction temperature T_{Jmax} of the chip.

Table 5-2 Thermal Resistance Coefficient Reference Table For Each Package

Package Type and Dimensions	Thermal Resistance Parameters (θ_{JA})	Unit
LQFP64 10mm*10mm/0.5mm pitch	55	℃/W

6 Ordering Information

Part Number		HC32M458KETI- LQFP64	HC32M458KCTI-LQFP64
GPIO		52	52
CPU	Core	Cortex-M4	Cortex-M4
	Frequency	200MHz	200MHz
Memory	Code Flash (w/i ECC)	512KB	256KB
	Data Flash	8KB	8KB
	SRAM (w/i ECC)	64KB	64KB
Power supply voltages		2.7~5.5V	2.7~5.5V
Temp Range		-40~105℃	-40~105℃
DMA		1unit*2ch	1unit*2ch
TIMER	Timer0	2unit	2unit
	TimerA	5unit	5unit
	Timer4	2unit	2unit
WDT		1ch	1ch
SWDT		1ch	1ch
Connectivity	USART	4ch	4ch
	I2C	1ch	1ch
	SPI	2ch	2ch
Analog	12-bit ADC	2unit, 17ch	2unit, 17ch
	8-bit DAC	2ch	2ch
	CMP	2ch	2ch
	OPA	2ch	2ch
	PVD	√	√
Security	TRNG	√	√
Co-processing	MAU	√	√
CRC		√	√
Package (mm*mm)		LQFP64(10*10)	LQFP64(10*10)
Packing		Tray	Tray
Pitch		0.5mm	0.5mm
Thickness		1.4mm	1.4mm

Please contact the sales window for the latest mass production information before ordering.

Revision History

Revision/Date	Changes
Rev1.00 Jul. 10, 2026	First official release.