XIAOHUA SEMICONDUCTOR

HC32F431 Series

32-bit ARM® Cortex®-M4 Microcontroller

Reference Manual

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Preface

Bit/Bit Field

A register contains a bit (one bit wide) or a bit field (multiple bit width), and the bit field is usually described as [y:x], starting from the x bit and ending at the y bit. Unless otherwise specified, decimal numbers are used in the bit field.

It is not recommended to use unspecified fields; otherwise, unpredictable consequences may be caused.

Register Address

The address of each register can be obtained by the base address of the system address division and the offset address of the register (see the "Register List" of each module for details).

Access Type

The following abbreviations are used for register description:

Access Type	Description
RW	Readable and writable.
RO	Read only. Writes are ignored.
WO	Write only. Read value undefined.
RWA	Readable and writable. Writable only when unlocked or in safe mode.
RWC	Readable and writable. Writing any value clears this bit.
RC	Read only. Writes are ignored. This bit is cleared automatically after reading.
RS	Read only. Writes are ignored. This bit is set automatically after reading.

Number Format

- 0x prefix is used for hexadecimal numbers
- 0b prefix is used for binary numbers
- Numbers without prefix are in decimal representation

Reserved (Res.)

Registers and bit fields marked with *Reserved* are reserved for future use. These should be written to their reset value unless otherwise stated in the Register Description. The read value of Reserved bit may be different in different devices or features.

Reset Value (Reset)

The reset value indicates the value after the register is reset. Registers need to be initialized and reset before use; otherwise, unpredictable consequences may be caused.

Peripheral Availability Description

For HC32F431 Series 32-bit ARM® Cortex®-M4 Microcontroller supported peripherals and their numbers, refer to the corresponding "Datasheet".

Security Statement

There may be potential security problems due to the use of a certain function or protocol, which need to be declared to remind users and avoid security risks.

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1 Product Introduction

HC32F431 Series is a high-performance MCU with maximum operating 120MHz frequency based on 32-bit ARM® Cortex®-M4 Microcontroller. The Cortex-M4 core integrates an FPU and DSP for single-precision floating-point operations, supporting all ARM single-precision data processing instructions, data types, and full DSP instruction sets. The core integrates an MPU to ensure system security.

HC32F431 Series integrates high-speed on-chip memory, including a maximum of 128KB of Flash and a maximum of 16KB SRAM with parity check functionality. Integrated Flash access acceleration unit to achieve single cycle program execution of the CPU on Flash. A polling bus matrix allows multiple bus masters to access memory and peripherals simultaneously, enhancing performance. The bus master includes CPU and DMA. In addition to the bus matrix, it supports data transfer between peripherals, basic arithmetic operations and mutual triggering of events, which can significantly reduce the transaction processing load of the CPU.

HC32F431 Series integrates rich peripheral functions. It includes 1 12-bit 3.6Msps ADC, 3 operational amplifiers (OPA), 1 12-bit DAC, 3 high-speed voltage comparators (CMP), 1 motor PWM timer (Timer4) supporting 8-channel complementary PWM outputs, 5 16-bit general-purpose timers (TimerA) capable of 3-phase quadrature encoder input and 14-channel Duty independently configurable PWM outputs, 2 16-bit general-purpose timers (Timer0) supporting 4-channel synchronous/asynchronous counting, 6 serial communication interfaces (I2C/USART/SPI), 1 32-bit Hall signal processing unit (HALL) with 3-channel Hall signal input, 1 mathematical arithmetic unit (MAU).

HC32F431 Series supports wide voltage (2.7-5.5V), wide temperature (-40-105℃), and multiple low-power modes.

Typical Application

HC32F431 Series is available in 64-pin, 48-pin, and 32-pin LQFP package, designed for high-performance variable frequency control in the industrial and consumer electronics markets, such as industrial fans, industrial water pumps, floor scrubbers, vacuum cleaners, electric two-wheelers, power tools, and other applications.

About This Manual

This manual describes the chip's functionalities, operational guidelines, and usage methods. For detailed chip specifications, refer to the corresponding "Datasheet".

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2 Memory Mapping

2.1 Memory Mapping

This MCU supports a 4GB linear address space, with addresses from 0x00000000 to 0xFFFFFFFF, including programs and data. Please refer to the table below for detailed memory mapping.

Table 2-1 Memory Mapping

Memory Classification(2)		Start Address(1)	End Address(1)	Space size	Module(3)	Description
System	-	0xE0100000	0xFFFFFFFF	511MB	Reserved	Custom space
	Private Peripheral External Bus	0xE00FF000	0xE00FFFFF	4KB	ROMTABLE	-
		0xE0042400	0xE00FEFFF	755KB	BLANK	-
		0xE0042000	0xE00423FF	1KB	DBGC	Debug control register area
		0xE0041000	0xE0041FFF	4KB	BLANK	-
		0xE0040000	0xE0040FFF	4KB	BLANK	-
	Private Peripheral Internal Bus	0xE000F000	0xE003FFFF	196KB	BLANK	-
		0xE000E000	0xE000EFFF	4KB	SCS	System control space NVIC/ MPU, etc.
		0xE0003000	0xE000DFFF	44KB	BLANK	-
		0xE0002000	0xE0002FFF	4KB	FPB	-
		0xE0001000	0xE0001FFF	4KB	BLANK	-
		0xE0000000	0xE0000FFF	4KB	BLANK	-
External Peripheral	-	0xA0000000	0xDFFFFFFF	1024MB	Reserved	-
Externel Storage	-	0x98000000	0x9FFFFFFF	128MB	Reserved	-
		0x88200000	0x97FFFFFF	254MB	Reserved	-
	-	0x88100000	0x881FFFFF	1MB	Reserved	-
		0x88000000	0x880FFFFF	1MB	Reserved	-
		0x80000000	0x87FFFFFF	128MB	Reserved	-
		0x60000000	0x7FFFFFFF	512MB	Reserved	-
Peripheral	-	0x42C00000	0x5FFFFFFF	468MB	Reserved	-
		0x42200000	0x42BFFFFF	10MB	PeriBitBand	-
		0x40100000	0x421FFFFF	33MB	Reserved	-
	-	0x400C0000	0x400FFFFF	256KB	Reserved	-
	-	0x40080000	0x400BFFFF	256KB	Reserved	-
		0x40078000	0x4007FFFF	32KB	Reserved	-
	-	0x40070000	0x40077FFF	32KB	Reserved	-
		0x40060000	0x4006FFFF	64KB	Reserved	-
	AHB1 Clock: HCLK	0x40055000	0x4005FFFF	44KB	BLANK	-
		0x40054C00	0x40054FFF	1KB	PERIC	Peripheral control register
		0x40054800	0x40054BFF	1KB	MAU	-
		0x40054400	0x400547FF	1KB	CMU	-
		0x40054000	0x400543FF	1KB	PWC, RMU	-
		0x40053800	0x40053FFF	2KB	GPIO	-
		0x40053400	0x400537FF	1KB	BLANK	-
		0x40053000	0x400533FF	1KB	DMA	-
		0x40052400	0x40052FFF	3KB	BLANK	-

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Memory Classification[2]		Start Address[1]	End Address[1]	Space size	Module[3]	Description
Peripheral	AHB1 Clock: HCLK	0x40052000	0x400523FF	1KB	DCU	-
		0x40051000	0x40051FFF	4KB	INTC	-
		0x40050C00	0x40050FFF	1KB	BLANK	-
		0x40050800	0x40050BFF	1KB	BLANK	-
		0x40050400	0x400507FF	1KB	CRC	-
		0x40050000	0x400503FF	1KB	BLANK	-
	APB4 Clock: PCLK3	0x4004E400	0x4004FFFF	7KB	BLANK	-
		0x4004E000	0x4004E3FF	1KB	I2C	-
		0x4004A800	0x4004DFFF	14KB	BLANK	-
		0x4004A400	0x4004A7FF	1KB	CMP_3	-
		0x4004A000	0x4004A3FF	1KB	CMP_1/2, DAC	-
		0x40049800	0x40049FFF	2KB	BLANK	-
		0x40049400	0x400497FF	1KB	SWDT	-
		0x40049000	0x400493FF	1KB	WDT	-
		0x400488000	0x40048FFF	2KB	BLANK	-
		0x40048400	0x400487FF	1KB	FCM	-
		0x40040000	0x400483FF	33KB	BLANK	-
	APB3 Clock: PCLK4	0x40030400	0x40047FFF	63KB	BLANK	-
		0x40030000	0x400303FF	1KB	ADC, OPA	-
	APB1 Clock: PCLK1	0x40024800	0x40037FFF	46KB	BLANK	-
		0x40024400	0x400247FF	1KB	Timer0_2	-
		0x40024000	0x400243FF	1KB	Timer0_1	-
		0x40022800	0x40023FFF	6KB	BLANK	-
		0x40022400	0x400227FF	1KB	BLANK	-
		0x40022000	0x400223FF	1KB	BLANK	-
		0x40021C00	0x40021FFF	1KB	BLANK	-
		0x40021800	0x40021BFF	1KB	BLANK	-
		0x40021400	0x400217FF	1KB	USART_4	-
		0x40021000	0x400213FF	1KB	USART_3	-
		0x40020C00	0x40020FFF	1KB	BLANK	-
		0x40020800	0x40020BFF	1KB	BLANK	-
		0x40020400	0x400207FF	1KB	BLANK	-
		0x40020000	0x400203FF	1KB	BLANK	-
	APB1 Clock: PCLK1	0x4001EC00	0x4001FFFF	5KB	BLANK	-
		0x4001E800	0x4001EBFF	1KB	HALL	-
		0x4001E400	0x4001E7FF	1KB	BLANK	-
		0x4001E000	0x4001E3FF	1KB	BLANK	-
		0x4001DC00	0x4001DFFF	1KB	BLANK	-
		0x4001D800	0x4001DBFF	1KB	BLANK	-
		0x4001D400	0x4001D7FF	1KB	USART_2	-
		0x4001D000	0x4001D3FF	1KB	USART_1	-
		0x4001CC00	0x4001CFFF	1KB	BLANK	-
		0x4001C800	0x4001CBFF	1KB	BLANK	-
		0x4001C400	0x4001C7FF	1KB	BLANK	-
		0x4001C000	0x4001C3FF	1KB	SPI	-

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Memory Classification[2]		Start Address[1]	End Address[1]	Space size	Module[3]	Description
Peripheral	APB1 Clock: PCLK1	0x40018000	0x4001BFFF	16KB	BLANK	-
		0x40017C00	0x40017FFF	1KB	EMB	-
		0x40017400	0x40017BFF	2KB	BLANK	-
		0x40017000	0x400173FF	1KB	Timer4	-
		0x40016400	0x40016FFF	3KB	BLANK	-
		0x40016000	0x400163FF	1KB	TimerA_5	-
		0x40015C00	0x40015FFF	1KB	TimerA_4	-
		0x40015800	0x40015BFF	1KB	TimerA_3	-
		0x40015400	0x400157FF	1KB	TimerA_2	-
		0x40015000	0x400153FF	1KB	TimerA_1	-
		0x40010C00	0x40014FFF	17KB	BLANK	-
		0x40010800	0x40010BFF	1KB	AOS	Internal trigger event register region
		0x40010400	0x400107FF	1KB	EFM	-
		0x40010000	0x400103FF	1KB	BLANK	-
	AHB Clock: PCLK1	0x4000F000	0x4000FFFF	4KB	Reserved	-
		0x4000E000	0x4000EFFF	4KB	Reserved	-
		0x4000C000	0x4000DFFF	8KB	Reserved	-
		0x4000B000	0x4000BFFF	4KB	Reserved	-
		0x40009400	0x4000AFFF	7KB	Reserved	-
		0x40009000	0x400093FF	1KB	Reserved	-
		0x40008C00	0x40008FFF	1KB	Reserved	-
		0x40008800	0x40008BFF	1KB	Reserved	-
		0x40008400	0x400087FF	1KB	Reserved	-
		0x40008000	0x400083FF	1KB	Reserved	-
		0x40000000	0x40007FFF	32KB	Reserved	-
SRAM	SRAM Clock: HCLK	0x22040000	0x3FFFFFFF	479.75MB	Reserved	-
		0x22000000	0x2203FFFF	256KB	SRAMBitBand	-
		0x20100000	0x21FFFFFF	31MB	Reserved	-
		0x20010000	0x200FFFFF	960KB	Reserved	-
		0x20020000	0x2000FFFF	56KB	Reserved	-
		0x20000000	0x20001FFF	8KB	SRAM1	-
CODE	SRAM Clock: HCLK	0x1FFFE000	0x1FFFFFFF	8KB	SRAMH	-
		0x03004000	0x1FFDFFFF	463.86MB	BLANK	-
	PCROP, Flash Clock: HCLK	0x01000E08	0x03003FFF	32MB	BLANK	-
		0x01000E00	0x01000E07	8B	PCROP	Code read protection
		0x01000C0C	0x01000DFF	500B	BLANK	-
		0x01000C00	0x01000C0B	12B	Data security protection	Used for configuration of data security protection
	-	0x00040000	0x01000BFF	15.75MB	BLANK	-
	-	0x00020200	0x0003FFFF	127.5KB	Reserved	-
	Flash Clock: HCLK	0x00020000	0x000201FF	0.5KB	ICG	-
		0x00000000	0x0001FFFF	128KB	Flash	-

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Note

1. Please refer to the "ARM Cortex-M4 Processor Technical Reference Manual Revision: r0p1".
2. For bus descriptions, please refer to the relevant descriptions in the "Bus Architecture (BUS) " chapter.
3. Reserved: Accessing the bus will cause a bus error; BLANK: Write access has no effect, and read access returns 0.

2.2 Bit Segment Space

Cortex-M4 memory mapping includes two bit segment regions. These regions map each word in the memory alias region to the corresponding bit in the memory bit segment region. Writing a word to the alias area is equivalent to a read-modify-write operation on the target bit of the bit segment region.

In this MCU, peripheral registers and SRAM are mapped to a bit segment region, enabling read and write operations on individual bit segments. These operations are only applicable to Cortex-M4 access and are invalid for other bus master interfaces (e.g., DMA).

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3 Bus Architecture (BUS)

3.1 Introduction

The main system consists of a 32-bit multi-layer AHB bus matrix, enabling the interconnection of the following host buses and slave buses:

- Host bus
  - Cortex-M4 core CPU-I bus, CPU-D bus, CPU-S bus
  - System DMA bus
- Slave bus
  - Code Flash ICODE bus
  - Code Flash DCODE bus
  - Code Flash MCODE bus (The bus for accessing Code Flash by components other than the CPU on the host)
  - System SRAMH (SRAMH 8KB) bus
  - System SRAM (SRAM1 8KB) bus
  - APB1 peripheral bus (AOS/EMB/Timer0/Timer4/TimerA/SPI/USART/EFM/HALL)
  - APB3 peripheral bus (ADC)
  - APB4 peripheral bus (FCM/WDT/SWDT/CMP/I2C)
  - AHB1 peripheral bus (INTC/DCU/GPIO/DMA/FCG/CMU/PWC/MAU/CRC)

With the bus matrix, efficient concurrent access from host buses to slave buses can be achieved.

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3.2 Bus Architecture

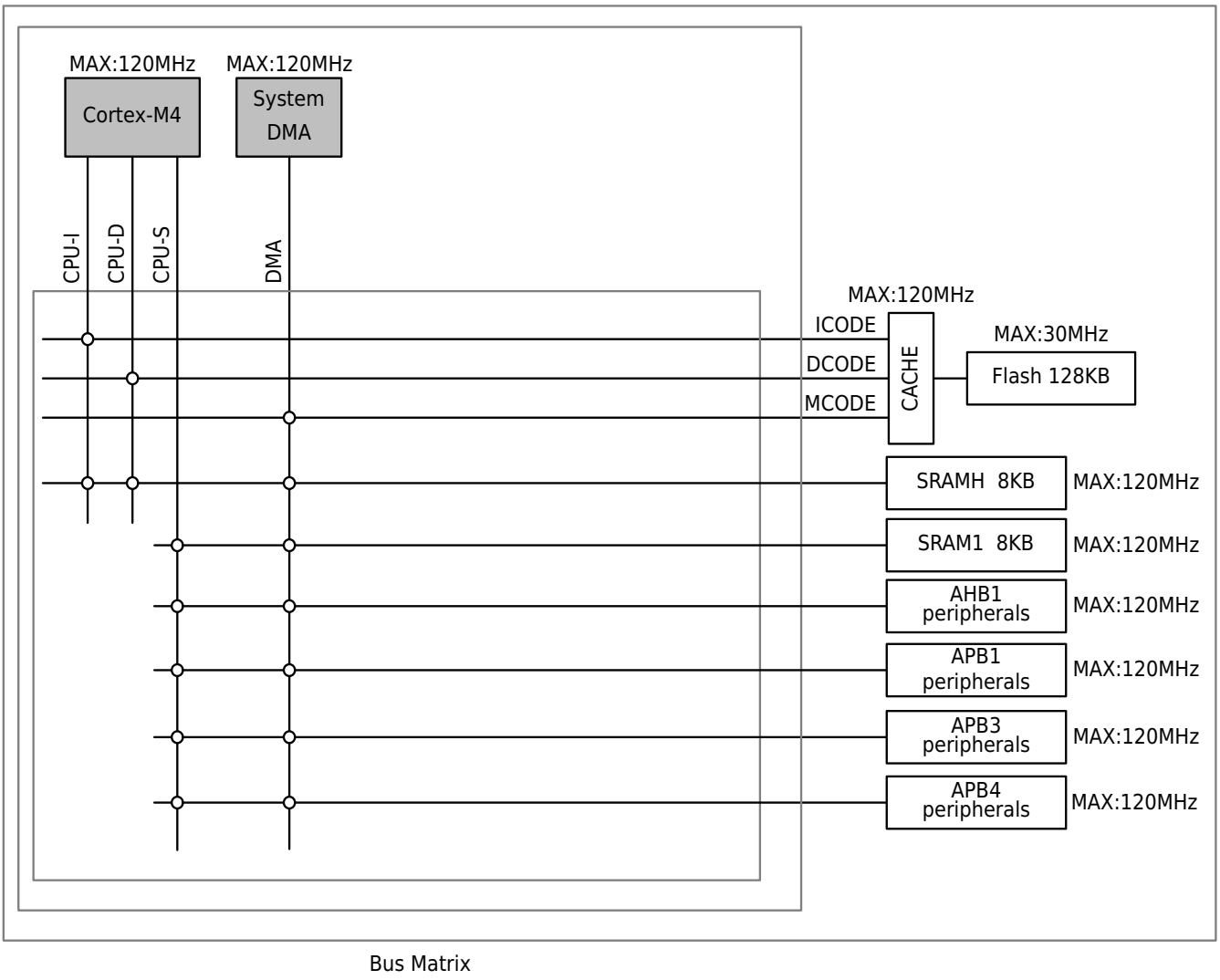

Figure 3-1 Bus Architecture Diagram

The bus matrix manages access arbitration between host buses. Arbitration uses a round-robin scheduling algorithm.

- CPU-I bus

  Cortex-M4 Core Command Bus: The CPU fetches instructions through this bus. Access targets: Code Flash and SRAMH containing code.

- CPU-D bus

  Cortex-M4 Core Data Bus: The CPU performs immediate number loading and debug access through this bus. Access targets: Code Flash and SRAMH containing code or data.

- CPU-S bus

  Cortex-M4 Core System Bus: The CPU accesses peripherals or system SRAM through this bus. It can also fetch instructions and immediate numbers through this bus (though less efficient than through the CPU-I bus and CPU-D bus). Access targets: SRAM1, all peripherals, and external extended space.

- DMA bus

  The system DMA has a dedicated bus through which it accesses data memory and peripherals. The access targets are Code Flash/SRAMH/SRAM1, all peripherals, and external extended space.

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3.3 Bus Function

The bus is responsible for implementing read and write access from the host to the slave.

Through the bus matrix, when the access targets of different host buses do not conflict, each access can be carried out simultaneously. For instance, CPU-I accesses Code Flash, CPU-D accesses SRAMH, CPU-S accesses APB peripherals, and DMA accesses SRAM1. These accesses can be carried out simultaneously.

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4 Reset Module Unit (RMU)

4.1 Introduction

The chip is configured with 12 reset modes:

- Power-on Reset (POR)
- NRST Pin Reset (NRST)
- Brown-out Reset (BOR)
- Programmable Voltage Detection 1 Reset (PVD1R)
- Programmable Voltage Detection 2 Reset (PVD2R)
- Watchdog Reset (WDTR)
- Special Watchdog Reset (SWDTR)
- Software Reset (SRST)
- RAM Parity Reset (RAMPR)
- Clock Frequency Error Reset (CKFER)
- XTAL Error Reset (XTALER)
- Cortex-M4 Lockup Reset (LKUPR)

4.2 Functional Description

4.2.1 Reset Mode and Reset Flag Bit

The reset mode and generating conditions are shown in the following table.

Table 4-1 Reset Mode and Generating Conditions

Reset Mode	Generating Condition
Power-on Reset	VCC powered on
NRST Pin Reset	NRST pin input low level
Brown-out Reset	VCC voltage drops below VBOR voltage
Programmable Voltage Detection 1 Reset	VCC voltage drops below PVD1 voltage
Programmable Voltage Detection 2 Reset	VCC voltage drops below PVD2 voltage
Watchdog Reset	Watchdog timer generates a refresh error or an overflow error
Special Watchdog Reset	Refresh error or overflow error occurred in special watchdog
Software Reset	Set the reset register bit (ARM register AIRCR.SYSRESETREQ bit)
RAM Parity Reset	Reset generated when a parity error occurs in RAM
Clock Frequency Error Reset	When the clock frequency monitoring function (FCM) detects a clock period error
XTAL Error Reset	Resetting of external high-speed oscillator abnormal shock
Cortex-M4 Lockup Reset (LKUPR)	When Cortex-M4 encounters a serious exception, it will stop its PC pointer at the current address and lock it, and reset the entire chip after a few clock period delays.

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When a reset occurs, the chip will set the corresponding reset flag according to the reset method, and the reset flag is as shown. For example, pin reset occurs, pin reset flag bit PINRF is set to 1, PINRF can be reset by writing CLRF after PINRF is set.

Table 4-2 Reset Mode and Reset Flag

Reset Flag	Reset Mode											
	Power-on Reset	Pin Reset	Brown-out Reset	Voltage Detection 1 Reset	Voltage Detection 2 Reset	Watchdog Reset	Special Watchdog Reset	Software Reset	RAM Parity Error Reset	Clock Frequency Error Reset	XTAL Error Reset	Cortex-M4 Lockup Reset
Power-on reset flag (RMU_RSTF0.PORF)	✓	-	-	-	-	-	-	-	-	-	-	-
Pin reset flag (RMU_RSTF0.PINRF)	×	✓	-	-	-	-	-	-	-	-	-	-
Brown-out reset flag (RMU_RSTF0.BORF)	×	×	✓	-	-	-	-	-	-	-	-	-
Programmable voltage detection 1 reset flag (RMU_RSTF0.PVD1RF)	×	×	-	✓	-	-	-	-	-	-	-	-
Programmable voltage detection 2 reset flag (RMU_RSTF0.PVD2RF)	×	×	-	-	✓	-	-	-	-	-	-	-
Watchdog reset flag (RMU_RSTF0.WDRF)	×	×	-	-	-	✓	-	-	-	-	-	-
Special watchdog reset flag (RMU_RSTF0.SWDRF)	×	×	-	-	-	-	✓	-	-	-	-	-
Software reset flag (RMU_RSTF0.SWRF)	×	×	-	-	-	-	-	✓	-	-	-	-
RAM parity error reset flag (RMU_RSTF0.RAPERF)	×	×	-	-	-	-	-	-	✓	-	-	-
Clock frequency error reset flag (RMU_RSTF0.CKFERF)	×	×	-	-	-	-	-	-	-	✓	-	-
XTAL error reset flag (RMU_RSTF0.XTALERF)	×	×	-	-	-	-	-	-	-	-	✓	-
Cortex-M4 Lockup reset flag (RSTF0.LKUPRF)	×	×	-	-	-	-	-	-	-	-	-	✓

Note

"✓" indicates setting; "×" indicates clearing; "-" indicates unchanged.

4.2.2 Reset Timing

4.2.2.1 Power-on Reset

Power-on reset is an internal reset caused by the power-on reset circuit, and the timing is as follows. After a certain period of time (T_{RSTPOR}) after the VCC voltage is higher than the power-on reset voltage V_{POR}, the internal reset of the chip is released, and the CPU starts to execute the code. When generating power-on reset, power-on reset flag RMU_RSTF0.PORF is set. For detailed instructions on power-on reset, see "Power-on/Power-down Reset Action Description" in the "Power Control (PWC)" chapter.

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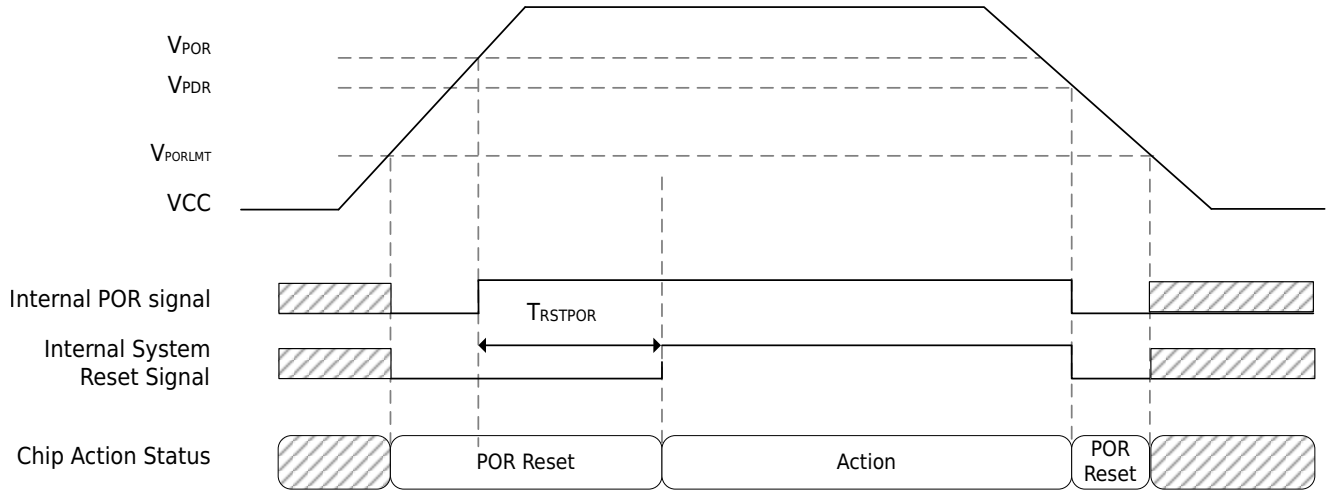

Figure 4-1 Power-on Reset Timing Diagram

4.2.2.2 NRST Pin Reset

Pin reset is caused by the NRST pin being driven to a low level. The reset timing is shown in the figure below. After the NRST pin maintains a low level above the T_{NRST} width, after a certain internal reset time (T_{INRST}), the internal reset is released.

When an NRST pin reset is generated, the pin reset flag RMU_RSTF0.PINRF is set.

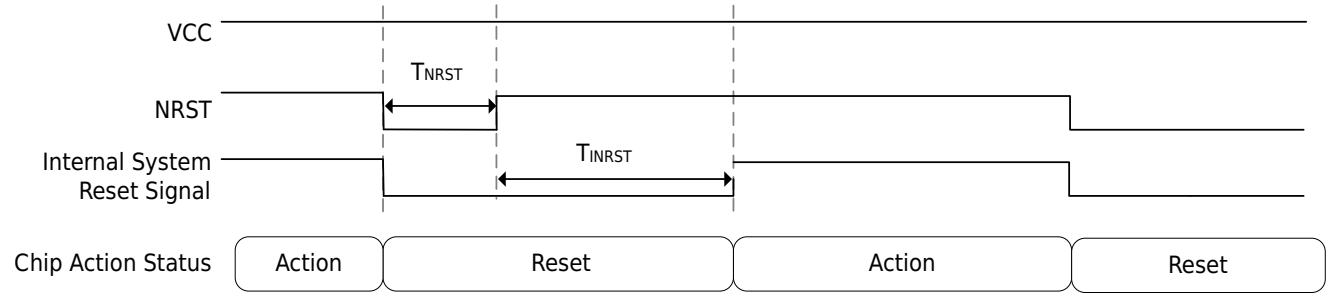

Figure 4-2 NRST Reset Timing Diagram

4.2.2.3 Brown Out Reset

Brown-out reset is an internal reset caused by the voltage monitoring circuit, and the timing is shown in the figure below. After the undervoltage is set as reset enable through the ICG register, if the VCC voltage is lower than the monitoring voltage V_{BOR}, RMU_RSTF0.BORF will be set. When the VCC voltage is higher than the monitoring voltage V_{BOR}, the reset will be released after the V_{BOR} reset time (T_{RSTBOR}).

For the reset setting of brown-out, please refer to the "Brown-out Reset (BOR) Description" in the "Power Control (PWC)" chapter.

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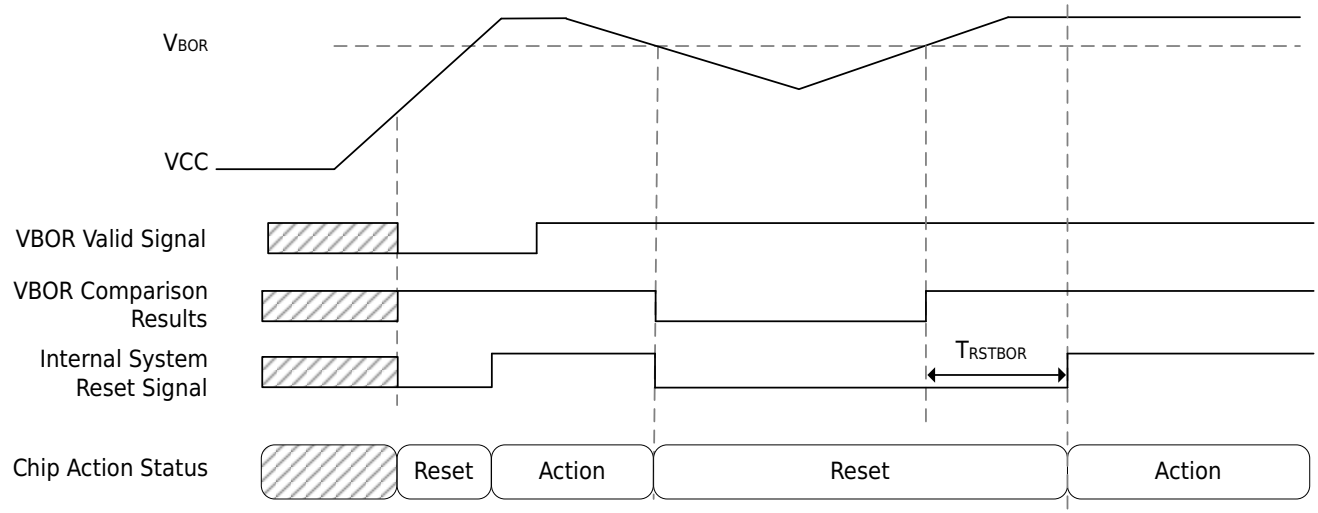

Figure 4-3 Brown-out Reset Timing Diagram

4.2.2.4 Programmable Voltage Detection 1 Reset, Programmable Voltage Detection 2 Reset

Programmable Voltage Detection 1 Reset and Programmable Voltage Detection 2 Reset are resets generated by the voltage monitoring circuit.

When the VCC voltage is lower than the monitoring voltage of the programmable voltage detection 1, a programmable voltage detection 1 reset may be generated according to the setting, and RMU_RSTF0.PVD1RF is set. When the VCC voltage is higher than the monitoring voltage of programmable voltage detection 1, the reset will be released after the reset time of PVD1 (T_{IPVD1}).

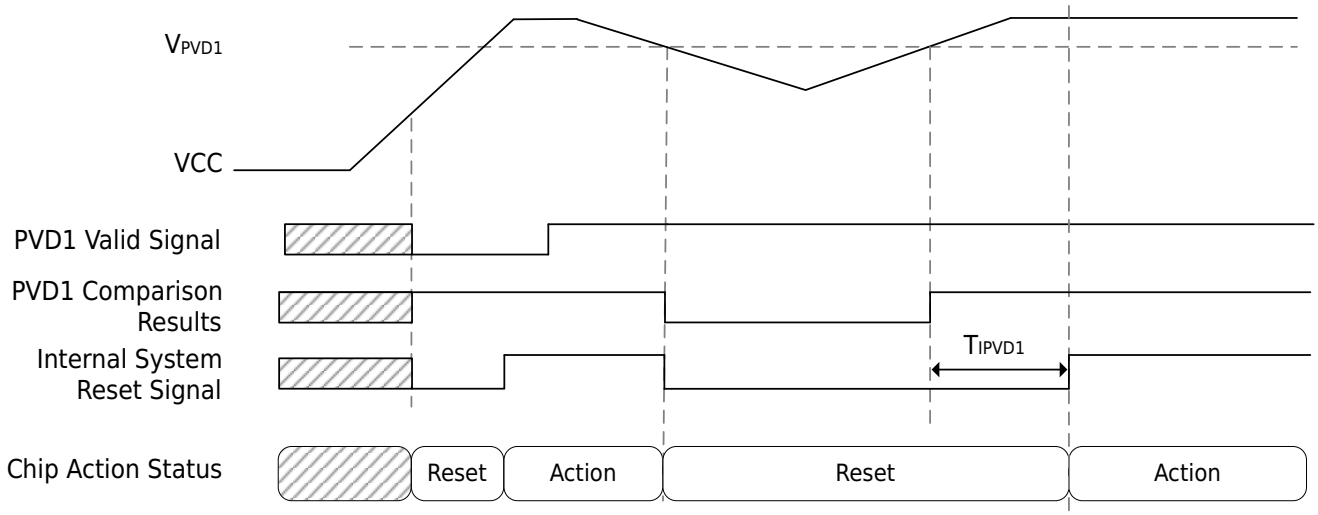

Figure 4-4 Programmable Voltage Detection 1 Reset Timing Diagram

When the VCC voltage is lower than the monitoring voltage of the programmable voltage detection 2, according to the setting, a programmable voltage detection 2 reset may be generated and RMU_RSTF0.PVD2RF is set. When the VCC voltage is higher than the monitoring voltage of programmable voltage detection 2, the reset will be released after the reset time of PVD2 (T_{IPVD2}).

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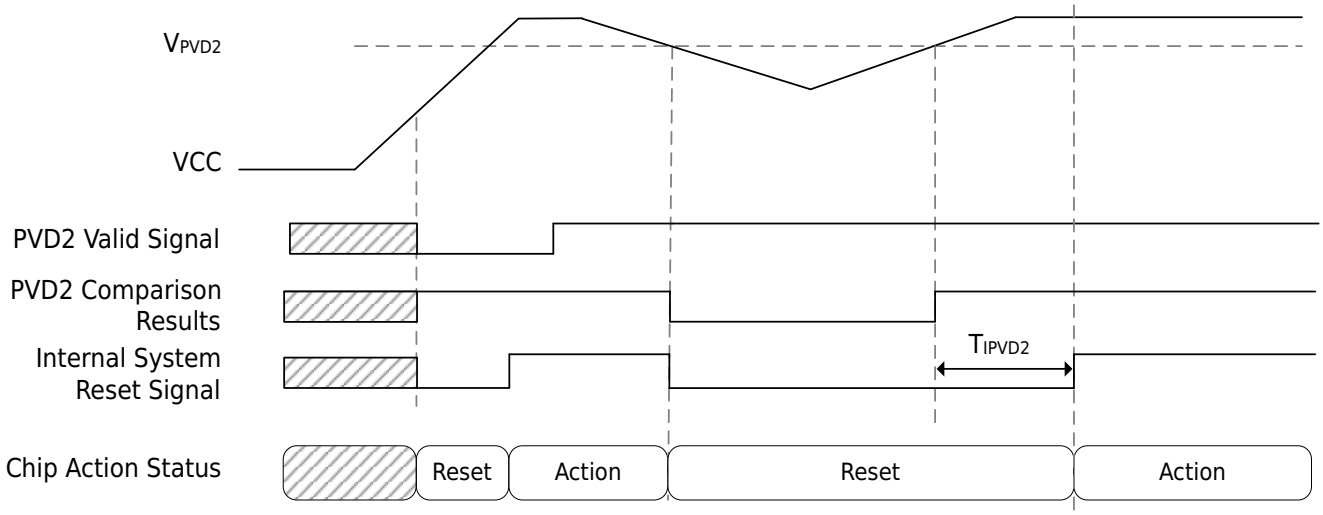

Figure 4-5 Programmable Voltage Detection 2 Reset Timing Diagram

For the reset settings of programmable voltage detection 1 and programmable voltage detection 2, see "Programmable Voltage Detection 1 (PVD1), Programmable Voltage Detection 2 (PVD2)" in the "Power Control (PWC)" chapter.

4.2.2.5 Watchdog Reset, Special Watchdog Reset

The watchdog reset is an internal reset caused by the watchdog timer, and the special watchdog reset is an internal reset caused by the special watchdog timer. The reset timing is as follows.

After the watchdog reset is set to be active, the watchdog reset will be generated when the watchdog timer underflows or the write operation is not performed during the refresh period. A watchdog reset sets RMU_RSTF0.WDRF. After the watchdog reset is generated, the chip is released from reset after the internal reset time T_{RIPT}.

After the special watchdog reset is set to be active, the watchdog reset will be generated when the special watchdog timer underflows or the write operation is not performed during the refresh period. Special watchdog reset RMU_RSTF0.SWDRF setup. After generating special watchdog reset, after internal reset time T_{RIPT}, the chip is released.

For details on watchdog reset and special watchdog reset, see the relevant description in the "Watchdog Timer (WDT/SWDT)" chapter.

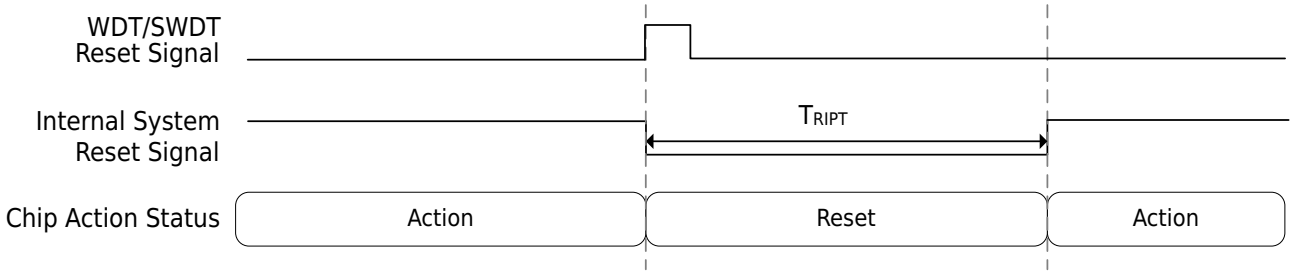

Figure 4-6 Watchdog and Special Watchdog Reset Timing Diagram

4.2.2.6 Software Reset

A software reset is generated by writing the AIRCR.SYSRESETREQ bit of ARM register. When generating software reset, RMU_RSTF0.SWRF bit is set. After the internal reset time T_{RIPT}, the chip is de-reset.

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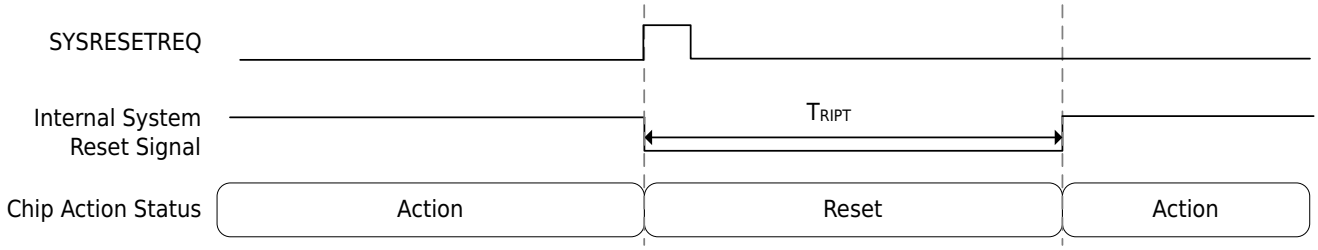

Figure 4-7 Software Reset Timing Diagram

4.2.2.7 RAM Parity Reset

When a RAM parity error occurs, a RAM parity reset may occur according to the settings. The reset timing is as follows. A RAM parity error sets RMU_RSTF0.RAPERF. After the internal reset time T_{RIPT}, the chip is de-reset.

For the setting of RAM parity error reset, please refer to the relevant description in the "Built-in SRAM (SRAM)" chapter.

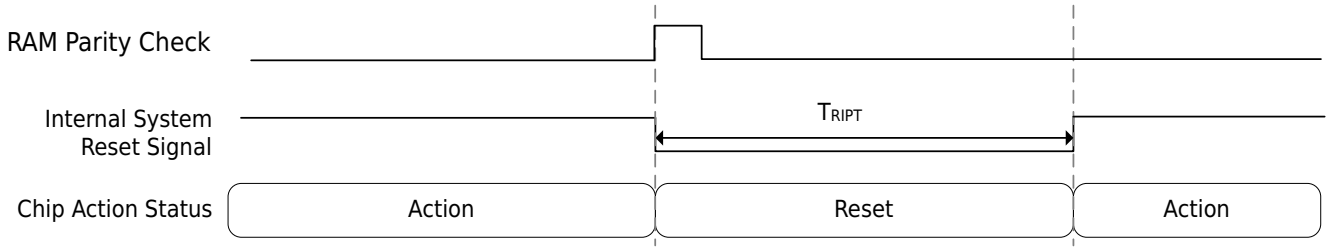

Figure 4-8 RAM Parity Reset Timing Diagram

4.2.2.8 Clock Frequency Error Reset

When the on-chip FCM module detects a clock frequency error, it can generate a clock frequency error reset according to the settings. The reset timing is as follows. Clock frequency error reset sets RMU_RSTF0.CKFERF. After the internal reset time T_{RIPT}, the chip is de-reset.

For the setting of clock frequency error reset, refer to "Clock Frequency Measurement" in the "Clock Module Unit (CMU)" chapter.

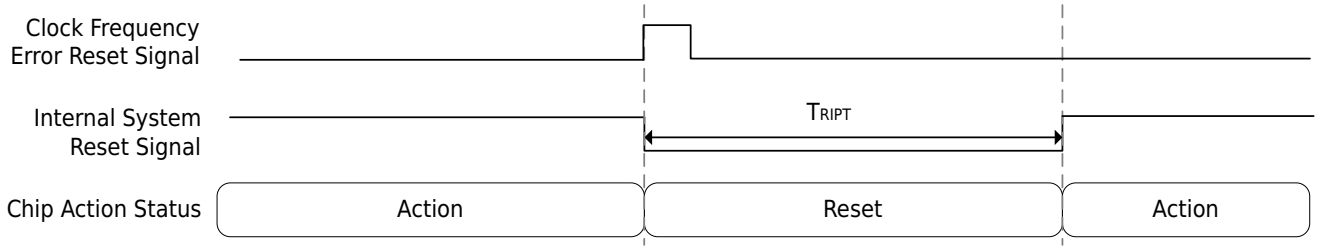

Figure 4-9 Clock Frequency Error Reset Timing Diagram

4.2.2.9 XTAL Error Reset

When the chip's oscillation stop detection is enabled and reset is also enabled, if an XTAL error occurs, the XTAL error reset will be generated, and the RMU_RSTF0.XTALERF will be set. After the internal reset time T_{RIPT}, the chip is de-reset.

For the setting of XTAL error reset, refer to "External High-speed Oscillator Fault Detection" in the "Clock Module Unit (CMU)" chapter.

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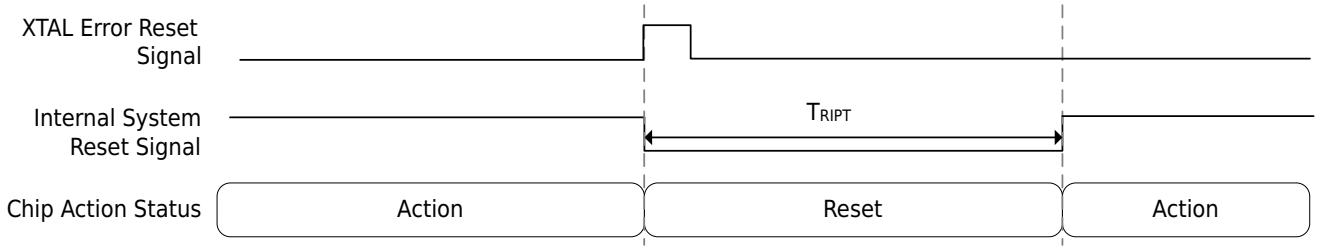

Figure 4-10 XTAL Error Reset Timing Diagram

4.2.2.10 Cortex-M4 Lockup Reset

When Cortex-M4 encounters a serious exception, it will stop its PC pointer at the current address, lock itself, and reset the entire chip after a delay of several clock periods. The timing is shown below. Cortex-M4 Lockup reset sets RMU_RSTF0.LKUPRF. After the internal reset time T_{RIPT}, the chip is de-reset.

Cortex-M4 Lockup reset can only be used after RMU_RSTF0.LKUPRF is clear.

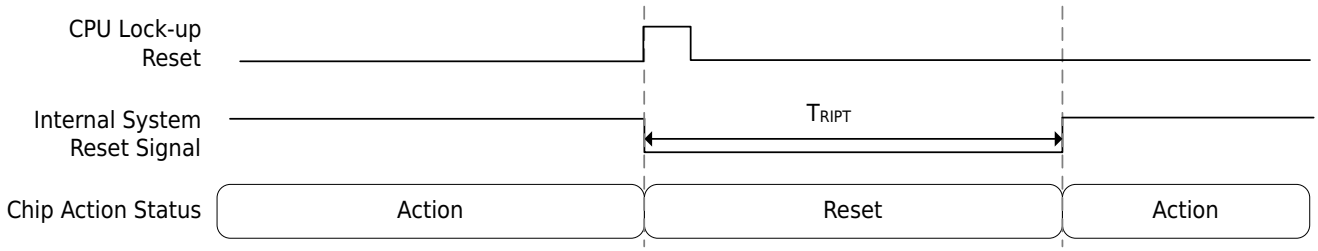

Figure 4-11 Cortex-M4 Lockup Reset Timing Diagram

4.2.3 Reset Mode Judgment

The reset mode can be judged according to the reset flag of RMU_RSTF0. Multiple reset flags may occur when two or more resets occur simultaneously. Multiple resets occur when the RMU_RSTF0.MULTIRF bit is 1. After reading RMU_RSTF0, all reset flags can be cleared to 0 by setting the CLRF bit. After setting and clearing RMU_RSTF0, wait at least 6 CPU clock periods before reading the RMU_RSTF0 register again.

4.2.4 Module Function Reset

In addition to the above-mentioned chip reset methods, the product also configures function reset registers RMU_FRST0 for each peripheral module. Writing 0 to the corresponding bit of RMU_FRST can reset the function of the corresponding module. After RMU_FRST is written to 0, it will be automatically set to 1 after 2 rising edges of peripheral module clock. After writing 0 to RMU_FRST, it is necessary to wait for at least 2 CPU clock periods before reading the RMU_FRST register again.

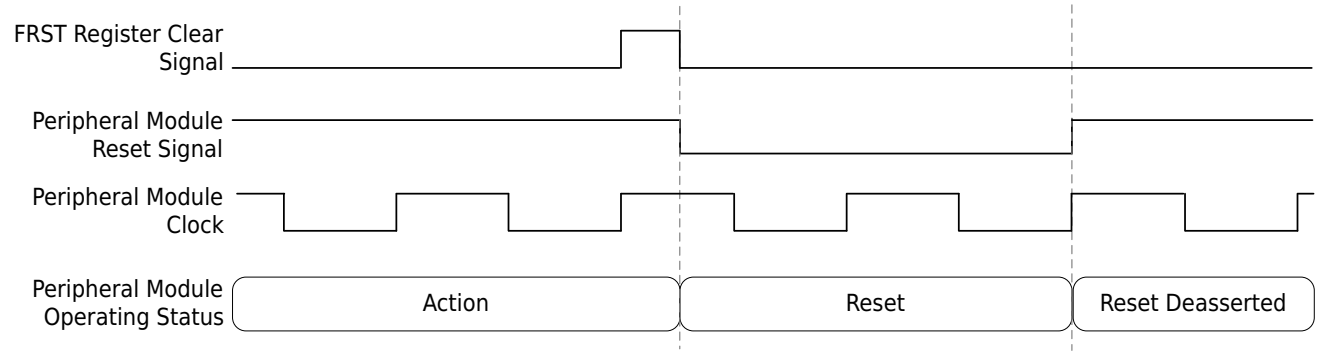

Figure 4-12 Module Function Reset

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4.2.5 Reset Condition

Table 4-3 Reset Conditions for Each Module

Modules	Register	Reset Source
DBGC	DBGC_MCUSTPCTL DBGC_MCUDBGCSTAT DBGC_FCRCCR0 DBGC_FCRCCR1 DBGC_FCRCDOR DBGC_FCRCREF DBGC_FMCCTL	Power-on reset
PWC	PWC_PVDLCR PWC_PVDCR1 PWC_PVDFCR PWC_PVDCR0 PWC_PVDICR PWC_PVDDSR.PVD1DETFLG PWC_PVDDSR.PVD2DETFLG	All reset sources other than the following: ● Programmable voltage detection 1 reset ● Programmable voltage detection 2 reset
	Other registers than the above	All reset sources
Registers other than the above modules		All reset sources

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4.3 Register Description

4.3.1 Register List

Base address: 0x40054100

Table 4-4 Reset Module Unit (RMU) Register Offset

Offset	Register	Description	Width
0x04	RMU_FRST0	Function Reset Control Register 0	32
0x00	RMU_RSTF0	Reset Flag Register 0	32

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4.3.2 Function Reset Control Register 0 (RMU_FRST0)

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFFFFFFFF																															
Name	DCU	CRC	SPI	I2C	USART4	USART3	USART2	USART1	Reserved	MAU	Reserved	TMR4	EMB	Reserved			TMR0_2	TMR0_1	Reserved	TMRA_5	TMRA_4	TMRA_3	TMRA_2	TMRA_1	FCM	HALL	DMA	AOS	CMP	Reserved		ADC
Access	RW	RW	RW	RW	RW	RW	RW	RW		RW		RW	RW				RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW			RW

Bit	Name	Functional Description	Access
31	DCU	DCU Reset Control ● 0b0: Function reset enabled ● 0b1: Function reset released	RW
30	CRC	CRC Reset Control ● 0b0: Function reset enabled ● 0b1: Function reset released	RW
29	SPI	SPI Reset Control ● 0b0: Function reset enabled ● 0b1: Function reset released	RW
28	I2C	I2C Reset Control ● 0b0: Function reset enabled ● 0b1: Function reset released	RW
27	USART4	USART4 Reset Control ● 0b0: Function reset enabled ● 0b1: Function reset released	RW
26	USART3	USART3 Reset Control ● 0b0: Function reset enabled ● 0b1: Function reset released	RW
25	USART2	USART2 Reset Control ● 0b0: Function reset enabled ● 0b1: Function reset released	RW
24	USART1	USART1 Reset Control ● 0b0: Function reset enabled ● 0b1: Function reset released	RW
23	*Reserved*	*Reads as 1, Write as 1*	-
22	MAU	MAU Reset Control ● 0b0: Function reset enabled ● 0b1: Function reset released	RW
21	*Reserved*	*Reads as 1, Write as 1*	-

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Bit	Name	Functional Description	Access
20	TMR4	Timer4 Reset Control ● 0b0: Function reset enabled ● 0b1: Function reset released	RW
19	EMB	EMB Reset Control ● 0b0: Function reset enabled ● 0b1: Function reset released	RW
18:16	*Reserved*	*All bits read as 1, Write as 1*	-
15	TMR0_2	Timer0 Unit 2 Reset Control ● 0b0: Function reset enabled ● 0b1: Function reset released	RW
14	TMR0_1	Timer0 Unit 1 Reset Control ● 0b0: Function reset enabled ● 0b1: Function reset released	RW
13	*Reserved*	*Reads as 1, Write as 1*	-
12	TMRA_5	TimerA Unit 5 Reset Control ● 0b0: Function reset enabled ● 0b1: Function reset released	RW
11	TMRA_4	TimerA Unit 4 Reset Control ● 0b0: Function reset enabled ● 0b1: Function reset released	RW
10	TMRA_3	TimerA Unit 3 Reset Control ● 0b0: Function reset enabled ● 0b1: Function reset released	RW
9	TMRA_2	TimerA Unit 2 Reset Control ● 0b0: Function reset enabled ● 0b1: Function reset released	RW
8	TMRA_1	TimerA Unit 1 Reset Control ● 0b0: Function reset enabled ● 0b1: Function reset released	RW
7	FCM	FCM Reset Control in CMU ● 0b0: Function reset enabled ● 0b1: Function reset released	RW
6	HALL	HALL Reset Control ● 0b0: Function reset enabled ● 0b1: Function reset released	RW
5	DMA	DMA Reset Control ● 0b0: Function reset enabled ● 0b1: Function reset released	RW
4	AOS	AOS Reset Control ● 0b0: Function reset enabled ● 0b1: Function reset released	RW

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Bit	Name	Functional Description	Access
3	CMP	CMP Reset Control ● 0b0: Function reset enabled ● 0b1: Function reset released	RW
2:1	*Reserved*	*All bits read as 1, Write as 1*	-
0	ADC	ADC Reset Control ● 0b0: Function reset enabled ● 0b1: Function reset released	RW

Note

The reset of the following registers is not controlled by the register RMU_FRST0:

- USART1_NFC, TMR_SYNENR

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4.3.3 Reset Flag Register 0 (RMU_RSTF0)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000XXXX (the reset value varies depending on the reset method)																															
Name	Reserved																CLRF	MULTIRF	XTALERF	LKUPRF	Reserved	RAMPERF	Reserved	SWRF	CKFERF	SWDRF	WDRF	PVD2RF	PVD1RF	BORF	PINRF	PORF
Access																	RW	RW	RW	RW		RW		RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15	CLRF	Clear Reset Flag Write 1 to reset the flag, write 0 has no effect; read always returns 0. **Note** The set action must be performed after RMU_RSTF0 is read.	RW
14	MULTIRF	2 or more Reset Occurrence Flags Set by hardware when two or more resets occur. Clear by setting CLRF. Read: ● 0b0: Two or more resets did not occur ● 0b1: Two or more resets occurred	RW
13	XTALERF	XTAL Error Reset Flag Set by hardware when a XTAL error reset occurs. Clear by setting CLRF. Read: ● 0b0: No reset occurred ● 0b1: Reset occurred	RW
12	LKUPRF	Cortex-M4 Lockup Reset Flag Set by hardware when a Cortex-M4 Lockup reset occurs. Clear by setting CLRF. Read: ● 0b0: No reset occurred ● 0b1: Reset occurred	RW
11	*Reserved*	-	-
10	RAMPERF	RAM Parity Error Reset Flag Set by hardware when a RAM parity error reset occurs. Clear by setting CLRF. Read: ● 0b0: No reset occurred ● 0b1: Reset occurred	RW

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Bit	Name	Functional Description	Access
9	*Reserved*	-	-
8	SWRF	Software Reset Flag Set by hardware when a software reset occurs. Clear by setting CLRF. Read: ● 0b0: No reset occurred ● 0b1: Reset occurred	RW
7	CKFERF	Clock Frequency Error Reset Flag Set by hardware when a clock frequency error reset occurs. Clear by setting CLRF. Read: ● 0b0: No reset occurred ● 0b1: Reset occurred	RW
6	SWDRF	Special Watchdog Reset Flag Set by hardware when a special watchdog reset occurs. Clear by setting CLRF. Read: ● 0b0: No reset occurred ● 0b1: Reset occurred	RW
5	WDRF	Watchdog Reset Flag Set by hardware when a watchdog reset occurs. Clear by setting CLRF. Read: ● 0b0: No reset occurred ● 0b1: Reset occurred	RW
4	PVD2RF	Programmable Voltage Detection 2 Reset Flag Set by hardware when a programmable voltage detection 2 reset occurs. Clear by setting CLRF. Read: ● 0b0: No reset occurred ● 0b1: Reset occurred	RW
3	PVD1RF	Programmable Voltage Detection 1 Reset Flag Set by hardware when a programmable voltage detection 1 reset occurs. Clear by setting CLRF. Read: ● 0b0: No reset occurred ● 0b1: Reset occurred	RW

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Bit	Name	Functional Description	Access
2	BORF	Brown-out Reset Flag Set by hardware when a brown-out reset occurs. Clear by setting CLRF. Read: ● 0b0: No reset occurred ● 0b1: Reset occurred	RW
1	PINRF	NRST Pin Reset Flag Set by hardware when a pin reset occurs. Clear by setting CLRF. Read: ● 0b0: No reset occurred ● 0b1: Reset occurred	RW
0	PORF	Power-on Reset Flag Set by hardware when a power-on reset occurs. Clear by setting CLRF. Read: ● 0b0: No reset occurred ● 0b1: Reset occurred	RW

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5 Clock Module Unit (CMU)

5.1 Introduction

The clock control unit provides a series of clock functions with different frequencies, including: an external high-speed oscillator, one PLL clock, an internal high-speed oscillator, an internal medium-speed oscillator, an internal low-speed oscillator, a clock prescaler, clock multiplexing, and clock gating circuit.

The clock control unit also provides a clock frequency measurement function. The clock frequency measurement circuit (FCM) monitors and measures the measurement target clock using the measurement reference clock. An interrupt or reset occurs when the setting range is exceeded.

AHB, APB, and Cortex-M4 clocks are derived from the System Clock. The maximum operating clock frequency of the System Clock can reach 120MHz, with 5 selectable clock sources:

1. External High-speed Oscillator (XTAL)
2. PLL Clock (PLL)
3. Internal High-speed Oscillator (HRC)
4. Internal Medium-speed Oscillator (MRC)
5. Internal Low-speed Oscillator (LRC)

For each clock source, it can be individually turned on and off when not in use to reduce power consumption. SWDT uses the internal low-speed oscillator as its counting clock source.

5.2 Features

Table 5-1 Clock Source Main Features

Clock Source	Specifications
External High-speed Oscillator (XTAL)	Crystal frequency range: 4-24MHz External clock input: Up to 24MHz Oscillator fault detection function
PLL Clock	Input clock: external high-speed oscillator or internal high-speed oscillator PLL input clock division: 1/2/4 division PFD input clock frequency = Input clock / PLL input clock division, with a frequency range of 4MHz-8MHz PLL multiplication factor: 80-120 times VCO oscillation frequency: 320MHz-480MHz PLLP output division ratio: arbitrary division from 2 to 16 PLLQ output division ratio: arbitrary division from 2 to 16 PLLP output frequency = (Input clock / PLL input clock division factor) * PLLN multiplication factor / PLLP clock division factor PLLQ output frequency = (Input clock / PLL input clock division factor) * PLLN multiplication factor / PLLQ clock division factor
Internal High-speed Oscillator (HRC)	Frequency: 12MHz Configure HRC division via the CMU_HRCCFGR register
Internal Medium-speed Oscillator (MRC)	Frequency: 8MHz
Internal Low-speed Oscillator (LRC)	Frequency: 32.768kHz Can be used as the counting clock for SWDT and Timer0

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5.3 Functional Description

5.3.1 System Block Diagram

5.3.1.1 Clock System Block Diagram

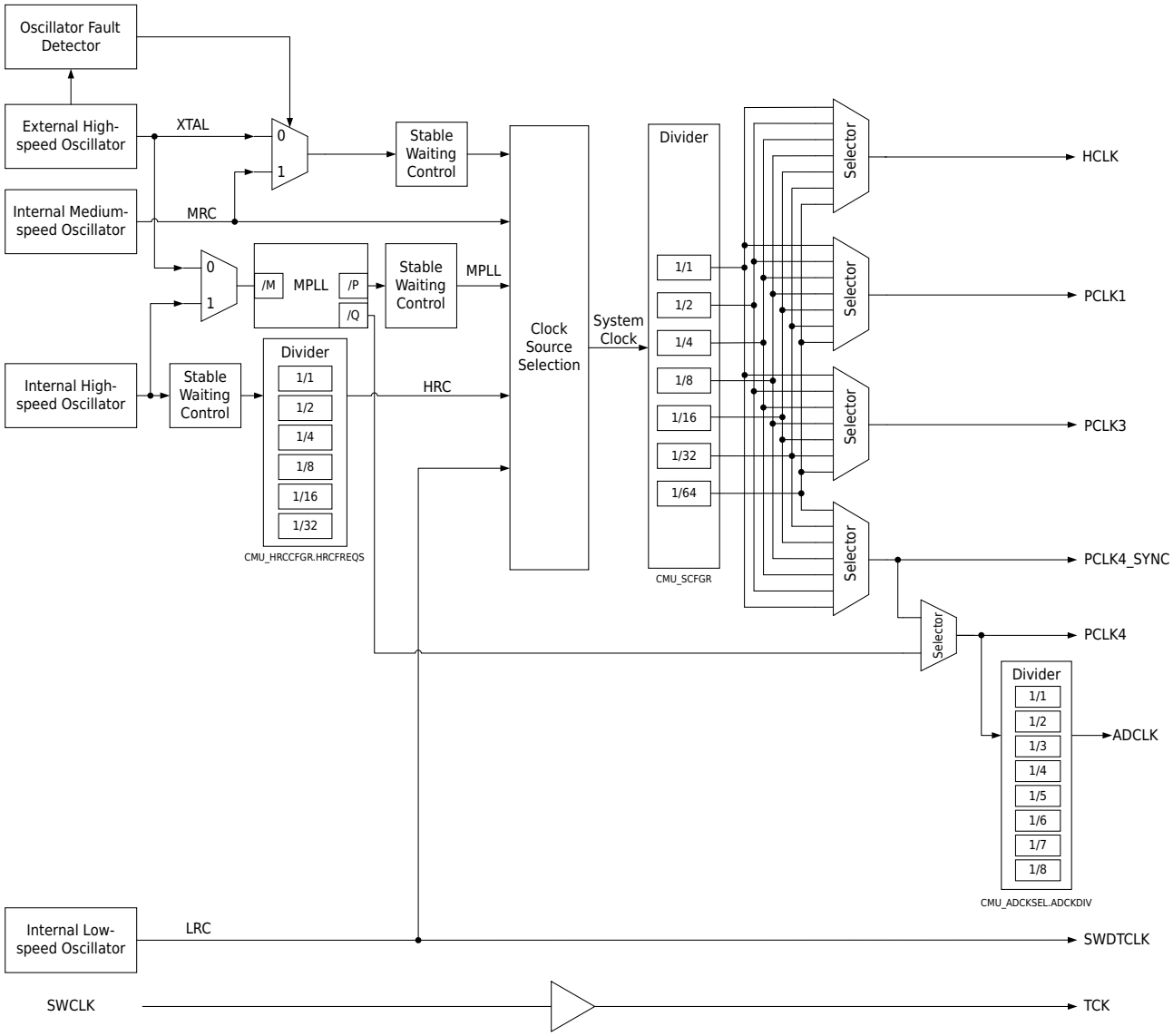

Figure 5-1 Clock System Block Diagram

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5.3.1.2 Clock Frequency Measurement Block Diagram

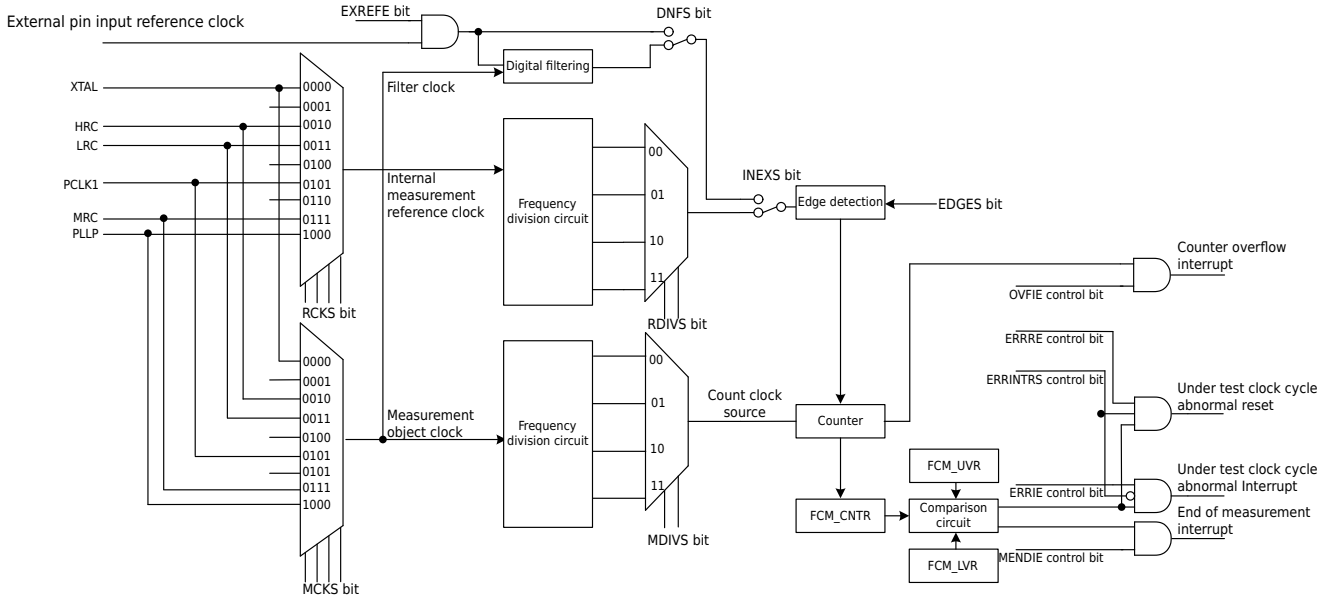

Figure 5-2 Clock Frequency Measurement Block Diagram

5.3.2 Working Clock Specifications

Table 5-2 Specifications for Each Internal Clock

Clock	Scope of Action	Specifications
HCLK	CPU, DMA, EFM, SRAMH, SRAM1, GPIO, INTC, CACHE, DCU, CRC, CMU, PWC, MAU	Maximum frequency: 120MHz Configured by the CMU_SCFGR.HCLKS bit Selectable system clock division: 1, 2, 4, 8, 16, 32, 64
PCLK1	USART_n (n=1-4), SPI, Timer0_n (n=1-2), Timer4, TimerA_n (n=1-5), EMB, AOS, HALL	Maximum frequency: 120MHz Configured by the CMU_SCFGR.PCLK1S bit Selectable system clock division: 1, 2, 4, 8, 16, 32, 64
PCLK3	I2C, SWDT, WDT, CMPn (n=1-3), FCM	Maximum frequency: 120MHz Configured by the CMU_SCFGR.PCLK3S bit Selectable system clock division: 1, 2, 4, 8, 16, 32, 64
PCLK4_SYNC	ADC Synchronous Clock	Maximum frequency: 120MHz Configured by the CMU_SCFGR.PCLK4S bit Selectable system clock division: 1, 2, 4, 8, 16, 32, 64
PCLK4	ADC Interface Clock	Configured by the CMU_ADCKSEL.ADCKSEL bit Selectable clock PCLK4_SYNC or PLLQ
ADCLK	ADC Sampling Conversion Clock	Maximum frequency: 80MHz Configured by the CMU_ADCKSEL.ADCKDIV bit Selectable dividers for PCLK4_SYNC: 1, 2, 3, 4, 5, 6, 7, 8 (When the PCLK4 clock source is PLLQ, dividers are not supported.)

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Clock	Scope of Action	Specifications
STCLK	SYSTICK Timer External Reference Clock	Internal low-speed oscillator clock: 32.768kHz Configured by the CLKSOURCE bit in the SYSTICK Control and Status Register of the CPU.
SWDTCLK	SWDT Counter Clock	Internal low-speed oscillator clock: 32.768kHz
TCK	SWD Clock	Maximum frequency: 20MHz

Among the respective clocks, the following rule must be observed:

1. HCLK frequency≥PCLK1, PCLK3, PCLK4 frequency

5.3.3 Crystal Oscillator Circuit

5.3.3.1 External High-speed Oscillator

5.3.3.1.1 Oscillator Mode

External high-speed oscillator provides a more accurate clock source for the system clock.

XTAL is turned on and off through the CMU_XTALCR.XTALSTP bit.

The CMU_OSCSTBSR.XTALSTBF bit indicates whether the external high-speed oscillator is stable or not. The stabilization time is configured through register CMU_XTALSTBCR. CMU_XTALSTBCR must be set at a stabilization time greater than or equal to that required by the crystal oscillator manufacturer.

The circuit constant of the crystal oscillator varies with the parasitic capacitance of the crystal oscillator and the installed circuit, so it must be discussed carefully with the crystal oscillator manufacturer. Oscillator features are closely associated with the user's circuit board design, and crystal oscillator and load capacitance must be as close to the oscillator pin as possible to minimize output distortion and oscillation stabilization time. The load capacitance value must be adjusted appropriately depending on the oscillator selected. Signal lines must not be routed near the oscillation circuit, otherwise normal oscillation may be disrupted by inductance.

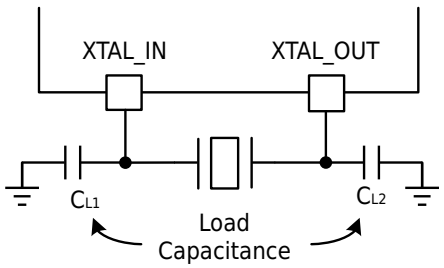

Figure 5-3 External High-Speed Oscillator Connection Example

5.3.3.1.2 Clock Input Mode

An external clock source must be provided in clock input mode. This mode is selected by setting the CMU_XTALCFGR.XTALMS bit to 1 and the CMU_XTALCR.XTALSTP bit to 0. An external clock signal with a duty cycle of approximately 50% must be used to drive the XTAL_IN pin. At this time, the XTAL_OUT pin can be configured as GPIO according to register settings.

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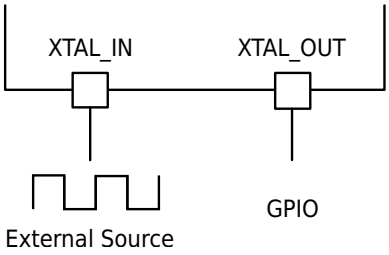

Figure 5-4 External Clock Input Connection Example

5.3.3.2 External High-speed Oscillator Fault Detection

Oscillator fault detection is used to detect whether the oscillation of the external high-speed oscillator (XTAL) is normal.

Open or close by register CMU_XTALSTDCR.XTALSTDE bit.

After reset release, the external high-speed oscillator stops oscillating, and the external high-speed oscillator fault detection function is disabled. To enable the external high-speed oscillator fault detection function, the external high-speed oscillator must be oscillating, and after waiting for the external high-speed oscillator to stabilize (CMU_OSCSTBSR.XTALSTBF is 1), it can be turned on through the CMU_XTALSTDCR.XTALSTDE bit.

Regardless of whether the system clock selects XTAL or a PLL with XTAL as the input source, the XTAL oscillation fault detection function must be enabled.

When the PLL selects the XTAL clock as the input source, the only available option is to generate a reset upon XTAL oscillation failure.

Since oscillator fault detection detects abnormal oscillation of the oscillator caused by external factors, the oscillator oscillation fault detection function should be disabled when stopping the external high-speed oscillator through software or transitioning to STOP mode.

When enabling XTAL oscillator fault detection (CMU_XTALSTDCR.XTALSTDE=1) from a disabled state (CMU_XTALSTDCR.XTALSTDE=0), the following precautions must be observed:

- Write 0 to the corresponding bits of the following register: CMU_XTALSTDCR.XTALSTDRE=0, CMU_XTALSTDCR.XTALSTDIE=0.
- Ensure XTAL is not used as the system clock source or PLL clock source.

After completing the above confirmation, configure and use the external high-speed oscillator fault detection by following these steps:

1. Set CMU_XTALSTDCR.XTALSTDE to 1 and maintain it for at least 1μs;
2. Write 0 to CMU_XTALSTDSR.XTALSTDF to clear the oscillator fault flag;
3. Configure the registers related to the XTAL oscillator fault response as required;
4. Configure the clock source as required.

When XTAL is used as the system clock source or PLL clock source, the software should not disable the MRC. Otherwise, stopping the oscillator and then switching to the MRC may cause unpredictable behavior.

If the external high-speed oscillator fails, the action waveform is shown in the following figure. For the operation procedure, please refer to "XTAL Fault Detection Action Detected".

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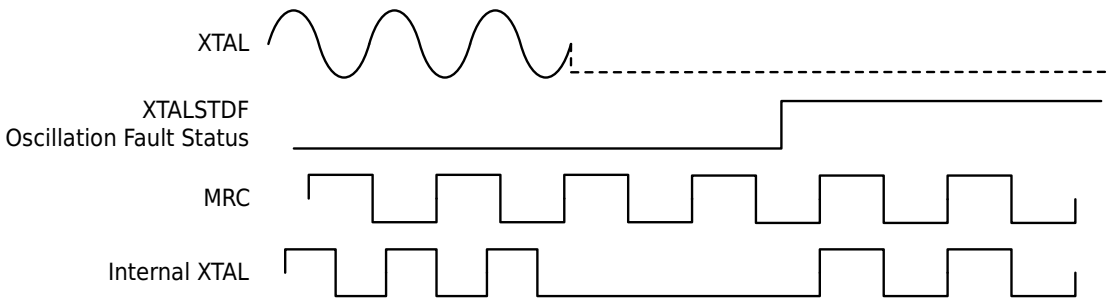

Figure 5-5 External High-speed Oscillator Fault Detection Example

5.3.3.2.1 Action upon Detection of XTAL Fault

When an external high-speed oscillator oscillation fault is detected, if the system clock selects the external high-speed oscillator as the system clock, the system clock will automatically switch to MRC.

When an oscillation fault of the external high-speed oscillator is detected, the EMB brake can be triggered. For detailed information, refer to the description in the "Emergency Brake Module (EMB) " chapter.

When the system clock is selected as XTAL and an XTAL oscillation fault is detected, the action example is as follows:

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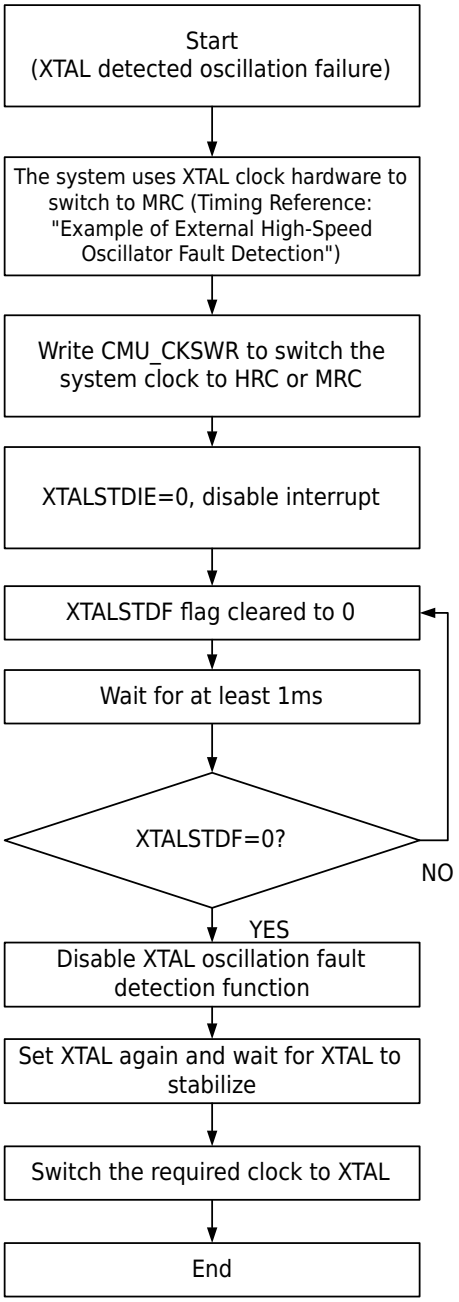

Figure 5-6 System Clock Selected as XTAL, Example of Detecting XTAL Oscillation Fault

5.3.3.2.2 Interrupt Reset Generated upon Detection of XTAL Oscillation Fault

The XTAL oscillation fault interrupt can be configured as a maskable interrupt or a non-maskable interrupt. For more information, please refer to the "Interrupt Controller (INTC) " chapter.

When the XTAL oscillation fault is configured as a reset, if an XTAL oscillation fault is detected, the chip will generate a reset. Please refer to the "Reset Module Unit (RMU) " chapter for reset actions.

Notice

With the interrupt/reset function enabled, if you need to enable the XTAL oscillation fault detection function again after disabling the XTAL oscillation fault detection function, please refer to the relevant description in the "External High-speed Oscillator Fault Detection" chapter for the operation steps.

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5.3.4 Internal RC Clock

5.3.4.1 HRC Clock

HRC clock signals are generated by the internal high-speed oscillator and can be directly used as the system clock or as PLL input. The frequency of HRC can be configured via CMU_HRCCFGR to 12MHz and its divided frequencies.

The advantage of the HRC oscillator is its low cost (no external components are required). In addition, its startup speed is faster than that of the XTAL crystal oscillator. However, even after calibration, its accuracy is not as good as that of an external crystal oscillator.

Frequency Calibration

Due to differences in production processes, the RC oscillator frequency of different chips varies. Therefore, each device is factory-calibrated to ensure accuracy. Please refer to the "Electrical Specifications-Operating Conditions-Internal Clock Source Characteristics-HRC" chapter of the Datasheet.

If the application is affected by temperature changes, this may also affect the accuracy of the RC oscillator.

CMU_OSCSTBSR.HRCSTBF indicates whether HRC is stable. At startup, hardware sets this bit to 1 before HRC can be used.

HRC can be turned on or off through CMU_HRCCR.HRCSTP bit.

5.3.4.2 MRC Clock

The MRC clock signal is generated by an internal 8MHz medium-speed oscillator and can be directly used as the system clock.

The advantage of the MRC oscillator is its fast startup speed.

Frequency Calibration

Due to differences in production processes, the RC oscillator frequency of different chips varies. Therefore, each device is factory-calibrated to ensure accuracy. Please refer to the "Electrical Specifications-Operating Conditions-Internal Clock Source Characteristics-MRC" chapter in the Datasheet.

If the application is affected by temperature changes, this may also affect the accuracy of the RC oscillator.

MRC can be turned on or off through the CMU_MRCCR.MRCSTP bit.

The MRC clock can also be used as a backup clock source in case of XTAL crystal oscillator fault. Please refer to " Action upon Detection of XTAL Fault".

5.3.4.3 LRC Clock

The LRC clock signal is generated by the 32.768kHz internal low-speed oscillator and can be used directly as the system clock.

The LRC oscillator features a fast start-up speed.

Frequency Calibration

Due to differences in production processes, the RC oscillator frequency of different chips varies. Therefore, each device is factory-calibrated to ensure accuracy. Please refer to the "Electrical Specifications-Operating Conditions-Internal Clock Source Characteristics-LRC" chapter in the Datasheet.

If the application is affected by voltage or temperature changes, this may also affect the accuracy of the RC oscillator.

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LRC can be turned on or off through the CMU_LRCCR.LRCSTP bit.

5.3.5 PLL Clock

This product is equipped with one PLL:

- The input clock (F_{in}) is uniformly configured via the CMU_PLLCFGR.PLLSRC bit, with the option to select the XTAL or HRC oscillator.

  The PLL input clock division factor (DIVM) is configured by CMU_PLLCFGR.PLLM. For example, when CMU_PLLCFGR.PLLM = 0b01, DIVM = 2.

  The PLLN multiplication factor (DIVN) is configured by CMU_PLLCFGR.PLLN. For example, when CMU_PLLCFGR.PLLN = 0b1001110, DIVN = 80.

  The VCO operating frequency range (F_{vco}) is configured by CMU_PLLCFGR.VCOIT. The frequency calculation formula is as follows:

  $$F_{VCO} = \frac{F_{in}}{DIVM} \times DIVN$$

- The PLL has two output clocks: PLLP and PLLQ. The PLLP clock can serve as the system clock, and the PLLQ clock can be used to generate the ADC clock. The division factors can be configured independently:
  - The PLLP clock division factor (DIVP) is configured by CMU_PLLCFGR.PLLP. For example, when CMU_PLLCFGR.PLLP = 0b0010, DIVP = 3.

    The frequency calculation formula is as follows:

    $$F_{PLLP} = \frac{F_{VCO}}{DIVP}$$

  - The PLLQ clock division factor (DIVQ) is configured by CMU_PLLCFGR.PLLQ. For example, when CMU_PLLCFGR.PLLQ = 0b0010, DIVQ = 3.

    The frequency calculation formula is as follows:

    $$F_{PLLQ} = \frac{F_{VCO}}{DIVQ}$$

Notice

1. Configure the PLL after the HRC or XTAL oscillator is stable.
2. Since PLL configuration parameters cannot be changed after the PLL is enabled, it is recommended to configure the PLL first and then enable it.
3. When entering STOP mode, the PLL will be disabled by hardware.

5.3.6 Clock Switching Steps

After system reset, the default system clock is MRC. Switch the clock source by setting the CMU_CKSW register. Please refer to "Clock Source Switch" for switching steps. Clock sources can only be switched from one to another when the target clock source is stable.

The waiting period of Flash should be configured correctly to prevent the system clock frequency from being larger than the maximum operating frequency of Flash. For detailed configuration, please refer to the "CPU Clock and Flash Read Time Relationship" section of the "Embedded Code Flash Memory (EFM)".

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Clock Source Switching

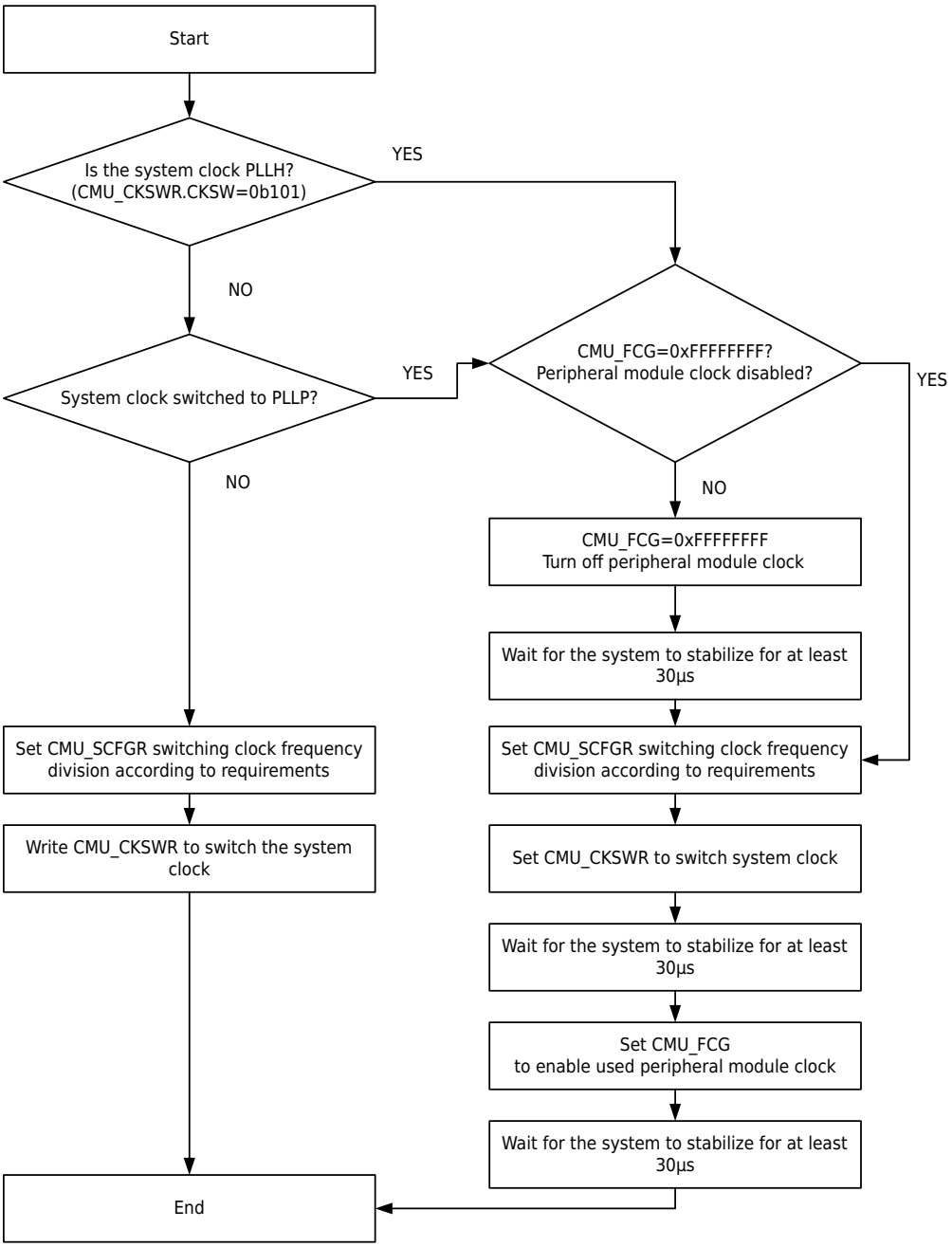

Figure 5-7 Clock Source Switching Flowchart

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Clock Division Switching

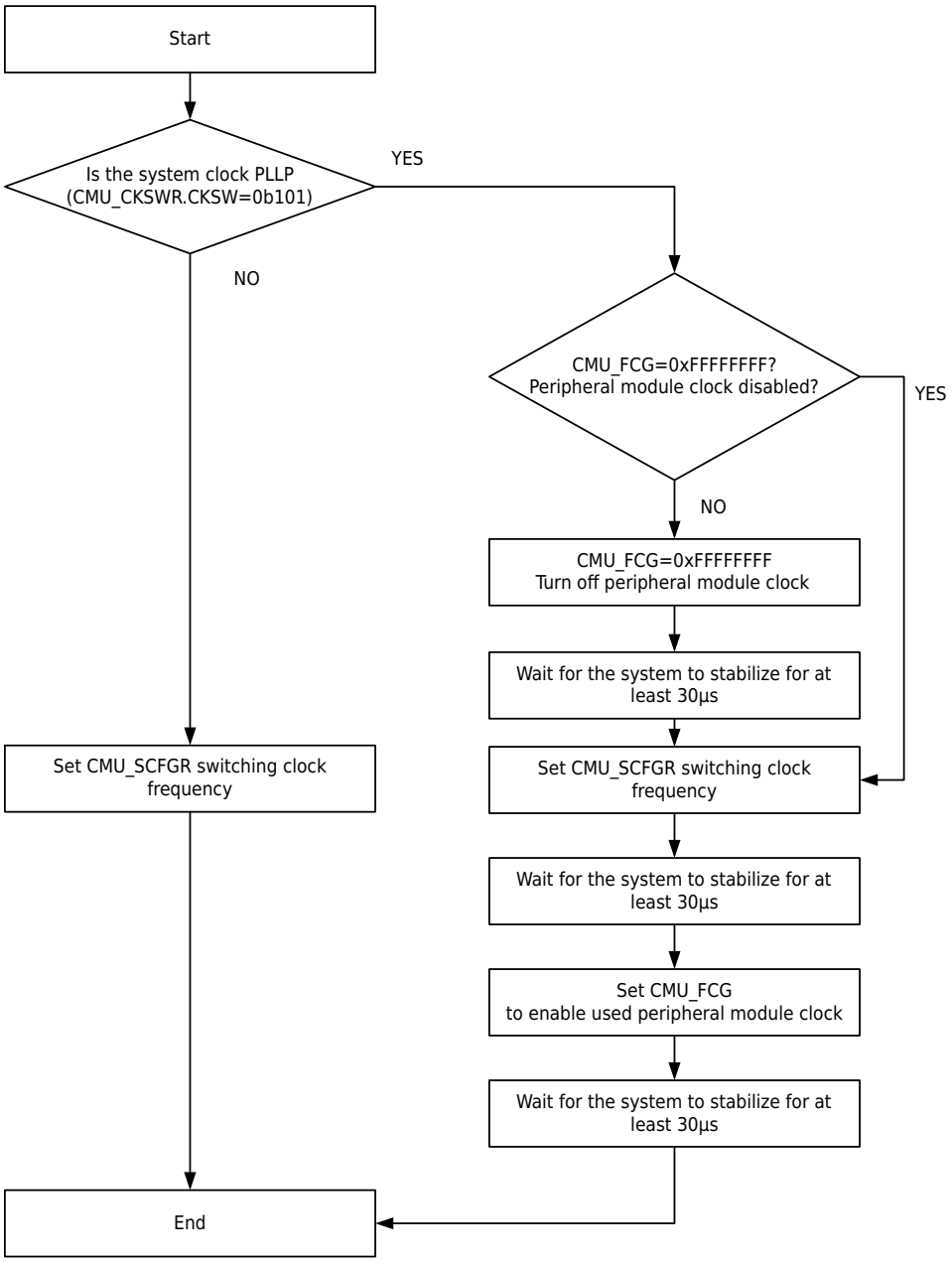

Figure 5-8 Clock Division Switching Flowchart

5.3.7 Clock Output Function

Users can output different clock sources to the MCO pin through a configurable pre-divider (1, 2, 4, 8,..., 128 division):

- HRC Clock
- MRC Clock
- LRC Clock
- XTAL Clock
- PLLP Clock
- PLLQ Clock
- System Clock

The desired clock source is selected by the CMU_MCOCFGR.MCOSEL bit.

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The output clock of MCO should not exceed 40MHz (maximum I/O speed).

5.3.8 Clock Frequency Measurement

5.3.8.1 Clock Frequency Measurement Function

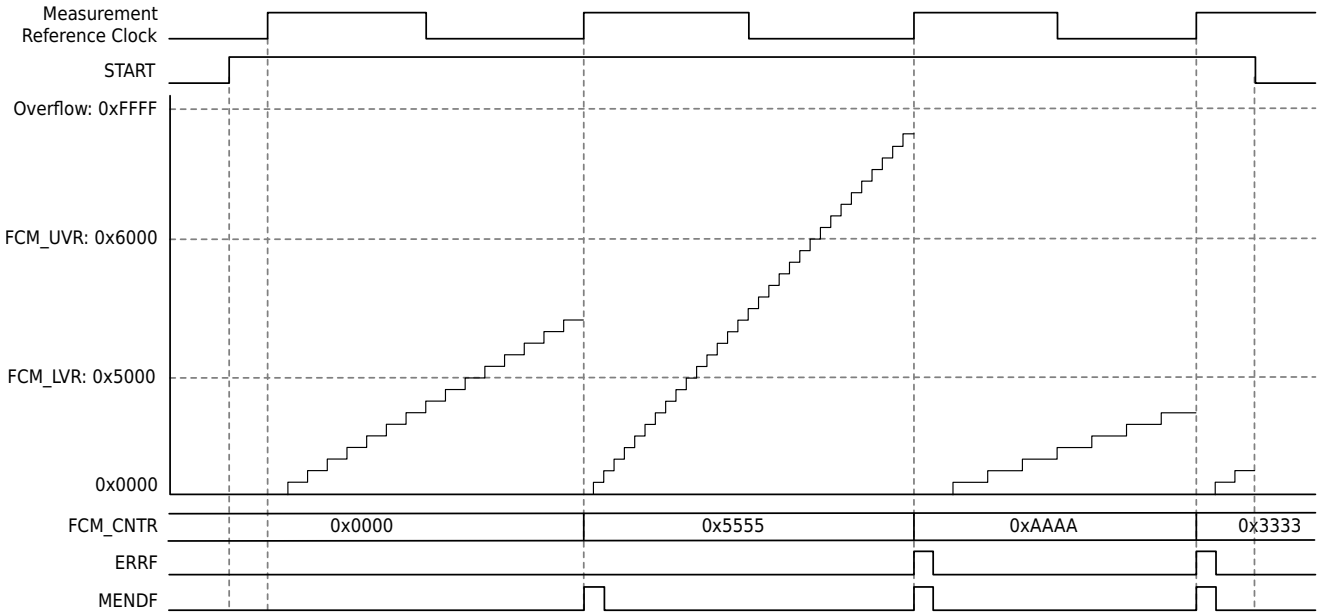

Figure 5-9 Clock Frequency Measurement Timing Diagram

- Select the reference clock and the clock to be measured, the clock division, and the active edge of the reference clock using FCM_MCCR/FCM_RCCR.
- After writing 1 to the FCM_STR.START bit, the active edge selected by the EDGES bit is detected, and the counter starts counting up.
- When the active edge selected by the next EDGES bit of the reference clock is detected, the value of the counter is saved to the FCM_CNTR register and compared with the set value of FCM_LVR/ FCM_UVR. When FCM_LVR ≤ FCM_CNTR ≤ FCM_UVR, the clock frequency measurement is normal. When FCM_LVR > FCM_CNTR or FCM_CNTR > FCM_UVR, the clock frequency is abnormal, and an interrupt or reset can occur based on the ERRINTRS/ERRRE/ERRIE settings.
- After the START bit of FCM_STR is written to 0, the counter counting is stopped and cleared.
- When FCM_LVR > FCM_CNTR or FCM_CNTR > FCM_UVR, the clock frequency is abnormal, and the abnormal source is FCM_FERR.

Note

Before configuring FCM_STR.START to 1 to start monitoring, if the measured clock has completely stopped oscillating, the FCM detection will be invalid and no error will be reported.

5.3.8.2 Digital Filtering Function

External pin input reference clock FCMREF has digital filtering function. Digital filtering function performs 3 samples based on the sampling clock selected by the DNFS bit. If the levels of the 3 samples are the same, this level is sent internally.

The digital filtering function can set the digital filtering function to be active or inactive and the sampling clock.

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5.3.8.3 Interrupt/Reset Function

The clock frequency measurement circuit supports three interrupt requests:

- Frequency abnormal interrupt
- Frequency measurement end interrupt
- Counter overflow interrupt

The clock frequency measurement circuit supports one reset request:

- Frequency abnormal reset

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5.4 Register Description

5.4.1 Register List

FCM base address: 0x40048400

Table 5-3 Clock Frequency Measurement (FCM) Register Offset

Offset	Register	Description	Width
0x00	FCM_LVR	FCM Lower Limit Control Register	32
0x04	FCM_UVR	FCM Upper Limit Control Register	32
0x08	FCM_CNTR	FCM Counter Register	32
0x0C	FCM_STR	FCM Start Control Register	32
0x10	FCM_MCCR	FCM Measurement Control Register	32
0x14	FCM_RCCR	FCM Reference Control Register	32
0x18	FCM_RIER	FCM Reset Interrupt Control Register	32
0x1C	FCM_SR	FCM Flag Register	32
0x20	FCM_CLR	FCM Flag Clear Register	32

CMU base address 1: 0x40054400

Table 5-4 Clock Module Unit (CMU) Register Offset

Offset	Register	Description	Width
0x00	CMU_ADCKSEL	CMU ADC Clock Config Register	16
0x04	CMU_XTALSTDSR	CMU XTAL Clock Stop Dectect Status Register	8
0x08	CMU_SCFGR	CMU Clock Divider Config Register	32
0x0C	CMU_CKSWR	CMU System Clock Source Switch Register	8
0x10	CMU_XTALCR	CMU XTAL Control Register	8
0x14	CMU_XTALCFGR	CMU XTAL Config Register	8
0x15	CMU_XTALSTBCR	CMU XTAL Stable Control Register	8
0x18	CMU_HRCCR	CMU HRC Control Register	8
0x20	CMU_OSCSTBSR	CMU Clock Source Stable Status Register	8
0x24	CMU_MCOCFGR	CMU MCO Clock Output Config Register	8
0x28	CMU_XTALSTDCR	CMU XTAL Clock Stop Dectect Control Register	8
0x30	CMU_FCG	CMU Function Clock Control Register	32
0x3C	CMU_LRCCR	CMU LRC Control Register	8

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Offset	Register	Description	Width
0x40	CMU_MRCCR	CMU MRC Control Register	8
0x44	CMU_PLLCFGR	CMU PLL Config Register	32
0x48	CMU_PLLCR	CMU PLL Control Register	8

EFM base address: 0x40010400

Table 5-5 Embedded Code Flash Memory (EFM) Register Offset

Offset	Register	Description	Width
0x0288	CMU_HRCCFGR	CMU HRC Config Register	8

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5.4.2 CMU XTAL Config Register (CMU_XTALCFGR)

Offset	Bit Position							
0x14	7	6	5	4	3	2	1	0
Reset	0x02							
Name	Reserved	XTALMS	FREQSEL		Reserved	NFBPS	XTALDRV	
Access		RW	RW			RW	RW	

Bit	Name	Functional Description	Access
7	*Reserved*	-	-
6	XTALMS	XTAL Mode Selection Bit ● 0b0: Oscillator mode ● 0b1: External clock input mode **Notice** When this bit is set to 1, the following functions will be invalid: ● CMU_XTALCFGR.REQSEL ● CMU_XTALCFGR.NFBPS ● CMU_XTALCFGR.XTALDRV ● CMU_XTALSTBCR.XTALSTB ● CMU_XTALSTDCR.XTALSTDE	RW
5:4	FREQSEL	XTAL Frequency Selection ● 0b00: 4MHz≤Crystal oscillator frequency<8MHz ● 0b01: 8MHz≤Crystal oscillator frequency<16MHz ● 0b10: 16MHz≤Crystal oscillator frequency<20MHz ● 0b11: 20MHz≤Crystal oscillator frequency≤24MHz	RW
3	*Reserved*	-	-
2	NFBPS	Filter Disable Control Bit ● 0b0: XTAL clock passes through the built-in filter circuit ● 0b1: Built-in filter circuit is disabled	RW
1:0	XTALDRV	XTAL Drive Capability Selection ● 0b00: Ultra-low drive capability ● 0b01: Low drive capability ● 0b10: Medium drive capability ● 0b11: High drive capability (recommended value) **Notice** Select the appropriate drive capability based on the crystal oscillator characteristics, load capacitance, and PCB parasitic parameters. Stronger drive capability results in higher power consumption; weaker drive capability results in lower power consumption.	RW

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5.4.3 CMU XTAL Stable Control Register (CMU_XTALSTBCR)

Offset	Bit Position							
0x15	7	6	5	4	3	2	1	0
Reset	0x00							
Name	Reserved					XTALSTB		
Access						RW		

Bit	Name	Functional Description	Access
7:3	*Reserved*	-	-
2:0	XTALSTB	XTAL Stabilization Time Selection ● 0b000: 2^8*XTAL periods ● 0b001: 2^9*XTAL periods ● 0b010: 2^{10}*XTAL periods ● 0b011: 2^{11}*XTAL periods ● 0b100: 2^{13}*XTAL periods ● 0b101: 2^{15}*XTAL periods ● 0b110: 2^{16}*XTAL periods ● 0b111: 2^{17}*XTAL periods **Note** This register can only be configured when CMU_XTALCR.XTALSTP=1 and CMU_OSCSTBSR.XTALSTBF=0. When CMU_XTALCFGR.XTALMS=1, this waiting time is ignored.	RW

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5.4.4 CMU XTAL Control Register (CMU_XTALCR)

Offset	Bit Position							
0x10	7	6	5	4	3	2	1	0
Reset	0x01							
Name	Reserved							XTALSTP
Access								RW

Bit	Name	Functional Description	Access
7:1	*Reserved*	-	-
0	XTALSTP	XTAL Oscillator Start/Stop Control ● 0b0: XTAL oscillator oscillating ● 0b1: XTAL oscillator stopped	RW

Notice

1. When XTAL is selected as system clock or PLL clock source, writing 1 to XTALSTP to stop XTAL oscillator is prohibited.
2. Software sets the XTAL oscillator to oscillate, and after confirming that the XTAL oscillator is stable through the XTALSTBF bit, the system can enter STOP mode or software sets the XTAL oscillator to stop.
3. The XTAL oscillator is set to stop by software, and the XTAL oscillator can be entered into STOP mode or restarted after confirming that the XTAL oscillator is stopped through the XTALSTBF bit.

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5.4.5 CMU XTAL Clock Stop Dectect Control Register (CMU_XTALSTDCR)

Offset	Bit Position							
0x28	7	6	5	4	3	2	1	0
Reset	0x00							
Name	XTALSTDE	Reserved				XTALSTDRIS	XTALSTDRE	XTALSTDIE
Access	RW					RW	RW	RW

Bit	Name	Functional Description	Access
7	XTALSTDE	XTAL Clock Stop Dectect Function Enabled ● 0b0: XTAL clock stop dectect disabled ● 0b1: XTAL clock stop dectect enabled **Note** Clock stop dectect involves detecting abnormal oscillations caused by external factors. Before entering STOP mode, please disable the clock stop dectect function.	RW
6:3	*Reserved*	-	-
2	XTALSTDRIS	XTAL Clock Stop Dectect Reset Interrupt Selection ● 0b0: XTAL clock stop dectect generates an interrupt ● 0b1: XTAL clock stop dectect generates a reset **Note** When PLL select XTAL clock as the input source, they can only select the XTAL clock stop dectect to generate reset function.	RW
1	XTALSTDRE	XTAL Clock Stop Dectect Reset Enabled ● 0b0: XTAL clock stop dectect reset disabled ● 0b1: XTAL clock stop dectect reset enabled	RW
0	XTALSTDIE	XTAL Clock Stop Dectect Interrupt Enabled ● 0b0: XTAL clock stop dectect interrupt disabled ● 0b1: XTAL clock stop dectect interrupt enabled **Note** To trigger the EMB brake, the XTALSTDIE bit needs to be set to 1.	RW

Notice

When XTAL is selected as system clock or PLL clock source, XTALSTP is disabled to write "1" to stop XTAL oscillator.

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5.4.6 CMU XTAL Clock Stop Dectect Status Register (CMU_XTALSTDSR)

Offset	Bit Position							
0x04	7	6	5	4	3	2	1	0
Reset	0x00							
Name	Reserved							XTALSTDF
Access								RW

Bit	Name	Functional Description	Access
7:1	*Reserved*	-	-
0	XTALSTDF	XTAL Clock Stop Dectect Status Bit ● 0b0: XTAL clock stop not detected ● 0b1: XTAL clock stop detected Setting conditions: ● XTAL clock stop dectect under XTALSTDE=1 Clearing conditions: ● When the system clock selects a clock other than XTAL, read as 1, write as 0	RW

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5.4.7 CMU HRC Config Register (CMU_HRCCFGR)

Offset	Bit Position							
0x0288	7	6	5	4	3	2	1	0
Reset	0xFF							
Name	Reserved					HRCFREQS		
Access						RW		

Bit	Name	Functional Description	Access
7:3	*Reserved*	-	-
2:0	HRCFREQS	HRC Frequency Selection Bit	RW

HRCFREQS[2:0]	HRC Frequency
0b000	12MHz
0b001	6MHz
0b010	3MHz
0b011	1.5MHz
0b100	750kHz
0b101-111	375kHz

Note

After write protection is removed by setting the EFM_FAPRT register, this field can be modified by software.

When HRC is used as the input clock for the PLL, the frequency division here does not affect the frequency of the PLL input clock.

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5.4.8 CMU HRC Control Register (CMU_HRCCR)

Offset	Bit Position							
0x18	7	6	5	4	3	2	1	0
Reset	0x00							
Name	Reserved							HRCSTP
Access								RW

Bit	Name	Functional Description	Access
7:1	*Reserved*	-	-
0	HRCSTP	HRC Oscillator Start Stop Bit ● 0b0: HRC oscillator oscillating ● 0b1: HRC oscillator stopped	RW

Notice

1. When HRC is selected as the system clock source or PLL clock source, it is forbidden to stop the HRC clock by writing 1 to HRCSTP.
2. After software sets the HRC oscillator to oscillate, and confirms that HRC is stable through the HRCSTBF bit, the system can enter STOP mode or stop HRC.
3. After software sets HRC to stop, and confirms that HRC has stopped through the HRCSTBF bit, the system can enter STOP mode.
4. After software sets HRC to stop, and confirms that HRC has stopped through the HRCSTBF bit, a minimum waiting period of at least 1μs is required before the HRC can be restarted.

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5.4.9 CMU MRC Control Register (CMU_MRCCR)

Offset	Bit Position							
0x40	7	6	5	4	3	2	1	0
Reset	0x00							
Name	Reserved							MRCSTP
Access								RW

Bit	Name	Functional Description	Access
7:1	*Reserved*	-	-
0	MRCSTP	MRC Oscillator Start/Stop Bit ● 0b0: MRC oscillator oscillating ● 0b1: MRC oscillator stopped **Note** ● The STOP mode wake-up action when PWC_STPMCR.CKSMRC bit is 1 is set when the MRC oscillator is oscillating.	RW

Notice

1. When MRC is selected as the system clock source, stopping the MRC clock by writing 1 to MRCSTP is prohibited.
2. After software sets the MRC oscillator to oscillate, wait for 5 MRC periods before entering STOP mode or stopping the MRC.
3. The software sets the MRC to stop, and waits for 5 MRC periods before entering the STOP mode or restarting the MRC.
4. When waiting for the PLL clock to stabilize, regardless of the setting of the MRCSTP bit, MRC is forced to oscillate.

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5.4.10 CMU LRC Control Register (CMU_LRCCR)

Offset	Bit Position							
0x3C	7	6	5	4	3	2	1	0
Reset	0x00							
Name	Reserved							LRCSTP
Access								RW

Bit	Name	Functional Description	Access
7:1	*Reserved*	-	-
0	LRCSTP	LRC Oscillator Start/Stop bit ● 0b0: LRC oscillator oscillating ● 0b1: LRC oscillator stopped	RW

Notice

- When LRC is selected as the system clock source, stopping the LRC clock by writing 1 to LRCSTP is prohibited.
- After software sets the LRC oscillator to oscillate, wait for 5 LRC periods before entering STOP mode or stopping the LRC.
- The software sets the LRC to stop, and waits for 5 LRC periods before entering the STOP mode or starting the LRC again.

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5.4.11 CMU PLL Config Register (CMU_PLLCFGR)

Offset	Bit Position																													
0x44	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x35004E11																															
Name	PLLP				PLLQ				Reserved								PLLN								PLLSRC	Reserved		VCOIT	Reserved			PLLM
Access	RW				RW												RW								RW			RW				RW

Bit	Name	Functional Description	Access
31:28	PLLP	PLLP Clock Division Coefficient PLLP output clock frequency = PLL VCO frequency/PLLP ● 0b0000: Setting prohibited ● 0b0001: Division by 2 ● 0b0010: Division by 3 ● …… ● 0b1110: Division by 15 ● 0b1111: Division by 16 **Note** Write PLLP under the PLL stop condition to set the frequency of the PLLP clock.	RW
27:24	PLLQ	PLLQ Clock Division Coefficient PLLQ output clock frequency = PLL VCO frequency / PLLQ ● 0b0000: Setting prohibited ● 0b0001: Division by 2 ● 0b0010: Division by 3 ● …… ● 0b1110: Division by 15 ● 0b1111: Division by 16 **Note** Write PLLQ under the PLL stop condition to set the frequency of the PLLQ clock.	RW
23:15	*Reserved*	-	-

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Bit	Name	Functional Description	Access
14:8	PLLN	PLL Multiplication Coefficient PLL VCO frequency = PLL VCO input frequency * PLLN ● 0b1001110: 80 ● 0b1001111: 81 ● ... ● 0b1110110: 120 ● Others: Setting prohibited **Note** Used to control the multiplication coefficient for the PLL VCO. Write PLLN under the PLL stop condition. Ensure the PLL VCO frequency is between 320 MHz and 480 MHz.	RW
7	PLLSRC	PLL Input Clock Source Selection ● 0b0: Select external high-speed oscillator ● 0b1: Select internal high-speed oscillator (HRC frequency is fixed at 12MHz, unaffected by the CMU_HRCCFGR.HRCFREQS configuration)	RW
6:5	*Reserved*	-	-
4	VCOIT	VCO Output Range Selection ● 0b0: 320MHz≤Fvco<430MHz ● 0b1: 430MHz≤Fvco≤480MHz	RW
3:2	*Reserved*	-	-
1:0	PLLM	PLL Input Clock Division Coefficient ● 0b00: Division by 1 ● 0b01: Division by 2 ● 0b10: Division by 4 ● 0b11: Setting prohibited **Note** Specifies the division of the PLL input clock before the PLL's VCO. Write PLLM when the PLL is stopped. Ensure the PLL's PFD input clock frequency is between 4 MHz and 8 MHz.	RW

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5.4.12 CMU PLL Control Register (CMU_PLLCR)

Offset	Bit Position							
0x48	7	6	5	4	3	2	1	0
Reset	0x01							
Name	Reserved							PLLOFF
Access								RW

Bit	Name	Functional Description	Access
7:1	*Reserved*	-	-
0	PLLOFF	PLL Enable ● 0b0: PLL operation starts ● 0b1: PLL stops **Note** Do not set this bit to 1 when the PLL clock is used as the system clock.	RW

Notice

- When the PLL is selected as the system clock source, it is prohibited to stop the PLL clock by writing 1 to PLLOFF.
- Software initiates the PLL action, and after confirming PLL stabilization via the PLLSTBF bit, the system can enter STOP mode or software-configured stop of PLL.
- Software stops the PLL, and after confirming via the PLLSTBF bit that the PLL has stopped, the system can enter Stop mode, or restart the PLL.
- When the PLL selects the XTAL oscillator as the clock source, set the PLL action to start after confirming that the XTAL oscillator is stable through the XTALSTBF bit. When the PLL selects HRC as the clock source, the PLL action can be set to start after confirming that HRC is stable through the HRCSTBF bit.

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5.4.13 CMU Clock Source Stable Status Register (CMU_OSCSTBSR)

Offset	Bit Position							
0x20	7	6	5	4	3	2	1	0
Reset	0x00							
Name	Reserved		PLLSTBF	Reserved	XTALSTBF	Reserved		HRCSTBF
Access			RO		RO			RO

Bit	Name	Functional Description	Access
7:6	*Reserved*	-	-
5	PLLSTBF	PLL Stability Flag Bit ● 0b0: PLL is stopped or unstable ● 0b1: PLL is stable	RO
4	*Reserved*	-	-
3	XTALSTBF	XTAL Stability Flag Bit ● 0b0: XTAL is stopped or unstable ● 0b1: XTAL is stable	RO
2:1	*Reserved*	-	-
0	HRCSTBF	HRC Stability Flag Bit ● 0b0: HRC is stopped or unstable ● 0b1: HRC is stable **Note** If the HRCSTBF flag bit is detected as not set (remaining at 0), the software must execute a restart procedure: stop the HRC → wait for 1 µs → restart the HRC again.	RO

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5.4.14 CMU System Clock Source Switch Register (CMU_CKSWR)

Offset	Bit Position							
0x0C	7	6	5	4	3	2	1	0
Reset	0x01							
Name	Reserved					CKSW		
Access						RW		

Bit	Name	Functional Description	Access
7:3	*Reserved*	-	-
2:0	CKSW	System Clock Source Switching ● 0b000: Select HRC clock as the system clock ● 0b001: Select MRC clock as the system clock ● 0b010: Select LRC clock as the system clock ● 0b011: Select XTAL clock as the system clock ● 0b101: Select PLL as the system clock ● Others: Setting prohibited **Note** ● Ensure that the target clock source is in a stable state before switching. Please refer to "Source Switching" for the operating steps. ● When the PWC_STPMCR.CKSMRC bit is 1, after waking up from STOP mode, this register initializes, and the system clock source selects MRC clock.	RW

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5.4.15 CMU Clock Divider Config Register (CMU_SCFGR)

Offset	Bit Position																													
0x08	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved					HCLKS			Reserved									PCLK4S			Reserved		PCLK3S				Reserved				PCLK1S	
Access						RW												RW					RW								RW	

Bit	Name	Functional Description	Access
31:27	*Reserved*	-	-
26:24	HCLKS	HCLK Clock Division Selection Bit ● 0b000: 1 division of the system clock ● 0b001: 2 division of the system clock ● 0b010: 4 division of the system clock ● 0b011: 8 division of the system clock ● 0b100: 16 division of the system clock ● 0b101: 32 division of the system clock ● 0b110: 64 division of the system clock ● 0b111: Setting prohibited **Note** When the PWC_STPMCR.CKSMRC bit is set to 1, after waking up from STOP mode, this register initializes, and HCLK is set to the system clock divided by 1.	RW
23:15	*Reserved*	-	-
14:12	PCLK4S	PCLK4_SYNC Clock Division Selection Bit ● 0b000: 1 division of the system clock ● 0b001: 2 division of the system clock ● 0b010: 4 division of the system clock ● 0b011: 8 division of the system clock ● 0b100: 16 division of the system clock ● 0b101: 32 division of the system clock ● 0b110: 64 division of the system clock ● 0b111: Setting prohibited **Note** When the PWC_STPMCR.CKSMRC bit is 1, after waking up from STOP mode, this register initializes, and PCLK4_SYNC is 1 division of the system clock.	RW
11	*Reserved*	-	-
10:8	PCLK3S	PCLK3 Clock Division Selection Bit ● 0b000: 1 division of the system clock ● 0b001: 2 division of the system clock	RW

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Bit	Name	Functional Description	Access
10:8	PCLK3S	● 0b010: 4 division of the system clock ● 0b011: 8 division of the system clock ● 0b100: 16 division of the system clock ● 0b101: 32 division of the system clock ● 0b110: 64 division of the system clock ● 0b111: Setting prohibited **Note** When the PWC_STPMCR.CKSMRC bit is 1, after waking up from STOP mode, this register initializes, and PCLK3 is 1 division of the system clock.	RW
7:3	*Reserved*	-	-
2:0	PCLK1S	PCLK1 Clock Division Selection Bit ● 0b000: 1 division of the system clock ● 0b001: 2 division of the system clock ● 0b010: 4 division of the system clock ● 0b011: 8 division of the system clock ● 0b100: 16 division of the system clock ● 0b101: 32 division of the system clock ● 0b110: 64 division of the system clock ● 0b111: Setting prohibited **Note** When the PWC_STPMCR.CKSMRC bit is 1, after waking up from STOP mode, this register initializes, and PCLK1 is 1 division of the system clock.	RW

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5.4.16 CMU ADC Clock Config Register (CMU_ADCKSEL)

Offset	Bit Position															
0x00	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved							ADCKSEL	Reserved					ADCKDIV		
Access								RW						RW		

Bit	Name	Functional Description	Access
15:9	*Reserved*	-	-
8	ADCKSEL	PCLK4 Clock Source Selection ● 0b0: PCLK4_SYNC ● 0b1: PLLQ **Note** When switching the target clock source to PLL, ensure that the PLL clock is in a stable state.	RW
7:3	*Reserved*	-	-
2:0	ADCKDIV	ADCLK Division Selection ● 0b000: PCLK4 ● 0b001: 2 division of the PCLK4 ● 0b010: 3 division of the PCLK4 ● 0b011: 4 division of the PCLK4 ● 0b100: 5 division of the PCLK4 ● 0b101: 6 division of the PCLK4 ● 0b110: 7 division of the PCLK4 ● 0b111: 8 division of the PCLK4 **Note** When PCLK4 selects PLLQ as the clock source, this bit setting is invalid, and ADCLK has the same frequency as the PLLQ clock.	RW

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5.4.17 CMU Function Clock Control Register (CMU_FCG)

Offset	Bit Position																													
0x30	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFFFFFFFF																															
Name	DCU	CRC	SPI	I2C	USART4	USART3	USART2	USART1	Reserved	MAU	Reserved	TMR4	EMB	Reserved			TMR0_2	TMR0_1	Reserved	TMRA_5	TMRA_4	TMRA_3	TMRA_2	TMRA_1	FCM	HALL	DMA	AOS	CMP	Reserved		ADC
Access	RW	RW	RW	RW	RW	RW	RW	RW		RW		RW	RW				RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW			RW

Bit	Name	Functional Description	Access
31	DCU	DCU Function Control ● 0b0: Function enabled ● 0b1: Function disabled	RW
30	CRC	CRC Function Control ● 0b0: Function enabled ● 0b1: Function disabled	RW
29	SPI	SPI Function Control ● 0b0: Function enabled ● 0b1: Function disabled	RW
28	I2C	I2C Function Control ● 0b0: Function enabled ● 0b1: Function disabled	RW
27	USART4	USART4 Function Control ● 0b0: Function enabled ● 0b1: Function disabled	RW
26	USART3	USART3 Function Control ● 0b0: Function enabled ● 0b1: Function disabled	RW
25	USART2	USART2 Function Control ● 0b0: Function enabled ● 0b1: Function disabled	RW
24	USART1	USART1 Function Control ● 0b0: Function enabled ● 0b1: Function disabled	RW
23	*Reserved*	*All bits read as 1, Write as 1.*	-
22	MAU	MAU Function Control ● 0b0: Function enabled ● 0b1: Function disabled	RW
21	*Reserved*	*All bits read as 1, Write as 1.*	-

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Bit	Name	Functional Description	Access
20	TMR4	TMR4 Function Control ● 0b0: Function enabled ● 0b1: Function disabled	RW
19	EMB	EMB Function Control ● 0b0: Function enabled ● 0b1: Function disabled	RW
18:16	*Reserved*	*All bits read as 1, Write as 1.*	-
15	TMR0_2	TMR0_2 Function Control ● 0b0: Function enabled ● 0b1: Function disabled	RW
14	TMR0_1	TMR0_1 Function Control ● 0b0: Function enabled ● 0b1: Function disabled	RW
13	*Reserved*	*All bits read as 1, Write as 1.*	-
12	TMRA_5	TMRA_5 Function Control ● 0b0: Function enabled ● 0b1: Function disabled	RW
11	TMRA_4	TMRA_4 Function Control ● 0b0: Function enabled ● 0b1: Function disabled	RW
10	TMRA_3	TMRA_3 Function Control ● 0b0: Function enabled ● 0b1: Function disabled	RW
9	TMRA_2	TMRA_2 Function Control ● 0b0: Function enabled ● 0b1: Function disabled	RW
8	TMRA_1	TMRA_1 Function Control ● 0b0: Function enabled ● 0b1: Function disabled	RW
7	FCM	FCM Function Control ● 0b0: Function enabled ● 0b1: Function disabled	RW
6	HALL	HALL Function Control ● 0b0: Function enabled ● 0b1: Function disabled	RW
5	DMA	DMA Function Control ● 0b0: Function enabled ● 0b1: Function disabled	RW
4	AOS	AOS Function Control ● 0b0: Function enabled ● 0b1: Function disabled	RW

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Bit	Name	Functional Description	Access
3	CMP	CMP Function Control ● 0b0: CMP1-CMP3, DAC function enabled ● 0b1: CMP1-CMP3, DAC function disabled	RW
2:1	*Reserved*	*All bits read as 1, Write as 1.*	-
0	ADC	ADC Function Control ● 0b0: Function enabled ● 0b1: Function disabled	RW

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5.4.18 CMU MCO Clock Output Config Register (CMU_MCOCFGR)

Offset	Bit Position							
0x24	7	6	5	4	3	2	1	0
Reset	0x00							
Name	MCOEN	MCODIV			MCOSEL			
Access	RW	RW			RW			

Bit	Name	Functional Description	Access
7	MCOEN	MCO Output Permission ● 0b0: Disable ● 0b1: Enable	RW
6:4	MCODIV	MCO Frequency Division Selection ● 0b000: Divide by 1 ● 0b001: Divide by 2 ● 0b010: Divide by 4 ● 0b011: Divide by 8 ● 0b100: Divide by 16 ● 0b101: Divide by 32 ● 0b110: Divide by 64 ● 0b111: Divide by 128	RW
3:0	MCOSEL	MCO Clock Source Selection ● 0b0000: HRC clock ● 0b0001: MRC clock ● 0b0010: LRC clock ● 0b0011: XTAL clock ● 0b0101: PLLP clock ● 0b0110: HCLK clock ● 0b1111: PLLQ clock ● Others: Setting prohibited	RW

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5.4.19 FCM Lower Limit Control Register (FCM_LVR)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																LVR															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	LVR	Lower Limit Compare Value Configure this register when the START bit is 0	RW

5.4.20 FCM Upper Limit Control Register (FCM_UVR)

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																UVR															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	UVR	Upper Limit Compare Value Configure this register when the START bit is 0	RW

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5.4.21 FCM Counter Register (FCM_CNTR)

Offset	Bit Position																													
0x08	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																CNTR															
Access																	RO															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	CNTR	Counter Value Save the counter value to this register when an active edge selected by the EDGES bit of the reference clock is detected (except for the first active edge after START=1)	RO

5.4.22 FCM Start Control Register (FCM_STR)

Offset	Bit Position																													
0x0C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																															START
Access																																RW

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-
0	START	Frequency Measurement Start Bit ● 0b0: Frequency measurement stop ● 0b1: Frequency measurement start	RW

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5.4.23 FCM Measurement Control Register (FCM_MCCR)

Offset	Bit Position																													
0x10	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								MCKS				Reserved		MDIVS	
Access																									RW						RW	

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7:4	MCKS	Measurement Object Clock Selection Bit ● 0b0000: XTAL ● 0b0010: HRC ● 0b0011: LRC ● 0b0101: PCLK1 ● 0b0111: MRC ● 0b1000: PLLP ● Others: Setting prohibited	RW
3:2	*Reserved*	-	-
1:0	MDIVS	Measurement Object Division Selection ● 0b00: No division ● 0b01: Divide by 4 ● 0b10: Divide by 8 ● 0b11: Divide by 32	RW

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5.4.24 FCM Reference Control Register (FCM_RCCR)

Offset	Bit Position																													
0x14	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																EXREFE	Reserved	EDGES		Reserved		DNFS		INEXS	RCKS				Reserved		RDIVS
Access																	RW		RW				RW		RW	RW						RW

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15	EXREFE	External Pin Input Reference Clock FCMREF Enable Bit ● 0b0: Disable external pin input reference clock FCMREF ● 0b1: Enable external pin input reference clock FCMREF	RW
14	*Reserved*	-	-
13:12	EDGES	Measurement Reference Edge Selection Bit ● 0b00: Rising edge ● 0b01: Falling edge ● 0b10: Rising and falling edges ● 0b11: Setting prohibited	RW
11:10	*Reserved*	-	-
9:8	DNFS	Digital Filtering Function Selection Bit ● 0b00: No filter function ● 0b01: Clock selected by MCKS bit as filter clock ● 0b10: 4 divisions of the clock selected by MCKS bit as filter clock ● 0b11: 16 divisions of the clock selected by MCKS bit as filter clock	RW
7	INEXS	Measurement Reference, Internal Clock, and Terminal Selection Bit ● 0b0: External pin input reference clock FCMREF ● 0b1: Clock selected by RCKS bit	RW
6:3	RCKS	Measurement Reference Clock Selection Bit ● 0b0000: XTAL ● 0b0010: HRC ● 0b0011: LRC ● 0b0101: PCLK1 ● 0b0111: MRC ● 0b1000: PLLP ● Others: Setting prohibited	RW
2	*Reserved*	-	-

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Bit	Name	Functional Description	Access
1:0	RDIVS	Measurement Reference Division Selection ● 0b00: Divide by 32 ● 0b01: Divide by 128 ● 0b10: Divide by 1024 ● 0b11: Divide by 8192 **Notice** When an external pin is used as the reference clock, this bit setting is invalid.	RW

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5.4.25 FCM Reset Interrupt Control Register (FCM_RIER)

Offset	Bit Position																															
0x18	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								ERRRE	Reserved		ERRINTRS	Reserved	OVFIE	MENDIE	ERRIE
Access																									RW			RW		RW	RW	RW

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7	ERRRE	Frequency Exception Reset Enable Bit ● 0b0: Disable ● 0b1: Enable	RW
6:5	*Reserved*	-	-
4	ERRINTRS	Frequency Exception Interrupt Reset Selection Bit ● 0b0: Interrupt occurs when frequency exception occurs ● 0b1: Reset occurs when frequency exception occurs	RW
3	*Reserved*	-	-
2	OVFIE	Counter Overflow Interrupt Enable Bit ● 0b0: Disable counter overflow interrupt ● 0b1: Enable counter overflow interrupt	RW
1	MENDIE	Measurement End Interrupt Enable Bit ● 0b0: Disable interrupt when measurement ends ● 0b1: Enable interrupt when measurement ends	RW
0	ERRIE	Frequency Exception Interrupt Enable Bit ● 0b0: Disable interrupt when frequency exception occurs ● 0b1: Enable interrupt when frequency exception occurs	RW

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5.4.26 FCM Flag Register (FCM_SR)

Offset	Bit Position																													
0x1C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																													OVF	MENDF	ERRF
Access																														RO	RO	RO

Bit	Name	Functional Description	Access
31:3	*Reserved*	-	-
2	OVF	Counter Overflow Flag Bit ● 0b0: Counter has not overflowed ● 0b1: Counter has overflowed	RO
1	MENDF	Measurement End Flag Bit ● 0b0: In measurement ● 0b1: Measurement end	RO
0	ERRF	Frequency Exception Flag Bit ● 0b0: No frequency exception occurred ● 0b1: Frequency exception occurred	RO

5.4.27 FCM Flag Clear Register (FCM_CLR)

Offset	Bit Position																													
0x20	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																													OVFCLR	MENDFCLR	ERRFCLR
Access																														WO	WO	WO

Bit	Name	Functional Description	Access
31:3	*Reserved*	-	-
2	OVFCLR	Counter Overflow Flag Clear Write 1 to clear the flag, write 0 has no effect.	WO
1	MENDFCLR	Measurement End Flag Clear Write 1 to clear the flag, write 0 has no effect.	WO
0	ERRFCLR	Frequency Exception Flag Clear Write 1 to clear the flag, write 0 has no effect.	WO

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6 Power Control (PWC)

6.1 Introduction

Power controller is used to control the supply, switching and detection in run modes and low power modes. The power controller consists of a power consumption control logic (PWCL), a power supply voltage detection unit (PVD).

The operating voltage (VCC) of the chip is 2.7V to 5.5V. The voltage regulator (LDO) supplies power to the VDD domain. The chip provides two low-power modes: SLEEP mode and STOP mode through the power consumption control logic (PWCL).

The power voltage detection unit (PVD) provides functions such as power on reset (POR), power down reset (PDR), brown out reset (BOR), programmable voltage detection 1 (PVD1), programmable voltage detection 2 (PVD2). Among them, POR, PDR, and BOR control the chip reset action by detecting the VCC voltage. PVD1 detects the VCC voltage and resets or interrupts the chip according to the register settings. PVD2 detects VCC voltage or external input detection voltage, and generates reset or interrupt according to register selection.

The analog blocks are equipped with dedicated supply pins for improved analog performance.

6.2 Functional Description

6.2.1 Power Distribution

6.2.1.1 Power Distribution Structure

The chip consists of VCC domain, VDD power domain and AVCC power domain.

- The VCC domain is powered by VCC/VSS pins and consists of power consumption control logic (PWCL), supply voltage detection unit (PVD), voltage regulator (LDO), external high-speed oscillator (XTAL) and other circuits.
- The VDD power domain consists of digital logic such as CPU, digital peripherals, RAM, FLASH, etc., and is powered by VDD generated by LDO.
- The AVCC power domain is an analog power domain, which is mainly composed of analog-to-digital converter (ADC), digital-to-analog converter (DAC), comparator (CMP), bandgap reference source circuit (HPBGR), operational amplifier (OPA), and input and output pins of analog system. It is powered by AVCC/AVSS pins. In order to provide high-precision analog performance, the analog area is equipped with an independent power supply. To ensure higher accuracy of the ADC, the reference voltage of the ADC uses dedicated pins (VREFH, VREFL).

The figure below is the power distribution diagram of the chip.

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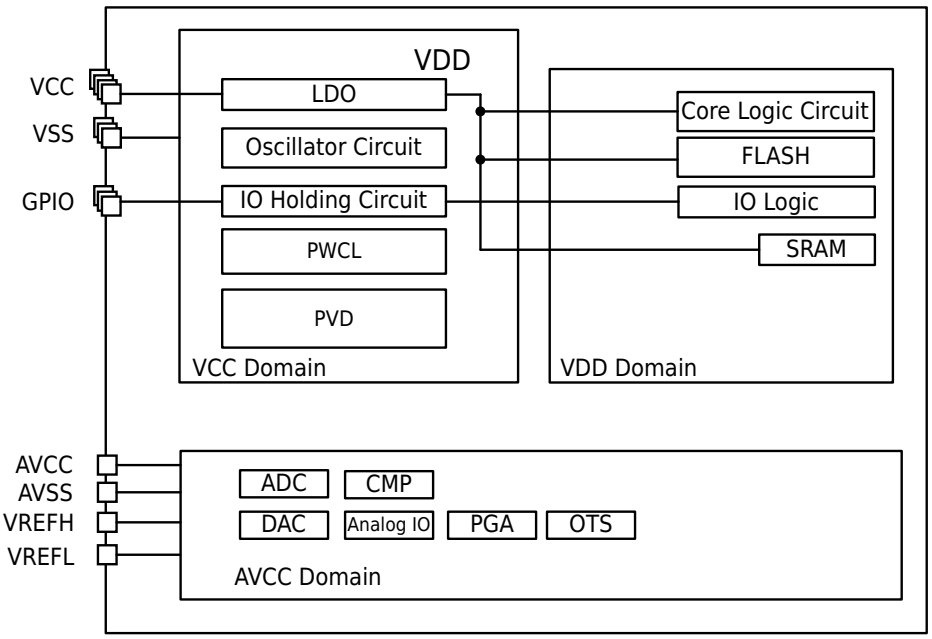

Figure 6-1 Power Supply Configuration Diagram

6.2.2 Power Voltage Detection Unit (PVD) Description

The power voltage detection unit (PVD) includes power on reset (POR), power down reset (PDR), brown out reset (BOR), programmable voltage detection 1 (PVD1), programmable voltage detection 2 (PVD2).

6.2.2.1 Power-on/Power-down Reset Action Description

The chip is integrated with power-on reset circuit and power-down reset circuit. The power-on reset and power-down reset waveforms are as shown. When VCC is higher than the specified threshold V_{POR}, after the T_{RSTPOR} time, the chip releases the power-on reset state, and the CPU starts to execute code. When VCC is lower than V_{PDR}, the chip remains in reset state. When power-on reset is used, the reset pin NRST must be 1. If the reset pin is pulled down, the chip will be reset and started by pin reset.

For detailed information on parameters such as V_{POR}, V_{PDR}, and T_{RSTPOR}, refer to the "Electrical Characteristics" chapter of the Datasheet.

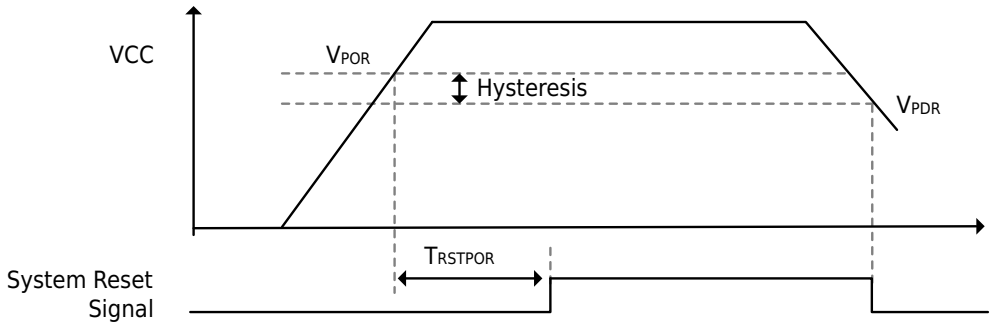

Figure 6-2 Power-on Reset, Power-down Reset Waveforms

6.2.2.2 Brown-out Reset (BOR) Description

During power-on, until VCC is higher than VBOR, a brown-out reset (BOR) will put the chip in reset.

The VBOR threshold is configured through the BOR_LEV, BORDIS of the initialization configuration bits (ICG). When BORDIS=0b0, the BOR detection voltage can be selected from 4 thresholds. When BORDIS is configured as 0b1, the chip performs reset control through power-on reset and power-down reset.

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Table 6-1 BOR Configuration

BORDIS	BOR_LEV	Description
0b1	0bXX	BOR Inactive
0b0	0b00	BOR Active, Select BOR Threshold 0 (VBOR0)
0b0	0b01	BOR Active, Select BOR Threshold 1 (VBOR1)
0b0	0b10	BOR Active, Select BOR Threshold 2 (VBOR2)
0b0	0b11	BOR Active, Select BOR Threshold 3 (VBOR3)

For the electrical characteristics of the BOR threshold, see the "Electrical Characteristics" chapter of the Datasheet.

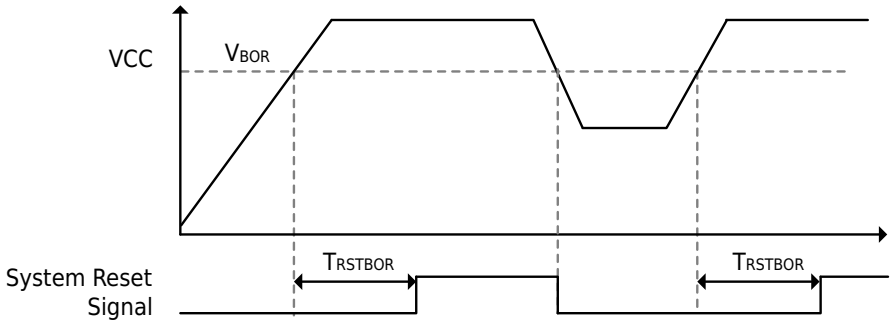

Figure 6-3 Brown-out Reset Waveform

6.2.2.3 Programmable Voltage Detection 1 (PVD1), Programmable Voltage Detection 2 (PVD2)

Programmable voltage detection 1 and programmable voltage detection 2 trigger corresponding reset or interrupt actions by detecting whether the VCC power supply voltage passes the detection threshold. Each detection circuit can be programmed and configured separately.

When the power supply voltage passes through the threshold voltage point of each detection circuit, the event can be programmed and configured as a reset/interrupt (maskable/non-maskable) .

The main features of programmable voltage detection are shown in the following table.

Table 6-2 PVD1/PVD2 Features

Item	PVD1	PVD2
Test Object	Whether VCC has passed the threshold voltage point (VPVD1) during the falling/rising process	Whether VCC passes through the threshold voltage point (VPVD2) during the falling/rising process, and whether the rising and falling of the external input voltage passes through the threshold voltage point
Detection Voltage Point	Configured by PVD1LVL	Configured by PVD2LVL
Reset	Reset: VCC<VPVD1; Reset release: VCC>VPVD1 after a certain reset processing time.	Reset: VCC<VPVD2; Reset release: VCC>VPVD2 after a certain reset processing time.

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Item	PVD1	PVD2
Interrupt	Configured as voltage detection 1 interrupt or non-maskable interrupt	Configured as voltage detection 2 interrupt or non-maskable interrupt
	VCC falls through the threshold voltage point (VPVD1) or VCC rises through the threshold voltage point (VPVD1) or VCC rises/falls through the threshold voltage point (VPVD1)	VCC falls through the threshold voltage point (VPVD2) or VCC rises through the threshold voltage point (VPVD2) or VCC rises/falls through the threshold voltage point (VPVD2)
Filter Function	Digital filtering	Digital filtering

6.2.2.4 PVD1, PVD2 Interrupt/Reset Block Diagram

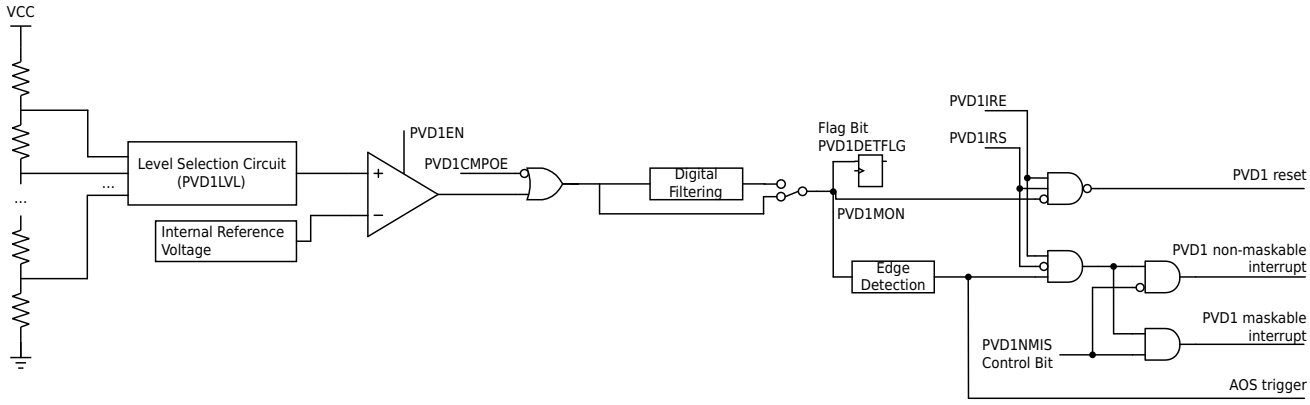

Figure 6-4 PVD1 Interrupt/Reset Block Diagram

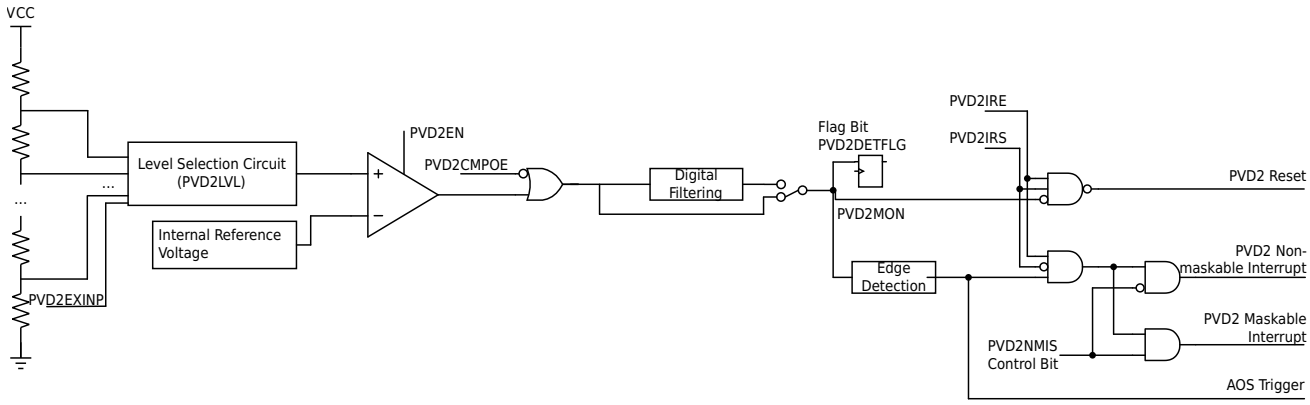

Figure 6-5 PVD2 Interrupt/Reset Block Diagram

6.2.2.5 Input/Output Pin

Pin Name	Input/Output	Function
PVD2EXINP	Input	External input PVD2 comparison voltage

6.2.2.6 PVD1 Interrupt and Reset

When using the PVD1 circuit in Stop mode, please observe the following precautions:

1. Stop Mode
   - The digital filter must be disabled.

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The figure below is the running timing diagram of the voltage monitoring 1 interrupt. PVD1DETFLG needs to be cleared before the interrupt can occur again.

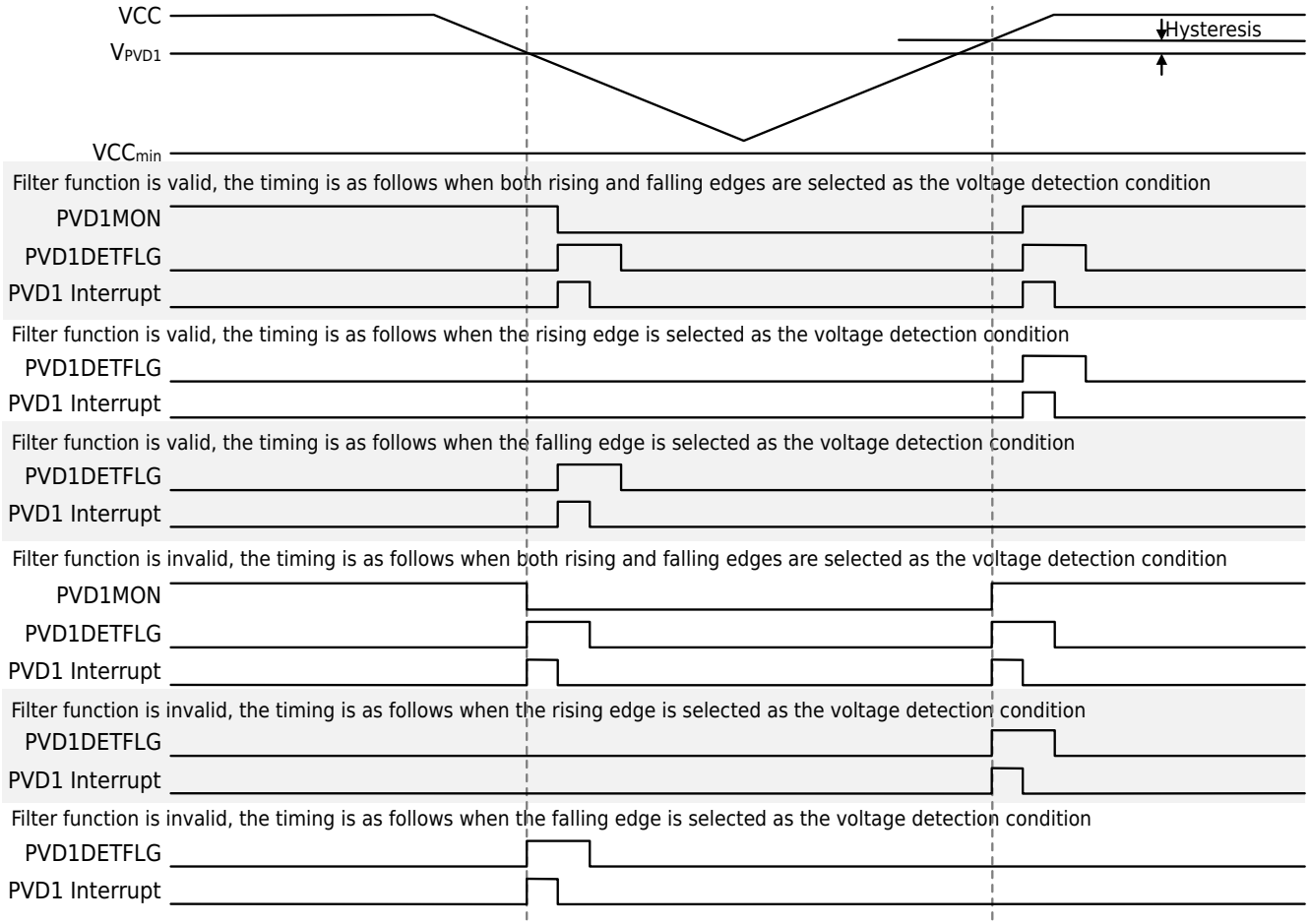

Figure 6-6 Power Monitor 1 Interrupt Timing Diagram

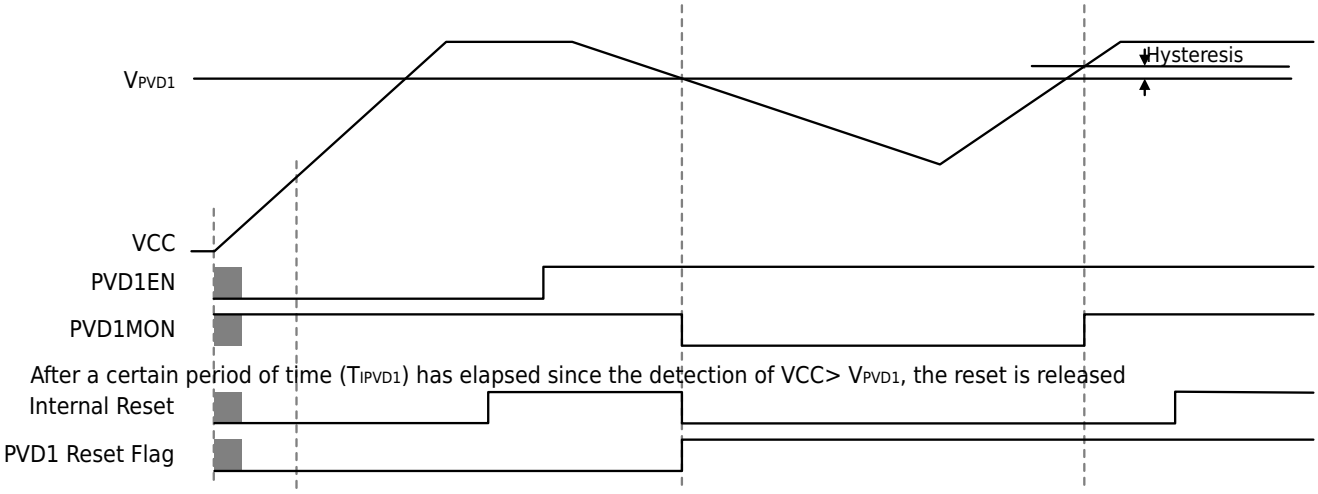

Figure 6-7 Power Monitor 1 Reset Timing Diagram

6.2.2.7 PVD2 Interrupt and Reset

When using the PVD2 circuit in Stop mode, please observe the following precautions:

1. Stop Mode
   - The digital filter must be disabled.

The figure below is the running timing diagram of the voltage monitoring 2 interrupt. PVD2DETFLG needs to be cleared before the interrupt can occur again.

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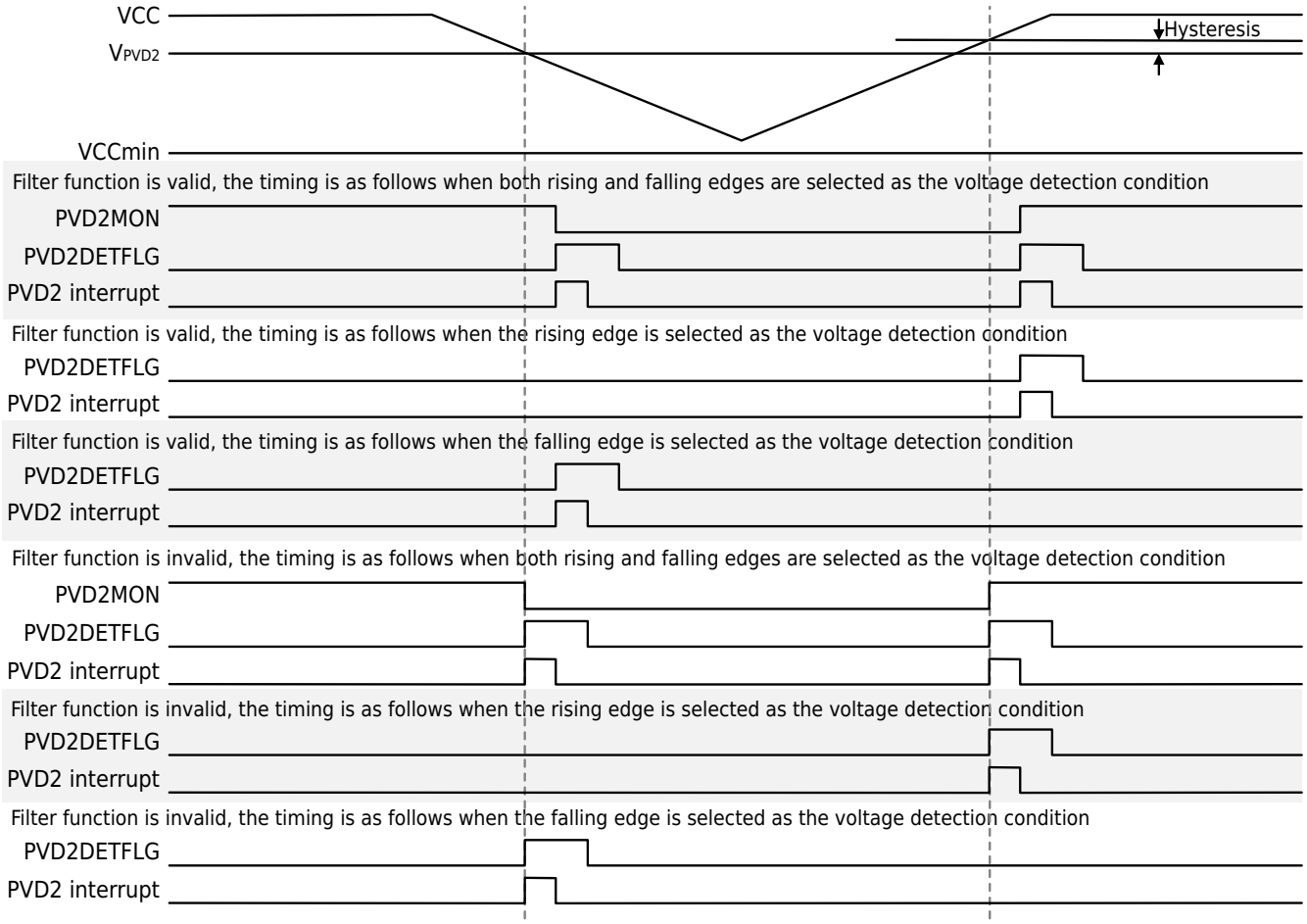

Figure 6-8 Power Monitor 2 Interrupt Timing Diagram

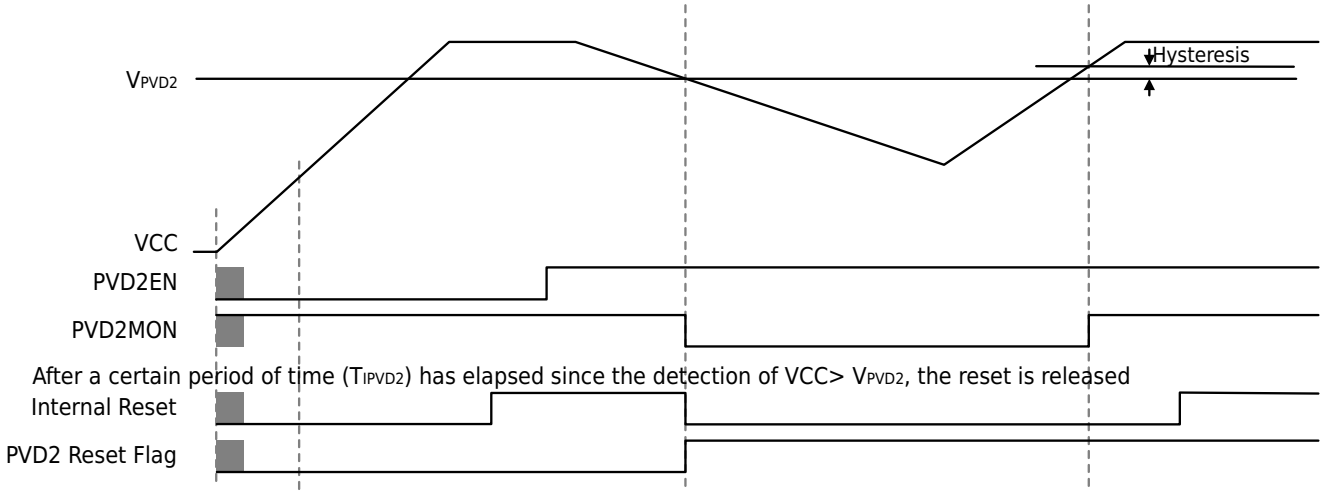

Figure 6-9 Power Monitor 2 Reset Timing Diagram

6.2.3 Action Mode and Low Power Mode

6.2.3.1 Mode Overview

After the system reset or power-on reset, all the power fields of the chip are in the power supply state, and the chip enters the run mode. In RUN mode, the CPU provides the clock through HCLK and executes program code.

In order to save power consumption when the CPU does not need to run, the system provides two low-power modes: Sleep mode, Stop mode. The low power consumption modes that the chip can be

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configured in are shown in the following table. In Sleep mode, the Cortex-M4 core of the chip stops operating, and the peripherals keep running; in Stop mode, the peripherals and CPU of the chip stop operating.

Table 6-4 Low Power Mode

Mode	Description
Sleep Mode	CPU clock stopped, peripherals keep running
Stop Mode	The chip peripherals and the clocks of CPU are stopped

Users can choose operating mode and low power mode based on the application to find the best balance between low power consumption, short start-up time, wake-up sources, and system execution efficiency.

Power consumption in operating mode can be optimized by the following methods:

1. Reduce system clock speed
2. Turn off the clock sources that are not in use
3. Set the CMU_FCG register to turn off unused functions

The operating conditions of low power mode and the status of each module in low power mode are shown in the table below.

Table 6-5 Operating Conditions of Low Power Mode and Status of Each Module in Low Power Mode

Item	Sleep mode	Stop mode
Entry	PWC_STPMCR.STOP=0b0 WFI	PWC_STPMCR.STOP=0b1 WFI
Release	To interrupt or reset arbitrarily	Interrupt or reset that can be used in Stop mode
External high-speed oscillator	Optional, can be enabled by software	Stop
Internal high-speed oscillator	Optional, can be enabled by software	Stop
Internal medium-speed oscillator	Optional, can be enabled by software	Stop
Internal low-speed oscillator	Optional, can be enabled by software	Optional, can be enabled by software
PLL	Optional, can be enabled by software	Stop
CPU	Stop (hold)	Stop (hold)
RAM	Optional, can be enabled by software	Stop (hold)
Flash	Optional, can be enabled by software	Stop (hold)
DMA	Optional, can be enabled by software	Stop (hold)
Voltage regulator	Enable	Enable
Power-on reset circuit	Enable	Enable
Brown-out reset BOR	Optional, can be enabled by software	Optional, can be enabled by software
Voltage detection module PVD	Optional, can be enabled by software	Optional, can be enabled by software
WDT	Optional, can be enabled by software	Stop (hold)
SWDT	Optional, can be enabled by software	Optional, can be enabled by software
Timer0	Optional, can be enabled by software	Optional, can be enabled by software
Other peripheral modules	Optional, can be enabled by software	Stop (hold)
ADC	Optional, can be enabled by software	Stop
DAC	Optional, can be enabled by software	Optional, can be enabled by software
CMP	Optional, can be enabled by software	Optional, can be enabled by software

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Item	Sleep mode	Stop mode
P36-P37	Optional, can be enabled by software	When used as an external high-speed oscillator, oscillator stops concussion and the pin state keeps the state before entering STOP mode; when set as GPIO or other peripheral functions, keep the status before STOP
NRST reset pin	Outside the chip is pulled up to VCC through circuit	Outside the chip is pulled up to VCC through resistance
MD	Optional, can be enabled by software	Hold
PB1, PB2	Optional, can be enabled by software When used as the SWD function, the built-in pull-up circuit is effective	Hold When used as the SWD function, the built-in pull-up circuit is effective
Other GPIO	Optional, can be enabled by software	Hold

6.2.3.2 RUN Mode

After the system power-on reset, or when MCU is wake-up from various low-power states, the MCU enters the running state.

6.2.3.3 Sleep Mode

In Sleep mode, the CPU stops running and its internal registers remain in the state before entering Sleep mode. The operating status of peripherals and other system modules other than the watchdog and dedicated watchdog does not change.

When set to auto-start through ICG, if the ICG0.WDTSLPOFF bit is 0b1, the watchdog stops counting in Sleep mode; if the WDTSLPOFF bit is 0b0, the watchdog continues counting in Sleep mode. When the ICG is not set to start automatically, start the watchdog via software startup, if the WDT_CR.SLPOFF bit is 0b1, the watchdog stops counting in Sleep mode; if the WDT_CR.SLPOFF bit is 0b0, the watchdog does not stop counting in Sleep mode.

When set to auto-start through ICG, if the ICG0.SWDTSLPOFF bit is 0b1, the dedicated watchdog stops counting in Sleep mode; if the SWDTSLPOFF bit is 0b0, the dedicated watchdog continues counting in Sleep mode.

- Enter Sleep Mode

  When PWC_STPMCR.STOP= 0b0, WFI instructions can be executed to enter Sleep mode.
- Exit Sleep Mode

  Any interrupt and reset can wake the chip from Sleep mode. When waking up by interrupt, the chip enters interrupt processing program. The chip enters the reset state when exiting Sleep mode through reset.

6.2.3.4 Stop Mode

In Stop mode, the CPU, most peripherals, and clock sources all stop. The chip maintains CPU internal register and SRAM data, peripheral state and pin state. In the Stop mode, because most of the clock sources stop working, the voltage regulator also reduces the drive capability, so the chip power consumption will be significantly reduced.

When set to auto-start through ICG, if the ICG0.SWDTSLPOFF bit is 0b1, the dedicated watchdog stops counting in Stop mode; if the SWDTSLPOFF bit is 0b0, the dedicated watchdog continues counting in Stop mode.

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Before executing the WFI command into Stop mode, make sure that FLASH is not programmed or erased and that the oscillation stop detect function is disabled, otherwise the chip will enter Sleep mode instead of Stop mode.

In Stop mode, the ADC also consumes power unless it is disabled before entering Stop mode. To disable the ADC, clear the ADC_STR.STRT bit, set CMU_FCG.ADC, and then execute the WFI instruction to enter Stop mode.

When waking from STOP mode:

- PWC_STPMCR.CKSMRC controls the clock source after wake-up. When CKSMRC=0b1, the system clock source after wake-up is selected as MRC; when CKSMRC=0b0, the system clock after wake-up remains the same as the clock source before entering STOP.
- PWC_STPMCR.FLNWT controls whether to wait for Flash stabilization after wake-up. When FLNWT=0b0, wake-up requires waiting for Flash stabilization; when FLNWT=0b1, wake-up does not require waiting for Flash stabilization. FLNWT can only be set when the program is running from RAM; otherwise, the chip's behavior after waking from STOP cannot be guaranteed.

Note

When entering STOP mode with the program running from RAM, selecting CKSMRC=0b1 allows the system to wake up in the shortest possible time.

After entering STOP mode, the high-precision BGR circuit (HPBGR) is disabled, which can reduce power consumption in STOP mode. If a comparator interrupt is to be used to exit Stop mode, do not disable the high-precision BGR circuit.

Note

Setting PWC_STPMCR.HPBGREN to 1 before entering STOP mode keeps the high-precision BGR circuit (HPBGR) enabled during STOP mode, but this results in higher power consumption in STOP mode.

Before executing the WFI instruction to enter Stop mode:

1. Ensure the DMA is in a stopped state; otherwise, the chip may exhibit unpredictable behavior.
2. Disable the digital filter for EIRQ; otherwise, that interrupt cannot be used for STOP wake-up.

When using a non-maskable interrupt to exit Stop mode, set the corresponding bit in INTC_NMIER to enable that interrupt. When using a maskable interrupt to exit Stop mode, set the corresponding bit in the INTC_WKEN register to enable the wake-up permission for that interrupt.

- Enter Stop mode

  Step1. Clear PWC_LPMCSR.LPMF;

  Step2. When PWC_STPMCR.STOP=0b1, execute WFI instruction to enter stop mode;

  Step3. Read PWC_LPMCSR.LPMF. If this bit is 1, the chip has entered STOP mode normally. If this bit is 0, return to step 2.

  For the status of the chip's peripherals and clock sources in Stop mode, see the table "Table 6-5 : Operating Conditions of Low Power Mode and Status of Each Module in Low Power Mode".

- Release Stop mode

  The Stop mode can be removed by reset and interrupt. The reset methods that can be used to release Stop mode include pin reset, power-on reset, brown-out reset (BOR), programmable voltage detect 1/2 reset and dedicated watchdog reset. Interrupt events that can be used to release stop mode: Pin interrupt EIRQ0-7, voltage detection 1 interrupt, voltage detection 2 interrupt, dedicated

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watchdog underflow interrupt, comparator interrupt, USART1 RX interrupt, Timer0 compare match interrupt.

When the chip releases the Stop mode through interrupt, it first activates the clock source used before entering the Stop mode. After all clock sources are stabilized, the chip releases the Stop mode.

When the WFI instruction is executed to enter the stop mode, an interrupt event that is not used to release the Stop mode is generated. The chip will respond to the interrupt first instead of entering the STOP mode. To prioritize entering STOP mode without executing the interrupt, interrupts that are not used to release the Stop mode must be disabled before executing the WFI instruction.

6.2.4 Methods to Reduce Power Consumption

The following methods can be used to optimize power consumption in Active Mode:

- Reduce the system clock speed
- Turn off unused clock sources
- Configure the CMU_FCG register to disable unused functions

6.2.4.1 Reduce System Clock Speed

In run mode, the speed of system clock (HCLK) and peripheral clock PCLK1/PCLK3/PCLK4 can be reduced by programming the prescaler register. These pre-dividers can also be used to reduce the speed of peripherals before entering Sleep mode. For more information, see "Clock Module Unit (CMU)".

6.2.4.2 Disable Unused Clock Sources

The system clock of the chip has the following clock sources:

- External high-speed oscillator (XTAL)
- PLL clock (PLL)
- Internal high-speed oscillator (HRC)
- Internal medium-speed oscillator (MRC)
- Internal low-speed oscillator (LRC)

For detailed information, please refer to the "Clock Module Unit (CMU)".

6.2.4.3 Stop Functional Clock

The peripheral module of the chip is provided with a clock stop function. By setting the register corresponding position bit, the unused modules can be disabled, and the clock of the corresponding module is also stopped to reduce the power consumption. In the module stop state, the register inside the module remains in the state it was in before stopping.

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6.3 Register Description

Register protection function is used to inactiveate the write operation of the register to protect the register from accidental overwriting.

Table 6-6 Register Protection List

Protected Register Bit	Protected Register
PWC_FPRC.FPRCB0	CMU_ADCKSEL, CMU_XTALSTDSR, CMU_SCFGR, CMU_CKSWR, CMU_XTALCR, CMU_XTALCFGR, CMU_XTALSTBCR, CMU_HRCCR, CMU_OSCSTBSR, CMU_MCOCFGR, CMU_XTALSTDCR, CMU_FCG, CMU_LRCCR, CMU_MRCCR, CMU_PLLCFGR, CMU_PLLCR
PWC_FPRC.FPRCB1	PWC_STPMCR, PWC_RAMCR, PWC_LPMCSCR, PWC_DBGC, RMU_RSTF0, RMU_FRST0
PWC_FPRC.FPRCB3	PWC_PVDCR0, PWC_PVDCR1, PWC_PVDFCR, PWC_PVDLCR, PWC_PVDICR, PWC_PVDDSR

6.3.1 Register List

Base Address: 0x40054000

Table 6-7 Power Control (PWC) Register Offset

Offset	Register	Description	Width
0x00	PWC_STPMCR	Stop Mode Control Register	8
0x0C	PWC_RAMCR	RAM Control Register	8
0x10	PWC_PVDCR0	PVD Control Register 0	8
0x14	PWC_PVDCR1	PVD Control Register 1	8
0x18	PWC_PVDFCR	PVD Filter Control Register	8
0x1C	PWC_PVDLCR	PVD Level Control Register	8
0x20	PWC_PVDICR	PVD Interrupt Control Register	8
0x24	PWC_PVDDSR	PVD Detection Status Register	8
0x30	PWC_FPRC	Function Protection Control Register	16
0x40	PWC_DBGC	Debug Mode Control Register	16
0x50	PWC_LPMCSR	Low Power Mode Status Register	16
0x52	PWC_LPMCSCR	Low Power Mode Status Clear Register	16

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6.3.2 Stop Mode Control Register (PWC_STPMCR)

Offset	Bit Position							
0x00	7	6	5	4	3	2	1	0
Reset	0x00							
Name	STOP	Reserved			HPBGREN	Reserved	CKSMRC	FLNWT
Access	RW				RW		RW	RW

Bit	Name	Functional Description	Access
7	STOP	STOP Mode Control Bit ● 0b0: CPU WFI enters SLEEP ● 0b1: CPU WFI enters STOP	RW
6:4	*Reserved*	-	-
3	HPBGREN	HPBGR Enable Control ● 0b0: HPBGR is invalid in STOP mode ● 0b1: HPBGR is valid in STOP mode	RW
2	*Reserved*	-	-
1	CKSMRC	System Clock Switch Control after STOP Wake-up ● 0b0: Maintain the system clock and its frequency division as they were before entering STOP mode ● 0b1: Switch system clock to MRC and initialize CMU_SCFGR register when waking up from STOP mode	RW
0	FLNWT	Flash Stable Wait Control during STOP Wake-up ● 0b0: Wait for FLASH to stabilize when waking up from STOP mode ● 0b1: Do not wait for FLASH to stabilize when waking up from STOP mode	RW

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6.3.3 RAM Control Register (PWC_RAMCR)

Offset	Bit Position							
0x0C	7	6	5	4	3	2	1	0
Reset	0x10							
Name	CRPEF	HRPEF	SRPEF	RPERDIS	Reserved			
Access	RW	RW	RW	RW				

Bit	Name	Functional Description	Access
7	CRPEF	Cache RAM Parity Error Flag Write 0 to clear the flag, write 1 has no effect Read: ● 0b0: No parity error has occurred ● 0b1: A parity error has occurred **Note** Always valid, set whenever a parity error occurs.	RW
6	HRPEF	High-Speed RAM Parity Error Flag Write 0 to clear the flag, write 1 has no effect Read: ● 0b0: No parity error has occurred ● 0b1: A parity error has occurred **Note** Always valid, set whenever a parity error occurs.	RW
5	SRPEF	RAM Parity Error Flag Write 0 to clear the flag, write 1 has no effect Read: ● 0b0: No parity error has occurred ● 0b1: A parity error has occurred **Note** Always valid, set whenever a parity error occurs.	RW
4	RPERDIS	RAM Parity Error Reset Enable ● 0b0: Reset is generated on RAM parity error ● 0b1: Reset is not generated on RAM parity error	RW
3:0	*Reserved*	-	-

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6.3.4 Low Power Mode Status Register (PWC_LPMCSR)

Offset	Bit Position															
0x50	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved															LPMF
Access																RO

Bit	Name	Functional Description	Access
15:1	*Reserved*	-	-
0	LPMF	Low Power Mode Flag Bit ● 0b0: The chip has not entered Stop mode ● 0b1: The chip has entered Stop mode	RO

6.3.5 Low Power Mode Status Clear Register (PWC_LPMCSCR)

Offset	Bit Position															
0x52	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved															LPMFC
Access																RW

Bit	Name	Functional Description	Access
15:1	*Reserved*	-	-
0	LPMFC	LPMF Flag Clear Write 1 to clear flag, write 0 has no effect; read always returns 0.	RW

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6.3.6 PVD Control Register 0 (PWC_PVDCR0)

Offset	Bit Position							
0x10	7	6	5	4	3	2	1	0
Reset	0x00							
Name	Reserved		PVD2EN	PVD1EN	Reserved			EXVCCINEN
Access			RW	RW				RW

Bit	Name	Functional Description	Access
7:6	*Reserved*	-	-
5	PVD2EN	Voltage Detection 2 Permissible ● 0b0: Voltage detection 2 circuit disabled ● 0b1: Voltage detection 2 circuit enabled	RW
4	PVD1EN	Voltage Detection 1 Permissible ● 0b0: Voltage detection 1 circuit disabled ● 0b1: Voltage detection 1 circuit enabled	RW
3:1	*Reserved*	-	-
0	EXVCCINEN	External VCC Voltage Input Enable ● 0b0: External VCC voltage input disabled ● 0b1: External VCC voltage input enabled	RW

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6.3.7 PVD Control Register 1 (PWC_PVDCR1)

Offset	Bit Position							
0x14	7	6	5	4	3	2	1	0
Reset	0x00							
Name	Reserved	PVD2CMPOE	PVD2IRS	PVD2IRE	Reserved	PVD1CMPOE	PVD1IRS	PVD1IRE
Access		RW	RW	RW		RW	RW	RW

Bit	Name	Functional Description	Access
7	*Reserved*	-	-
6	PVD2CMPOE	PVD2 Compare Result Output Enabled ● 0b0: Disable output of comparison result of comparator 2 ● 0b1: Enable output the comparison result of comparator 2	RW
5	PVD2IRS	PVD2 Interrupt Reset Selection ● 0b0: Generate PVD2 interrupt when VCC changes to meet the detection conditions ● 0b1: PVD2 reset is generated during the falling process through VPVD2	RW
4	PVD2IRE	PVD2 Interrupt Reset Enabled ● 0b0: Disable ● 0b1: Enable **Note** Please write 1 to this bit when the PWC_PVDCR0.PVD2EN bit is 1 and the PVD2CMPOE bit is 1.	RW
3	*Reserved*	-	-
2	PVD1CMPOE	PVD1 Compare Result Output Enabled ● 0b0: Disable output of comparison result of comparator 1 ● 0b1: Enable output the comparison result of comparator 1	RW
1	PVD1IRS	PVD1 Interrupt Reset Selection ● 0b0: Generate PVD1 interrupt when VCC changes to meet the detection conditions ● 0b1: PVD1 reset is generated during the falling process through VPVD1	RW
0	PVD1IRE	PVD1 Interrupt Reset Enabled ● 0b0: Disable ● 0b1: Enable **Note** Please write 1 to this bit when the PWC_PVDCR0.PVD1EN bit is 1 and the PVD1CMPOE bit is 1.	RW

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6.3.8 PVD Filter Control Register (PWC_PVDFCR)

Offset	Bit Position							
0x18	7	6	5	4	3	2	1	0
Reset	0x11							
Name	Reserved	PVD2NFCKS		PVD2NFDIS	Reserved	PVD1NFCKS		PVD1NFDIS
Access		RW		RW		RW		RW

Bit	Name	Functional Description	Access
7	*Reserved*	-	-
6:5	PVD2NFCKS	PVD2 Digital Filter Sampling Clock Selection ● 0b00: 2 filter clock periods ● 0b01: 4 filter clock periods ● 0b10: 8 filter clock periods ● 0b11: 16 filter clock periods Filter clock period=LRC period **Note** This bit can only be rewritten when the PVD2NFDIS bit is 1.	RW
4	PVD2NFDIS	PVD2 Digital Filter Shield ● 0b0: Digital filter enabled ● 0b1: Digital filter disabled	RW
3	*Reserved*	-	-
2:1	PVD1NFCKS	PVD1 Digital Filter Sampling Clock Selection ● 0b00: 2 filter clock periods ● 0b01: 4 filter clock periods ● 0b10: 8 filter clock periods ● 0b11: 16 filter clock periods Filter clock period=LRC period **Note** This bit can only be rewritten when the PVD1NFDIS bit is 1.	RW
0	PVD1NFDIS	PVD1 Digital Filter Shield ● 0b0: Digital filter enabled ● 0b1: Digital filter disabled	RW

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6.3.9 PVD Level Control Register (PWC_PVDLCR)

Offset	Bit Position							
0x1C	7	6	5	4	3	2	1	0
Reset	0x00							
Name	PVD2LVL				PVD1LVL			
Access	RW				RW			

Bit	Name	Functional Description	Access
7:4	PVD2LVL	PVD2 Threshold Voltage Selection ● 0b0000: 2.50V ● 0b0001: 2.65V ● 0b0010: 2.80V ● 0b0011: 2.95V ● 0b0100: 3.10V ● 0b0101: 3.25V ● 0b0110: 3.40V ● 0b0111: 3.55V ● 0b1000: 3.70V ● 0b1001: 3.85V ● 0b1010: 4.00V ● 0b1011: 4.15V ● 0b1100: 4.30V ● 0b1101: 4.45V ● 0b1110: 4.60V ● 0b1111: 4.75V	RW
3:0	PVD1LVL	PVD1 Threshold Voltage Selection ● 0b0000: 2.50V ● 0b0001: 2.65V ● 0b0010: 2.80V ● 0b0011: 2.95V ● 0b0100: 3.10V ● 0b0101: 3.25V ● 0b0110: 3.40V ● 0b0111: 3.55V ● 0b1000: 3.70V ● 0b1001: 3.85V ● 0b1010: 4.00V ● 0b1011: 4.15V ● 0b1100: 4.30V ● 0b1101: 4.45V ● 0b1110: 4.60V ● 0b1111: 4.75V	RW

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6.3.10 PVD Interrupt Control Register (PWC_PVDICR)

Offset	Bit Position							
0x20	7	6	5	4	3	2	1	0
Reset	0x00							
Name	Reserved	PVD2EDGS		PVD2NMIS	Reserved	PVD1EDGS		PVD1NMIS
Access		RW		RW		RW		RW

Bit	Name	Functional Description	Access
7	*Reserved*	-	-
6:5	PVD2EDGS	PVD2 Detection Condition Selection ● 0b00: When VCC < VPVD2 (falling) is detected ● 0b01: When VCC ≥ VPVD2 (rising) is detected ● 0b10: When VCC < VPVD2 (falling) is detected or when VCC ≥ VPVD2 (rising) is detected ● 0b11: Setting prohibited	RW
4	PVD2NMIS	PVD2 Interrupt Type Selection ● 0b0: PVD2 interrupt as non-maskable interrupt ● 0b1: PVD2 interrupt as maskable interrupt	RW
3	*Reserved*	-	-
2:1	PVD1EDGS	PVD1 Detection Condition Selection ● 0b00: When VCC < VPVD1 (falling) is detected ● 0b01: When VCC ≥ VPVD1 (rising) is detected ● 0b10: When VCC < VPVD1 (falling) is detected or when VCC ≥ VPVD1 (rising) is detected ● 0b11: Setting prohibited	RW
0	PVD1NMIS	PVD1 Interrupt Type Selection ● 0b0: PVD1 interrupt as non-maskable interrupt ● 0b1: PVD1 interrupt as maskable interrupt	RW

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6.3.11 PVD Detection Status Register (PWC_PVDDSR)

Offset	Bit Position							
0x24	7	6	5	4	3	2	1	0
Reset	0x11							
Name	Reserved		PVD2DETFLG	PVD2MON	Reserved		PVD1DETFLG	PVD1MON
Access			RW	RO			RW	RO

Bit	Name	Functional Description	Access
7:6	*Reserved*	-	-
5	PVD2DETFLG	PVD2 Detection Flag Bit After reading this bit, write any value to the PWC_PVDDSR register to clear this flag bit Read: ● 0b0: PVD2 does not detect VCC passing through VPVD2 ● 0b1: PVD2 detects that VCC passes through VPVD2 **Note** This bit is valid when the PWC_PVDCR0.PVD2EN bit is 1 and the PWC_PVDCR1.PVD2CMPOE bit is 1.	RW
4	PVD2MON	PVD2 Monitoring Bit ● 0b0: VCC ≤ VPVD2 or external input comparison voltage ≤ PVD2 internal reference voltage ● 0b1: When PVD2 is disabled or VCC>VPVD2 or external input comparison voltage>PVD2 internal reference voltage	RO
3:2	*Reserved*	-	-
1	PVD1DETFLG	PVD1 Detection Flag Bit After reading this bit, write any value to the PWC_PVDDSR register to clear this flag bit Read: ● 0b0: PVD1 does not detect VCC passing through VPVD1 ● 0b1: PVD1 detects that VCC passes through VPVD1 **Note** This bit is valid when the PWC_PVDCR0.PVD1EN bit is 1 and the PWC_PVDCR1.PVD1CMPOE bit is 1.	RW
0	PVD1MON	PVD1 Monitoring Bit ● 0b0: VCC<VPVD1 ● 0b1: When PVD1 is disabled or VCC>VPVD1	RO

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6.3.12 Function Protection Control Register (PWC_FPRC)

Offset	Bit Position															
0x30	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	PWC_FPRCWE								FPRCB7	FPRCB6	FPRCB5	FPRCB4	FPRCB3	FPRCB2	FPRCB1	FPRCB0
Access	RW								RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
15:8	PWC_FPRCWE	PWC_FPRC Register Write Enabled When writing FPRCB7-FPRCB0, 0xA5 must be written to PWC_FPRCWE at the same time; read always returns 0	RW
7	FPRCB7	FPRC Bit7 Reserved, Read as 0, Write as 0	RW
6	FPRCB6	FPRC Bit6 Reserved, Read as 0, Write as 0	RW
5	FPRCB5	FPRC Bit5 Reserved, Read as 0, Write as 0	RW
4	FPRCB4	FPRC Bit4 Reserved, Read as 0, Write as 0	RW
3	FPRCB3	FPRC Bit3 For the protection objects, please refer to the "Register Protection List": ● 0b0: Object write disabled ● 0b1: Object write enabled	RW
2	FPRCB2	FPRC Bit2 Reserved, Read as 0, Write as 0	RW
1	FPRCB1	FPRC Bit1 For the protection objects, please refer to the "Register Protection List": ● 0b0: Object write disabled ● 0b1: Object write enabled	RW
0	FPRCB0	FPRC Bit0 For the protection objects, please refer to the "Register Protection List": ● 0b0: Object write disabled ● 0b1: Object write enabled	RW

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6.3.13 Debug Mode Control Register (PWC_DBGC)

Offset	Bit Position															
0x40	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved															DBGEN
Access																RW

Bit	Name	Functional Description	Access
15:1	*Reserved*	-	-
0	DBGEN	Debug Enable ● 0b0: Debug mode disabled when in STOP mode ● 0b1: Debug mode enabled when in STOP mode	RW

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7 Initialization Configuration (ICG)

7.1 Introduction

After the chip's reset is released, the hardware circuit reads data from FLASH addresses 0x00020000-0x00020010 and loads it into the Initialization Configuration (ICG) register. Users can modify the ICG register by programming or erasing the corresponding FLASH addresses of the sectors. Addresses 0x00020018-0x0002001F are the data security protection enable region; for details, please contact the sales window. The register reset value is determined by FLASH data.

7.2 Register Description

7.2.1 Register List

Base address: 0x00020000

Table 7-1 Initialization Configuration (ICG) Register Offset

Offset	Register	Description	Width
0x000	ICG0	Initialization Configuration Register 0	32
0x004	ICG1	Initialization Configuration Register 1	32
0x008	ICG2	Initialization Configuration Register 2	32
0x00C	ICG3	Initialization Configuration Register 3	32
0x010	ICG4	Initialization Configuration Register 4	32

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7.2.2 Initialization Configuration Register 0 (ICG0)

Offset	Bit Position																													
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	Reserved			WDTSLPOFF	WDTWDPT				WDTCKS				WDTPERI		WDTITS	WDTAUTS	Reserved			SWDTSLPOFF	SWDTWDPT				SWDTCKS				SWDTPERI		SWDTITS	SWDTAUTS
Access				RO	RO				RO				RO		RO	RO				RO	RO				RO				RO		RO	RO

Bit	Name	Functional Description	Access
31:29	*Reserved*	*All bits read as 1, Write as 1*	-
28	WDTSLPOFF	WDT Counting Stops in Sleep Mode ● 0b0: WDT counting does not stop in Sleep mode ● 0b1: WDT counting stops in Sleep mode	RO
27:24	WDTWDPT	Refresh Allowed Area Count Percentage Allowed interval for refreshing the WDT count value: ● 0b0000: 0%-100% ● 0b0001: 0%-25% ● 0b0010: 25%-50% ● 0b0011: 0%-50% ● 0b0100: 50%-75% ● 0b0101: 0%-25%, 50%-75% ● 0b0110: 25%-75% ● 0b0111: 0%-75% ● 0b1000: 75%-100% ● 0b1001: 0%-25%, 75%-100% ● 0b1010: 25%-50%, 75%-100% ● 0b1011: 0%-50%, 75%-100% ● 0b1100: 50%-100% ● 0b1101: 0%-25%, 50%-100% ● 0b1110: 25%-100% ● 0b1111: 0%-100%	RO
23:20	WDTCKS	WDT Count Clock ● 0b0010: PCLK3/4 ● 0b0110: PCLK3/64 ● 0b0111: PCLK3/128 ● 0b1000: PCLK3/256 ● 0b1001: PCLK3/512 ● 0b1010: PCLK3/1024 ● 0b1011: PCLK3/2048 ● 0b1101: PCLK3/8192 ● Others: Reserved	RO

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Bit	Name	Functional Description	Access
19:18	WDTPERI	WDT Count Overflow Period ● 0b00: 256 periods ● 0b01: 4096 periods ● 0b10: 16384 periods ● 0b11: 65536 periods	RO
17	WDTITS	WDT Interrupt Selection ● 0b0: Interrupt request ● 0b1: Reset request	RO
16	WDTAUTS	WDT Auto Start ● 0b0: After reset, WDT auto-starts (hardware start) ● 0b1: After reset, WDT is in stopped state	RO
15:13	*Reserved*	*All bits read as 1, Write as 1*	-
12	SWDTSLPOFF	SWDT Counting Stops in Sleep/Stop Mode ● 0b0: SWDT counting does not stop in Sleep mode/Stop mode ● 0b1: SWDT counting stops in Sleep mode/Stop mode	RO
11:8	SWDTWDPT	Refresh Allowed Area Count Percentage Allowed interval for refreshing the SWDT count value: ● 0b0000: 0%-100% ● 0b0001: 0%-25% ● 0b0010: 25%-50% ● 0b0011: 0%-50% ● 0b0100: 50%-75% ● 0b0101: 0%-25%, 50%-75% ● 0b0110: 25%-75% ● 0b0111: 0%-75% ● 0b1000: 75%-100% ● 0b1001: 0%-25%, 75%-100% ● 0b1010: 25%-50%, 75%-100% ● 0b1011: 0%-50%, 75%-100% ● 0b1100: 50%-100% ● 0b1101: 0%-25%, 50%-100% ● 0b1110: 25%-100% ● 0b1111: 0%-100%	RO
7:4	SWDTCKS	SWDT Counter Clock ● 0b0000: SWDTCLK ● 0b0100: SWDTCLK/16 ● 0b0101: SWDTCLK/32 ● 0b0110: SWDTCLK/64 ● 0b0111: SWDTCLK/128 ● 0b1000: SWDTCLK/256 ● 0b1011: SWDTCLK/2048 ● Others: Reserved	RO

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Bit	Name	Functional Description	Access
3:2	SWDTPERI	SWDT Count Overflow Period ● 0b00: 256 periods ● 0b01: 4096 periods ● 0b10: 16384 periods ● 0b11: 65536 periods	RO
1	SWDTITS	SWDT Interrupt Selection ● 0b0: Interrupt request ● 0b1: Reset request	RO
0	SWDTAUTS	SWDT Auto Start ● 0b0: After reset, SWDT auto-starts (hardware start) ● 0b1: After reset, SWDT is in stopped state	RO

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7.2.3 Initialization Configuration Register 1 (ICG1)

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	BORDIS	Reserved							BOR_LEV		Reserved																				LKUPDIS	
Access	RO								RO																						RO	

Bit	Name	Functional Description	Access
31	BORDIS	BOR Action Selection ● 0b0: Enable BOR action after reset ● 0b1: Disable BOR action after reset	RO
30:26	*Reserved*	*All bits read as 1, Write as 1*	-
25:24	BOR_LEV	BOR Threshold Voltage Selection ● 0b00: 2.50V ● 0b01: 2.80V ● 0b10: 3.55V ● 0b11: 3.85V	RO
23:1	*Reserved*	*All bits read as 1, Write as 1*	-
0	LKUPDIS	LKUP Reset Disable Control ● 0b0: Cortex-M4 LOCKUP reset valid ● 0b1: Cortex-M4 LOCKUP reset invalid	RO

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7.2.4 Initialization Configuration Register 2 (ICG2)

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	Reserved																															
Access																																

Bit	Name	Functional Description	Access
31:0	*Reserved*	*All bits read as 1, Write as 1*	-

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7.2.5 Initialization Configuration Register 3 (ICG3)

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	Reserved																								NMIICGEN	NMIEN	NMIFEN	NMITRG	NMIFCLK		Reserved	
Access																									RO	RO	RO	RO	RO			

Bit	Name	Functional Description	Access
31:8	*Reserved*	*All bits read as 1, Write as 1*	-
7	NMIICGEN	NMI Pin ICG Setting Enable ● 0b0: NMI pin ICG setting enable ● 0b1: NMI pin ICG setting disable	RO
6	NMIEN	NMI Pin Interrupt Enable ● 0b0: Disable ● 0b1: Enable	RO
5	NMIFEN	NMI Digital Filter Enable ● 0b0: Disable ● 0b1: Enable	RO
4	NMITRG	NMI Pin Edge Triggering ● 0b0: Falling edge ● 0b1: Rising edge	RO
3:2	NMIFCLK	Filter Sampling Clock Selection ● 0b00: PCLK1 ● 0b01: PCLK1/8 ● 0b10: PCLK1/32 ● 0b11: PCLK1/64	RO
1:0	*Reserved*	*All bits read as 1, Write as 1*	-

7.2.6 Initialization Configuration Register 4 (ICG4)

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	FCRCREF																															
Access	RO																															

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Bit	Name	Functional Description	Access
31:0	FCRCREF	FCRC Reference Value Flash CRC check reference value	RO

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8 Embedded Code Flash Memory (EFM)

8.1 Introduction

The Flash interface accesses Flash through the ICODE, DCODE, and MCODE buses. The interface can perform programming, erasing and full erasing operations on Flash. Besides, it can accelerate code execution through caching mechanisms.

8.2 Features

- Two independent cache areas: ICODE bus cache space 1KBytes (128x64); DCODE bus cache space 64Bytes (8x64)
- Supports proprietary code read protection (PCROP) function
- Supports Flash data CRC check function
- Support data security protection[*1]

Note

1. For specific specifications regarding Flash security protection, please consult the sales contact.

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8.3 Functional Description

8.3.1 Embedded Flash

Flash has the following main features:

- Up to 128KBytes capacity, with a total of 256 sectors, each sector is 512Bytes.
- 64-bit wide data read, with a 64-bit wide read cache buffer to accelerate code execution.
- Programming unit is 1/2/4Bytes. Erase unit is 512Bytes.

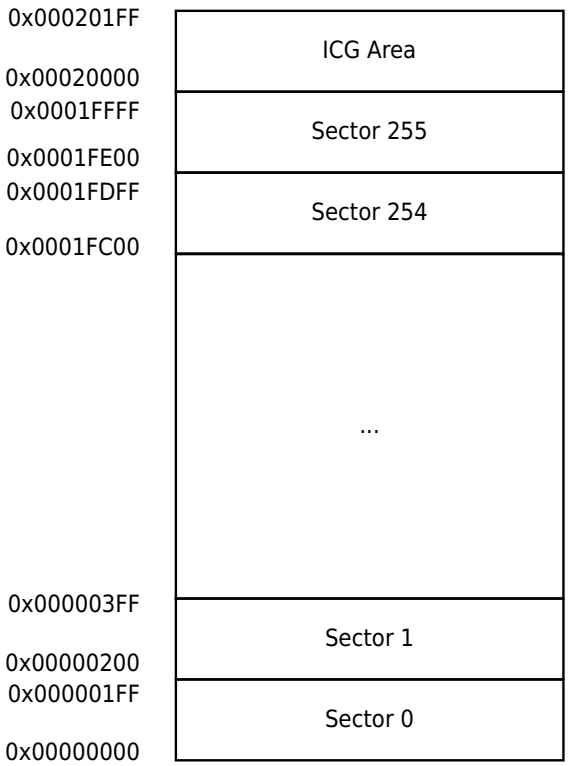

Figure 8-1 Flash Address Distribution

The ICG area is an independent sector that can be programmed and sector-erased. A full erase operation cannot be initiated for the ICG area. When a full erase is initiated for the Flash main memory, the ICG area will be erased along with it.

8.3.2 Read Interface

8.3.2.1 CPU Clock and Flash Read Time Relationship

To correctly read Flash data, users need to set the wait period count (EFM_FRMC.FLWT) based on the CPU operation frequency.

After system reset, the CPU clock source is MRC (8MHz), and the Flash read wait period is 0. Users are recommended to follow these steps to modify the CPU frequency and Flash read wait period bits: The number of waiting periods is shown in the table below.

Table 8-1 CPU Clock Frequency and Flash Read Wait Cycle Comparison Table

CPU Clock Frequency (HCLK)	Read Wait Cycle Setting
100MHz<HCLK≤120MHz	EFM_FRMC.FLWT=0b100
75MHz<HCLK≤100MHz	EFM_FRMC.FLWT=0b011

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CPU Clock Frequency (HCLK)	Read Wait Cycle Setting
50MHz<HCLK≤75MHz	EFM_FRMC.FLWT=0b010
25MHz<HCLK≤50MHz	EFM_FRMC.FLWT=0b001
HCLK≤25MHz	EFM_FRMC.FLWT=0b000

CPU Frequency Increase Steps:

Step1. Write the new read wait period setting to the EFM_FRMC.FLWT register.

Step2. Read the EFM_FRMC register to check if the new wait period setting is successful.

Step3. Increase the CPU clock frequency by setting the CMU_CKSWR.CKSW register or the CMU_SCFGR.HCLKS register.

Step4. Read the CMU_CKSWR or CMU_SCFGR register to check if the new setting is successful.

CPU Frequency Reduction Steps:

Step1. Decrease the CPU clock frequency by setting the CMU_CKSWR.CKSW register or the CMU_SCFGR.HCLKS register.

Step2. Read the register CMU_CKSWR or CMU_SCFGR to check if the new setting is successful.

Step3. Write the new read wait period setting to the EFM_FRMC.FLWT register.

Step4. Read the EFM_FRMC register to check if the new wait period setting is successful.

8.3.3 Flash Read Acceleration Cache

Each Flash read operation is a 64-bit read, with data sent to the CPU and also stored in a buffer register.

To enable fast reading of Flash data, the Flash controller is configured with a read acceleration cache that optimizes read wait periods. To maximize processor performance, this accelerator stores ICODE and DCODE bus access data in cache memory, improving program execution speed.

The system provides 1.0625KBytes of space as cache memory to actively reduce the time loss caused by instruction jump. Enable the cache function by setting the EFM_FRMC.ICACHE/DCACHE bit to 1. Whenever an instruction or data miss occurs (i.e., the requested instruction or data is not present in the currently used instruction line or cache memory), the system copies the newly read data line (64 bits) into cache memory. If the instruction or data requested by the CPU is already in the cache, it can be obtained immediately without any delay. When the cache memory is full, the LRU (Least Recently Used) strategy is used to determine which data in the cache memory to replace.

When the CPU reads instructions or data, the Flash address is buffered. When there is a cache hit, the number of Flash read periods changes, as shown in the table below.

Table 8-2 Actual Flash Read Cycle Count

EFM_FRMC. FLWT Setting	Cache Disable		Cache Enable	
	Buffer Hit	Buffer Miss	Buffer or Cache Hit	Miss in Both Buffer and Cache
0	1	1	1	1
1	1	2	1	2
2	1	3	1	3
N(N>2)	1	N+1	1	N+1

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8.3.4 Flash Programming and Erasing Operations

8.3.4.1 Overview of Programming and Erasing Operations

Flash supports programming, sector erasing, and full erasing operations.

The Flash programming unit is 1/2/4 Bytes. The sector erasing unit is 512Bytes. Flash programming is divided into three modes: single programming without read-back mode, single programming with read-back mode, and continuous programming mode. During Flash programming/erasing, if EFM_FWMC.BUSHLDCTL=0 is set, the bus is held until the erase/write operation ends; if EFM_FWMC.BUSHLDCTL=1 is set, the bus is released.

Before Flash programming/erasing, please disable the cache function. The following sections describe the setup steps for programming and erasing operations respectively.

8.3.4.2 Flash (Sector Erasing/Programming) Window Protection

Flash provides window protection for sector erasing/programming. Flash can only be erased/programmed within the allowed area; otherwise, an erase/write error occurs. During sector erasing/programming operations, the hardware circuit will first determine whether the operation is within the allowed area (full erasing mode is not restricted by window protection). The start and end positions of the window are set by the registers EFM_FPMTSW and EFM_FPMTEW.

The specific protection functions are as follows:

1. If register EFM_FPMTEW = register EFM_FPMTSW, the entire Flash area can be erased and programmed.
2. If register EFM_FPMTEW > register EFM_FPMTSW, and the erasing/programming address is between the two registers (including EFM_FPMTEW and EFM_FPMTSW), then the erasing/programming action will be executed.
3. If register EFM_FPMTEW < register EFM_FPMTSW, the entire Flash area cannot be erased or programmed.

If the protection window start or end address is set in the middle of a sector, and the erase address is between the start and end addresses, then the sectors containing the start and end addresses will both be erased. As shown in the figure below, the shaded area addresses are outside the window, but sector erase will erase them:

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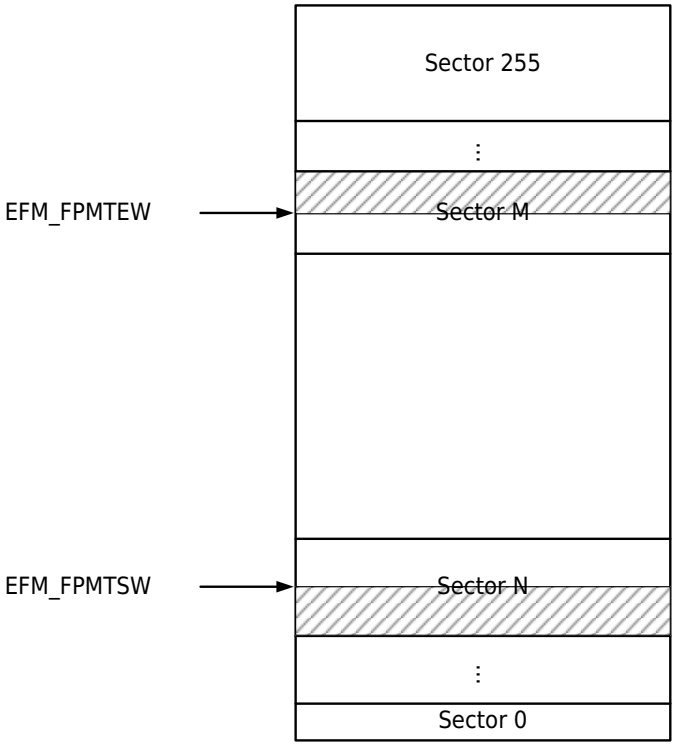

Figure 8-2 Flash Window Protection

8.3.4.3 Single Programming Without Read-back Function

The steps for single programming without read-back mode are as follows:

Step1. Disable the Flash register write protection. (Write 0x0123 to EFM_FAPRT first, then write 0x3210)

Step2. Enable the programming/erasing mode permission. (EFM_FWMC.PEMODE=0b1)

Step3. Set the single programming mode. (EFM_FWMC.PEMOD=0b001)

Step4. Read back the programming/erasing mode, confirm it is single programming mode before proceeding to the next step. (EFM_FWMC.PEMOD=0b001)

Step5. Write 32/16/8-bit data to the programming address. The programming address should be aligned according to the data width.

Step6. Wait for the Flash operation to end and for it to be in an idle state. (EFM_FSR.OPTEND=1, EFM_FSR.RDY=1)

Step7. Read the programming address value and check if it matches the written value:

If they match, programming is successful. If they do not match, the Flash address has been corrupted and should be permanently discarded.

Step8. Clear the end of programming flag. (EFM_FSR.OPTEND)

8.3.4.4 Single Programming With Read-back Function

Single programming with read-back mode refers to the hardware automatically reading the programming address data after programming ends and comparing it with the written data to verify correctness by checking the flag bit EFM_FSR.MISMTCH.

The steps for setting the read mode for single programming are as follows:

Step1. Disable the Flash register write protection. (EFM_FAPRT writes 0x0123 first, then writes 0x3210)

Step2. Enable the programming/erasing mode. (EFM_FWMC.PEMODE=0b1)

Step3. Set single programming with read-back mode. (EFM_FWMC.PEMOD=0b010)

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Step4. Read back the programming/erasing mode to confirm it is single programming with read-back mode before proceeding to the next step. (EFM_FWMC.PEMOD=0b010)

Step5. Write 32/16/8 bits of data to the programming address. The programming address should be aligned according to the programming data width.

Step6. Wait for the Flash operation to end and for it to be in an idle state. (EFM_FSR.OPTEND=1, EFM_FSR.RDY=1)

Step7. Check the programming self-read result flag bit (EFM_FSR.MISMTCH) :

If 0, programming is successful. If 1, the Flash address has been corrupted and should be permanently discarded.

Step8. Clear the programming end flag bit (EFM_FSR.OPTEND).

8.3.4.5 Continuous Programming Function

When programming Flash addresses consecutively, it is recommended to use continuous programming mode. Continuous programming mode can save over 50% of the time compared to single programming mode. In continuous programming mode, the interval between Flash address write commands should not exceed 25μs. The steps for setting up continuous programming operations are as follows:

Step1. Disable the Flash register write protection. (EFM_FAPRT writes 0x0123 first, then writes 0x3210)

Step2. Enable the programming/erasing mode. (EFM_FWMC.PEMODE=0b1)

Step3. Set continuous programming mode. (EFM_FWMC.PEMOD=0b011)

Step4. Read back the programming/erasing mode and confirm it is continuous programming mode before proceeding to the next step. (EFM_FWMC.PEMOD=0b011)

Step5. Write 32/16/8-bit data to the programming address. The programming address should be aligned according to the programming data width.

The programming program needs to run in an area outside Flash (such as the RAM area).

Step6. Wait for the operation end flag bit (EFM_FSR.OPTEND) to be set.

Step7. Clear the operation end flag bit until EFM_FSR.OPTEND reads 0.

Step8. Repeat steps 5-7 until all data is written.

Step9. Change the continuous programming mode to read-only mode to exit continuous programming mode. (EFM_FWMC.PEMOD=0b000)

Step10. Wait for Flash to be in an idle state. (EFM_FSR.RDY=1)

Step11. Read the programming address and check if it matches the written value.

If they match, programming is successful. If they do not match, the Flash address has been corrupted and should be permanently discarded.

Note

During Flash continuous programming, if a read operation to Flash occurs, an indeterminate value will be read. The read operation will set the read conflict bit EFM_FSR.RDCOLERR, which needs to be cleared by setting the EFM_FSCLR register.

Continuous programming can only be used for the main memory space (0x00000-0x1FFFF). Do not use continuous programming for storage spaces outside the main memory space (such as the ICG area).

8.3.4.6 Sector Erasing Function

After performing a sector erasing operation on Flash, the data in the sector (512Bytes of space) is refreshed to all 1s.

The steps for setting the sector erasing operation are as follows:

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Step1. Remove the Flash register write protection (EFM_FAPRT first writes 0x0123, then writes 0x3210).

Step2. Enable the programming/erasing mode. (EFM_FWMC.PEMODE=0b1)

Step3. Set sector erasing mode (EFM_FWMC.PEMOD=0b100).

Step4. Read back the programming/erasing mode and confirm it is in erasing mode before proceeding to the next step. (EFM_FWMC.PEMOD=0b100)

Step5. Write any 32-bit value to any address within the sector to be erased.

Step6. Wait for the Flash operation to end and for it to be in an idle state. (EFM_FSR.OPTEND=1, EFM_FSR.RDY=1)

Step7. Clear the erasing end flag bit. (EFM_FSR.OPTEND)

8.3.4.7 Full Erasing Function

The steps for setting the full erasing operation are as follows:

Step1. Remove the Flash register write protection (EFM_FAPRT first writes 0x0123, then writes 0x3210).

Step2. Enable the programming/erasing mode. (EFM_FWMC.PEMODE=0b1)

Step3. Set the full erasing mode. (EFM_FWMC.PEMOD=0b101)

Step4. Read back the programming/erasing mode, confirm it is full erasing mode before proceeding to the next step. (EFM_FWMC.PEMOD=0b101)

Step5. Write any 32-bit value to any address within the Flash block to be erased.

Step6. Wait for the Flash operation to end and for it to be in an idle state. (EFM_FSR.OPTEND=1, EFM_FSR.RDY=1)

Step7. Clear the erasing end flag bit. (EFM_FSR.OPTEND)

8.3.4.8 Bus Hold Function

By setting the EFM_FWMC.BUSHLDCTL bit, you can control whether the bus is held or released during Flash programming/erasing. When the bus is set to the held state, the CPU waits for the Flash programming or erasing to complete before fetching instructions from Flash to continue execution. When the bus is set to the released state, instructions must be placed in a space other than Flash (such as RAM), and the CPU fetches instructions from that space (e.g., RAM) to continue execution while Flash is being programmed or erased. If instructions are located in Flash and the bus is in the released state, when Flash is being programmed or erased, the CPU will attempt to fetch instructions from Flash, which may cause it to fetch incorrect instructions, leading to the chip running away.

8.3.5 Proprietary Code Read Out Protection (PCROP)

The Flash provides Proprietary Code Read Out Protection (PCROP) for intellectual property code. Data in the PCROP-protected area can only be executed but not read; otherwise, a read error (EFM_FSR.RDERR=1) and a bus error occur. Sectors protected by PCROP cannot be sector-erased, programmed, or fully erased; otherwise, an erase/write error (EFM_FSR.PEPRTERR=1) occurs. Disabling the PCROP function triggers a full erasing of the main memory (the ICG sector will not be erased). The PCROP function can be used in combination with the security protection function.

PCROP function enabling procedure:

Step1. Burn the target file into the protected area.

Step2. Program the PCROP function enable code 0x29163505 at address 0x01000E00-0x01000E03 according to the programming procedure.

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Step3. Program the PCROP function protection area settings at address 0x01000E04-0x01000E07 according to the programming procedure, where 0x01000E04-0x01000E05 is the PCROP protection start sector number, and 0x01000E06-0x01000E07 is the PCROP protection end sector number.

Step4. Wait for EFM_FSR.OPTEND=1.

Step5. Perform a system reset to reload the protection area settings.

Step6. Read the FPCROPFG register to confirm the protection range is set correctly.

Step7. Read the FOCDPRTFG register to confirm the PCROP function is enabled.

The condition for PCROP to be enabled is that the enable code is valid and the protection area setting is legal.

PCROP function disabling procedure method 1:

Step1. Initiate a sector erasing on any address within 0x01000E00-0x01000E07.

Step2. Wait for EFM_FSR.OPTEND=1.

Step3. Perform a system reset to reload the protection area settings.

Step4. Read the FOCDPRTFG register to confirm the PCROP function is disabled.

PCROP function disabling procedure method 2:

Step1. Initiate PCROP disable via DBGC_FMCCTL.PCROPERSREQ. This request remains effective even when Flash security protection is active.

Step2. Confirm PCROP has been successfully disabled via DBGC_FMCCTL.PCROPERSACK.

Step3. Perform a system reset to reload the protection area settings.

Step4. Read the FOCDPRTFG register to confirm the PCROP function is disabled.

The Flash memory map after enabling the PCROP function is shown in the following figure. If the address range to be protected is [0x4000, 0x6000), then PCROPSR=0x20, PCROPER=0x2F. The set PCROPSR and PCROPER are both included within the protected range; the sector after PCROPER+1 is outside the protection range. PCROPER cannot exceed the Flash main memory capacity; otherwise, the PCROP function setting fails.

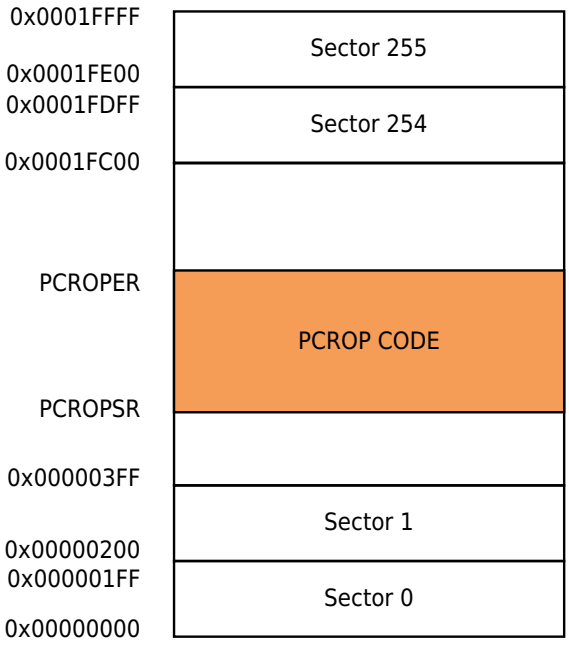

Figure 8-3 Memory Schematic After PCROP Enable

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Notice

1. Sector 0 cannot be selected as the PCROP function security protection area because it contains the interrupt vector table. Security protection area code must not be placed in Sector 0 during compilation.
2. For software usage precautions, refer to the PCROP function application note. Do not compile literal pools or other DBUS content into the PCROP protection area.
3. After the PCROP function is enabled, addresses 0x01000E00-0x01000E07 cannot be programmed; only sector erasing is possible.
4. For the register definitions and descriptions related to PCROP function disabling procedure method 2, please refer to the "Debug Controller (DBGC)" chapter.

8.3.6 Flash Data CRC Check Function

Before the chip reset is released, a Flash data CRC check request can be initiated via the debug interface. After the chip initialization is complete, the CRC calculation result for the selected Flash data area is returned to the debug interface. The CRC algorithm complies with CRC32 as defined by ISO/IEC13239. For specific information, please refer to the "CRC Operation (CRC)" chapter.

The usage flow of the Flash data CRC check function is shown in the figure below. For related register definitions and descriptions, please refer to the "Debug Controller (DBGC)" chapter.

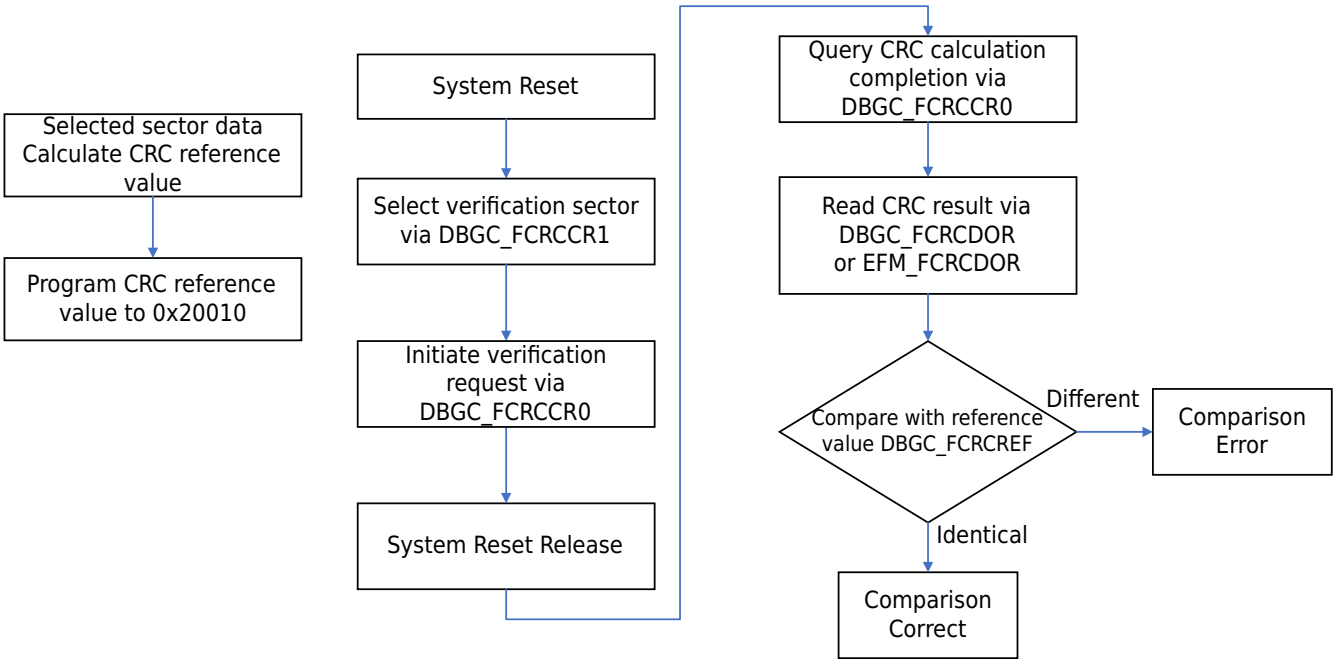

Figure 8-4 Flash Data CRC Check Function Usage Flow

8.3.7 Interrupt

The EFM module has 3 interrupts: PE (program/erase) error interrupt, bus conflict interrupt, and operation end interrupt, which can be queried by reading the EFM_FSR register status flag bits.

1. PE error interrupt EFM_PEERR:
   - **Set:**
     - Perform programming or sector erasing operations on write-protected addresses (EFM_FSR.PEPRTERR=1); perform programming/erasing operations on addresses within the window protection area or PCROP protection area, or perform a full erasing on Flash after PCROP is enabled (EFM_FSR.PEPRTERR=1).

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- Perform programming, sector erasing, or full erasing operations without setting the erase/write mode (EFM_FSR.PEWERR=1).
- In single programming Read-Back mode, the hardware automatically reads a value from the programming address that is inconsistent with the written value (EFM_FSR.MISMTCH=1).

- **Clear:**

  Write 1 to the corresponding flag clear bit in the EFM_FSCLR register to clear the status bit.

2. Flash read/write conflict or illegal read interrupt EFM_RDCOLERR:
   - **Set:**
     - A Flash read operation occurs during Flash continuous programming mode (EFM_FSR.COLERR=1).
     - A Flash read/write operation occurs during Flash stop mode (EFM_FSR.COLERR=1).
     - A Flash read/write operation occurs before Flash programming/erasing is completed (EFM_FSR.COLERR=1).
     - An illegal read operation occurs on the PCROP protected area after the PCROP function is enabled (EFM_FSR.RDERR=1).
   - **Clear:**

     Write 1 to the corresponding flag clear bit in the EFM_FSCLR register to clear the status bit.
3. End of operation interrupt EFM_OPTEND:
   - **Set:**
     - Programming mode: End of programming for a single address (EFM_FSR.OPTEND=1). When writing 32/16/8-bit data, Flash will be programmed 2/1/1 times, and the operation end interrupt will only occur once.
     - Erasing mode: Sector erasing, full erasing end (EFM_FSR.OPTEND=1).
   - **Clear:**

     Write 1 to the corresponding flag clear bit in the EFM_FSCLR register to clear the status bit.

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8.4 Register Description

8.4.1 Register List

Base Address: 0x40010400

Table 8-3 Embedded Code Flash Memory (EFM) Register Offset

Offset	Register	Description	Width
0x0000	EFM_FAPRT	Flash Access Protect Register	32
0x0004	EFM_FSTP	Flash Stop Register	32
0x0008	EFM_FRMC	Flash Read Mode Register	32
0x000C	EFM_FWMC	Flash Write Mode Register	32
0x0010	EFM_FSR	Flash State Register	32
0x0014	EFM_FSCLR	Flash State Clear Register	32
0x0018	EFM_FITE	Flash Interrupt Enable Register	32
0x0020	EFM_FPMTSW	Flash Permit Start Window Register	32
0x0024	EFM_FPMTEW	Flash Permit End Window Register	32
0x0050	FEM_UQID0	UNIQUE ID Register 0	32
0x0054	EFM_UQID1	UNIQUE ID Register 1	32
0x0058	EFM_UQID2	UNIQUE ID Register 2	32
0x0070	EFM_FOCDPRTFG	Flash Ocd Protect Flag Register	32
0x0120	EFM_FCRCDOR	Flash CRC Data Out Register	32
0x0128	EFM_FPCROPFG	Flash PCROP Set Flag Register	32

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8.4.2 Flash Access Protect Register (EFM_FAPRT)

Offset	Bit Position																													
0x0000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																FAPRT															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	FAPRT	EFM Register Write Protection EFM register access write-protection register. Release method: FAPRT writes 16-bit data "0x0123" first, then writes 16-bit data "0x3210". The EFM register reverts to protected state after a system reset. When EFM register access protection is enabled, the read value of this register is 0x00000000. When EFM register access protection is disabled, the register reads as 0x00000001.	RW

8.4.3 Flash Stop Register (EFM_FSTP)

Offset	Bit Position																													
0x0004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																															FSTP
Access																																RW

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-
0	FSTP	Flash Stop Mode Control ● 0b0: Flash active state ● 0b1: Flash in stop mode **Note** When this bit is set from 1 to 0, please confirm that the FSR.RDY bit is 1 before accessing Flash.	RW

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8.4.4 Flash Read Mode Register (EFM_FRMC)

Offset	Bit Position																													
0x0008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved												CRST	Reserved	DCACHE	ICACHE	Reserved														FLWT	
Access													RW		RW	RW														RW		

Bit	Name	Functional Description	Access
31:20	*Reserved*	-	-
19	CRST	Cache Reset ● 0b0: Cache data is de-asserted from reset ● 0b1: Cache data reset (buffer, cache)	RW
18	*Reserved*	-	-
17	DCACHE	DCODE Cache Permission Bits ● 0b0: Disable DCODE cache function ● 0b1: Enable DCODE cache function	RW
16	ICACHE	ICODE Cache Permission Bits ● 0b0: Disable ICODE cache function ● 0b1: Enable ICODE cache function	RW
15:3	*Reserved*	-	-
2:0	FLWT	Flash Read Inserted Wait Period ● 0b000: No read wait period is inserted ● 0b001: Insert 1 read wait period ● 0b010: Insert 2 read wait periods ● …… ● 0b110: Insert 6 read wait periods ● 0b111: Insert 7 read wait periods	RW

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8.4.5 Flash Write Mode Register (EFM_FWMC)

Offset	Bit Position																													
0x000C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																							BUSHLDCTL	Reserved	PEMOD			Reserved			PEMODE
Access																								RW		RW						RW

Bit	Name	Functional Description	Access
31:9	*Reserved*	-	-
8	BUSHLDCTL	Bus Control During Flash Programming/Erasing ● 0b0: During Flash programming and erasing, the bus is occupied ● 0b1: During Flash programming and erasing, the bus is released	RW
7	*Reserved*	-	-
6:4	PEMOD	Flash Programming/Erasing Mode ● 0b000: Read-only Mode ● 0b001: Single Programming without Read-back Mode ● 0b010: Single Programming with Read-back Mode ● 0b011: Continuous Programming Mode ● 0b100: Sector Erasing Mode ● 0b101: Full Erasing Mode ● 0b110/0b111: Read-only Mode	RW
3:1	*Reserved*	-	-
0	PEMODE	PEMOD Rewrite Enable ● 0b0: PEMOD rewrite prohibited ● 0b1: PEMOD rewrite permitted	RW

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8.4.6 Flash State Register (EFM_FSR)

Offset	Bit Position																													
0x0010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000100																															
Name	Reserved																							RDY	Reserved	RDERR	COLERR	OPTEND	MISMTCH	Reserved	PEPRTERR	PEWERR
Access																								RO		RO	RO	RO	RO		RO	RO

Bit	Name	Functional Description	Access
31:9	*Reserved*	-	-
8	RDY	Flash Busy/Idle State ● 0b0: Flash busy ● 0b1: Flash idle	RO
7	*Reserved*	-	-
6	RDERR	PCROP Function Protection Read Error ● 0b0: Flash read is normal under PCROP function protection ● 0b1: Flash read error under PCROP function protection An illegal read operation occurred on the protected area while the PCROP function is enabled	RO
5	COLERR	Flash Read and Write Conflict Error Flag Bit ● 0b0: No flag generated ● 0b1: Generate flag Setting conditions: ● Read and write operations on Flash when RDY is not set ● In continuous programming mode, writing to Flash 0 without setting Clearing conditions: ● Write 1 to the corresponding clear bit of EFM_FSCLR	RO
4	OPTEND	Flash Space Programming/Erasing/Full Erasing Operation End Flag Bit ● 0b0: No flag generated ● 0b1: Generate flag Setting conditions: ● End of programming/erasing/full erasing operation Clearing conditions: ● Write 1 to the corresponding clear bit of EFM_FSCLR	RO

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Bit	Name	Functional Description	Access
3	MISMTCH	Flash Space Single Programming Read-Back Value Inconsistency Flag Bit ● 0b0: No flag generated ● 0b1: Generate flag Setting conditions: ● In single programming read-back mode, the read data from Flash after programming is inconsistent with the written value Clearing conditions: ● Write 1 to the corresponding clear bit of EFM_FSCLR	RO
2	*Reserved*	-	-
1	PEPRTERR	Programming/Erasing Protected Address Error Flag Bit ● 0b0: Programming/erasing address is in an allowed rewrite area ● 0b1: Programming/erasing action performed on a protected window or write-protected address Setting conditions: ● Programming/erasing an address within the window protection area, PCROP protection area, or performing a full chip erase on Flash after PCROP is enabled Clearing conditions: ● Write 1 to the corresponding clear bit in EFM_FSCLR	RO
0	PEWERR	Mode Write Error Flag Bit ● 0b0: Writing to Flash in the permitted erase/write mode state ● 0b1: Erase/write Flash operation performed in a non-erase/write mode Setting conditions: ● Erase/write Flash operation performed in a non-erase/write mode Clearing conditions: ● Write 1 to the corresponding clear bit in EFM_FSCLR	RO

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8.4.7 Flash State Clear Register (EFM_FSCLR)

Offset	Bit Position																													
0x0014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																									RDERRCLR	COLERRCLR	OPTENDCLR	MISMTCHCLR	Reserved	PEPRTERRCLR	PEWERRCLR
Access																										RW	RW	RW	RW		RW	RW

Bit	Name	Functional Description	Access
31:7	*Reserved*	-	-
6	RDERRCLR	Read Error Flag Clear Writing 1 clears the FSR.RDERR bit, writing 0 has no effect; read value is always 0	RW
5	COLERRCLR	Clear the Read and Write Conflict Error Flag of Flash Write 1 to clear the FSR.COLERR bit, write 0 has no effect; read always returns 0	RW
4	OPTENDCLR	Clear the Space Programming/Erasing/Full Erasing End Flag of Flash Write 1 to clear the FSR.OPTEND bit, write 0 has no effect; read always returns 0	RW
3	MISMTCHCLR	Clear the Space Single Programming Read-back Value Inconsistency Flag of Flash Write 1 to clear the FSR.MISMTCH bit, write 0 has no effect; read always returns 0	RW
2	*Reserved*	-	-
1	PEPRTERRCLR	Protected Address Programming/Erasing Error Flag Clear Write 1 to clear the FSR.PEPRTERR bit, writie 0 has no effect; reading always returns 0	RW
0	PEWERRCLR	Mode Write Error Flag Clear Write 1 to clear the FSR.PEWERR bit, write 0 has no effect; reading always returns 0	RW

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8.4.8 Flash Interrupt Enable Register (EFM_FITE)

Offset	Bit Position																													
0x0018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																													COLERRITE	OPTENDITE	PEERRITE
Access																														RW	RW	RW

Bit	Name	Functional Description	Access
31:3	*Reserved*	-	-
2	COLERRITE	Read and Write Conflict Error Interrupt Enabled ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW
1	OPTENDITE	Operation End Interrupt Enabled ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW
0	PEERRITE	Programming/Erasing Error Interrupt Enabled ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW

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8.4.9 Flash Permit Start Window Register (EFM_FPMTSW)

Offset	Bit Position																													
0x0020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																FPMTSW															
Access																	RW															

Bit	Name	Functional Description	Access
31:17	*Reserved*	-	-
16:0	FPMTSW	Protection Address The start address of the area to be protected	RW

8.4.10 Flash Permit End Window Register (EFM_FPMTEW)

Offset	Bit Position																													
0x0024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																FPMTEW															
Access																	RW															

Bit	Name	Functional Description	Access
31:17	*Reserved*	-	-
16:0	FPMTEW	Protection Address The end address of the area to be protected	RW

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8.4.11 UNIQUE ID Register (EFM_UQID0)

Offset	Bit Position																													
0x0050	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	LOT_ID[7:0]								WAFER_ID								X_LOCATION								Y_LOCATION							
Access	RO								RO								RO								RO							

Bit	Name	Functional Description	Access
31:24	LOT_ID[7:0]	LOT ID Chip LOT ID [7:0]	RO
23:16	WAFER_ID	Wafer ID	RO
15:8	X_LOCATION	X-Coordinate X-coordinate of the chip on the Wafer	RO
7:0	Y_LOCATION	Y-Coordinate Y-coordinate of the chip on the Wafer	RO

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8.4.12 UNIQUE ID Register (EFM_UQID1)

Offset	Bit Position																													
0x0054	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	LOT_ID[39:8]																															
Access	RO																															

Bit	Name	Functional Description	Access
31:0	LOT_ID[39:8]	LOT ID Chip LOT ID [39:8]	RO

8.4.13 UNIQUE ID Register (EFM_UQID2)

Offset	Bit Position																													
0x0058	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	PTNMFG																Reserved								LOT_ID[47:40]							
Access	RO																								RO							

Bit	Name	Functional Description	Access
31:16	PTNMFG	Product Name Mark Product PART NAME identification mark For example, 0xF431 indicates F431	RO
15:8	*Reserved*	-	-
7:0	LOT_ID[47:40]	LOT ID Chip LOT ID[47:40]	RO

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8.4.14 Flash Ocd Protect Flag Register (EFM_FOCDPRTFG)

Offset	Bit Position																															
0x0070	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																												PCROPST	Reserved		
Access																													RO			

Bit	Name	Functional Description	Access
31:4	*Reserved*	-	-
3	PCROPST	PCROP Function Flag Bit ● 0b0: PCROP function disabled ● 0b1: PCROP function enabled	RO
2:0	*Reserved*	-	-

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8.4.15 Flash CRC Data Out Register (EFM_FCRCDOR)

Offset	Bit Position																													
0x0120	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	DOR																															
Access	RO																															

Bit	Name	Functional Decription	Access
31:0	DOR	FCRC calculation result	RO

8.4.16 Flash PCROP Set Flag Register (EFM_FPCROPFG)

Offset	Bit Position																													
0x0128	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	PCROPER																PCROPSR															
Access	RO																RO															

Bit	Name	Functional Description	Access
31:16	PCROPER	PCROP Protection End Sector ● 0: Sector 0 ● 1: Sector 1 ● 2: Sector 2 ● ... ● 255: Sector 255 **Note** The function is invalid if PCROPER ≥ PCROPSR or if it is all ones.	RO
15:0	PCROPSR	PCROP Protection Start Sector ● 0: Sector 0 ● 1: Sector 1 ● 2: Sector 2 ● ... ● 255: Sector 255 **Notice** Do not set Sector 0 as a protected area.	RO

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8.5 Precautions

1. When erasing and writing to Flash, resetting or erasing/writing operation can forcibly stop the action and the Flash data cannot be guaranteed. Users can perform only after disabling the reset and erasing the address.
2. After the erasing/writing operation is completed, the hardware circuit automatically reset the cache loop.
3. Repeated programming on the same address cannot ensure the correctness of the data.
4. In continuous programming mode, the Flash analog circuit is in a high-voltage state. A long-term high-voltage state can affect the Flash features. Once continuous programming is completed, exit immediately. MCU is disabled to enter low power mode (Sleep mode, Stop mode) in continuous programming mode.
5. When the bus is in release state (EFM_FWMC.BUSHLDCTL=1) during programming and erasing, set the vectors and subroutines to RAM.
6. Continuously changing the programming/erasing mode (EFM_FWMC.PEMOD) may cause the write to fail, requiring a repeated write.

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9 Built-in SRAM (SRAM)

9.1 Introduction

This product has 16KB system SRAM (SRAMH/SRAM1).

Each SRAM can be accessed as a byte, half-word (16 bits), or full-word (32 bits). All SRAM read and write operations can be performed at the fastest CPU speed (120MHz) with 0 wait period (i.e., in 1 clock cycle).

SRAM1 and SRAMH have a parity check, with one check bit for each byte of data. When the RAM parity check reset function is enabled, an SRAM parity check reset will be generated if a parity error occurs during the reading of SRAM data.

9.2 Functional Description

9.2.1 SRAM Space Allocation

Table 9-1 SRAM Space Allocation

Name	Capacity	Address Range	Check Mode
SRAM1	8KB	0x20000000-0x20001FFF	Parity check
SRAMH	8KB	0x1FFFE000-0x1FFFFFFF	Parity check

9.3 Precautions

1. A SRAM parity check reset will occur when reading from an uninitialized SRAM address.
2. When NMI interrupts or resets triggered by RAM parity errors are allowed, the entire RAM space to be used must be initialized on a word-by-word basis during data access operations.

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10 General-Purpose I/O (GPIO)

10.1 Introduction

Some of the abbreviations used in this chapter are:

- Px (x=0 to 5,7,9,A,B,D,E) represents a group of ports, such as P0 represents a group of 3 I/O ports P00-PA02.
- Pxy (x=0 to 5,7,9,A,B,D,E, y=0-7, the same below) represents a single I/O port, such as the P11 port represents the 2rd I/O in the P1 group.
- General Purpose Input Output (GPIO).
- NOD (Nmos Open Drain) NMOS open drain output mode.

10.2 Features

- Each port group has 8 I/O pins, which may be less than 8 depending on actual configuration
- Supports pull-up input
- Supports push-pull, open-drain output mode
- Supports high and low drive modes
- Supports free switching between CMOS/Schmitt input modes
- Supports for external interrupt input
- Supports I/O pin peripheral function multiplexing, one I/O pin can have up to 10 optional multiplexing functions
- Individual I/O pins can be programmed independently

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10.3 Functional Description

10.3.1 Function Block Diagram

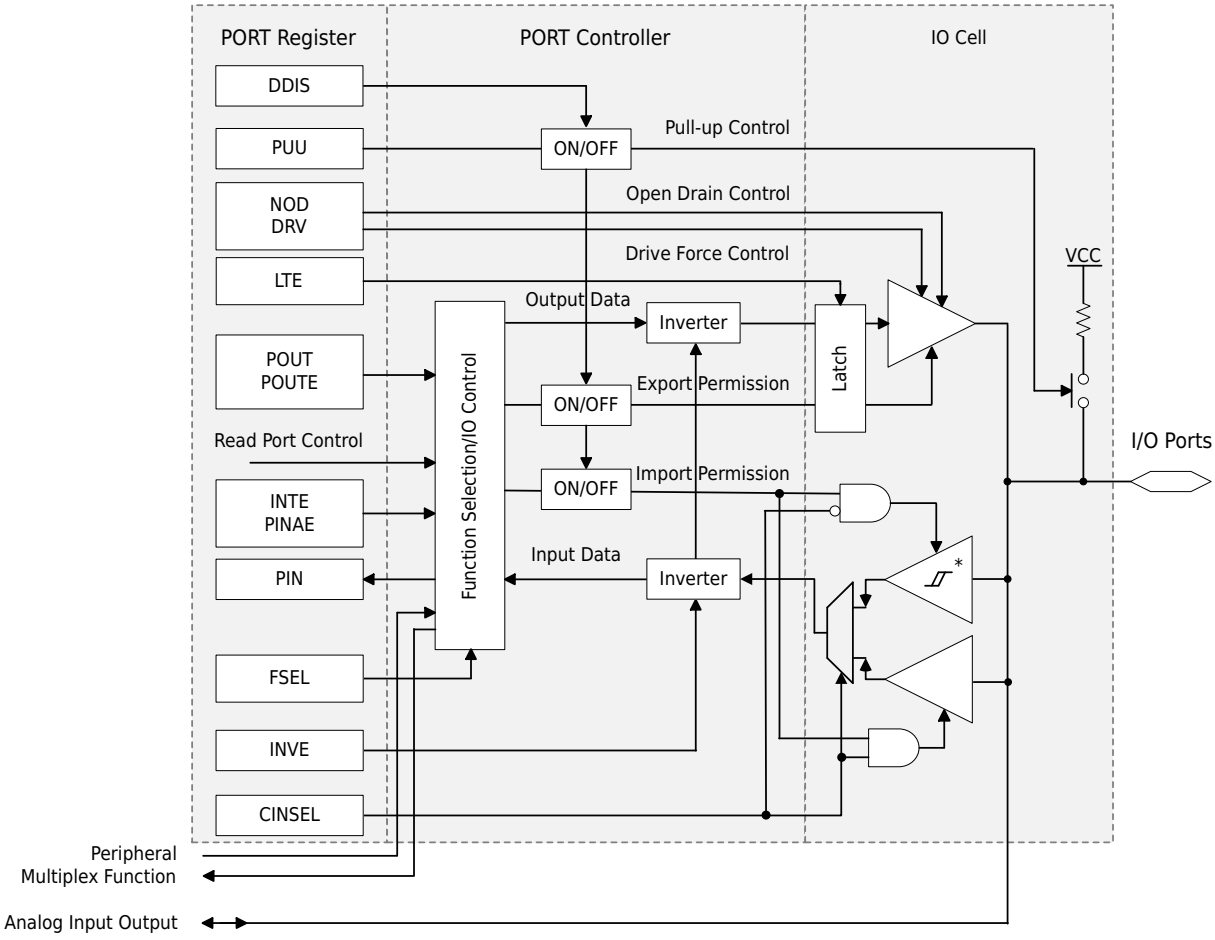

Figure 10-1 Port Basic Structure Diagram

For detailed GPIO port number, and drive capability configuration, please refer to the "Pin Definitions" chapter in the "Datasheet".

10.3.2 General Input/Output GPIO Function

General Input Function GPI

Each I/O has a general-purpose input GPI function, and when the digital function disable bit PCRxy.DDIS is 0, the GPI function is always enabled, regardless of the setting value of PFSRxy.FSEL. The status of the current port can be obtained by accessing port input data register PIDRx. The corresponding single I/O port status can also be queried through the register PCRxy.PIN, and the PIDRx.PINy register bit is equivalent to the PCRxy.PIN bit.

By default, I/O input MOS is turned off to reduce power consumption. Only when the PIDRx or PCRxy register is read, I/O input MOS is opened. If required, you can also set the register PINAER.PINAEx to 1 to keep the I/O input MOS in the open state.

When the system runs at a high-speed clock and PINAER is set to 0, the input status value may not be read correctly in a single period due to the delay of the I/O input. At this time, it is necessary to set the register PCCR.RDWT and insert several wait periods. For details, refer to the description of the PCCR register.

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General Output Function GPO

Except for input-specific ports, other I/O ports have general output GPO capabilities. The GPO function can be enabled by setting the port function selection register PFSRxy.FSEL to 0x0.

When the GPO function is active, the output value can be controlled by setting the generic output permission register POERx to enable or disable the output of I/O and the generic output data register PODRx. The output values of I/O can also be controlled using the following three registers: PORRx register, POSRx register, and POTRx register. Writing 1 to the corresponding bits in the register can make the corresponding I/O output 0, 1, invert. I/O output status does not change at write 0.

The above registers each operate on a group of 8 PORTs. For easy control of a single I/O, I/O output can also be allowed or disabled by setting PCRxy.POUTE, where the PCRxy.POUTE register bit is equivalent to POERx.POUTEy. The output value of I/O can be controlled by setting PCRxy.POUT, where the PCRxy.POUT register bit is equivalent to PODRx.POUTy. PCRxy is suitable for controlling a single PORT and POERx/PODRx is suitable for controlling 8-bit set of PORTs.

After the system is reset, except for the SDW multiplexing ports PB1/PB2, the initial functions of other ports are GPO (PFSRxy.FSEL=0x0) and are in high-impedance state (output disabled POUTE=0).

Note

Port P50 is multiplexed with MD. When the reset port NRST is released, P50/MD must be fixed to a low level so that the system can enter user mode. After the mode is established, P50 can be used as a normal IO.

10.3.3 Peripheral Function

Through the register PFSRxy.FSEL, each port can configure up to 10 functions. These include the generic output GPO function corresponding to FSEL=0x0. For the specific functions of each port configuration, please refer to the "Pin Definitions-Pin Function Description" in the "Datasheet".

SWD/TOOL0 debug function, use the register PSPCR to select. PSPCR.SPFE[z], when z=0-1 is 1, the PFSRxy.FSEL bit of the corresponding port is disabled, that is, the priority of SPFE is higher than that of FSEL. The initial value of the PSPCR register is 0x03, and the SWD/TOOL0 function is enabled. If you want to set these ports as functions other than SWD/TOOL0, you need to write 0 to the corresponding SPFE[z] bit first.

10.3.4 External Interrupt EIRQ Input Function

Most of the I/O ports have an external interrupt input function. When the PCRxy.INTE bit is set to 1, this I/O will be enabled as the external interrupt source EIRQy input (for example: P00 corresponds to EIRQ2, P01 corresponds to EIRQ4). Each EIRQy can be configured with more than one I/O. Please do not allow multiple I/O inputs simultaneously for each EIRQy.

When I/O port is used as external interrupt EIRQ, I/O port needs to combine with interrupt controller INTC, set filter, interrupt trigger edge, interrupt number and so on. For details, please refer to the relevant description in the "Interrupt Controller (INTC)" chapter.

10.3.5 Analog Function

Some I/O ports have analog input and output functions (including primary oscillators). When used as an analog function, please write 1 to the register PCRxy.DDIS to disable the digital function of the current port.

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10.3.6 General Control

The general control functions described below are independent of the specific function selected for the port, i.e., the setting of PFSRxy.FSEL, unless otherwise specified.

Pull Up Resistor

Each I/O port has an internal pull-up resistor. The PCRxy.PUU bit of the register can be set to allow this function. When there is no input to the I/O port, the internal part is in a weak pull-up state. Pull-up is automatically disable when the I/O port is in the output state.

Note

When the I/O port selects the I2Cx_SCL/I2Cx_SDA function, the setting of the register PUU will be ignored, and the internal pull-up function will be forced to be disabled.

Drive Capability Control

Each I/O port has 2 levels of high and low drive capability adjustable, and the register PCRxy.DRV can be set as required.

This feature is only enable if the port is in the output state.

Open-drain Output Mode

Set the PCRxy.NOD bit to set the I/O port to NMOS open-drain output mode. When NOD is active, the corresponding port can output 0 normally, and the port will be in high resistance state when output 1.

When the I/O port selects the I2Cx_SCL/I2Cx_SDA function, the setting of the register NOD will be ignored, and the open-drain output mode is forced to be enabled.

CMOS/Schmitt Input Mode

Each I/O port supports two input modes: CMOS and Schmitt. You can set the register PCRxy.CINSEL bit option, setting it to 0 means Schmitt input, and setting it to 1 means CMOS input. The default is Schmitt input.

When using the I/O input function, please set the input type according to actual needs.

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10.4 Register Description

In this section, general-purpose registers (including PIDRx, PODRx, POERx, POSRx, PORRx, POTRx) support 8-bit, 16-bit, and 32-bit access; other registers (including PSPCR, PCCR, PINAER, PWPR, PCRxy, PFSRxy) support 16-bit and 32-bit access. These registers are combined as follows for 32-bit access:

Table 10-1 PORT Register List for 32-bit Access

Address	Bit31-Bit24	Bit23-Bit16	Bit15-Bit8	Bit7-Bit0
0x40053800+0x4*m	PIDR(z+3)	PIDR(z+2)	PIDR(z+1)	PIDRz
0x40053810+0x4*m	PODR(z+3)	PODR(z+2)	PODR(z+1)	PODRz
0x40053820+0x4*m	POER(z+3)	POER(z+2)	POER(z+1)	POERz
0x40053830+0x4*m	POSR(z+3)	POSR(z+2)	POSR(z+1)	POSRz
0x40053840+0x4*m	PORR(z+3)	PORR(z+2)	PORR(z+1)	PORRz
0x40053850+0x4*m	POTR(z+3)	POTR(z+2)	POTR(z+1)	POTRz
0x40053B00	Reserved		PSPCR	
0x40053B04	PINAER		PCCR	
0x40053B08	Reserved		PWPR	
0x40053C00+0x20*n+0x4*y	PFSRxy		PCRxy	

Note

Unless otherwise specified, all register offset calculation formulas in this section are:

- For m=0-3, z is a hexadecimal number, with the following correspondence: when m=0, z=0; when m=1, z=4; when m=2, z=8; when m=3, z=C. For non-existent registers, the read value will always be 0.
- x=0-5,7,9,A,B,D,E corresponds to n=0-5,7,9,A,B,D,E, y=0-7.

10.4.1 Register List

Base address: 0x40053800

Table 10-2 General-Purpose IO (GPIO) Register Offset

Offset	Register	Description	Width
0x00+0x1*n	PIDRx	General Input Data Register (x=0 to 5,7,9,A,B,D,E)	8
0x10+0x1*n	PODRx	General Output Data Register (x=0 to 5,7,9,A,B,D,E)	8
0x20+0x1*n	POERx	General Output Enable Register (x=0 to 5,7,9,A,B,D,E)	8
0x30+0x1*n	POSRx	General Output Set Register (x=0 to 5,7,9,A,B,D,E)	8
0x40+0x1*n	PORRx	General Output Reset Register (x=0 to 5,7,9,A,B,D,E)	8

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Offset	Register	Description	Width
0x50+0x1*n	POTRx	General Output Toggle Register (x=0 to 5,7,9,A,B,D,E)	8
0x300	PSPCR	Special Control Register	16
0x304	PCCR	Common Control Register	16
0x306	PINAER	Input Control Register	16
0x308	PWPR	Write Protection Register	16
0x400+0x0x20*n+0x4*y	PCRxy	General Control Register (x=0 to 5,7,9,A,B,D,E)	16
0x402+0x0x20*n+0x4*y	PFSRxy	Function Select Register (x=0 to 5,7,9,A,B,D,E)	16

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10.4.2 General Input Data Register (PIDRx)

Offset: 0x00+0x1*n

Offset	Bit Position							
-	7	6	5	4	3	2	1	0
Reset	0xXX							
Name	PIN7	PIN6	PIN5	PIN4	PIN3	PIN2	PIN1	PIN0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Bit	Name	Functional Description	Access
7:0	PINy (y=7-0)	Input Status Corresponding to Px7-Px0 ports respectively: ● 0b0: I/O port input state is low level ● 0b1: I/O port input state is high level	RO

Note

When the port digital function is not disabled (PCRxy.DDIS=0), the input status of the port can be obtained by reading this register, regardless of the setting value of the function selection register PFSRxy.FSEL.

There is no variable read value for the corresponding bit of the port.

When the port digital function is disabled (PCRxy.DDIS=1), since the I/O input MOS is in the off state, the corresponding PIN bit read value is a fixed value 0x0.

10.4.3 General Output Data Register (PODRx)

Offset: 0x10+0x1*n

Offset	Bit Position							
-	7	6	5	4	3	2	1	0
Reset	0x00							
Name	POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0
Access	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
7:0	POUTy (y=7-0)	Output Data Corresponding to Px7-Px0 ports respectively: ● 0b0: Output low level ● 0b1: Output high level	RW

Note

Override this register to change the output status of the corresponding port when the I/O port is set to GPO.

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10.4.4 General Output Enable Register (POERx)

Offset: 0x20+0x1*n

Offset	Bit Position							
-	7	6	5	4	3	2	1	0
Reset	0x00							
Name	POUTE7	POUTE6	POUTE5	POUTE4	POUTE3	POUTE2	POUTE1	POUTE0
Access	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
7:0	POUTEy (y=7-0)	Output Enable Corresponding to Px7-Px0 ports respectively: ● 0b0: Output disabled ● 0b1: Output enabled	RW

Note

When the I/O port is set to GPO and this register is set to 1, the PODRx setting is output to the corresponding I/O port. When this register is set to 0, the output is closed and the port is in high resistance state.

It is forbidden to set the corresponding bit of a non-existent port to 1.

10.4.5 General Output Set Register (POSRx)

Offset: 0x30+0x1*n

Offset	Bit Position							
-	7	6	5	4	3	2	1	0
Reset	0x00							
Name	POS7	POS6	POS5	POS4	POS3	POS2	POS1	POS0
Access	WO	WO	WO	WO	WO	WO	WO	WO

Bit	Name	Functional Description	Access
7:0	POSy (y=7-0)	Output Height Corresponding to Px7-Px0 ports respectively: ● 0b0: The corresponding PODRx.POUTy does not change ● 0b1: The corresponding PODRx.POUTy is set to 1	WO

Note

The read value for this register is always 0. In 32-bit/16-bit access, when PORy and POSy of the same I/O are written to 1 at the same time, PORy has a higher priority, that is, the corresponding POUTy is cleared.

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10.4.6 General Output Reset Register (PORRx)

Offset: 0x40+0x1*n

Offset	Bit Position							
-	7	6	5	4	3	2	1	0
Reset	0x00							
Name	POR7	POR6	POR5	POR4	POR3	POR2	POR1	POR0
Access	WO	WO	WO	WO	WO	WO	WO	WO

Bit	Name	Functional Description	Access
7:0	PORy (y=7-0)	Output Low Corresponding to Px7-Px0 ports respectively: ● 0b0: The corresponding PODRx.POUTy does not change ● 0b1: The corresponding PODRx.POUTy is cleared	WO

Note

The read value for this register is always 0.

10.4.7 General Output Toggle Register (POTRx)

Offset: 0x50+0x1*n

Offset	Bit Position							
-	7	6	5	4	3	2	1	0
Reset	0x00							
Name	POT7	POT6	POT5	POT4	POT3	POT2	POT1	POT0
Access	WO	WO	WO	WO	WO	WO	WO	WO

Bit	Name	Functional Description	Access
7:0	POTy (y=7-0)	Output Inversion Corresponding to Px7-Px0 ports respectively: ● 0b0: The corresponding PODRx.POUTy does not change ● 0b1: The corresponding PODRx.POUTy is inverted	WO

Note

The read value for this register is always 0.

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10.4.8 Special Control Register (PSPCR)

Offset	Bit Position															
0x300	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0003															
Name	Reserved														SPFE[1:0]	
Access															RW	

Bit	Name	Functional Description	Access
15:2	*Reserved*	-	-
1	SPFE[1]	Special Function Selection ● 0b0: TOOL0 function disabled ● 0b1: TOOL0 function enabled	RW
0	SPFE[0]	Special Function Selection ● 0b0: SWCLK/SWDIO function disabled ● 0b1: SWCLK/SWDIO function enabled	RW

Note

The PSPCR.SPFE have higher priority than the PFSRxy.FSEL.

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10.4.9 Common Control Register (PCCR)

Offset	Bit Position															
0x304	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x4000															
Name	RDWT		Reserved													
Access	RW															

Bit	Name	Functional Description	Access
15:14	RDWT	Read Port Waiting Set the number of wait periods inserted when reading register PIDRx and PCRxy	RW
13:0	*Reserved*	-	-

Operating Frequency	Minimum Waiting Period	Setting Value
0<HCLK≤40MHz	0 period	0b00-0b11
40MHz<HCLK≤80MHz	1 period	0b01-0b11
80MHz<HCLK≤120MHz	2 periods	0b10-0b11

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10.4.10 Input Control Register (PINAER)

Offset	Bit Position															
0x306	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	PINAE															
Access	RW															

Bit	Name	Functional Description	Access
15:0	PINAE	Input Normally-Open ● 0b0: Input MOS normally-open disabled ● 0b1: Input MOS normally-open enabled The correspondence between each bit of PINAE and the I/O port is: ● PINAE[0] Control P00-P02 ● PINAE[1] Control P10, P11 ● PINAE[2] Control P22-P24 ● PINAE[3] Control P30-P33, P36, P37 ● PINAE[4] Control P40-P47 ● PINAE[5] Control P50 ● PINAE[7] Control P70-P76 ● PINAE[9] Control P91-P94 ● PINAE[10] Control PA2-PA5 ● PINAE[11] Control PB0-PB7 ● PINAE[13] Control PD3-PD7 ● PINAE[14] Control PE2	RW

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10.4.11 Write Protection Register (PWPR)

Offset	Bit Position															
0x308	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	WP								Reserved							WE
Access	WO															RW

Bit	Name	Functional Description	Access
15:8	WP	Write Protection Code When WE needs to be set to 1, 0xA5 must be written to WP at the same time; read always returns 0	WO
7:1	*Reserved*	-	-
0	WE	Write Enable ● 0b0: PSPCR, PCCR, PCRxy, PFSRxy register write disabled ● 0b1: PSPCR, PCCR, PCRxy, PFSRxy register write enabled	RW

Note

Writing 0xA501 to this register will set WE to 1; writing other values will clear WE to 0.

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10.4.12 General Control Register (PCRxy)

Offset: 0x400+0x0x20*n+0x4*y

Offset	Bit Position															
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0X00															
Name	DDIS	Reserved			INTE	CINSEL	INVE	PIN	Reserved	PUU	LTE	DRV	Reserved	NOD	POUTE	POUT
Access	RW				RW	RW	RW	RO		RW	RW	RW		RW	RW	RW

Bit	Name	Functional Description	Access
15	DDIS	Digital Function Disabled ● 0b0: Digital function enabled ● 0b1: Digital function disabled	RW
14:12	*Reserved*	-	-
11	INTE	External Interrupt Enabled ● 0b0: External interrupt input disabled ● 0b1: External interrupt input enabled	RW
10	CINSEL	Input Modes Selection ● 0b0: Schmitt input ● 0b1: CMOS input	RW
9	INVE	Inverse Enabled ● 0b0: Input and output data not inverted ● 0b1: Input and output data inverted	RW
8	PIN	Input Status ● 0b0: I/O port input state is low level ● 0b1: I/O port input state is high level The function is consistent with the register PIDRx.PINy	RO
7	*Reserved*	-	-
6	PUU	Pull-up Enabled ● 0b0: Internal pull-up resistor disabled ● 0b1: Internal pull-up resistor enabled	RW
5	LTE	Latch Output ● 0b0: Output latch invalid ● 0b1: Output latch valid	RW
4	DRV	Drive Mode Selection ● 0b0: Low drive force mode ● 0b1: High drive force mode	RW
3	*Reserved*	-	-

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Bit	Name	Functional Description	Access
2	NOD	NMOS Open-drain ● 0b0: Normal CMOS output mode ● 0b1: NMOS open-drain output mode	RW
1	POUTE	Output Permission ● 0b0: Output disabled ● 0b1: Output enabled The function is consistent with the register POERx.POUTEy	RW
0	POUT	Output Data ● 0b0: Output low level ● 0b1: Output high level The function is consistent with the register PODRx.POUTy	RW

Note

1. When DDIS is set to 1, all digital functions of the corresponding port are forcibly disabled, including general-purpose input and output, peripheral digital input and output, pull-up/pull-down functions, and external interrupt input functions. When the port is used as an analog input, please set the DDIS bit to 1.
2. When LTE is set to 1 Output Lock active, the current output status of the port remains until LTE is written to 0. This function is mainly used when the port function is switched. To avoid system malfunction caused by unexpected burrs in port output during function switching, before the function switching, the output status of the port is latched in LTE write 1, and then the register switch function is selected. Finally, the LTE write 0 is unlatched and the port status is updated to a new function.
3. When INVE is set to 1, the input and output data of the port will be inverted, including the GPIO function and other peripheral input and output functions.
4. CINSEL is used to set the I/O input mode and affects all digital input functions such as GPI, EIRQ and peripheral inputs. After selecting the I2C function using PFSRxy.FSEL, the CMOS/Schmitt input of this I/O will be controlled by the I2C module.

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10.4.13 Function Select Register (PFSRxy)

Offset: 0x402+0x0x20*n+0x4*y

Offset	Bit Position															
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved												FSEL			
Access													RW			

Bit	Name	Functional Description	Access
15:4	*Reserved*	-	-
3:0	FSEL	Function Selection For the function configuration of each port, refer to the "Pin Definitions-Pin Function Description" in Datasheet.	RW

Note

- I/O port can select one of several features configured on the port via FSEL. Setting FSEL to 0 means selecting Func0, setting it to 1 means selecting Func1, and so on. Setting it to 15 means selecting Func15. The general output function GPO corresponding to Func0.
- After reset, the initial state of the PB1 and PB2 ports is that the SWD function is enabled. When configuring the FSEL to select a function, you must first write 0 to PSPCR.SPFE[0] to disable the SWD function.
- Port P50 is multiplexed with MD. When the reset port NRST is released, P50/MD must be held low to allow the system to enter user mode. After the mode is established, when configuring the FSEL to select a function, you must first write 0 to PSPCR.SPFE[1] to disable the TOOL0 function.

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10.5 Precautions

1. Do not set the same feature to multiple ports.
2. When using the analog function, please turn off the digital function of the corresponding port (PCRxy.DDIS=0b1).
3. Please switch the port function when the output latch enabled (PCRxy.LTE=0b1) to avoid unexpected glitches on the port output during switching.

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11 Interrupt Controller (INTC)

11.1 Introduction

The interrupt controller (INTC) selects an interrupt event as an interrupt request and sends it to NVIC to wake up WFI; selects interrupt event as event input (RXEV) to wake up WFE; select low power consumption mode (Sleep mode and Stop mode) of interrupt event wake-up system ; control external interrupts and software interrupts.

The main features of INTC are as follows:

1. Maskable interrupts: INTC is equipped with 124 interrupt events, which are processed and sent to NVIC as interrupt requests (IRQ). It supports 74 IRQs, each IRQ corresponds to one or more interrupt events.

   Note
   For more instructions on exception and NVIC programming, please refer to the "Arm Cortex-M4 Processor Technical Reference Manual".

2. Programmable priority of NVIC: 16 programmable priorities (4-bit interrupt priority register is used).
3. Non-maskable interrupts: Multiple system interrupt event requests can be independently selected as non-maskable interrupts, and each interrupt event is equipped with independent enable, flag and flag clear registers.
4. Equipped with 8 external pin interrupt events.
5. Equipped with multiple interrupt events, please refer to the "Interrupt Event List" for the specific number.
6. Equipped with 24 software interrupt events.
7. Interrupt wakes up system Sleep mode and Stop mode.

Table 11-1 External Interrupt Input Pin

Pin Name	I/O	Description
EIRQ0	Input	External Interrupt Event 0
EIRQ1	Input	External Interrupt Event 1
EIRQ2	Input	External Interrupt Event 2
EIRQ3	Input	External Interrupt Event 3
EIRQ4	Input	External Interrupt Event 4
EIRQ5	Input	External Interrupt Event 5
EIRQ6	Input	External Interrupt Event 6
EIRQ7	Input	External Interrupt Event 7

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11.2 Vector Digraph

11.2.1 Interrupt Vector Digraph

Table 11-2 Interrupt Vector Table

Vector Address	Vector No.	IRQ No.	Interrupt Source	Description
ARM Core Interrupts				
0x00000000	0	-	ARM core	Initial Stack Pointer
0x00000004	1	-	ARM core	Initial Program Counter
0x00000008	2	-	ARM core	Non-maskable Interrupt (NMI)
0x0000000C	3	-	ARM core	Hard Fault
0x00000010	4	-	ARM core	Mem Manage Fault
0x00000014	5	-	ARM core	Bus Fault
0x00000018	6	-	ARM core	Usage Fault
0x0000001C	7	-	ARM core	Reserved
0x00000020	8	-	ARM core	Reserved
0x00000024	9	-	ARM core	Reserved
0x00000028	10	-	ARM core	Reserved
0x0000002C	11	-	ARM core	Supervisor Call (SVCall)
0x00000030	12	-	ARM core	Debug Monitor
0x00000034	13	-	ARM core	Reserved
0x00000038	14	-	ARM core	Pendable request for system service (PendSV)
0x0000003C	15	-	ARM core	System tick timer (SysTick)
Non-ARM Core Interrupts				
0x00000040	16	0	INTC_INTSEL0	Interrupt event/software interrupt 0 selected by register INTC_INTSEL0
0x00000044	17	1	INTC_INTSEL1	Interrupt event/software interrupt 1 selected by register INTC_INTSEL1
0x00000048	18	2	INTC_INTSEL2	Interrupt event/software interrupt 2 selected by register INTC_INTSEL2
0x0000004C	19	3	INTC_INTSEL3	Interrupt event/software interrupt 3 selected by register INTC_INTSEL3
0x00000050	20	4	INTC_INTSEL4	Interrupt event/software interrupt 4 selected by register INTC_INTSEL4
0x00000054	21	5	INTC_INTSEL5	Interrupt event/software interrupt 5 selected by register INTC_INTSEL5
0x00000058	22	6	INTC_INTSEL6	Interrupt event/software interrupt 6 selected by register INTC_INTSEL6
0x0000005C	23	7	INTC_INTSEL7	Interrupt event/software interrupt 7 selected by register INTC_INTSEL7
0x00000060	24	8	INTC_INTSEL8	Interrupt event/software interrupt 8 selected by register INTC_INTSEL8
0x00000064	25	9	INTC_INTSEL9	Interrupt event/software interrupt 9 selected by register INTC_INTSEL9
0x00000068	26	10	INTC_INTSEL10	Interrupt event/software interrupt 10 selected by register INTC_INTSEL10
0x0000006C	27	11	INTC_INTSEL11	Interrupt event/software interrupt 11 selected by register INTC_INTSEL11
0x00000070	28	12	INTC_INTSEL12	Interrupt event/software interrupt 12 selected by register INTC_INTSEL12

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Vector Address	Vector No.	IRQ No.	Interrupt Source	Description
0x00000074	29	13	INTC_INTSEL13	Interrupt event/software interrupt 13 selected by register INTC_INTSEL13
0x00000078	30	14	INTC_INTSEL14	Interrupt event/software interrupt 14 selected by register INTC_INTSEL14
0x0000007C	31	15	INTC_INTSEL15	Interrupt event/software interrupt 15 selected by register INTC_INTSEL15
0x00000080	32	16	PORT	External Interrupt 0 / Software Interrupt 16
0x00000084	33	17	PORT	External Interrupt 1 / Software Interrupt 17
0x00000088	34	18	PORT	External Interrupt 2 / Software Interrupt 18
0x0000008C	35	19	PORT	External Interrupt 3 / Software Interrupt 19
0x00000090	36	20	PORT	External Interrupt 4 / Software Interrupt 20
0x00000094	37	21	PORT	External Interrupt 5 / Software Interrupt 21
0x00000098	38	22	PORT	External Interrupt 6 / Software Interrupt 22
0x0000009C	39	23	PORT	External Interrupt 7 / Software Interrupt 23
0x000000A0	40	24	DMA	Transfer Error Interrupt
0x000000A4	41	25	DMA	Channel 0 Transfer Complete Interrupt / Channel 0 Block Transfer Complete Interrupt
0x000000A8	42	26	DMA	Channel 1 Transfer Complete Interrupt / Channel 1 Block Transfer Complete Interrupt
0x000000AC	43	27	DMA	Channel 2 Transfer Complete Interrupt / Channel 2 Block Transfer Complete Interrupt
0x000000B0	44	28	DMA	Channel 3 Transfer Complete Interrupt / Channel 3 Block Transfer Complete Interrupt
0x000000B4	45	29	EFM	Programming (Erase) Error Interrupt / Read/Write Conflict Error Interrupt
0x000000B8	46	30	EFM	Operation End Interrupt
0x000000BC	47	31	DCU	DCU Interrupt
0x000000C0	48	32	FPU	FPU Interrupt
0x000000C4	49	33	MAU	Square Root Operation Interrupt
0x000000C8	50	34	Timer0_1	Channel A, B Count Compare Match Interrupt / Input Capture Interrupt / Count Overflow Interrupt
0x000000CC	51	35	Timer0_2	Channel A, B Count Compare Match Interrupt / Input Capture Interrupt / Count Overflow Interrupt
0x000000D0	52	36	CMU	XTAL Oscillation Fault Interrupt
0x000000D4	53	37	SWDT	Count Underflow / Refresh Error Interrupt
0x000000D8	54	38	TimerA_1	Count Period Match Interrupt
0x000000DC	55	39	TimerA_1	Count Compare Match Interrupt
0x000000E0	56	40	TimerA_2	Count Period Match Interrupt
0x000000E4	57	41	TimerA_2	Count Compare Match Interrupt
0x000000E8	58	42	TimerA_3	Count Period Match Interrupt
0x000000EC	59	43	TimerA_3	Count Compare Match Interrupt
0x000000F0	60	44	TimerA_4	Count Period Match Interrupt
0x000000F4	61	45	TimerA_4	Count Compare Match Interrupt
0x000000F8	62	46	EMB	Group 0 Interrupt
0x000000FC	63	47	EMB	Group 1 Interrupt
0x00000100	64	48	Timer4	General Count Compare Match Interrupt
0x00000104	65	49	Timer4	Count Period Match Interrupt
0x00000108	66	50	Timer4	Reload Count Match Interrupt
0x0000010C	67	51	Timer4	Dedicated Count Compare Match Interrupt

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Vector Address	Vector No.	IRQ No.	Interrupt Source	Description
0x00000110	68	52	USART_1	USART_1 Interrupt (excluding TCI and RX line wake-up stop mode interrupt)
0x00000114	69	53	USART_1	USART_1_TCI Interrupt
0x00000118	70	54	SPI	SPI Interrupt
0x0000011C	71	55	TimerA_5	Count Period Match Interrupt
0x00000120	72	56	TimerA_5	Count Compare Match Interrupt
0x00000124	73	57	USART_2	USART_2 Interrupt (excluding TCI interrupt)
0x00000128	74	58	USART_2	USART_2_TCI Interrupt
0x0000012C	75	59	USART_3	USART_3 Interrupt (excluding TCI interrupt)
0x00000130	76	60	USART_3	USART_3_TCI Interrupt
0x00000134	77	61	USART_4	USART_4 Interrupt (excluding TCI interrupt)
0x00000138	78	62	USART_4	USART_4_TCI Interrupt
0x0000013C	79	63	HALL	Capture/Overflow Interrupt
0x00000140	80	64	CMP	CMP1 Interrupt
0x00000144	81	65	CMP	CMP2 Interrupt
0x00000148	82	66	CMP	CMP3 Interrupt
0x0000014C	83	67	I2C	I2C Interrupt
0x00000150	84	68	USART_1	RX Line Wake-up Stop Mode Interrupt
0x00000154	85	69	PWC	Programmable Voltage Detector 1 (PVD1) Interrupt
0x00000158	86	70	PWC	Programmable Voltage Detector 2 (PVD2) Interrupt
0x0000015C	87	71	CMU	FCM Clock Frequency Measurement Interrupt
0x00000160	88	72	WDT	Count Underflow/Refresh Error Interrupt
0x00000164	89	73	ADC	ADC Interrupt

Note

For the interrupt event number selected by the INTC_INTSEL register, see the Interrupt Event List.

IRQ numbers 74-239 correspond to vectors that are not configured for any interrupt event. Do not use them.

11.2.2 Interrupt Event List

Interrupt events are generated by peripherals and are called interrupt sources when they are input as IRQs; When used as RXEV input, it is called an event source; when used as a peripheral trigger event, it is called a trigger source; Interrupt events can also be used as a condition to return from low power mode.

SN	Interrupt Event No.	Modules	Interrupt Name	Interrupt Type(1)	Interrupt Source	Trigger Source	NVIC Interrupt Request (IRQ) Number Mapping	
							Type A (INTC_INTSEL Write Event Number)(2)	Type B (Fixed)
0	0x000	PORT	EIRQ0	P/L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[16]
1	0x001		EIRQ1	P/L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[17]
2	0x002		EIRQ2	P/L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[18]
3	0x003		EIRQ3	P/L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[19]
4	0x004		EIRQ4	P/L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[20]
5	0x005		EIRQ5	P/L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[21]

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SN	Interrupt Event No.	Modules	Interrupt Name	Interrupt Type(1)	Interrupt Source	Trigger Source	NVIC Interrupt Request (IRQ) Number Mapping	
							Type A (INTC_INTSEL Write Event Number)(2)	Type B (Fixed)
6	0x006	PORT	EIRQ6	P/L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[22]
7	0x007		EIRQ7	P/L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[23]
8	0x008		-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
9	0x009		-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
10	0x00A		-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
11	0x00B		-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
12	0x00C		-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
13	0x00D		-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
14	0x00E		-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
15	0x00F		-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
16	0x010	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
17	0x011	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
18	0x012	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
19	0x013	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
20	0x014	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
21	0x015	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
22	0x016	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
23	0x017	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
24	0x018	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
25	0x019	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
26	0x01A	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
27	0x01B	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
28	0x01C	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
29	0x01D	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
30	0x01E	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
31	0x01F	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
32	0x020	DMA	DMA_ERR	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[24]
33	0x021		DMA_TC0	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[25]
34	0x022		DMA_BTC0	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
35	0x023		DMA_TC1	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[26]
36	0x024		DMA_BTC1	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
37	0x025		DMA_TC2	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[27]
38	0x026		DMA_BTC2	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
39	0x027		DMA_TC3	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[28]
40	0x028		DMA_BTC3	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
41	0x029	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
42	0x02A	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
43	0x02B	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
44	0x02C	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
45	0x02D	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
46	0x02E	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
47	0x02F	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-

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SN	Interrupt Event No.	Modules	Interrupt Name	Interrupt Type(1)	Interrupt Source	Trigger Source	NVIC Interrupt Request (IRQ) Number Mapping	
							Type A (INTC_INTSEL Write Event Number)(2)	Type B (Fixed)
48	0x030	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
49	0x031	EFM	EFM_PEERR	P	✓	-	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[29]
50	0x032		EFM_RDCOL	P	✓	-	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
51	0x033		EFM_OPTEND	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[30]
52	0x034	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
53	0x035	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
54	0x036	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
55	0x037	DCU	DCU	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[31]
56	0x038	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
57	0x039	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
58	0x03A	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
59	0x03B	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
60	0x03C	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
61	0x03D	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
62	0x03E	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
63	0x03F	FPU	FPU_ERR	L	✓	-	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[32]
64	0x040	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
65	0x041	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
66	0x042	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
67	0x043	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
68	0x044	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
69	0x045	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
70	0x046	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
71	0x047	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
72	0x048	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
73	0x049	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
74	0x04A	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
75	0x04B	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
76	0x04C	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
77	0x04D	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
78	0x04E	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
79	0x04F	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
80	0x050	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
81	0x051	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
82	0x052	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
83	0x053	MAU	MAU_SQRT	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[33]
84	0x054	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
85	0x055	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
86	0x056	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
87	0x057	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
88	0x058	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
89	0x059	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-

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SN	Interrupt Event No.	Modules	Interrupt Name	Interrupt Type(1)	Interrupt Source	Trigger Source	NVIC Interrupt Request (IRQ) Number Mapping	
							Type A (INTC_INTSEL Write Event Number)(2)	Type B (Fixed)
90	0x05A	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
91	0x05B	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
92	0x05C	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
93	0x05D	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
94	0x05E	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
95	0x05F	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
96	0x060	Timer0_1	TMR0_1_CMPA	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[34]
97	0x061		TMR0_1_CMPB	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
98	0x062		TMR0_1_OVFA	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
99	0x063		TMR0_1_OVFB	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
100	0x064	Timer0_2	TMR0_2_CMPA	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[35]
101	0x065		TMR0_2_CMPB	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
102	0x066		TMR0_2_OVFA	P	✓	-	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
103	0x067		TMR0_2_OVFB	P	✓	-	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
104	0x068	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
105	0x069	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
106	0x06A	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
107	0x06B	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
108	0x06C	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
109	0x06D	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
110	0x06E	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
111	0x06F	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
112	0x070	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
113	0x071	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
114	0x072	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
115	0x073	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
116	0x074	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
117	0x075	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
118	0x076	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
119	0x077	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
120	0x078	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
121	0x079	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
122	0x07A	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
123	0x07B	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
124	0x07C	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
125	0x07D	XTAL	XTAL_STOP	L	✓	-	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[36]
126	0x07E	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
127	0x07F	SWDT	SWDT_REFUDF	P	✓	-	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[37]
128	0x080	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
129	0x081	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
130	0x082	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
131	0x083	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-

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SN	Interrupt Event No.	Modules	Interrupt Name	Interrupt Type(1)	Interrupt Source	Trigger Source	NVIC Interrupt Request (IRQ) Number Mapping	
							Type A (INTC_INTSEL Write Event Number)(2)	Type B (Fixed)
132	0x084	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
133	0x085	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
134	0x086	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
135	0x087	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
136	0x088	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
137	0x089	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
138	0x08A	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
139	0x08B	TimerA_1	TMRA_1_OVF	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[38]
140	0x08C		TMRA_1_UDF	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
141	0x08D		TMRA_1_CMP	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[39]
142	0x08E	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
143	0x08F	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
144	0x090	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
145	0x091	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
146	0x092	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
147	0x093	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
148	0x094	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
149	0x095	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
150	0x096	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
151	0x097	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
152	0x098	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
153	0x099	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
154	0x09A	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
155	0x09B	TimerA_2	TMRA_2_OVF	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[40]
156	0x09C		TMRA_2_UDF	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
157	0x09D		TMRA_2_CMP	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[41]
158	0x09E	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
159	0x09F	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
160	0x09B	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
161	0x0A1	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
162	0x0A2	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
163	0x0A3	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
164	0x0A4	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
165	0x0A5	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
166	0x0A6	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
167	0x0A7	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
168	0x0A8	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
171	0x0AB	TimerA_3	TMRA_3_OVF	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[42]
172	0x0AC		TMRA_3_UDF	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
173	0x0AD		TMRA_3_CMP	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[43]
174	0x0AE	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
175	0x0AF	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-

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SN	Interrupt Event No.	Modules	Interrupt Name	Interrupt Type(1)	Interrupt Source	Trigger Source	NVIC Interrupt Request (IRQ) Number Mapping	
							Type A (INTC_INTSEL Write Event Number)(2)	Type B (Fixed)
176	0x0B0	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
177	0x0B1	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
178	0x0B2	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
179	0x0B3	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
180	0x0B4	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
181	0x0B5	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
182	0x0B6	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
183	0x0B7	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
184	0x0B8	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
185	0x0B9	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
186	0x0BA	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
187	0x0BB	TimerA_4	TMRA_4_OVF	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[44]
188	0x0BC		TMRA_4_UDF	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	-
189	0x0BD		TMRA_4_CMP	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[45]
190	0x0BE	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
191	0x0BF	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
192	0x0C0	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
193	0x0C1	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
194	0x0C2	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
195	0x0C3	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
196	0x0C4	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
197	0x0C5	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
198	0x0C6	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
199	0x0C7	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
200	0x0C8	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
201	0x0C9	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
202	0x0CA	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
203	0x0CB	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
204	0x0CC	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
205	0x0CD	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
206	0x0CE	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
207	0x0CF	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
208	0x0D0	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
209	0x0D1	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
210	0x0D2	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
211	0x0D3	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
212	0x0D4	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
213	0x0D5	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
214	0x0D6	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
215	0x0D7	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
216	0x0D8	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
217	0x0D9	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-

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SN	Interrupt Event No.	Modules	Interrupt Name	Interrupt Type(1)	Interrupt Source	Trigger Source	NVIC Interrupt Request (IRQ) Number Mapping	
							Type A (INTC_INTSEL Write Event Number)(2)	Type B (Fixed)
218	0x0DA	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
219	0x0DB	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
220	0x0DC	EMB	EMB_GR0	L	√	-	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[46]
221	0x0DD		EMB_GR1	L	√	-	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[47]
222	0x0DE	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
223	0x0DF	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
224	0x0E0	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
225	0x0E1	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
226	0x0E2	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
227	0x0E3	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
228	0x0E4	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
229	0x0E5	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
230	0x0E6	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
231	0x0E7	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
232	0x0E8	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
233	0x0E9	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
234	0x0EA	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
235	0x0EB	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
236	0x0EC	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
237	0x0ED	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
238	0x0EE	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
239	0x0EF	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
240	0x0F0	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
241	0x0F1	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
242	0x0F2	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
243	0x0F3	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
244	0x0F4	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
245	0x0F5	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
246	0x0F6	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
247	0x0F7	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
248	0x0F8	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
249	0x0F9	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
250	0x0FA	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
251	0x0FB	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
252	0x0FC	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
253	0x0FD	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
254	0x0FE	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
255	0x0FF	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
256	0x100	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
257	0x101	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
258	0x102	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
259	0x103	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-

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SN	Interrupt Event No.	Modules	Interrupt Name	Interrupt Type(1)	Interrupt Source	Trigger Source	NVIC Interrupt Request (IRQ) Number Mapping	
							Type A (INTC_INTSEL Write Event Number)(2)	Type B (Fixed)
260	0x104	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
261	0x105	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
262	0x106	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
263	0x107	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
264	0x108	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
265	0x109	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
266	0x10A	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
267	0x10B	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
268	0x10C	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
269	0x10D	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
270	0x10E	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
271	0x10F	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
272	0x110	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
273	0x111	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
274	0x112	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
275	0x113	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
276	0x114	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
277	0x115	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
278	0x116	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
279	0x117	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
280	0x118	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
281	0x119	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
282	0x11A	-	-	-	-	-	-	-
283	0x11B	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
284	0x11C	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
285	0x11D	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
286	0x11E	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
287	0x11F	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
288	0x120	Timer4	TMR4_GCMUH	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[48]
289	0x121		TMR4_GCMUL	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
290	0x122		TMR4_GCMVH	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
291	0x123		TMR4_GCMVL	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
292	0x124		TMR4_GCMWH	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
293	0x125		TMR4_GCMWL	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
294	0x126		TMR4_GCMXH	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
295	0x127		TMR4_GCMXL	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
296	0x128		TMR4_GOVF	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[49]
297	0x129		TMR4_GUDF	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
298	0x12A		TMR4_GRLU	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[50]
299	0x12B		TMR4_GRLV	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
300	0x12C		TMR4_GRLW	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
301	0x12D		TMR4_GRLX	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑

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SN	Interrupt Event No.	Modules	Interrupt Name	Interrupt Type(1)	Interrupt Source	Trigger Source	NVIC Interrupt Request (IRQ) Number Mapping	
							Type A (INTC_INTSEL Write Event Number)(2)	Type B (Fixed)
302	0x12E	Timer4	TMR4_SCM0	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[51]
303	0x12F		TMR4_SCM1	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
304	0x130		TMR4_SCM2	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
305	0x131		TMR4_SCM3	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
306	0x132		TMR4_SCM4	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
307	0x133		TMR4_SCM5	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
308	0x134		TMR4_SCM6	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
309	0x135		TMR4_SCM7	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
310	0x136	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
311	0x137	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
312	0x138	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
313	0x139	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
314	0x13A	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
315	0x13B	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
316	0x13C	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
317	0x13D	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
318	0x13E	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
319	0x13F	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
320	0x140	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
321	0x141	USART_1	USART_1_EI	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[52]
322	0x142		USART_1_RI	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
323	0x143		USART_1_TI	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
324	0x144		USART_1_RTO	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
325	0x145		USART_1_TENDI	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
326	0x146		USART_1_TCI	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[53]
327	0x147	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
328	0x148	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
329	0x149	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
330	0x14A	SPI	SPI_SPRI	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[54]
331	0x14B		SPI_SPTI	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
332	0x14C		SPI_SPII	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
333	0x14D		SPI_SPEI	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
334	0x14E		SPI_SPEND	P	-	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
335	0x14F	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
336	0x150	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
337	0x151	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
338	0x152	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
339	0x153	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
340	0x154	TimerA_5	TMRA_5_OVF	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[55]
341	0x155		TMRA_5_UDF	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
342	0x156		TMRA_5_CMP	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[56]
343	0x157	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-

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SN	Interrupt Event No.	Modules	Interrupt Name	Interrupt Type(1)	Interrupt Source	Trigger Source	NVIC Interrupt Request (IRQ) Number Mapping	
							Type A (INTC_INTSEL Write Event Number)(2)	Type B (Fixed)
344	0x158	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
345	0x159	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
346	0x15A	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
347	0x15B	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
348	0x15C	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
349	0x15D	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
350	0x15E	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
351	0x15F	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
352	0x160	USART_2	USART_2_BRKWKPI	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[57]
353	0x161		USART_2_EI	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
354	0x162		USART_2_RI	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
355	0x163		USART_2_TI	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
356	0x164		USART_2_RTO	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
357	0x165		USART_2_TENDI	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
358	0x166		USART_2_TCI	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[58]
359	0x167	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
360	0x168	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
361	0x169	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
362	0x16A	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
363	0x16B	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
364	0x16C	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
365	0x16D	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
366	0x16E	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
367	0x16F	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
368	0x170	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
369	0x171	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
370	0x172	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
371	0x173	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
372	0x174	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
373	0x175	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
374	0x176	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
375	0x177	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
376	0x178	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
377	0x179	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
378	0x17A	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
379	0x17B	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
380	0x17C	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
381	0x17D	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
382	0x17E	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
383	0x17F	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-

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SN	Interrupt Event No.	Modules	Interrupt Name	Interrupt Type(1)	Interrupt Source	Trigger Source	NVIC Interrupt Request (IRQ) Number Mapping	
							Type A (INTC_INTSEL Write Event Number)(2)	Type B (Fixed)
384	0x180	USART_3	USART_3_BRKWKPI	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[59]
385	0x181		USART_3_EI	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
386	0x182		USART_3_RI	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
387	0x183		USART_3_TI	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
388	0x184		USART_3_RTO	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
389	0x185		USART_3_TENDI	L	✓	-	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
390	0x186		USART_3_TCI	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[60]
391	0x187	USART_4	USART_4_BRKWKPI	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[61]
392	0x188		USART_4_EI	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
393	0x189		USART_4_RI	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
394	0x18A		USART_4_TI	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
395	0x18B		USART_4_RTO	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
396	0x18C		USART_4_TENDI	L	✓	-	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
397	0x18D		USART_4_TCI	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[62]
398	0x18E	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
399	0x18F	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
400	0x190	HALL	HALL_CMP	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[63]
401	0x191	HALL	HALL_OVF	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
402	0x192	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
403	0x193	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
404	0x194	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
405	0x195	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
406	0x196	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
407	0x197	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
408	0x198	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
409	0x199	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
410	0x19A	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
411	0x19B	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
412	0x19C	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
413	0x19D	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
414	0x19E	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
415	0x19F	AOS	AOS_STRG	P	-	✓	-	-
416	0x1A0	CMP	CMP_1_IRQ	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[64]
417	0x1A1		CMP_2_IRQ	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[65]
418	0x1A2		CMP_3_IRQ	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[66]
419	0x1A3	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
420	0x1A4	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
421	0x1A5	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
422	0x1A6	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
423	0x1A7	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
424	0x1A8	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
425	0x1A9	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-

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SN	Interrupt Event No.	Modules	Interrupt Name	Interrupt Type(1)	Interrupt Source	Trigger Source	NVIC Interrupt Request (IRQ) Number Mapping	
							Type A (INTC_INTSEL Write Event Number)(2)	Type B (Fixed)
426	0x1AA	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
427	0x1AB	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
428	0x1AC	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
429	0x1AD	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
430	0x1AE	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
431	0x1AF	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
432	0x1B0	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
433	0x1B1	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
434	0x1B2	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
435	0x1B3	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
436	0x1B4	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
437	0x1B5	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
438	0x1B6	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
439	0x1B7	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
440	0x1B8	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
441	0x1B9	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
442	0x1BA	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
443	0x1BB	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
444	0x1BC	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
445	0x1BD	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
446	0x1BE	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
447	0x1BF	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
448	0x1C0	I2C	I2C_RXI	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[67]
449	0x1C1		I2C_TXI	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
450	0x1C2		I2C_TEI	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
451	0x1C3		I2C_EEI	L	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
452	0x1C4	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
453	0x1C5	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
454	0x1C6	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
455	0x1C7	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
456	0x1C8	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
457	0x1C9	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
458	0x1CA	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
459	0x1CB	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
460	0x1CC	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
461	0x1CD	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
462	0x1CE	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
463	0x1CF	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
464	0x1D0	USART_1	USART_1_WUPI	Edge	✓	-	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[68]
465	0x1D1	PVD	PVD_PVD1	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[69]
466	0x1D2		PVD_PVD2	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[70]
467	0x1D3	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-

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SN	Interrupt Event No.	Modules	Interrupt Name	Interrupt Type(1)	Interrupt Source	Trigger Source	NVIC Interrupt Request (IRQ) Number Mapping	
							Type A (INTC_INTSEL Write Event Number)(2)	Type B (Fixed)
468	0x1D4	FCM	FCMFERRI	L	✓	-	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[71]
469	0x1D5		FCMMENDI	L	✓	-	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
470	0x1D6		FCMCOVFI	L	✓	-	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
471	0x1D7	WDT	WDT_REFUDF	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[72]
472	0x1D8	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
473	0x1D9	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
474	0x1DA	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
475	0x1DB	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
476	0x1DC	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
477	0x1DD	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
478	0x1DE	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
479	0x1DF	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
480	0x1E0	ADC	ADC_EOCA	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	IRQ[73]
481	0x1E1		ADC_EOCB	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
482	0x1E2		ADC_EOCC	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
483	0x1E3		ADC_CMP0	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
484	0x1E4		ADC_CMP1	P	✓	✓	IRQ[0]-[15] (INTC_INTSEL0-15)	↑
485	0x1E5	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
486	0x1E6	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
487	0x1E7	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
488	0x1E8	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
489	0x1E9	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
490	0x1EA	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
491	0x1EB	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
492	0x1EC	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
493	0x1ED	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
494	0x1EE	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
495	0x1EF	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
496	0x1F0	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
497	0x1F1	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
498	0x1F2	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
499	0x1F3	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
500	0x1F4	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
501	0x1F5	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
502	0x1F6	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
503	0x1F7	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
504	0x1F8	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
505	0x1F9	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
506	0x1FA	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
507	0x1FB	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
508	0x1FC	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
509	0x1FD	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-

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SN	Interrupt Event No.	Modules	Interrupt Name	Interrupt Type(1)	Interrupt Source	Trigger Source	NVIC Interrupt Request (IRQ) Number Mapping	
							Type A (INTC_INTSEL Write Event Number)(2)	Type B (Fixed)
510	0x1FE	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-
511	0x1FF	-	-	-	-	-	IRQ[0]-[15] (INTC_INTSEL0-15)	-

Note

1. "P" means pulse interruption, and "L" means level interruption. The interrupt flag bit must be cleared in the interrupt handler for level interrupts.
2. If the interrupt event is not configured, the number selected by the interrupt selection register has no effect.
3. AOS_STRG is generated by software setting the INTSFTTRG.STRG bit register.
4. "↑" means the IRQ number is the same as above.

11.3 Functional Description

11.3.1 Function Block Diagram

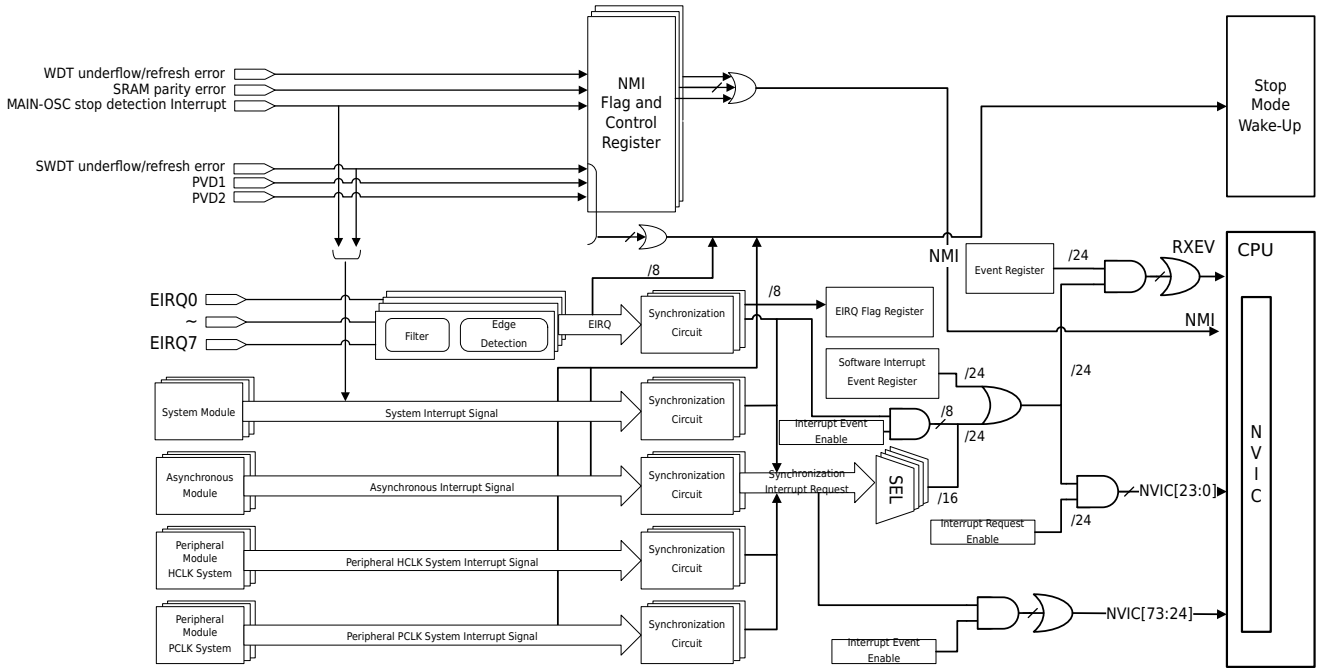

Figure 11-1 Interrupt System Block Diagram

11.3.2 Non-maskable Interrupt

The non-maskable interrupt events are as follows:

- NMI pin interrupt
- XTAL oscillation fault interrupt
- WDT underflow/refresh error interrupt
- SWDT underflow/refresh error interrupt
- Low voltage detection PVD1 interrupt

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- Low voltage detection PVD2 interrupt
- SRAM parity error interrupt

Non-maskable interrupts have the highest priority and can select multiple interrupt events. The status of each interrupt event can be queried through the interrupt flag register (INTC_NMIFR). Please make sure all the flag bits are "0" before the non-maskable interrupt processing exits. Non-maskable interrupts are disabled by default and can be configured via the ICG or control registers.

When you need to use non-maskable interrupts, please set them according to the following process:

1. Configure the corresponding functions for non-maskable interrupt events.
2. Write 1 to each bit of INTC_NMIFCR to clear the interrupt flag and prevent malfunction.
3. Set the interrupt enable register INTC_NMIER to enable the corresponding interrupt event.

The ICG configuration applies only to the external NMI pin. Enable the ICG configuration by setting the ICG3.NMIICGDIS bit. Set ICG3.NMITRG to select the NMI trigger edge; set ICG3.NMIFCLK to select the digital filter sampling clock; set ICG3.NMIFEN to enable the digital filter; set ICG3.NMIEN to enable the NMI pin interrupt. After the ICG is configured, register settings become invalid. For the register description of ICG3, refer to the "Initialization Configuration (ICG)" chapter.

Notice

Once the corresponding bit of INTC_NMIER is set to 1, it cannot be changed unless a reset occurs.

11.3.3 External Interruption

Equipped with 8 external interrupt events, the interrupt status can be queried through the interrupt flag register (INTC_EIFR). When using external interrupts, follow the procedure below:

1. Configure the corresponding external pin to the external interrupt function.
2. Write 1 to the respective bits of INTC_EIFCR to clear the interrupt flags and prevent false triggering.
3. Clear INTC_EIRQCRx.EFEN (x=0 to 7) bit to disable the digital filter.
4. Configure INTC_EIRQCRx.EIRQTRG bit to select the trigger edge or level; set the EISMPCLK bit to choose the digital filter sampling clock; then set the EFEN bit to enable the digital filter.

11.3.4 Interrupt Event Multiplexer

The interrupt controller includes a 512-to-1 interrupt event multiplexer for each NIVC interrupt request 0-15. By writing the interrupt event number into the corresponding interrupt event selection registers INTC_INTSEL0-15, any one of all interrupt events can be selected as the interrupt source for that interrupt request. For specific interrupt event numbers, refer to the "Interrupt Event List". When using NIVC interrupt requests 0-15, you may set the corresponding bit in the INTC_INTEN register to 0 to disable that interrupt event request. This prevents a single interrupt event from generating two interrupts simultaneously.

11.3.5 Software Interrupt

The software interrupt function can generate an interrupt request by directly writing to the software interrupt register INTC_SWIER. A total of 24 software interrupts are available, corresponding to NVIC interrupt request numbers 0-23. Their enablement is controlled by the interrupt enable register INTC_IER.

11.3.6 Event Input

NIVC interrupt requests numbered 0-23 can also be used as event inputs (RXEV) to wake up the core (WFE), with their enablement controlled by the event enable register INTC_EVTER.

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The functional block diagram of interrupt requests and event inputs is shown below:

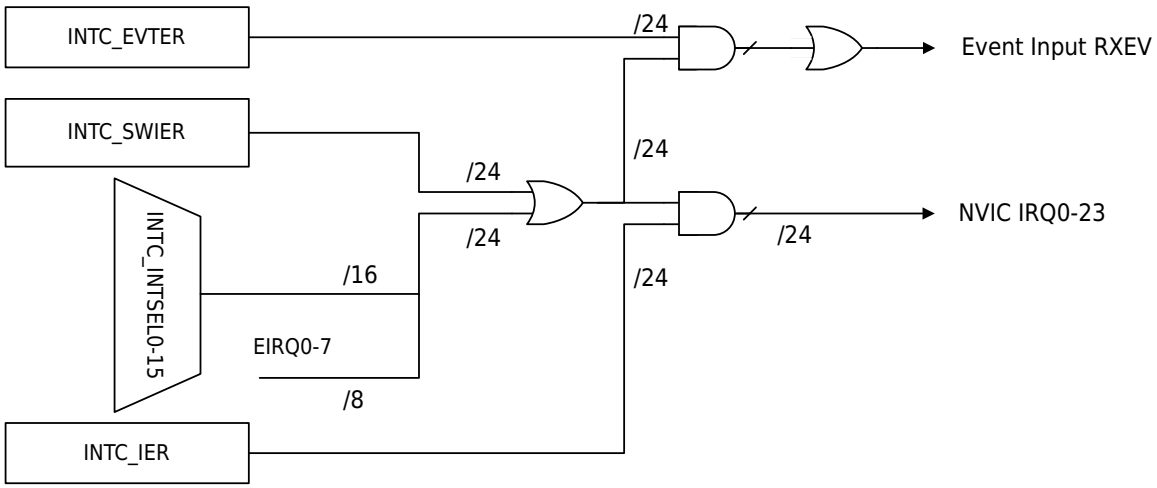

Figure 11-2 Interrupt Request/Event Input Selection

11.3.7 WFE Event Management

The interrupt controller can wake up the core (WFE) through interrupt requests and event inputs.

- Interrupt Request Wake-up Core

  Select an interrupt event, set INTC_INTSEL according to the selected interrupt request and enable the INTC_IER register (without enabling the interrupt request in NVIC). Set the INTC_EVTER register to disabled, and enable the SEVONPEND bit in the Cortex-M4 core control register SCR. Executing WFE puts the core into Sleep mode. When the selected interrupt event occurs, the core is awakened from sleep mode but does not enter the interrupt handler.

- Event Input Wake-up Core

  Select an interrupt event, set INTC_INTSEL according to the selected interrupt request and enable the INTC_EVTER register. The INTC_IER register is set to disabled. Executing WFE puts the core into sleep mode. When the selected interrupt event occurs, the core is woken up from sleep mode.

11.3.8 Noise Filter

In order to eliminate input noise, the NMI pin and external interrupt EIRQx (x=0-7) are each configured with both digital and analog filters.

The NMI pin digital filter is enabled by the INTC_NMICR.NFEN bit; the EIRQ digital filter is enabled by the INTC_EIRQCRx.EFEN bit. When the filter sampling clock samples three consecutive identical levels on the port, that level is considered valid and transmitted to the module's internal logic. Levels that are not identical for three consecutive samples are filtered out as external noise and are not transmitted internally. The NMI digital filter sampling period is set by the INTC_NMICR.SMPCLK bit; the EIRQ digital filter sampling period is set by the INTC_EIRQCRx.EISMPCLK bit.

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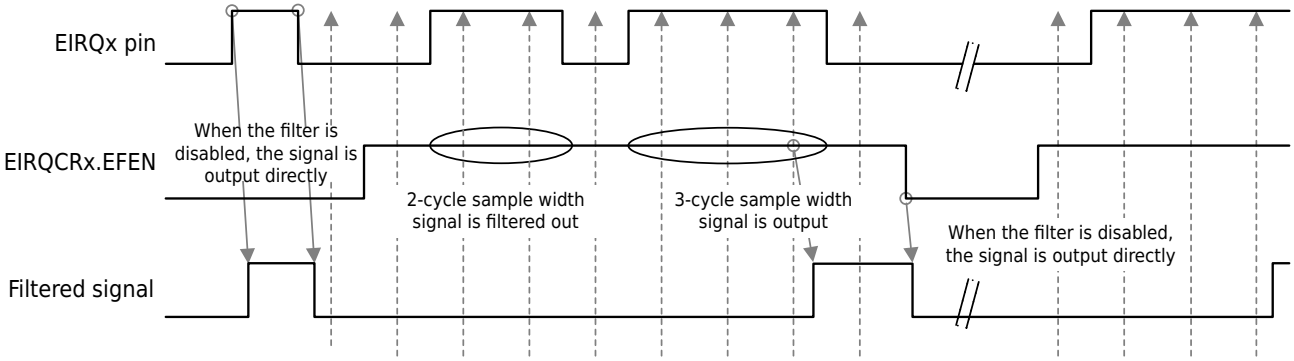

Figure 11-3 Digital Filter Operation Diagram

The NMI pin analog filter is enabled by the INTC_NMICR.NOCEN bit; the EIRQ analog filter is enabled by the INTC_EIRQCRx.NOCEN bit. After enabling, the NMI and EIRQ signals are filtered with the filter widths selected by the INTC_NMICR.NOCSEL and INTC_EIRQCRx.NOCSEL bits, respectively.

The two filters are independent of each other and can be enabled or disabled separately. When both are enabled, the signal first passes through the analog filter and then the digital filter before entering the internal circuit.

The digital filter must be turned off before entering the stop mode. The digital filter is enabled after returning from the stop mode. The analog filter can work in stop mode.

11.3.9 Low Power Mode Return

Sleep Mode Return

To wake up the CPU from Sleep mode using an interrupt request, configure the following:

- Select an interrupt event as the interrupt request.
  If using interrupt requests 0-23, configure the INTC_IER register.
- Enable the corresponding interrupt in the NVIC.
- If using a non-maskable interrupt, configure the INTC_NMIER register.

Stop Mode Return

To return from Stop mode via an interrupt request, configure the following:

- Select an interrupt event as the interrupt request.
  If using interrupt requests 0-23, configure the INTC_IER register.
- Enable the interrupt source via the INTC_WKEN register.
  If non-maskable interrupts are used, enable the interrupt events through the INTC_NMIER register. The non-maskable interrupts that can wake up the stop mode are: low voltage detection PVD1 interrupt, low voltage detection PVD2 interrupt, SWDT underflow/refresh error interrupt.
- Enable the corresponding interrupt request in the NVIC.

Non-maskable Interrupt and WFI Command

Before executing the WFI instruction, please confirm that all status bits of the non-maskable interrupt flag register INTC_NMIFR are 0.

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11.4 Register Description

11.4.1 Register List

Base Address: 0x40051000

Table 11-4 Interrupt Controller (INTC) Register Offset

Offset	Register	Description	Width
0x0000	INTC_NMICR	NMI Pin Interruption Control Register	32
0x0004	INTC_NMIER	Non-maskable Interrupt Enable Register	32
0x0008	INTC_NMIFR	Non-maskable Interrupt Flag Register	32
0x000C	INTC_NMIFCR	Non-maskable Interrupt Flag Clear Register	32
0x0010+0x4*x	INTC_EIRQCRx	External Interrupt Control Register x (x=0-7)	32
0x0054	INTC_EIFR	External Interrupt Flag Register	32
0x0058	INTC_EIFCR	External Interrupt Flag Clear Register	32
0x005C+0x4*x	INTC_INTSELx	Interrupt Event Select Register x (x=0-15)	32
0x025C+0x4*x	INTC_INTENx	Interrupt Event Enable Register x (x=0-15)	32
0x0050	INTC_WKEN	Stop Mode Wake-up Event Enable Register	32
0x029C	INTC_SWIER	Software Interrupt Register	32
0x02A0	INTC_EVTER	Event Enable Register	32
0x02A4	INTC_IER	Interrupt Request Enable Register	32
0x02A8	INTC_FPUIER	FPU Interrupt Enable Register	32

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11.4.2 NMI Pin Interrupt Control Register (INTC_NMICR)

Offset	Bit Position																													
0x0000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																NOCEN	Reserved	NOCSEL		Reserved				NFEN	Reserved	SMPCLK		Reserved			NMITRG
Access																	RW		RW						RW		RW					RW

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15	NOCEN	NMI Pin Analog Filter Enable ● 0b0: Disable digital filter function ● 0b1: Enable analog filter function The filter width is determined by NOCSEL.	RW
14	*Reserved*	-	-
13:12	NOCSEL	Analog Filter Width Selection ● 0b00: Filter width range 1 ● 0b01: Filter width range 2 ● 0b10: Filter width range 3 ● 0b11: Filter width range 4 For specific values for each range, please refer to the relevant descriptions in the "Electrical Characteristics - NMI Filter Characteristics" chapter of the Datasheet.	RW
11:8	*Reserved*	-	-
7	NFEN	NMI Pin Digital Filter Enable ● 0b0: Diable digital filter function ● 0b1: Enable digital filter function	RW
6	*Reserved*	-	-
5:4	SMPCLK	NMI Pin Digital Filter Sampling Cycle Selection ● 0b00: 1 ×PCLK3 period ● 0b01: 8 ×PCLK3 periods ● 0b10: 32 ×PCLK3 periods ● 0b11: 64 ×PCLK3 periods	RW
3:1	*Reserved*	-	-
0	NMITRG	NMI Pin Trigger Edge Selection ● 0b0: Falling edge ● 0b1: Rising edge	RW

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11.4.3 Non-maskable Interrupt Enable Register (INTC_NMIER)

Offset	Bit Position																													
0x0004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																				WDTEN	Reserved		RPARERREN	Reserved		XATLSTPEN	Reserved		PVD2EN	PVD1EN	SWDTEN	NMIEN
Access																					RW			RW			RW			RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:12	*Reserved*	-	-
11	WDTEN	WDT Underflow/Refresh Error Interrupt Selection ● 0b0: Disable interrupt as non-maskable interrupt source ● 0b1: Select the interrupt as a non-maskable interrupt source	RW
10:9	*Reserved*	-	-
8	RPARERREN	SRAM Parity Error Interrupt Selection ● 0b0: Disable interrupt as non-maskable interrupt source ● 0b1: Select the interrupt as a non-maskable interrupt source	RW
7:6	*Reserved*	-	-
5	XATLSTPEN	XTAL Oscillation Failure Interrupt Selection ● 0b0: Disable interrupt as non-maskable interrupt source ● 0b1: Select the interrupt as a non-maskable interrupt source	RW
4	*Reserved*	-	-
3	PVD2EN	PVD2 Interrupt Selection ● 0b0: Disable interrupt as non-maskable interrupt source ● 0b1: Select the interrupt as a non-maskable interrupt source	RW
2	PVD1EN	PVD1 Interrupt Selection ● 0b0: Disable interrupt as non-maskable interrupt source ● 0b1: Select the interrupt as a non-maskable interrupt source	RW
1	SWDTEN	SWDT Underflow/Refresh Error Interrupt Selection ● 0b0: Disable interrupt as non-maskable interrupt source ● 0b1: Select the interrupt as a non-maskable interrupt source	RW
0	NMIEN	NMI Pin Interrupt Selection ● 0b0: Disable interrupt as non-maskable interrupt source ● 0b1: Select the interrupt as a non-maskable interrupt source	RW

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11.4.4 Non-maskable Interrupt Flag Register (INTC_NMIFR)

Offset	Bit Position																													
0x0008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																				WDTF	Reserved		RPARERRF	Reserved		XTALSTPF	Reserved	PVD2F	PVD1F	SWDTF	NMIF
Access																					RO			RO			RO		RO	RO	RO	RO

Bit	Name	Functional Description	Access
31:12	*Reserved*	-	-
11	WDTF	WDT Underflow/Refresh Error Interrupt Flag ● 0b0: No WDT underflow/refresh error interrupt request occurred ● 0b1: WDT underflow/refresh error interrupt request occurred	RO
10:9	*Reserved*	-	-
8	RPARERRF	SRAM Parity Error Interrupt Flag ● 0b0: No SRAM parity error interrupt request occurred ● 0b1: SRAM parity error interrupt request occurred	RW
7:6	*Reserved*	-	-
5	XTALSTPF	XTAL Oscillation Fault Interrupt Flag ● 0b0: No XTAL oscillation failure interrupt request occurred ● 0b1: XTAL oscillation failure interrupt request occurred	RO
4	*Reserved*	-	-
3	PVD2F	PVD2 Interrupt Flag ● 0b0: No PVD2 interrupt request occurred ● 0b1: PVD2 interrupt request occurred	RO
2	PVD1F	PVD1 Interrupt Flag ● 0b0: No PVD1 interrupt request occurred ● 0b1: PVD1 interrupt request occurred	RO
1	SWDTF	SWDT Underflow/Refresh Error Interrupt Flag ● 0b0: No SWDT underflow/refresh request occurred ● 0b1: SWDT underflow/refresh request occurred	RO
0	NMIF	NMI Pin Interrupt Flag ● 0b0: No NMI pin interrupt request occurred ● 0b1: NMI pin interrupt request occurred	RO

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11.4.5 Non-maskable Interrupt Flag Clear Register (INTC_NMIFCR)

Offset	Bit Position																													
0x000C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																				WDTFCLR	Reserved		RPARERRFCLR	Reserved		XATLSTPFCLR	Reserved	PVD2FCLR	PVD1FCLR	SWDTFCLR	NMIFCLR
Access																					WO			WO			WO		WO	WO	WO	WO

Bit	Name	Functional Description	Access
31:12	*Reserved*	-	-
11	WDTFCLR	WDT Underflow/Refresh Error Interrupt Flag Clear Write 1 to clear the flag, write 0 has no effect; read always returns 0	WO
10:9	*Reserved*	-	-
8	RPARERRFCLR	SRAM Parity Error Interrupt Flag Clear Write 1 to clear the flag, write 0 has no effect; read always returns 0	RW
7:6	*Reserved*	-	-
5	XATLSTPFCLR	XTAL Oscillation Failure Interrupt Flag Clear Write 1 to clear the flag, write 0 has no effect; read always returns 0	WO
4	*Reserved*	-	-
3	PVD2FCLR	PVD2 Interrupt Flag Clear Write 1 to clear the flag, write 0 has no effect; read always returns 0	WO
2	PVD1FCLR	PVD1 Interrupt Flag Clear Write 1 to clear the flag, write 0 has no effect; read always returns 0	WO
1	SWDTFCLR	SWDT Underflow/Refresh Error Interrupt Flag Clear Write 1 to clear the flag, write 0 has no effect; read always returns 0	WO
0	NMIFCLR	NMI Pin Interrupt Flag Clear Write 1 to clear the flag, write 0 has no effect; read always returns 0	WO

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11.4.6 External Interrupt Control Register (INTC_EIRQCRx) (x=0-7)

Offset: 0x0010+0x4*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																NOCEN	Reserved	NOCSEL		Reserved				EFEN	Reserved	EISMPCLK		Reserved		EIRQTRG	
Access																	RW		RW						RW		RW				RW	

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15	NOCEN	EIRQ Analog Filter Enabled ● 0b0: Disable analog filter function ● 0b1: Enable analog filter function The filter width is determined by NOCSEL.	RW
14	*Reserved*	-	-
13:12	NOCSEL	Analog Filter Filtering Width Selection ● 0b00: Filtering width level 1 ● 0b01: Filtering width level 2 ● 0b10: Filtering width level 3 ● 0b11: Filtering width level 4 For the specific values for each range, please refer to the relevant description in the "Electrical Characteristics-EIRQ Filter Characteristics" section in the Datasheet.	RW
11:8	*Reserved*	-	-
7	EFEN	EIRQ Digital Filter Enabled ● 0b0: Disable digital filter function ● 0b1: Enable digital filter function	RW
6	*Reserved*	-	-
5:4	EISMPCLK	Digital Filter Sampling Period Selection ● 0b00: 1 × PCLK3 period ● 0b01: 8 × PCLK3 period ● 0b10: 32 × PCLK3 period ● 0b11: 64 × PCLK3 period	RW
3:2	*Reserved*	-	-
1:0	EIRQTRG	Trigger Selection ● 0b00: Falling edge ● 0b01: Rising edge ● 0b10: Double edge ● 0b11: Low level	RW

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11.4.7 External Interrupt Flag Register (INTC_EIFR)

Offset	Bit Position																													
0x0054	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								EIF							
Access																									RO							

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7:0	EIF	EIRQ Flag Bit Corresponding to EIF7-EIF0: ● 0b0: EIRQ event did not occur, or the EIFCLR bit was cleared by writing ● 0b1: The selected EIRQ event occurs	RO

11.4.8 External Interrupt Flag Clear Register (INTC_EIFCR)

Offset	Bit Position																													
0x0058	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								EIFCLR							
Access																									WO							

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7:0	EIFCLR	EIRQ Flag Clear Bit Corresponding to EIFCLR7-EIFCLR0, write 1 to clear the corresponding bit of the INTC_EIFR register, write 0 has no effect; read always returns 0.	WO

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11.4.9 Interrupt Event Select Register (INTC_INTSELx) (x=0-15)

Offset: 0x005C+0x4*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000001FF																															
Name	Reserved																							INTSEL								
Access																								RW								

Bit	Name	Functional Description	Access
31:9	*Reserved*	-	-
8:0	INTSEL	Interrupt Event Request Selection Select the interrupt event request corresponding to 0x000-0x1FE, see the Interrupt Event Table for details	RW

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11.4.10 Interrupt Event Enable Register (INTC_INTENx) (x=0-15)

Offset: 0x025C+0x4*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFFFFFFFF																															
Name	INTENy																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	INTENy (y=31-0)	Interrupt Event Enabled Corresponding interrupt event number z (z=x*32+y) ● 0b0: Interrupt event disabled ● 0b1: Interrupt event enabled **Note** ● The interrupt event set to "0" will not be received by the NVIC interrupt request numbered 15 and later. ● The bit corresponding to the sequence number of the unconfigured interrupt event is a read-only bit and is "1" when read out.	RW

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11.4.11 Stop Mode Wake-up Event Enable Register (INTC_WKEN)

Offset	Bit Position																													
0x0050	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved					RXWKEN	Reserved		TMR0CMPWKEN	Reserved			CMP2WKEN	PVD2WKEN	PVD1WKEN	SWDTWKEN	Reserved								EIRQWKEN							
Access						RW			RW				RW	RW	RW	RW									RW							

Bit	Name	Functional Description	Access
31:27	*Reserved*	-	-
26	RXWKEN	USART_1 RX Line Stop Mode Wake-up Enabled ● 0b0: Wake-up disabled ● 0b1: Wake-up enabled	RW
25:24	*Reserved*	-	-
23	TMR0CMPWKEN	TMR0_1_CMPA Stop Mode Wake-up Enabled ● 0b0: Wake-up disabled ● 0b1: Wake-up enabled	RW
22:20	*Reserved*	-	-
19	CMP2WKEN	CMP2 Stop Mode Wake-up Enabled ● 0b0: Wake-up disabled ● 0b1: Wake-up enabled	RW
18	PVD2WKEN	PVD2 Stop Mode Wake-up Enabled ● 0b0: Wake-up disabled ● 0b1: Wake-up enabled	RW
17	PVD1WKEN	PVD1 Stop Mode Wake-up Enabled ● 0b0: Wake-up disabled ● 0b1: Wake-up enabled	RW
16	SWDTWKEN	SWDT_REFUDF Stop Mode Wake-up Enabled ● 0b0: Wake-up disabled ● 0b1: Wake-up enabled	RW
15:8	*Reserved*	-	-
7:0	EIRQWKEN	EIRQ Stop Mode Wake-up Enabled Corresponding to EIRQWKEN7-EIRQWKEN0: ● 0b0: Wake-up disabled ● 0b1: Wake-up enabled	RW

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11.4.12 Software Interrupt Register (INTC_SWIER)

Offset	Bit Position																													
0x029C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																						SWIE									
Access																							RW									

Bit	Name	Functional Description	Access
31:24	*Reserved*	-	-
23:0	SWIE	Software Interrupt Corresponding to SWIE23-SWIE0: ● 0b0: No software interrupt occurred ● 0b1: Software interrupt occurred **Note** A software interrupt occurs after writing "1" from "0". To trigger it again, it must first be cleared by writing "0".	RW

11.4.13 Event Enable Register (INTC_EVTER)

Offset	Bit Position																													
0x02A0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																						EVTE									
Access																							RW									

Bit	Name	Functional Description	Access
31:24	*Reserved*	-	-
23:0	EVTE	Event Enabled Corresponding to EVTE23-EVTE0: ● 0b0: Event selection disabled ● 0b1: Event selection enabled	RW

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11.4.14 Interrupt Request Enable Register (INTC_IER)

Offset	Bit Position																													
0x02A4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00FFFFFF																															
Name	Reserved								IEN																							
Access									RW																							

Bit	Name	Functional Description	Access
31:24	*Reserved*	-	-
23:0	IEN	Interrupt Enable IEN23-IEN0 correspond to NVIC interrupt requests 23-0 respectively: ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled When disabled, the interrupt events corresponding to each interrupt request will not be received by NVIC.	RW

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11.4.15 FPU Interrupt Enable Register (INTC_FPUIER)

Offset	Bit Position																													
0x02A8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																										IDCIEN	IXCIEN	UFCIEN	OFCIEN	DZCIEN	IOCIEN
Access																											RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:6	*Reserved*	-	-
5	IDCIEN	FPU IDCI Interrupt Enable Bit ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW
4	IXCIEN	FPU IXCI Interrupt Enable Bit ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW
3	UFCIEN	FPU UFCI Interrupt Enable Bit ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW
2	OFCIEN	FPU OFCI Interrupt Enable Bit ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW
1	DZCIEN	FPU DZCI Interrupt Enable Bit ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW
0	IOCIEN	FPU IOCI Interrupt Enable Bit ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW

11.5 Precautions

For a description of ARM core interrupts, please refer to the "ARM Processor Cortex®-M4 Technical Reference Manual (ARM DDI 0439D)".

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12 Automatic Operation System (AOS)

12.1 Introduction

The Automatic Operation System (AOS) is used to achieve coordination between peripherals without the assistance of the CPU. It utilizes events generated by peripherals as AOS sources, such as timer comparison matches, timer counting overflow, various states of the sending and receiving data of the communication module (idle, receive data full, transmit data end, transmit data empty), ADC conversion end events, etc., to trigger actions of other peripherals. The triggered peripheral actions are referred to as AOS targets.

Users can select one or more AOS sources to trigger the same AOS target based on their needs.

12.2 Features

The AOS has multiple trigger sources, please refer to the "AOS Source Events". Unless specifically restricted, each AOS target can select one or more of these as trigger sources. When multiple trigger sources are required, two common trigger sources can be selected through the common trigger source selection registers 1 and 2, which are shared by all AOS targets. Thus, for an AOS target, up to 3 trigger sources can be selected, and any of these can trigger the AOS target action when an event occurs.

Triggering can be done by hardware from peripheral circuits or by software through register writes.

The peripherals and their quantities that can serve as AOS targets are as follows:

- 1 DCU trigger targets
- 5 DMA trigger targets
- 1 Timer0 trigger target
- 1 Timer4 trigger target
- 2 TimerA trigger targets
- 1 sets of 3 ADC trigger targets for ADC sequence triggering

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12.3 Functional Description

12.3.1 Function Block Diagram

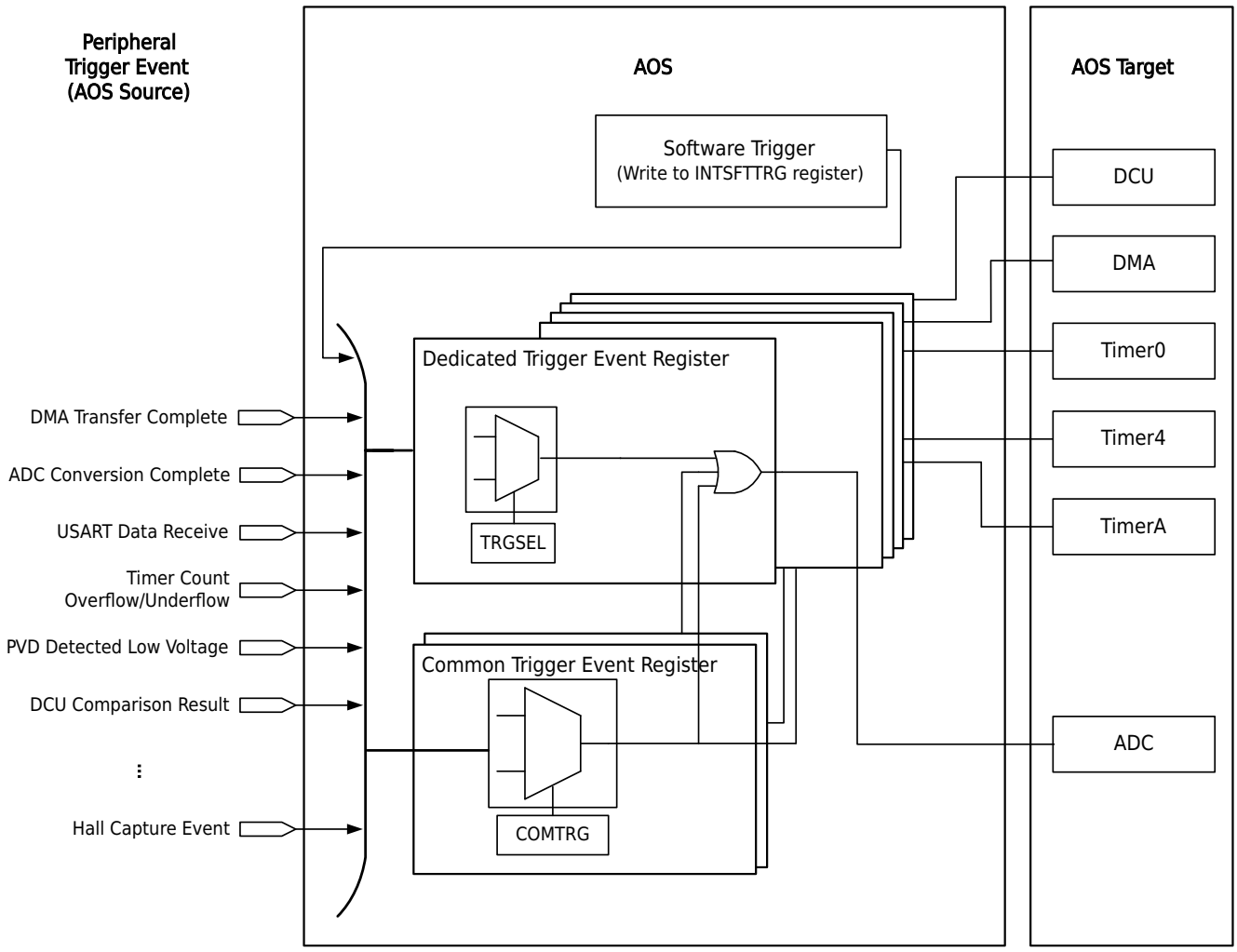

Figure 12-1 AOS Module Block Diagram

12.3.2 AOS Source Events and Targets

The AOS source event numbers are listed in the Interrupt Event List in the "Interrupt Controller (INTC) " chapter. Events marked with a "✓" in the "Trigger Source" column can be used as AOS sources. The AOS targets are listed in the table below.

Table 12-1 AOS Target List

Modules	SN	Action
DCU	0	Trigger addition/subtraction operation
DMA	1	Trigger channel 0 starting transmission
	2	Trigger channel 1 starting transmission
	3	Trigger channel 2 starting transmission
	4	Trigger channel 3 starting transmission
	5	Trigger event trigger channel reset
Timer0	6	Trigger counter start/stop/clear/capture

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Modules	SN	Action
Timer4	7	Trigger counter start
TimerA	8	Trigger Unit 1/3/5 counter start/stop/clear/increment/decrement
		Trigger Unit 2/4 counter input capture
	9	Trigger Unit 2/4 counter start/stop/clear/increment/decrement
		Trigger Unit 1/3/5 counter input capture
ADC	10	Trigger sequence A/B/C analog-to-digital conversion start
	11	Trigger sequence A/B/C analog-to-digital conversion start
	12	Trigger sequence A/B/C analog-to-digital conversion start

12.3.3 Dedicated Trigger Source

For peripheral circuit modules with AOS targets, each AOS target is equipped with a dedicated peripheral trigger source selection register. When the event number corresponding to an AOS source is written to this register, the AOS target selects this AOS source as its trigger source. When an AOS source event occurs, the event is passed to the AOS target through the AOS, and the peripheral circuit of the AOS target starts its action based on its settings.

12.3.4 Common Trigger Source

In addition to the dedicated peripheral trigger source selection registers for each AOS target, the AOS also configures two common trigger source selection registers (AOS_COMTRGSEL1, AOS_COMTRGSEL2). These are used to achieve the function of triggering one or more AOS targets with the same trigger source, or triggering the same AOS target with multiple AOS trigger sources. To use them, first set the common trigger source enable bit to active in the dedicated peripheral trigger source selection register for the AOS target, and then write the event number corresponding to the AOS source in the common trigger source selection register. When an AOS source event occurs, the event is passed to the AOS target through the common trigger source of the AOS, and the peripheral circuit of the AOS target starts its action based on its settings. When both dedicated and common trigger sources are set, up to 3 AOS sources can trigger the same AOS target simultaneously. Any of the 3 AOS sources can trigger the AOS target when an event occurs.

All AOS targets share these two common trigger sources. Therefore, when other AOS targets are not using the event selected by the common trigger source selection register, the common trigger source enable bit should be set to inactive in its dedicated peripheral trigger source selection register to prevent erroneous triggering.

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12.4 Register Description

12.4.1 Register List

Base address: 0x40010800

Table 12-2 Automatic Operation System (AOS) Register Offset

Offset	Register	Description	Width
0x00	INTSFTTRG	Software Trigger Event Register	32
0x04+0x04*x	DMA_TRGSELx	DMA Transfer Start Trigger Source Selection Register (x=0-3)	32
0x14	DMA_RC_TRGSEL	DMA Re-config Trigger Source Selection Register	32
0x18	DCU_TRGSEL	DCU Trigger Source Selection Register	32
0x1C	TMR0_TRGSEL	Timer0 Hardware Trigger Event Selection Register	32
0x20+0x04*x	TMRA_TRGSELx	TimerA Hardware Trigger Event Selection Register (x=0-1)	32
0x28	TMR4_TRGSEL	Timer4 Hardware Trigger Event Selection Register	32
0x2C+0x04*x	ADC_TRGSELx	ADC Conversion Start On-Chip Trigger Source Selection Register (x=0-2)	32
0x38	AOS_COMTRGSEL1	Common Trigger Source Selection Register 1	32
0x3C	AOS_COMTRGSEL2	Common Trigger Source Selection Register 2	32

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12.4.2 Software Trigger Event Register (INTSFTTRG)

Writing 1 to this register generates a trigger event each time.

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																															STRG
Access																																WO

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-
0	STRG	Software Trigger Writing 1 generates a software trigger event; writing 0 has no effect	WO

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12.4.3 DMA Transfer Start Trigger Source Selection Register (DMA_TRGSELx) (x=0-3)

After enabling DMA, please use this register to select the trigger event source. When the peripheral event corresponding to the assigned number occurs, the DMA will be triggered by this event to initiate and carry out the data transfer.

Each data transfer channel corresponds to one register.

Offset: 0x04+0x04*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000001FF																															
Name	COMEN	Reserved																						TRGSEL								
Access	RW																							RW								

Bit	Name	Functional Description	Access
31	COMEN[1]	Common Trigger Enabled ● 0b0: Disable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL2 ● 0b1: Enable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL2	RW
30	COMEN[0]	Common Trigger Enabled ● 0b0: Disable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL1 ● 0b1: Enable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL1	RW
29:9	*Reserved*	-	-
8:0	TRGSEL	Trigger Source Selection Write the number of the peripheral circuit event to be selected	RW

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12.4.4 DMA Channel Reset Trigger Source Selection Register (DMA_RC_TRGSEL)

After enabling DMA, use this register to select the trigger event source. When the peripheral event corresponding to the number occurs, DMA will be triggered to reset the channel.

Offset	Bit Position																													
0x14	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000001FF																															
Name	COMEN	Reserved																						TRGSEL								
Access	RW																							RW								

Bit	Name	Functional Description	Access
31	COMEN[1]	Common Trigger Enabled ● 0b0: Disable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL2 ● 0b1: Enable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL2	RW
30	COMEN[0]	Common Trigger Enabled ● 0b0: Disable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL1 ● 0b1: Enable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL1	RW
29:9	*Reserved*	-	-
8:0	TRGSEL	Trigger Source Selection Write the number of the peripheral circuit event to be selected	RW

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12.4.5 DCU Trigger Source Selection Register (DCU_TRGSEL)

After selecting the hardware trigger start mode in the DCU, use this register to select the trigger event source. When the peripheral event corresponding to the number occurs, the DCU will be triggered to start and perform calculations by this event.

Offset	Bit Position																													
0x18	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000001FF																															
Name	COMEN	Reserved																						TRGSEL								
Access	RW																							RW								

Bit	Name	Functional Description	Access
31	COMEN[1]	Common Trigger Enabled ● 0b0: Disable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL2 ● 0b1: Enable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL2	RW
30	COMEN[0]	Common Trigger Enabled ● 0b0: Disable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL1 ● 0b1: Enable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL1	RW
29:9	*Reserved*	-	-
8:0	TRGSEL	Trigger Source Selection Write the number of the peripheral circuit event to be selected	RW

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12.4.6 Timer0 Hardware Trigger Event Selection Register (TMR0_TRGSEL)

After selecting hardware trigger in Timer0, use this register to select the trigger event source. When the peripheral event corresponding to the number occurs, Timer0 will be triggered to act (including start/stop/clear/input capture) by this event.

All Timer0 units and their channels share this register.

Offset	Bit Position																													
0x1C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000001FF																															
Name	COMEN	Reserved																						TRGSEL								
Access	RW																							RW								

Bit	Name	Functional Description	Access
31	COMEN[1]	Common Trigger Enabled ● 0b0: Disable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL2 ● 0b1: Enable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL2	RW
30	COMEN[0]	Common Trigger Enabled ● 0b0: Disable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL1 ● 0b1: Enable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL1	RW
29:9	*Reserved*	-	-
8:0	TRGSEL	Trigger Source Selection Write the number of the peripheral circuit event to be selected	RW

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12.4.7 TimerA Hardware Trigger Event Selection Register (TMRA_TRGSELx) (x=0-1)

After selecting internal hardware trigger in TimerA, use this register to select the trigger event source. When the peripheral event corresponding to the number occurs, TimerA will be triggered to act (including start/stop/clear/input capture) by this event.

All TimerA units share these 2 registers.

Offset: 0x20+0x04*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000001FF																															
Name	COMEN	Reserved																						TRGSEL								
Access	RW																							RW								

Bit	Name	Functional Description	Access
31	COMEN[1]	Common Trigger Enabled ● 0b0: Disable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL2 ● 0b1: Enable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL2	RW
30	COMEN[0]	Common Trigger Enabled ● 0b0: Disable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL1 ● 0b1: Enable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL1	RW
29:9	*Reserved*	-	-
8:0	TRGSEL	Trigger Source Selection Write the number of the peripheral circuit event to be selected	RW

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12.4.8 Timer4 Hardware Trigger Event Selection Register (TMR4_TRGSEL)

After selecting internal trigger hardware synchronization in Timer4, use this register to select the trigger event source. When the peripheral circuit event corresponding to the number occurs, Timer4 will be triggered for hardware synchronization by this event.

Offset	Bit Position																													
0x28	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000001FF																															
Name	COMEN	Reserved																										TRGSEL				
Access	RW																											RW				

Bit	Name	Functional Description	Access
31	COMEN[1]	Common Trigger Enabled ● 0b0: Disable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL2 ● 0b1: Enable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL2	RW
30	COMEN[0]	Common Trigger Enabled ● 0b0: Disable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL1 ● 0b1: Enable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL1	RW
29:9	*Reserved*	-	-
8:0	TRGSEL	Trigger Source Selection Write the number of the peripheral circuit event to be selected	RW

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12.4.9 ADC Conversion Start On-Chip Trigger Source Selection Register (ADC_TRGSELx) (x=0-2)

After selecting the on-chip trigger mode in ADC, use this register to select the trigger event source. When the peripheral event corresponding to the number occurs, ADC will be triggered to start ADC conversion by this event.

Sequence A/B/C of ADC share these 3 registers.

Offset: 0x2C+0x04*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000001FF																															
Name	COMEN	Reserved																						TRGSEL								
Access	RW																							RW								

Bit	Name	Functional Description	Access
31	COMEN[1]	Common Trigger Enabled ● 0b0: Disable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL2 ● 0b1: Enable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL2	RW
30	COMEN[0]	Common Trigger Enabled ● 0b0: Disable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL1 ● 0b1: Enable triggering of this AOS target by the common trigger event of AOS_COMTRGSEL1	RW
29:9	*Reserved*	-	-
8:0	TRGSEL	Trigger Source Selection Write the number of the peripheral circuit event to be selected	RW

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12.4.10 Common Trigger Source Selection Register (AOS_COMTRGSELx) (x=1-2)

Write the trigger event number to AOS_COMTRGSEL1/2. When the peripheral circuit event corresponding to the number occurs, if the COMEN bit in the dedicated trigger source selection register of one or more AOS targets is 1, the peripheral event corresponding to the number will trigger the start of this one or more AOS targets.

Offset: 0x38 (AOS_COMTRGSEL1), 0x3C (AOS_COMTRGSEL2)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000001FF																															
Name	Reserved																							COMTRG								
Access																								RW								

Bit	Name	Functional Description	Access
31:9	*Reserved*	-	-
8:0	COMTRG	Trigger Source Selection Write the number of the peripheral circuit event to be selected	RW

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13 DMA Controller (DMA)

13.1 Introduction

DMA is used to transfer data between memory and peripheral function modules, enabling data exchange between memories, between memory and peripheral function modules, and between peripheral function modules without CPU involvement.

13.2 Features

- The DMA bus is independent of the CPU bus and transmits data according to the AMBA AHB-Lite bus protocol
- With 1 DMA control units, a total of 4 independent channels, which can independently operate different DMA transfer functions
- The start source of each channel is configured through an independent trigger source selection register
- 1 block per request
- The data block is a minimum of one data and can be up to 1024 data
- The width of each data item can be configured as 8-bit, 16-bit, or 32-bit
- It can be configured for 1-65535 transfers or infinite transfers
- The source address and destination address can be independently configured as fixed, incrementing, decrementing, repeated jump, or specified offset jump
- 3 types of interrupts can be generated: block transfer completed interrupt, transfer completed interrupt, and transfer error interrupt. Each interrupt can be configured to be masked or unmasked. Among them, block transfer completed and transfer completed can be used as event outputs, serving as trigger sources for other peripheral modules
- Support chain transfer function, enabling the transfer of multiple data blocks in a single request
- Support channel reset triggered by external events
- Support software-triggered start of transfer and software-triggered channel reset
- When not in use, it can be set to stop state to reduce power consumption

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13.3 Functional Description

13.3.1 DMA Block Diagram

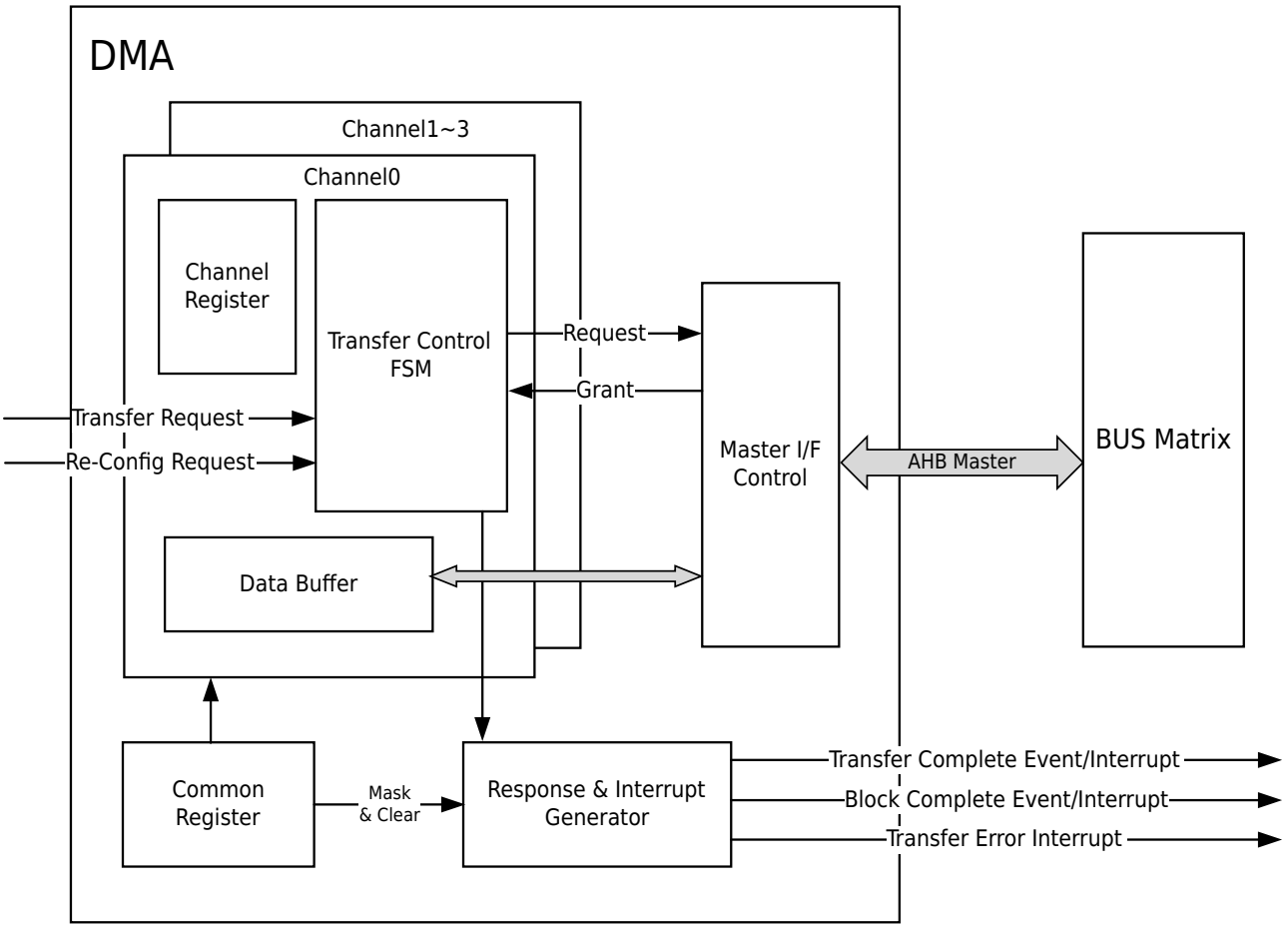

Figure 13-1 DMA Architecture Diagram

13.3.2 Enabling the DMA Controller

To use DMA, you need to first write 0 to the CMU_FCG.DMA bit to allow DMA clock supply, and then write 1 to the DMA_EN.EN bit. At the same time, DMA requires peripheral circuits to initiate transfers, so the CMU_FCG.AOS peripheral circuit trigger function bit also needs to be written to 0.

When DMA is not in use or the chip needs to enter STOP mode, please set DMA_EN.EN to 0 and write to CMU_FCG to turn off the DMA clock. Before setting EN to 0, please confirm that DMA_CHSTAT.DMAACT is 0 to ensure that DMA has completed all transfers.

13.3.3 Channel Selection and Channel Priority

The DMA control unit contains 4 channels, and each channel can independently configure transfer functions.

The channel priority order is: Channel 0 > Channel 1 >... > Channel 3.

When multiple channels in a DMA unit request transfer, they will be executed in priority order. But the channel that is already in transit will not be interrupted, the high priority channel will not start until the current channel transmission is complete.

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13.3.4 Start DMA

DMA is started by requests generated by peripheral circuits, which are configured through the trigger source selection register (DMA_TRGSELx, where x=0-3) for each channel independently. DMA can be started by writing to the DMA_SWREQ.SWREQ register for software-triggered transfer. When a peripheral circuit generates a start request or software writes to a register to generate a start request, and DMA transfer enable is active (DMA_EN.EN=1), and the transfer channel is in the permitted state (DMA_CHEN.CHEN[x]=1), channel x transfer starts.

Before use, you need to set the peripheral circuit trigger function and DMA function enable bits in CMU_FCG register to active.

13.3.5 Data Block

The amount of data transferred each time DMA is started is expressed in blocks. The size of the block is set by register DMA_DTCTLx.BLKSIZE, and the maximum size that can be set is 1024 data. The data width of each is determined by DMA_CHCTLx.HSIZE and can be 8-bit, 16-bit, or 32-bit.

13.3.6 Transfer Address Control

The source address and destination address of the transfer can be set to fixed, incrementing, decrementing, repeated jump, or NonSequence jump through registers.

- **Fixed:** The source address and destination address will be fixed during the transmission process.
- **Incrementing and Decrementing:** The source address and destination address increase or decrease by the value of HSIZE after each data item transfer. For example, when HSIZE is 8-bit, the address increases/decreases by 1 each time; for 16-bit, it increases/decreases by 2; for 32-bit, it increases/decreases by 4.
- **Repeating Jump:** After transferring a specified number of data items, the source and destination addresses return to their initial values. The amount of data that needs to be transferred before the address repeats the jump, that is, the size of the repeated area is set by the size of the register DMA_RPT.
- **NonSequence Jump:** After transferring a specified number of data items, the source and destination addresses skip a specified offset. The offset for address jump and the amount of data to be transferred before jump, i.e., the size of the NonSequence zone, are set by the DMA_SNSEQCTL/ DMA_DNSEQCTL registers. When the conditions for address repeated jump and NonSequence jump are met simultaneously, address repeated jump is executed.

13.3.7 Transfer Count

The total number of data blocks transferred by DMA is set by the DMA_DTCTLx.CNT bit. The maximum number of transmissions can be set to 65535. Each time a data block is transferred, the register value decrements by 1. When the register value becomes 0, it indicates that all data transfer for the channel is completed, and the channel transfer permission bit (DMA_CHEN.CHEN[x]) is automatically cleared, generating a transfer completed interrupt. If DMA_DTCTLx.CNT is set to 0 at the beginning of the transfer, it means unlimited transmission, and each start requests to transmit a data block, but the channel transmission permission bit is not cleared, and the transmission completion interrupt will not be generated.

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Note

After CHEN[x] is automatically cleared, to restart the channel, you need to reconfigure the channel configuration register and then write 1 to CHEN[x] to enable the channel. Otherwise, the subsequent transfer will start from the state at the end of the last transfer, i.e., the source/destination address will be the next address corresponding to the last transfer, and CNT will be 0 for unlimited transfer.

13.3.8 Chain Transfer

DMA controller has the function of chain transfer. The chain transfer needs to configure the following 8 registers, a total of 8 words, called a descriptor which contains the source address, destination address, data control information, address control information, chain pointer and transmission control information of the chain transfer.

- DMA_SARx
- DMA_DARx
- DMA_DTCTLx
- DMA_RPTx
- DMA_SNSEQCTLx
- DMA_DNSEQCTLx
- DMA_LLPx
- DMA_CHCTLx

Where LLP is called a Linked-List Pointer where the value represents the next descriptor's first address in the memory. When using chained transfer, first write the register DMA_CHCTLx.LLPEN to enable chained transfer, and write the descriptor information of the first transfer into the corresponding register. Then initialize the descriptors for subsequent transfers sequentially in memory. To end chain transfer, set DMA_CHCTLx.LLPEN to inactive in the last descriptor, and the DMA controller will end chain transfer after transfer completion.

When the last transfer of a descriptor completes, the next descriptor specified by LLP is loaded into the channel configuration register. Wait for the next transfer request input to start the first transfer of the new descriptor. Or according to register DMA_CHCTLx.LLPRUN settings, starting the first transfer directly after loading the new descriptor.

- When DMA_CHCTLx.LLPRUN=0, after the last block transfer of the current descriptor, the new channel descriptor is loaded into the channel register. BTC and TC interrupts are generated as usual, and then the DMA waits for the next transfer request to start transferring the newly loaded descriptor.
- When DMA_CHCTLx.LLPRUN=1, the transfer of the new descriptor starts immediately after loading, and neither BTC nor TC interrupt is generated for the last block transfer of the old descriptor.

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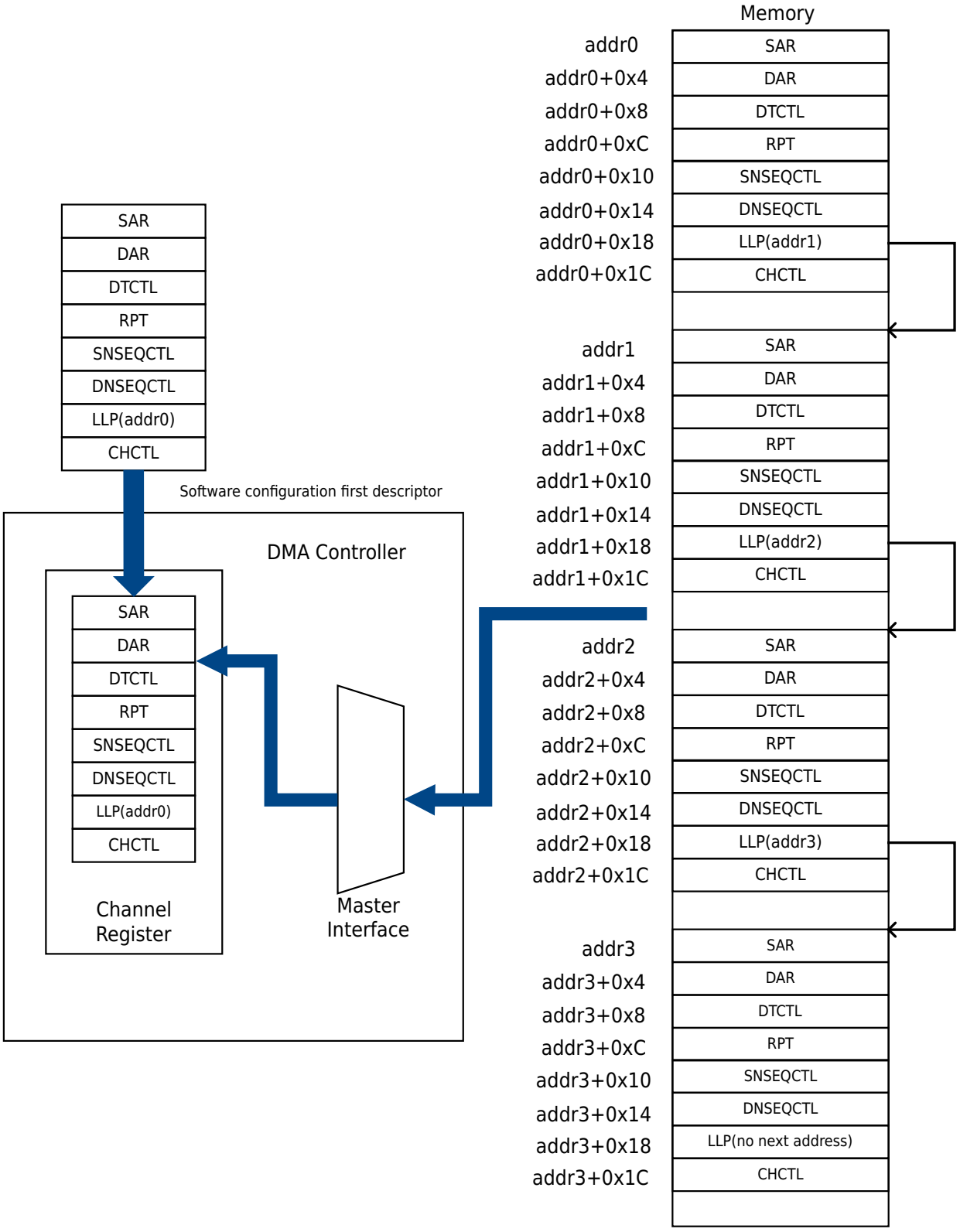

Figure 13-2 Chain Transmission Diagram

13.3.9 NonSequence Address Transfer

Using NonSequence address transfer can realize source address and destination address to jump according to a certain offset after a certain amount of data is transmitted. Taking source address NonSequence as an example: First, set DMA_CHCTLx.SNSEQEN to 1 to enable NonSequence address transfer. The jump direction is set forward or backward according to DMA_CHCTLx.SINC, and then configure DMA_SNSEQCTLx to set the specific jump mode. The control of the destination address is

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similar to that of the source address, with corresponding control registers being DMA_CHCTLx.DNSEQEN, DMA_CHCTLx.DINC, and DMA_DNSEQCTLx. The transfer process proceeds as shown in the following diagram.

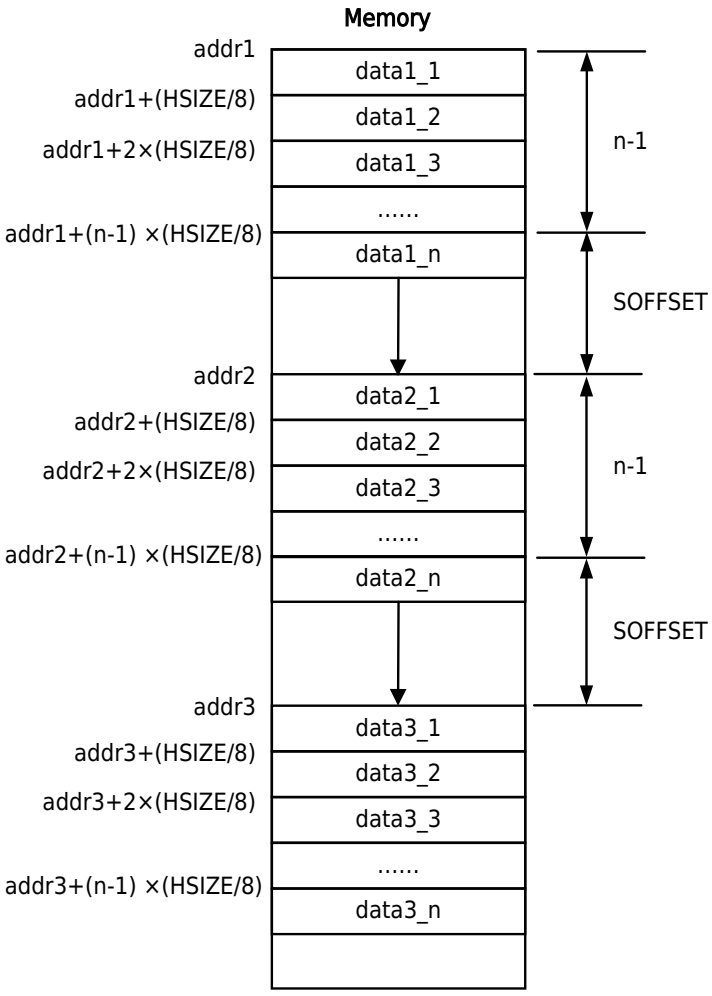

Figure 13-3 Schematic Diagram of NonSequence Address Transfer (Taking source address as an example)

n=SNSCNT

addr2=addr1+(n-1) ×(HSIZE/8) +SOFFSET×(HSIZE/8)

addr3=addr2+(n-1) ×(HSIZE/8) +SOFFSET×(HSIZE/8)

Where HSIZE is the data width (bit), which can be 8 bits (byte), 16 bits (half-word), or 32 bits (word).

13.3.10 Channel Reset

The channel reset function refers to modifying the internal status register of the channel through the event request of the peripheral circuit, and reconfiguring the next data transmission mode. Set register DMA_RCFGCTL.RCFGEN to 1 to allow channel reset. Select the reset request source through the DMA_RC_TRGSEL register or trigger channel reset through software by writing to the DMA_SWREQ.SWRCFGREQ register. When the selected reset request source input or software writing to the register generates a reset request, the channel selected by DMA_RCFGCTL.RCFGCHS is updated according to the specified mode. The reset request only updates the internal state and does not start actual data transfer.

There are 3 ways to reset channels: linked list pointer, NonSequence, and repeated.

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- When the linked list pointer reset is selected, the descriptor and internal state of the channel are all updated to the new descriptor pointed to by the linked list pointer LLP. Subsequent transfer requests are transferred according to the new descriptor.
- When selecting NonSequence or repeated reset, the channel internal state is updated as described in the following table.

Table 13-1 Channel Reset Description

Reset Modes (DMA_RCFGCTL)			Channel internal state		
CNTMD	SARMD	DARMD	Remaining Transfers Counter	Source address of next transmission	Destination address of next transmission
0x0	Arbitrary	Arbitrary	Remains unchanged	Updated based on SARMD	Updated based on DARMD
0x1	0x0	Arbitrary	Remains unchanged	Remains unchanged	Updated based on DARMD
	0x1		Updated to the value after the next NonSequence jump in the source address in normal state	Updated to the start address of the next source address NonSequence transfer region	
	0x2, 0x3		Updated to the value after the next repeated jump in the source address in normal state	Updated to the initial setting in the DMA_SARx register	
0x2, 0x3	Arbitrary	0x0	Remains unchanged	Updated based on SARMD	Remains unchanged
		0x1	Updated to the value after the next NonSequence jump in the destination address in normal state		Updated to the start address of the next destination address NonSequence region
		0x2, 0x3	Updated to the value after the next repeated jump in the destination address in normal state		Updated to the initial setting in the DMA_DARx register

Note

When the reset function is enabled, the channel uses DMA_RPTBx and DMA_SNSEQCTLBx, DMA_DNSEQCTLBx to control repeated jump and NonSequence jump of transfer addresses. Register DMA_RPTx and DMA_SNSEQCTLx, DMA_DNSEQCTLx are inactive.

In the DMA action shown in the following diagram, each transfer request starts the transfer of one data block. After the first reset request, the controller skips data blocks blk1_3 and blk1_4, and the transfer address is updated to the starting address of the next NonSequence zone, i.e., addr2. After the second reset request occurs, the remaining number of transfers is updated to 0, that is, all data transfers are completed, the channel permission bit is automatically cleared to 0, and a transfer completion interrupt and event are generated.

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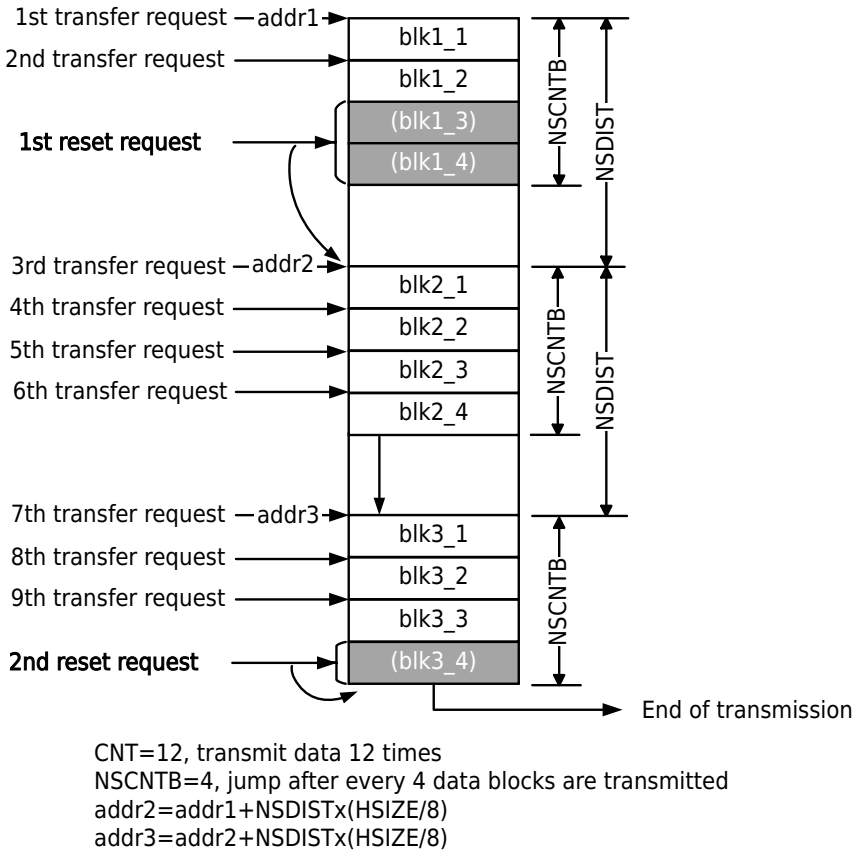

CNT=12, transmit data 12 times
NSCNTB=4, jump after every 4 data blocks are transmitted
addr2=addr1+NSDISTx(HSIZE/8)
addr3=addr2+NSDISTx(HSIZE/8)

Figure 13-4 Schematic Diagram of NonSequence Reset

13.3.11 Early Termination of Transfer

During transfer, the DMA_CHEN.CHENx bit remains active. For non-chain transfers, the transfer count set in register DMA_DTCTLx completes automatically and sets the bit to inactive. For chain transfers, the transfer count of the last chain transfer completes automatically and sets the bit to inactive. During transfer, if software writes 1 to DMA_CHENCLR.CHENCLRx, DMA will terminate the transfer after completing the current data read and write, and the DMA_CHEN.CHENx bit is cleared.

Notice

When software writes 1 to the CHENCLRx bit to terminate the transfer early, DMA does not save the transfer state at the time of termination. Without resetting the channel configuration register (descriptor) state and setting CHENx to 1 to re-enable the channel, DMA will retransmit the terminated data block instead of resuming from the breakpoint after a transfer request input.

13.3.12 Interrupt

The DMA controller can generate the following three types of interrupts:

- **Data Block Complete Interrupt DMA_BTCx:** generated after completing a data block transfer.
- **Transmission Complete Interrupt DMA_TCx:** generated after completing the transfer count set by DMA_DTCTLx.CNT.
- **Transmission Error Interrupt DMA_ERR:** when the start request overflows (that is, the channel triggers the start request again when the last request of the channel has not been responded), or when a bus error occurs during the transmission (such as accessing an illegal address or a protected address) an interrupt is generated, where in a bus error terminates the transfer immediately.

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Except for the transfer request overflow error, all other interrupts can be enabled or disabled through the DMA_CHCTLx.IE register. Additionally, all interrupts have independent MASK registers to mask the interrupts.

The above-mentioned DMA_BTCx and DMA_TCx interrupts can also be used as event signal outputs and can be used as trigger sources for other peripheral circuits. The event output is controlled by the MASK register but not by the DMA_CHCTLx.IE bit. DMA_BTCx, DMA_TCx, and DMA_ERR events will set the corresponding status bits in the register, regardless of the DMA_CHCTLx.IE or MASK register settings.

13.4 Operation Example

13.4.1 Memory-to-Memory Transfer

Target

Transfer 12 data items from RAM address 0x20000000 to 0x20001000, with a data width of 32-bit.

Register Setting

1. Enable the DMA controller by writing 1 to DMA_EN.EN.
2. Select a channel, for example channel 0, and configure the channel registers to achieve:
   a. Write DMA_SAR0 to configure the source address as SRAM region 0x20000000.
   b. Write DMA_DAR0 to configure the destination address as SRAM region 0x20001000.
   c. Write the DMA_DTCTL0 configuration data block size is 4, the number of transfers is 3, after each transfer one data block to produce block transfer complete interrupt, after 3 transfers complete one transfer complete interrupt
   d. Write DMA_RPT register configures the repeating area of the source address to be 6, that is, the original source address is reloaded after 6 addresses have been transmitted.
   e. Configure the channel control registers DMA_CHCTL0 to achieve:
      1) The source address and destination address chained transfer is disabled.
      2) The source address repeat enabled, destination address increment.
      3) The data width is 32-bit.
      4) Interrupt enable active.
   f. Configure the trigger source controller DMA_TRGSEL0 to select software trigger as the start request for DMA channel 0.
   g. Write 1 to the channel enable bit DMA_CHEN.CHEN0 to enable channel 0.
3. Write to the peripheral event software trigger register INTSFTTRG.STRG to 1 to send the first software start request, and DMA starts transferring data.

Transfer Process

Since the size of the data block is 4, the first transmission begins when INTSFTTRG.STRG is 1. When a data block transfer is completed, the transfer count DMA_MONDTCTL0.CNT is decremented by 1, and produces a block transfer completion interrupt, the software can continue to write INTSFTTRG.STRG in the interrupt subroutine to start the second transmission. During the second transmission, due to the source address repeat zone size of 6, after transferring 2 addresses, the source address will reload the initial address 0x20000000, and continue to transfer the remaining 2 addresses. After the second transmission is completed, the number of transfers DMA_MONDTCTL0.CNT is reduced by 1, and a block transfer completion interrupt is generated, and the software can continue to write INTSFTTRG.STRG in the interrupt subroutine to start the third transfer. After the third transmission is completed, the number of transfers DMA_MONDTCTL0.CNT is reduced to 0, that is, this transmission is all completed, DMA

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generates a block transfer completion interrupt and a transfer completion interrupt, and the channel enable bit DMA_CHEN.CHEN0 will be automatically cleared.

Figure 13-5 Application Example 1: Memory-to-Memory Transfer

13.4.2 Memory-to-Peripheral Transfer

Target

Transfer 10 data items of 16-bit width from RAM address 0x20000000 to the transmit buffer register of a communication module. The communication module generates a transfer request after sending each data item. After the last data item is sent, DMA generates a transfer completed interrupt.

Register Setting

1. Enable the DMA controller by writing 1 to DMA_EN.EN.
2. Configure DMA_INTMSK1 to mask the block transfer completed interrupt and enable the transfer completed interrupt.
3. Select a channel, for example channel 0, and configure the channel registers to achieve:
   a. Write DMA_SAR0 to configure the source address as SRAM region 0x20000000.
   b. Write DMA_DAR0 to configure destination address to register address of peripheral circuit 0x40000000.
   c. Write DMA_DTCTL0 configuration data block size is 1, number of transfers is 10, each transfer request is delivered once, one data at a time.
   d. Configure the channel control registers DMA_CHCTL0 to achieve:
      1) The source address and destination address chained transfer is disabled.
      2) The source address increment, destination address fixed.
      3) The source address and destination address data width is 16-bit.
      4) Interrupt enable active.
   e. Configure the trigger source controller DMA_TRGSEL0 to select the transmit buffer empty status of the communication module as the start request for DMA channel 0.
   f. Write 1 to the channel enable bit DMA_CHEN.CHEN0 to enable channel 0.

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Transfer Process

After the channel is enabled, DMA waits for the transmission request from the communication module. After the transmission request is generated, the DMA transmits the data in the RAM to the transmission buffer register of the communication module and waits for the second transmission request from the communication module. Because the block transfer completion interrupt is masked, the DMA does not generate interrupt request at this time. When all 10 data transfers are completed, DMA generates a transfer completion interrupt, and the channel enable bit DMA_CHEN.CHEN0 will be automatically cleared.

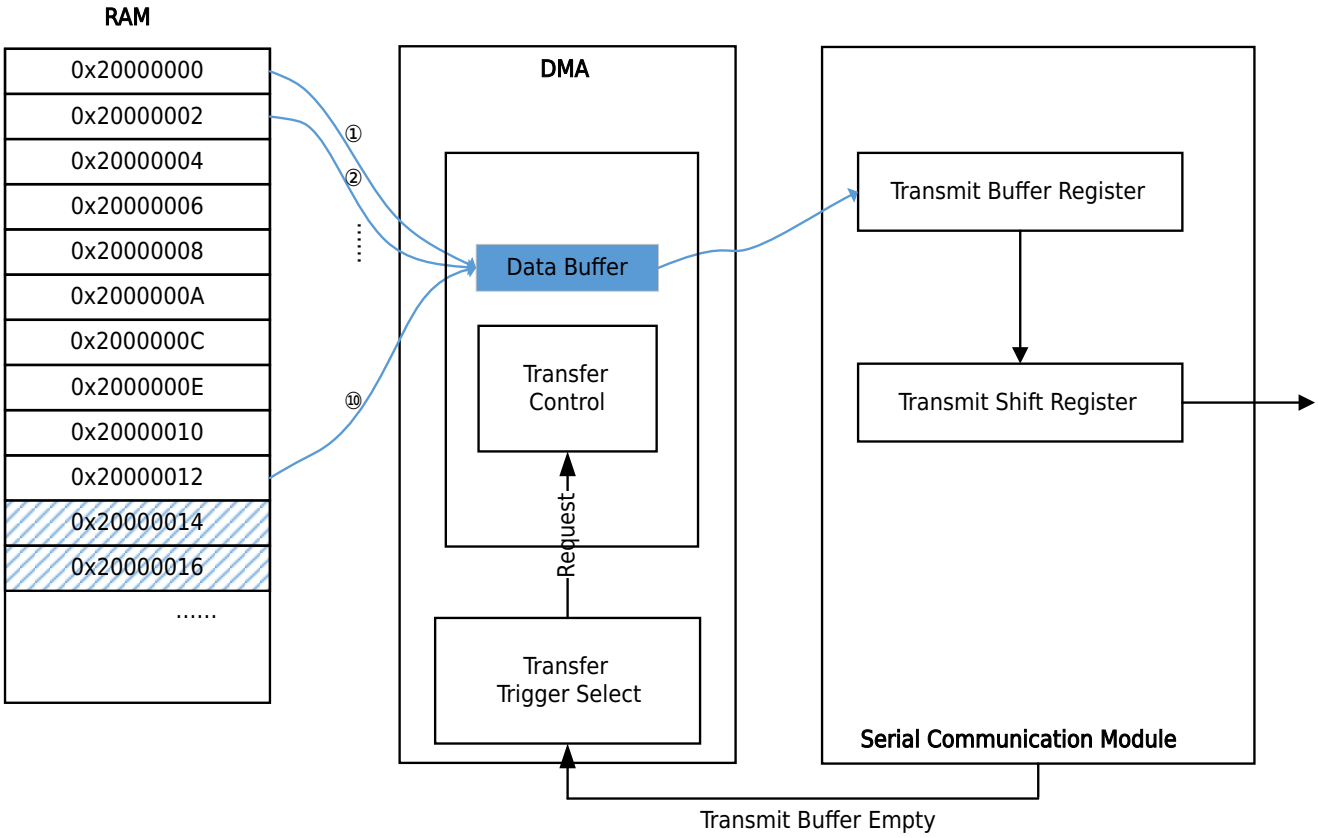

Figure 13-6 Application Example 2: Memory-to-Peripheral Transfer

13.4.3 Memory-to-Memory Chain Transfer

Target

Perform chain transfer to transfer 3 data blocks from RAM to 3 different addresses. Where, first block: 10 data items of 32-bit width, from 0x20000000 to 0x20001000. Second block: 20 data items of 16-bit width, from 0x20000100 to 0x20001100. Third block: 40 data items of 8-bit width, from 0x20000200 to 0x20001200.

Register Setting

1. Enable the DMA controller by writing 1 to DMA_EN.EN.
2. Select a channel, e.g., channel 0, and configure the first transfer descriptor (descriptor0) as follows:
   a. Write DMA_SAR0 to configure the source address as SRAM region 0x20000000.
   b. Write DMA_DAR0 to configure the destination address as SRAM region 0x20001000.
   c. Write DMA_DTCTL0 to configure the block size as 10.
   d. Write the address of the second descriptor (descriptor1) 0x20001800 to the linked list pointer register DMA_LLP0.

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e. Configure the channel control register DMA_CHCTL0 to configure the transmission parameters for the first data block as follows:
   1) Chain transfer enabled.
   2) Chain transfer mode is to directly start the next transfer.
   3) Source address and destination address increment.
   4) The data width is 32-bit.
   5) Interrupt enable inactive.

3. Configure the second transfer descriptor (descriptor1) at address 0x20001800 in RAM as follows:
   a. Write 32-bit data 0x20000100 to 0x20001800, which is the source address for the second transfer.
   b. Write 32-bit data 0x20001100 to 0x20001804, which is the destination address for the second transfer.
   c. Write to 0x20001808 to configure the block size as 20.
   d. Write 32-bit data 0x20001820 to 0x20001818, which is the address of the third transfer descriptor (descriptor2).
   e. Write the control data for the second transfer to 0x2000181C, which configures:
      1) Chain transfer enabled.
      2) Chain transfer mode is to directly start the next transfer.
      3) Source address and destination address increment.
      4) The data width is 16-bit.
      5) Interrupt enable inactive.
4. Configure the third transfer descriptor (descriptor2) at address 0x20001820 in RAM as follows:
   a. Write the 32-bit data 0x20000200 to 0x20001820; this sets the source address for the third transfer.
   b. Write the 32-bit data 0x20001200 to 0x20001824; this sets the destination address for the third transfer.
   c. Block size as 40 at 0x20001828.
   d. Last transfer in chain at 0x20001838 by writing 32-bit data 0x0.
   e. Write the control data for the third transfer to 0x2000183C, which configures:
      1) Chain transfer disabled.
      2) Source address and destination address increment.
      3) The data width is 8-bit.
      4) Interrupt enable active.
5. Configure the DMA_TRGSEL0 register to select software trigger as the start request for DMA channel 0.
6. Write 1 to the channel enable bit DMA_CHEN.CHEN0 to enable channel 0.
7. Write INTSFTTRG.STRG to 1 to send a start request, and DMA starts transferring data.

Transfer Process

The software starts DMA and starts transmission. After the first transmission is completed, due to the chain transfer mode being set to directly start the next transmission and interrupts being disabled, DMA reads the second transfer descriptor (descriptor1) into the channel register. The second transmission starts directly based on the parameters configured in the descriptor. After the second transmission is completed, the third transfer descriptor (descriptor2) is read into the channel register. The third transmission starts based on the parameters configured in the descriptor. After the third transmission is complete, the last transmission is linked according to the configuration information, and because the

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interrupt enable is enabled, DMA will generate a transfer completion interrupt and clear the channel enable bit DMA_CHEN.CHEN0.

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13.5 Register Description

13.5.1 Register List

Base address: 0x40053000

Table 13-2 DMA Controller (DMA) Register Offset

Offset	Register	Description	Width
0x00	DMA_EN	DMA Enable Register	32
0x04	DMA_INTSTAT0	Interrupt Status Register 0	32
0x08	DMA_INTSTAT1	Interrupt Status Register 1	32
0x0C	DMA_INTMASK0	Interrupt Mask Register 0	32
0x10	DMA_INTMASK1	Interrupt Mask Register 1	32
0x14	DMA_INTCLR0	Interrupt Status Clear Register 0	32
0x18	DMA_INTCLR1	Interrupt Status Clear Register 1	32
0x1C	DMA_CHEN	Channel Enable Register	32
0x20	DMA_REQSTAT	Transfer Request Status Register	32
0x24	DMA_CHSTAT	Channel Status Register	32
0x2C	DMA_RCFGCTL	Channel Reset Control Register	32
0x30	DMA_SWREQ	Software Trigger Register	32
0x34	DMA_CHENCLR	Channel Enable Reset Register	32
0x40+0x40*x	DMA_SARx	Transmission Source Address Register	32
0x44+0x40*x	DMA_DARx	Transmission Destination Address Register	32
0x48+0x40*x	DMA_DTCTLx	Transfer Data Control Register	32
0x4C+0x40*x	DMA_RPTx	Address Repeat Control Register	32
0x4C+0x40*x	DMA_RPTBx	Address Repeat Control Register B	32
0x50+0x40*x	DMA_SNSEQCTLx	Source Address NonSequence Control Register	32
0x50+0x40*x	DMA_SNSEQCTLBx	Source Address NonSequence Control Register B	32
0x54+0x40*x	DMA_DNSEQCTLx	Destination Address NonSequence Control Register	32
0x54+0x40*x	DMA_DNSEQCTBx	Destination Address NonSequence Control Register B	32
0x58+0x40*x	DMA_LLPx	Linked List Pointer Register	32
0x5C+0x40*x	DMA_CHCTLx	Channel Control Register	32

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Offset	Register	Description	Width
0x60+0x40*x	DMA_MONSARx	Source Address Monitor Register	32
0x64+0x40*x	DMA_MONDARx	Destination Address Monitor Register	32
0x68+0x40*x	DMA_MONDTCTLx	Transfer Data Control Monitor Register	32
0x6C+0x40*x	DMA_MONRPTx	Address Repeat Control Monitor Register	32
0x70+0x40*x	DMA_MONSNSEQCTLx	Source Address NonSequence Control Monitor Register	32
0x74+0x40*x	DMA_MONDNSEQCTLx	Destination Address NonSequence Control Monitor Register	32

Note

The x in the table represents the existence of multiple registers, with values 0-3.

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13.5.2 DMA Enable Register (DMA_EN)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																															EN
Access																																RW

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-
0	EN	DMA Enable Bit ● 0b0: Disable ● 0b1: Enable	RW

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13.5.3 Interrupt Status Register 0 (DMA_INTSTAT0)

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																REQERR				Reserved								TRNERR			
Access																	RO												RO			

Bit	Name	Functional Description	Access
31:20	*Reserved*	-	-
19:16	REQERR	Transfer Request Overflow Error Interrupt Bit Corresponding to REQERR3-REQERR0: ● 0b0: No transfer request overflow error for this channel ● 0b1: Transfer request overflow error for this channel, meaning a new transfer request arrived while the previous request is still pending **Note** Each bit corresponds to a transmission channel.	RO
15:4	*Reserved*	-	-
3:0	TRNERR	Transfer Error Interrupt Bit Corresponding to TRNERR3-TRNERR0: ● 0b0: No transfer error for this channel ● 0b1: Transfer error for this channel **Note** Each bit corresponds to a transmission channel.	RO

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13.5.4 Interrupt Status Register 1 (DMA_INTSTAT1)

Offset	Bit Position																													
0x08	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved												BTC				Reserved												TC			
Access													RO																RO			

Bit	Name	Functional Description	Access
31:20	*Reserved*	-	-
19:16	BTC	Block Transfer Complete Interrupt Bit For BTC3-BTC0, the interrupt occurs after the completion of one block transfer: ● 0b0: No block transfer interrupt for this channel. ● 0b1: Block transfer interrupt for this channel. **Note** Each bit corresponds to a transmission channel.	RO
15:4	*Reserved*	-	-
3:0	TC	Transfer Complete Interrupt Bit Corresponding to TC3-TC0, this interrupt occurs after completing the number of transmissions set by DMA_DTCTLx.CNT: ● 0b0: No transfer completed interrupt for this channel. ● 0b1: Transfer completed interrupt for this channel. **Note** Each bit corresponds to a transmission channel.	RO

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13.5.5 Interrupt Mask Register 0 (DMA_INTMASK0)

Offset	Bit Position																													
0x0C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved													MSKREQERR			Reserved													MSKTRNERR		
Access														RW																RW		

Bit	Name	Functional Description	Access
31:20	*Reserved*	-	-
19:16	MSKREQERR	Transmission Request Overflow Interrupt Mask Corresponding to MSKREQERR3-MSKREQERR0: ● 0b0: Do not mask the transfer request overflow interrupt. ● 0b1: Mask the transfer request overflow interrupt. **Note** Each bit corresponds to a transmission channel.	RW
15:4	*Reserved*	-	-
3:0	MSKTRNERR	Transfer Error Interrupt Mask Corresponding to MSKTRNERR3-MSKTRNERR0: ● 0b0: Do not mask the transfer error interrupt. ● 0b1: Mask the transfer error interrupt. **Note** Each bit corresponds to a transmission channel.	RW

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13.5.6 Interrupt Mask Register 1(DMA_INTMASK1)

Offset	Bit Position																													
0x10	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved												MSKBTC				Reserved												MSKTC			
Access													RW																RW			

Bit	Name	Functional Description	Access
31:20	*Reserved*	-	-
19:16	MSKBTC	Block Transfer Complete Interrupt Mask Corresponding to MSKBTC3-MSKBTC0: ● 0b0: Do not mask the block transfer completed interrupt. ● 0b1: Mask the block transfer completed interrupt. **Note** Each bit corresponds to a transmission channel.	RW
15:4	*Reserved*	-	-
3:0	MSKTC	Transfer Completed Interrupt Mask Corresponding to MSKTC3-MSKTC0: ● 0b0: Do not mask the transfer completed interrupt. ● 0b1: Mask the transfer completed interrupt. **Note** Each bit corresponds to a transmission channel.	RW

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13.5.7 Interrupt Status Clear Register 0 (DMA_INTCLR0)

Offset	Bit Position																													
0x14	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved												CLRREQERR				Reserved												CLRTRNERR			
Access													WO																WO			

Bit	Name	Functional Description	Access
31:20	*Reserved*	-	-
19:16	CLRREQERR	Transfer Request Overflow Error Interrupt Reset Corresponding to CLRREQERR3-CLRREQERR0: Write 1 to reset the transfer request overflow error interrupt status bit, write 0 has no effect; read always returns 0. **Note** Each bit corresponds to a transmission channel.	WO
15:4	*Reserved*	-	-
3:0	CLRTRNERR	Transfer Error Interrupt Reset Bit Corresponding to CLRTRNERR3-CLRTRNERR0: Write 1 to reset the transfer error interrupt status bit, write 0 has no effect; read always returns 0. **Note** Each bit corresponds to a transmission channel.	WO

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13.5.8 Interrupt Status Clear Register 1 (DMA_INTCLR1)

Offset	Bit Position																													
0x18	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved													CLRBTC			Reserved												CLRTC			
Access														WO															WO		

Bit	Name	Functional Description	Access
31:20	*Reserved*	-	-
19:16	CLRBTC	Block Transfer Complete Interrupt Reset Corresponding to CLRBTC3-CLRBTC0: Write 1 to reset the block transfer completed interrupt status bit, write 0 has no effect; read always returns 0. **Note** Each bit corresponds to a transmission channel.	WO
15:4	*Reserved*	-	-
3:0	CLRTC	Transfer Completed Interrupt Reset Corresponding to CLRTC3-CLRTC0: Write 1 to reset the transfer completed interrupt status bit, write 0 has no effect; read always returns 0. **Note** Each bit corresponds to a transmission channel.	WO

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13.5.9 Channel Enable Register (DMA_CHEN)

Offset	Bit Position																															
0x1C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																														CHEN	
Access																															RW	

Bit	Name	Functional Description	Access
31:4	*Reserved*	-	-
3:0	CHEN	Channel Enable Bit Corresponding to CHEN3-CHEN0: ● 0b0: The channel is disabled ● 0b1: The channel is enabled Write 1 to CHEN[x] sets CHEN[x] to 1, write 0 has no effect. When writing 1 to the DMA_CHENCLR.CHENCLR[x] bit, CHEN[x] clears 0 and forces to interrupt the ongoing transport of channel x. The enable bit remains at 1 during the transmission process, and will be automatically cleared to 0 after the number of transmissions set by register DMA_DTCTLx.CNT is completed. If DMA_DTCTLx.CNT is set to 0, it will not be automatically cleared after the transfer is completed, which means unlimited transfers. **Note** ● Each bit corresponds to a transmission channel. ● Set CHEN[x] to 1 after configuring all 8 descriptor registers for channel x to enable the channel. When CHEN[x] is 1, write operations to the descriptor registers for channel x has no effect.	RW

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13.5.10 Transfer Request Status Register (DMA_REQSTAT)

Offset	Bit Position																													
0x20	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																RCFGREQ	Reserved												CHREQ		
Access																	RO													RO		

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15	RCFGREQ	Channel Reset Request Flag ● 0b0: No channel reset request. ● 0b1: Channel reset request present. **Note** Set to 1 after external reset request input; cleared to 0 after channel reset initiation or when channel reset is disabled.	RO
14:4	*Reserved*	-	-
3:0	CHREQ	Channel Transfer Request Flag Bit Corresponding to CHREQ3-CHREQ0: ● 0b0: No transfer request for this channel ● 0b1: Transfer request for this channel present **Note** Each bit corresponds to a transmission channel. Set to 1 after external transfer request input; cleared to 0 after transfer initiation for the channel, transmission error, or when the transfer permission bit (DMAEN or CHEN[x]) is written to 0. If this bit is 1, and another transfer request is input for the channel, a transfer request overflow error occurs, the second request is ignored, but this flag bit remains 1, continuing to wait for transfer.	RO

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13.5.11 Channel Status Register (DMA_CHSTAT)

Offset	Bit Position																													
0x24	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved												CHACT				Reserved														RCFGACT	DMAACT
Access													RO																		RO	RO

Bit	Name	Functional Description	Access
31:20	*Reserved*	-	-
19:16	CHACT	Transfer Action Channel Monitor Bit Corresponding to CHACT3-CHACT0: ● 0b0: The channel is idle ● 0b1: The channel is in action **Note** Each bit corresponds to a transmission channel.	RO
15:2	*Reserved*	-	-
1	RCFGACT	DMA Channel Reset Action Monitor Bit ● 0b0: DMA is not in channel reset action ● 0b1: DMA is in channel reset action	RO
0	DMAACT	DMA Action Monitor Bit ● 0b0: DMA is not in transfer action ● 0b1: DMA is in transfer action	RO

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13.5.12 Channel Reset Control Register (DMA_RCFGCTL)

Offset	Bit Position																													
0x2C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved										CNTMD		DARMD		SARMD		Reserved		RCFGCHS		Reserved									RCFGLLP	RCFGEN	
Access											RW		RW		RW				RW											RW	RW	

Bit	Name	Functional Description	Access
31:22	*Reserved*	-	-
21:20	CNTMD	Remaining Transfer Count Counter Reset Method ● 0b00: Remain unchanged ● 0b01: Source address mode ● 0b10/0b11: Destination address mode When source address mode is selected, and source address Non-Sequence reset is selected, the remaining transfer count counter updates to the state after the transfer count specified by DMA_SNSEQCTLBx.SNSCNTB; when source address repeat is selected, the counter updates to the state after the transfer count specified by DMA_RPTBx.SRPTB. When the source address selection is held, the remaining transfer times counter also remains unchanged. When the destination address mode is selected, it is similar to the source address mode.	RW
19:18	DARMD	Destination Address Reset Mode ● 0b00: Remain unchanged ● 0b01: NonSequence reset, the next transfer's destination address updates to addr_base + (DMA_DNSEQCTLBx.DNSDIST x DMA_CHCTLx.HSIZE(bit) /8), where addr_base is the starting address of the current NonSequence transmission region. ● 0b10/0b11: Repeated reset, the next transfer's destination address updates to the initial setting value of the DMA_DARx register. **Notice** Only set DARMD[1:0] to 0b01 when destination address NonSequence is enabled (DMA_CHCTLx.DNSEQEN=1) for this channel. Only set DARMD[1] to 1 when destination address repeated transfer is enabled (DMA_CHCTLx.DRPTEN=1) for this channel.	RW

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Bit	Name	Functional Description	Access
17:16	SARMD	Source Address Reset Method ● 0b00: Remain unchanged ● 0b01: NonSequence reset, the next transfer's source address updates to addr_base + (DMA_SNSEQCTLBx.SNSDIST x DMA_CHCTLx.HSIZE(bit) /8), where addr_base is the starting address of the current NonSequence transmission region. ● 0b10/0b11: Repeated reset, the next transfer's source address updates to the initial setting value of the DMA_SARx register. **Notice** Only set SARMD[1:0] to 0b01 when source address NonSequence is enabled (DMA_CHCTLx.SNSEQEN=1) for this channel. Only set SARMD[1] to 1 when source address repeated transfer is enabled (DMA_CHCTLx.SRPTEN=1) for this channel.	RW
15:12	*Reserved*	-	-
11:8	RCFGCHS	Reset Channel Selection ● 0x0: Channel 0 ● 0x1: Channel 1 ● ... ● 0x3: Channel 3 ● Others: Setting prohibited	RW
7:2	*Reserved*	-	-
1	RCFGLLP	Linked List Pointer Channel Reset ● 0b0: Linked list pointer reset inactive ● 0b1: Linked list pointer reset active **Notice** When RCFGPLL is set to 1, the channel will reload a new descriptor from memory, so Bits 21-16 of this register are inactive.	RW
0	RCFGEN	Channel Reset Permission ● 0b0: Disable event-triggered channel configuration register forced update ● 0b1: Enable event-triggered channel configuration register forced update	RW

Notice

Set this register when DMA_EN.EN is 0, and it must be set before the first transfer of the reset channel.

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13.5.13 Software Trigger Register (DMA_SWREQ)

Offset	Bit Position																													
0x30	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	SWRCFGWP								SWREQWP								SWRCFGREQ	Reserved													SWREQ	
Access	WO								WO								WO														WO	

Bit	Name	Functional Description	Access
31:24	SWRCFGWP	Software Channel Reset Request Write Protection Software reset request write protection, write 0xA2 to SWRCFGWP to release write protection	WO
23:16	SWREQWP	Software Channel Trigger Request Write Protection Software trigger request write protection, write 0xA1 to SWREQWP to release write protection	WO
15	SWRCFGREQ	Software Channel Reset Request Writing 1 (with SWRCFGWP written to 0xA2) generates a software channel reset request, write 0 has no effect. **Note** Software-triggered channel reset function, equivalent to AOS trigger effect.	WO
14:4	*Reserved*	-	-
3:0	SWREQ	Software Channel Trigger Request Corresponding to SWREQ3-SWREQ0: Writing 1 (with SWREQWP written to 0xA1) generates a software channel reset request, write 0 has no effect. **Note** Each bit corresponds to a transmission channel. Software-triggered start and transfer, equivalent to AOS trigger effect.	WO

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13.5.14 Channel Enable Reset Register (DMA_CHENCLR)

Offset	Bit Position																													
0x34	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																													CHENCLR		
Access																														WO		

Bit	Name	Functional Description	Access
31:4	*Reserved*	-	-
3:0	CHENCLR	Channel Enable Bit Reset Write 1 to reset the channel enable bit CHEN, write 0 has no effect; read always returns 0. When writing 1, if the channel is currently transferring, DMA will forcibly terminate the transfer after completing the current data read/write. **Note** Each bit corresponds to a transmission channel.	WO

13.5.15 Transmission Source Address Register (DMA_SARx) (x=0-3)

Offset: 0x40+0x40*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	SAR																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	SAR	Transfer Source Address Set transfer source address **Note** ● When the transfer data width is 16-bit, i.e. DMA_CHCTLx.HSIZE=0b01, SAR[0] is disabled. ● When the transfer data width is 32-bit, i.e. DMA_CHCTLx.HSIZE=0b10/0b11, SAR[1:0] is disabled.	RW

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13.5.16 Transmission Destination Address Register (DMA_DARx) (x=0-3)

Offset: 0x44+0x40*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	DAR																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	DAR	Transmission Destination Address Set transmission destination address **Note** ● When the transfer data width is 16-bit, i.e. DMA_CHCTLx.HSIZE=0b01, DAR[0] is disabled. ● When the transfer data width is 32-bit, i.e. DMA_CHCTLx.HSIZE=0b10/0b11, DAR[1:0] is disabled.	RW

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13.5.17 Transfer Data Control Register (DMA_DTCTLx) (x=0-3)

Offset: 0x48+0x40*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000001																															
Name	CNT																Reserved						BLKSIZE									
Access	RW																						RW									

Bit	Name	Functional Description	Access
31:16	CNT	Transfer Count The total number of transfers, each request starts the transfer of a data block, the number of transfers is decremented by 1 when it is completed, and a transfer completion interrupt occurs when it is reduced to 0. If it is set to 0, it means unlimited transmission. Each time a data block is requested to be transmitted, the transmission times counter will remain at 0 when it is completed, and no transmission completion interrupt will be generated.	RW
15:10	*Reserved*	-	-
9:0	BLKSIZE	Data Block Size Set the size of the data block, up to 1024 pieces of data can be configured. The width of each data item is determined by the DMA_CHCTLx.HSIZE bit. Register value set to 1 transfers 1 data item, set to 0 transfers 1024 data items.	RW

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13.5.18 Address Repeat Control Register (DMA_RPTx) (x=0-3)

Offset: 0x4C+0x40*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved										DRPT[9:0]										Reserved						SRPT[9:0]			
Access											RW																RW			

Bit	Name	Functional Description	Access
31:26	*Reserved*	-	-
25:16	DRPT[9:0]	Destination Address Repeat Area Size Set destination address repeat area size The destination device reloads the destination address to the initial setting value of the DMA_DARx register after transferring DRPT data items. Register set to 10 reloads the address after transferring 10 data items, set to 0 reloads after 1024 data items. The width of each data item is determined by DMA_CHCTLx.HSIZE.	RW
15:10	*Reserved*	-	-
9:0	SRPT[9:0]	Source Address Repeat Area Size Set the source address repeat area size The source device reloads the source address to the initial setting value of the DMA_SARx register after transferring SRPT data items. Register set to 10 reloads the address after transferring 10 data items, set to 0 reloads after 1024 data items. The width of each data item is determined by DMA_CHCTLx.HSIZE.	RW

Note

1. This register configures the size of the source and destination address repeat regions. Repeat transfer requires configuring the DMA_CHCTLx.SRPTEN/DRPTEN bits to be active, and configuring the DMA_CHCTLx.SINC/DINC bits to enable address update as increment or decrement. When configuring the DMA_CHCTLx.SINC/DINC bits to enable address update as fixed, address repeated jump is invalid.
2. This register is disabled when the channel's reset function is enabled.

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13.5.19 Address Repeat Control Register B (DMA_RPTBx) (x=0-3)

Offset: 0x4C+0x40*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved										DRPTB[9:0]						Reserved						SRPTB[9:0]									
Access											RW												RW									

Bit	Name	Functional Description	Access
31:26	*Reserved*	-	-
25:16	DRPTB[9:0]	Destination Address Repeat Area Size Set destination address repeat area size The destination device reloads the destination address to the initial setting value of the DMA_DARx register after transferring DRPTB blocks. The block size is determined by DMA_DTCTLx.BLKSIZE and DMA_CHCTLx.HSIZE.	RW
15:10	*Reserved*	-	-
9:0	SRPTB[9:0]	Source Address Repeat Area Size Set the source address repeat area size The source device reloads the initial value set in the DMA_SARx register into the source address after transferring every SRPTB blocks of data. The block size is determined by DMA_DTCTLx.BLKSIZE and DMA_CHCTLx.HSIZE.	RW

Note

1. This register configures the size of the source and destination address repeat regions. Repeat transfer requires configuring the DMA_CHCTLx.SRPTEN/DRPTEN bits to be active, and configuring the DMA_CHCTLx.SINC/DINC bits to enable address update as increment or decrement. When configuring the DMA_CHCTLx.SINC/DINC bits to enable address update as fixed, address repeated jump is invalid.
2. This register is only active when the channel's reset function is enabled, replacing the DMA_RPTx register. It is disabled when the channel's reset function is disabled.

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13.5.20 Source Address NonSequence Control Register (DMA_SNSEQCTLx) (x=0-3)

Offset: 0x50+0x40*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	SNSCNT[11:0]												SOFFSET[19:0]																			
Access	RW												RW																			

Bit	Name	Functional Description	Access
31:20	SNSCNT[11:0]	Source Address Jump Data Size Set the amount of data transferred before the source address jumps. After the source device transmits SNSCNT data, the source address jumps according to the offset specified by SOFFSET. If the register is set to 10, the address will jump after every 10 data transmissions, if it is set to 0, the address will jump after every 4096 data transmissions.	RW
19:0	SOFFSET[19:0]	Source Address Jump Offset When NonSequence address transmission, set the offset of the source address jump. The offset is relative to the current transfer address, that is, the last transfer address before the jump. The jump direction is forward or backward according to the DMA_CHCTLx.SINC bit. For details, refer to Schematic Diagram of NonSequence Address Transfer. NonSequence address transfer is disabled when DMA_CHCTLx.SINC is set to fixed address. The jump address will be calculated according to the number of bits set by the data width (DMA_CHCTLx.HSIZE) and the value of SOFFSET. Address Offset=SOFFSET×(DMA_CHCTLx.HSIZE(bit)/8) For example, when SOFFSET is set to 10, and the data width is 32-bit, the address offset is 10×4=40; if the data width is 16-bit, the offset is 10×2=20; if 8-bit, the offset is 10×1=10. The next transmission's source address=current source address ± address offset	RW

Note

1. NonSequence for the source device requires configuring the DMA_CHCTLx.SNSEQEN bit to be active, and configuring the DMA_CHCTLx.SINC bit to enable address update as increment or decrement.
2. This register is disabled when the channel's reset function is enabled.

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13.5.21 Source Address NonSequence Control Register B (DMA_SNSEQCTLBx) (x=0-3)

Offset: 0x50+0x40*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	SNSCNTB[11:0]												SNSDIST[19:0]																			
Access	RW												RW																			

Bit	Name	Functional Description	Access
31:20	SNSCNTB[11:0]	Source Address Jump Data Size Set the amount of data transferred before the source address jumps. After the source device transmits SNSCNTB data blocks, the source address jumps according to the address interval specified by SNSDIST. The block size is determined by DMA_DTCTLx.BLKSIZE and DMA_CHCTLx.HSIZE.	RW
19:0	SNSDIST[19:0]	Source NonSequence Area Address Distance When NonSequence address transmission, set the distance between two NonSequence areas of the source device. The jump direction is forward or backward according to the DMA_CHCTLx.SINC bit. For details, refer to Figure 13-4 : Schematic Diagram of NonSequence Reset. NonSequence address transfer is disabled when DMA_CHCTLx.SINC is set to fixed address. The address spacing is calculated based on the data width defined by the DMA_CHCTLx.HSIZE bit field and the SNSDIST value as follows: Address Distance=SNSDIST×(DMA_CHCTLx.HSIZE(bit)/8) For example, when SNSDIST is set to 10, and the data width is 32-bit, the address distance is 10×4=40; if 16-bit, the distance is 10×2=20; if 8-bit, the distance is 10×1=10. The next transmission's source address=starting address of the current source NonSequence region ± address distance.	RW

Note

1. NonSequence for the source device requires configuring the DMA_CHCTLx.SNSEQEN bit to be active, and configuring the DMA_CHCTLx.SINC bit to enable address update as increment or decrement.
2. This register is only active when the channel's reset function is enabled, replacing the DMA_SNSEQCTLx register. It is disabled when the channel's reset function is disabled.

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13.5.22 Destination Address NonSequence Control Register (DMA_DNSEQCTLx) (x=0-3)

Offset: 0x54+0x40*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	DNSCNT[11:0]												DOFFSET[19:0]																			
Access	RW												RW																			

Bit	Name	Functional Description	Access
31:20	DNSCNT[11:0]	Destination Address Jump Data Size Set the amount of data transferred before the destination address jumps. After the destination device transmits DNSCNT data, the destination address jumps according to the offset specified by DOFFSET. If the register is set to 10, the address will jump after every 10 data transmissions, if it is set to 0, the address will jump after every 4096 data transmissions.	RW
19:0	DOFFSET[19:0]	Destination Address Jump Address Offset When NonSequence address transfer, set the offset of the destination address jump. The offset is relative to the current transfer address, that is, the last transfer address before the jump. The jump direction is forward or backward according to the DMA_CHCTLx.DINC bit. For details, refer to the Schematic Diagram of NonSequence Address Transfer. NonSequence address transfer is disabled when DMA_CHCTLx.DINC is set to fixed address. The jump address is calculated based on the bit count set by the data width (DMA_CHCTLx.HSIZE) and the DOFFSET value. Address Offset=DOFFSET×(DMA_CHCTLx.HSIZE(bit)/8) For example, when DOFFSET is set to 10, and the data width is 32-bit, the address offset is 10×4=40; if 16-bit, the offset is 10×2=20; if 8-bit, the offset is 10×1=10. The next transmission's destination address=current destination address ± address offset.	RW

Note

1. NonSequence for the destination device requires configuring the DMA_CHCTLx.DNSEQEN bit to be active, and configuring the DMA_CHCTLx.DINC bit to enable address update as increment or decrement.
2. This register is disabled when the channel's reset function is enabled.

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13.5.23 Destination Address NonSequence Control Register B (DMA_DNSEQCTLBx) (x=0-3)

Offset: 0x54+0x40*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	DNSCNTB[11:0]												DNSDIST[19:0]																			
Access	RW												RW																			

Bit	Name	Functional Description	Access
31:20	DNSCNTB[11:0]	Destination Address Jump Data Size Set the amount of data transferred before the destination address jumps. The destination device jumps the destination address by the DNSDIST-specified distance after transferring SNSCNTB blocks. The block size is determined by DMA_DTCTLx.BLKSIZE and DMA_CHCTLx.HSIZE.	RW
19:0	DNSDIST[19:0]	Destination NonSequence Region Address Distance When NonSequence address transmission, set the distance between two NonSequence areas of the destination device. The jump direction is forward or backward according to the DMA_CHCTLx.DINC bit. For details, refer to Figure 13-4 : Schematic Diagram of NonSequence Reset. NonSequence address transfer is disabled when DMA_CHCTLx.DINC is set to fixed address. The address distance is calculated based on the bit count set by the data width (DMA_CHCTLx.HSIZE) and the DNSDIST value. Address Distance=DNSDIST×(DMA_CHCTLx.HSIZE(bit) /8) For example, when DNSDIST is set to 10, and the data width is 32-bit, the address distance is 10×4=40; if 16-bit, the distance is 10×2=20; if 8-bit, the distance is 10×1=10. The next transmission's destination address=starting address of the current destination NonSequence region ± address distance	RW

Note

1. NonSequence for the destination device requires configuring the DMA_CHCTLx.DNSEQEN bit to be active, and configuring the DMA_CHCTLx.DINC bit to enable address update as increment or decrement.
2. This register is only active when the channel's reset function is enabled, replacing the DMA_DNSEQCTLx register. It is disabled when the channel's reset function is disabled.

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13.5.24 Linked List Pointer Register (DMA_LLPx) (x=0-3)

Offset: 0x58+0x40*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	LLP[31:2]																														Reserved	
Access	RW																															

Bit	Name	Functional Description	Access
31:2	LLP[31:2]	Linked List Pointer When the chain transmission is enabled, set the address of the next transmission descriptor to word alignment, that is, LLP[1:0] is fixed to 0	RW
1:0	*Reserved*	-	-

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13.5.25 Channel Control Register (DMA_CHCTLx) (x=0-3)

Offset: 0x5C+0x40*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00001000																															
Name	Reserved																			IE	LLPRUN	LLPEN	HSIZE		DNSEQEN	SNSEQEN	DRPTEN	SRPTEN	DINC		SINC	
Access																				RW	RW	RW	RW		RW	RW	RW	RW	RW		RW	

Bit	Name	Functional Description	Access
31:13	*Reserved*	-	-
12	IE	Interrupt Enable Bit Configure whether the channel generates an interrupt ● 0b0: The channel does not generate an interrupt ● 0b1: The channel generates an interrupt	RW
11	LLPRUN	Chain Transfer Mode Selection When the chain transfer is active, set whether to start the transfer corresponding to the new descriptor immediately after loading the new descriptor specified by the linked list pointer when the current transfer is complete ● 0b0: Do not initiate transfer immediately, wait for the next transfer request ● 0b1: Initiate transfer immediately after the new descriptor is loaded	RW
10	LLPEN	Chain Transfer Enable ● 0b0: Chain transfer is disabled ● 0b1: Chain transfer is enabled	RW
9:8	HSIZE	Transfer Data Width ● 0b00: 8-bit ● 0b01: 16-bit ● 0b10/0b11: 32-bit	RW
7	DNSEQEN	Destination Address NonSequence Enabled ● 0b0: NonSequence address transfer disabled ● 0b1: NonSequence address transfer enabled	RW
6	SNSEQEN	Source Address NonSequence Enabled ● 0b0: NonSequence address transfer disabled ● 0b1: NonSequence address transfer enabled	RW
5	DRPTEN	Destination Address Repeat Enable Bit Set whether to allow the destination address to reload the initial value ● 0b0: Do not reload the initial value ● 0b1: Reload the initial value for address repeat transfer	RW

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Bit	Name	Functional Description	Access
4	SRPTEN	Source Address Repeat Enable Bit Set whether to allow the source address to reload the initial value ● 0b0: Do not reload the initial value ● 0b1: Reload the initial value for address repeat transfer	RW
3:2	DINC	Destination Address Update Method ● 0b00: Fixed ● 0b01: Incrementing ● 0b10/0b11: Decrementing	RW
1:0	SINC	Source Address Update Method ● 0b00: Fixed ● 0b01: Incrementing ● 0b10/0b11: Decrementing	RW

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13.5.26 Source Address Monitor Register (DMA_MONSARx) (x=0-3)

Offset: 0x60+0x40*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	SAR																															
Access	RO																															

Bit	Name	Functional Description	Access
31:0	SAR	Transfer Source Address Set source address **Note** ● When the transfer data width is 16-bit, i.e., DMA_CHCTLx.HSIZE=0b01, SAR[0] is invalid. ● When the transfer data width is 32-bit, i.e., DMA_CHCTLx.HSIZE=0b10/0b11, SAR[1:0] is invalid.	RO

Note

The DMA_SARx register remains unchanged before and after DMA transfer, while the DMA_MONSARx register updates after each data block transfer by DMA. DMA_MONSARx.SAR updates to the next transmission address based on the fixed/incrementing/decrementing/repeated jump/NonSequence jump settings.

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13.5.27 Destination Address Monitor Register (DMA_MONDARx) (x=0-3)

Offset: 0x64+0x40*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	DAR																															
Access	RO																															

Bit	Name	Functional Description	Access
31:0	DAR	Transmission Destination Address Set transmission destination address **Note** ● When the transfer data width is 16-bit, i.e., DMA_CHCTLx.HSIZE=0b01, DAR[0] is invalid. ● When the transfer data width is 32-bit, i.e., DMA_CHCTLx.HSIZE=0b10/0b11, DAR[1:0] is invalid.	RO

Note

The DMA_DARx register remains unchanged before and after DMA transfer, while the DMA_MONDARx register updates after each block transfer. DMA_MONDARx.DAR updates to the next transmission address based on the fixed/incrementing/decrementing/repeated jump/NonSequence jump settings.

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13.5.28 Transfer Data Control Monitor Register (DMA_MONDTCTLx) (x=0-3)

Offset: 0x68+0x40*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000001																															
Name	CNT[15:0]																Reserved						BLKSIZE[9:0]									
Access	RO																						RO									

Bit	Name	Functional Description	Access
31:16	CNT[15:0]	Transfer Count The number of transfers remaining **Note** When the transfer count is 0 (DMA_DTCTLx.CNT=0x0000), this bit field remains 0.	RO
15:10	*Reserved*	-	-
9:0	BLKSIZE[9:0]	Data block size **Note** When this bit field is 0, it indicates that 1024 data items are transferred per transaction.	RO

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13.5.29 Address Repeat Control Monitor Register (DMA_MONRPTx) (x=0-3)

Offset: 0x6C+0x40*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved										DRPT[9:0]						Reserved						SRPT[9:0]									
Access											RO												RO									

Bit	Name	Functional Description	Access
31:26	*Reserved*	-	-
25:16	DRPT[9:0]	Destination Address Repeat Region Size	RO
15:10	*Reserved*	-	-
9:0	SRPT[9:0]	Source Address Repeat Region Size	RO

Note

The (DMA_RPTx) register remains unchanged before and after DMA transfer, while the (DMA_MONRPTx) register updates after each block transfer.

DMA_MONRPTx.SRPT[9:0] and DMA_MONRPTx.DRPT[9:0] update as follows:

- When channel reset is disabled: subtract the block size, and reload the DMA_RPTx setting value when it is reduced to 0.
- When channel reset is enabled: Decrement by 1, reload the initial value when it reaches 0.

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13.5.30 Source Address NonSequence Control Monitor Register (DMA_MONSNSEQCTLx) (x=0-3)

Offset: 0x70+0x40*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	SNSCNT[11:0]												SOFFSET[19:0]																			
Access	RO												RO																			

Bit	Name	Functional Description	Access
31:20	SNSCNT[11:0]	Source Address Jump Data Size Set the amount of data transferred before the source address jump	RO
19:0	SOFFSET[19:0]	Source Address Jump Offset Source address offset	RO

Note

The DMA_SNSEQCTLx register remains unchanged before and after DMA transfer, while the DMA_MONSNSEQCTLx register updates after each data block transfer by DMA.

Update method for DMA_MONSNSEQCTLx.SNSCNT[11:0]:

- When channel reset is disabled: Subtract the block size, reload initial value of DMA_SNSEQCTLx when it is reduced to 0.
- When channel reset is enabled: Decrement by 1, reload the initial value when it reaches 0.

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13.5.31 Destination Address NonSequence Control Monitor Register (DMA_MONDNSEQCTLx) (x=0-3)

Offset: 0x74+0x40*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	DNSCNT[11:0]												DOFFSET[19:0]																			
Access	RO												RO																			

Bit	Name	Functional Description	Access
31:20	DNSCNT[11:0]	Destination Address Jump Data Size Set the amount of data transferred before the destination address jump	RO
19:0	DOFFSET[19:0]	Destination Address Jump Address Offset Destination address offset	RO

Note

The DMA_DNSEQCTLx register remains unchanged before and after DMA transfer, while the DMA_MONDNSEQCTLx register updates after each data block transfer by DMA.

Update method for DMA_MONDNSEQCTLx.SNSCNT[11:0]:

- When channel reset is disabled: Subtract block size, reload initial value of DMA_DNSEQCTLx when it is reduced to 0.
- When channel reset is enabled: Decrement by 1, reload the initial value when it reaches 0.

13.6 Precautions

- DMA registers only support 32-bit read and write operations, 8-bit/16-bit read and write operations are inactive.

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14 Voltage Comparator (CMP)

14.1 Introduction

Voltage Comparator (hereinafter referred to as CMP) is a peripheral module that compares two analog voltages and outputs the comparison result. This product is equipped with two groups of 3 comparison channels: CMP1 and CMP2, and CMP3.

14.2 Features

- 3 comparison channels can independently perform normal comparison
- The combination of CMP1 and CMP2 can implement the window comparison function
- Each comparison channel's positive and negative voltage inputs have multiple input sources (IO, DAC) to choose from
- Hysteresis voltage is configurable
- A noise filter can filter the comparator output, with 7 sampling clocks to choose from
- Timer PWM can be used for comparator blanking window control
- Interrupts can be generated at the edges of comparison result changes, other peripherals can be triggered, and STOP mode can be woken up
- Compare results can be monitored through registers and output to the external pin VCOUT
- Compare results can be used for EMB control events

14.3 Functional Description

14.3.1 Function Block Diagram

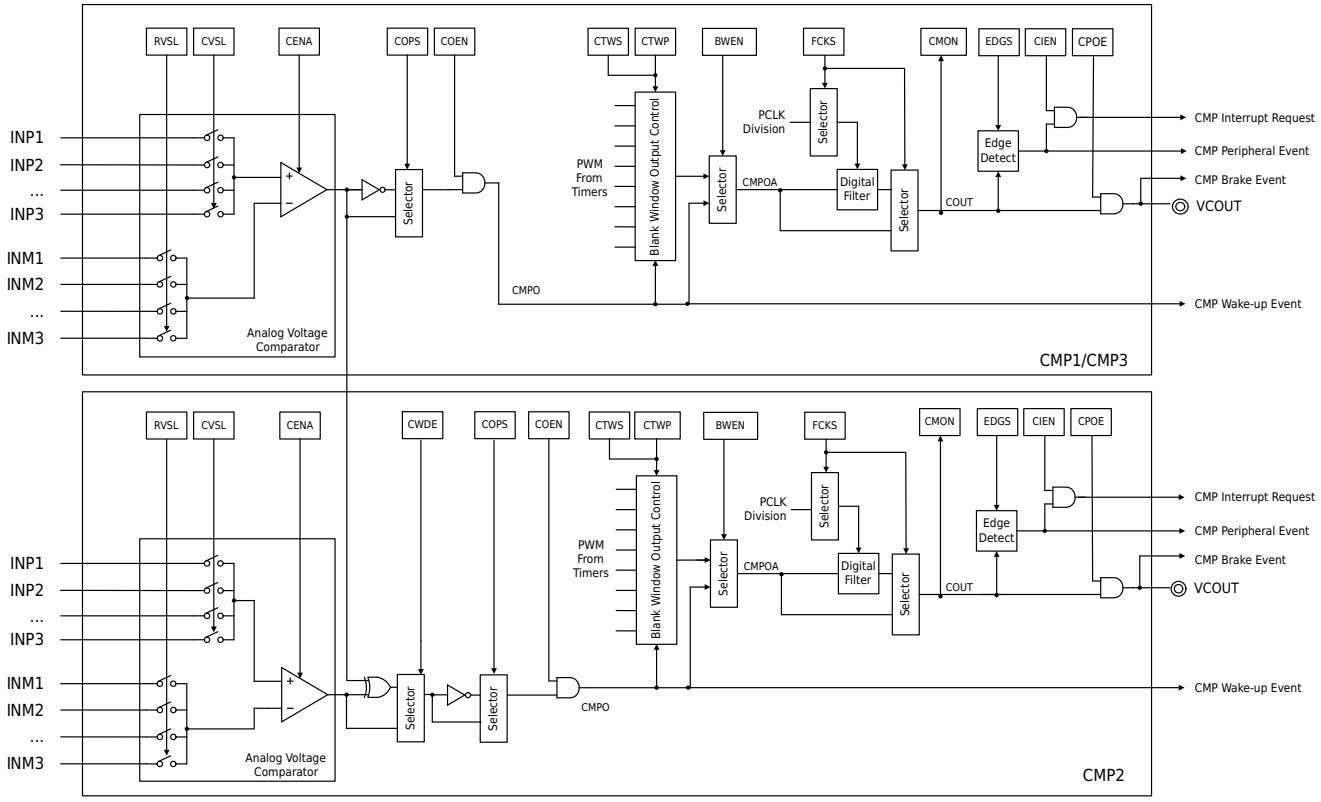

Figure 14-1 CMP Function Block Diagram

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Table 14-1 CMP Pin List

Pin Name	Input/Output	Function
AVCC	Input	Analog Power
AVSS	Input	Analog Ground
CMP1_INP1	Input	CMP1 Positive Analog Input
CMP1_INP2	Input	CMP1 Positive Analog Input
CMP1_INP3	Input	CMP1 Positive Analog Input
CMP123_INM1	Input	CMP1-3 Negative Analog Input
CMP123_INM2	Input	CMP1-3 Negative Analog Input
CMP2_INP1	Input	CMP2 Positive Analog Input
CMP2_INP2	Input	CMP2 Positive Analog Input
CMP2_INP3	Input	CMP2 Positive Analog Input
CMP3_INP1	Input	CMP3 Positive Analog Input
CMP3_INP2	Input	CMP3 Positive Analog Input
CMP3_INP3	Input	CMP3 Positive Analog Input
CMP1_VCOUT	Output	CMP1 External Port Output
CMP2_VCOUT	Output	CMP2 External Port Output
CMP3_VCOUT	Output	CMP3 External Port Output
CMP_VCOUT	Output	CMP1-3 External Port Output

14.3.2 Input Selection

The analog inputs of CMP1-3 are selected according to the following table.

Table 14-2 CMP Positive Input List

Compare Channel	CVSL=0b001 (INP1)	CVSL=0b010 (INP2)	CVSL=0b100 (INP3)
CMP1	CMP1_INP1	CMP1_INP2	CMP1_INP3
CMP2	CMP2_INP1	CMP2_INP2	CMP2_INP3
CMP3	CMP3_INP1	CMP3_INP2	CMP3_INP3

Table 14-3 CMP Negative Input List

Compare Channel	RVSL=0b001 (INM1)	RVSL=0b010 (INM2)	RVSL=0b100 (INM3)
CMP1	CMP123_INM1	CMP123_INM2	DAO
CMP2	CMP123_INM1	CMP123_INM2	DAO
CMP3	CMP123_INM1	CMP123_INM2	DAO

14.3.3 Normal Compare

CMP1-3 can independently perform normal comparison. Taking CMP1 as an example, the setting steps are as follows:

Step1. Enable CMP1 module function (CMU_FCG.CMP write 0).

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Step2. Set CMP_PMSR.CVSL to select the positive voltage.
Set CMP_PMSR.RVSL to select the negative voltage.

Step3. Set CMP_MDR.CENA to 1 to enable the comparator.

Step4. Wait for the comparator to stabilize t_{CMP} (for specific values, see the "Electrical Specifications" in the "Datasheet").

Step5. Set CMP_FIR.FCKS to set the sampling period for digital filtering.
Set CMP_FIR.EDGS and CMP_FIR.CIEN to set the edge where the interrupt occurs.

Step6. Set CMP_OCR.CPOE and CMP_OCR.COPS to set the output of VCOUT.

Step7. Set CMP_OCR.COEN to 1 to allow comparator output.

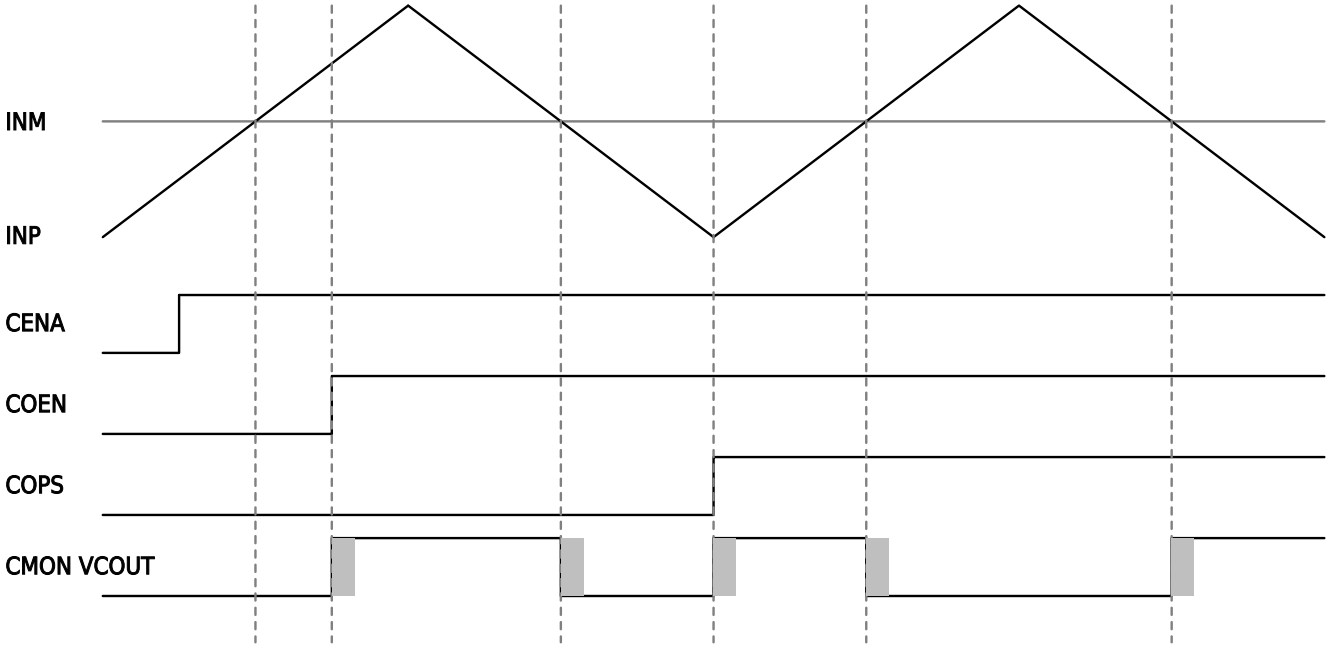

Figure 14-2 Voltage Comparison Diagram

As shown in the figure above, during non-inverting output, if the positive voltage is higher than the negative voltage after CMP output is enabled, the CMP_OMR.CMON bit is 1; if the positive voltage is lower than the negative voltage, the CMON bit is 0. During inverting output, the result of CMON is opposite to that during non-inverting output. If a digital filter is used, due to synchronization and filter sampling, the edge of CMON changes will be at least 6 CMPCLK periods late.

14.3.4 Window Compare

Window comparison can be achieved when CMP1/CMP2 operate simultaneously. The setting steps are as follows:

Step1. Enable CMP1 and CMP2 module functions (CMU_FCG.CMP write 0).

Step2. Set CMP1_PMSR.CVSL to select the positive voltage as the lower limit of the window.
Set CMP1_PMSR.RVSL to select the negative terminal voltage.

Step3. Set CMP2_PMSR.RVSL to select the same negative terminal voltage as CMP1.
Set CMP2_PMSR.CVSL to select the positive terminal voltage as the upper limit of the window.

Step4. Set CMP2_MDR.WDEN to 1 to start window comparison;

Step5. Set CMP1_MDR.CENA and CMP2_MDR.CENA to 1 to start the comparators.

Step6. Wait for the stabilization time t_{CMP} (refer to the "Electrical Specifications" section of the Datasheet for specific values).

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Step7. Set CMP2_FIR.FCKS to set the digital filter.
Set CMP2_FIR.EDGS, CMP2_FIR.CIEN to set interrupt and edge detection conditions.

Step8. Set CMP2_OCR.CPOE, CMP2_OCR.COPS to set the output of VCOUT;

Step9. Set CMP1_OCR.COEN and CMP2_OCR.COEN to 1 to allow comparator output.

During window comparison, CMP2 completes the monitoring, filtering, interrupting, and outputting of comparison results.

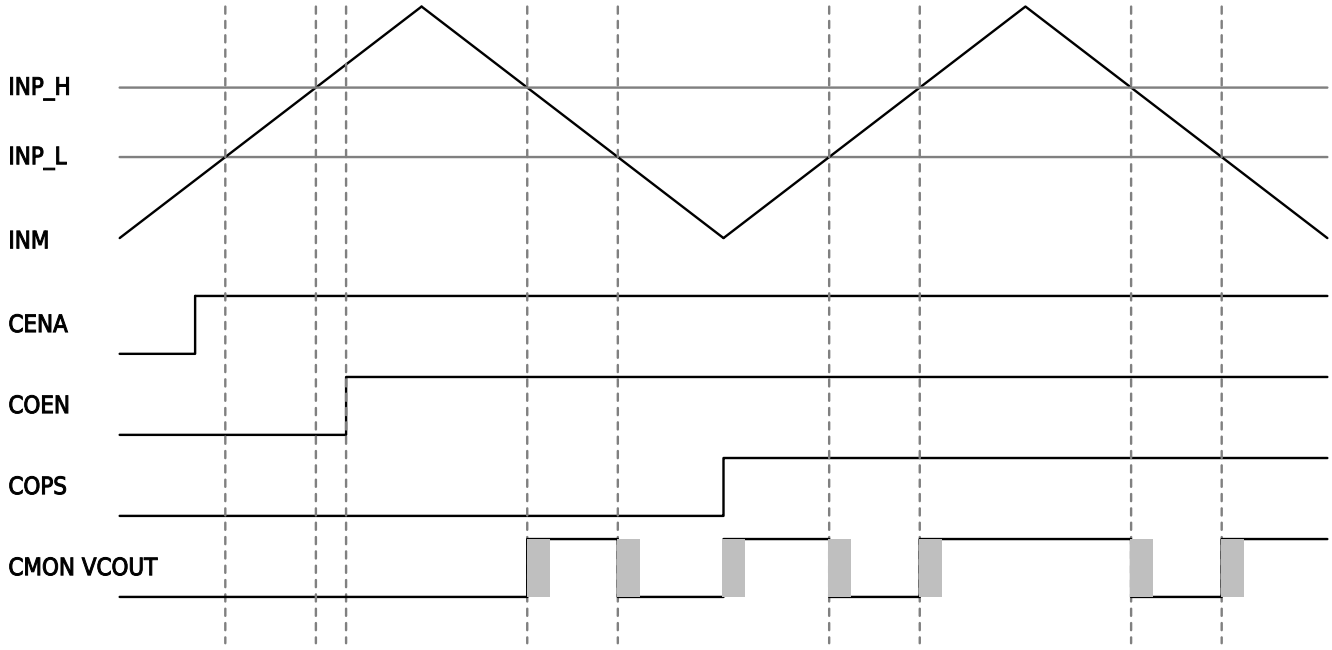

Figure 14-3 Window Compare Diagram

As shown in the figure above, during non-inverting output, if the negative voltage is within the window composed of the two positive voltages after CMP output is enabled, the CMP2_OMR.CMON bit is 1; if the negative voltage is outside the window composed of the two positive voltages, the CMON bit is 0. During inverting output, the result of CMON is opposite to that during non-inverting output. If a digital filter is used, due to synchronization and filter sampling, the edge of CMON changes will be at least 6 CMPCLK periods late.

14.3.5 Input Scan

Input scanning enables multiple inputs to be compared with the same input in turn. When using this function, first select the positive or negative input for scanning by setting the CMP_MDR.CSMD bit. Then, select the specific positive/negative inputs that participate in the scanning by setting the CMP_SCCR.SISL bit. The CMP_SCCR.SPRD bit sets the scanning period, which is the time interval for switching inputs during scanning. The SSTB bit sets the time to turn off the CMP output after switching inputs; this is to wait for the CMP output to stabilize and thus prevent false operations of the system.

Set the CMP_MDR.CSST bit to 1 to start scanning. During scanning, non-scanned ports remain unchanged, and scanned ports switch cyclically according to the set scanning period. If a rising edge is detected in the comparison result during this period, CSST is automatically cleared and scanning stops. At this point, the current input status of the positive and negative terminals can be determined by reading the CMP_SCMR register. When CSST is written to 1 again, the scanning action restarts.

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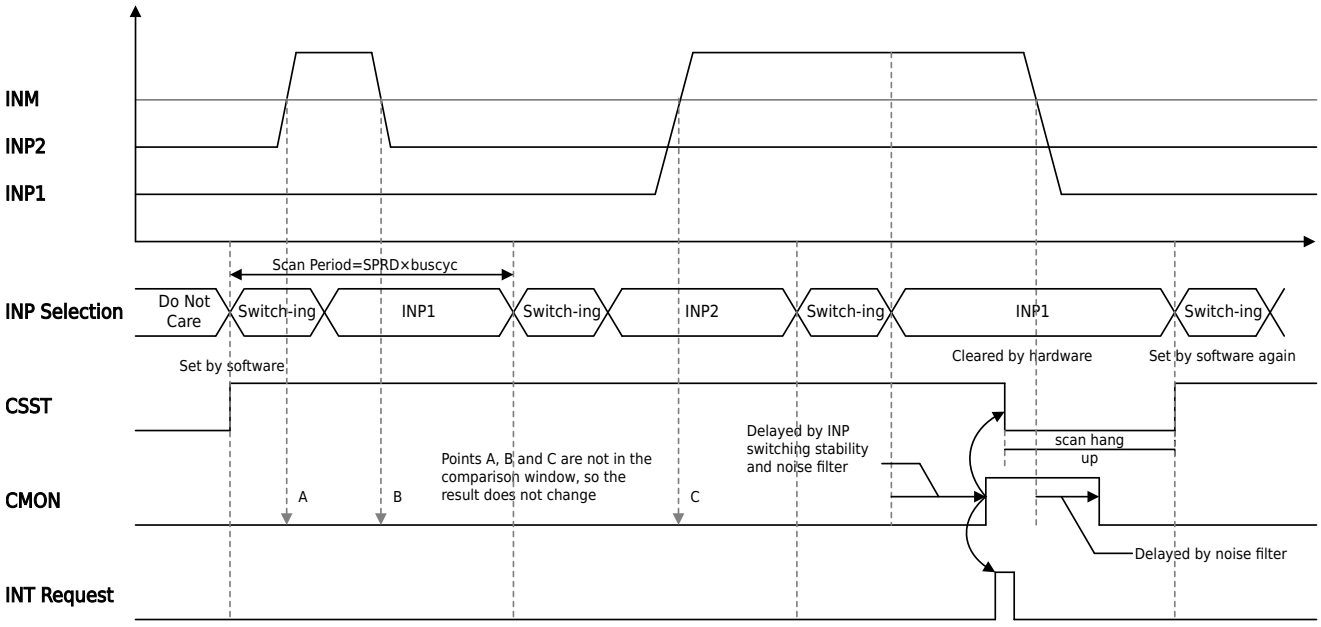

Figure 14-4 Input Scanning Diagram

The above figure is a schematic diagram of the action of scanning two positive inputs. In the first two scanning periods, since the changes in INP1 and INP2 (points A, B, C in the diagram) do not occur within their respective scanning periods, the comparison result does not change. When INP1 is scanned again next, INP1 is higher than INM, causing the comparator to invert. At this point, the comparator output is closed to wait for the input to stabilize. After the comparator output stabilizes, the comparison result is output after noise filtering. At the same time, the scanning action automatically stops and an interrupt is generated. Next, CMP will continue to work in the state of comparing INP1 with INM until software restarts scanning.

Please follow the following process for setup when using:

Step1. Set CMP_MDR.CSMD to 0b10 or 0b11;

Step2. When CSMD is set to 0b10, set CMP_PMSR.RVSL to select an INM input;
When CSMD is set to 0b11, set CMP_PMSR.CVSL to select an INP input;

Step3. Set CMP_SCCR.SISL to select the scanning target port;
Set CMP_SCCR.SSTB to config the output stabilization time;
Set CMP_SCCR.SPRD to config the scanning period;

Step4. Set CMP_FIR.EDGS to select rising edge detection;
Set CMP_FIR.CIEN to allow interrupts;

Step5. Set CMP_MDR.CENA to start the comparator;

Step6. Wait for the stabilization time t_{CMP} of the comparator (refer to the "Electrical Specifications" section of the Datasheet for specific values);

Step7. Set CMP_OCR.COEN to allow comparator output;

Step8. Set CMP_MDR.CSST to start scanning.

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Note

To ensure correct operation, the set values must satisfy "Scanning period > Output stabilization time + Filter sampling period×4 + CMPCLK period×8". At the same time, rising edge detection should be set to automatically stop scanning or generate an interrupt. If falling edge detection is required, it can be achieved by setting CMP inverting output. In addition, since the input scanning of CMP1/2 needs to be started separately, it is difficult to achieve synchronization. It is recommended not to use input scanning during window comparison.

14.3.6 Window Output

The CMP can use the outputs of Timer4 as Blank-Window signals to control the windowed output of the comparison result CMPOA, providing convenience for applications such as timer PWM zero-crossing detection. There are two modes for window output: level mode and edge mode.

1. Level Mode

   When windowed output is enabled (set the CMP_OCR.BWEN bit to 1) and level mode is selected (set the CMP_OCR.BWMD bit to 0), select one or more timer PWMs as Blank-Windows through the CMP_BWSR1.CTWS bit, and select the active level for each Blank-Window through the CMP_BWSR1.CTWP bit. In this way, when a Blank-Window is active, the windowed output CMPOA is fixed to the state set by the CMP_OCR.BWOL bit.

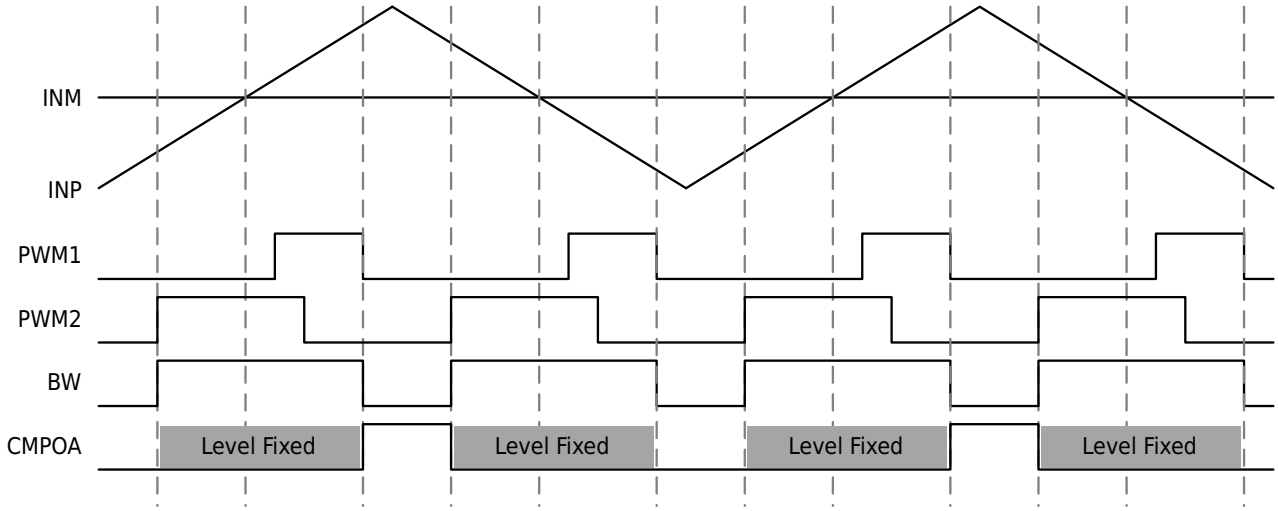

Figure 14-5 Window Output Diagram I

As shown in the figure above, two PWM signals are selected as the Blank-Window, both configured as active-high. When the Blank-Window is enabled, the output state of CMPOA is forced to low level. Thus, when the Blank-Window signal is at a high level, CMPOA is forced to a low level; when Blank-Window is at a low level, CMPOA outputs the normal comparator result.

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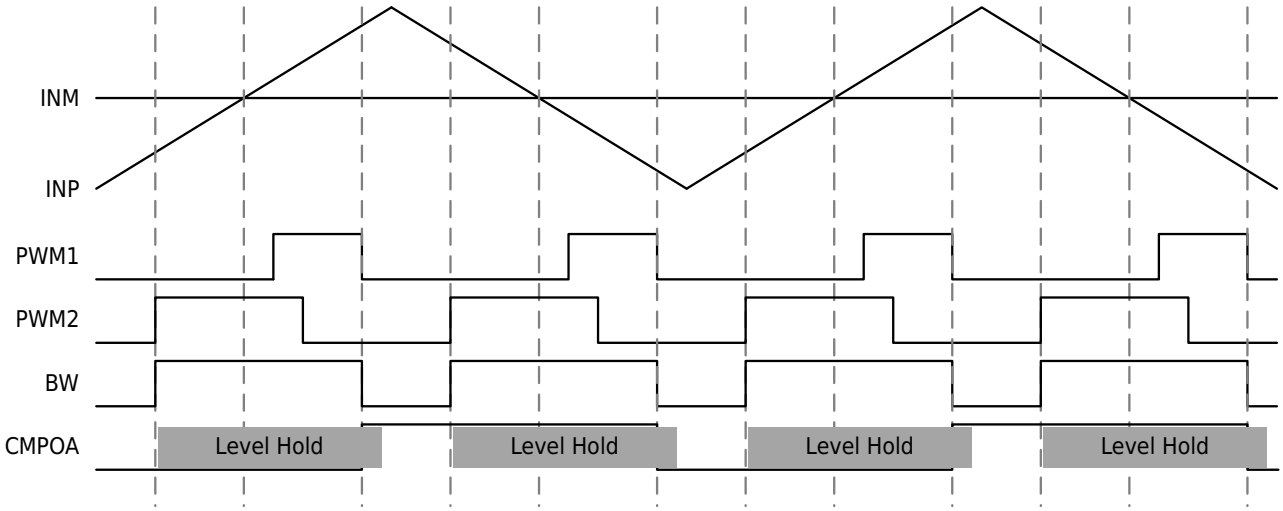

Figure 14-6 Window Output Diagram II

As shown in the diagram above, two PWMs are selected as Blank-Windows, both active at high level. When a Blank-Window is active, the output status of CMPOA is set to hold. Thus,when the Blank-Window signal is high, CMPOA maintains its previous state; when Blank-Window is at a low level, CMPOA outputs the normal comparator result,but the output is delayed by 1 to 3 CMPCLK periods due to synchronization and sampling.

2. Edge Mode

When windowed output is enabled (set the CMP_OCR.BWEN bit to 1) and edge mode is selected (set the CMP_OCR.BWMD bit to 1), select one or more timer PWMs as Blank-Windows through the CMP_BWSR1.CTWS bit, and select the active edge of the window signal through the CMP_BWSR2.TWEG. In this way, when a Blank-Window signal is active at the specified edge, the windowed output CMPOA is fixed to the state set by the CMP_OCR.BWOL bit and maintained for N CMPCLK periods set by the CMP_BWSR2.MSKW.

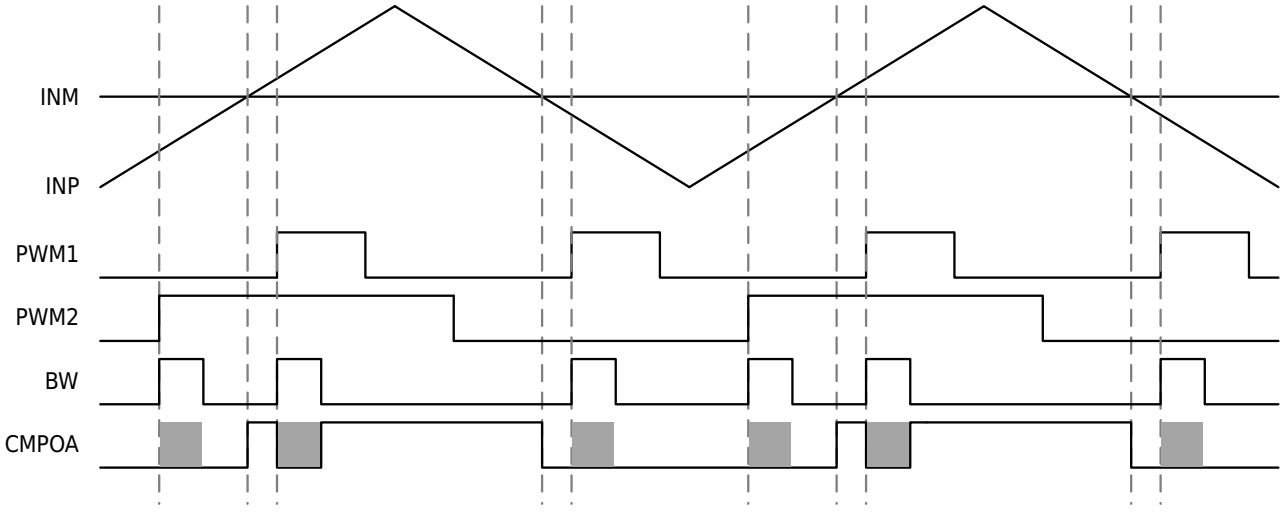

Figure 14-7 Window Output Diagram III

As shown in the diagram above, two PWMs are selected as Blank-Windows, with the rising edge selected as the active edge. When a Blank-Window is active, the output status of CMPOA is set to low level. As a result, a Blank-Window signal is generated at each rising edge of the PWM signal. When the Blank-Window signal is at a high level, CMPOA is fixed at a low level, and when the Blank-Window signal is at a low level, CMPOA outputs the comparison result normally.

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14.3.7 Hysteresis Function

To avoid false outputs caused by noise signals, each comparison channel has a configurable hysteresis function, and the hysteresis voltage can be selected through the CMP_MDR.HYST bit. The hysteresis function is disabled when the HYST bit is set to 0b000.

14.3.8 Noise Filter

Each comparison channel contains a noise filter. The noise filter samples the comparator output CMPOA during each sampling clock period. If the same value is sampled three consecutive times, the value is output to COUT in the next sampling clock period; otherwise, COUT remains unchanged. The sampling clock can be selected through the CMP_FIR.FCKS bit. The noise filter is disabled when the FCKS bit is set to 0b00.

14.3.9 External Pin Output

The comparison result COUT output by the noise filter can be output to the external port VCOUT. Whether VCOUT output is enabled and the output polarity (non-inverting output or inverting output) can be set through the CMP_OCR.CPOE and COPS bits. After reset, the port corresponding to VCOUT is a general-purpose port in input status. Therefore, it must also be set to VCOUT output function through the port register.

14.3.10 12-bit DAC Configuration

A 12-bit DAC provides an internal voltage for the CMP. The output voltage during operation is:

Two 8-bit DACs provides two internal voltage for the CMP. The output voltage during operation is:

Output Voltage = Reference Voltage × Conversion Data / 4095

The DAC conversion data is set by DAC_DADR. Please refer to the following procedure for configuration:

Step1. Set DAC_DADR to configure the conversion data.

Step2. Set DAC_DACR to configure the reference voltage.

Step3. Set DAC_DACR to enable the DAC.

Step4. Wait for the DAC startup time T_{wakeup}. (For specific values, please refer to the "Electrical Specifications" chapter in the "Datasheet".)

Step5. Configure the comparator.

14.3.11 Interrupt and Event

Interrupt requests can be generated for the results of all comparison channels. When using, the CMP_FIR.CIEN bit must be set to 1, and the edge of the comparison result that can generate an interrupt is set through the CMP_FIR.EDGS bit (value other than 0b00). If noise filtering and inverting output are used, edge detection is performed on the signal after noise filtering and inverting output.

When INTC_WKEN.CMP*WKEN=1, CMPO can wake up the stop low power mode. The system will be woken up and an interrupt will be generated when CMPO changes from low to high.

The generation conditions for peripheral trigger events and interrupt requests are the same, but the event trigger function must be enabled or disabled through the hardware trigger source register of the target peripheral, independent of the CIEN bit.

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14.4 Register Description

14.4.1 Register List

- CMP1 base address: 0x4004A000
- CMP2 base address: 0x4004A100
- CMP3 base address: 0x4004A400

Table 14-4 Voltage Comparator (CMP) Register Offset

Offset	Register	Description	Width
0x00	CMP_MDR	Comparator Working Mode Register	8
0x01	CMP_FIR	Comparator Filter and Interrupt Register	8
0x02	CMP_OCR	Comparator Output Control Register	8
0x03	CMP_OMR	Comparator Output Monitoring Register	8
0x04	CMP_PMSR	Comparator Positive and Negative Input Selection Register	32
0x10	CMP_BWSR1	Comparator Blank Window Output Source Register 1	32
0x14	CMP_BWSR2	Comparator Blank Window Output Source Register 2	16
0x18	CMP_SCCR	Comparator Input Scan Control Register	32
0x1C	CMP_SCMR	Comparator Input Scan Monitoring Register	32

DAC base address: 0x4004A000

Table 14-5 12-bit DAC Register Offset

Offset	Register	Description	Width
0x0C	DAC_DADR	DAC Data Register	16
0x0E	DAC_DACR	DAC Control Register	8

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14.4.2 Comparator Working Mode Register (CMP_MDR)

Offset	Bit Position							
0x00	7	6	5	4	3	2	1	0
Reset	0x00							
Name	CSST	CSMD		WDEN	HYST			CENA
Access	RW	RW		RW	RW			RW

Bit	Name	Functional Description	Access
7	CSST	Input Scan Start ● 0b0: Stop input scanning ● 0b1: Start input scanning	RW
6:5	CSMD	Input Scan Mode ● 0b0x: Disable input scanning ● 0b10: Scan positive input INP ● 0b11: Scan negative input INM	RW
4	WDEN	Window Compare Selection ● 0b0: Normal compare mode ● 0b1: Window compare mode **Note** This bit exists only in CMP2. After setting to window compare mode, the filtering, edge detection, and output control for the window comparison results are all performed by CMP2.	RW
3:1	HYST	Hysteresis Voltage Selection ● 0b000: 0mV (no hysteresis) ● 0b001: 10mV ● 0b010: 20mV ● 0b011: 30mV ● 0b100: 40mV ● 0b101: 50mV ● 0b110: 60mV ● 0b111: 70mV **Note** The values above are typical values. For the error range, please refer to the "Electrical Specifications" chapter in the "Datasheet". When the CMP and ADC input pins are multiplexed, the hysteresis function of the CMP must be disabled.	RW

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Bit	Name	Functional Description	Access
0	CENA	Comparator Operation Permission ● 0b0: Comparator stopped ● 0b1: Comparator working **Note** After setting CENA from 0 to 1 each time, please wait for T_{cmp} stabilization time (for specific values, please refer to the "Electrical Specifications" chapter in the "Datasheet") before performing subsequent operations.	RW

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14.4.3 Comparator Filter and Interrupt Register (CMP_FIR)

Offset	Bit Position							
0x01	7	6	5	4	3	2	1	0
Reset	0x00							
Name	CRF	CFF	EDGS		CIEN	FCKS		
Access	RW	RW	RW		RW	RW		

Bit	Name	Functional Description	Access
7	CRF	Comparator Output Rising Edge Flag Write 1 to clear the flag, write 0 has no effect Read: ● 0b0: Rising edge of comparator output COUT not detected ● 0b1: Rising edge of comparator output COUT detected	RW
6	CFF	Comparator Output Falling Edge Flag Write 1 to clear the flag, write 0 has no effect Read: ● 0b0: Falling edge of comparator output COUT not detected ● 0b1: Falling edge of comparator output COUT detected	RW
5:4	EDGS	Comparator Output Edge Detection Selection ● 0b00: Not detect edges of comparator output COUT ● 0b01: Detect rising edge of comparator output COUT ● 0b10: Detect falling edge of comparator output COUT ● 0b11: Detect rising and falling edges of comparator output COUT **Note** Changing this bit may cause a interrupt or peripheral trigger event, so set the register if the interrupt disable or peripheral trigger is disabled. After register settings, please clear the corresponding interrupt flag.	RW
3	CIEN	Comparator Interrupt Permission ● 0b0: Comparator interrupt disabled ● 0b1: Comparator interrupt enabled	RW

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Bit	Name	Functional Description	Access
2:0	FCKS	Comparator Result Filtering Sample Selection ● 0b000: Noise filter not used ● 0b001: Noise filter used, sampling through PCLK3/4 ● 0b010: Noise filter used, sampling through PCLK3/8 ● 0b011: Noise filter used, sampling through PCLK3/16 ● 0b100: Noise filter used, sampling through PCLK3/32 ● 0b101: Noise filter used, sampling through PCLK3/64 ● 0b110: Noise filter used, sampling through PCLK3/128 ● 0b111: Noise filter used, sampling through PCLK3/256 **Note** Please rewrite this bit when the comparator output is disabled (i.e., the CMP_OCR.COEN is "0"). When switching this bit from "0b000" to other values, please use the filtered output after 4 samples as the interrupt request or peripheral trigger event. Changing this bit may cause a interrupt or peripheral trigger event, so set the register if the interrupt disable or peripheral trigger is disabled. After register settings, please clear the corresponding interrupt flag. In input scan mode, the sampling division of the noise filter can only be set to a maximum of 0b100; otherwise, the timing requirements of the scan cycle cannot be met.	RW

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14.4.4 Comparator Output Control Register (CMP_OCR)

Offset	Bit Position							
0x02	7	6	5	4	3	2	1	0
Reset	0x00							
Name	BWOL		BWMD	BWEN	Reserved	CPOE	COPS	COEN
Access	RW		RW	RW		RW	RW	RW

Bit	Name	Functional Description	Access
7:6	BWOL	Blank-Window Output Level ● 0b00: During the active period of the Blank-Window, the CMPOA outputs a low level. ● 0b01: During the active period of the Blank-Window, the CMPOA outputs a high level. ● 0b1x: During the active period of the Blank-Window, the CMPOA output is held. **Note** When Blank-Window is enabled, with BWOL set to 0b00 or 0b01, and CMP_FIR.FCKS set to 0b000, EMB cannot use the output of this comparator to control the PWM output of TMR4.	RW
5	BWMD	Blank-Window Mode ● 0b0: Level mode ● 0b1: Edge mode	RW
4	BWEN	Blank-Window Enable ● 0b0: Disable ● 0b1: Enable	RW
3	*Reserved*	-	-
2	CPOE	VCOUT Output Enable ● 0b0: VCOUT output disabled ● 0b1: VCOUT output enabled	RW
1	COPS	Comparator Output Polarity Selection ● 0b0: Comparator non-inverting output ● 0b1: Comparator inverting output **Note** Please rewrite COPS when the comparator output is disabled (i.e., COEN bit is 0). Changing the COPS bit may cause an interrupt or peripheral trigger event, so please set this register in the state where the interrupt is disabled or the peripheral trigger function is disabled. After register settings, please clear the corresponding interrupt flag.	RW

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Bit	Name	Functional Description	Access
0	COEN	Comparator Output Permissible ● 0b0: Comparator output disabled (comparator output fixed at low level) ● 0b1: Comparator output enabled	RW

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14.4.5 Comparator Output Monitoring Register (CMP_OMR)

Offset	Bit Position							
0x03	7	6	5	4	3	2	1	0
Reset	0x00							
Name	Reserved							CMON
Access								RO

Bit	Name	Functional Description	Access
7:1	*Reserved*	-	-
0	CMON	Compare Result Monitoring In normal comparative mode: ● 0b0: Positive voltage < negative voltage ● 0b1: Positive voltage > negative voltage In window comparison mode (this bit is only valid for CMP2): ● 0b0: Positive voltage < lower negative voltage, or positive voltage > upper negative voltage ● 0b1: Lower negative voltage < positive voltage < upper negative voltage	RO

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14.4.6 Comparator Positive and Negative Input Selection Register (CMP_PMSR)

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved															CVSL				Reserved										RVSL		
Access																RW														RW		

Bit	Name	Functional Description	Access
31:19	*Reserved*	-	-
18:16	CVSL	Positive Input Selection Select the positive input voltage of the voltage comparator. The positive inputs are detailed in the CMP Positive Input List: ● 0b000: No positive voltage input ● 0b001: Select INP1 as positive voltage ● 0b010: Select INP2 as positive voltage ● 0b100: Select INP3 as positive voltage ● Others: Setting prohibited **Note** When the positive terminal input scanning is active (i.e., CMP_MDR.CSMD = 0b10), the setting of this register is invalid. Please rewrite CVSL when the comparator output is disabled (i.e., CMP_OCR.COEN = 0). After each rewrite of CVSL, wait 300ns before enabling the comparator output (i.e., setting CMP_OCR.COEN to 1). Changing CVSL may cause interrupts or peripheral trigger events, so please set this register when interrupts are disabled or peripheral trigger functions are inactive. After setting the register, clear the corresponding interrupt flags.	RW
15:3	*Reserved*	-	-
2:0	RVSL	Negative Input Selection Select the negative input voltage of the voltage comparator. The selected inputs are detailed in the CMP Negative Input List: ● 0b000: No negative voltage input ● 0b001: Select INM1 as negative voltage ● 0b010: Select INM2 as negative voltage ● 0b100: Select INM3 as negative voltage ● Others: Setting prohibited	RW

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Bit	Name	Functional Description	Access
2:0	RVSL	**Note** When scanning the negative input is enabled (i.e., CMP_MDR.CSMD=0b11), the register setting is disabled. Modify RVSL only when the comparator output is disabled (i.e., the CMP_OCR.COEN bit is set to 0). Please wait for 300ns after rewriting RVSL before enabling the comparator output (i.e., setting the CMP_OCR.COEN bit to 1). Changing RVSL may cause an interrupt or peripheral trigger event, so please set this register in the state where the interrupt is disabled or the peripheral trigger function is disabled. After register settings, please clear the corresponding interrupt flag.	RW

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14.4.7 Comparator Blank Window Output Source Register 1 (CMP_BWSR1)

Offset	Bit Position																													
0x10	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved								CTWP7	CTWP6	CTWP5	CTWP4	CTWP3	CTWP2	CTWP1	CTWP0	Reserved								CTWS7	CTWS6	CTWS5	CTWS4	CTWS3	CTWS2	CTWS1	CTWS0
Access									RW	RW	RW	RW	RW	RW	RW	RW									RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:24	*Reserved*	-	-
23:16	CTWPn (n=7-0)	Window Signal Polarity When Blank-Window is in level mode (CMP_OCR.BWMD=0), set the active level of the window signal used to MASK the comparator output (this bit setting is only active when the corresponding CTWS is 1) : ● 0b0: Comparator output closed when window signal is high ● 0b1: Comparator output closed when window signal is low	RW
15:8	*Reserved*	-	-
7:0	CTWSn (n=7-0)	Window Signal Enable When Blank-Window is enable (CMP_OCR.BWEN=1), select the window signal used to MASK the comparator output. The timer PWM signals corresponding to each bit are detailed in the table below: ● 0b0: Do not select timer PWM output as window signal ● 0b1: Select timer PWM output as window signal	RW

Table 14-18 Timer Window PWM List

CTWS Bit	CMP1	CMP2	CMP3
7	TMR4_OXL	TMR4_OXL	TMR4_OXL
6	TMR4_OXH	TMR4_OXH	TMR4_OXH
5	TMR4_OWL	TMR4_OWL	TMR4_OWL
4	TMR4_OWH	TMR4_OWH	TMR4_OWH
3	TMR4_OVL	TMR4_OVL	TMR4_OVL
2	TMR4_OVH	TMR4_OVH	TMR4_OVH
1	TMR4_OUL	TMR4_OUL	TMR4_OUL
0	TMR4_OUH	TMR4_OUH	TMR4_OUH

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14.4.8 Comparator Blank Window Output Source Register 2 (CMP_BWSR2)

Offset	Bit Position															
0x14	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved						TWEG		MSKW							
Access							RW		RW							

Bit	Name	Functional Description	Access
15:10	*Reserved*	-	-
9:8	TWEG	Window Signal Edge When Blank-Window is in edge mode (CMP_OCR.BWMD=1), set the active edge of the window signal used to MASK the comparator output. ● 0b00: No active edge ● 0b01: Comparator output closed at the rising edge of the window signal ● 0b10: Comparator output closed at the falling edge of the window signal ● 0b11: Comparator output closed at the changing edge of the window signal	RW
7:0	MSKW	Blank-Window Active Width When Blank-Window is in edge mode (CMP_OCR.BWMD=1), set the width of the MASK comparator output. The settable range is 0-255. When the edge set by the TWEG bit is detected in the window signal, the comparator output will be closed and last for the number of CMPCLK periods set by the MSKW bit.	RW

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14.4.9 Comparator Input Scan Control Register (CMP_SCCR)

Offset	Bit Position																													
0x18	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved		SSTB						SPRD								Reserved													SISL		
Access			RW						RW																					RW		

Bit	Name	Functional Description	Access
31:30	*Reserved*	-	-
29:24	SSTB	Output Stabilization Time Output stabilization time of CMP after switching inputs during input scanning. CMP Output Stabilization Time=CMPCLK Period×SSTB Setting Value **Notice** 1. Please set the INP switching stabilization time to be greater than the "Input Channel Switching Stabilization Time" specified in the "Electrical Specifications" section of the Datasheet, taking into account the CMPCLK period. 2. If you need to rewrite SSTB, please stop scanning first.	RW
23:16	SPRD	Input Switching Period Time interval for switching inputs during input scanning, i.e., scanning period. Scanning Period=CMPCLK Period×SPRD Setting Value **Notice** 1. To ensure correct operation, when setting SPRD, please confirm that: Scanning Period > Output Stabilization Time + Filter Sampling Period×4 + CMPCLK Period×8 2. If SPRD needs to be rewritten, please stop scanning first. 3. In input scan mode, subject to the above constraints, the sampling division of the noise filter can only be set to a maximum of PCLK3/32 (CMP_FIR.FCKS≤0b100).	RW
15:3	*Reserved*	-	-
2:0	SISL	Input Selection When scanning the positive input, Bit2-Bit0 correspond to the CMP positive inputs INP3-INP1, respectively When scanning the negative input, Bit2-Bit0 correspond to the CMP negative inputs INM3-INM1, respectively ● 0b0: The input is not the scanning target ● 0b1: The input is the scanning target **Notice** If SISL needs to be rewritten, please stop scanning first.	RW

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14.4.10 Comparator Input Scan Monitoring Register (CMP_SCMR)

Offset	Bit Position																													
0x1C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved													CVST			Reserved													RVST		
Access														RO																RO		

Bit	Name	Functional Description	Access
31:19	*Reserved*	-	-
18:16	CVST	CMP Positive Side Input Status Used to monitor the CMP input status during input scanning. Bit18-Bit16 correspond to the CMP positive inputs INP3-INP1, the selected input is detailed in theCMP Positive Input List: ● 0b0: Not comparing INPn (n=3-1) ● 0b1: Comparing INPn (n=3-1)	RO
15:3	*Reserved*	-	-
2:0	RVST	CMP Negative Side Input Status Used to monitor the CMP input status during input scanning. Bit2-Bit0 correspond to the CMP negative inputs INM3-INM1, the selected input is detailed in theCMP Negative Input List: ● 0b0: Not comparing INMn (n=3-1) ● 0b1: Comparing INMn (n=3-1)	RO

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14.4.11 DAC Data Register (DAC_DADR)

Offset	Bit Position															
0x0C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved				DADR											
Access					RW											

Bit	Name	Functional Description	Access
15:12	*Reserved*	-	-
11:0	DADR	Conversion Data Converts the data setting value	RW

14.4.12 DAC Control Register (DAC_DACR)

Offset	Bit Position							
0x0E	7	6	5	4	3	2	1	0
Reset	0x00							
Name	REFSEL		Reserved		DA2POE	Reserved		DAEN
Access	RW				RW			RW

Bit	Name	Functional Description	Access
7:6	REFSEL	DAC Reference Voltage Selection The following internal voltage are typical values; for error ranges, refer to the "Datasheet": ● 0b00: AVCC ● 0b11: Internal 1.2V reference voltage ● Others: Setting prohibited	RW
5:4	*Reserved*	-	-
3	DA2POE	DAC Output to Port Enabled ● 0b0: DAC output to port disabled ● 0b1: DAC output to port enabled **Notice** The port output is unloaded and intended for debugging purposes only.	RW
2:1	*Reserved*	-	-

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Bit	Name	Functional Description	Access
0	DAEN	DAC Enabled ● 0b0: DAC disabled ● 0b1: DAC enabled	RW

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14.5 Precautions

14.5.1 Module Stop Function

CMP has a module stop function, which can turn off the digital part of the module by setting the module stop register.

CMP1-CMP3 share a module stop control bit (CMU_FCG.Bit3).

All comparator channels are initially in the stopped state, and their respective registers can only be accessed when the module is set to work. Please refer to the "Action Mode and Low Power Mode" section of the "Power Control (PWC) " chapter for register settings.

14.5.2 Power Consumption During Module Stop

When CMP transitions from the working state to the module stop state, the comparator will continue to operate, and the power consumption is equivalent to the working state. To further reduce power consumption, please clear the CMP_MDR.CENA bit.

14.5.3 Power Consumption During Stop Low Power Mode

When the chip enters stop low power mode, if CMP is in the working state, it will continue to operate after entering stop low power mode, and the power consumption is equivalent to the level before entering stop low power mode. To further reduce power consumption, please clear the CMP_MDR.CENA bit before entering stop low power mode.

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15 Analog-to-Digital Converter (ADC)

15.1 Introduction

The 12-bit ADC is an analog-to-digital converter that adopts the successive approximation method. This MCU is equipped with 1 ADC units, a maximum of 16 channels, which can convert analog signals from external pins. Analog input channels can be arbitrarily combined into a sequence for single scan or continuous scan conversion. Supports continuous multiple conversions on any specified channel and averaging of the conversion results. The ADC block also includes an analog watchdog function that monitors the conversion results of any specified channel to detect if they exceed user-set ranges.

15.2 Features

- High Performance
  - 12-bit resolution
  - The clock source of the ADC sampling conversion clock ADCLK is PCLK4 (set by the CMU_ADCKSEL register)
  - Sampling Rate: 3.6Msps (ADCLK=80MHz, 12-bit, 8 sampling cycles, 14 conversion cycles)
  - Independent programming of channel sampling time is supported
  - Each channel has an independent data register
  - Data registers can be configured for left/right alignment
  - Continuous multiple conversion averaging function
  - Oversampling function
  - Analog watchdog to monitor conversion results
  - The ADC module can be set to stop when not in use
- Analog Input Channel
  - Total of 16 external analog inputs
- Conversion Start Conditions
  - Software setup conversion started
  - Peripheral synchronously trigger the conversion to start
  - External pin trigger the conversion to start
- Conversion Mode
  - 3 scan sequences A, B, C, optionally specifying a single or multiple channels
  - Sequence A single scan
  - Sequence A continuous scan
  - Dual sequence scan, with sequences A and B independently selecting trigger sources, and sequence B having higher priority than A
  - Triple sequence scan, with sequences A, B, and C independently selecting trigger sources, sequence C having higher priority than B, and sequence B having higher priority than A.
- Interrupt and Event Signal Output
  - Sequence A scan end interrupt and event ADC_EOCA
  - Sequence B scan end interrupt and event ADC_EOCB
  - Sequence C scan end interrupt and event ADC_EOCC
  - Analog watchdog 0 compare interrupt and event ADC_CMP0

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- Analog watchdog 1 compare interrupt and event ADC_CMP1
- All the event outputs mentioned above can start DMA

15.3 Functional Description

15.3.1 Function Block Diagram

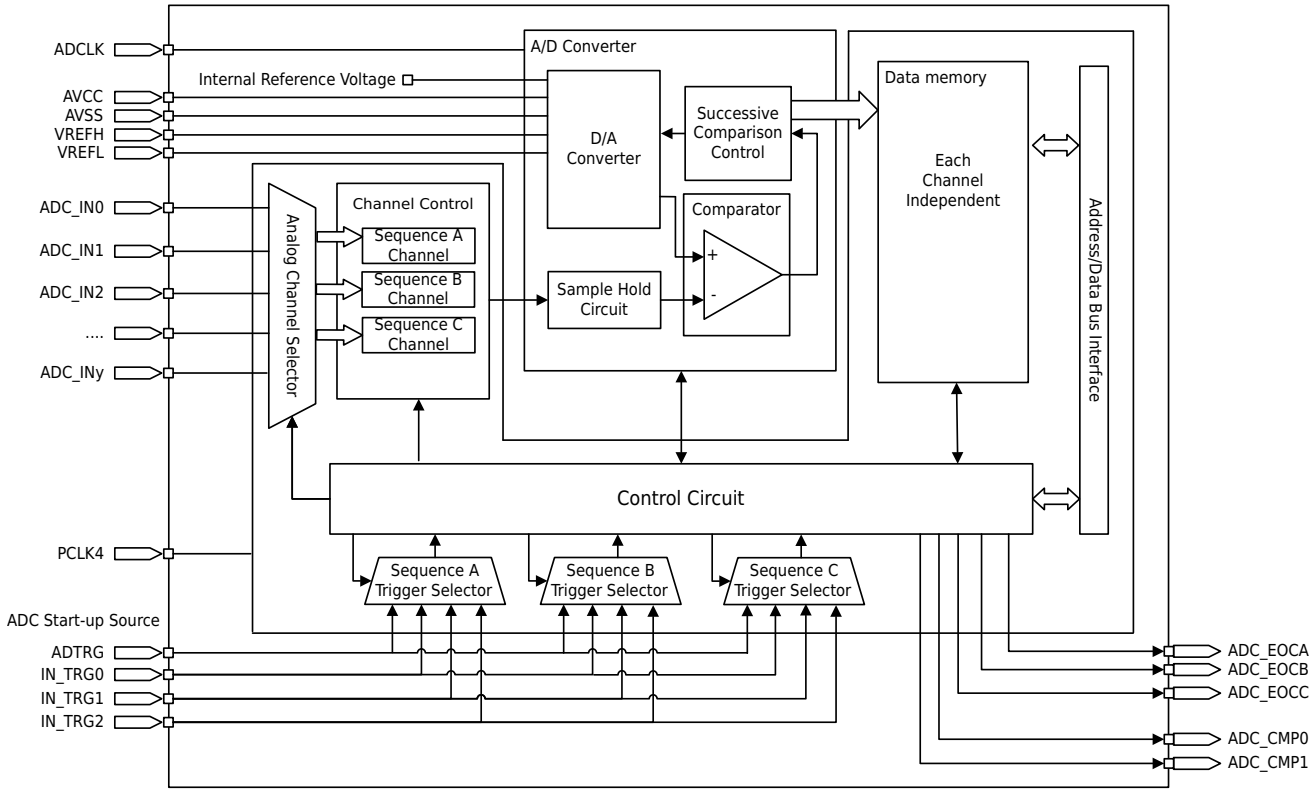

Figure 15-1 ADC Block Diagram

Table 15-1 ADC Input Signal Description

ADC Reference Ground		VREFL
ADC Reference Voltage		Internal Reference Voltage/VREFH
Analog Channel	CH0	ADC_IN0
	CH1	ADC_IN1
	CH2	ADC_IN2
	CH3	ADC_IN3
	CH4	ADC_IN4
	CH5	ADC_IN5
	CH6	ADC_IN6
	CH7	ADC_IN7
	CH8	ADC_IN8
	CH9	ADC_IN9
	CH10	ADC_IN10
	CH11	ADC_IN11

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Analog Channel	CH12	ADC_IN12
	CH13	ADC_IN13
	CH14	ADC_IN14
	CH15	ADC_IN15
Operational Amplifier	OPA1	P: OPA1P; N: OPA1N; O: OPA1O/ADC_IN4;
	OPA2	P: OPA2P; N: OPA2N; O: OPA2O/ADC_IN7;
	OPA3	P: OPA3P; N: OPA3N; O: OPA3O/ADC_IN6;
External Pin Start Trigger Input		ADTRG
Internal Start Trigger Input		IN_TRG0
		IN_TRG1
		IN_TRG2

15.3.2 ADC Clock

The ADC sampling and conversion clock ADCLK source is PCLK4, which can be set to a division factor within the range of 1-8 for PCLK4. When the PCLK4 clock source is selected as PLLQ, ADCLK is the same as PLLQ, maintaining the same frequency.

Notice

The ADCLK frequency should be set within 80MHz.

15.3.3 Channel Selection

The ADC module has multiple channels, which can be configured into three sequences for conversion: Sequence A, Sequence B, and Sequence C. Sequences A, B, and C are equipped with independent channel selection registers: ADC_CHSELRA, ADC_CHSELRB, and ADC_CHSELRC. Each bit in the register represents a channel; for example, writing 1 to Bit0 indicates conversion of CH0, and writing 0 indicates no conversion of CH0. The three sequences can independently select any one or multiple channels for conversion. For example: if ADC_CHSELRA is set to 0x0055 and ADC_CHSELRB is set to 0x0002, then when the trigger condition for Sequence A occurs, channels CH0, CH2, CH4, and CH6 will be converted sequentially. When the trigger condition for Sequence B occurs, channel CH1 will be converted.

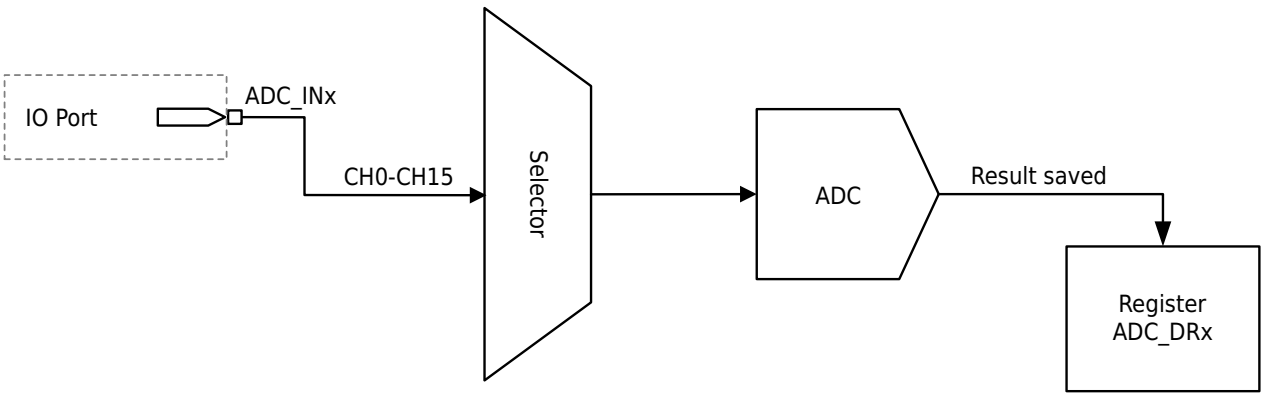

Figure 15-2 Channel Selection

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Notice

Do not select the same channel for sequences A, B, C. For non-existent channels, do not set the corresponding registers and leave them in their reset state.

15.3.4 Trigger Source Selection

Sequences A, B, C independently select trigger sources. The selectable trigger sources include external ports ADTRG and internal events IN_TRG0/1/2. Among them, port ADTRG triggers are active on falling edges. IN_TRG0/1/2 are set by registers ADC_TRGSEL0/1/2, which can select rich event sources inside the chip. Additionally, writing to the ADC_STR register can generate a software trigger signal for sequence A, but can only be used when the ADC is in standby mode. Software triggers are independent of the ADC_TRGSR register.

15.3.5 Sequence A Single Scan Mode

Set ADC_CR0.MS to 0b000 to select sequence A single scan mode.

In this mode, when the trigger condition for sequence A selected by ADC_TRGSR register occurs or ADC_STR.STRT is written to 1 for software trigger, and then the ADC starts, sequentially sampling and converting all channels selected in ADC_CHSELRA. Conversion results are stored in the corresponding data registers ADC_DR. ADC_STR.STRT remains 1 during the ADC conversion process, and is automatically cleared to 0 when all channel conversions are completed, and the ADC enters the conversion standby state, waiting for the next trigger condition to occur.

When all channel conversion ends, the sequence A conversion end flag bit ADC_ISR.EOCAF is set to 1 and the sequence A conversion end event ADC_EOCA is generated, which can be used to start the DMA. If the ADC_ICR.EOCAIEN is 1, the sequence A conversion end interrupt request is generated in the state of interrupt enable.

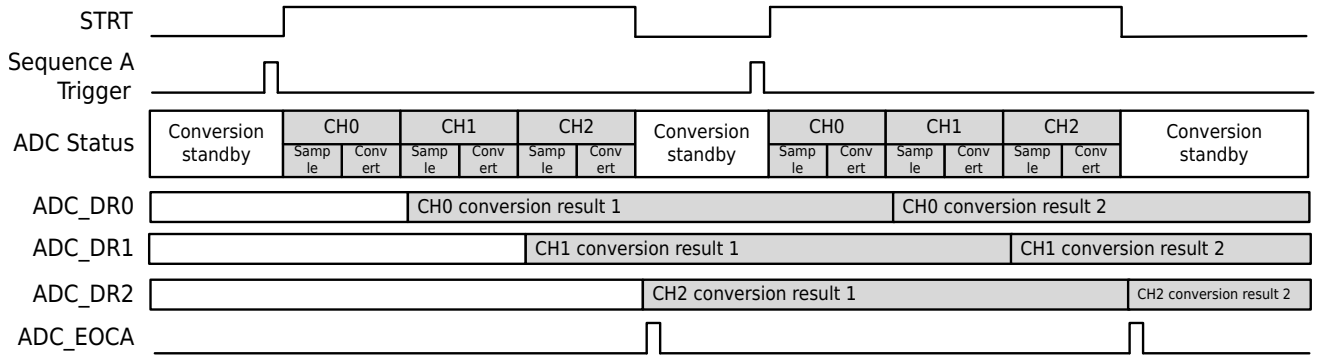

Figure 15-3 Sequence A Single Scan Mode

Software flow for sequence A single scan mode:

Step1. Confirm ADC_STR.STRT is 0, placing the ADC in conversion standby mode;

Step2. Set ADC_CR0.MS to 0b000 to select sequence A single scan mode;

Step3. Set sequence A channel selection register ADC_CHSELRA;

Step4. Set the sampling time register ADC_SSTR;

Step5. Write 1 to ADC_STR.STRT for software trigger of sequence A or set ADC_TRGSR to select the trigger condition for sequence A;

Step6. Poll the sequence A conversion end flag bit EOCAF;

Step7. Read the channel data registers ADC_DR;

Step8. Write 0 to clear the EOCAF flag bit, preparing for the next conversion.

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The CPU query modes in steps 6-8 above can also be replaced by interrupt mode, use the ADC_EOCA interrupt to handle the converted data. Or start DMA read data using the ADC_EOCA event.

15.3.6 Sequence A Continuous Scan Mode

Set ADC_CR0.MS to 0b001 to select sequence A continuous scan mode.

Sequence A continuous scan mode is similar to single scan mode, but after all channels are converted, conversion sequence A is restarted instead of entering standby mode. STRT bits also do not automatically clear 0.

Write 0 to the STRT bit and read STRT to confirm 0 to determine that the ADC enters the conversion standby state when a continuous scan needs to be stopped.

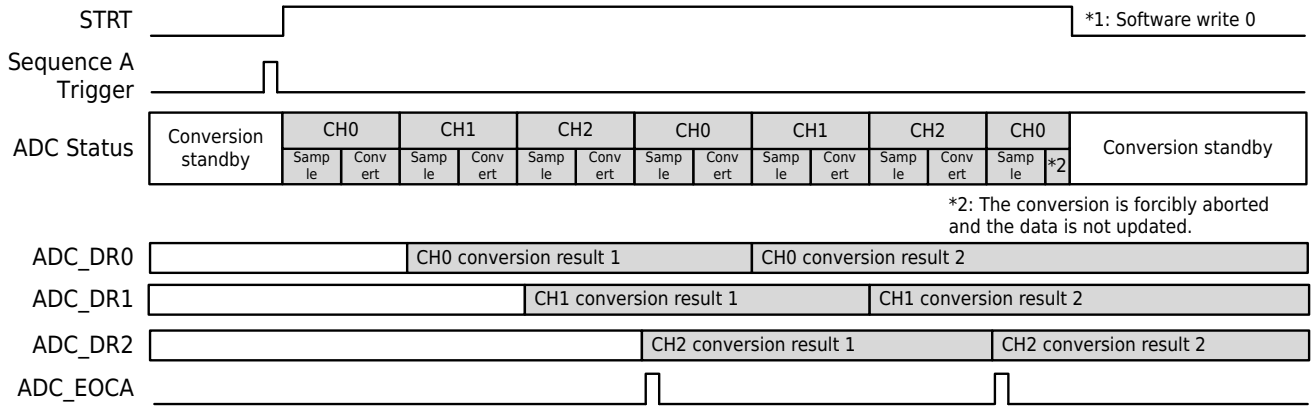

Figure 15-4 Continuous Scan

Software flow for sequence A continuous scan mode:

Step1. Confirm ADC_STR.STRT is 0, placing the ADC in conversion standby mode;

Step2. Set ADC_CR0.MS to 0b001 to select sequence A continuous scan mode;

Step3. Set sequence A channel selection register ADC_CHSELRA;

Step4. Set the sampling time register ADC_SSTR;

Step5. Write 1 to ADC_STR.STRT for software trigger of sequence A or set ADC_TRGSR to select the trigger condition for sequence A;

Step6. Poll the sequence A conversion end flag bit EOCAF;

Step7. Read the channel data registers ADC_DR;

Step8. Write 0 to clear the EOCAF flag for preparation of the next conversion.

Step9. Write 0 to the STRT bit when you do not need to continue the conversion, and read STRT to confirm 0 to determine the ADC is in conversion standby.

The query modes in steps 6-8 can be replaced with interrupt handling, use the ADC_EOCA interrupt to handle the converted data. Or start DMA read data using the ADC_EOCA event.

Notice

Because it is a continuous conversion, the interval between each scan is relatively short, especially when only one channel is selected for conversion. It is recommended to use the ADC_EOCA event to start DMA read data in order to avoid data loss due to intimely processing in query mode.

15.3.7 Dual Sequence Scan Mode

Set ADC_CR0.MS to 0b010 or 0b011 to select dual sequence scan mode, allowing both sequences A and B to be started by their respective trigger conditions.

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When MS=0b010, sequences A and B are equivalent to two independent single scan sequences. MS=0b011, sequence A is continuous scan mode, sequence B is single scan mode.

Sequence A is triggered by ADC_TRGSR.TRGSELA and selects channels with ADC_CHSELRA. Sequence B is triggered by ADC_TRGSR.TRGSELB and selects channels with ADC_CHSELRB.

When the conversion of all channels in sequence A is completed, the sequence A conversion end flag bit ADC_ISR.EOCAF is set to 1 and the sequence A conversion end event ADC_EOCA is generated. If the sequence A conversion end flag bit ADC_ISCR.EOCAIEN is set to 1, the sequence A conversion end interrupt request is generated in the state of interrupted permission. When the conversion of all channels of sequence B ends, the sequence B conversion end flag ADC_ISR.EOCBF is set to 1, and the sequence B conversion end event ADC_EOCB is generated. If ADC_ISCR.EOCBIEN is 1, the interrupt is enabled and the sequence B conversion end interrupt is generated at the same time.

In dual sequence scanning mode, sequence B will be prioritized when sequence A is competing with sequence B, that is, sequence B has higher priority than sequence A. Please refer to the table below for details.

Table 15-2 Various Conflicts Between Sequences A and B

ADC Conversion	Trigger Signal Occurrence	Mode of Treatment	
		ADC_CR1.RSCHSEL=0	ADC_CR1.RSCHSEL=1
During Sequence A Conversion	Sequence A Triggering	Inactive trigger signal	
	Sequence B Triggering	1. Sequence A conversion interrupted. After the interrupted channel completes conversion (data is not updated), sequence B conversion started 2. After Sequence B conversion completes, sequence A continues from interrupted channel	1. Sequence A conversion interrupted. After the interrupted channel completes conversion (data is not updated), sequence B conversion started 2. After Sequence B conversion completes, sequence A restarts from first channel
During Sequence B Conversion	Sequence A Triggering	Sequence B all channel conversion is complete and sequence A conversion is started	
	Sequence B Triggering	Inactive trigger signal	
In AD idle, sequence A and B are triggered simultaneously		Sequence B starts first, after all channel conversions are complete, sequence A conversions are started	

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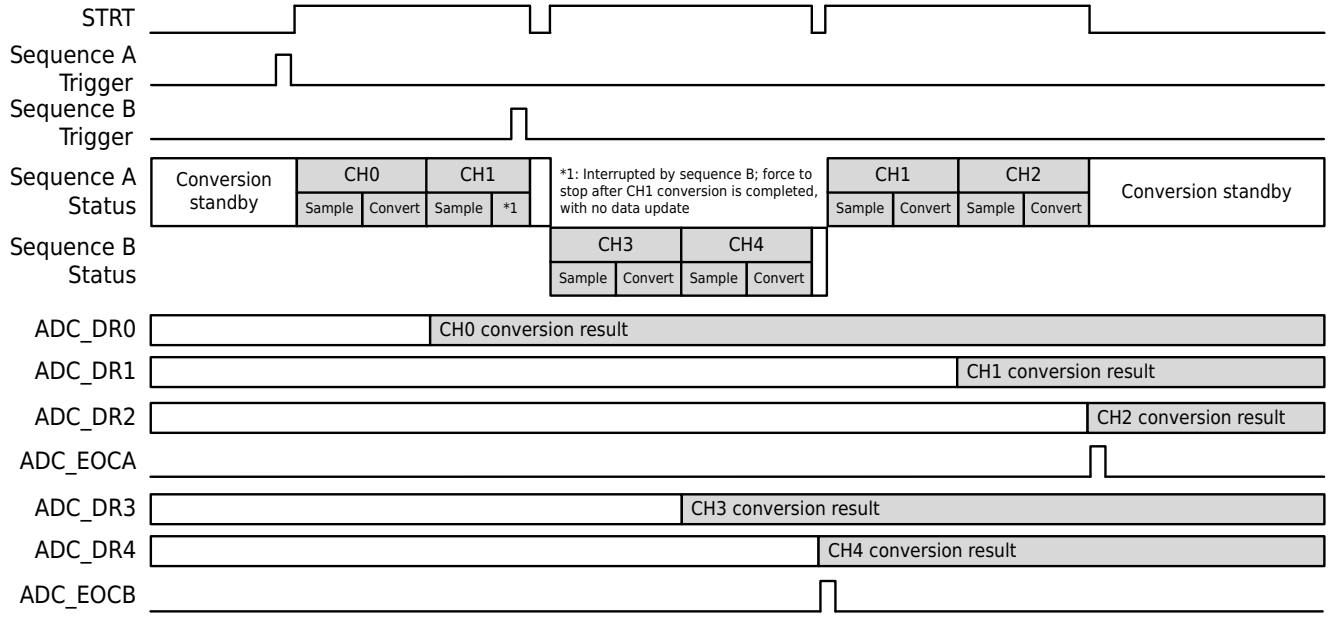

Figure 15-5 Dual Sequence Scan Mode (Sequence A Restarts from Interrupted Channel)

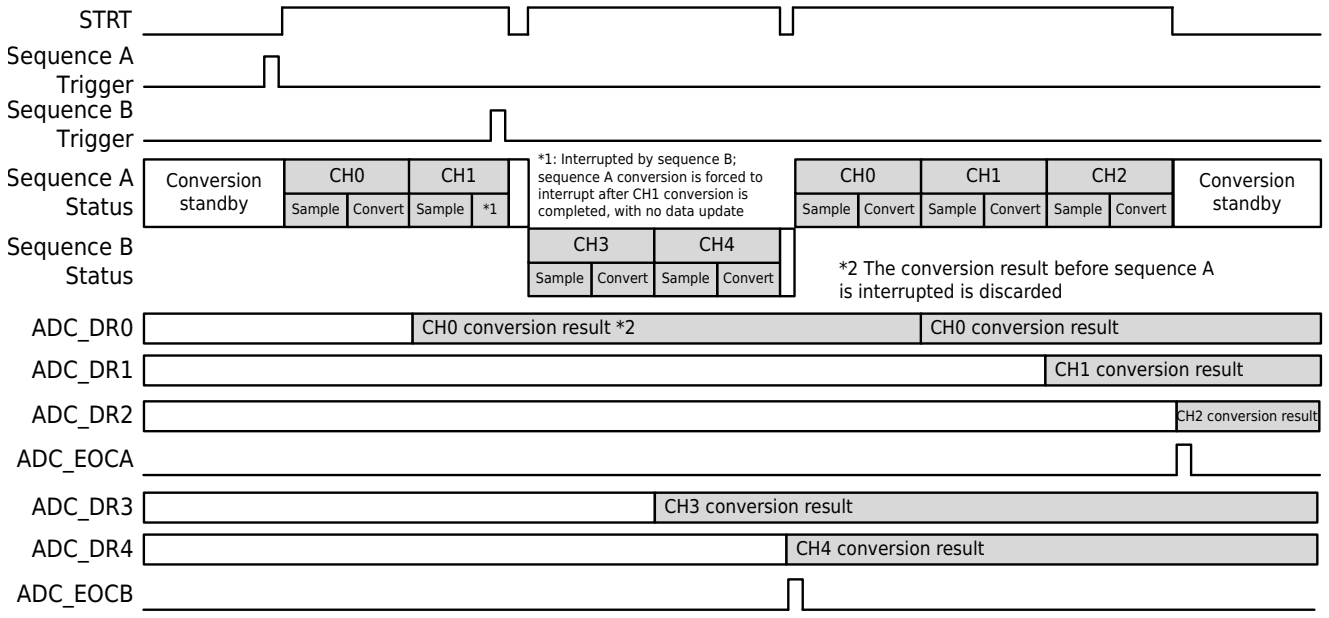

Figure 15-6 Dual Sequence Scan Mode (Sequence A Restarts from First Channel)

Software flow for dual sequence scan mode:

Step1. Confirm ADC_STR.STRT is 0, placing the ADC in standby mode;

Step2. Set ADC_CR0.MS to 0b010 or 0b011 to select dual sequence scan mode;

Step3. Set ADC_CR1.RSCHSEL register to select the startup method after sequence A is interrupted;

Step4. Set sequence A channel selection register ADC_CHSELRA;

Step5. Set sequence B channel selection register ADC_CHSELRB;

Step6. Set the sampling time register ADC_SSTR;

Step7. (Optional) Set ADC_TRGSR register to select the trigger conditions for sequence A;

Step8. Set ADC_TRGSR register to select the trigger conditions for sequence B;

Step9. Handle conversion data after sequence A or B conversion ends by polling EOCAF, EOCBF, using ADC_EOCA, ADC_EOCB interrupts, or initiating DMA.

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Notice

Do not select the same channel for sequences A and B. Do not select the same trigger source for sequences A and B.

15.3.8 Triple Sequence Scan Mode

The ADC control register ADC_CR0.MS is set to 0b110 or 0b111 by selecting the triple sequence scan mode. That is, Sequences A, B, and C can each be started by their respective trigger conditions.

When MS=0b110, Sequences A, B, and C are equivalent to three independent single scan sequences. When MS=0b111, Sequence A is in continuous scan mode, while B and C are in single scan mode.

The trigger source for Sequence A is selected by ADC_TRGSR.TRGSELA, and the conversion channels are selected by ADC_CHSELRA. The trigger source for Sequence B is selected by ADC_TRGSR.TRGSELB, and the conversion channels are selected by ADC_CHSELRB. The trigger source for Sequence C is selected by ADC_TRGSR.TRGSELC, and the conversion channels are selected by ADC_CHSELRC.

When all channels of Sequence A finish conversion, the Sequence A conversion end flag ADC_ISR.EOCAF is set to 1, and the Sequence A conversion end event ADC_EOCA is generated. If ADC_ISCR.EOCAIEN is 1 and interrupts are permitted, a Sequence A conversion end interrupt request is also generated. When all channels of Sequence B finish conversion, the Sequence B conversion end flag ADC_ISR.EOCBF is set to 1, and the Sequence B conversion end event ADC_EOCB is generated. If ADC_ISCR.EOCBIEN is 1 and interrupts are permitted, a Sequence B conversion end interrupt request is also generated. When all channels of Sequence C finish conversion, the Sequence C conversion end flag ADC_ISR.EOCCF is set to 1, and the Sequence C conversion end event ADC_EOCC is generated. If ADC_ISCR.EOCCIEN is 1 and interrupts are permitted, a Sequence C conversion end interrupt request is also generated.

In triple sequence scan mode, when Sequence A, B, and C compete, Sequence C will be processed first, Sequence B will be processed next, and Sequence A will be processed last. That is, Sequence C has higher priority than Sequence B and A, and Sequence B has higher priority than Sequence A. For specific details, please refer to the table below.

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Table 15-3 Various Contention Scenarios for Sequences A and B

ADC Conversion	Trigger Signal Occurrence	Processing Method	
		ADC_CR1.RSCHSEL=0	ADC_CR1.RSCHSEL=1
During Sequence A Conversion	Sequence A trigger	The trigger signal is invalid	
	Sequence B Trigger	1. Sequence A conversion is interrupted. After the interrupted channel completes conversion (data is not updated), Sequence B conversion starts, and ADC_ISR.SASTPDF is set to 1. 2. After Sequence B conversion completes, Sequence A resumes conversion from the interrupted channel.	1. Sequence A conversion is interrupted. After the interrupted channel completes conversion (data is not updated), Sequence B conversion starts, and ADC_ISR.SASTPDF is set to 1. 2. After Sequence B conversion completes, Sequence A restarts conversion from the first channel.
	Sequence C trigger	1. Sequence A conversion is interrupted. After the interrupted channel completes conversion (data is not updated), Sequence C conversion starts, and ADC_ISR.SASTPDF is set to 1. 2. After Sequence C conversion completes, Sequence A resumes conversion from the interrupted channel.	1. Sequence A conversion is interrupted. After the interrupted channel completes conversion (data is not updated), Sequence C conversion starts, and ADC_ISR.SASTPDF is set to 1. 2. After Sequence C conversion completes, Sequence A restarts conversion from the first channel.
During Sequence B Conversion	Sequence A trigger	After all channels of Sequence B complete conversion, Sequence A conversion starts.	
	Sequence B trigger	The trigger signal is invalid	
	Sequence C trigger	1. Sequence B conversion is interrupted. After the interrupted channel completes conversion (data is not updated), Sequence C conversion starts, and ADC_ISR.SBSTPDF is set to 1. 2. After Sequence C conversion completes, Sequence B resumes conversion from the interrupted channel.	1. Sequence B conversion is interrupted. After the interrupted channel completes conversion (data is not updated), Sequence C conversion starts, and ADC_ISR.SBSTPDF is set to 1. 2. After Sequence C conversion completes, Sequence B restarts conversion from the first channel.

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ADC Conversion	Trigger Signal Occurrence	Processing Method	
		ADC_CR1.RSCHSEL=0	ADC_CR1.RSCHSEL=1
During Sequence C Conversion	Sequence A trigger	After all channels of Sequence C complete conversion, Sequence A conversion starts.	
	Sequence B trigger	After all channels of Sequence C complete conversion, Sequence B conversion starts.	
	Sequence C trigger	The trigger signal is invalid	
ADC idle, Sequence A, B, C triggered simultaneously		Sequence C starts first. After all its channels complete conversion, Sequence B conversion starts. After all its channels complete conversion, Sequence A conversion starts.	

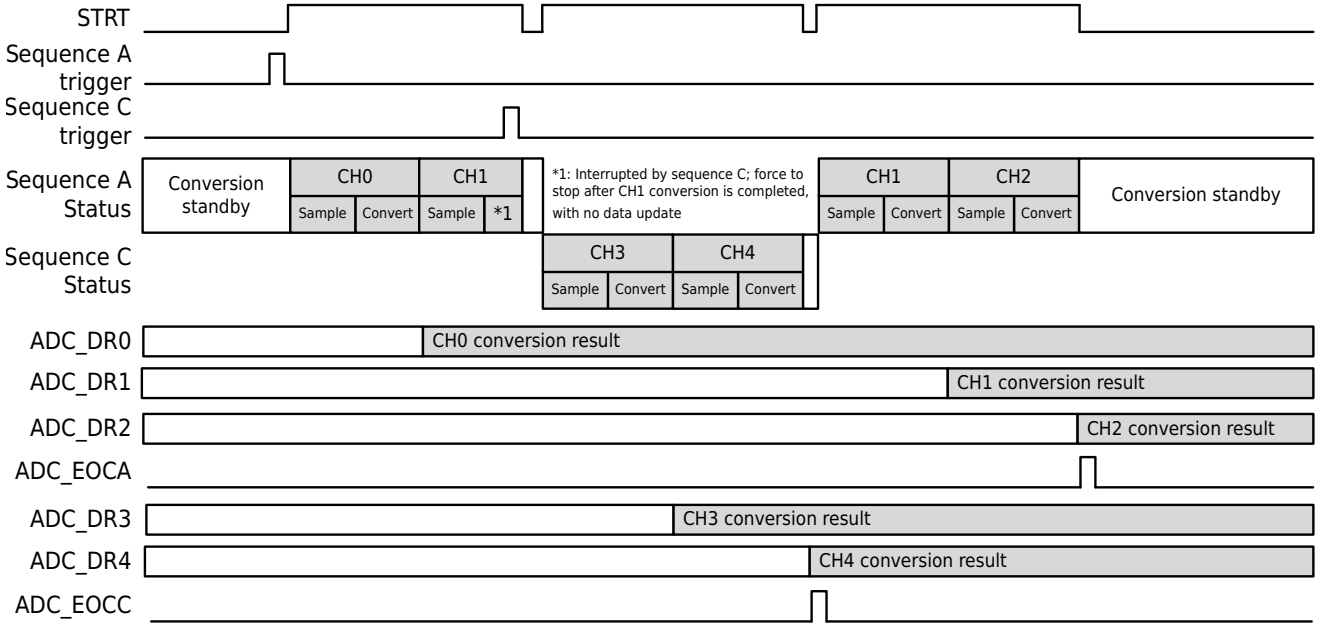

Figure 15-7 Triple Sequence Scan Mode (Sequence A Restarts from Interrupted Channel)

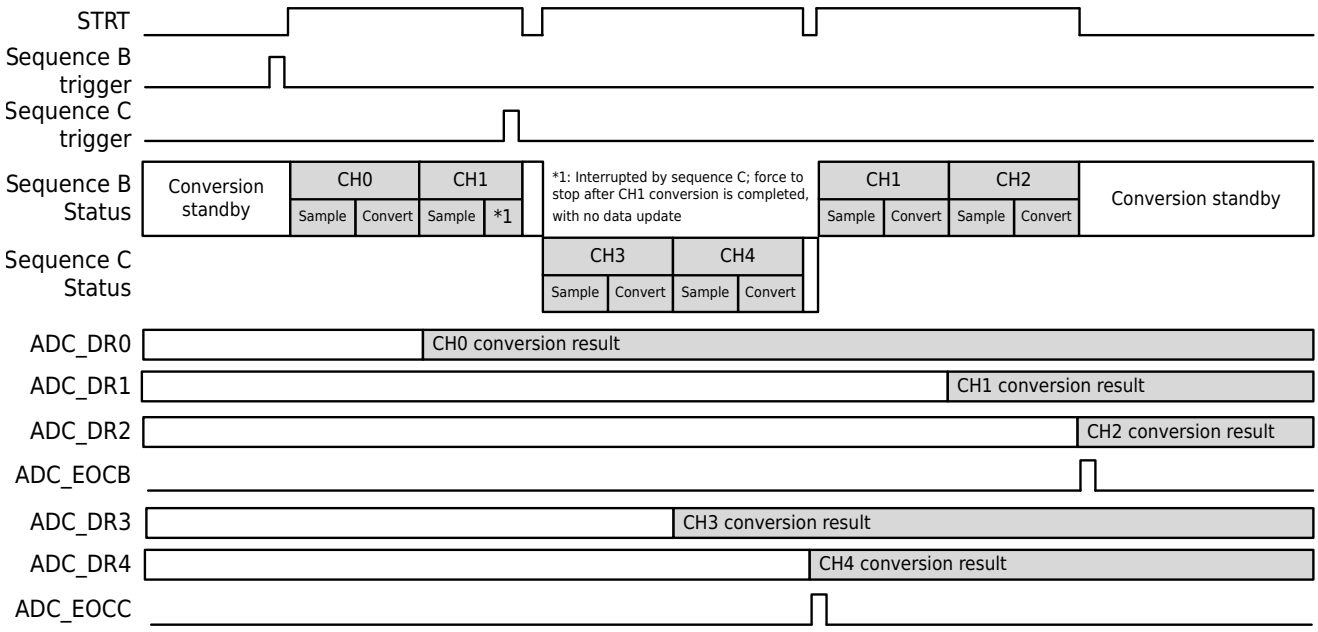

Figure 15-8 Triple Sequence Scan Mode (Sequence B Restarts from Interrupted Channel)

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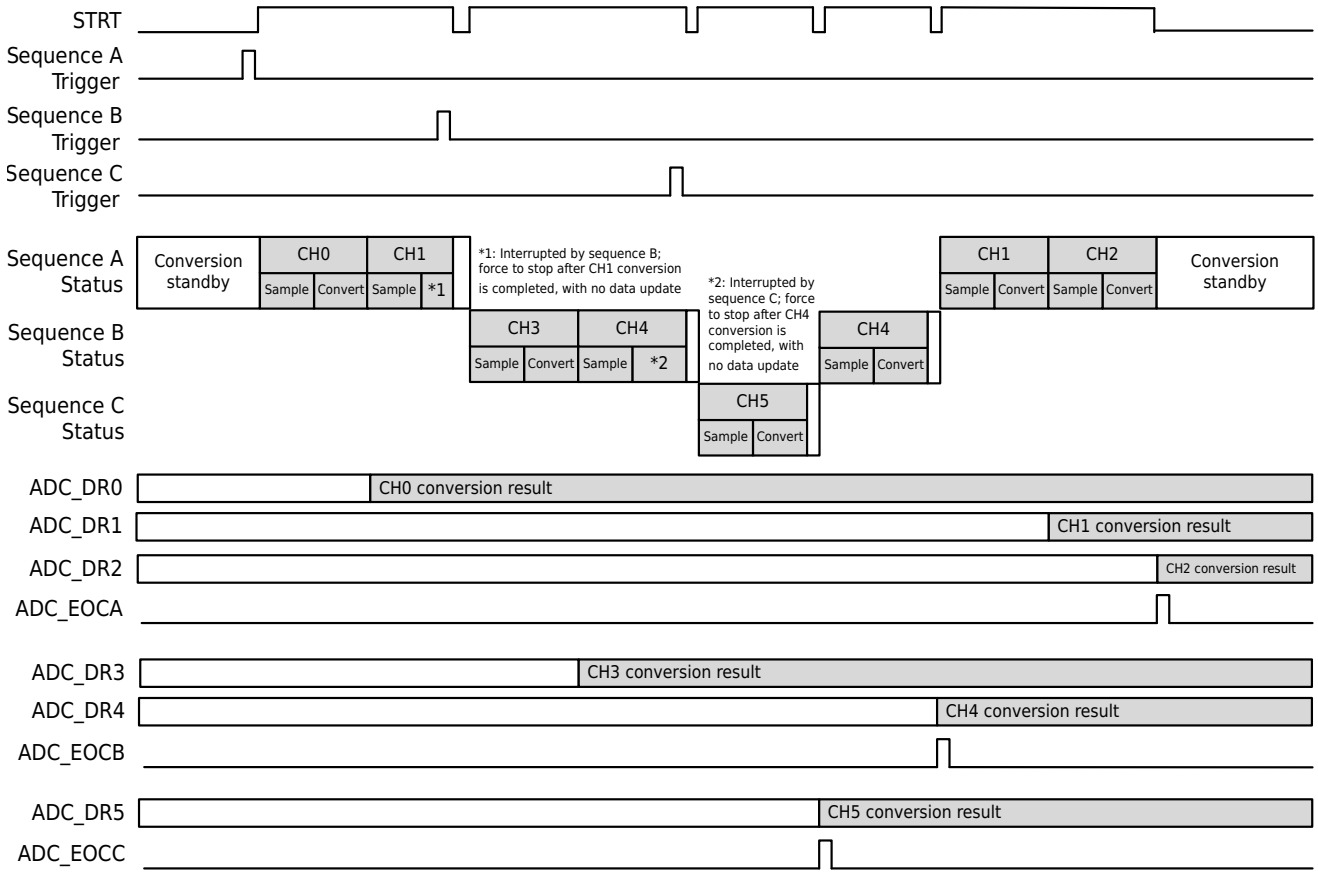

Figure 15-9 Triple Sequence Scan Mode (Sequences A and B Restart from Interrupted Channel)

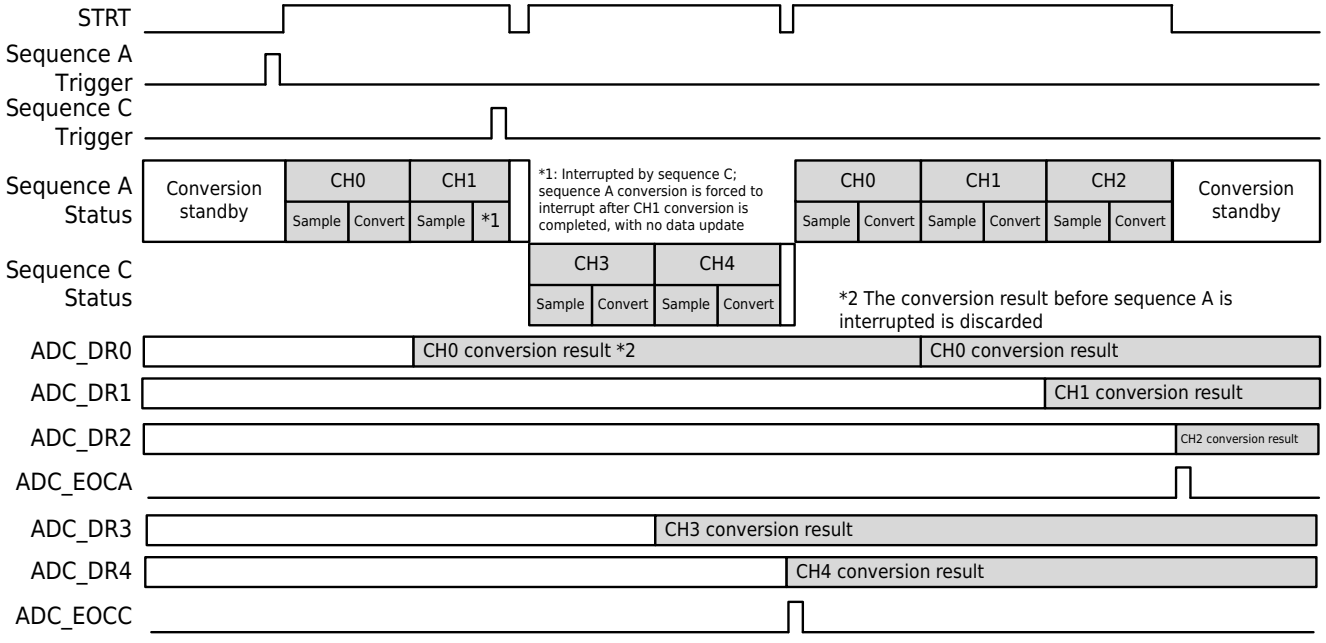

Figure 15-10 Triple Sequence Scan Mode (Sequence A Restarts from First Channel)

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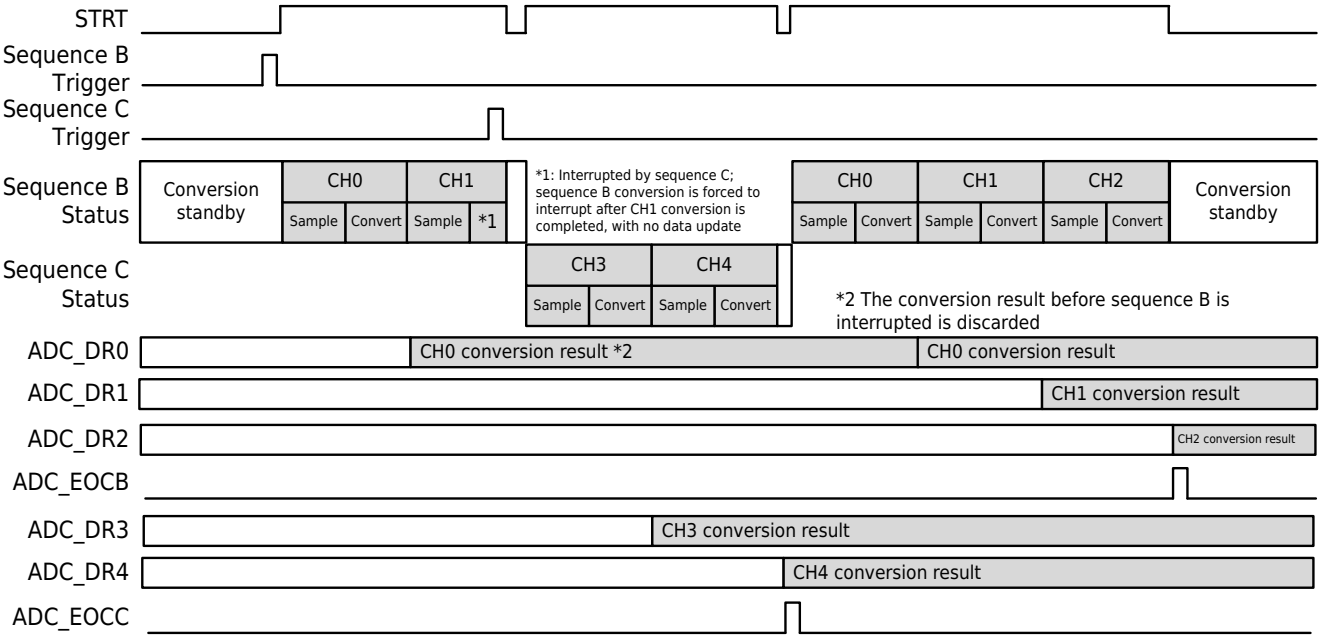

Figure 15-11 Triple Sequence Scan Mode (Sequence B Restarts from First Channel)

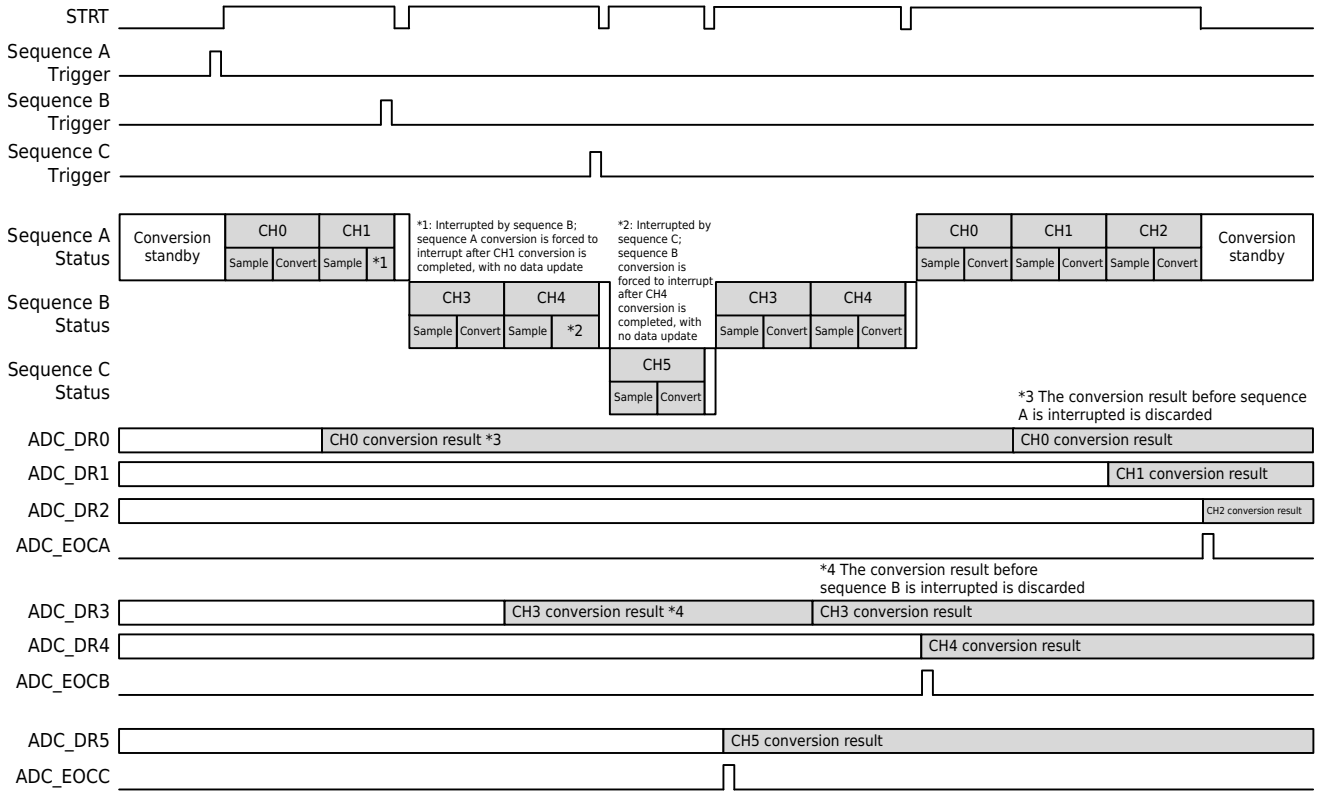

Figure 15-12 Triple Sequence Scan Mode (Sequences A and B Restart from First Channel)

Software workflow in the triple sequence scan mode:

Step1. Confirm ADC_STR.STRT is 0, indicating the ADC is in conversion standby state.

Step2. Set the ADC control register ADC_CR0.MS to 0b110 or 0b111 to select triple sequence scan mode.

Step3. Set register ADC_CR1.RSCHSEL to select the restart method for interrupted Sequence A/B.

Step4. Set Sequence A channel selection register ADC_CHSELRA.

Step5. Set Sequence B channel selection register ADC_CHSELRB.

Step6. Set Sequence C channel selection register ADC_CHSELRC.

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Step7. Set the sampling time register ADC_SSTR.

Step8. (Optional) Set register ADC_TRGSR to select the trigger condition for Sequence A.

Step9. Set register ADC_TRGSR to select the trigger condition for Sequence B.

Step10. Set register ADC_TRGSR to select the trigger condition for Sequence C.

Step11. Process conversion data after Sequence A, B, or C conversion is completed by polling EOCAF, EOCBF, EOCCF, or via ADC_EOCA, ADC_EOCB, ADC_EOCC interrupts, or by starting DMA.

Notice

Do not select the same channel in Sequence A, B, and C. Do not select the same trigger source for Sequence A, B, and C.

15.3.9 Analog Watchdog Function

The analog watchdog function refers to comparing the conversion result at the end of an ADC conversion for a channel. This ADC supports two comparison windows: window 0 and window 1. Taking window 0 as an example, as shown in the figure below, if the conversion result is within the protected area, a watchdog comparison interrupt and event ADC_CMP0 are generated.

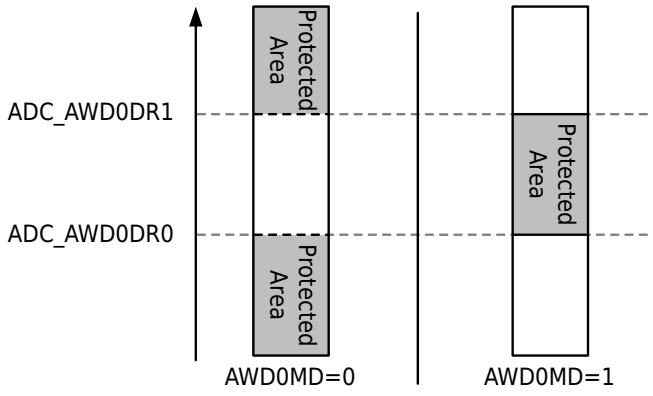

Figure 15-13 Analog Watchdog Protected Area (Comparative Mode)

Software flow for using the analog watchdog function (Taking window 0 as an example) :

Step1. Set the threshold registers AD_AWD0DR0 and ADC_AWD0DR1;

Step2. Set the comparison channel register (ADC_AWD0CHSR) to select the channels to be compared;

Step3. Set ADC_AWDCR.AWD0MD to select the comparative mode;

Step4. Set ADC_AWDCR.AWD0IEN interrupt permission bit;

Step5. Set ADC_AWDCR.AWD0EN to enable the watchdog window 0 comparison function;

Step6. Set the scan mode according to the previous steps and start the ADC conversion;

Step7. In the ADC_CMP0 interrupt or after ADC conversion ends, query the comparison status register (ADC_AWDSR.AWD0F) and process the comparison result accordingly.

The usage of comparison window 1 is the same as window 0.

Two comparison windows can be used in combination. When the window combination function is enabled, at the end of the conversion for the channel selected in window 1, the comparison interrupt ADC_CMP1 outputs not just the comparison result from window 1 alone, but a combined result of logical OR, AND, or XOR of the comparison results from windows 0 and 1, as set.

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The software flow for using the window combination comparison function is similar to using the windows individually. After setting up windows 0 and 1, additionally set the ADC_AWDCR.AWDCM register to select the combination method.

15.3.10 Sampling Time and Conversion Time for Analog Inputs

In single scan mode, ADC conversion can be started by software settings, internal triggers IN_TRG0/1/2, and external pin triggers ADTRG startup mode. After the scan conversion delay time t_D, the ADC module starts to sample and convert the analog channel. After all the conversions are completed, the conversion end delay time t_{ED} enters the standby state, and a scan is finally completed. The continuous scanning mode is similar to a single scanning mode, except that there is no t_D time at the second time of the sequence and at the start of the sequence.

The conversion time of a single channel is $t_{CONV}=t_{SPL}+t_{CMP}$. Among them, t_{SPL} represents the sampling time of the analog input, and the number of sampling periods can be adjusted according to the input impedance setting register ADC_SSTR. t_{CMP} represents the successive comparison time, 14 ADCLK for 12-bit precision.

The time of one scan conversion $t_{SCAN} = t_D + \sum t_{CONV} + t_{ED}$. Among them, $\sum t_{CONV}$ represents the sum of the conversion time of all scanning channels. Since the sampling time t_{SPL}can be set independently, the conversion time t_{CONV} of each channel can be different.

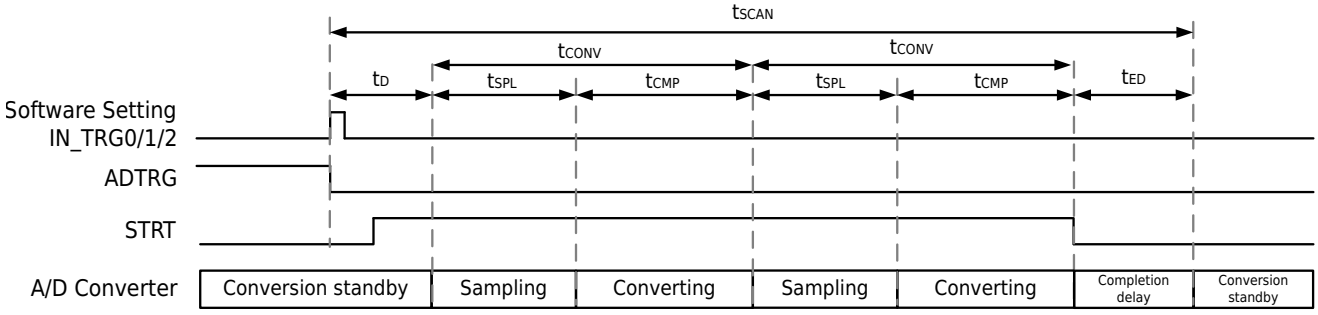

Figure 15-14 ADC Conversion Time Diagram

Table 15-4 ADC Conversion Time

Name		Description		Conditions			
				Synchronous Peripheral Trigger	Asynchronous Peripheral Trigger(1)	External Pin Trigger	Software Trigger
t_D		Scan start processing time	ADC is idle, start conversion	4 ADCLK	3 PCLK4 + 4 ADCLK + 1 PCLK4_SYNC	2 PCLK4 + 4 ADCLK	3 ADCLK
			Sequence A conversion interrupted, start sequence B conversion	After completing this conversion	After completing this conversion	After completing this conversion	-
t_{CONV}	t_{SPL}	Sample time		ADC_SSTRx.SST x ADCLK			
	t_{CMP}	Successive conversion time	12-bit resolution	14 ADCLK			
t_{ED}		Scan completion processing time		3 ADCLK			
t_{TD}		Minimum continuous trigger interval		$\sum t_{CONV}$ + 6 ADCLK			

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Note

1. Asynchronous peripheral trigger refers to the scenario of peripheral triggering when the PCLK4 clock source is PLLQ (with ADCLK having the same frequency as PLLQ). In this case, the peripheral module clock and the ADC module clock have an asynchronous relationship. PCLK4_SYNC represents the system clock after being divided by CMU_SCFGR.PCLK4S.

15.3.11 ADC Data Register Automatic Clear Function

When ADC_CR0.CLREN is 1, the ADC_DR register will be automatically cleared to 0x0000 after being read by the CPU or DMA.

Using this function allows detection of whether the ADC_DR register has been updated. Examples are provided below.

- When ADC_CR0.CLREN is 0, automatic clear function disabled, if the analog quantity to be measured (0x0222) is not converted for some reason or the result is not updated to the ADC_DR register, the ADC_DR register will continue to hold the previous conversion value (0x0111). During ADC conversion completion interrupt handling, the not updated value (0x0111) will be read. To detect whether the ADC conversion value is enabled, it is necessary to additionally store the previous conversion value in RAM and judge by comparing the conversion results.
- When ADC_CR0.CLREN is 1, automatic clear function enabled, after the previous conversion result (0x0111) is read by the CPU or DMA, the ADC_DR register will be automatically cleared to 0x0000. After subsequent ADC conversions, if the conversion result is not correctly transferred to the ADC_DR register, the ADC_DR register will remain at 0x0000. In this case, if 0x0000 is read during interrupt handling, it is easy to determine whether the ADC conversion data has been stored correctly.

15.3.12 Conversion Data Averaging Function

The ADC conversion averaging function refers to performing 2, 4, 8, 16, 32, 64, 128, or 256 consecutive conversions on the same channel and averaging the conversion results before storing them in the data register. Using the averaging function can remove certain noise components and make the conversion results more precise.

The register ADC_CR0.AVCNT sets the number of consecutive conversions, and the register ADC_AVCHSELR selects any one or more channels to be averaged.

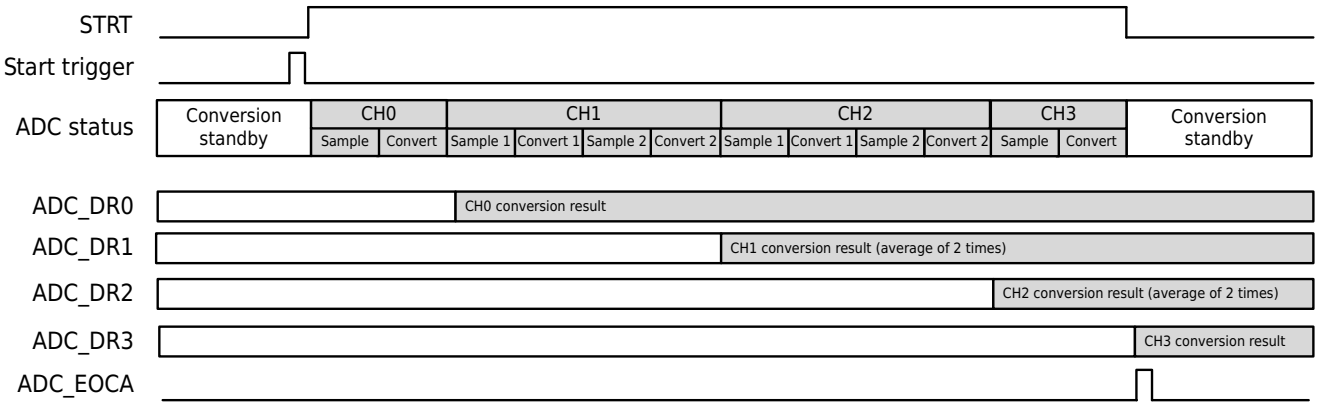

Figure 15-15 Conversion Action When Averaging Function is Enabled

In the diagram above, in sequence A single scan mode, 4 channels CH0-3 are selected for conversion, with CH1 and CH2 set to twice averaging mode. During the scanning process, CH1 and 2 will perform

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two consecutive conversions, and save the averaged results to the data registers ADC_DR1 and 2 of the corresponding channel.

15.3.13 Oversampling

By setting ADC_CR2.OVSMOD to 1 and selecting any one or more channels for oversampling through setting ADC_AVCHSELR, the AD enters oversampling mode. In this mode, multiple consecutive sampling conversions and result shifting are performed to obtain a 16-bit precision conversion result. The final conversion result is calculated using the following formula:

$$\text{AD oversampling result} = \frac{1}{2^M} \times \sum_{n=1}^{n=N} \text{AD conversion result of the nth time} \quad (2^M \le N)$$

Among them:

- The sample rate N is set through ADC_CR0.AVCNT and can be set to 2 to 256 samples.
- The divisor series M is set through ADC_CR2.OVSS and can be set to shift right by up to 8 bits.

15.3.14 Operational Amplifier (OPA)

This product is equipped with 3 operational amplifiers (OPA). Each OPA can be enabled by setting the ADC_OPACR.OPAxEN bit and can operate independently.

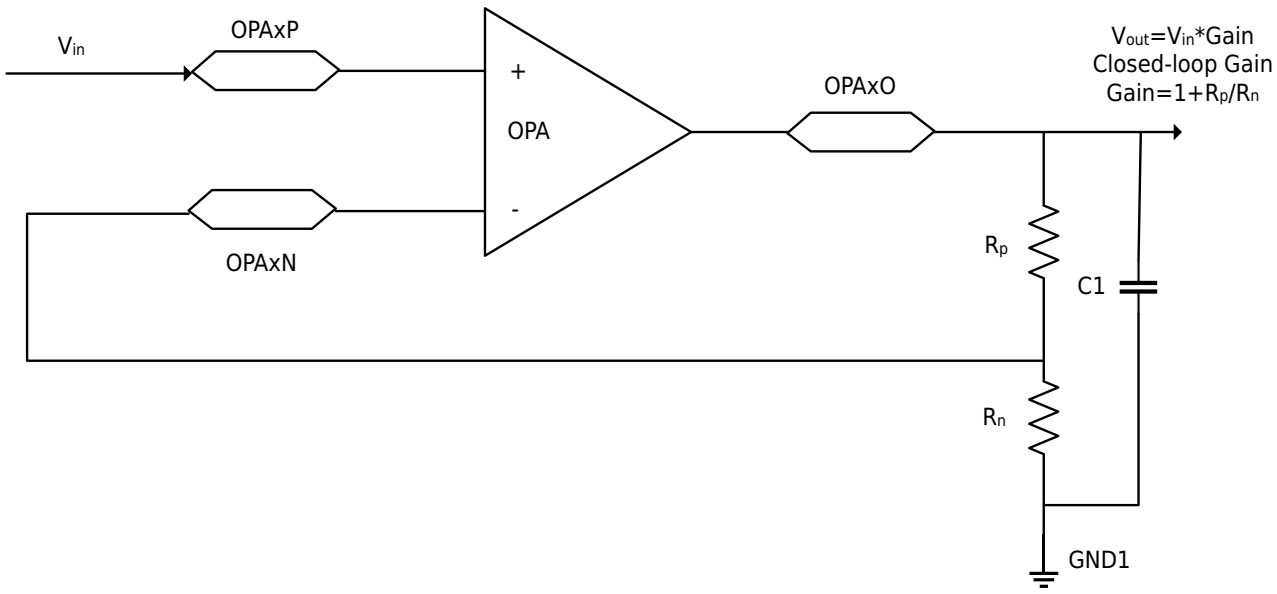

Figure 15-16 OPA Operation Diagram

The OPA can be used in combination with the ADC and CMP. As shown in the following figure, the OPA output pin OPAxO is multiplexed with the analog channel pins of the ADC/CMP, allowing the OPA output to be used for ADC conversion or voltage comparison.

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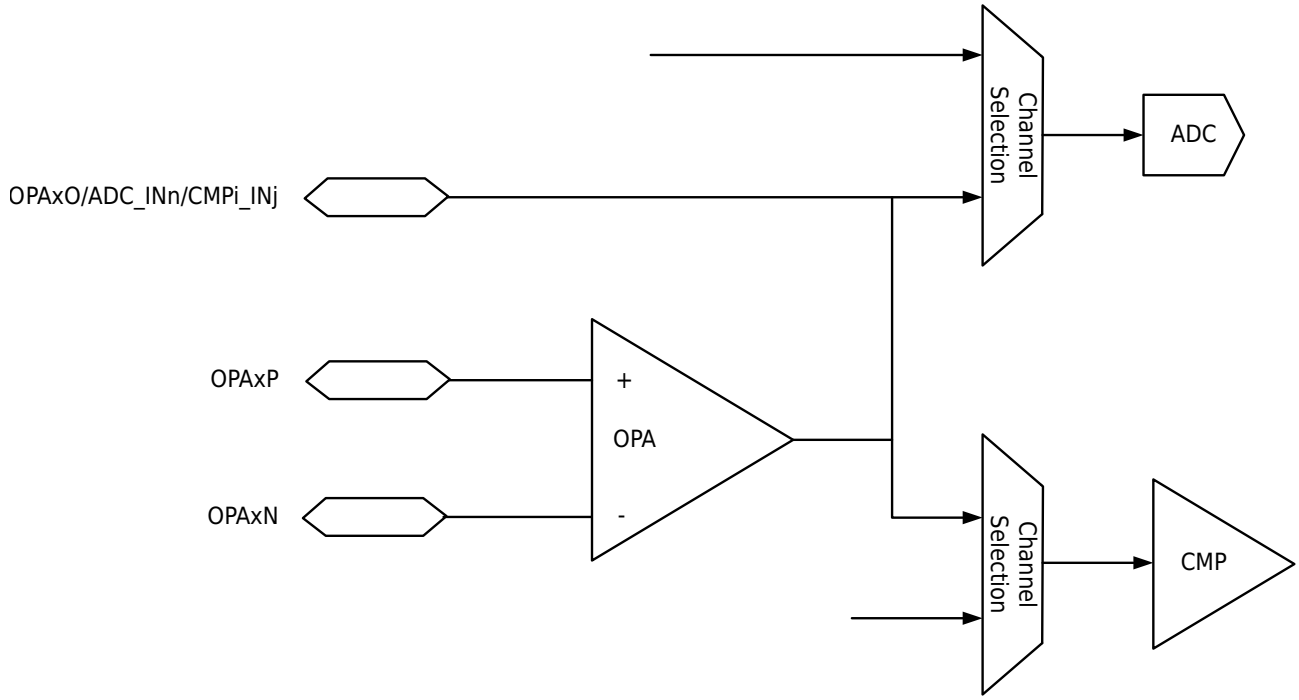

Figure 15-17 Diagram of Combining OPA with ADC/CMP

15.3.15 Interrupt and Events

The ADC block can generate the following kinds of event outputs. When each event occurs, if the corresponding interrupt enable register is set to active, an interrupt request is simultaneously output.

- For sequence A scan end ADC_EOCA, corresponding to interrupt enable register ADC_ICR.EOCAIEN
- For sequence B scan end ADC_EOCB, corresponding to interrupt enable register ADC_ICR.EOCBIEN
- For sequence C scan end ADC_EOCC, corresponding to interrupt enable register ADC_ICR.EOCCIEN
- For analog watchdog window 0 compare ADC_CMP0, corresponding interrupt enable register ADC_AWDCR.AWD0IEN
- For analog watchdog window 1 compare ADC_CMP1, corresponding interrupt enable register ADC_AWDCR.AWD1IEN

The above all event outputs can initiate other on-chip peripheral modules, including starting DMA transfer. Using DMA transfer allows continuous reading of ADC conversion results without software intervention, fully implemented by hardware, reducing CPU load. DMA settings are described in the relevant sections of the "DMA Controller (DMA) " chapter. Event signal output is independent of the interrupt enable bit control, and will be output as long as the condition occurs.

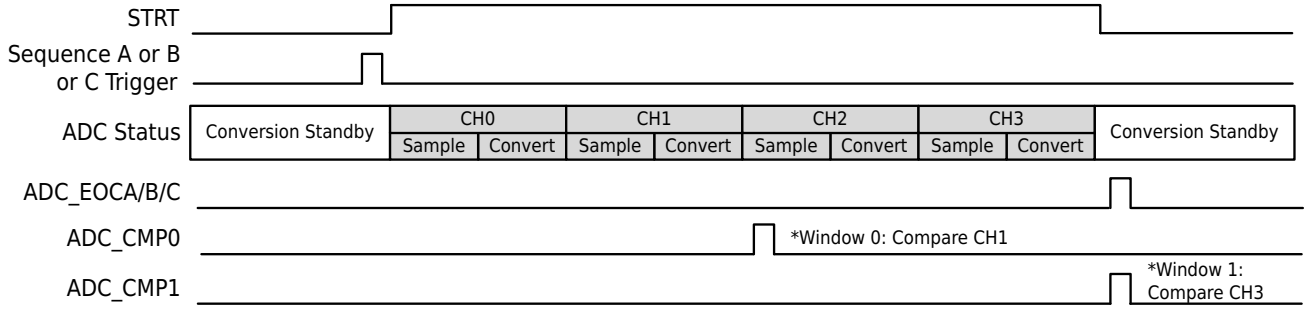

Figure 15-18 ADC Interrupt and Event Output Timing

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15.4 Register Description

15.4.1 Register List

Base Address: 0x40030000

Table 15-5 Analog-to-Digital Converter (ADC) Register Offset

Offset	Register	Description	Width
0x00	ADC_STR	ADC Start Register	8
0x02	ADC_CR0	ADC Control Register 0	16
0x04	ADC_CR1	ADC Control Register 1	16
0x06	ADC_CR2	ADC Control Register 2	16
0x0C	ADC_CHSELRA	ADC Sequence A Channel Select Register	32
0x10	ADC_CHSELRB	ADC Sequence B Channel Select Register	32
0x14	ADC_AVCHSELR	ADC Average Channel Select Register	32
0x1C	ADC_TRGSR	ADC Trigger Select Register	32
0x20+0x1*x	ADC_SSTRx	ADC Channel x Sampling Time Register (x=0-15)	8
0x40	ADC_CHSELRC	ADC Sequence C Channel Select Register	32
0x44	ADC_ISR	ADC Interrupt Flag Register	8
0x45	ADC_ICR	ADC Interrupt Enable Register	8
0x46	ADC_ISCLRR	ADC Interrupt Flag Clear Register	8
0x50+0x2*x	ADC_DRx	ADC Channel x Convert Data Register (x=0-15)	16
0xA0	ADC_AWDCR	ADC Analog Watchdog Control Register	16
0xA2	ADC_AWDSR	ADC Analog Watchdog Status Register	8
0xA3	ADC_AWDSCLRR	ADC Analog Watchdog Status Clear Register	8
0xA4+0x8*x+0x2*y	ADC_AWDxDRy	ADC Analog Watchdog x Compare Data Register y (x=0-1, y=0-1)	16
0xA8+0x8*x	ADC_AWDxCHSR	ADC Analog Watchdog x Channel Select Register (x=0-1)	8
0xC0	ADC_OPACR	OPA Control Register	32

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15.4.2 ADC Start Register (ADC_STR)

Offset	Bit Position							
0x00	7	6	5	4	3	2	1	0
Reset	0x00							
Name	Reserved							STRT
Access								RW

Bit	Name	Functional Description	Access
7:1	*Reserved*	-	-
0	STRT	ADC Conversion Start ● 0b0: Stop conversion ● 0b1: Start conversion Set Conditions: 1. Software setting 2. The selected trigger condition occurs 3. During ADC conversion Clear Conditions: 1. Software clearing 0 2. Automatically clears to 0 after conversion ends **Note** ● Writing 1 to STRT when STRT is 0 (ADC idle) generates a software trigger to start sequence A. ● Writing 1 to STRT has no effect when STRT is 1 (ADC active). ● Writing 0 to STRT when STRT is 1 forces the ADC conversion to stop. If the ADC_TRGSR sets a value other than 0x0 and does not want the ADC to restart, set the ADC_TRGSR to 0 before writing 0 to the STRT. ● Write 0 has no effect when STRT is 0.	RW

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15.4.3 ADC Control Register 0 (ADC_CR0)

Note

Please set this register when ADC_STR.STRT is 0.

Offset	Bit Position															
0x02	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0800															
Name	Reserved						AVCNT		DFMT	CLREN	Reserved			MS		
Access							RW		RW	RW				RW		

Bit	Name	Functional Description	Access
15:11	*Reserved*	-	-
10:8	AVCNT	Number Selection ● 0b000: Average of 2 consecutive conversions ● 0b001: Average of 4 consecutive conversions ● 0b010: Average of 8 consecutive conversions ● 0b011: Average of 16 consecutive conversions ● 0b100: Average of 32 consecutive conversions ● 0b101: Average of 64 consecutive conversions ● 0b110: Average of 128 consecutive conversions ● 0b111: Average of 256 consecutive conversions	RW
7	DFMT	Data Format ● 0b0: Right-align conversion data ● 0b1: Left-align conversion data **Note** This bit setting has no effect in oversampling mode.	RW
6	CLREN	Data Register Automatic Clear ● 0b0: Disable automatic clear ● 0b1: Enable automatic clear **Note** When the CLREN bit is set, the ADC_DRx register will be automatically cleared after being read by the CPU, DMA, etc. The automatic clear function is mainly used to detect whether the data register has been updated.	RW
5:3	*Reserved*	-	-

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Bit	Name	Functional Description	Access
2:0	MS	Mode Selection ● 0b000: Sequence A single scan mode, sequence B is invalid ● 0b001: Sequence A continuous scan mode, sequence B is invalid ● 0b010: Sequence A single scan mode, sequence B single scan mode ● 0b011: Sequence A continuous scan mode, sequence B single scan mode ● 0b110: Sequence A single scan mode, sequence B and sequence C single scan mode ● 0b111: Sequence A continuous scan mode, sequence B and sequence C single scan mode ● Others: Setting prohibited	RW

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15.4.4 ADC Control Register 1 (ADC_CR1)

Note

Please set this register when ADC_STR.STRT is 0.

Offset	Bit Position															
0x04	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00C0															
Name	Reserved								SREF		Reserved			RSCHSEL	Reserved	
Access									RW					RW		

Bit	Name	Functional Description	Access
15:8	*Reserved*	-	-
7:6	SREF	ADC Positive Reference Voltage Selection ● 0b00: Internal 2.5V reference voltage ● 0b01: Internal 4.2V reference voltage ● 0b10: External reference voltage VREFH ● 0b11: AVCC	RW
5:3	*Reserved*	-	-
2	RSCHSEL	Sequence A, B Restart Channel Selection ● 0b0: After being interrupted by a higher-priority sequence, when the lower-priority sequence restarts, it resumes scanning from the interrupted channel ● 0b1: After being interrupted by a higher-priority sequence, when the lower-priority sequence restarts, it starts scanning anew from the first channel.	RW
1:0	*Reserved*	-	-

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15.4.5 ADC Control Register 2 (ADC_CR2)

Note

Please set this register when ADC_STR.STRT is 0.

Offset	Bit Position															
0x06	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved			OVSMOD	OVSS				Reserved							
Access				RW	RW											

Bit	Name	Functional Description	Access
15:13	*Reserved*	-	-
12	OVSMOD	Oversampling Mode ● 0b0: Normal mode ● 0b1: Oversampling mode	RW
11:8	OVSS	Shift Selection ● 0b0000: No shift ● 0b0001: Shift right by 1 bit ● 0b0010: Shift right by 2 bit ● 0b0011: Shift right by 3 bit ● 0b0100: Shift right by 4 bit ● 0b0101: Shift right by 5 bit ● 0b0110: Shift right by 6 bit ● 0b0111: Shift right by 7 bit ● 0b1000: Shift right by 8 bit ● Others: Setting prohibited **Note** This bit setting has no effect when OVSMOD=0 (normal mode).	RW
7:0	*Reserved*	-	-

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15.4.6 ADC Sequence A Channel Select Register (ADC_CHSELRA)

Note

Please set this register when ADC_STR.STRT is 0.

Offset	Bit Position																													
0x0C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	CHSELA																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	CHSELA	Conversion Channel Selection For sequence A channel selection, each bit represents a channel. CHSELA[x] represents channel CHx, and any combination can be selected. ● 0b0: Corresponding channel is not selected ● 0b1: Corresponding channel is selected **Notice** Please do not select the same channel for both sequences A, B, and C. ADC supports channels 0-15. Unsupported channels need to be set to 0.	RW

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15.4.7 ADC Sequence B Channel Select Register (ADC_CHSELRB)

Note

Please set this register when ADC_STR.STRT is 0.

Offset	Bit Position																													
0x10	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	CHSELB																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	CHSELB	Conversion Channel Selection For sequence B channel selection, each bit represents a channel. CHSELB[x] represents channel CHx, and any combination can be selected. ● 0b0: Corresponding channel is not selected ● 0b1: Corresponding channel is selected **Notice** This is only valid in dual sequence or three sequences scan mode. Please do not select the same channel for both sequences A, B, and C. ADC supports channels 0-15. Unsupported channels need to be set to 0.	RW

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15.4.8 ADC Average Channel Select Register (ADC_AVCHSELR)

Note

Please set this register when ADC_STR.STRT is 0.

Offset	Bit Position																													
0x14	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	AVCHSEL																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	AVCHSEL	Average Channel Selection Each bit represents a channel, AVCHSEL[x] represents channel CHx, and any combination can be selected. ● 0b0: Corresponding channel is not selected ● 0b1: Corresponding channel is selected **Notice** When AVCHSEL and the corresponding channel in ADC_CHSELRA or ADC_CHSELRB or ADC_CHSELRC are selected simultaneously, that channel will continuously perform the set number of ADC conversions during scanning, and the conversion results will be averaged and updated into the data register. If the corresponding AVCHSEL channel is not set, the channel will perform a single conversion. ADC supports channels 0-15. Unsupported channels need to be set to 0.	RW

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15.4.9 ADC Trigger Select Register (ADC_TRGSR)

Note

Please set this register when ADC_STR.STRT is 0.

Offset	Bit Position																													
0x1C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved								TRGENC	Reserved				TRGSELC			TRGENB	Reserved				TRGSELB			TRGENA	Reserved				TRGSELA		
Access									RW					RW			RW					RW			RW					RW		

Bit	Name	Functional Description	Access
31:24	*Reserved*	-	-
23	TRGENC	Sequence C Trigger Enabled ● 0b0: Disable sequence C internal or external pin trigger ● 0b1: Enable sequence C internal or external pin trigger **Note** This is only valid in sequence C active mode and invalid in other modes. External pin trigger is selected as active. If ADTRG transitions from "High" to "Low", a falling edge is detected, and the scan conversion starts. Please keep "Low" for at least 1.5*PCLK4 periods.	RW
22:19	*Reserved*	-	-
18:16	TRGSELC	Sequence C Trigger Condition Selection In sequence C active mode (ADC_CR0.MS[2:1]=0b11), as the trigger condition for sequence C. Three sequences scan: ● 0b000: ADTRG ● 0b001: IN_TRG0 ● 0b010: IN_TRG1 ● 0b011: IN_TRG0 +IN_TRG1 ● 0b100: IN_TRG2 ● 0b101: IN_TRG0 +IN_TRG2 ● 0b110: IN_TRG1 +IN_TRG2 ● 0b111: IN_TRG0 +IN_TRG1 +IN_TRG2 **Note** This is only valid in sequence C active mode and invalid in other modes. The interval between two triggers must be greater than or equal to the scan period t_{SCAN}, and if less, the trigger is disabled.	RW

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Bit	Name	Functional Description	Access
15	TRGENB	Sequence B Trigger Enabled ● 0b0: Disable sequence B internal or external pin trigger ● 0b1: Enable sequence B internal or external pin trigger **Note** External pin trigger is selected as active. If ADTRG transitions from "High" to "Low", a falling edge is detected, and the scan conversion starts. Please keep "Low" for at least 1.5*PCLK4 periods.	RW
14:11	*Reserved*	-	-
10:8	TRGSELB	Sequence B Trigger Condition Selection In sequence B active mode (ADC_CR0.MS[1]=1), as the trigger condition for sequence B. Non-three sequences scan: ● 0bx00: ADTRG ● 0bx01: IN_TRG0 ● 0bx10: IN_TRG1 ● 0bx11: IN_TRG0 +IN_TRG1 Three sequences scan: ● 0b000: ADTRG ● 0b001: IN_TRG0 ● 0b010: IN_TRG1 ● 0b011: IN_TRG0 +IN_TRG1 ● 0b100: IN_TRG2 ● 0b101: IN_TRG0 +IN_TRG2 ● 0b110: IN_TRG1 +IN_TRG2 ● 0b111: IN_TRG0 +IN_TRG1 +IN_TRG2 **Note** This is only valid in sequence B active mode and invalid in other modes. The interval between two triggers must be greater than or equal to the scan period t_{SCAN}, and if less, the trigger is disabled.	RW
7	TRGENA	Sequence A Trigger Enabled ● 0b0: Disable sequence A internal or external pin trigger ● 0b1: Enable sequence A internal or external pin trigger **Note** External pin trigger is selected as active. If ADTRG transitions from "High" to "Low", a falling edge is detected, and the scan conversion starts. Please keep "Low" for at least 1.5*PCLK4 periods.	RW
6:3	*Reserved*	-	-
2:0	TRGSELA	Sequence A Trigger Condition Selection Trigger conditions for sequence A. Non-three sequences scan: ● 0bx00: ADTRG ● 0bx01: IN_TRG0	RW

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Bit	Name	Functional Description	Access
2:0	TRGSELA	● 0bx10: IN_TRG1 ● 0bx11: IN_TRG0 +IN_TRG1 Three sequences scan: ● 0b000: ADTRG ● 0b001: IN_TRG0 ● 0b010: IN_TRG1 ● 0b011: IN_TRG0 +IN_TRG1 ● 0b100: IN_TRG2 ● 0b101: IN_TRG0 +IN_TRG2 ● 0b110: IN_TRG1 +IN_TRG2 ● 0b111: IN_TRG0 +IN_TRG1 +IN_TRG2 **Note** Writing 1 to ADC_STR.STRT for software trigger when the ADC is idle ignores the settings of TRGENA and TRGSELA, and directly starts ADC conversion. The interval between two triggers must be greater than or equal to the scan period t_{SCAN}, and if less, the trigger is disabled.	RW

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15.4.10 ADC Channel x Sampling Time Register (ADC_SSTRx) (x=0-15)

Note

Please set this register when ADC_STR.STRT is 0.

Offset: 0x20+0x1*x

Offset	Bit Position							
-	7	6	5	4	3	2	1	0
Reset	0x04							
Name	SST							
Access	RW							

Bit	Name	Functional Description	Access
7:0	SST	Sample Period Count ● 0x00-0x01: Setting prohibited ● 0x02-0xFF: Correspond to 2-255 ADCLK clock periods respectively Channels CH0-15 are set by ADC_SSTRx (x=0-15) . **Note** When the ADCLK frequency is 80MHz, a sampling period is 12.5ns, and the initial conversion state has 8 sampling periods. Register can be set to adjust sampling time when external input impedance R_{AIN} is too large with insufficient sampling time or ADCLK frequency is low. The sample time should not be less than 2 periods. $SST \geqq (R_{AIN}+R_{ADC}) * C_{ADC} * \ln(2^{N+2}) * f_{ADC} + 1$ Where: R_{AIN} represents external input impedance (Ω), R_{ADC} represents internal sampling switch resistance (Ω), C_{ADC} represents internal sampling and retention capacitance (F), N represents AD resolution (12), and f_{ADC} represents ADCLK frequency (Hz). For specific information, please refer to the relevant sections of the "Electrical Specifications" chapter in the Datasheet.	RW

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15.4.11 ADC Sequence C Channel Select Register (ADC_CHSELRC)

Note

Please set this register when ADC_STR.STRT is 0.

Offset	Bit Position																													
0x40	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	CHSELC																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	CHSELC	Conversion Channel Selection For sequence C channel selection, each bit represents a channel. CHSELC[x] represents channel CHx, and any combination can be selected. ● 0b0: Corresponding channel is not selected ● 0b1: Corresponding channel is selected **Notice** This is only valid in three sequences scan mode. Please do not select the same channel for both sequences A, B, and C. ADC supports channels 0-15. Unsupported channels need to be set to 0.	RW

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15.4.12 ADC Interrupt Flag Register (ADC_ISR)

Offset	Bit Position							
0x44	7	6	5	4	3	2	1	0
Reset	0x00							
Name	Reserved		SBSTPDF	SASTPDF	Reserved	EOCCF	EOCBF	EOCAF
Access			RO	RO		RO	RO	RO

Bit	Name	Functional Description	Access
7:6	*Reserved*	-	-
5	SBSTPDF	Sequence B Interrupt Flag ● 0b0: Sequence B is not interrupted ● 0b1: Sequence B is interrupted **Note** In three sequences scan mode, this bit is set to 1 when sequence B is interrupted by sequence C with higher priority during scanning.	RO
4	SASTPDF	Sequence A Interrupt Flag ● 0b0: Sequence A is not interrupted ● 0b1: Sequence A is interrupted **Note** In dual sequence or three sequences scan mode, this bit is set to 1 when sequence A is interrupted by sequence B or C with higher priority during scanning.	RO
3	*Reserved*	-	-
2	EOCCF	Sequence C Conversion Complete Flag ● 0b0: The selected channels in sequence C have not been scanned completely ● 0b1: All selected channels in sequence C have been scanned completely **Note** This bit is set to 1 after all selected channels in sequence C have been scanned completely.	RO
1	EOCBF	Sequence B Conversion Complete Flag ● 0b0: The selected channels in sequence B have not been scanned completely ● 0b1: All selected channels in sequence B have been scanned completely **Note** This bit is set to 1 after all selected channels in sequence B have been scanned completely.	RO

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Bit	Name	Functional Description	Access
0	EOCAF	Sequence A Conversion Complete Flag ● 0b0: The selected channels in sequence A have not been scanned completely ● 0b1: All selected channels in sequence A have been scanned completely **Note** This bit is set to 1 after all selected channels in sequence A have been scanned completely.	RO

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15.4.13 ADC Interrupt Enable Register (ADC_ICR)

Offset	Bit Position							
0x45	7	6	5	4	3	2	1	0
Reset	0x07							
Name	Reserved					EOCCIEN	EOCBIEN	EOCAIEN
Access						RW	RW	RW

Bit	Name	Functional Description	Access
7:3	*Reserved*	-	-
2	EOCCIEN	Sequence C Conversion Complete Interrupt Enabled ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW
1	EOCBIEN	Sequence B Conversion Complete Interrupt Enabled ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW
0	EOCAIEN	Sequence A Conversion Complete Interrupt Enabled ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW

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15.4.14 ADC Interrupt Flag Clear Register (ADC_ISCLRR)

Offset	Bit Position							
0x46	7	6	5	4	3	2	1	0
Reset	0x00							
Name	Reserved		CLRSBSTPDF	CLRSASTPDF	Reserved	CLREOCCF	CLREOCBF	CLREOCAF
Access			WO	WO		WO	WO	WO

Bit	Name	Functional Description	Access
7:6	*Reserved*	-	-
5	CLRSBSTPDF	Sequence B Interrupt Flag Reset Write 1 to reset the SBSTPDF bit, write 0 has no effect; read always returns 0.	WO
4	CLRSASTPDF	Sequence A Interrupt Flag Reset Write 1 to reset the SASTPDF bit, write 0 has no effect; read always returns 0	WO
3	*Reserved*	-	-
2	CLREOCCF	Sequence C Conversion Complete Flag Reset Write 1 to reset the EOCCF bit, write 0 has no effect; read always returns 0.	WO
1	CLREOCBF	Sequence B Conversion Complete Flag Reset Write 1 to reset the EOCBF bit, write 0 has no effect; read always returns 0.	WO
0	CLREOCAF	Sequence A Conversion Complete Flag Reset Write 1 to reset the EOCAF bit, write 0 has no effect; read always returns 0.	WO

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15.4.15 ADC Channel x Convert Data Register (ADC_DRx) (x=0-15)

This register is a read-only register used to store the ADC conversion data for each channel. The storage method of conversion result data varies depending on the oversampling mode, data alignment, and conversion resolution.

Offset: 0x50+0x2*x

Oversampling Mode

Offset	Bit Position															
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	AD[15:0]															
Access	RO															

Data Right Alignment - 12-bit Resolution

Offset	Bit Position															
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved				AD[11:0]											
Access					RO											

Data Left Alignment - 12-bit Resolution

Offset	Bit Position															
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	AD[11:0]												Reserved			
Access	RO															

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15.4.16 ADC Analog Watchdog Control Register (ADC_AWDCR)

Offset	Bit Position															
0xA0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved						AWDCM		Reserved	AWD1MD	AWD1IEN	AWD1EN	Reserved	AWD0MD	AWD0IEN	AWD0EN
Access							RW			RW	RW	RW		RW	RW	RW

Bit	Name	Functional Description	Access
15:10	*Reserved*	-	-
9:8	AWDCM	Watchdog Window Combination Selection ● 0b00: Window combination inactive, ADC_CMP1 outputs independent comparison results for Window 1 ● 0b01: Window combination active, ADC_CMP1 outputs logical OR of comparison results for Window 0 and Window 1 ● 0b10: Window combination active, ADC_CMP1 outputs logical AND of comparison results for Window 0 and Window 1 ● 0b11: Window combination active, ADC_CMP1 outputs logical XOR of comparison results for Window 0 and Window 1 **Note** When using the window combination function, both Window 0 and Window 1 must be enabled (i.e., AWD0EN is written to 1, AWD1EN is written to 1). If the comparison channels selected for Window 0 and Window 1 are different, please ensure that during the scan conversion process, the channel selected for Window 1 is converted after the channel selected for Window 0. The ADC_CMP1 interrupt or event is output when the conversion of the channel selected for Window 1 ends.	RW
7	*Reserved*	-	-
6	AWD1MD	Watchdog Window 1 Compare Mode Window 1 Protected Area Selection: ● 0b0: Conversion result < AWD1DR0, or conversion result > AWD1DR1 ● 0b1: Conversion result ≥ AWD1DR0, and conversion result ≤ AWD1DR1	RW
5	AWD1IEN	Watchdog Window 1 Interrupt Enabled ● 0b0: Watchdog Window 1 comparison interrupt ADC_CMP1 inactive ● 0b1: Watchdog Window 1 comparison interrupt ADC_CMP1 enabled	RW
4	AWD1EN	Watchdog Window 1 Compare Enabled ● 0b0: Watchdog Window 1 comparison function inactive ● 0b1: Watchdog Window 1 comparison function enabled	RW

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Bit	Name	Functional Description	Access
3	*Reserved*	-	-
2	AWD0MD	Watchdog Window 0 Compare Mode Window 0 Protected Area Selection: ● 0b0: Conversion result < AWD0DR0, or conversion result > AWD0DR1 ● 0b1: Conversion result ≥ AWD0DR0, and conversion result ≤ AWD0DR1	RW
1	AWD0IEN	Watchdog Window 0 Interrupt Enabled ● 0b0: Watchdog Window 0 comparison interrupt ADC_CMP0 inactive ● 0b1: Watchdog Window 0 comparison interrupt ADC_CMP0 enabled	RW
0	AWD0EN	Watchdog Window 0 Compare Enabled ● 0b0: Watchdog Window 0 comparison function inactive ● 0b1: Watchdog Window 0 comparison function enabled	RW

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15.4.17 ADC Analog Watchdog Status Register (ADC_AWDSR)

Offset	Bit Position							
0xA2	7	6	5	4	3	2	1	0
Reset	0x00							
Name	Reserved			AWDCMF	Reserved		AWD1F	AWD0F
Access				RO			RO	RO

Bit	Name	Functional Description	Access
7:5	*Reserved*	-	-
4	AWDCMF	Watchdog Window Combination Compare Status Bit ● 0b0: Compare result of Window 0 and Window 1 does not meet the combination condition ● 0b1: Compare result of Window 0 and Window 1 meets the combination condition **Note** When the watchdog window combination comparison function is enabled (i.e., ADC_AWDCR.AWDCM[1:0]=0b01/0b10/0b11), this bit is set to 1 when the conversion of the channel selected for Window 1 ends and the comparison result of Window 0 and Window 1 meets the combination condition.	RO
3:2	*Reserved*	-	-
1	AWD1F	Watchdog Window 1 Comparative Status Bit ● 0b0: Conversion result does not meet the comparison condition ● 0b1: Conversion result meets the comparison condition **Note** This bit is set to 1 when the conversion of the channel selected for Window 1 ends and the conversion result meets the comparison condition.	RO
0	AWD0F	Watchdog Window 0 Comparative Status Bit ● 0b0: Conversion result does not meet the comparison condition ● 0b1: Conversion result meets the comparison condition **Note** This bit is set to 1 when the conversion of the channel selected for Window 0 ends and the conversion result meets the comparison condition.	RO

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15.4.18 ADC Analog Watchdog Status Clear Register (ADC_AWDSCLRR)

Offset	Bit Position							
0xA3	7	6	5	4	3	2	1	0
Reset	0x00							
Name	Reserved			CLRAWDCMF	Reserved		CLRAWD1F	CLRAWD0F
Access				WO			WO	WO

Bit	Name	Functional Description	Access
7:5	*Reserved*	-	-
4	CLRAWDCMF	Watchdog Window Combination Compare Status Bit Reset Write 1 to reset AWDCMF status bit, write 0 has no effect; read always returns 0	WO
3:2	*Reserved*	-	-
1	CLRAWD1F	Watchdog Window 1 Compare Status Bit Reset Write 1 to reset AWD1F status bit, write 0 has no effect; read always returns 0	WO
0	CLRAWD0F	Watchdog Window 0 Compare Status Bit Reset Write 1 to reset AWD0F status bit, write 0 has no effect; read always returns 0	WO

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15.4.19 ADC Analog Watchdog x Compare Data Register y (ADC_AWDxDRy) (x=0-1, y=0-1)

Offset: 0xA4+0x8*x+0x2*y

Offset	Bit Position															
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000 (AWDxDR0); 0xFFFF (AWDxDR1)															
Name	AWDDR															
Access	RW															

Bit	Name	Functional Description	Access
15:0	AWDDR	Comparative Data AWD0DR0 sets the low threshold for Window 0, and AWD0DR1 sets the high threshold for Window 0. AWD1DR0 sets the low threshold for Window 1, and AWD1DR1 sets the high threshold for Window 1. AWD0DR0, AWD0DR1, AWD1DR0 and AWD1DR1 vary depending on the alignment (right-aligned or left-aligned data) . ● Right-aligned data-12-bit resolution: Low 12 bits [11:0] are available ● Left-aligned data-12-bit resolution: High 12 bits [15:4] are available **Note** The unused bits of AWD0DR0, AWD0DR1, AWD1DR0, AWD1DR1 need to be filled with 0.	RW

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15.4.20 ADC Analog Watchdog x Channel Select Register (ADC_AWDxCHSR) (x=0-1)

Offset: 0xA8+0x8*x

Offset	Bit Position							
-	7	6	5	4	3	2	1	0
Reset	0x00							
Name	Reserved			AWDCH				
Access				RW				

Bit	Name	Functional Description	Access
7:5	*Reserved*	-	-
4:0	AWDCH	Watchdog Compare Channel Selection Select the comparison channel for Window x. ● 0x00: CH0 (Channel 0) ● 0x01: CH1 (Channel 1) ● …… ● 0x0F: CH15 (Channel 15) ● Others: Setting prohibited **Notice** Please do not set non-existent channels.	RW

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15.4.21 OPA Control Register (ADC_OPACR)

Offset	Bit Position																													
0xC0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																													OPA3EN	OPA2EN	OPA1EN
Access																														RW	RW	RW

Bit	Name	Functional Description	Access
31:3	*Reserved*	-	-
2	OPA3EN	OPA3 Enable ● 0b0: Disable ● 0b1: Enable	RW
1	OPA2EN	OPA2 Enable ● 0b0: Disable ● 0b1: Enable	RW
0	OPA1EN	OPA1 Enable ● 0b0: Disable ● 0b1: Enable	RW

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15.5 Precautions

15.5.1 Precautions for Reading Data Registers

Please access ADC_DR in half-word units. Do not access data registers in byte units.

15.5.2 Precautions for Handling Scan Completion Interrupts

When two consecutive scan conversions are performed on the same channel, during the period from the completion of interrupt handling in the first conversion to the completion of interrupt handling in the second conversion, if the CPU does not read the first converted data in time, the second converted data will overwrite the first converted data.

15.5.3 Precautions for Module Stop and Low Power Settings

The ADC module can be stopped and power consumption reduced by setting the CMU_FCG register. The ADC is initially in the stopped state. To start the ADC module, first set the corresponding bit in the CMU_FCG register to cancel the stop, and wait for 1μs before starting the ADC conversion.

Before setting the module to stop, please confirm that the ADC is in the conversion stop state, i.e., the ADC_STR.STRT bit is 0.

Before setting the system to enter STOP mode, please set the ADC to module Stop mode first.

For specific descriptions, please refer to the relevant sections of the "Action Mode and Low Power Mode" section in the "Power Control (PWC) " chapter.

15.5.4 ADC Conversion Analog Channel Input Pin Settings

When setting a chip pin as an ADC analog channel input, please first disable the digital function (PCRxy.DDIS) of the corresponding pin. For specific descriptions, please refer to the "General-Purpose I/O (GPIO)" chapter.

15.5.5 Noise Control

To prevent abnormal voltages such as surges from damaging the analog input pin, it is recommended to use the protection circuit shown in the "Electrical Specifications" chapter in the Datasheet.

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16 Digital-to-Analog Converter (DAC)

16.1 Introduction

This MCU is equipped with 1 12-bit digital-to-analog converter (DAC) unit. DAC unit includes 1 DAC conversion channel. The analog voltage output range has two selectable settings.

16.2 Features

- 1 DAC conversion channel
- The output can be used as the negative-end voltage for the voltage comparator (CMP)

16.3 Functional Description

For relevant functional descriptions and usage introductions, please refer to the section "Functional Description-12-bit DAC Configuration" in the chapter "Voltage Comparator (CMP)".

16.4 Register Description

For introductions to relevant registers, please refer to the "Register Description" section in the chapter "Voltage Comparator (CMP)".

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17 General Control Timer (Timer4)

17.1 Introduction

The General Control Timer 4 is a timer module designed for three-phase motor control, offering a variety of solutions for different three-phase motor control applications. It supports both triangular and sawtooth waveform modes, enabling the generation of various PWM waveforms. It also features buffer functionality and supports EMB control. 1 unit of Timer4 is carried in this product family.

17.2 Features

The following table outlines the basic functions and features of Timer4.

Table 17-1 Basic Functions and Features of Timer4

Waveform mode	Sawtooth wave, triangle wave
Basic function	Up/Down-counting direction
	Buffer function
	General PWM output
	General compare match event
	Overflow/Underflow/Reload count match event
	Special compare match event
	Hardware counter start
	Software-synchronized counter start
	EMB control
Interrupt type	General compare match interrupt
	Count period match interrupt
	Reload count match interrupt
	Special compare match interrupt

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17.3 Functional Description

17.3.1 Timer4 Block Diagram

The figure below describes the basic architecture of the general control timer Timer4.

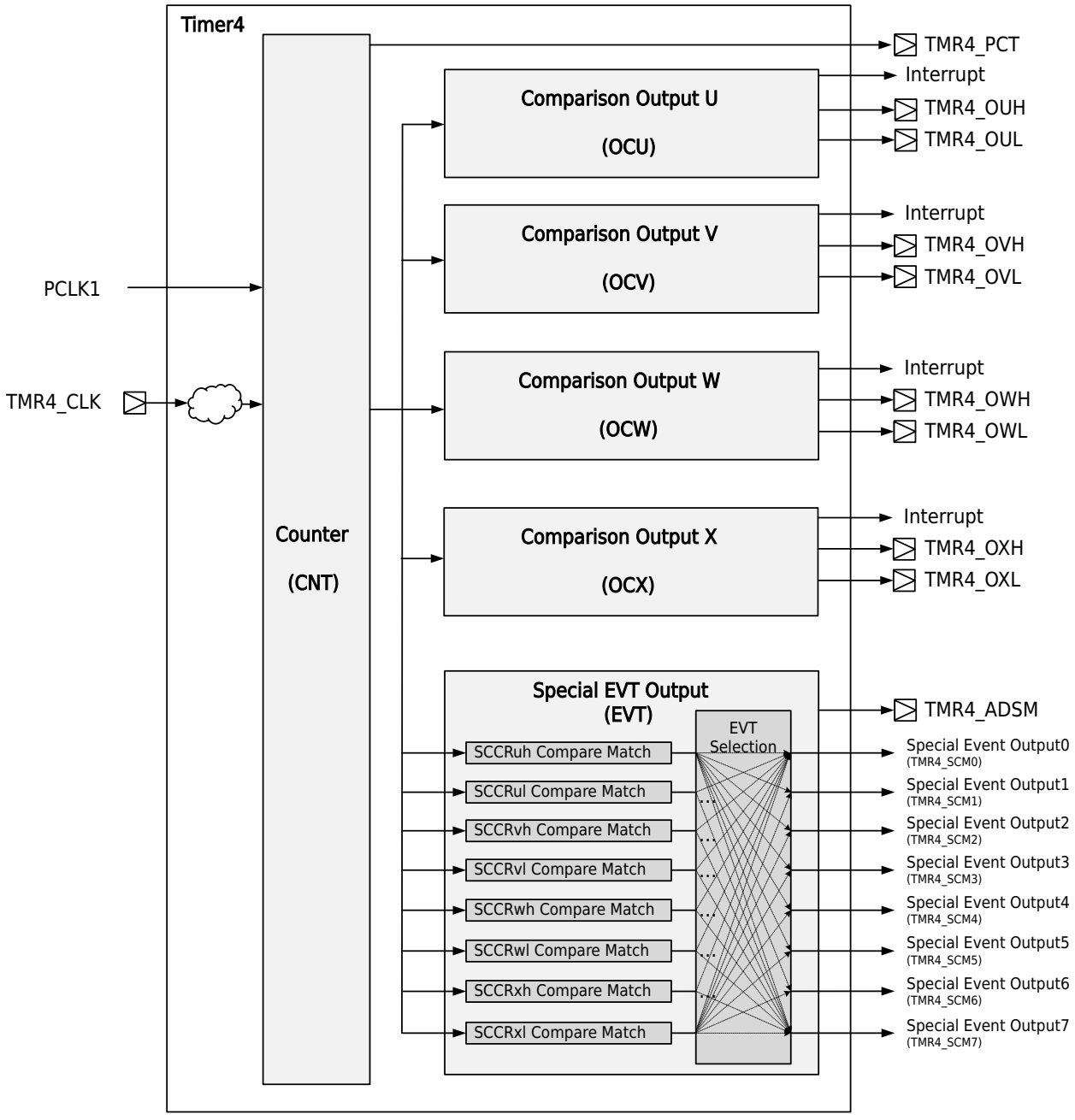

Figure 17-1 Timer4 Basic Block Diagram

The following table lists the input and output ports of Timer4.

Table 17-2 Timer4 Port List

Port Name	Direction	Function
TMR4_CLK	Input	Count clock input port
TMR4_PCT	Output	PWM periodic output monitoring
TMR4_ADSM	Output	Special event output monitoring

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Port Name	Direction	Function
TMR4_OUH	Output	PWM output port
TMR4_OUL		
TMR4_OVH		
TMR4_OVL		
TMR4_OWH		
TMR4_OWL		
TMR4_OXH		
TMR4_OXL		

17.3.2 Basic Actions

17.3.2.1 Waveform Mode

Timer4 has two basic counting waveform modes, sawtooth wave mode and triangle wave mode. The two waveform modes can be implemented based on the setting of CCSR.MODE.

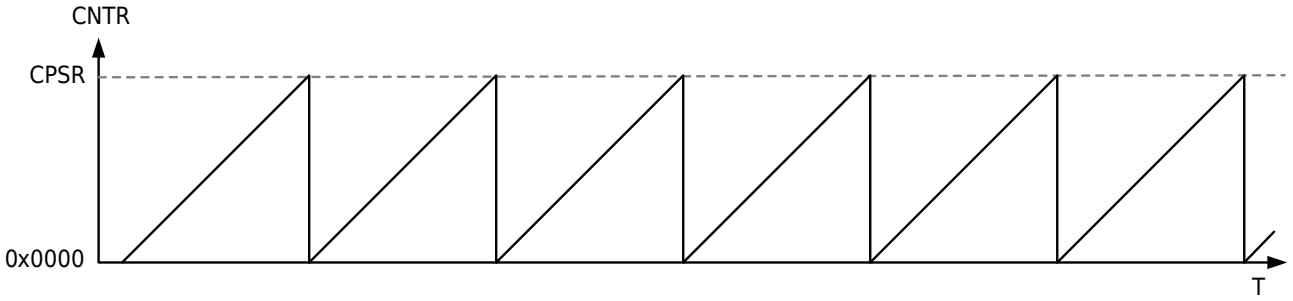

Figure 17-2 Timer4 Sawtooth Waveform

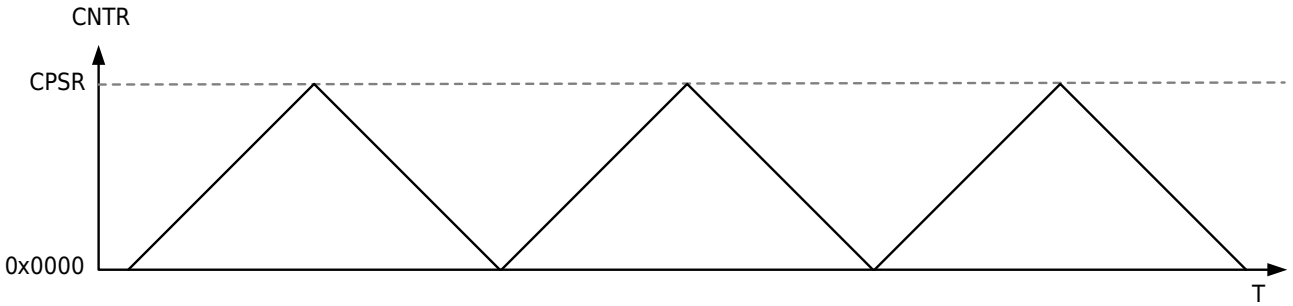

Figure 17-3 Timer4 Triangle Waveform

17.3.2.2 Counting Action

- The sawtooth wave counting operation and control process are shown in the figure below:

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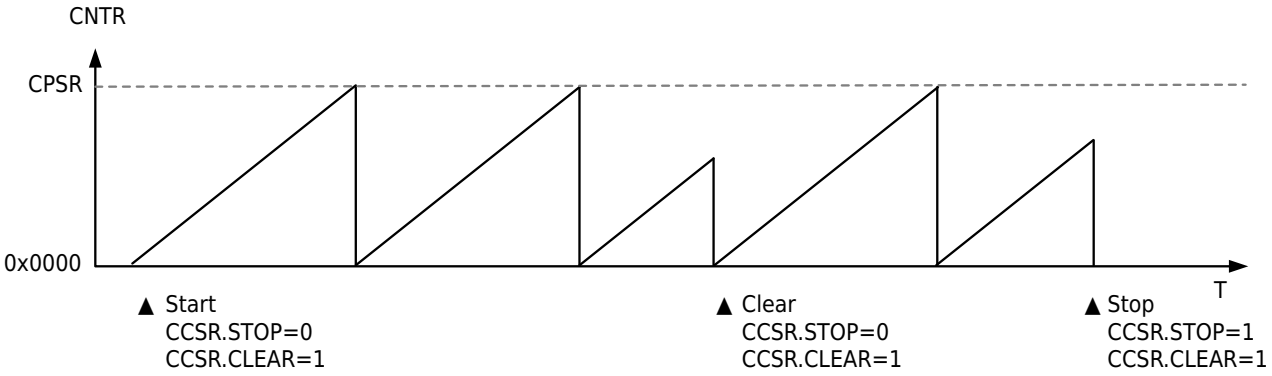

Figure 17-4 Timer4 Sawtooth Wave Mode Counting Action

1. Setting mode CCSR.MODE=0.
2. Set the count peak CPSR register.
3. By writing CCSR.STOP=0 and CCSR.CLEAR=1, the counter count value (CNTR) is initialized to 0x0000 and the counting operation is started. The counter value starts counting up from 0x0000. When it reaches the peak value (CPSR), the count value returns to 0x0000, and this operation is repeated in sequence.
4. Counting period=(CPSR + 1) ×counting clock period.
5. During the counting process, writing CCSR.STOP=0 and CCSR.CLEAR=1 can initialize the counting value to 0x0000 and continue counting operation.
6. During the counting process, writing CCSR.STOP=1 and CCSR.CLEAR=1 can initialize the count value to 0x0000 and stop the counting operation.

- The triangle wave counting operation and control process are shown in the figure below:

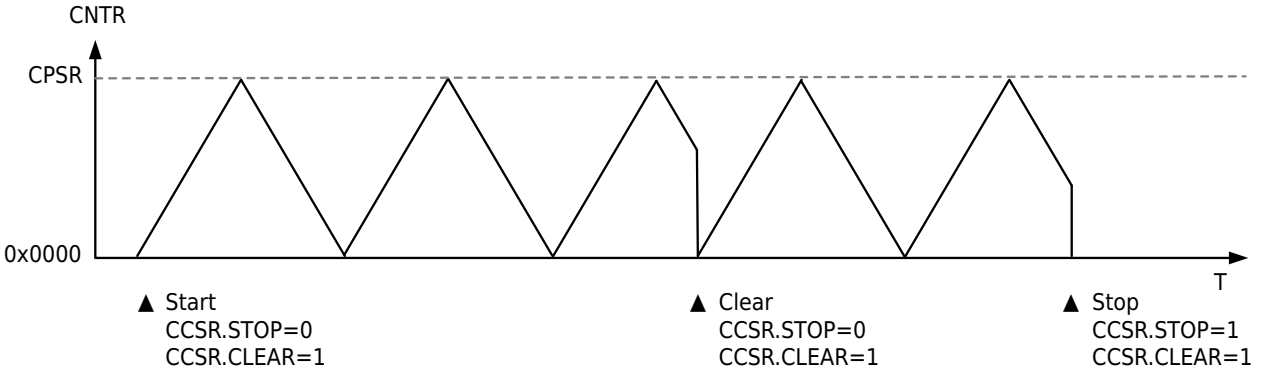

Figure 17-5 Timer4 Triangle Wave Mode Counting Action

1. Setting mode CCSR.MODE=1.
2. Set the count peak CPSR register.
3. By writing CCSR.STOP=0 and CCSR.CLEAR=1, the counter count value (CNTR) is initialized to 0x0000 and the counting operation is started. The counter value starts counting up from 0x0000 and counts up before reaching the counting peak value; when the peak value (CPSR) is reached, the counter starts counting down until the count value returns to 0x0000; then the counting operation is repeated again, and this operation is repeated in sequence.
4. Counting period=CPSR×2×counting clock period.
5. During the counting process, writing CCSR.STOP=0 and CCSR.CLEAR=1 can initialize the count value to 0x0000 and restart the increment counting operation, and then repeat the above operation.

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6. During the counting process, writing CCSR.STOP=1 and CCSR.CLEAR=1 can initialize the count value to 0x0000 and stop the counting operation.

17.3.2.3 Compare Output

Each PWM channel of Timer4 has three compare point registers: OCCR1, OCCR2, and OCCR3. Taking the uh channel as an example: the compare point registers are OCCR1uh, OCCR2uh, and OCCR3uh. The actual compare point OCCRuh is selected and switched among these three registers. The OCSR.OCRSENH bit configures the compare point switching mode. The switching pattern differs between sawtooth wave mode and triangular wave mode: there are three switching modes in sawtooth wave mode, and four in triangular wave mode.

The following describes the compare point switching patterns for the two counting modes, using the uh channel as an example.

Sawtooth Wave Compare Point Switching Mode

1. Compare point switching mode 1 (OCSRu.OCRSENH=0b00): The compare point OCCRuh value is OCCR1uh.
2. Compare point switching mode 2 (OCSRu.OCRSENH=0b01): At the start of counting, the compare point OCCRuh value is OCCR1uh. It switches to OCCR2uh after the count value matches OCCRuh, and switches back to OCCR1uh after a count overflow.
3. Compare point switching mode 3 (OCSRu.OCRSENH=0b10): At the start of counting, the compare point OCCRuh value is OCCR1uh. It switches to OCCR2uh after the first match between the count value and OCCRuh, switches to OCCR3uh after the second match, and switches back to OCCR1uh after a count overflow.

The following three figures show waveform output examples of the compare output module in sawtooth wave counting mode.

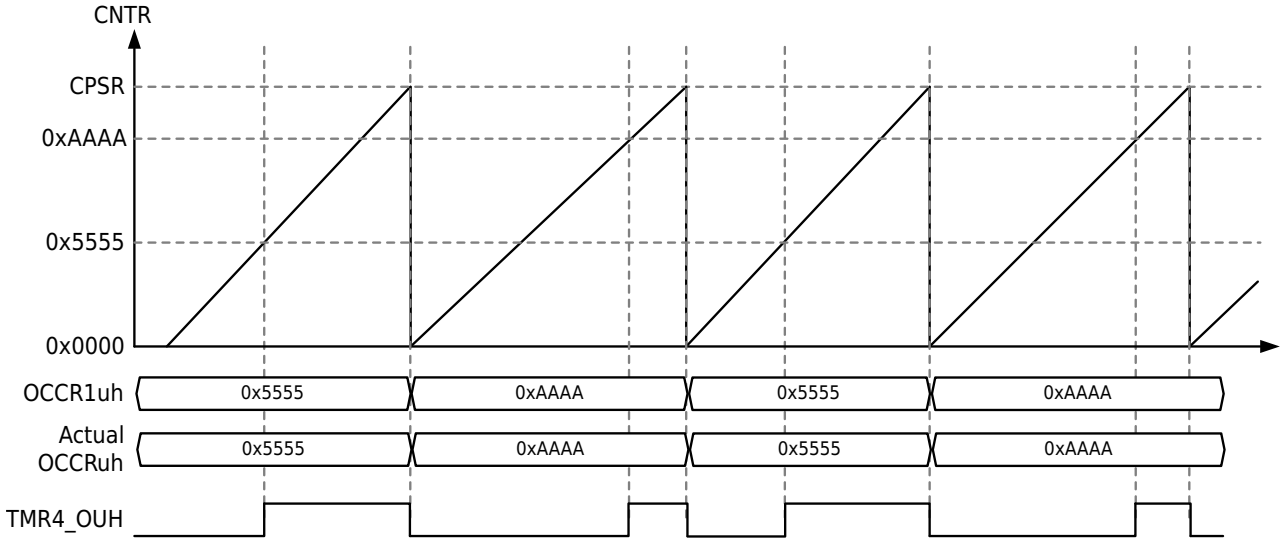

Figure 17-6 Sawtooth Wave Mode Waveform Output Example when OCSRu.OCRSENH=0b00

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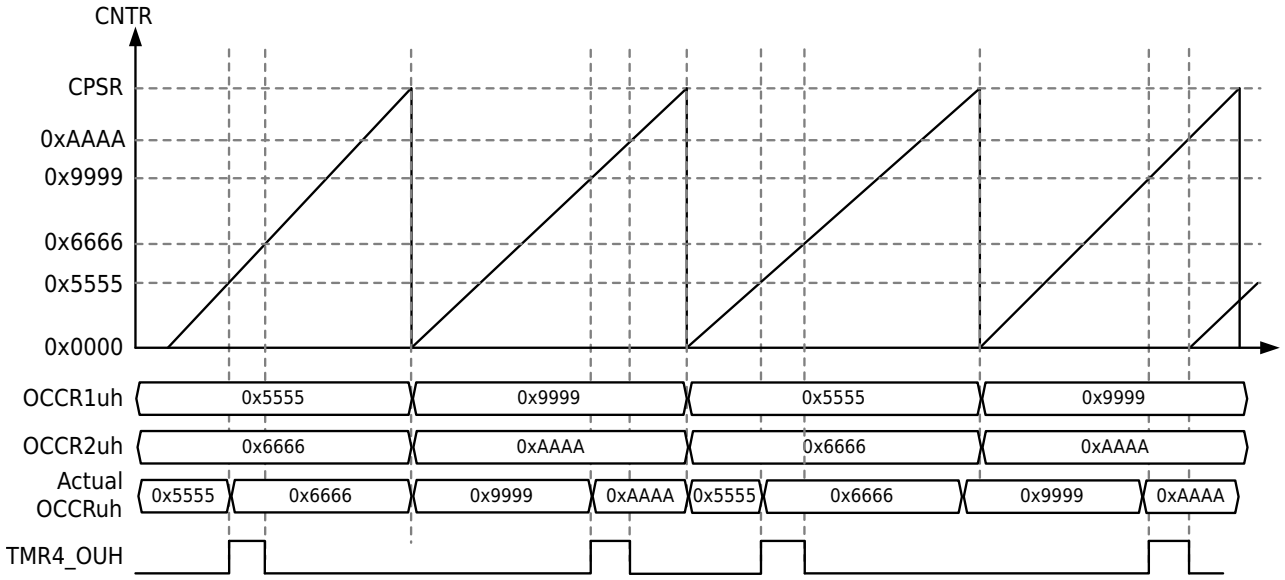

Figure 17-7 Sawtooth Wave Mode Waveform Output Example when OCSRu.OCRSENH=0b01

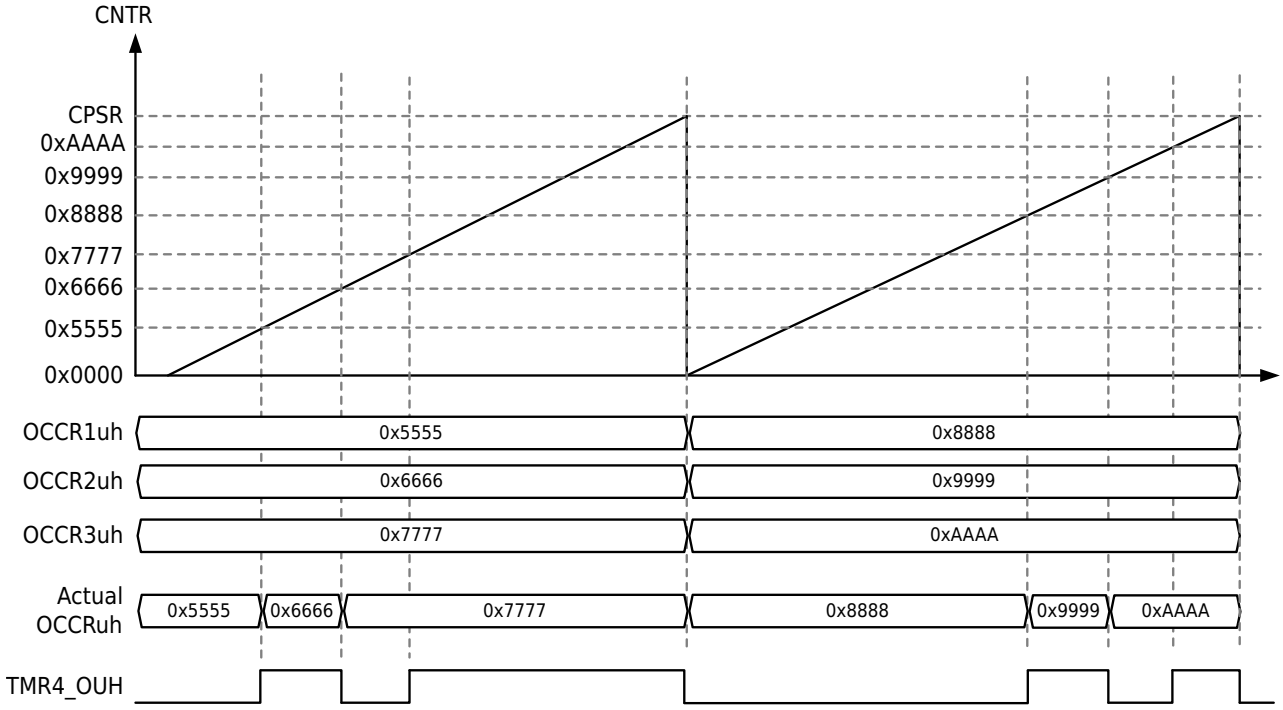

Figure 17-8 Sawtooth Wave Mode Waveform Output Example when OCSRu.OCRSENH=0b10

Triangular Wave Compare Point Switching Mode

1. Compare point switching mode 1 (OCSRu.OCRSENH=0b00): The compare point OCCRuh value is OCCR1uh.
2. Compare point switching mode 2 (OCSRu.OCRSENH=0b01): During up-counting (count value 0 → CPSR-1), the compare point OCCRuh value is OCCR1uh. During down-counting (count value CPSR → 1), the compare point OCCRuh value is OCCR2uh.
3. Compare point switching mode 3 (OCSRu.OCRSENH=0b10): At the start of up-counting, the compare point OCCRuh value is OCCR1uh. It switches to OCCR2uh after the first match between the count value and OCCRuh during up-counting, and switches to OCCR3uh after the count value overflows.
4. Compare point switching mode 4 (OCSRu.OCRSENH=0b11): At the start of up-counting, the compare point OCCRuh value is OCCR1uh. It switches to OCCR2uh after the count value overflows, and

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switches to OCCR3uh after the first match between the count value and OCCRuh during down-counting.

The following four figures show waveform output examples of the compare output module in triangular wave counting mode.

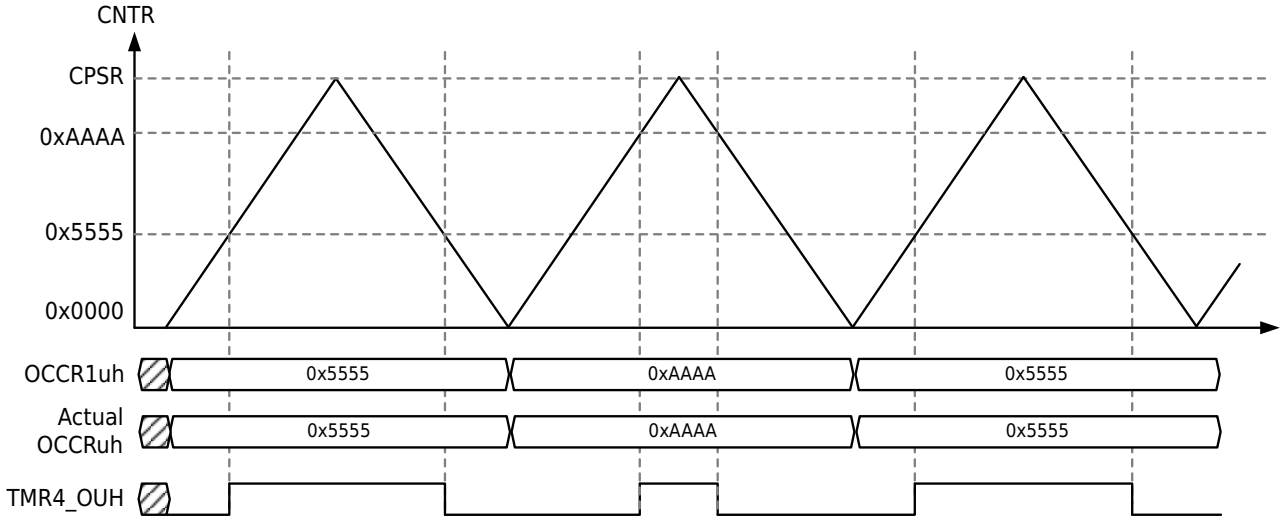

Figure 17-9 Triangular Wave Mode Waveform Output Example when OCSRu.OCRSENH=0b00

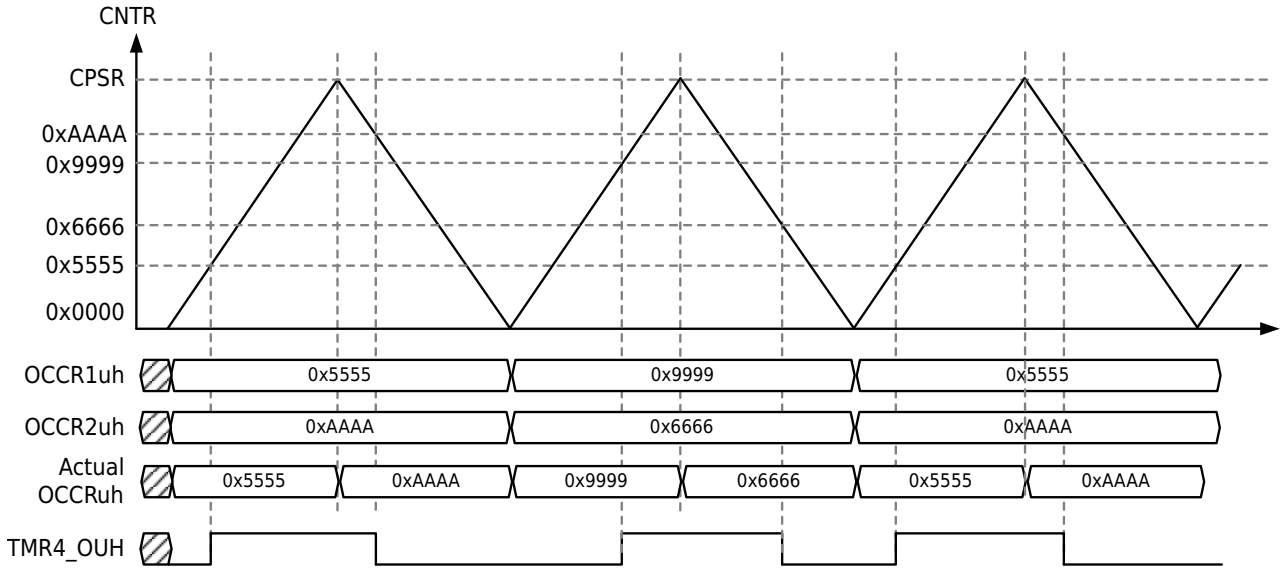

Figure 17-10 Triangular Wave Mode Waveform Output Example when OCSRu.OCRSENH=0b01

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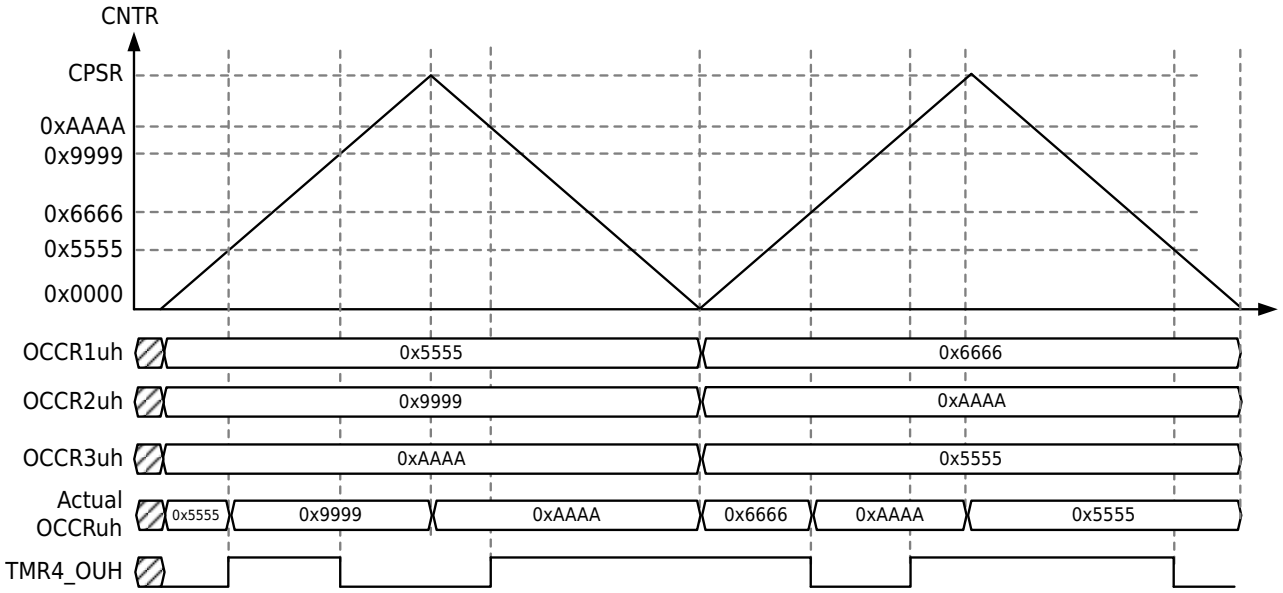

Figure 17-11 Triangular Wave Mode Waveform Output Example when OCSRu.OCRSENH=0b10

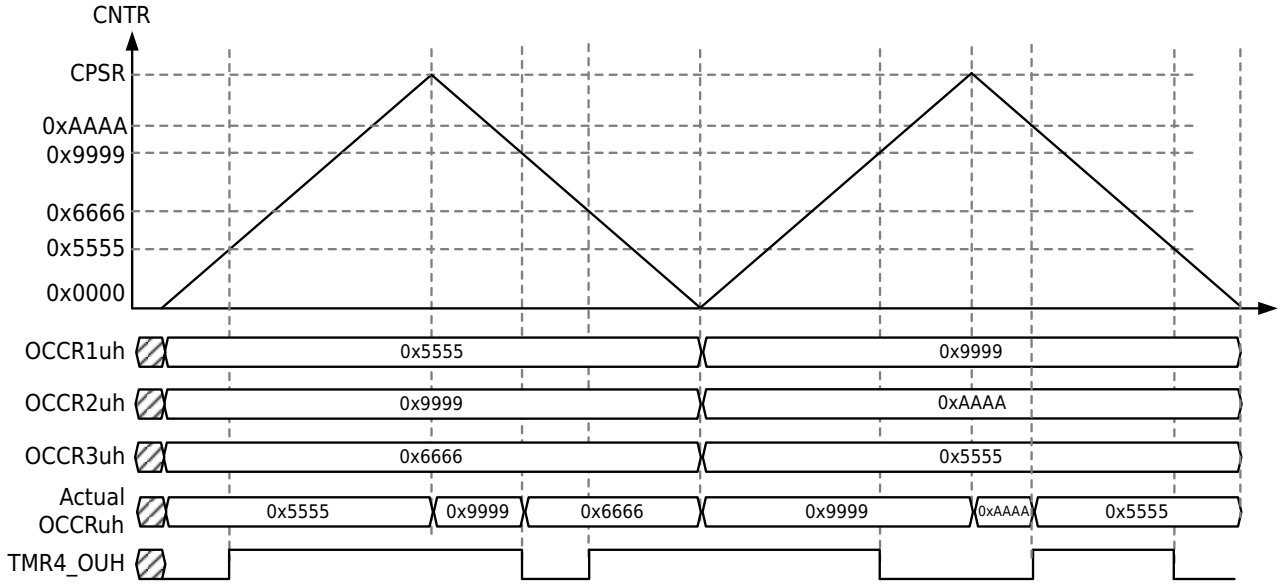

Figure 17-12 Triangular Wave Mode Waveform Output Example when OCSRu.OCRSENH=0b11

17.3.3 Buffer Function

The Timer4 module provides buffer function for the CPSR Register, the OCCR Register (OCCR1, OCCR2, OCCR3), the OCMR Register, the SCCR Register, and the SCMR Register.

17.3.3.1 Period Value Register Buffer Function

The CPSR Register supports buffer function. When a peak count value is written, it is first stored in the buffer register. The data is transferred from the buffer register to the CPSR register under the following conditions:

1. When the buffer function is disabled (CCSR.BUFEN=0), the written data is immediately transferred from the buffer register to the CPSR register.
2. When the buffer function is enabled (CCSR.BUFEN=1) and the periodic interval response function is not enabled (CPCR.CPSRLMCP=0, CPCR.CPSRLMCZ=0), data is transferred from the buffer register to the CPSR register when the counter stops (CCSR.STOP=1) or when the counter value is "0x0000".

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3. When the buffer function is enabled (CCSR.BUFEN=1) and the overflow point periodic interval response link function is enabled (CPCR.CPSRLMCP=1), data is transferred from the buffer register to the CPSR register when the counter stops (CCSR.STOP=1) or when the overflow point periodic interval counter is 0 (CVPR.PIC=0) and the count value overflows.
4. When the buffer function is enabled (CCSR.BUFEN=1) and the underflow point periodic interval response link function is enabled (CPCR.CPSRLMCZ=1), data is transferred from the buffer register to the CPSR register when the counter stops (CCSR.STOP=1) or when the underflow point periodic interval counter is 0 (CVPR.ZIC=0) and the count value underflows.

Notice

When reading from the CPSR, the value read is not from the buffer register but from the CPSR register itself. If the buffer function is enabled, the value read before the transfer is completed is not the most recently written value, but the previously loaded value of CPSR.

- When the sawtooth wave mode is on and the buffer function is disabled, modify the operation of the count peak CPSR:

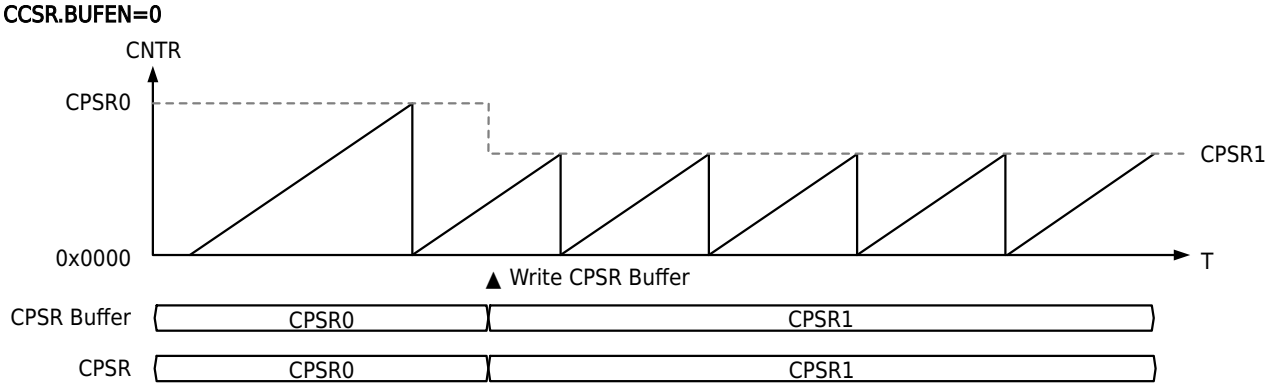

Figure 17-13 Modify Sawtooth Count Period when the Buffer is Disabled

Notice

When the buffer function is disabled, the written data is immediately transferred from the buffer register to the CPSR register, and the counting period changes immediately after the write operation is completed. In this case, if the written value is smaller than the current counter value, the counter will continue incrementing until it reaches 0xFFFF. Therefore, special caution is required in such scenarios.

- When the sawtooth wave mode is on, the buffer function is enabled, the periodic interval response link function is disabled, modify the operation of the count peak CPSR:

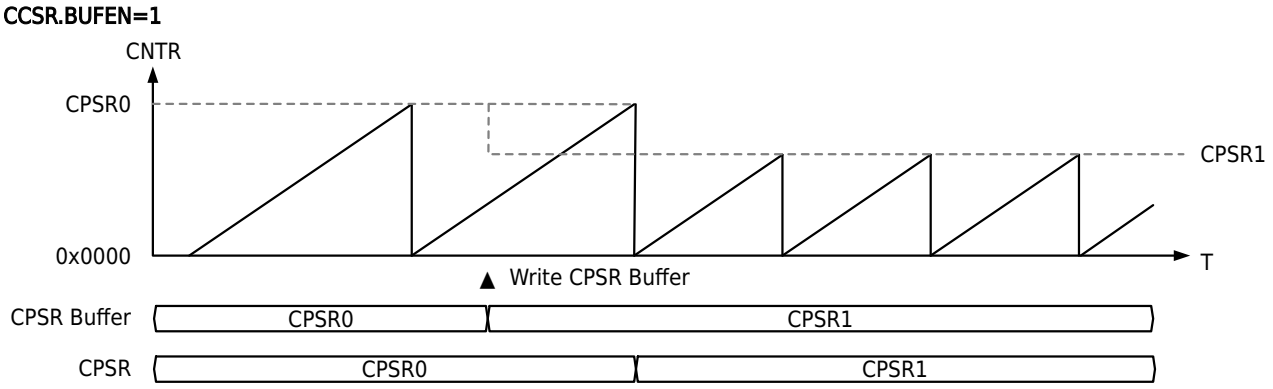

Figure 17-14 Modify Sawtooth Wave Count Period when the Buffer is Enabled

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When the buffer function is enabled, the written data is transferred from the buffer register to the CPSR register when the counter stops or when the counter value is "0x0000".

- Operation for modifying the count peak value CPSR when in sawtooth wave mode with buffer function enabled and overflow point periodic interval response link function enabled:

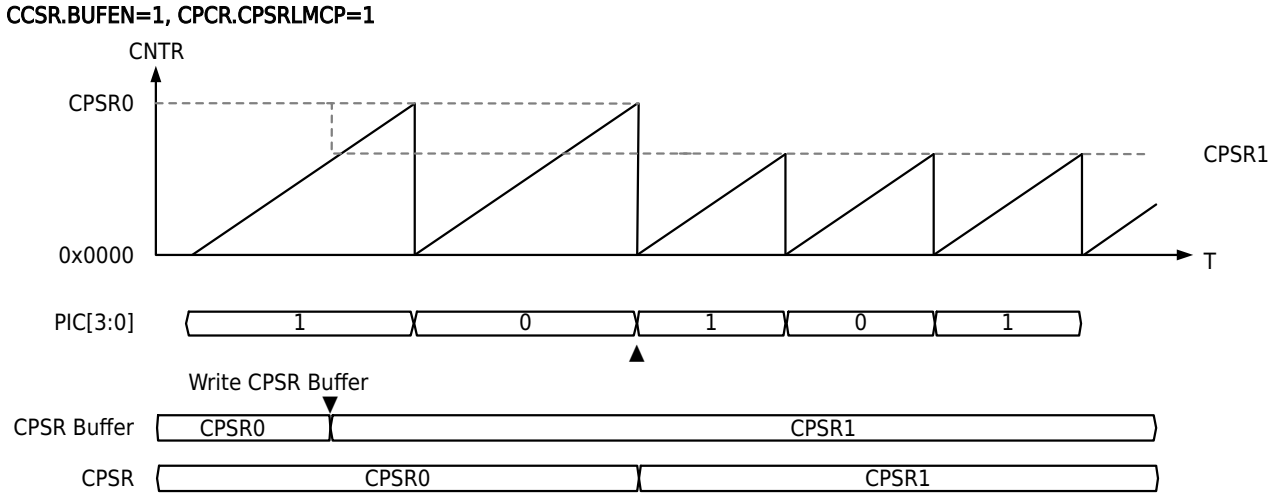

Figure 17-15 Modify Sawtooth Wave Count Period when Buffer is Enabled and Periodic Interval Response Link Function at Overflow Point is Enabled

The periodic interval counter (CVPR.PIC) counts down from 1 to 0, and the overflow interrupt is generated at the moment marked ▲ (count peak). At the moment marked ▼, the CPSR register is rewritten, and the written data is stored in the CPSR buffer register. The data loading operation, transferring data from the buffer register to the CPSR register, occurs when the counter stops or when the counter value equals CPSR and the periodic interval counter (CVPR.PIC) is 0.

- Operation to modify the count peak CPSR when in sawtooth wave mode with buffer function enabled and periodic interval response link function at underflow point enabled:

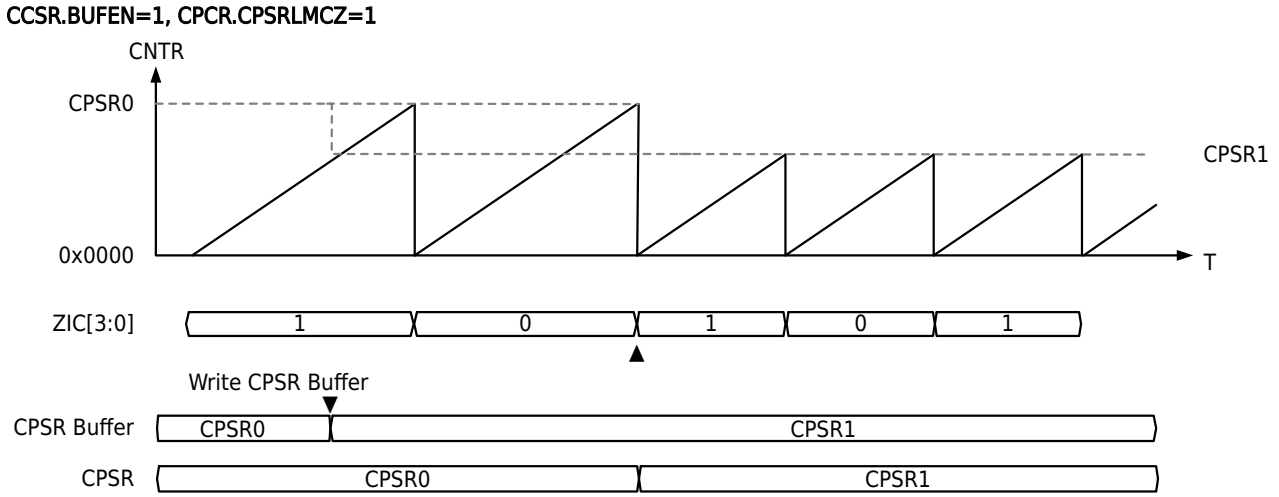

Figure 17-16 Modify Sawtooth Wave Count Period when Buffer is Enabled and Periodic Interval Response Link Function at Underflow Point is Enabled

The periodic interval counter (CVPR.ZIC) counts down from 1 to 0, and the underflow interrupt is generated at the moment marked ▲ (counter value is 0). At the moment marked ▼, the CPSR register is rewritten, and the written data is stored in the CPSR buffer register. The data loading operation, transferring data from the buffer register to the CPSR register, occurs when the counter stops or when the counter value is 0 and the periodic interval counter (CVPR.ZIC) is 0.

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- When the triangle wave mode is on, the buffer function is enabled, the periodic interval response link function is disabled, modify the operation of the count peak CPSR:

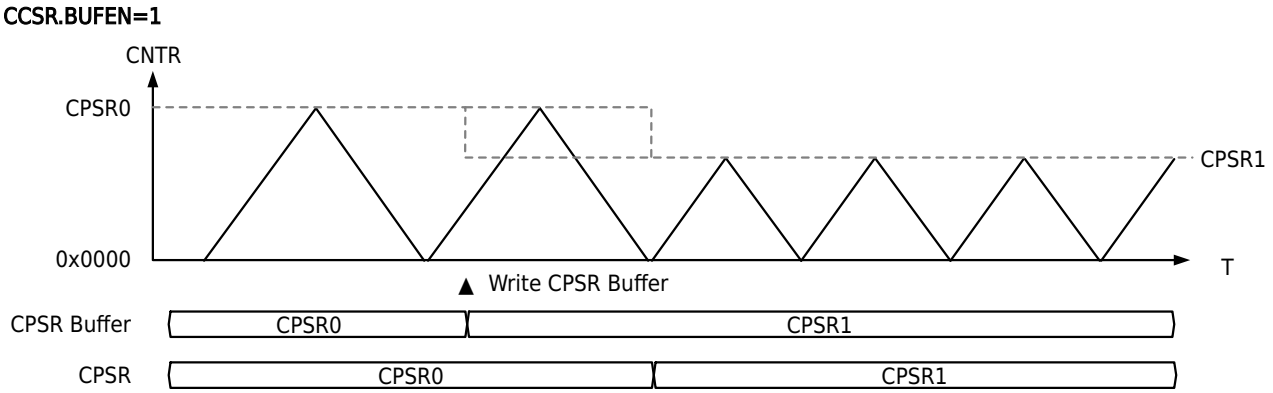

Figure 17-17 Modify Triangular Wave Count Period when Buffer is Enabled

In triangle wave counting mode, when the buffer function is enabled, the data written to the buffer register is transferred to the CPSR register when the counter stops or the next counter value is "0x0000." The change in the counter period occurs at the start of the next counter period after the write operation is completed.

- Operation to modify the count peak CPSR when in triangle wave mode with buffer function enabled and periodic interval response link function at overflow point enabled:

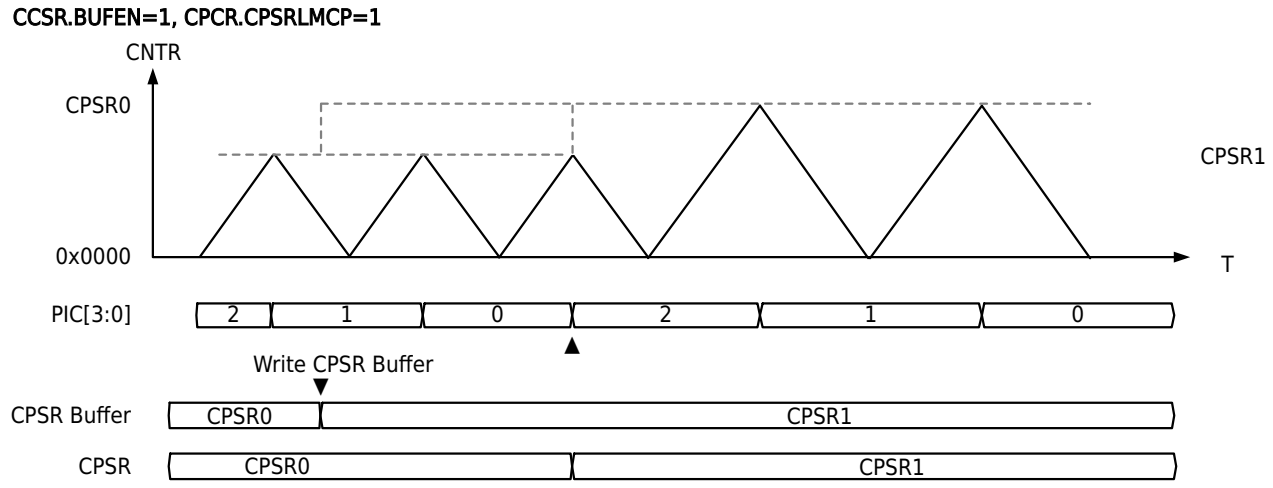

Figure 17-18 Modify Triangular Wave Count Period when Buffer is Enabled and Periodic Interval Response Link at Overflow Point is Enabled

The periodic interval counter (CVPR.PIC) counts down from 1 to 0, and the overflow interrupt is generated at the moment marked ▲ (count peak). At the moment marked ▼, the CPSR register is rewritten, and the written data is stored in the CPSR buffer register. The data loading operation, transferring data from the buffer register to the CPSR register, occurs when the counter stops or when the counter value equals CPSR and the periodic interval counter (CVPR.PIC) is 0.

Notice

When the overflow point periodic interval response link function is enabled and the newly written CPSR1 is less than the old CPSR0, the down-counting after CPSR is updated to CPSR1 will generate one additional overflow match.

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- When in triangular wave mode with buffer function enabled and underflow point periodic interval response link function enabled, the operation to modify the count peak value CPSR is:

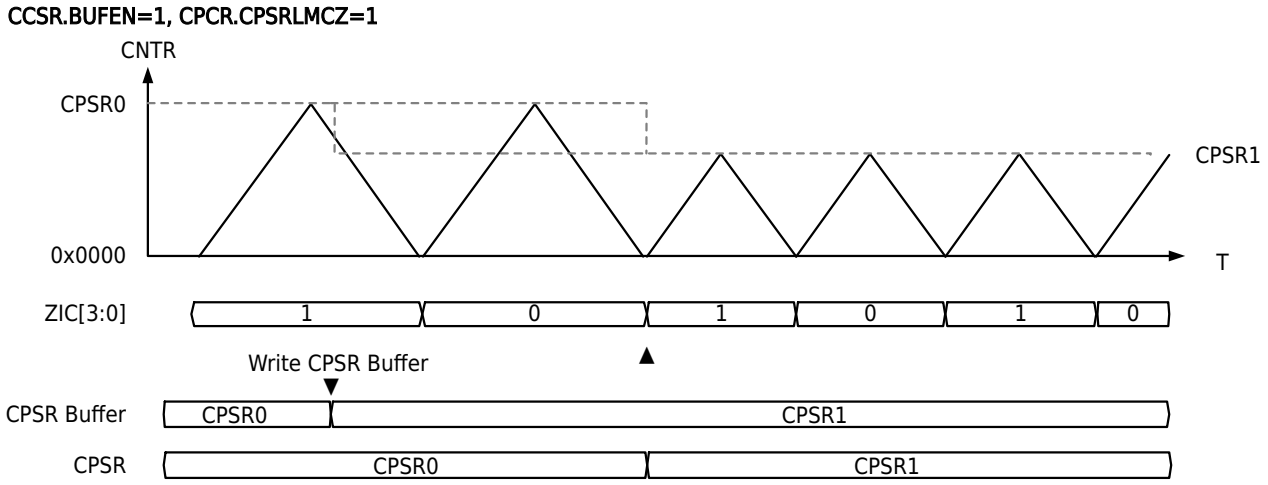

Figure 17-19 Cache Enable and Enable Underflow Point Periodic Interval Response Link when Modifying Triangular Wave Counting Period

The period interval counter (CVPR.ZIC) counts down from 1 to 0, and the underflow interrupt is generated at the flag ▲ (when the count value is 0). At the ▼ moment, the CPSR register is rewritten, and the written data is stored in the CPSR buffer register. The data loading operation is performed when the counter stops or when the counter value is 0x0000 and the period interval counter (CVPR.ZIC) is 0, transferring data from the buffer register to the CPSR register.

17.3.3.2 General Compare Register Buffer Function

The general compare reference register (OCCR1m/OCCR2m/OCCR3m, m=uh/ul/vh/vl/wh/wl/xh/xl) and the general mode control register (OCMR) both have buffer register functions. When the buffer function is enabled, the data is loaded into the OCCR1m/OCCR2m/OCCR3m and OCMR registers at the specified transmission time. The OCCR1m/OCCR2m/OCCR3m buffer function is used to synchronize the change of the comparison value during the counting process, while the OCMR buffer function is used to synchronize the change of the internal PWM output at the counting overflow point (sawtooth wave), valley point, or peak point (triangle wave).

Since the cache functions of OCCR1m/OCCR2m/OCCR3m are consistent, OCCR1m is used as an example below to illustrate the buffer function of the general compare reference value register.

1. **When the link transmission of output comparison with the counter period interval response function is disabled, the buffer value is loaded into the register at the set counting state. In this case, the loading process is independent of the counter period interval counter.**

   The figure below shows the waveform (x=L or H) when the general output compare OCCR (Take OCCR1m for example) buffer function is enabled, the counter is loaded at zero value (OCER.CxBUFEN=0b01), and the counter period interval response link is disabled (OCER.LMCx=0).

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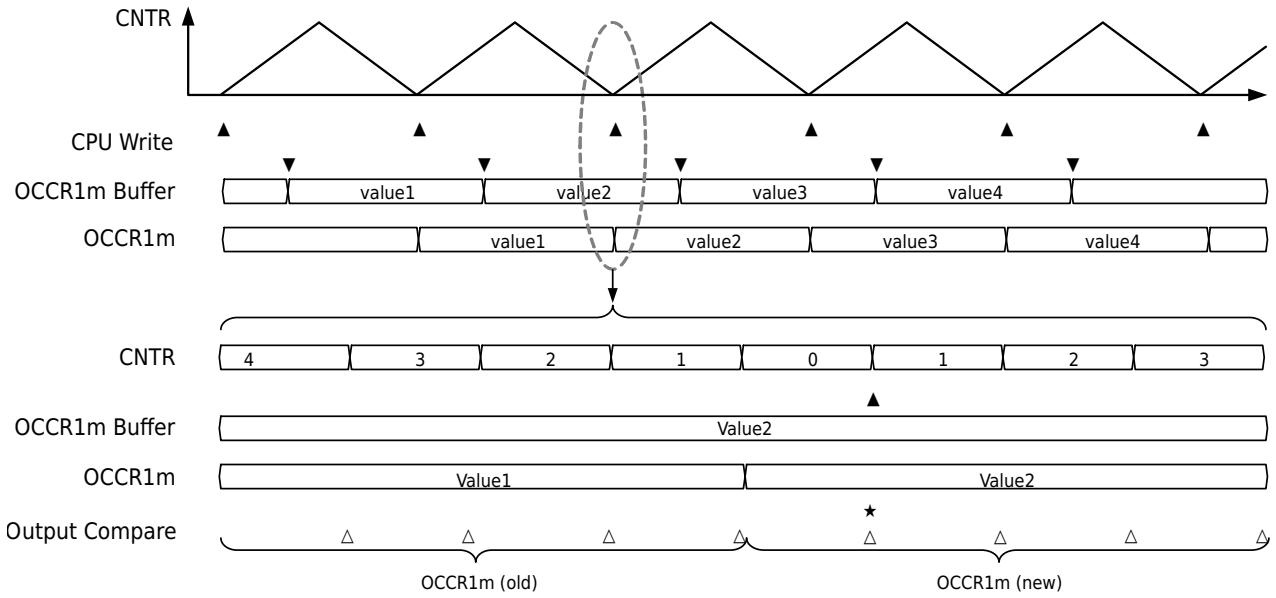

Figure 17-20 OCCR Buffer Data Transmission (Period Interval Response Link Disabled)

The upper part of the figure is a global schematic diagram, and the lower part is an enlarged view of the transmission operation.

The counter is in triangle wave counting mode, and the underflow interrupt is triggered at the flag ▲ (valley point). At ▼, the CPU rewrites the OCCR register and the data written is stored in the OCCR buffer register. After that, when the counter count is 0x0000, the data loading operation is performed, from the buffer register to the OCCR register, and the interrupt flag IRQZF is generated.

At △, the output comparison is based on the OCCR register value and counter value matching event, changing the PWM output and setting the OCSR.OCFx bit (x=L or H). After the ★ point (counter value=0x0000), the port output control operates based on the new OCCR data. Before the ★ point, the operation is based on the original OCCR data.

The figure illustrates the transmission operation of the OCCR buffer register at the counting valley point, and the buffer transfer operation of the OCMR buffer register is similar; similarly, the transmission operation at the counting peak point is also similar. New data becomes active immediately after the transmission time (newly written data will control the PWM output and set the interrupt flag).

2. **When the counter period interval response link is enabled, the buffer register transfer operation for the buffer value is executed when the counter is in the set counting state and the count value of the period interval counter is 0.**

   The figure below shows the waveform (x=L or H) when the general output compare OCCR (Take OCCR1m for example) buffer function is enabled, the counter is loaded at zero value (OCER.CxBUFEN=0b01), and the counter period interval response link is enabled (OCER.LMCx=1).

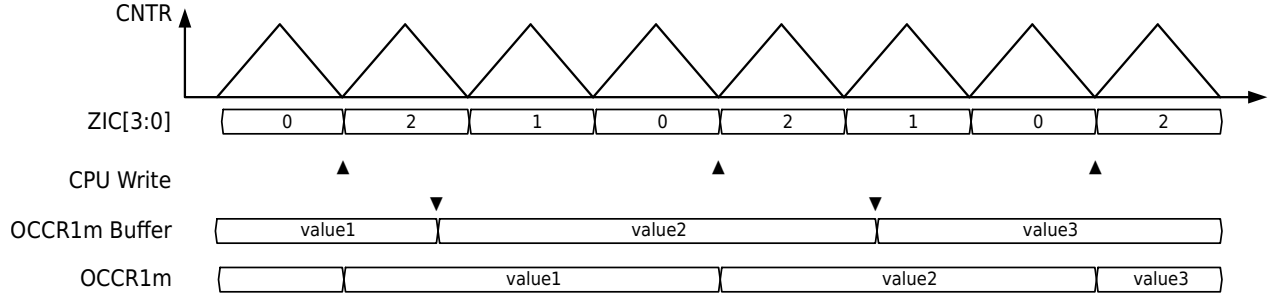

Figure 17-21 OCCR Buffer Data Transmission (Period Interval Response Link Enabled)

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The counter is in triangle wave counting mode, and the period interval counter (CVPR.ZIC) counts down from 2 to 0. The underflow interrupt is triggered at the flag ▲ (valley point). At ▼, the CPU rewrites the OCCR register, and the written data is stored in the OCCR buffer register. After that, when the counter count value is 0x0000 and the period interval counter (CVPR.ZIC) is 0, the data is loaded from the buffer register to the OCCR register, and the interrupt flag IRQZF is generated.

The figure shows the OCCR buffer register transfer operation at the counting valley point, and the OCMR buffer register transfer operation is similar. Similarly, the transfer operation at the counting peak is similar. The new data takes effect immediately after the transmission time (the new write data will control the PWM output and interrupt flag).

When using the channel link operation mode, enabling both the OCCRuh and OCCRul buffer functions can generate a variety of different PWM output waveforms. As shown in the figure below, while the output compare registers OCCRuh and OCCRul remain unchanged, changing the OCMR register value will make in_opul output different waveform signals.

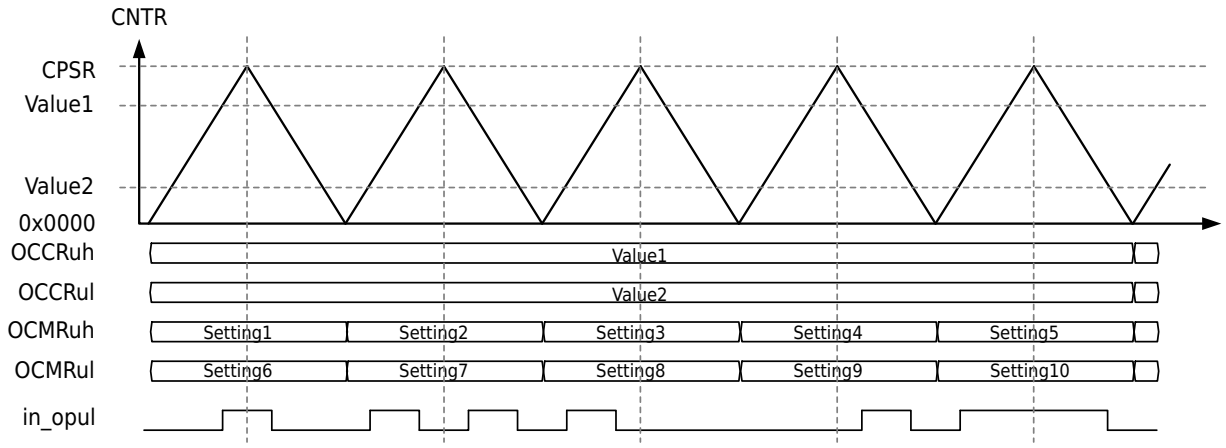

Figure 17-22 Output Compare Buffer Data Transfer (OCMR Buffer Enabled)

17.3.3.3 Special Compare Register Buffer Function

The SCCR register and SCMR register both have buffer function registers. When the buffer function is enabled, the values written by the CPU to the SCCR and SCMR buffer registers are loaded into the SCCR and SCMR registers at the set counter state.

1. **When the counter period interval response link transmission is disabled, the buffer transmission operation is solely related to the counter state and is not affected by the counter period interval counter.**

   The following figure illustrates the operation when the register buffer function is enabled, the counter period interval response link transmission is disabled (SCSR.LMC=0), and the counter is at zero value (SCSR.BUFEN=0b01), transferring data to the SCCR and SCMR registers.

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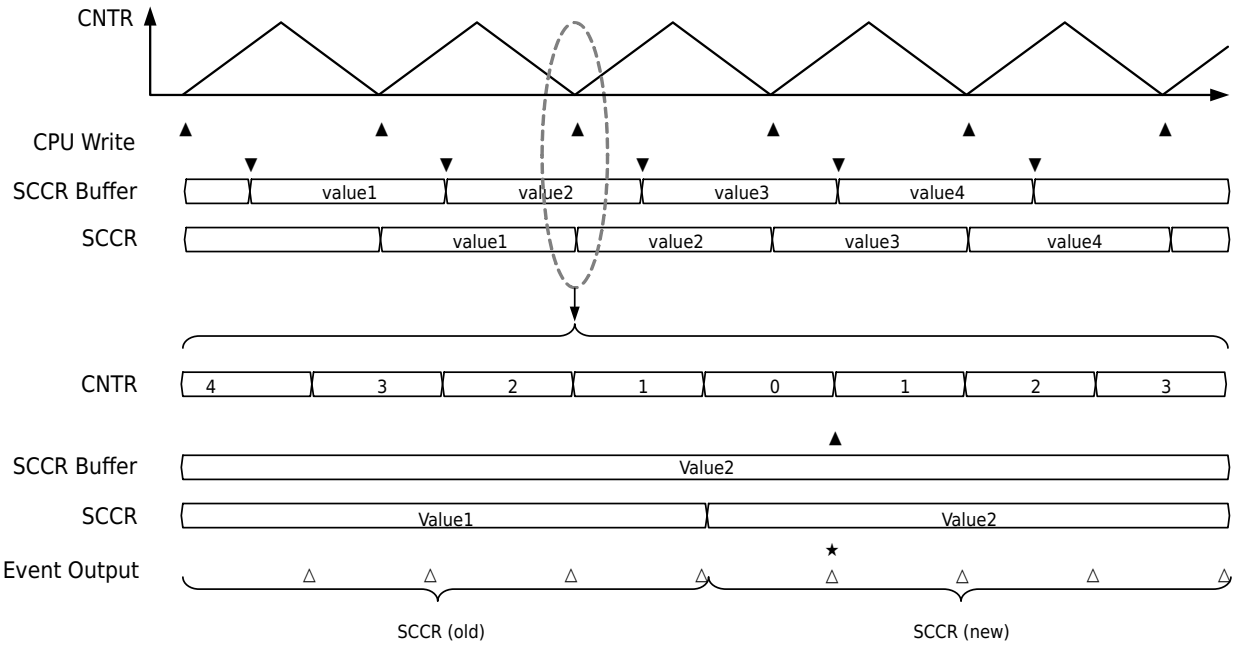

Figure 17-23 SCCR Buffer Transmission Operation (Period Interval Response Link Transmission Disabled)

The upper part of the figure is a global schematic diagram, and the lower part is a local enlarged diagram of the Buffer register transfer operation.

The counter is in triangle wave counting mode, and the underflow interrupt is triggered at the flag ▲ (valley point). At ▼, the CPU rewrites the SCCR register and the data written is stored in the SCCR buffer register. Afterwards, when the counter count value is 0x0000, the data loading operation is performed, and the data is transferred from the buffer register to the SCCR register, and the interrupt flag IRQZF is generated at the same time.

At time △, a comparison operation is performed based on the configured value in the SCCR register and the counter value. After time ★ (when the counter value equals 0x0000), the special event output signal operates according to the new SCCR data. Before the ★ point, the operation is based on the original SCCR data.

The figure illustrates the transmission operation of the SCCR buffer register at the counting valley point, and the buffer transfer operation of the SCMR buffer register is similar; similarly, the transmission operation at the counting peak point is also similar. The new data takes effect immediately after the transmission moment (the newly written data will set the special event output signal and interrupt flag).

2. **When the counter period interval response link is enabled, the buffer register transfer operation is executed when the buffer value is in the set counting state and the count value of the period interval counter is 0.**

   The following figure shows the schematic diagram of enabling the SCCR buffer function, loading the counter at zero value (SCSR.BUFEN=0b01), and enabling the counter periodic interval response link transmission (SCSR.LMC=1).

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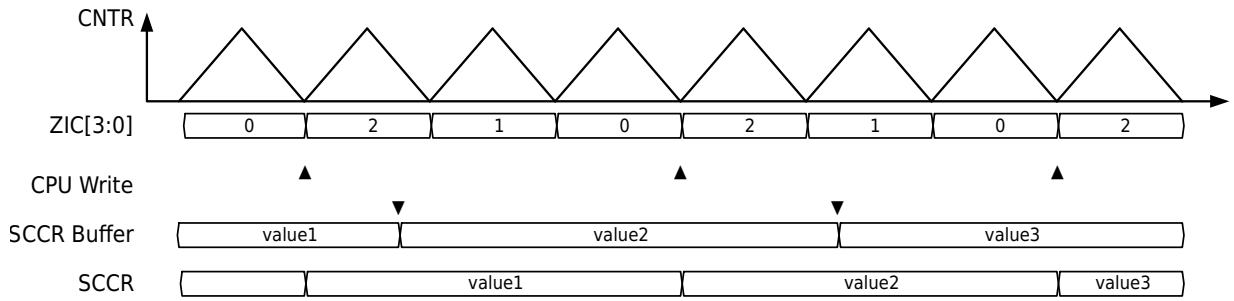


Figure 17-24 SCCR Buffer Transmission Operation (when Periodic Interval Response Link Transmission Enabled)

The counter is in triangle wave counting mode, and the period interval counter (CVPR.ZIC) counts down from 2 to 0. The underflow interrupt is triggered at the flag ▲ (valley point). At ▼, the CPU rewrites the SCCR register and the data written is stored in the SCCR buffer register. After the counter value reaches 0x0000 and the period interval counter (CVPR.ZIC) is 0, the data load operation occurs, and the data is transferred from the buffer register to the SCCR register, triggering the interrupt flag IRQZF.

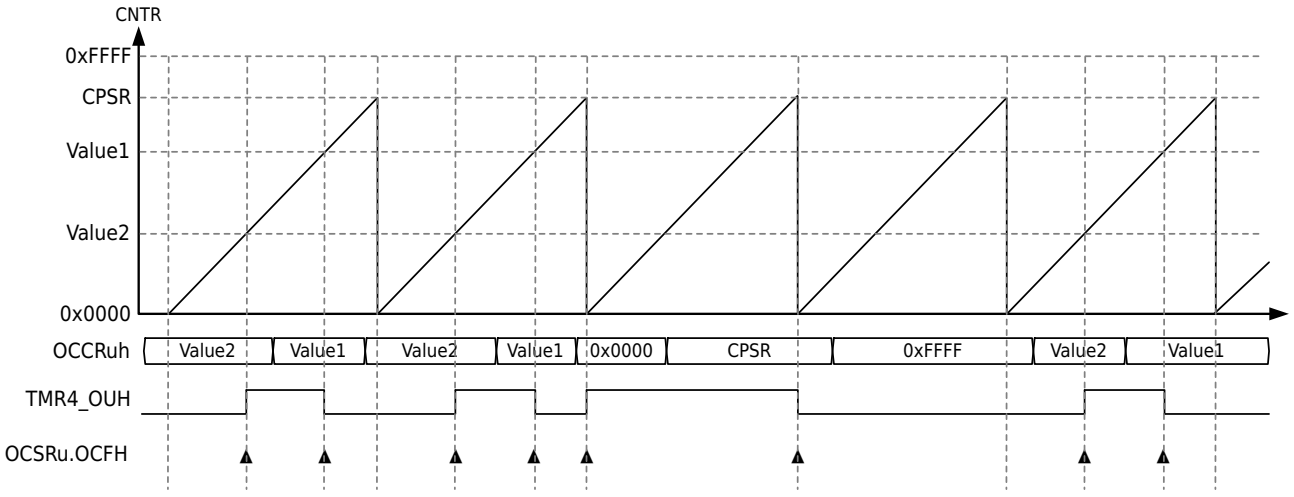
17.3.4 General PWM Output

17.3.4.1 Overview

When OCCR*h, OCCR*l, OCMR*h, OCMR*l, PSCR.OE*H, PSCR.OE*L, PDAR*, PDBR*, PSCR.OS*H, PSCR.OS*L, and OCER* are mentioned later in this section, the wildcard character "* " represents u, v, w, x; when referring to internal output signals in_op*h, in_op*l, the wildcard character "*" represents u, v, w, x; when referring to ports TMR4_O*H, TMR4_O*L, the wildcard character "*" represents U, V, W, X. OCCR*l and OCMR*h represent the actually compare reference value.

17.3.4.2 Independent PWM Output

In the pass-through mode (POCR.PWMMD=0b00), the references of OCCR*h and OCCR*l and the port output states of OCMR*h and OCMR*l are set respectively to achieve different PWM outputs. At this time, the PWM output of each port is controlled independently. Before using the independent PWM output mode, you need to set the MOE, OE*H, OE*L bits (PSCR register) to enable the output of Timer4. For detailed description, please refer to "PWM Status Control Register (TMR4_PSCR)". The following two figures are examples of independent PWM output under sawtooth wave and triangle wave of unit 1.



OCMRuh.OCFUCH=OCMRuh.OCFZRH=OCMRuh.OCFPKH=0b1
OCMRuh.OPZRH=OCMRuh.OPUCH=OCMRuh.OPPKH=0b11
Write 0 to the rest bits of the OCMRuh register

Figure 17-25 Sawtooth Independent PWM Output Example

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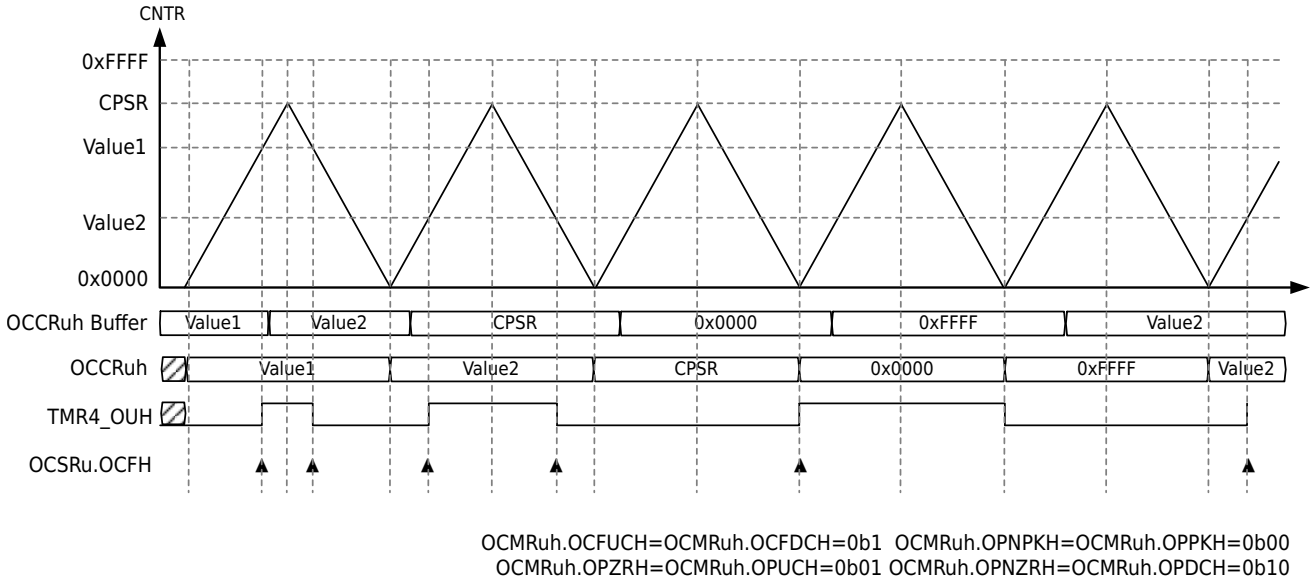

Figure 17-26 Triangle Independent PWM Output Example

Note

The pass-through mode means that the internal output signal (in_op*h, in_op*l) generated by the comparison match of the value of the general compare reference register (OCCR*h, OCCR*l) is directly output to the corresponding port (TMR4_O*H, TMR4_O*L).

17.3.4.3 Extended PWM Output

In pass-through mode (POCR.PWMMD=0b00), the port output status of TMR4_O*L can also be determined by the extension bit (Bit31-16) in the OCMR*l register. The setting of this extension bit is related to the OCCR*h reference, thereby realizing extended PWM output on the TMR4_O*L port. Before using the extended PWM output mode, you need to set the MOE, OE*H, OE*L bits (PSCR register) to enable the output of Timer4. For detailed description, please refer to the "PWM Status Control Register (TMR4_PSCR)". The figure below shows the PWM output of TMR4_OUH and TMR4_OUL ports in this mode.

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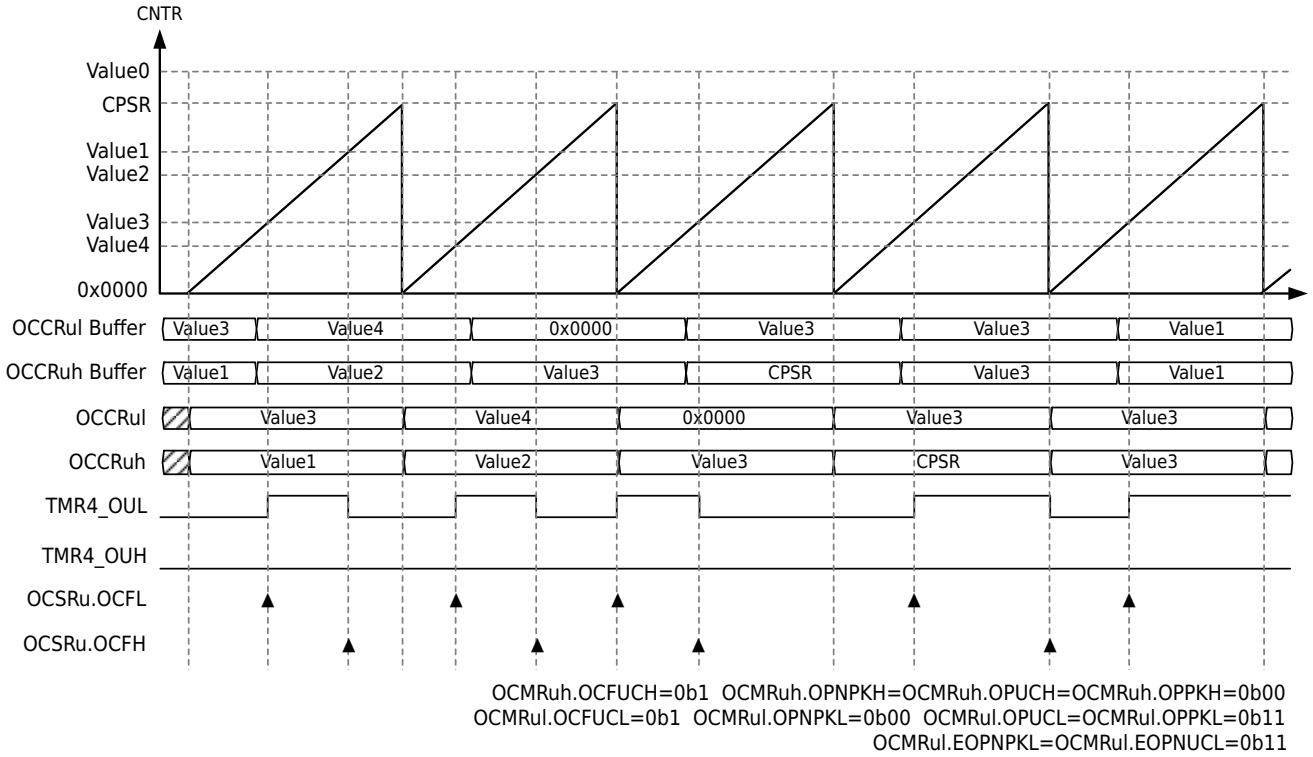

Figure 17-27 Sawtooth Wave Extended PWM Output

Note

In independent PWM output mode, the port status of TMR4_O*L is determined by Bit15-Bit4 of the OCMRxl register and is only related to the OCCR*l reference.

17.3.4.4 Complementary PWM Output

Software Setting for Complementary PWM Output

In the pass-through mode (POCR.PWMMD=0b00), directly set the OCCR*h and OCCR*l references to realize a pair of complementary PWM waveforms output to the port. The same setting of 4 groups of ports can realize 4-phase complementary PWM output.

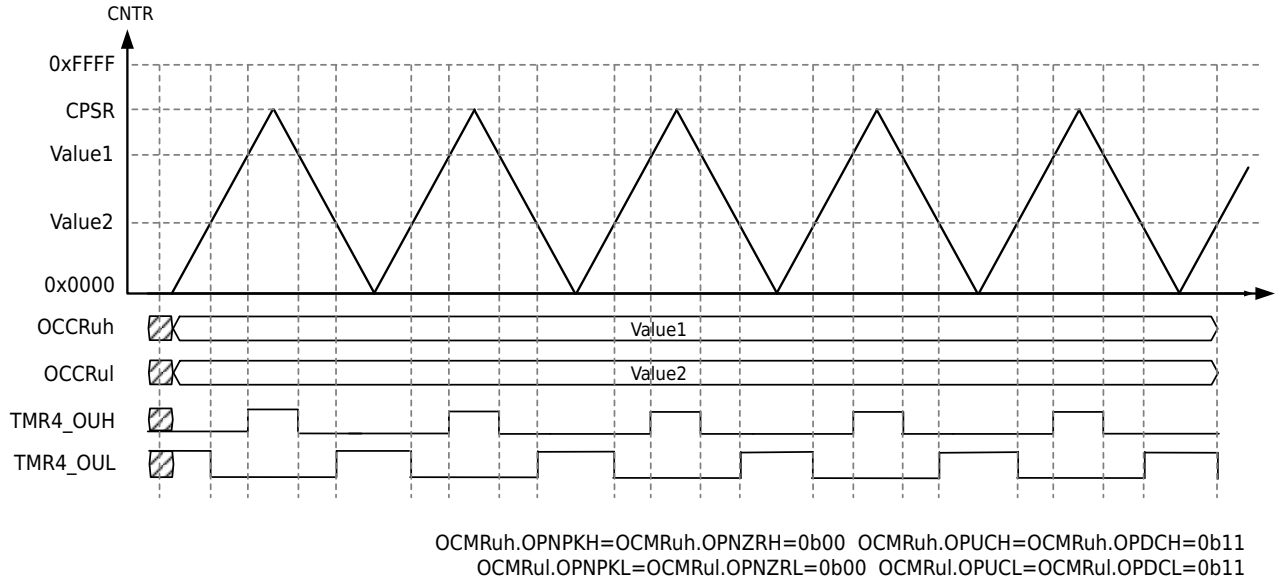

Figure 17-28 Software Implementation of Complementary PWM Output

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Hardware Implementation of Complementary PWM Output

In the dead-zone generator mode (POCR.PWMMD=0b01), the internal output signal (in_op*l) generated by a comparison match of the general compare control register (OCCR*l) and the set values in the PWM dead-zone control registers (PDAR/PDBR) are used to generate complementary PWM output through hardware, with timing offsets.

In this mode, the polarity of the output of the TMR4_O*H port is the same as that of in_op*l, and the polarity of the output of the TMR4_O*L port is opposite to that of in_op*l. The figure below is an example of complementary PWM output in dead-zone timer mode.

If the rising edge of in_op*l is detected, the TMR4_O*L output becomes low level, and the dead zone counter loads the set value of the PDBR* register and starts counting down. When the count value becomes 0x0000, the counter stops and TMR4_O*H outputs high level; If the falling edge of in_op*l is detected, the TMR4_O*H output becomes low level, and the dead zone counter loads the set value of the PDAR* register and starts counting down. When the count value becomes 0x0000, the counter stops and makes TMR4_O*L output high level.

By setting the PWM dead zone control registers PDAR and PDBR, the dead zone time of output rise and fall changes can be set accordingly.

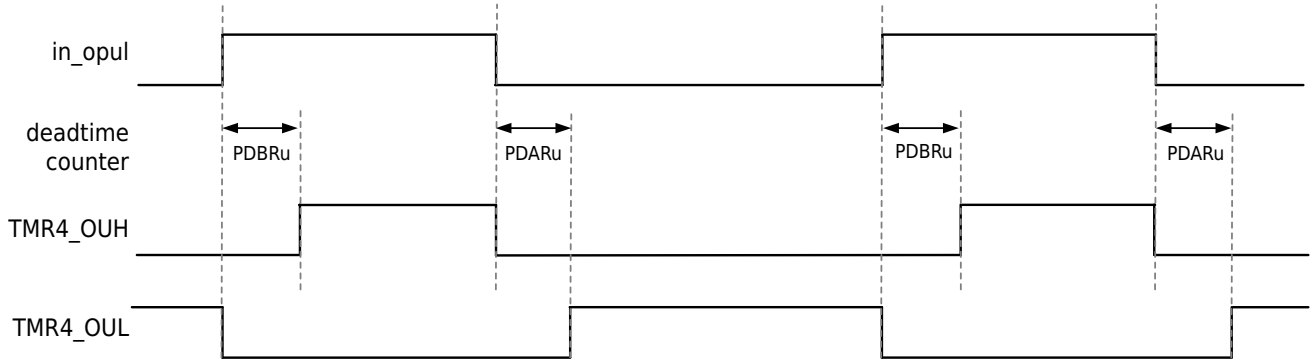

Figure 17-29 Complementary PWM Output in Dead-Zone Generator Mode

When the high-level pulse width of in_op*l is less than the dead time set by PDBR, only the TMR4_O*L output becomes low level. The condition for the TMR4_O*L output level to become high is when the dead time set by the PDAR register has passed after the falling edge of in_op*l. In this case, the TMR4_O*H output will continue to remain at a low level.

When the low level pulse width of in_op*l is less than the dead time set by PDAR, only the TMR4_O*H output becomes low level. The condition for the TMR4_O*H output level to become high is after the dead time set by the PDBR register after the rising edge of in_op*l. In this case, the TMR4_O*L output will continue to remain at a low level. As shown in the figure below.

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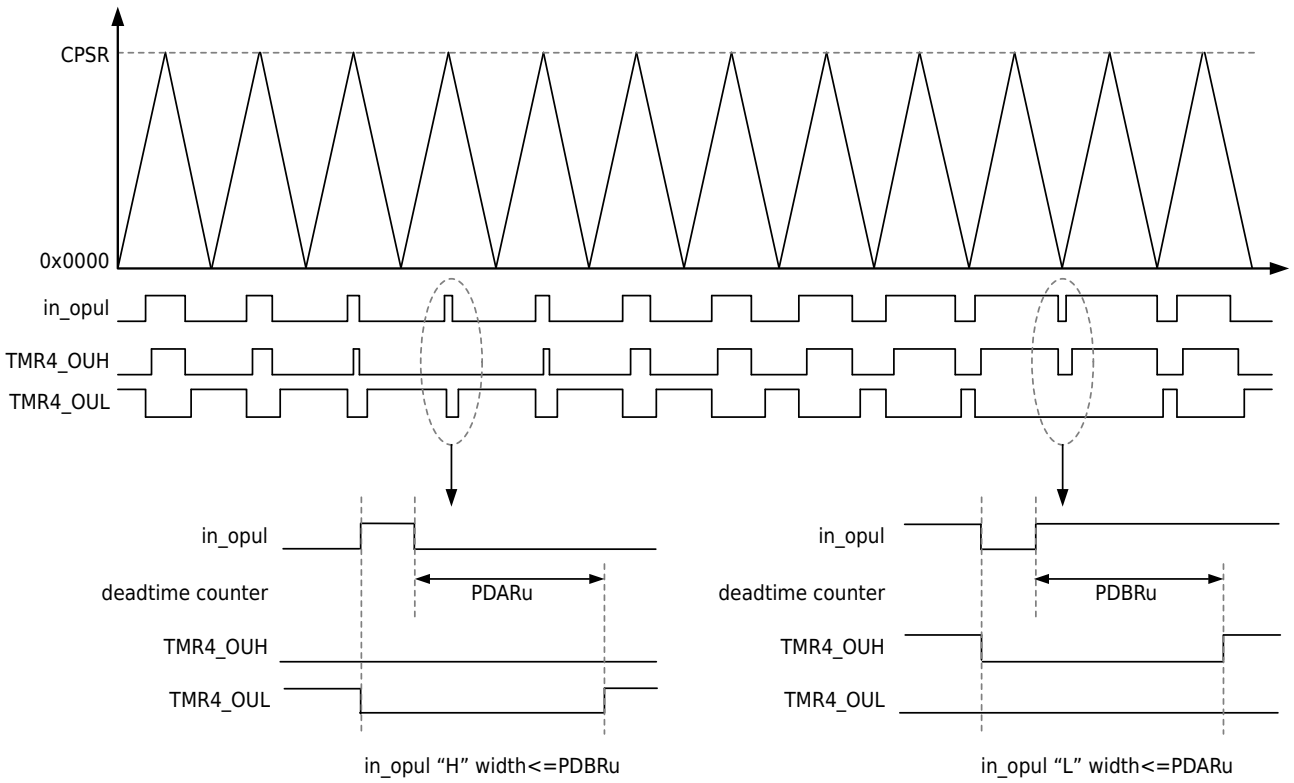

Figure 17-30 Waveform Output in Dead-Zone Timer Mode with Pulse Width Anomalies

Based on the hardware implementation of dead-zone output, pulse width monitoring can also be applied to the internal compare match signal (in_op*l), enabling filtering control of the in_op*l signal. This method, where the in_op*l signal undergoes pulse width filtering, is called the Dead-Zone Counter Filter Mode (POCR.PWMMD=0b10).

In the Dead-Zone Counter Filter Mode, the filter width is determined by the value set in the PFSR register. When the pulse width of in_op*l exceeds the time set in the PFSR register, the filter counter will delay the in_op*l signal by the time set in PFSR before outputting it. The output will then follow the dead-zone timer mode to generate complementary PWM signals.

If the rising edge of the signal in_op*l is detected, the filter counter loads the PFSR register value and starts measuring the high level width of in_op*l. When the high level pulse width of in_op*l is greater than the time set by the register PFSR, after the time set by PFSR, the TMR4_O*L output becomes low level, and the dead zone counter loads the set value of the PDBR register and starts counting down. When the count value becomes 0x0000, the counter stops and makes TMR4_O*H output high level. If the falling edge of the signal in_op*l is detected, the filter counter loads the PFSR register value and starts to measure the low-level width of in_op*l. When the low-level pulse width of in_op*l is greater than the time set by the register PFSR, after PFSR After the set time, the TMR4_O*H output becomes low level, and the dead zone counter loads the set value of the PDAR register and starts counting down. When the count value becomes 0x0000, the counter stops and makes TMR4_O*L output high level. When the level pulse width of in_op*l is less than the time set by PFSR register, the outputs TMR4_O*H and TMR4_O*L will remain unchanged.

The following figure shows an example of complementary PWM output in dead-zone counter filter mode.

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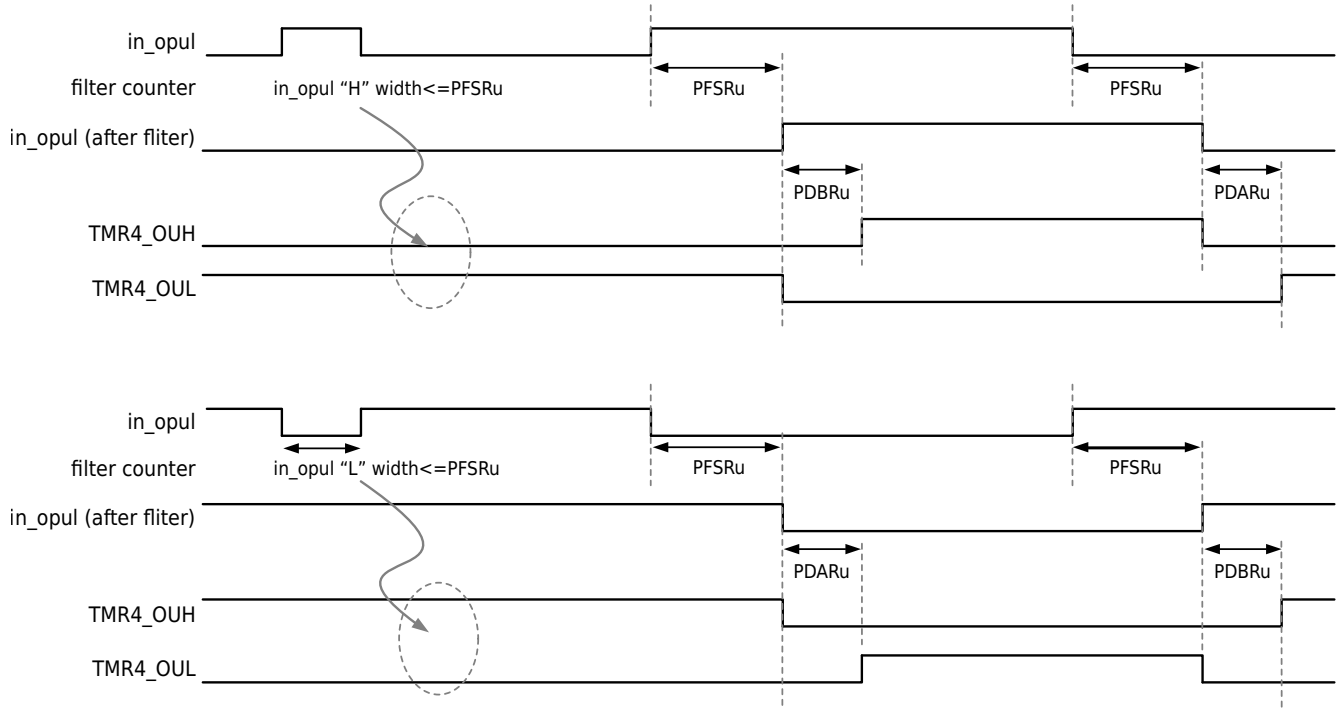

Figure 17-31 Complementary PWM Output in Dead-Zone Timer Filter Mode

Note

Before using software or hardware complementary PWM output mode, you need to set the MOE, OE*H, OE*L bits (PSCR register) to enable the output of Timer4. For detailed description, please refer to the "PWM Status Control Register (TMR4_PSCR)".

17.3.5 Periodic Interval Response

The underflow interrupt mask counter is used to reduce (mask) the number of times the underflow flag (CCSR.IRQZF) is set. The underflow interrupt mask counter (CVPR.ZIC) operates as a down counter and is loaded with the value set by CVPR.ZIM at the beginning. When CVPR.ZIC=0, the underflow flag (CCSR.IRQZF) is set to 1.

The overflow interrupt mask counter is used to reduce (mask) the number of times the overflow flag (CCSR.IRQPF) is set. The overflow interrupt mask counter (CVPR.PIC) operates as a down counter and is loaded with the value set by CVPR.PIM at the beginning. When CVPR.PIC=0, the overflow flag (CCSR.IRQPF) is set to 1.

The figure below is the setting timing diagram of IRQZF and IRQPF in periodic interval response.

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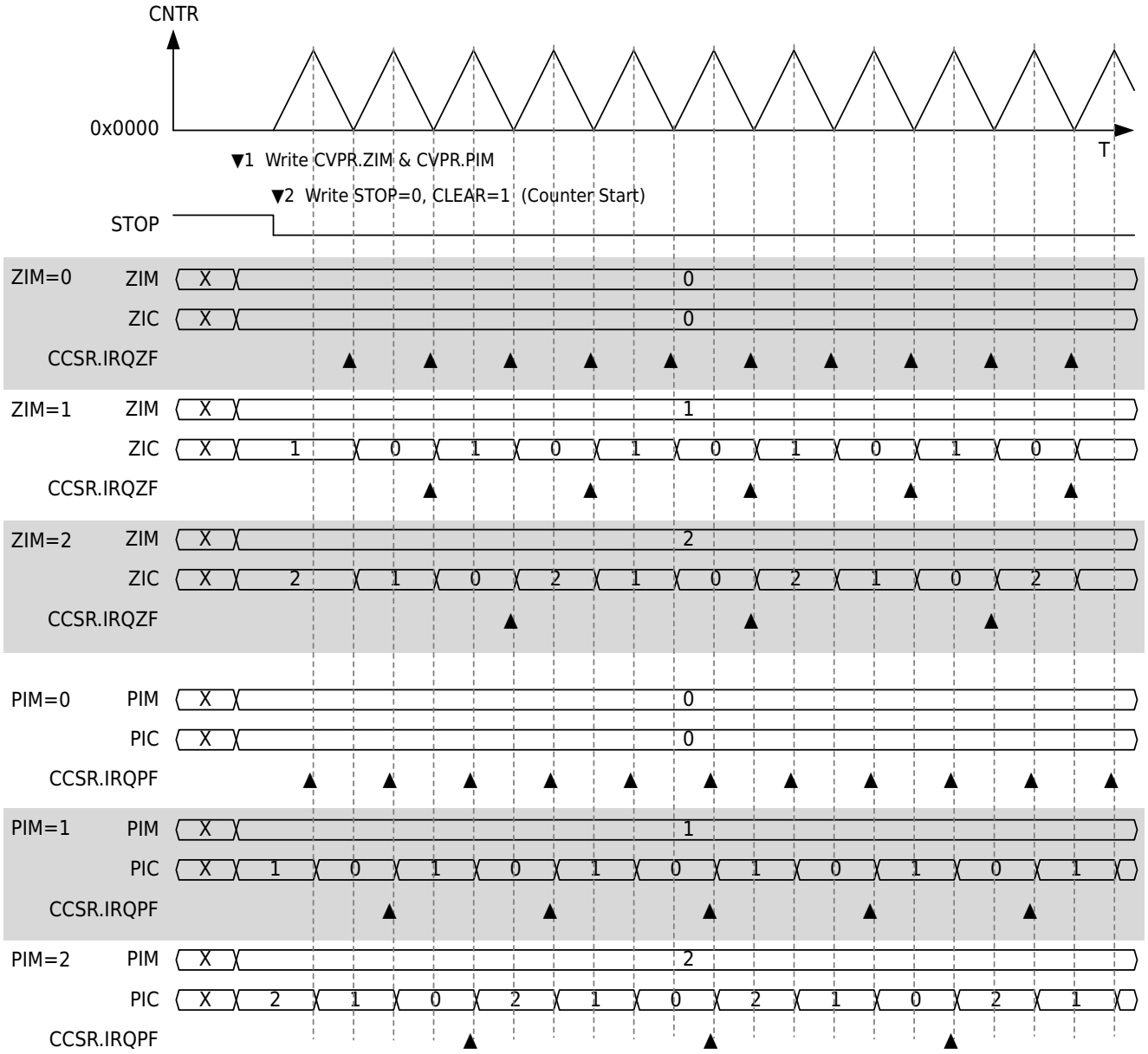

Figure 17-32 Periodic Interval Response Timing Diagram

Note

- When the counter is stopped, write the initialization values of CVPR.ZIM and CVPR.PIM, and the initial values are immediately reflected in the internal counters (CVPR.ZIC, CVPR.PIC).
- Initialize and start the counter (STOP=0 and CLEAR=1). The counter starts counting up from zero after the bus is reset or CLEAR=1 is initialized from software. At this moment, the CCSR.IRQZF flag is not set immediately. After that, whenever the count value of the interrupt mask counter is 0x0000 and the count value of the counter is 0x0000 and CPSR, the flag ▲ is the moment when CCSR.IRQZF or CCSR.IRQPF is set.
- When the counter is running, if CVPR.ZIM and CVPR.PIM are written, the set value will not be immediately reflected in the interrupt mask counter (CVPR.ZIC and CVPR.PIC). If a soft reset (CLEAR=1) is written, the written CVPR.ZIM and CVPR.PIM values will be immediately loaded as the initial values of the interrupt mask counter.

The compare match event (special event output) of the SCCRm register also has a period interval response function. The figure below shows the periodic interval response output of the special event output signal.

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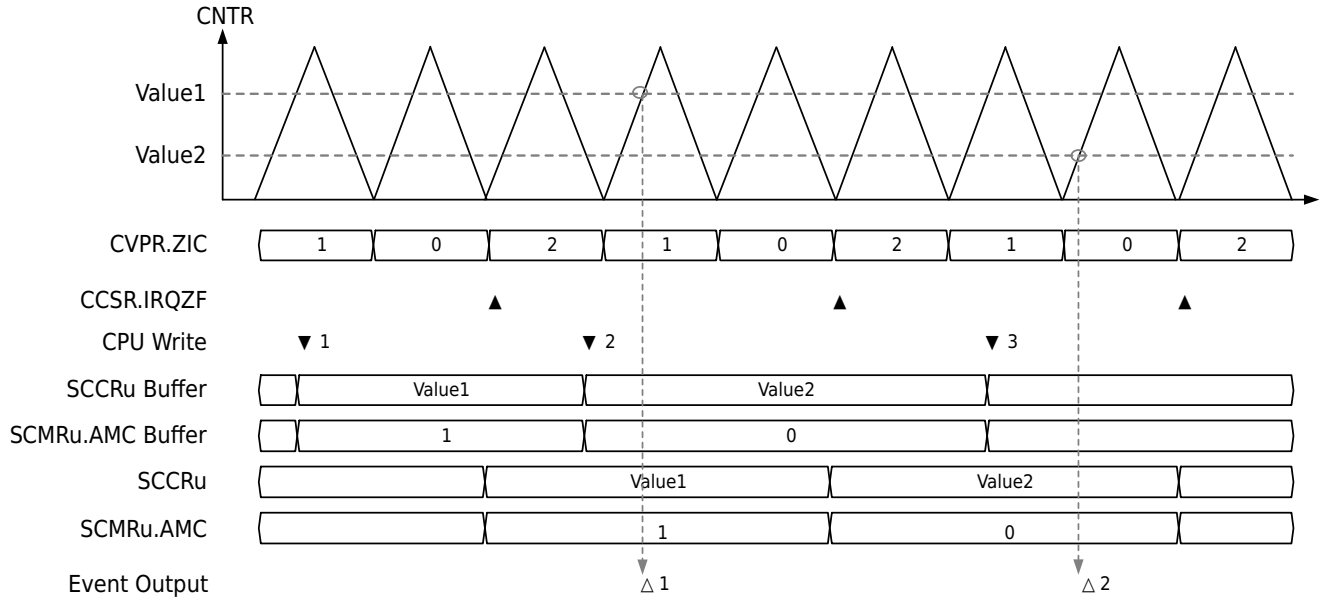

Figure 17-33 Special Event Output Signal Periodic Interval Response Output

The counter is in triangle wave counting mode, and the underflow interrupt mask counter (CVPR.ZIC) counts down from 2-0. An underflow interrupt is generated at time ▲.

At time ▼1, value1 is written to the SCCRu buffer register. Meanwhile, MZCE=1, MPCE=0, AMC=0001 are written to the SCMRu buffer register. After that, the buffer registers SCCRu and SCMRu transfer operations are performed at time ▲. Because MZCE=1 and AMC=1 and the count value=SCCRu=Value1, at time △1, the special event output signal is set.

At time ▼2, value2 is written to the SCCRu buffer register. Meanwhile, MZCE=1, MPCE=0, AMC=0000 are written to the SCMRu buffer register. After that, the buffer registers SCCRu and SCMRu transfer operations are performed at time ▲. Because MZCE=1 and AMC=0 and the count value=SCCRu=Value2, at time △2, the special event output signal is set.

17.3.6 EMB Control

Timer 4 unit has an output inactive event interface connected to the EMB event output from the EMB module. The abnormal condition event selected on this interface can be set from the EMB side (refer to the "Emergency Brake Module (EMB) " chapter).

During the normal output period of the 4 groups of PWM ports in unit, if the EMB abnormal event from the EMB is detected, the PSCR.MOE bit is cleared asynchronously by hardware, and the output state of each PWM port changes to the preset state. According to the settings of PSCR.OS*H and PSCR.OS*L, the preset port state can be output high impedance, output low level or output high level.

For example, if PSCR.OSUH=0b01 is set, an EMB event is generated during the normal output period of the TMR4_OUH port of Timer4, and the output on the TMR4_OUH port changes to a high impedance state.

After the condition that triggers the EMB abnormal event is disabled, the user can clear the EMB exception event by writing the EMB_STATCLR0 register. If PSCR.AOE=1 at this time, the PSCR.MOE bit will be automatically set by hardware at the next count underflow point (the underflow point here is the actual count zero point of the counter, which is not affected by the set value of the register CVPR), and then the PWM port will resume normal output; if PSCR.AOE=0 at this time, PSCR.MOE needs to be set by software to restore the PWM port to normal output.

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It should be noted that the asynchronous signal of MOE is used to control the PWM output enable in hardware. When the value of MOE changes, it is necessary to wait for several clock periods to read the actual value on the bus (it is necessary to wait for 4 Timer4 bus clock periods after the EMB abnormal event occurs, and it is necessary to wait for 6 Timer4 bus clock periods after the EMB abnormal event is resolved).

For detailed operation methods of EMB, please refer to the relevant description of the "Emergency Brake Module (EMB)" chapter.

17.3.7 Monitoring Output

Timer4 unit has a PWM period output monitoring port TMR4_PCT and a special event output monitoring port TMR4_ADSM. These monitoring ports are output to the outside, and users can flexibly control the application system based on the port change information.

The PWM period output monitoring port TMR4_PCT is used to monitor the current counter count state. In the triangle wave mode, each time the count reaches the peak or trough, a flip occurs on the monitoring port TMR4_PCT. The following figure is an example of the counting direction signal.

The period output monitoring function of the TMR4_PCT port is only used when the counting clock is not divided (CCSR.CKDIV=0x0).

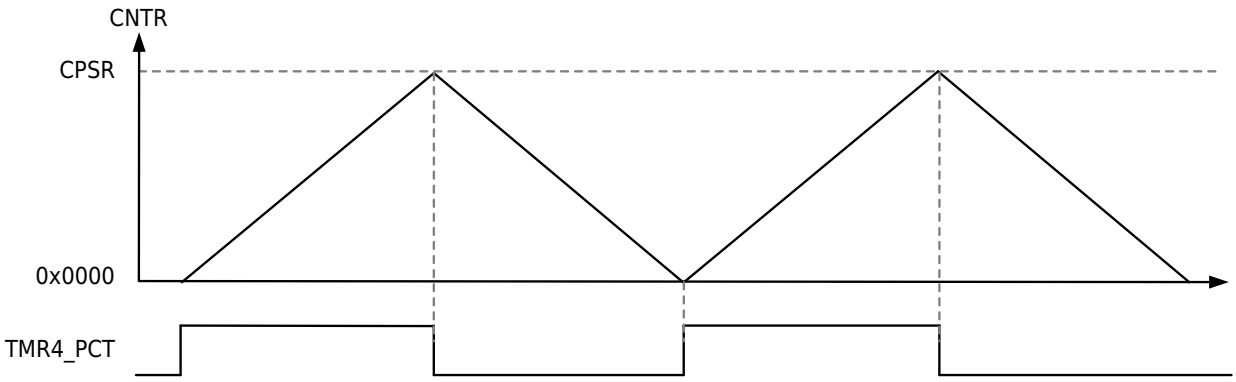

Figure 17-34 PWM Period Output Monitoring Example

The special event output monitoring port TMR4_ADSM can be used to monitor the special comparison event of the internal counter. Select the special comparison output channel that needs to be monitored through the SCER.EVTRS bit. When the compare reference on this channel and the counter produce a comparison match, the monitoring port TMR4_ADSM will be set (the output is high); when the counter count on this channel returns to zero (the sawtooth wave overflows and the triangle wave counts to the trough), the monitoring port TMR4_ADSM will be reset (the output is low).

It should be noted that when the configuration register TMR4_SCSRm enables both up-counting EVT and down-counting EVT (TMR4_SCSRm.UEN=1 and TMR4_SCSRm.DEN=1), the synchronization signal output to the external port is only active for up-counting EVT.

The following figure shows an example of the synchronized signal output to the port in comparison start mode (SCSRm.EVTMS=0). After the EVT is enable in up-counting mode, TMR4_ADSM is set. After the counter underflows, TMR4_ADSM is cleared.

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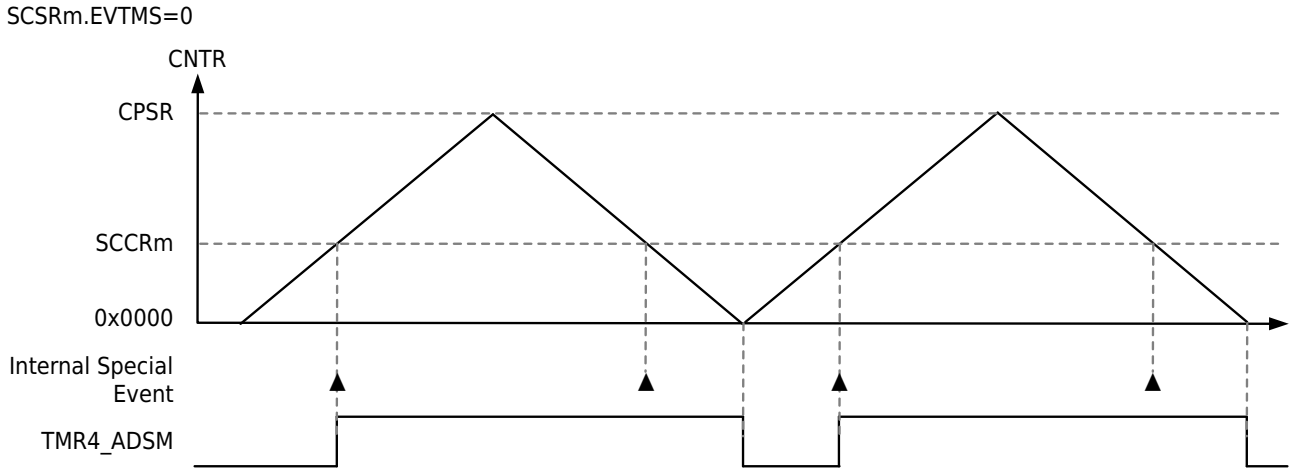

Figure 17-35 Special Event Output TMR4_ADSM Timing in Compare Start Mode

17.3.8 Hardware Startup

Timer4 can implement the counter startup function through internal hardware trigger events.

Timer4 has an internal hardware trigger source. The event source can be selected by setting the corresponding number in the hardware trigger event selection register. For details of the register content, please refer to the "Timer4 Hardware Trigger Event Selection Register (TMR4_TRGSEL)" section of "Automatic Operation System (AOS) ". For specific event correspondence, please refer to the "Interrupt Controller (INTC) " section. When using the internal hardware trigger function, it is necessary to set the peripheral circuit trigger function enable bit of CMU_FCG to 1 first.

17.3.9 Synchronous Starting

This product is configured with a TMR_SYNENR Register for synchronizing the start of the Timers included in the product (Timer0, Timer4, TimerA). For usage and register description, refer to the "General Timer (Timer0)" chapter. Do not use this function when this timer is counting asynchronously.

17.3.10 Interrupt and Event

General Count Compare Match Interrupt and Event

There are a total of 8 OCCRm registers, each of which can generate a compare match enable signal when matched with the counter value. When the count compare matches, the OCSRn.OCFH and OCSRn.OCFL bits in the OCSRn register will be set to 1 respectively. At this time, if OCSRn.OCIEH and OCSRn.OCIEL are set to enable interrupts, the corresponding interrupt request (TMR4_GCMmn, m=U, V, W, X; n=H, L) will also be triggered.

The general count compare match event can be used to trigger other modules. For the event number, please refer to the "Interrupt Event List" in the "Interrupt Controller (INTC) " chapter.

Count Period Match Interrupt and Event

When the sawtooth wave counts to the overflow point or underflow point, the triangle wave counts to the valley point or peak point, the CCSR.IRQPF or CCSR.IRQZF bit will be set to 1. At this time, if the CCSR.IRQPEN or CCSR.IRQZEN bit is set to enable interrupt, the count period match interrupt (TMR4_GOVF and TMR4_GUDF) can be triggered at the corresponding time point.

The count period match event can be used to trigger other modules. For event numbers, refer to the "Interrupt Event List" in the "Interrupt Controller (INTC) " chapter.

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Reload Count Match Interrupt and Event

When the reload function is enabled, TMR4_PFSRn serves as the period count value for the reload timer. When counting is enabled, the counter is reloaded with the value in TMR4_PFSRn and performs a decrement operation. After completing one period, a reload count interrupt request is generated, the RCSR.RTIFU, RCSR.RTIFV, RCSR.RTIFW, and RCSR.RTIFX bits are set to 1, respectively. If the interrupt masks RCSR.RTIDU, RCSR.RTIDV, RCSR.RTIDW, and RCSR.RTIFX are disabled, the corresponding reload compare match interrupt requests (TMR4_RLOm, where m=U, V, W, X) will be triggered.

Reload compare match events can be used to trigger other modules; for the event numbers, refer to the "Interrupt Event List" in the "Interrupt Controller (INTC) " chapter.

Special Compare Match Interrupts and Events

The 8 SCCRm registers of Timer4 generate 8 special event output signals corresponding to them, which can be used to select and trigger other modules, such as starting the ADC.

During the clock counting process, if the SCCRm register has a count comparison match event , a corresponding enable request signal will be generated. This request signal can be assigned to any EVT event output signal (configured via the SCSR.EVTOS bit) to trigger other modules. At this time, if SCIR.ITEN0-7 is set to enable interrupt, the corresponding special compare match interrupt request (TMR4_SCM0-7) will also be triggered.

The output of this event request signal can be configured for either Comparison Start Mode or Delay Start Mode. In comparison start mode (SCSR.EVTMS=0), after the count compare match event of SCCR is generated, the special event output signal is directly output; in delay start mode (SCSR.EVTMS=1), after the count compare match event of OCCR*h or OCCR*l (selected by SCSR.EVTDS bit) is generated, the special event output signal is output after the reference period time set by SCCR. The figure below illustrates an example of the event request signal output in Delay Start Mode.

Special compare match events can be used to trigger other modules. For event numbers, please refer to the "Interrupt Event List" in the "Interrupt Controller (INTC) " chapter.

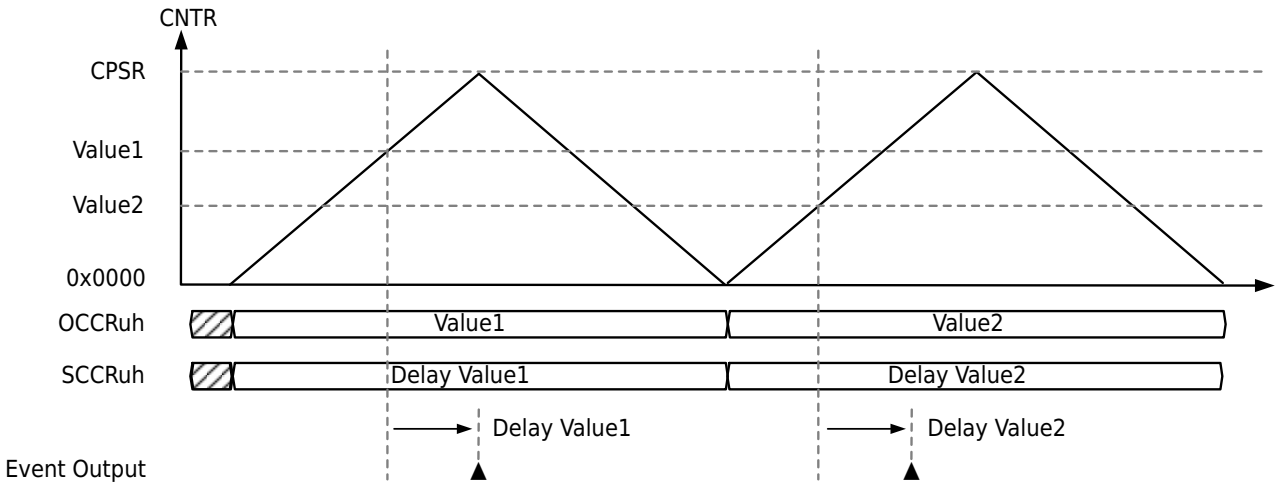

Figure 17-36 Output Timing of Special Event Output Signal in Delayed Start Mode

Note

During delay counting, if another match event between OCCR and the counter occurs, the delay counter reloads and begins decrementing again. Therefore, if the interval between OCCR match events is shorter than the delay period defined by SCCR, the special event output request signal may never be generated.

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17.4 Register Description

17.4.1 Register List

Base address: 0x40017000

Table 17-3 General Control Timer (Timer4) Register Offset

Offset	Register	Description	Width
0x0054	TMR4_CNTR	Count Value Register	16
0x0050	TMR4_CPSR	Period Value Register	16
0x0058	TMR4_CCSR	Control Status Register	16
0x005A	TMR4_CVPR	Valid Period Register	16
0x0070	TMR4_CPCR	Period Control Register	16
0x0000	TMR4_OCCR1uh	General Compare Reference Register 1UH	16
0x0002	TMR4_OCCR2uh	General Compare Reference Register 2UH	16
0x0100	TMR4_OCCR3uh	General Compare Reference Register 3UH	16
0x0004	TMR4_OCCR1ul	General Compare Reference Register 1UL	16
0x0006	TMR4_OCCR2ul	General Compare Reference Register 2UL	16
0x0104	TMR4_OCCR3ul	General Compare Reference Register 3UL	16
0x0008	TMR4_OCCR1vh	General Compare Reference Register 1VH	16
0x000A	TMR4_OCCR2vh	General Compare Reference Register 2VH	16
0x0108	TMR4_OCCR3vh	General Compare Reference Register 3VH	16
0x000C	TMR4_OCCR1vl	General Compare Reference Register 1VL	16
0x000E	TMR4_OCCR2vl	General Compare Reference Register 2VL	16
0x010C	TMR4_OCCR3vl	General Compare Reference Register 3VL	16
0x0010	TMR4_OCCR1wh	General Compare Reference Register 1WH	16
0x0012	TMR4_OCCR2wh	General Compare Reference Register 2WH	16
0x0110	TMR4_OCCR3wh	General Compare Reference Register 3WH	16

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Offset	Register	Description	Width
0x0014	TMR4_OCCR1wl	General Compare Reference Register 1WL	16
0x0016	TMR4_OCCR2wl	General Compare Reference Register 2WL	16
0x0114	TMR4_OCCR3wl	General Compare Reference Register 3WL	16
0x0018	TMR4_OCCR1xh	General Compare Reference Register 1XH	16
0x001A	TMR4_OCCR2xh	General Compare Reference Register 2XH	16
0x0118	TMR4_OCCR3xh	General Compare Reference Register 3XH	16
0x001C	TMR4_OCCR1xl	General Compare Reference Register 1XL	16
0x001E	TMR4_OCCR2xl	General Compare Reference Register 2XL	16
0x011C	TMR4_OCCR3xl	General Compare Reference Register 3XL	16
0x0020	TMR4_OCSRu	General Control Status Register U	16
0x0024	TMR4_OCSRv	General Control Status Register V	16
0x0028	TMR4_OCSRw	General Control Status Register W	16
0x002C	TMR4_OCSRx	General Control Status Register x	16
0x0022	TMR4_OCERu	General Extended Control Register U	16
0x0026	TMR4_OCERv	General Extended Control Register V	16
0x002A	TMR4_OCERw	General Extended Control Register W	16
0x002E	TMR4_OCERx	General Extended Control Register X	16
0x0030	TMR4_OCMRuh	General Mode Control Register UH	16
0x0034	TMR4_OCMRul	General Mode Control Register UL	32
0x0038	TMR4_OCMRvh	General Mode Control Register VH	16
0x003C	TMR4_OCMRvl	General Mode Control Register VL	32
0x0040	TMR4_OCMRwh	General Mode Control Register WH	16
0x0044	TMR4_OCMRwl	General Mode Control Register WL	32
0x0048	TMR4_OCMRxh	General Mode Control Register XH	16
0x004C	TMR4_OCMRxl	General Mode Control Register XL	32
0x00B0	TMR4_SCCRuh	Special Compare Reference Register UH	16

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Offset	Register	Description	Width
0x00B4	TMR4_SCCRul	Special Compare Reference Register UL	16
0x00B8	TMR4_SCCRvh	Special Compare Reference Register VH	16
0x00BC	TMR4_SCCRvl	Special Compare Reference Register VL	16
0x00C0	TMR4_SCCRwh	Special Compare Reference Register WH	16
0x00C4	TMR4_SCCRwl	Special Compare Reference Register WL	16
0x00C8	TMR4_SCCRxh	Special Compare Reference Register XH	16
0x00CC	TMR4_SCCRxl	Special Compare Reference Register XL	16
0x00D0	TMR4_SCSRuh	Special Control Status Register UH	16
0x00D4	TMR4_SCSRul	Special Control Status Register UL	16
0x00D8	TMR4_SCSRvh	Special Control Status Register VH	16
0x00DC	TMR4_SCSRvl	Special Control Status Register VL	16
0x00E0	TMR4_SCSRwh	Special Control Status Register WH	16
0x00E4	TMR4_SCSRwl	Special Control Status Register WL	16
0x00E8	TMR4_SCSRxh	Special Control Status Register XH	16
0x00EC	TMR4_SCSRxl	Special Control Status Register XL	16
0x00D2	TMR4_SCMRuh	Special Mode Control Register UH	16
0x00D6	TMR4_SCMRul	Special Mode Control Register UL	16
0x00DA	TMR4_SCMRvh	Special Mode Control Register VH	16
0x00DE	TMR4_SCMRvl	Special Mode Control Register VL	16
0x00E2	TMR4_SCMRwh	Special Mode Control Register WH	16
0x00E6	TMR4_SCMRwl	Special Mode Control Register WL	16
0x00EA	TMR4_SCMRxh	Special Mode Control Register XH	16
0x00EE	TMR4_SCMRxl	Special Mode Control Register XL	16
0x00F0	TMR4_SCER	Special Extended Control Register	16
0x00A0	TMR4_POCRu	PWM Basic Control Register U	16
0x00A4	TMR4_POCRv	PWM Basic Control Register V	16
0x00A8	TMR4_POCRw	PWM Basic Control Register W	16
0x00AC	TMR4_POCRx	PWM Basic Control Register X	16
0x005C	TMR4_PSCR	PWM Status Control Register	32

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Offset	Register	Description	Width
0x0082	TMR4_PFSRu	PWM Filter Control Register U	16
0x008A	TMR4_PFSRv	PWM Filter Control Register V	16
0x0092	TMR4_PFSRw	PWM Filter Control Register W	16
0x009A	TMR4_PFSRx	PWM Filter Control Register X	16
0x0084	TMR4_PDARu	PWM Dead Zone Control Register AU	16
0x0086	TMR4_PDBRu	PWM Dead Zone Control Register BU	16
0x008C	TMR4_PDARv	PWM Dead Zone Control Register AV	16
0x008E	TMR4_PDBRv	PWM Dead Zone Control Register BV	16
0x0094	TMR4_PDARw	PWM Dead Zone Control Register AW	16
0x0096	TMR4_PDBRw	PWM Dead Zone Control Register BW	16
0x009C	TMR4_PDARx	PWM Dead Zone Control Register AX	16
0x009E	TMR4_PDBRx	PWM Dead Zone Control Register BX	16
0x00F4	TMR4_RCSR	Reload Control Status Register	32
0x00F8	TMR4_SCIR	Special Interrupt Control Register	16
0x00FC	TMR4_SCFR	Special Flag Control Register	16
0x0060	TMR4_BFCRu	Buffer Control Register U	32
0x0064	TMR4_BFCRv	Buffer Control Register V	32
0x0068	TMR4_BFCRw	Buffer Control Register W	32
0x006C	TMR4_BFCRx	Buffer Control Register X	32

Note

In the detailed description of registers that follow in this section, m=uh, ul, vh, vl, wh, wl, xh, xl, and n=u, v, w, x. The registers indicated by m correspond to the output control of ports TMR4_OUH, TMR4_OUL, TMR4_OVH, TMR4_OVL, TMR4_OWH, TMR4_OWL, TMR4_OXH, and TMR4_OXL when the function is implemented; The registers indicated by n correspond to the output controls of ports TMR4_OUx, TMR4_OVx, TMR4_OWx, TMR4_OXx, etc. when the function is implemented, where x=H or L, and the specific control of H or L has corresponding symmetrical bits in these registers.

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17.4.2 Count Value Register (TMR4_CNTR)

Offset	Bit Position															
0x0054	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	CNTR															
Access	RW															

Bit	Name	Functional Description	Access
15:0	CNTR	Counter Current Value When counting is stopped, the counter value can be initialized by writing a value to this register. During counting, this bit indicates the current counter value. **Notice** Writing to this register is prohibited while counting is in progress.	RW

17.4.3 Period Value Register (TMR4_CPSR)

Offset	Bit Position															
0x0050	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFFFF															
Name	CPSR															
Access	RW															

Bit	Name	Functional Description	Access
15:0	CPSR	General Period Reference Counter period value **Note** When reading data from this address area, the value read is not from the buffer register, but from the CPSR register.	RW

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17.4.4 Control Status Register (TMR4_CCSR)

Offset	Bit Position															
0x0058	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0040															
Name	ECKEN	Reserved	HST	Reserved	IRQZF	IRQZEN	IRQPF	IRQPEN	BUFEN	STOP	MODE	CLEAR	CKDIV			
Access	RW		RW		RW	RW	RW	RW	RW	RW	RW	RW	RW			

Bit	Name	Functional Description	Access
15	ECKEN	Clock Source Selection ● 0b0: Internal PCLK1 clock ● 0b1: External TMR4_CLK port input clock **Note** ● This bit is set when the counter stops. ● When operating with an external input clock, after the counter operation starts, the first edge of the external input clock, whether rising or falling, is ignored and the counting operation starts from the subsequent edge.	RW
14	*Reserved*	-	-
13	HST	Hardware Start Enabled Condition: The event specified in the TMR4_TRGSEL register occurs ● 0b0: Hardware start disabled upon condition match ● 0b1: When the condition matches, the hardware start is enabled, and the counter begins counting	RW
12	*Reserved*	-	-
11	IRQZF	Underflow Status ● 0b0: No count underflow has occurred ● 0b1: Count underflow occurred **Note** ● When using the period interval response function, the condition for setting this bit is determined by the period interval counter settings configured in the CVPR. ● When the counter is reset by the bus or when CLEAR=1 is written, the IRQZF bit will not be set.	RW
10	IRQZEN	Underflow Interrupt Enabled ● 0b0: Disable the IRQZF interrupt from being generated to the CPU ● 0b1: Enable the IRQZF interrupt from being generated to the CPU	RW

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Bit	Name	Functional Description	Access
9	IRQPF	Overflow Status ● 0b0: No count overflow occurred ● 0b1: Count overflow occurred **Note** ● When using the period interval response function, the condition for setting this bit is determined by the period interval counter settings configured in the CVPR. ● When the counter is reset by the bus or when CLEAR=1 is written, the IRQPF bit will not be set.	RW
8	IRQPEN	Overflow Interrupt Enabled ● 0b0: Disable the IRQPF interrupt from being generated to the CPU ● 0b1: Enable the IRQPF interrupt from being generated to the CPU	RW
7	BUFEN	Buffer Enabled ● 0b0: Disable CPSR buffer function ● 0b1: Enable CPSR buffer function	RW
6	STOP	Counter Enabled ● 0b0: Counter started ● 0b1: Counter stopped	RW
5	MODE	Waveform Mode ● 0b0: Sawtooth wave mode (supports only up counting) ● 0b1: Triangle wave mode	RW
4	CLEAR	Counter Clear Write 1 to clear the counter, write 0 has no effect; read always returns 0	RW
3:0	CKDIV	Count Clock Division Frequency This bit indicates the count clock frequency division of the basic counter ● 0b0000: Count clock is PCLK1 ● 0b0001: Count clock is PCLK1/2 ● 0b0010: Count clock is PCLK1/4 ● 0b0011: Count clock is PCLK1/8 ● 0b0100: Count clock is PCLK1/16 ● 0b0101: Count clock is PCLK1/32 ● 0b0110: Count clock is PCLK1/64 ● 0b0111: Count clock is PCLK1/128 ● 0b1000: Count clock is PCLK1/256 ● 0b1001: Count clock is PCLK1/512 ● 0b1010: Count clock is PCLK1/1024 ● Others: Setting prohibited **Note** When the clock source is internal PCLK1, frequency division is enabled.	RW

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17.4.5 Valid Period Register (TMR4_CVPR)

Offset	Bit Position															
0x005A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	PIC				ZIC				PIM				ZIM			
Access	RO				RO				RW				RW			

Bit	Name	Functional Description	Access
15:12	PIC	Overflow Interrupt Mask Status PIC is a down counter. When CNTR counts overflow interrupts, the value of PIC is reduced by 1. Reading PIC can obtain the number of overflow interrupts that need to be masked. Write condition: The value of PIM is loaded into PIC if one of the following is met: 1. Write PIM when counter is stoped (CCSR.STOP=1) 2. Counter clearing action occurs (CCSR.CLEAR writes 1) 3. PIC=0 and CNTR count overflow interrupt occurs	RO
11:8	ZIC	Underflow Interrupt Mask Status ZIC is a down counter. When CNTR counts underflow interrupts, the value of ZIC decreases by 1. Reading ZIC can obtain the number of underflow interrupts that need to be masked. Write condition: counter stopped state (CCSR.STOP=1) Write condition: The value of ZIM is loaded into ZIC if one of the following is met: 1. Counter clearing action occurs (CCSR.CLEAR writes 1) 2. ZIC=0 and CNTR count underflow interrupt occurs	RO
7:4	PIM	Overflow Interrupt Mask Setting Set the number of overflow interrupts to be masked	RW
3:0	ZIM	Underflow Interrupt Mask Setting Set the number of underflow interrupts to be masked	RW

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17.4.6 Period Control Register (TMR4_CPCR)

Offset	Bit Position															
0x0070	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved														CPSRLMCZ	CPSRLMCP
Access															RW	RW

Bit	Name	Functional Description	Access
15:2	*Reserved*	-	-
1	CPSRLMCZ	CPSR Underflow Point Periodic Interval Response Function Link ● 0b0: CPSR underflow point periodic interval response function link is invalid. ● 0b1: CPSR underflow point periodic interval response function link is valid. CPSR performs cache transfer when CVPR.ZIC=0b0000 and counting underflows.	RW
0	CPSRLMCP	CPSR Overflow Point Periodic Interval Response Function Link ● 0b0: CPSR overflow point periodic interval response function link is invalid. ● 0b1: CPSR overflow point periodic interval response function link is valid. CPSR performs cache transfer when CVPR.PIC=0b0000 and counting overflows.	RW

17.4.7 General Compare Reference Register 1 (TMR4_OCCR1m)

Offset: 0x0000 (TMR4_OCCR1uh), 0x0004 (TMR4_OCCR1ul), 0x0008 (TMR4_OCCR1vh), 0x000C (TMR4_OCCR1vl), 0x0010 (TMR4_OCCR1wh), 0x0014 (TMR4_OCCR1wl), 0x0018 (TMR4_OCCR1xh), 0x001C (TMR4_OCCR1xl)

Offset	Bit Position															
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	OCCR1															
Access	RW															

Bit	Name	Functional Description	Access
15:0	OCCR1	General Comparison Reference Value 1 **Note** When reading data from this address region, the value read is not from the buffer register, but from the OCCR1 register.	RW

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17.4.8 General Compare Reference Register 2 (TMR4_OCCR2m)

Offset: 0x0002 (TMR4_OCCR2uh), 0x0006 (TMR4_OCCR2ul), 0x000A (TMR4_OCCR2vh), 0x000E (TMR4_OCCR2vl), 0x0012 (TMR4_OCCR2wh), 0x0016 (TMR4_OCCR2wl), 0x001A (TMR4_OCCR2xh), 0x001E (TMR4_OCCR2xl)

Offset	Bit Position															
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	OCCR2															
Access	RW															

Bit	Name	Functional Description	Access
15:0	OCCR2	General Compare Reference Value 2 **Note** When reading data from this address region, the value read is not from the buffer register, but from the OCCR2 register.	RW

17.4.9 General Compare Reference Register 3 (TMR4_OCCR3m)

Offset: 0x0100 (TMR4_OCCR3uh), 0x0104 (TMR4_OCCR3ul), 0x0108 (TMR4_OCCR3vh), 0x010C (TMR4_OCCR3vl), 0x0110 (TMR4_OCCR3wh), 0x0114 (TMR4_OCCR3wl), 0x0118 (TMR4_OCCR3xh), 0x011C (TMR4_OCCR3xl)

Offset	Bit Position															
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	OCCR3															
Access	RW															

Bit	Name	Functional Description	Access
15:0	OCCR3	General Compare Reference Value 3 **Note** When reading data from this address region, the value read is not from the buffer register, but from the OCCR3 register.	RW

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17.4.10 General Control Status Register (TMR4_OCSRn)

Offset: 0x0020 (TMR4_OCSRu), 0x0024(TMR4_OCSRv), 0x0028(TMR4_OCSRw) , 0x002C(TMR4_OCSRx)

Offset	Bit Position															
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved				OCRSENL		OCRSENH		OCFL	OCFH	OCIEL	OCIEH	OCPL	OCPH	OCEL	OCEH
Access					RW		RW		RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
15:12	*Reserved*	-	-
11:10	OCRSENL	Compare Point Switching Mode L ● 0b00: Compare point switching mode 1 ● 0b01: Compare point switching mode 2 ● 0b10: Compare point switching mode 3 ● 0b11: Compare point switching mode 4	RW
9:8	OCRSENH	Compare Point Switching Mode H ● 0b00: Compare point switching mode 1 ● 0b01: Compare point switching mode 2 ● 0b10: Compare point switching mode 3 ● 0b11: Compare point switching mode 4	RW
7	OCFL	Count Match Flag L ● 0b0: The counter value is not equal to the OCCR*l setting value ● 0b1: The counter value is equal to the OCCR*l setting value **Note** This bit is enabled only when OCEL=1.	RW
6	OCFH	Count Match Flag H ● 0b0: The counter value is not equal to the OCCR*h setting value ● 0b1: The counter value is equal to the OCCR*h setting value **Note** This bit is enabled only when OCEH=1.	RW
5	OCIEL	Count Match Interrupt Enable L ● 0b0: When OCFL is set, no interrupt occurs ● 0b1: When OCFL is set, an interrupt occurs	RW
4	OCIEH	Count Match Interrupt Enable H ● 0b0: When OCFH is set, no interrupt occurs ● 0b1: When OCFH is set, an interrupt occurs	RW

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Bit	Name	Functional Description	Access
3	OCPL	Port Status L When Comparison Output Is Disabled Write: ● 0b0: When OCEL=0, in_op*l outputs low level ● 0b1: When OCEL=0, in_op*l outputs high level Read: ● 0b0: The current state of in_op*l is low level ● 0b1: The current state of in_op*l is high level	RW
2	OCPH	Port Status H When Comparison Output Is Disabled Write: ● 0b0: When OCEH=0, in_op*h outputs low level ● 0b1: When OCEH=0, in_op*h outputs high level Read: ● 0b0: The current state of in_op*h is low level ● 0b1: The current state of in_op*h is high level	RW
1	OCEL	Port Output Selection L ● 0b0: When compare output is disabled, the state of in_op*l port is determined by OCPL. ● 0b1: When compare output is enabled, the state of in_op*l port is determined by the settings of OCMR*l and the OCFL status.	RW
0	OCEH	Port Output Selection H ● 0b0: When compare output is disabled, the state of in_op*h port is determined by OCPH. ● 0b1: When compare output is enabled, the state of in_op*h port is determined by the settings of OCMR*h and the OCFH status.	RW

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17.4.11 General Extended Control Register (TMR4_OCERn)

Offset: 0x0022 (TMR4_OCERu), 0x0026(TMR4_OCERv), 0x002A(TMR4_OCERw), 0x002E(TMR4_OCERx)

Offset	Bit Position															
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved		MCECL	MCECH	LMML	LMMH	LMCL	LMCH	MLBUFEN		MHBUFEN		CLBUFEN		CHBUFEN	
Access			RW	RW	RW	RW	RW	RW	RW		RW		RW		RW	

Bit	Name	Functional Description	Access
15:14	*Reserved*	-	-
13	MCECL	Count Match Additional Condition Enable L Additional Condition: Count overflow (CNTR=CPSR) and OCCR*l > CPSR. ● 0b0: Disable this condition as a matching condition. ● 0b1: Enable this condition as a matching condition. When the condition is met, OCCR*l will generate a count match. **Note** 1. This bit can only be modified when the output comparison function is disabled (OCSR.OCEL=0). 2. For details, refer to the precautions in the TMR4_OCMRm register description.	RW
12	MCECH	Count Match Additional Condition Enable H Additional Condition: Count overflow (CNTR=CPSR) and OCCR*h > CPSR. ● 0b0: Disable this condition as a matching condition. ● 0b1: Enable this condition as a matching condition. When the condition is met, OCCR*h will generate a count match. **Note** 1. This bit can only be modified when the output comparison function is disabled (OCSR.OCEH=0). 2. For detailed information, refer to the notes in the TMR4_OCMRm register description.	RW
11	LMML	OCMR*l Periodic Interval Response Function Link L ● 0b0: The periodic interval response function link is disabled. The buffer transmission of OCMR*l is determined by the MLBUFEN setting. ● 0b1: The periodic interval response function link is enabled. The buffer transmission of OCMR*l, in addition to the MLBUFEN setting, must also meet the conditions where CVPR.PIC=0b0000 (when counting overflows) or CVPR.ZIC=0b0000 (when counting underflows).	RW

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Bit	Name	Functional Description	Access
10	LMMH	OCMR*h Periodic Interval Response Function Link H ● 0b0: The periodic interval response function link is disabled. The buffer transmission of OCMR*h is determined by the MHBUFEN setting. ● 0b1: The periodic interval response function link is enabled. In addition to the MHBUFEN setting, the buffer transmission of OCMR*h must also satisfy the condition where CVPR.PIC=0b0000 (when counting overflows) or CVPR.ZIC=0b0000 (when counting underflows).	RW
9	LMCL	OCCR*l Periodic Interval Response Function Link L ● 0b0: The periodic interval response function link is disabled. The buffer transmission of OCMR*l is determined by the CLBUFEN setting. ● 0b1: The periodic interval response function link is enabled. In addition to the CLBUFEN setting, the buffer transmission of OCCR*l must also satisfy the condition where CVPR.PIC=0b0000 (when counting overflows) or CVPR.ZIC=0b0000 (when counting underflows).	RW
8	LMCH	OCCR*h Periodic Interval Response Function Link H ● 0b0: The periodic interval response function link is disabled. The buffer transmission of OCCR*h is determined by the CHBUFEN setting. ● 0b1: The periodic interval response function link is enabled. In addition to the CHBUFEN setting, the buffer transmission of OCCR*h must also satisfy the condition where CVPR.PIC=0b0000 (when counting overflows) or CVPR.ZIC=0b0000 (when counting underflows).	RW
7:6	MLBUFEN	OCMR*l Buffer Transmission ● 0b00: The value of the OCMR*l buffer register is directly written to OCMR*l ● 0b01: The value of the OCMR*l buffer register is written to OCMR*l when the counter underflows ● 0b10: The value of the OCMR*l buffer register is written to OCMR*l when the counter overflows ● 0b11: The value of the OCMR*l buffer register is written to OCMR*l when the counter either overflows or underflows	RW
5:4	MHBUFEN	OCMR*h Buffer Transmission ● 0b00: The value of the OCMR*h buffer register is directly written to OCMR*h ● 0b01: The value of the OCMR*h buffer register is written to OCMR*h when the counter underflows ● 0b10: The value of the OCMR*h buffer register is written to OCMR*h when the counter overflows ● 0b11: The value of the OCMR*h buffer register is written to OCMR*h when the counter either overflows or underflows	RW

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Bit	Name	Functional Description	Access
3:2	CLBUFEN	OCCR*l Buffer Transmission ● 0b00: The value of the OCCR*l buffer register is directly written to OCCR*l. ● 0b01: The value of the OCCR*l buffer register is written to OCCR*l when the counter underflows. ● 0b10: The value of the OCCR*l buffer register is written to OCCR*l when the counter overflows. ● 0b11: The value of the OCCR*l buffer register is written to OCCR*l when the counter either overflows or underflows.	RW
1:0	CHBUFEN	OCCR*h Buffer Transmission ● 0b00: The value of the OCCR*h buffer register is directly written to OCCR*h ● 0b01: The value of the OCCR*h buffer register is written to OCCR*h when the counter underflows ● 0b10: The value of the OCCR*h buffer register is written to OCCR*h when the counter overflows ● 0b11: The value of the OCCR*h buffer register is written to OCCR*h when the counter either overflows or underflows	RW

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17.4.12 General Mode Control Register (TMR4_OCMRm)

Offset: 0x0030 (TMR4_OCMRuh), 0x0034 (TMR4_OCMRul), 0x0038 (TMR4_OCMRvh), 0x003C (TMR4_OCMRvl), 0x0040 (TMR4_OCMRwh), 0x0044 (TMR4_OCMRwl), 0x0048 (TMR4_OCMRxh), 0x004C (TMR4_OCMRxl)

TMR4_OCMRuh, TMR4_OCMRvh, TMR4_OCMRwh, TMR4_OCMRxh Register:

Offset	Bit Position															
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	OPNZRH		OPNPKH		OPZRH		OPUCH		OPPKH		OPDCH		OCFZRH	OCFUCH	OCFPKH	OCFDCH
Access	RW		RW		RW		RW		RW		RW		RW	RW	RW	RW

Table 17-25 OCCR*h Count Match List

Condition Number	Determines whether the OCCR*h count matches or not
1	No
2	Yes

Bit	Name	Functional Description	Access
15:14	OPNZRH	Underflow Condition 1 Port State H Underflow condition 1 (Simultaneously satisfied): Count underflow and OCCR*h counts do not match. ● 0b00: When the condition is satisfied, in_op*h remains un-changed ● 0b01: When the condition is satisfied, in_op*h outputs high level ● 0b10: When the condition is satisfied, in_op*h outputs low level ● 0b11: When the condition is satisfied, in_op*h outputs inverted state	RW
13:12	OPNPKH	Overflow Condition 1 Port State H Overflow condition 1 (Simultaneously satisfied): Count overflow and OCCR*h counts do not match. ● 0b00: When the condition is satisfied, in_op*h remains un-changed ● 0b01: When the condition is satisfied, in_op*h outputs high level ● 0b10: When the condition is satisfied, in_op*h outputs low level ● 0b11: When the condition is satisfied, in_op*h outputs inverted state	RW

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Bit	Name	Functional Description	Access
11:10	OPZRH	Underflow Condition 2 Port State H Underflow condition 2 (Simultaneously satisfied): Count underflow and OCCR*h counts do not match. ● 0b00: When the condition is satisfied, in_op*h remains un-changed ● 0b01: When the condition is satisfied, in_op*h outputs high level ● 0b10: When the condition is satisfied, in_op*h outputs low level ● 0b11: When the condition is satisfied, in_op*h outputs inverted state	RW
9:8	OPUCH	Up Counting Condition 2 Port State H Up counting condition 2 (Simultaneously satisfied): the counter counts up, and the OCCR*h counts match ● 0b00: When the condition is satisfied, in_op*h remains un-changed ● 0b01: When the condition is satisfied, in_op*h outputs high level ● 0b10: When the condition is satisfied, in_op*h outputs low level ● 0b11: When the condition is satisfied, in_op*h outputs inverted state	RW
7:6	OPPKH	Overflow Condition 2 Port State H Overflow Condition 2 (Simultaneously satisfied): Count overflow and OCCR*h counts match ● 0b00: When the condition is satisfied, in_op*h remains un-changed ● 0b01: When the condition is satisfied, in_op*h outputs high level ● 0b10: When the condition is satisfied, in_op*h outputs low level ● 0b11: When the condition is satisfied, in_op*h outputs inverted state	RW
5:4	OPDCH	Down Counting Condition 2 Port State H Down counting condition 2 (Simultaneously satisfied): the counter counts down, and the OCCR*h counts match ● 0b00: When the condition is satisfied, in_op*h remains un-changed ● 0b01: When the condition is satisfied, in_op*h outputs high level ● 0b10: When the condition is satisfied, in_op*h outputs low level ● 0b11: When the condition is satisfied, in_op*h outputs inverted state	RW
3	OCFZRH	Underflow Point OCFH Status H Condition (Simultaneously satisfied): count underflow, OCCR*h counts match ● 0b0: When the condition is met, the OCSR.OCFH bit remains unchanged ● 0b1: When the condition is met, the OCSR.OCFH bit is set	RW
2	OCFUCH	Up Counting OCFH State H Conditions (Simultaneously satisfied): counter counts up, OCCR*h counts match ● 0b0: When the condition is met, the OCSR.OCFH bit remains unchanged ● 0b1: When the condition is met, the OCSR.OCFH bit is set	RW

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Bit	Name	Functional Description	Access
1	OCFPKH	Overflow Point OCFH State H Condition (Simultaneously satisfied): count overflow, OCCR*h counts match ● 0b0: When the condition is met, the OCSR.OCFH bit remains unchanged ● 0b1: When the condition is met, the OCSR.OCFH bit is set	RW
0	OCFDCH	Down Counting OCFH State H Conditions (Simultaneously satisfied): counter counts down, OCCR*h counts match ● 0b0: When the condition is met, the OCSR.OCFH bit remains unchanged ● 0b1: When the condition is met, the OCSR.OCFH bit is set	RW

TMR4_OCMRul, TMR4_OCMRvl, TMR4_OCMRwl, TMR4_OCMRxl Register:

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	EOPNZRL		EOPNPKL		EOPZRL		EOPUCL		EOPPKL		EOPDCL		EOPNUCL		EOPNDCL		OPNZRL		OPNPKL		OPZRL		OPUCL		OPPKL		OPDCL		OCFZRL	OCFUCL	OCFPKL	OCFDCL
Access	RW		RW		RW		RW		RW		RW		RW		RW		RW		RW		RW		RW		RW		RW		RW	RW	RW	RW

Table 17-28 OCCR*h/l Count Match List

Condition Number	Determines whether the OCCR*h count matches or not	Determines whether the OCCR*l count matches or not
1	No	No
2	No	Yes
3	Yes	No
4	Yes	Yes

Bit	Name	Functional Description	Access
31:30	EOPNZRL	Underflow Condition 3 Port State L Underflow condition 3 (Simultaneously satisfied): Counting under-flow, OCCR*l counts do not match, OCCR*h counts match ● 0b00: When the condition is satisfied, in_op*l remains un-changed ● 0b01: When the condition is satisfied, in_op*l outputs high level ● 0b10: When the condition is satisfied, in_op*l outputs low level ● 0b11: When the condition is satisfied the output of in_op*l is reversed	RW

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Bit	Name	Functional Description	Access
29:28	EOPNPKL	Overflow Condition 3 Port State L Overflow condition 3 (Simultaneously satisfied): Counting overflow, OCCR*l counts do not match, OCCR*h counts match ● 0b00: When the condition is satisfied, in_op*l remains unchanged ● 0b01: When the condition is satisfied, in_op*l outputs high level ● 0b10: When the condition is satisfied, in_op*l outputs low level ● 0b11: When the condition is satisfied the output of in_op*l is reversed	RW
27:26	EOPZRL	Underflow Condition 4 Port State L Underflow condition 4 (Simultaneously satisfied): Counting underflow, OCCR*l counts match, OCCR*h counts match ● 0b00: When the condition is satisfied, in_op*l remains unchanged ● 0b01: When the condition is satisfied, in_op*l outputs high level ● 0b10: When the condition is satisfied, in_op*l outputs low level ● 0b11: When the condition is satisfied the output of in_op*l is reversed	RW
25:24	EOPUCL	Up Counting Condition 4 Port State L Up counting condition 4 (Simultaneously satisfied): counter counts up, OCCR*l counts match, OCCR*h counts match ● 0b00: When the condition is satisfied, in_op*l remains unchanged ● 0b01: When the condition is satisfied, in_op*l outputs high level ● 0b10: When the condition is satisfied, in_op*l outputs low level ● 0b11: When the condition is satisfied the output of in_op*l is reversed	RW
23:22	EOPPKL	Overflow Condition 4 Port State L Overflow condition 4 (Simultaneously satisfied): count overflow, OCCR*l counts match, OCCR*h counts match ● 0b00: When the condition is satisfied, in_op*l remains unchanged ● 0b01: When the condition is satisfied, in_op*l outputs high level ● 0b10: When the condition is satisfied, in_op*l outputs low level ● 0b11: When the condition is satisfied the output of in_op*l is reversed	RW
21:20	EOPDCL	Down Counting Condition 4 Port State L Down counting condition 4 (Simultaneously satisfied): counter counts down, OCCR*l counts match, OCCR*h counts match ● 0b00: When the condition is satisfied, in_op*l remains unchanged ● 0b01: When the condition is satisfied, in_op*l outputs high level ● 0b10: When the condition is satisfied, in_op*l outputs low level ● 0b11: When the condition is satisfied the output of in_op*l is reversed	RW

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Bit	Name	Functional Description	Access
19:18	EOPNUCL	Up Counting Condition 3 Port State L Up counting condition 3 (Simultaneously satisfied): the counter counts up, OCCR*l counts do not match, OCCR*h counts match ● 0b00: When the condition is satisfied, in_op*l remains unchanged ● 0b01: When the condition is satisfied, in_op*l outputs high level ● 0b10: When the condition is satisfied, in_op*l outputs low level ● 0b11: When the condition is satisfied the output of in_op*l is reversed	RW
17:16	EOPNDCL	Down Counting Condition 3 Port State L Down counting condition 3 (Simultaneously satisfied): counter counts down, OCCR*l counts do not match, OCCR*h counts match ● 0b00: When the condition is satisfied, in_op*l remains unchanged ● 0b01: When the condition is satisfied, in_op*l outputs high level ● 0b10: When the condition is satisfied, in_op*l outputs low level ● 0b11: When the condition is satisfied the output of in_op*l is reversed	RW
15:14	OPNZRL	Underflow Condition 1 Port State L Underflow condition 1 (Simultaneously satisfied): Counting underflow, OCCR*l counts do not match, OCCR*h counts match, ● 0b00: When the condition is satisfied, in_op*l remains unchanged ● 0b01: When the condition is satisfied, in_op*l outputs high level ● 0b10: When the condition is satisfied, in_op*l outputs low level ● 0b11: When the condition is satisfied the output of in_op*l is reversed	RW
13:12	OPNPKL	Overflow Condition 1 Port State L Overflow condition 1 (Simultaneously satisfied): count overflow, OCCR*l counts match, OCCR*h counts do not match ● 0b00: When the condition is satisfied, in_op*l remains unchanged ● 0b01: When the condition is satisfied, in_op*l outputs high level ● 0b10: When the condition is satisfied, in_op*l outputs low level ● 0b11: When the condition is satisfied the output of in_op*l is reversed	RW
11:10	OPZRL	Underflow Condition 2 Port State L Underflow condition 2 (Simultaneously satisfied): Counting underflow, OCCR*l counts match, OCCR*h counts do not match ● 0b00: When the condition is satisfied, in_op*l remains unchanged ● 0b01: When the condition is satisfied, in_op*l outputs high level ● 0b10: When the condition is satisfied, in_op*l outputs low level ● 0b11: When the condition is satisfied the output of in_op*l is reversed	RW

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Bit	Name	Functional Description	Access
9:8	OPUCL	Up Counting Condition 2 Port State L Up counting condition 2 (Simultaneously satisfied): The counter counts up, OCCR*l counts match, OCCR*h counts do not match ● 0b00: When the condition is satisfied, in_op*l remains un-changed ● 0b01: When the condition is satisfied, in_op*l outputs high level ● 0b10: When the condition is satisfied, in_op*l outputs low level ● 0b11: When the condition is satisfied the output of in_op*l is reversed	RW
7:6	OPPKL	Overflow Condition 2 Port State L Overflow condition 2 (Simultaneously satisfied): Count overflow, OCCR*l counts match, OCCR*h counts do not match ● 0b00: When the condition is satisfied, in_op*l remains un-changed ● 0b01: When the condition is satisfied, in_op*l outputs high level ● 0b10: When the condition is satisfied, in_op*l outputs low level ● 0b11: When the condition is satisfied the output of in_op*l is reversed	RW
5:4	OPDCL	Down Counting Condition 2 Port State L Down counting condition 2 (Simultaneously satisfied): counter counts down, OCCR*l counts match, OCCR*h counts do not match ● 0b00: When the condition is satisfied, in_op*l remains un-changed ● 0b01: When the condition is satisfied, in_op*l outputs high level ● 0b10: When the condition is satisfied, in_op*l outputs low level ● 0b11: When the condition is satisfied the output of in_op*l is reversed	RW
3	OCFZRL	Underflow Point OCFL State L Condition (Simultaneously satisfied): count underflow, OCCR*l counts match ● 0b0: When the condition is met, the OCSR.OCFL bit remains unchanged ● 0b1: When the condition is met, the OCSR.OCFL bit is set	RW
2	OCFUCL	Up Counting OCFL State L Conditions (Simultaneously satisfied): counter counts up, OCCR*l counts match ● 0b0: When the condition is met, the OCSR.OCFL bit remains unchanged ● 0b1: When the condition is met, the OCSR.OCFL bit is set	RW
1	OCFPKL	Overflow Point OCFL State L Conditions (Simultaneously satisfied): count overflow, OCCR*l counts match ● 0b0: When the condition is met, the OCSR.OCFL bit remains unchanged ● 0b1: When the condition is met, the OCSR.OCFL bit is set	RW

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Bit	Name	Functional Description	Access
0	OCFDCL	Down Counting OCFL State L Conditions (Simultaneously satisfied): counter counts down, OCCR*l counts match ● 0b0: When the condition is met, the OCSR.OCFL bit remains unchanged ● 0b1: When the condition is met, the OCSR.OCFL bit is set	RW

Notice

1. When reading data from this address area, the value read is not from the buffer register, but from the OCMR register.
2. TMR4_O*L can be determined by OCCR*l and the count value of the counter (independent operation mode), or OCCR*h and the count value of the counter and OCCR*l and the count value of the counter (linked operation mode). Write the same 12-bit value to Bit[31:20] and Bit[15:4] of register OCMR*l, and write 0b0000 to OCMR*l[19:16]. At this time, the in_op*l output will not be affected by OCCR*h, but only by OCCR*l. Independent operation mode: channel*H is configured by OCCR*h, and channel*L is configured by OCCR*l. If the independent operation mode does not meet the above conditions, it is the linked operation mode: channel*L output is affected by both OCCR*h and OCCR*l.
3. When the following two conditions are met, it is also considered to meet the conditions set by OCMR*h.OPPKH:
   a. CCSR.MODE=1 && Count overflow && OCCR*h=0xFFFF
   b. OCER*.MCECH=1 && Count overflow && OCCR*h≥CNTR
4. When the following two conditions are met, it is also considered to meet the conditions set by OCMR*l.OPPKL:
   a. CCSR.MODE=1 && Count overflow && OCCR*l=0xFFFF
   b. OCER*.MCECL=1 && Count overflow && OCCR*l≥CNTR

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17.4.13 Special Compare Reference Register (TMR4_SCCRm)

Offset: 0x00B0 (TMR4_SCCRuh), 0x00B4 (TMR4_SCCRul), 0x00B8 (TMR4_SCCRvh), 0x00BC (TMR4_SCCRvl), 0x00C0 (TMR4_SCCRwh), 0x00C4 (TMR4_SCCRwl), 0x00C8 (TMR4_SCCRxh), 0x00CC (TMR4_SCCRxl)

Offset	Bit Position															
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	SCCR															
Access	RW															

Bit	Name	Functional Description	Access
15:0	SCCR	Special Compare Reference Special compare reference (Compare start mode) or delayed reference (Delay start mode) **Note** When reading data from this address area, the value read is not from the buffer register, but from the SCCR register.	RW

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17.4.14 General Control Status Register (TMR4_SCSRm)

Offset: 0x00D0 (TMR4_SCSRuh), 0x00D4 (TMR4_SCSRul), 0x00D8 (TMR4_SCSRvh), 0x00DC (TMR4_SCSRvl), 0x00E0 (TMR4_SCSRwh), 0x00E4 (TMR4_SCSRwl), 0x00E8 (TMR4_SCSRxh), 0x00EC (TMR4_SCSRxl)

Offset	Bit Position															
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	ZEN	UEN	PEN	DEN	Reserved		EVTDS	EVTMS	Reserved		LMC	EVTOS			BUFEN	
Access	RW	RW	RW	RW			RW	RW			RW	RW			RW	

Bit	Name	Functional Description	Access
15	ZEN	Underflow Point EVT Enabled ● 0b0: When the count underflows, EVT has no operation ● 0b1: When the count underflows: ▶ When EVTMS=0&SCCR compare match&SCMR setting match, EVT starts output ▶ When EVTMS=1&OCCR compare match&SCMR setting match, EVT delay mode starts	RW
14	UEN	Up Counting EVT Enabled ● 0b0: When counting up, EVT has no operation ● 0b1: When counting up: ▶ When EVTMS=0&SCCR compare match&SCMR setting match, EVT starts output ▶ When EVTMS=1&OCCR compare match&SCMR setting match, EVT delay mode starts	RW
13	PEN	Overflow Point EVT Enabled ● 0b0: When the count overflows, EVT has no operation ● 0b1: When the count overflows: ▶ When EVTMS=0&SCCR compare match&SCMR setting match, EVT starts output ▶ When EVTMS=1&OCCR compare match&SCMR setting match, EVT delay mode starts	RW
12	DEN	Down Counting EVT Enabled ● 0b0: When counting down, EVT has no operation ● 0b1: When counting down: ▶ When EVTMS=0&SCCR compare match&SCMR setting match, EVT starts output ▶ When EVTMS=1&OCCR compare match&SCMR setting match, EVT delay mode starts	RW
11:10	*Reserved*	-	-

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Bit	Name	Functional Description	Access
9	EVTDS	EVT Delay Object Selection ● 0b0: In delayed start mode, OCCR*h is used as the delayed comparison match object ● 0b1: In delayed start mode, OCCR*l is used as the delayed comparison match object **Note** This bit is invalid when EVTMS=0.	RW
8	EVTMS	EVT Mode Selection ● 0b0: Compare start mode (triggered by the comparison result of CNTR and SCCR) ● 0b1: Delay start mode (triggered after the comparison match event is delayed by SCCR)	RW
7:6	*Reserved*	-	-
5	LMC	Periodic Interval Response Function Link ● 0b0: Periodic interval response function link is disabled, and the buffer transfer of SCCR is determined by the BUFEN setting ● 0b1: Periodic interval response function link is enabled, and the buffer transfer of SCCR must satisfy CVPR.PIC=0b0000 (when the count overflows) or CVPR.ZIC=0b0000 (when the count underflows) based on the BUFEN setting	RW
4:2	EVTOS	EVT Output Selection ● 0b000: Special match event output to Special Event 0 (TMR4_SCM0) ● 0b001: Special match event output to Special Event 1 (TMR4_SCM1) ● 0b010: Special match event output to Special Event 2 (TMR4_SCM2) ● 0b011: Special match event output to Special Event 3 (TMR4_SCM3) ● 0b100: Special match event output to Special Event 4 (TMR4_SCM4) ● 0b101: Special match event output to Special Event 5 (TMR4_SCM5) ● 0b110: Special match event output to Special Event 6 (TMR4_SCM6) ● 0b111: Special match event output to Special Event 7 (TMR4_SCM7)	RW
1:0	BUFEN	SCCR&SCMR Buffer Transmission ● 0b00: The values of the SCCR and SCMR buffer registers are directly written to SCCR and SCMR ● 0b01: The values of the SCCR and SCMR buffer registers are written to SCCR and SCMR when the count underflows ● 0b10: The values of the SCCR and SCMR buffer registers are written to SCCR and SCMR when the count overflows ● 0b11: The values of the SCCR and SCMR buffer registers are written to SCCR and SCMR when the count underflows or overflows	RW

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17.4.15 Special Extended Control Register (TMR4_SCER)

Offset	Bit Position															
0x00F0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved							PCTS	Reserved				EVTRS			
Access								RW					RW			

Bit	Name	Functional Description	Access
15:9	*Reserved*	-	-
8	PCTS	Count Direction Output Enabled When the counter works in triangle wave mode, control the count direction output to the port ● 0b0: Disable the count direction signal output to the TMR4_PCT port ● 0b1: Enable the count direction signal output to the TMR4_PCT port	RW
7:4	*Reserved*	-	-
3:0	EVTRS	Special Event Output Selection ● 0b0000: Disable special event output to port ● 0b0001: The EVT of Special Event 0 (TMR4_SCM0) is output to TMR4_ADSM port ● 0b0010: The EVT of Special Event 1 (TMR4_SCM1) is output to the TMR4_ADSM port ● 0b0011: The EVT of Special Event 2 (TMR4_SCM2) is output to the TMR4_ADSM port ● 0b0100: The EVT of Special Event 3 (TMR4_SCM3) is output to the TMR4_ADSM port ● 0b0101: The EVT of Special Event 4 (TMR4_SCM4) is output to the TMR4_ADSM port ● 0b0110: The EVT of Special Event 5 (TMR4_SCM5) is output to the TMR4_ADSM port ● 0b1000: The EVT of Special Event 6 (TMR4_SCM6) is output to the TMR4_ADSM port ● 0b1001: The EVT of Special Event 7 (TMR4_SCM7) is output to the TMR4_ADSM port ● Others: Setting prohibited	RW

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17.4.16 Special Mode Control Register (TMR4_SCMRm)

Offset: 0x00D2 (TMR4_SCMRuh), 0x00D6 (TMR4_SCMRul), 0x00DA (TMR4_SCMRvh), 0x00DE (TMR4_SCMRvl), 0x00E2 (TMR4_SCMRwh), 0x00E6 (TMR4_SCMRwl), 0x00EA (TMR4_SCMRxh), 0x00EE (TMR4_SCMRxl)

Offset	Bit Position															
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFF00															
Name	Reserved								MPCE	MZCE	Reserved		AMC			
Access									RW	RW			RW			

Bit	Name	Functional Description	Access
15:8	*Reserved*	*All bits read as 1, Write as 1*	-
7	MPCE	Periodic Interval Response Enabled ● 0b0: Disable AMC and CVPR.PIC comparison ● 0b1: Enable AMC and CVPR.PIC comparison	RW
6	MZCE	Periodic Interval Response Enabled ● 0b0: Disable comparison between AMC and CVPR.ZIC ● 0b1: Enable comparison between AMC and CVPR.ZIC	RW
5:4	*Reserved*	-	-
3:0	AMC	Special Event Output Period Interval Value This bit sets the period interval value of the special event output function. When AMC and CVPR.PIC or CVPR.ZIC are equal, the special event output function is disabled	RW

Note

When reading data from this address area, the value read is not from the buffer register, but from the SCMR register.

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17.4.17 PWM Control Register (TMR4_POCRn)

Offset: 0x00A0 (TMR4_POCRu), 0x00A4(TMR4_POCRv), 0x00A8(TMR4_POCRw), 0x00AC(TMR4_POCRx)

Offset	Bit Position															
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFF00															
Name	Reserved								LVLS		PWMMD		Reserved	DIVCK		
Access									RW		RW			RW		

Bit	Name	Functional Description	Access
15:8	*Reserved*	*All bits read as 1, Write as 1*	-
7:6	LVLS	PWM Output Polarity Control ● 0b00: Neither TMR4_O*H nor TMR4_O*L outputs are inverted ● 0b01: The outputs of TMR4_O*H and TMR4_O*L are both inverted ● 0b10: The output of TMR4_O*H is inverted, and the output of TMR4_O*L is not inverted ● 0b11: The output of TMR4_O*H is not inverted, and the output of TMR4_O*L is inverted	RW
5:4	PWMMD	PWM Output Mode ● 0b00: Pass-through mode ● 0b01: Dead-zone timer mode ● 0b10: Dead-zone timer filter mode ● 0b11: Setting prohibited	RW
3	*Reserved*	-	-
2:0	DIVCK	Count Clock Division Frequency This bit indicates the count clock division of the filter counter, dead zone counter and reload counter. ● 0b000: Count clock is PCLK1 ● 0b001: Count clock is PCLK1/2 ● 0b010: Count clock is PCLK1/4 ● 0b011: Count clock is PCLK1/8 ● 0b100: Count clock is PCLK1/16 ● 0b101: Count clock is PCLK1/32 ● 0b110: Count clock is PCLK1/64 ● 0b111: Count clock is PCLK1/128	RW

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17.4.18 PWM Status Control Register (TMR4_PSCR)

Offset	Bit Position																													
0x005C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x55550000																															
Name	OSXL	OSXH	OSWL	OSWH	OSVL	OSVH	OSUL	OSUH	Reserved												ODT	AOE	MOE	OEXL	OEXH	OEWL	OEWH	OEVL	OEVH	OEUL	OEUH
Access	RW	RW	RW	RW	RW	RW	RW	RW													RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:30	OSXL	TMR4_OXL Output Disable Status Conditions: 1. EMB event occurs; 2. Software writes MOE=0; 3. MOE=1&OEXL=0 ● 0b00: When one of the above conditions is met, the TMR4_OXL port outputs normally ● 0b01: When one of the above conditions is met, the TMR4_OXL port output is Hi-Z ● 0b10: When one of the above conditions is met, the TMR4_OXL port output is fixed at a low level ● 0b11: When one of the above conditions is met, the TMR4_OXL port output is fixed at a high level **Note** This bit can only be modified when Timer4 is stopped (CCSR.STOP=1).	RW
29:28	OSXH	TMR4_OXH Output Disable Status Conditions: 1. EMB event occurs; 2. Software writes MOE=0; 3. MOE=1&OEXH=0 ● 0b00: When one of the above conditions is met, the TMR4_OXH port outputs normally ● 0b01: When one of the above conditions is met, the TMR4_OXH port output is Hi-Z ● 0b10: When one of the above conditions is met, the TMR4_OXH port output is fixed at a low level ● 0b11: When one of the above conditions is met, the TMR4_OXH port output is fixed at a high level **Note** This bit can only be modified when Timer4 is stopped (CCSR.STOP=1).	RW

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Bit	Name	Functional Description	Access
27:26	OSWL	TMR4_OWL Output Disable Status Conditions: 1. EMB event occurs; 2. Software writes MOE=0; 3. MOE=1&OEWL=0 ● 0b00: When one of the above conditions is met, the TMR4_OWL port outputs normally ● 0b01: When one of the above conditions is met, the TMR4_OWL port output is Hi-Z ● 0b10: When one of the above conditions is met, the TMR4_OUL port output is fixed at a low level ● 0b11: When one of the above conditions is met, the TMR4_OWL port output is fixed at a high level **Note** This bit can only be modified when Timer4 is stopped (CCSR.STOP=1).	RW
25:24	OSWH	TMR4_OWH Output Disable Status Conditions: 1. EMB event occurs; 2. Software writes MOE=0; 3. MOE=1&OEWH=0 ● 0b00: When one of the above conditions is met, the TMR4_OWH port outputs normally ● 0b01: When one of the above conditions is met, the TMR4_OWH port output is Hi-Z ● 0b10: When one of the above conditions is met, the TMR4_OWH port output is fixed at a low level ● 0b11: When one of the above conditions is met, the TMR4_OWH port output is fixed at a high level **Note** This bit can only be modified when Timer4 is stopped (CCSR.STOP=1).	RW
23:22	OSVL	TMR4_OVL Output Disable Status Conditions: 1. EMB event occurs; 2. Software writes MOE=0; 3. MOE=1&OEVL=0 ● 0b00: When one of the above conditions is met, the TMR4_OVL port outputs normally ● 0b01: When one of the above conditions is met, the TMR4_OVL port output is Hi-Z ● 0b10: When one of the above conditions is met, the TMR4_OVL port output is fixed at a low level ● 0b11: When one of the above conditions is met, the TMR4_OVL port output is fixed at a high level **Note** This bit can only be modified when Timer4 is stopped (CCSR.STOP=1).	RW

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Bit	Name	Functional Description	Access
21:20	OSVH	TMR4_OVH Output Disable Status Conditions: 1. EMB event occurs; 2. Software writes MOE=0; 3. MOE=1&OEVH=0 ● 0b00: When one of the above conditions is met, the TMR4_OVH port outputs normally ● 0b01: When one of the above conditions is met, the TMR4_OVH port output is Hi-Z ● 0b10: When one of the above conditions is met, the TMR4_OVH port output is fixed at a low level ● 0b11: When one of the above conditions is met, the TMR4_OVH port output is fixed at a high level **Note** This bit can only be modified when Timer4 is stopped (CCSR.STOP=1).	RW
19:18	OSUL	TMR4_OUL Output Disable Status Conditions: 1. EMB event occurs; 2. Software writes MOE=0; 3. MOE=1&OEUL=0 ● 0b00: When one of the above conditions is met, the TMR4_OUL port outputs normally ● 0b01: When one of the above conditions is met, the TMR4_OUL port output is Hi-Z ● 0b10: When one of the above conditions is met, the TMR4_OUL port output is fixed at a low level ● 0b11: When one of the above conditions is met, the TMR4_OUL port output is fixed at a high level **Note** This bit can only be modified when Timer4 is stopped (CCSR.STOP=1).	RW
17:16	OSUH	TMR4_OUH Output Disable Status Conditions: 1. EMB event occurs; 2. Software writes MOE=0; 3. MOE=1&OEUH=0 ● 0b00: When one of the above conditions is met, the TMR4_OUH port outputs normally ● 0b01: When one of the above conditions is met, the TMR4_OUH port output is Hi-Z ● 0b10: When one of the above conditions is met, the TMR4_OUH port output is fixed at a low level ● 0b11: When one of the above conditions is met, the TMR4_OUH port output is fixed at a high level **Note** This bit can only be modified when Timer4 is stopped (CCSR.STOP=1).	RW
15:12	*Reserved*	-	-

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Bit	Name	Functional Description	Access
11:10	ODT	Port Enable Bit Active Time Condition: After the value of port enable bit OE*L, OE*H is changed ● 0b0x: When the condition is met, it takes effect immediately ● 0b10: When the condition is met, it takes effect when the counter underflows next time ● 0b11: When the condition is met, it takes effect when the counter overflows next time	RW
9	AOE	Automatic Output Enable ● 0b0: After the EMB event is cleared, the MOE bit can only be set to 1 by software to restore normal PWM output ● 0b1: After the EMB event is cleared, the MOE bit is automatically set to 1 by hardware at the next count underflow point, and the PWM output returns to normal **Note** Setting EMB_STATCLR or clearing EMB_SOE can clear the EMB event.	RW
8	MOE	Master Output Enable ● 0b0: TMR4_O*H/L port outputs the state specified by the OS*H/L bit ● 0b1: TMR4_O*H, TMR4_O*L port outputs are enabled when the OE*H, OE*L bits are set to enable **Note** This bit is cleared immediately by hardware after an EMB event occurs. After the EMB event is cleared, this bit can be set to 1 by software or automatically by hardware according to the setting of the AOE bit.	RW
7	OEXL	TMR4_OXL Output Enabled ● 0b0: TMR4_OXL port output state is set by the OSXL bit ● 0b1: When MOE=1, TMR4_OWL port outputs normal PWM waveform	RW
6	OEXH	TMR4_OXH Output Enabled ● 0b0: TMR4_OXH port output state is set by OSXH bit ● 0b1: When MOE=1, TMR4_OXH port outputs normal PWM waveform	RW
5	OEWL	TMR4_OWL Output Enabled ● 0b0: TMR4_OWL port output state is set by the OSWL bit ● 0b1: When MOE=1, TMR4_OWL port outputs normal PWM waveform	RW
4	OEWH	TMR4_OWH Output Enabled ● 0b0: TMR4_OWH port output state is set by the OSWH bit ● 0b1: When MOE=1, TMR4_OWH port outputs normal PWM waveform	RW
3	OEVL	TMR4_OVL Output Enabled ● 0b0: TMR4_OVL port output state is set by the OSVL bit ● 0b1: When MOE=1, TMR4_OVL port outputs normal PWM waveform	RW

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Bit	Name	Functional Description	Access
2	OEVH	TMR4_OVH Output Enabled ● 0b0: TMR4_OVH port output state is set by the OSVH bit ● 0b1: When MOE=1, TMR4_OVH port outputs normal PWM waveform	RW
1	OEUL	TMR4_OUL Output Enabled ● 0b0: TMR4_OUL port output state is set by the OSUL bit ● 0b1: When MOE=1, TMR4_OUL port outputs normal PWM waveform	RW
0	OEUH	TMR4_OUH Output Enabled ● 0b0: TMR4_OUH port output state is set by the OSUH bit ● 0b1: When MOE=1, TMR4_OUH port outputs normal PWM waveform	RW

The following table shows the relationship between the PWM port output status and the register setting value:

MOE bits	OE*L/H bits	OS*L/H bits	TMR4_O*L/H output enable
0b1	0b0	0b00	Normal output (Timer4 drive)
		0b01	Hi-Z
		0b10	Low Level
		0b11	High Level
	0b1	0bXX	Normal output (Timer4 drive)
0b0	0bX	0b00	Normal output (Timer4 drive)
		0b01	Hi-Z
		0b10	Low Level
		0b11	High Level

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17.4.19 PWM Filter Control Register (TMR4_PFSRn)

Offset: 0x0082 (TMR4_PFSRu), 0x008A(TMR4_PFSRv), 0x0092(TMR4_PFSRw), 0x009A(TMR4_PFSRx)

Offset	Bit Position															
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	PFSR															
Access	RW															

Bit	Name	Functional Description	Access
15:0	PFSR	Filter Initial Value Filter count initial value **Note** When the dead timer filter mode is not selected in the PWM waveform output mode, the 16-bit filter counter is used as a 16-bit reload counter, which can generate interrupt output periodically. This function is independent of the PWM waveform generator function.	RW

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17.4.20 PWM Dead Zone Control Register A (TMR4_PDARn)

Offset: 0x0084 (TMR4_PDARu), 0x008C(TMR4_PDARv), 0x0094(TMR4_PDARw), 0x009C(TMR4_PDARx)

Offset	Bit Position															
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	PDAR															
Access	RW															

Bit	Name	Functional Description	Access
15:0	PDAR	Dead Zone Initial Value Dead zone count initial value	RW

17.4.21 PWM Dead Zone Control Register B (TMR4_PDBRn)

Offset: 0x0086 (TMR4_PDBRu), 0x008E(TMR4_PDBRv), 0x0096(TMR4_PDBRw), 0x009E(TMR4_PDBRx)

Offset	Bit Position															
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	PDBR															
Access	RW															

Bit	Name	Functional Description	Access
15:0	PDBR	Dead Zone Initial Value Dead zone count initial value	RW

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17.4.22 Reload Control Status Register (TMR4_RCSR)

Offset	Bit Position																													
0x00F4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved												RTSX	RTEX	RTICX	RTIFX	RTSW	RTEW	RTICW	RTIFW	RTSV	RTEV	RTICV	RTIFV	RTSU	RTEU	RTICU	RTIFU	RTIDX	RTIDW	RTIDV	RTIDU
Access													RW	RW	RW	RO	RW	RW	RW	RO	RW	RW	RW	RO	RW	RW	RW	RO	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:20	*Reserved*	-	-
19	RTSX	Reload Counter Stop X Writing 1 stops reloading counter X and clears RTIFX, write 0 has no effect; read always returns 0	RW
18	RTEX	Reload Counter Start X Write 1 to start reloading counter X, write 0 has no effect. Read: ● 0b0: Reload counter X stopped ● 0b1: Reload counter X started	RW
17	RTICX	Clear Count Match Status X Write 1 to clear RTIFX flag bit, write 0 has no effect; read always returns 0	RW
16	RTIFX	Count Match Status X ● 0b0: The reload counter count value does not match PFSRx ● 0b1: The reload counter count value matches PFSRx	RO
15	RTSW	Reload Counter Stop W Writing 1 stops reloading counter W and clears RTIFW, write 0 has no effect; read always returns 0	RW
14	RTEW	Reload Counter Start W Write 1 to start reloading counter W, write 0 has no effect. Read: ● 0b0: Reload counter W stopped ● 0b1: Reload counter W started	RW
13	RTICW	Clear Count Match Status W Write 1 to clear RTIFW flag bit, write 0 has no effect; read always returns 0	RW
12	RTIFW	Count Match Status W ● 0b0: The reload counter count value does not match PFSRw ● 0b1: The reload counter count value matches PFSRw	RO
11	RTSV	Reload Counter Stop V Writing 1 stops reloading counter V and clears RTIFV, write 0 has no effect; read always returns 0	RW

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Bit	Name	Functional Description	Access
10	RTEV	Reload Counter Start V Write 1 to start reloading counter V, write 0 has no effect. Read: ● 0b0: Reload counter V stopped ● 0b1: Reload counter V started	RW
9	RTICV	Clear Count Match Status V Write 1 to clear RTIFV flag bit, write 0 has no effect; read always returns 0	RW
8	RTIFV	Count Match Status V ● 0b0: The reload counter count value does not match PFSRv ● 0b1: The reload counter count value matches PFSRv	RO
7	RTSU	Reload Counter Stop U Writing 1 stops reloading counter U and clears RTIFU, write 0 has no effect; read always returns 0	RW
6	RTEU	Reload Counter Start U Write 1 to start reloading counter U, write 0 has no effect. Read: ● 0b0: Reload counter U stopped ● 0b1: Reload counter U started	RW
5	RTICU	Clear Count Match Status U Write 1 to clear RTIFU flag bit, write 0 has no effect; read always returns 0	RW
4	RTIFU	Count Match Status U ● 0b0: The reload counter count value does not match PFSRu ● 0b1: The reload counter count value matches PFSRu	RO
3	RTIDX	Reload Interrupt Mask X ● 0b0: Reload interrupt X output is enabled when the reload function is active. ● 0b1: Reload interrupt X output is disabled when the reload function is active.	RW
2	RTIDW	Reload Interrupt Mask W ● 0b0: Reload interrupt W output is enabled when the reload function is active. ● 0b1: Reload interrupt W output is disabled when the reload function is active.	RW
1	RTIDV	Reload Interrupt Mask V ● 0b0: Reload interrupt V output is enabled when the reload function is active. ● 0b1: Reload interrupt V output is disabled when the reload function is active.	RW
0	RTIDU	Reload Interrupt Mask U ● 0b0: Reload interrupt U output is enabled when the reload function is active. ● 0b1: Reload interrupt U output is disabled when the reload function is active.	RW

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17.4.23 Special Interrupt Control Register (TMR4_SCIR)

Offset	Bit Position															
0x00F8	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFF00															
Name	Reserved								ITEN7	ITEN6	ITEN5	ITEN4	ITEN3	ITEN2	ITEN1	ITEN0
Access									RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
15:8	*Reserved*	-	-
7	ITEN7	Special Match Interrupt 7 Enabled ● 0b0: Disable ● 0b1: Enable	RW
6	ITEN6	Special Match Interrupt 6 Enabled ● 0b0: Disable ● 0b1: Enable	RW
5	ITEN5	Special Match Interrupt 5 Enabled ● 0b0: Disable ● 0b1: Enable	RW
4	ITEN4	Special Match Interrupt 4 Enabled ● 0b0: Disable ● 0b1: Enable	RW
3	ITEN3	Special Match Interrupt 3 Enabled ● 0b0: Disable ● 0b1: Enable	RW
2	ITEN2	Special Match Interrupt 2 Enabled ● 0b0: Disable ● 0b1: Enable	RW
1	ITEN1	Special Match Interrupt 1 Enabled ● 0b0: Disable ● 0b1: Enable	RW
0	ITEN0	Special Match Interrupt 0 Enabled ● 0b0: Disable ● 0b1: Enable	RW

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17.4.24 Special Flag Control Register (TMR4_SCFR)

Offset	Bit Position															
0x00FC	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFF00															
Name	Reserved								SF7	SF6	SF5	SF4	SF3	SF2	SF1	SF0
Access									RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
15:8	*Reserved*	-	-
7	SF7	Special Compare Match Flag Bit 7 ● 0b0: No occurrence of special count compare match event 7 ● 0b1: Special count compare match event 7 occurred	RW
6	SF6	Special Compare Match Flag Bit 6 ● 0b0: No occurrence of special count compare match event 6 ● 0b1: Special count compare match event 6 occurred	RW
5	SF5	Special Compare Match Flag Bit 5 ● 0b0: No occurrence of special count compare match event 5 ● 0b1: Special count compare match event 5 occurred	RW
4	SF4	Special Compare Match Flag Bit 4 ● 0b0: No occurrence of special count compare match event 4 ● 0b1: Special count compare match event 4 occurred	RW
3	SF3	Special Compare Match Flag Bit 3 ● 0b0: No occurrence of special count compare match event 3 ● 0b1: Special count compare match event 3 occurred	RW
2	SF2	Special Compare Match Flag Bit 2 ● 0b0: No occurrence of special count compare match event 2 ● 0b1: Special count compare match event 2 occurred	RW
1	SF1	Special Compare Match Flag Bit 1 ● 0b0: No occurrence of special count compare match event 1 ● 0b1: Special count compare match event 1 occurred	RW
0	SF0	Special Compare Match Flag Bit 0 ● 0b0: No occurrence of special count compare match event 0 ● 0b1: Special count compare match event 0 occurred	RW

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17.4.25 Buffer Control Register (TMR4_BFCRn)

Offset: 0x0060 (TMR4_BFCRu), 0x0064 (TMR4_BFCRv), 0x0068 (TMR4_BFCRw), 0x006C (TMR4_BFCRx)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved														OCRSLMCL	OCRSLMCH	Reserved													OCRSBUFENL	OCRSBUFENH	
Access															RW	RW														RW	RW	

Bit	Name	Functional Description	Access
31:18	*Reserved*	-	-
17	OCRSLMCL	Compare Point Switching Mode Register Periodic Interval Response Function Link L ● 0b0: Periodic interval response function link is invalid. The buffer transfer of OCRSENLn is determined by the OCRSBUFENL setting. ● 0b1: Periodic interval response function link is valid. The buffer transfer of OCRSENLn must additionally satisfy CVPR.PIC=0b0000 (on counter overflow) or CVPR.ZIC=0b0000 (on counter underflow), on top of the OCRSBUFENL setting.	RW
16	OCRSLMCH	Compare Point Switching Mode Register Periodic Interval Response Function Link H ● 0b0: Periodic interval response function link is invalid. The buffer transfer of OCRSENHn is determined by the OCRSBUFENH setting. ● 0b1: Periodic interval response function link is valid. The buffer transfer of OCRSENHn must additionally satisfy CVPR.PIC=0b0000 (on counter overflow) or CVPR.ZIC=0b0000 (on counter underflow), on top of the OCRSBUFENH setting.	RW
15:4	*Reserved*	-	-
3:2	OCRSBUFENL	Compare Point Switching Mode Register Buffer Transfer L ● 0b00: The value of the OCSR.OCRSENL buffer register is directly written to OCSR.OCRSENL. ● 0b01: The value of the OCSR.OCRSENL buffer register is written to OCSR.OCRSENL on counter underflow. ● 0b10: The value of the OCSR.OCRSENL buffer register is written to OCSR.OCRSENL on counter overflow. ● 0b11: The value of the OCSR.OCRSENL buffer register is written to OCSR.OCRSENL on counter underflow or overflow.	RW

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Bit	Name	Functional Description	Access
1:0	OCRSBU-FENH	Compare Point Switching Mode Register Buffer Transfer H ● 0b00: The value of the OCSR.OCRSENH buffer register is directly written to OCSR.OCRSENH. ● 0b01: The value of the OCSR.OCRSENH buffer register is written to OCSR.OCRSENH on counter underflow. ● 0b10: The value of the OCSR.OCRSENH buffer register is written to OCSR.OCRSENH on counter overflow. ● 0b11: The value of the OCSR.OCRSENH buffer register is written to OCSR.OCRSENH on counter underflow or overflow.	RW

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18 Emergency Brake Module (EMB)

18.1 Introduction

The emergency brake module is a function module that generates contorl events output to the timer when certain conditions are met to stop the timer or change the PWM signal output to the external motor. The following factors are used to generate control events:

- External port input level change
- Level of Timer4 PWM output port occurs in phase (same high or same low)
- Voltage comparator comparison results
- XTAL stops oscillating
- Write register software control

18.2 Functional Description

18.2.1 EMB Channel Function Block Diagram

The EMB is used to output an event signal to the timer module with PWM function (Timer4, TimerA_5) when certain conditions are met, notifying the timer module to control the current PWM output. The EMB module has 2 Groups, where Group0 is used to control Timer4, and Group1 is used to control TimerA_5.

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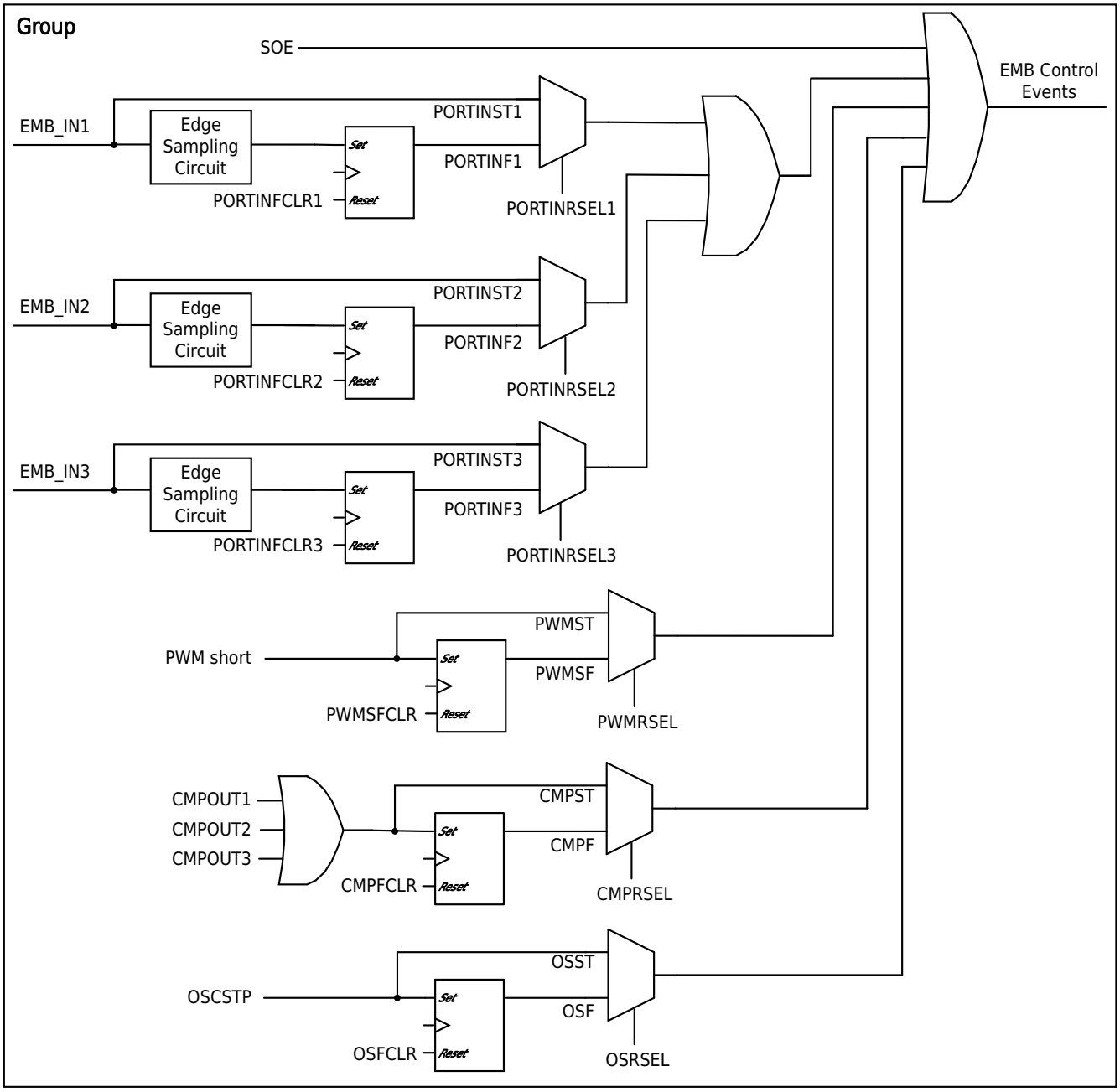

Figure 18-1 EMB Channel Function Block Diagram

18.2.2 EMB Structure Block Diagram

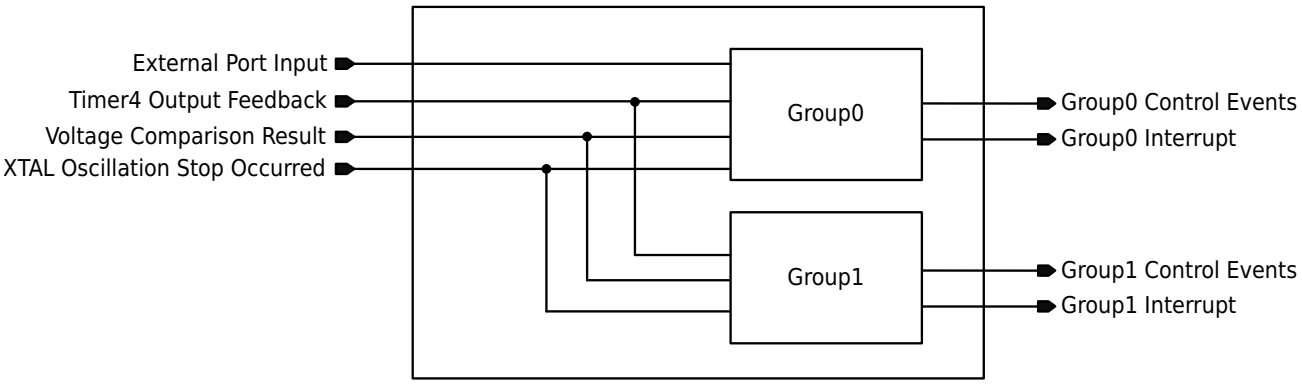

Figure 18-2 EMB Structure Block Diagram

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18.2.3 Control PWM Signal Output When External Port Input Level Changes

The EMB has 3 external ports (hereinafter referred to as y, y=1-3) used to control the PWM signal output when the input level changes. Each group can independently set one or more of the 3 external ports to be active, and the port allocation is shown in the table below.

Table 18-1 EMB Port Assignment

Port	PIN Name
EMB_IN1	P22, P70
EMB_IN2	PB1, PB4
EMB_IN3	P00, PE2

When using an external port input level change to control PWM signal output:

1. Configure the EMB_CTL1 register: Enable the port input via PORTINENy, and set the port active level via INVSELy.
2. Configure the EMB_INTEN register: Enable the interrupt via PORTININTENy.

After completing the settings, when EMB_INy generates a valid level that meets the condition, EMB_STAT.PORTINSTy (Port Input Control Status) is set.

When EMB_INy generates a qualified level transition (edge change), EMB_STAT.PORTINFy (Port Input Control Flag) is set; if the interrupt is enabled at this time, a port input control interrupt is generated.

Notice

The port input control flag bit PORTINFy is set only when an edge change is detected.

INVSEL=0 detects a rising edge (low-to-high level transition); INVSEL=1 detects a falling edge (high-to-low level transition).

Special case: When INVSEL=1, if the external signal initially remains at a low level with no edge change, the port input control flag bit will be set.

External Port Input Filter Function

Configure the EMB_CTL2.NFENy bit to enable the external port input filter function. The filter clock is set via EMB_CTL2.NFSELy.

The filter samples the input signal according to the filter clock and uses a three-sample consistency method for filtering. That is, when the filter clock samples three consecutive consistent levels on the port, that level is considered valid and transmitted to the module's internal logic. Levels with less than three consistent samples are treated as external noise and filtered out, not transmitted internally.

External Port Immediate Release Function

The EMB control event is output to Timer4 and TimerA_5 via the EMB_RLSSEL.PORTINRSELy register selection, which chooses between EMB_STAT.PORTINSTy or EMB_STAT.PORTINFy. After receiving the control event, Timer4 and TimerA_5 can set their output ports to normal output, high level, low level, or high-impedance state according to the register settings. For specific configurations, please refer to the "PWM Status Control Register (TMR4_PSCR)" in the "General Control Timer (Timer4)" chapter and the "Emergency Port Status Control Register (TMRA_EPSCR)" in the "General Timer (TimerA)" chapter.

- When PORTINRSELy=1, when the port input level becomes invalid, EMB_STAT.PORTINSTy is automatically cleared, and the control event is immediately released.

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- When PORTINRSELy=0, you need to write to EMB_STATCLR.PORTINFCLRy to clear the EMB_STAT.PORTINFy bit, thereby releasing the control event.

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18.2.4 Control PWM Signal Output When PWM Output Port Level Occurs In-phase (same high or same low)

Note
Only Group0 supports this function.

Group0 is used to monitor the complementary PWM output signals of Timer4. Timer4 PWM in-phase can trigger a brake. In the following, y refers to the four output groups of Timer4, where y=0-3.

When using Timer4 PWM output in-phase control for PWM signal output:

1. Configure register EMB_CTL1: Enable short-circuit output control via PWMSENy.
2. Configure register EMB_CTL2: Select the effective level to be monitored via PWMLVy.
3. Configure register EMB_INTEN: Enable the PWM output in-phase control interrupt via PWMSINTEN.

After configuration is complete, the EMB monitors the complementary PWM output signals of Timer4. When the output signals are both high or both low, EMB_STAT.PWMST (PWM output status) is set, and simultaneously EMB_STAT.PWMSF (PWM output in-phase control flag) is set. If the interrupt is enabled at this time, a PWM output in-phase interrupt is generated.

PWM Output Control Immediate Release

The EMB control event is output to Timer4 via register EMB_RLSSEL.PWMRSEL, selected from either EMB_STAT.PWMST or EMB_STAT.PWMSF. After receiving the control event, Timer4 can set the output port to normal output, high level, low level, or high-impedance state according to the register settings. For specific configurations, please refer to the "PWM Status Control Register (TMR4_PSCR)" in the "General Control Timer (Timer4)" chapter.

- When PWMRSEL=1, once the PWM output both-high or both-low state is resolved, EMB_STAT.PWMST will be automatically cleared, and the control event will be released immediately.
- When PWMRSEL=0, after the PWM output both-high or both-low state is resolved, it is necessary to write EMB_STATCLR.PWMSFCLR to clear the EMB_STAT.PWMSF bit before the control event is released.

Table 18-2 EMB Group Comparison Table

Port Name	Function	Corresponding Group	EMB_CTL1 Control Bit	EMB_CTL2 Control Bit
TMR4_OUH	Complementary PWM output signal of Timer4	Group0	PWMSEN3	PWMLV3
TMR4_OUL				
TMR4_OVH			PWMSEN2	PWMLV2
TMR4_OVL				
TMR4_OWH			PWMSEN1	PWMLV1
TMR4_OWL				
TMR4_OXH			PWMSEN0	PWMLV0
TMR4_OXL				

18.2.5 Control PWM Signal Output According to Voltage Comparator Compare Result

Each Group of the EMB can send control event signals to Timer4 and TimerA_5 based on the comparison result of the voltage comparator. In the following description, y refers to the three comparison channels.

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For the setting of the voltage comparator output result, please refer to the relevant description in the "Voltage Comparator (CMP)" chapter.

When using the CMP comparison result to control PWM signal output:

1. Configure the EMB_CTL1 register: Enable the voltage comparator comparison result output control via CMPENy.
2. Configure the EMB_INTEN register: Enable the voltage comparator comparison result control interrupt via CMPINTEN.

After configuration is complete, when the voltage comparator comparison result flag is set, EMB_STAT.CMPST (Voltage Comparator Status) is set, and EMB_STAT.CMPF (Voltage Comparator Control Flag) is also set. If the interrupt is enabled at this time, the voltage comparator comparison result control generates an interrupt.

Voltage Comparator Comparison Result Control Immediate Release

The EMB control event is output to Timer4 and TimerA_5 via the EMB_RLSSEL.CMPRSEL register selection from either EMB_STAT.CMPST or EMB_STAT.CMPF. After receiving the control event, Timer4 and TimerA_5 can set their output ports to normal output, high level, low level, or high-impedance state according to the register settings. For specific configurations, please refer to the "PWM Status Control Register (TMR4_PSCR)" in the "General Control Timer (Timer4)" chapter and the "Emergency Port Status Control Register (TMRA_EPSCR)" in the "General Timer (TimerA)" chapter.

- When CMPRSEL=1, the control event is released immediately when the voltage comparator result becomes invalid, and EMB_STAT.CMPST is automatically cleared.
- When CMPRSEL=0, after the voltage comparator result becomes invalid, it is necessary to write EMB_STATCLR.CMPFCLR to clear the EMB_STAT.CMPF bit to release the control event.

18.2.6 Controlling PWM Signal Output When XTAL Stops Oscillating

Each Group of the EMB can send a control event signal to Timer4 and TimerA_5 when an XTAL stop oscillation occurs.

To use XTAL stop oscillation to control PWM signal output:

1. Configure register EMB_CTL1: Enable XTAL stop oscillation control via OSCSTPEN.
2. Configure register EMB_INTEN: Enable the XTAL stop oscillation control interrupt via OSINTEN.

After configuration is complete, when the selected XTAL stop oscillation flag is set, EMB_STAT.OSST (XTAL Stop Oscillation Status) is set, and simultaneously EMB_STAT.OSF (XTAL Stop Oscillation Flag) is set. If the interrupt is enabled at this time, the XTAL stop oscillation control generates an interrupt.

Notice

When the trigger source "XTAL Stop Oscillation" control is enabled (EMB_CTL1.OSCSTPEN=1), after disabling the XTAL oscillation fault detection function, if you need to re-enable the XTAL oscillation fault detection function, please refer to the "External High-Speed Oscillator Fault Detection" section in the *Clock Controller (CMU)* chapter for detailed steps.

Immediate Release of XTAL Stop Oscillation Control

The EMB control event selects whether to output to Timer4 and TimerA_5 via EMB_STAT.OSST or EMB_STAT.OSF through register EMB_RLSSEL.OSRSEL. After receiving the control event, Timer4 and TimerA_5 can set their output ports to normal output, high level, low level, or high-impedance state according to the register settings. For specific configurations, please see the "PWM Status Control

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Register (TMR4_PSCR)" section in the *General Control Timer (Timer4)* chapter and the "Emergency Port Status Control Register (TMRA_EPSCR)" section in the *General Timer (TimerA)* chapter.

- When OSRSEL=1, when the XTAL stop oscillation signal becomes invalid, EMB_STAT.OSST will be automatically cleared, and the control event will be released immediately.
- When OSRSEL=0, after the XTAL stop oscillation signal becomes invalid, you need to write EMB_STATCLR.OSFCLR to clear the EMB_STAT.OSF bit to release the control event.

18.2.7 Write Register Software Control PWM Signal Output

The EMB software output enable control register (EMB_SOE) allows users to send control signals to Timer4 and TimerA_5 directly through software setting and resetting. When the software controls the PWM output, no interrupt request is generated.

- When SOE=1, notify the corresponding module that an EMB event has occurred.
- When SOE=0, the PWM outputs normally.

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18.3 Register Description

18.3.1 Register List

- EMB Group0 Base Address: 0x40017C00
- EMB Group1 Base Address: 0x40017C20

Note

EMB contains 2 Groups, namely Group0-1.

Table 18-3 Emergency Brake Module (EMB) Register Offset

Offset	Register	Description	Width
0x00	EMB_CTL1	EMB Control Register 1 (Group 0)	32
0x00	EMB_CTL1	EMB Control Register 1 (Group1)	32
0x04	EMB_CTL2	EMB Control Register 2 (Group 0)	32
0x04	EMB_CTL2	EMB Control Register 2 (Group 1)	32
0x08	EMB_SOE	EMB Software Output Enable Register (Group0-1)	32
0x0C	EMB_STAT	EMB Status Register (Group0)	32
0x0C	EMB_STAT	EMB Status Register (Group1)	32
0x10	EMB_STATCLR	EMB Status Clear Register (Group0)	32
0x10	EMB_STATCLR	EMB Status Clear Register (Group1)	32
0x14	EMB_INTEN	EMB Interrupt Enable Register (Group0)	32
0x14	EMB_INTEN	EMB Interrupt Enable Register (Group1)	32
0x18	EMB_RLSSEL	EMB Control PWM Output Release Select Register (Group0)	32
0x18	EMB_RLSSEL	EMB Control PWM Output Release Select Register (Group1)	32

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18.3.2 EMB Control Register 1 (EMB_CTL1) (Group0)

This register is a one-time write register, that is, it can only be written once after reset.

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved							INVSEL3	INVSEL2	INVSEL1	Reserved			PORTINEN3	PORTINEN2	PORTINEN1	Reserved							PWMSEN3	PWMSEN2	PWMSEN1	PWMSEN0	OSCSTPEN	Reserved	CMPEN3	CMPEN2	CMPEN1
Access								RW	RW	RW				RW	RW	RW								RW	RW	RW	RW	RW		RW	RW	RW

Bit	Name	Functional Description	Access
31:25	*Reserved*	-	-
24	INVSEL3	Port Input 3 Active Level Selection ● 0b0: High level enabled ● 0b1: Low level enabled	RW
23	INVSEL2	Port Input 2 Active Level Selection ● 0b0: High level enabled ● 0b1: Low level enabled	RW
22	INVSEL1	Port Input 1 Active Level Selection ● 0b0: High level enabled ● 0b1: Low level enabled	RW
21:19	*Reserved*	-	-
18	PORTINEN3	Port Input 3 Control Enabled ● 0b0: Port input control disabled ● 0b1: Port input control enabled	RW
17	PORTINEN2	Port Input 2 Control Enabled ● 0b0: Port input control disabled ● 0b1: Port input control enabled	RW
16	PORTINEN1	Port Input 1 Control Enabled ● 0b0: Port input control disabled ● 0b1: Port input control enabled	RW
15:9	*Reserved*	-	-
8	PWMSEN3	TMR4_OUH/L Short Circuit Output Control Enabled ● 0b0: Output control is disabled when short circuit occurs ● 0b1: Output control is enabled when short circuit occurs	RW
7	PWMSEN2	TMR4_OVH/L Short Circuit Output Control Enabled ● 0b0: Output control is disabled when short circuit occurs ● 0b1: Output control is enabled when short circuit occurs	RW

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Bit	Name	Functional Description	Access
6	PWMSEN1	TMR4_OWH/L Short Circuit Output Control Enabled ● 0b0: Output control is disabled when short circuit occurs ● 0b1: Output control is enabled when short circuit occurs	RW
5	PWMSEN0	TMR4_OXH/L Short Circuit Output Control Enabled ● 0b0: Output control is disabled when short circuit occurs ● 0b1: Output control is enabled when short circuit occurs	RW
4	OSCSTPEN	XTAL Stop Oscillation Control Enabled ● 0b0: Output control on XTAL stop oscillation disable ● 0b1: Output control on XTAL stop oscillation enable	RW
3	*Reserved*	-	-
2	CMPEN3	CMP3 Voltage Comparator Comparison Result Control Enabled ● 0b0: Voltage comparator comparison result output control disabled ● 0b1: Voltage comparator comparison result output control enabled	RW
1	CMPEN2	CMP2 Voltage Comparator Comparison Result Control Enabled ● 0b0: Voltage comparator comparison result output control disabled ● 0b1: Voltage comparator comparison result output control enabled	RW
0	CMPEN1	CMP1 Voltage Comparator Comparison Result Control Enabled ● 0b0: Voltage comparator comparison result output control disabled ● 0b1: Voltage comparator comparison result output control enabled	RW

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18.3.3 EMB Control Register 1 (EMB_CTL1) (Group1)

This register is a one-time write register, that is, it can only be written once after reset.

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved							INVSEL3	INVSEL2	INVSEL1	Reserved			PORTINEN3	PORTINEN2	PORTINEN1	Reserved											OSCSTPEN	Reserved	CMPEN3	CMPEN2	CMPEN1
Access								RW	RW	RW				RW	RW	RW												RW		RW	RW	RW

Bit	Name	Functional Description	Access
31:25	*Reserved*	-	-
24	INVSEL3	Port Input 3 Active Level Selection ● 0b0: High level enabled ● 0b1: Low level enabled	RW
23	INVSEL2	Port Input 2 Active Level Selection ● 0b0: High level enabled ● 0b1: Low level enabled	RW
22	INVSEL1	Port Input 1 Active Level Selection ● 0b0: High level enabled ● 0b1: Low level enabled	RW
21:19	*Reserved*	-	-
18	PORTINEN3	Port Input 3 Control Enabled ● 0b0: Port input control disabled ● 0b1: Port input control enabled	RW
17	PORTINEN2	Port Input 2 Control Enabled ● 0b0: Port input control disabled ● 0b1: Port input control enabled	RW
16	PORTINEN1	Port Input 1 Control Enabled ● 0b0: Port input control disabled ● 0b1: Port input control enabled	RW
15:5	*Reserved*	-	-
4	OSCSTPEN	XTAL Stop Oscillation Control Enabled ● 0b0: Output control is invalid when XTAL stop oscillation occurs ● 0b1: Output control is valid when XTAL stop oscillation occurs	RW
3	*Reserved*	-	-

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Bit	Name	Functional Description	Access
2	CMPEN3	CMP3 Voltage Comparator Comparison Result Control Enabled ● 0b0: Voltage comparator comparison result output control disabled ● 0b1: Voltage comparator comparison result output control enabled	RW
1	CMPEN2	CMP2 Voltage Comparator Comparison Result Control Enabled ● 0b0: Voltage comparator comparison result output control disabled ● 0b1: Voltage comparator comparison result output control enabled	RW
0	CMPEN1	CMP1 Voltage Comparator Comparison Result Control Enabled ● 0b0: Voltage comparator comparison result output control disabled ● 0b1: Voltage comparator comparison result output control enabled	RW

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18.3.4 EMB Control Register 2 (EMB_CTL2) (Group0)

This register is a single-write register, meaning it can only be written once after a reset.

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved	NFEN3	NFSEL3			NFEN2	NFSEL2			NFEN1	NFSEL1			Reserved															PWMLV3	PWMLV2	PWMLV1	PWMLV0
Access		RW	RW			RW	RW			RW	RW																	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31	*Reserved*	-	-
30	NFEN3	Port Input 3 Digital Filter Enable ● 0b0: Filter Disable ● 0b1: Filter Enable	RW
29:26	NFSEL3	Port Input 3 Digital Filter Clock Selection ● 0b0000: Use PCLK1 for filtering ● 0b0001: Use PCLK1 divided by 2 for filtering ● 0b0010: Use PCLK1 divided by 4 for filtering ● 0b0011: Use PCLK1 divided by 8 for filtering ● 0b0100: Use PCLK1 divided by 16 for filtering ● 0b0101: Use PCLK1 divided by 32 for filtering ● 0b0110: Use PCLK1 divided by 64 for filtering ● 0b0111: Use PCLK1 divided by 128 for filtering ● 0b1000: Use PCLK1 divided by 256 for filtering ● 0b1001: Use PCLK1 divided by 512 for filtering	RW
25	NFEN2	Port Input 2 Digital Filter Enable ● 0b0: Filter Disable ● 0b1: Filter Enable	RW
24:21	NFSEL2	Port Input 2 Digital Filter Clock Selection ● 0b0000: Use PCLK1 for filtering ● 0b0001: Use PCLK1 divided by 2 for filtering ● 0b0010: Use PCLK1 divided by 4 for filtering ● 0b0011: Use PCLK1 divided by 8 for filtering ● 0b0100: Use PCLK1 divided by 16 for filtering ● 0b0101: Use PCLK1 divided by 32 for filtering ● 0b0110: Use PCLK1 divided by 64 for filtering ● 0b0111: Use PCLK1 divided by 128 for filtering ● 0b1000: Use PCLK1 divided by 256 for filtering ● 0b1001: Use PCLK1 divided by 512 for filtering	RW
20	NFEN1	Port Input 1 Digital Filter Enable ● 0b0: Filter Disable ● 0b1: Filter Enable	RW

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Bit	Name	Functional Description	Access
19:16	NFSEL1	Port Input 1 Digital Filter Clock Selection ● 0b0000: Use PCLK1 for filtering ● 0b0001: Use PCLK1 divided by 2 for filtering ● 0b0010: Use PCLK1 divided by 4 for filtering ● 0b0011: Use PCLK1 divided by 8 for filtering ● 0b0100: Use PCLK1 divided by 16 for filtering ● 0b0101: Use PCLK1 divided by 32 for filtering ● 0b0110: Use PCLK1 divided by 64 for filtering ● 0b0111: Use PCLK1 divided by 128 for filtering ● 0b1000: Use PCLK1 divided by 256 for filtering ● 0b1001: Use PCLK1 divided by 512 for filtering	RW
15:4	*Reserved*	-	-
3	PWMLV3	TMR4_OUH/L Output Active Level Selection ● 0b0: Low level is the active level ● 0b1: High level is the active level	RW
2	PWMLV2	TMR4_OVH/L Output Active Level Selection ● 0b0: Low level is the active level ● 0b1: High level is the active level	RW
1	PWMLV1	TMR4_OWH/L Output Active Level Selection ● 0b0: Low level is the active level ● 0b1: High level is the active level	RW
0	PWMLV0	TMR4_OXH/L Output Active Level Selection ● 0b0: Low level is the active level ● 0b1: High level is the active level	RW

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18.3.5 EMB Control Register 2 (EMB_CTL2) (Group1)

This register is a single-write register, meaning it can only be written once after a reset.

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved	NFEN3	NFSEL3			NFEN2	NFSEL2			NFEN1	NFSEL1			Reserved																		
Access		RW	RW			RW	RW			RW	RW																					

Bit	Name	Functional Description	Access
31	*Reserved*	-	-
30	NFEN3	Port Input 3 Digital Filter Enable ● 0b0: Filter Disable ● 0b1: Filter Enable	RW
29:26	NFSEL3	Port Input 3 Digital Filter Clock Selection ● 0b0000: Use PCLK1 for filtering ● 0b0001: Use PCLK1 divided by 2 for filtering ● 0b0010: Use PCLK1 divided by 4 for filtering ● 0b0011: Use PCLK1 divided by 8 for filtering ● 0b0100: Use PCLK1 divided by 16 for filtering ● 0b0101: Use PCLK1 divided by 32 for filtering ● 0b0110: Use PCLK1 divided by 64 for filtering ● 0b0111: Use PCLK1 divided by 128 for filtering ● 0b1000: Use PCLK1 divided by 256 for filtering ● 0b1001: Use PCLK1 divided by 512 for filtering	RW
25	NFEN2	Port Input 2 Digital Filter Enable ● 0b0: Filter Disable ● 0b1: Filter Enable	RW
24:21	NFSEL2	Port Input 2 Digital Filter Clock Selection ● 0b0000: Use PCLK1 for filtering ● 0b0001: Use PCLK1 divided by 2 for filtering ● 0b0010: Use PCLK1 divided by 4 for filtering ● 0b0011: Use PCLK1 divided by 8 for filtering ● 0b0100: Use PCLK1 divided by 16 for filtering ● 0b0101: Use PCLK1 divided by 32 for filtering ● 0b0110: Use PCLK1 divided by 64 for filtering ● 0b0111: Use PCLK1 divided by 128 for filtering ● 0b1000: Use PCLK1 divided by 256 for filtering ● 0b1001: Use PCLK1 divided by 512 for filtering	RW
20	NFEN1	Port Input 1 Digital Filter Enable ● 0b0: Filter Disable ● 0b1: Filter Enable	RW

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Bit	Name	Functional Description	Access
19:16	NFSEL1	Port Input 1 Digital Filter Clock Selection ● 0b0000: Use PCLK1 for filtering ● 0b0001: Use PCLK1 divided by 2 for filtering ● 0b0010: Use PCLK1 divided by 4 for filtering ● 0b0011: Use PCLK1 divided by 8 for filtering ● 0b0100: Use PCLK1 divided by 16 for filtering ● 0b0101: Use PCLK1 divided by 32 for filtering ● 0b0110: Use PCLK1 divided by 64 for filtering ● 0b0111: Use PCLK1 divided by 128 for filtering ● 0b1000: Use PCLK1 divided by 256 for filtering ● 0b1001: Use PCLK1 divided by 512 for filtering	RW
15:0	*Reserved*	-	-

18.3.6 EMB Software Output Enable Register (EMB_SOE) (Group0-1)

Offset	Bit Position																													
0x08	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																															SOE
Access																																RW

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-
0	SOE	Software Control Output ● 0b0: Normal PWM output ● 0b1: EMB event occurs	RW

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18.3.7 EMB Status Register (EMB_STAT) (Group0)

Offset	Bit Position																													
0x0C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved															PORTINST3	PORTINST2	PORTINST1	Reserved			PORTINF3	PORTINF2	PORTINF1	OSST	CMPST	PWMST	Reserved	OSF	CMPF	PWMSF	Reserved
Access																RO	RO	RO				RO	RO	RO	RO	RO	RO		RO	RO	RO	

Bit	Name	Functional Description	Access
31:17	*Reserved*	-	-
16	PORTINST3	Port Input 3 Control Status ● 0b0: Port input control is in the disable level state ● 0b1: Port input control is in the enable level state	RO
15	PORTINST2	Port Input 2 Control Status ● 0b0: Port input control is in the disable level state ● 0b1: Port input control is in the enable level state	RO
14	PORTINST1	Port Input 1 Control Status ● 0b0: Port input control is in the disable level state ● 0b1: Port input control is in the enable level state	RO
13:11	*Reserved*	-	-
10	PORTINF3	Port Input 3 Control Flag Bit Set when EMB_STAT.PORTINST3=1. Clear 0 when EMB_STATCLR.PORTINFCLR3 writes 1.	RO
9	PORTINF2	Port Input 2 Control Flag Bit Set when EMB_STAT.PORTINST2=1. Clear 0 when EMB_STATCLR.PORTINFCLR2 writes 1.	RO
8	PORTINF1	Port Input 1 Control Flag Bit Set when EMB_STAT.PORTINST1 is 1. Clear 0 when EMB_STATCLR.PORTINFCLR1 writes 1.	RO
7	OSST	XTAL Stops Oscillating Status ● 0b0: XTAL doesn't stop oscillating ● 0b1: XTAL stops oscillating	RO
6	CMPST	Voltage Comparator Status ● 0b0: The voltage comparator comparison result flag bit is not set ● 0b1: The voltage comparator comparison result flag bit is set	RO
5	PWMST	PWM Output Status ● 0b0: No PWM output in-phase occurs ● 0b1: PWM output in-phase occurs	RO

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Bit	Name	Functional Description	Access
4	*Reserved*	-	-
3	OSF	XTAL Stops Oscillating Flag Bit Set when EMB_STAT.OSST is 1. Clear 0 when EMB_STATCLR.OSFCLR writes 1.	RO
2	CMPF	CMP Control Flag Bit Set when EMB_STAT.CMPST is 1. Clear 0 when EMB_STATCLR.CMPFCLR writes 1.	RO
1	PWMSF	PWM Output In-phase Control Flag Bit Set when EMB_STAT.PWMST=1. Clear 0 when EMB_STATCLR.PWMSCLR writes 1.	RO
0	*Reserved*	-	-

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18.3.8 EMB Status Register (EMB_STAT) (Group1)

Offset	Bit Position																													
0x0C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved															PORTINST3	PORTINST2	PORTINST1	Reserved			PORTINF3	PORTINF2	PORTINF1	OSST	CMPST	Reserved		OSF	CMPF	Reserved	
Access																RO	RO	RO				RO	RO	RO	RO	RO			RO	RO		

Bit	Name	Functional Description	Access
31:17	*Reserved*	-	-
16	PORTINST3	Port Input 3 Control Status ● 0b0: Port input control is in the disable level state ● 0b1: Port input control is in the enable level state	RO
15	PORTINST2	Port Input 2 Control Status ● 0b0: Port input control is in the disable level state ● 0b1: Port input control is in the enable level state	RO
14	PORTINST1	Port Input 1 Control Status ● 0b0: Port input control is in the disable level state ● 0b1: Port input control is in the enable level state	RO
13:11	*Reserved*	-	-
10	PORTINF3	Port Input 3 Control Flag Bit Set when EMB_STAT.PORTINST3=1. Clear 0 when EMB_STATCLR.PORTINFCLR3 writes 1.	RO
9	PORTINF2	Port Input 2 Control Flag Bit Set when EMB_STAT.PORTINST2=1. Clear 0 when EMB_STATCLR.PORTINFCLR2 writes 1.	RO
8	PORTINF1	Port Input 1 Control Flag Bit Set when EMB_STAT.PORTINST1 is 1 Clear 0 when EMB_STATCLR.PORTINFCLR1 writes 1.	RO
7	OSST	XTAL Stops Oscillating Status ● 0b0: XTAL doesn't stop oscillating ● 0b1: XTAL stops oscillating	RO
6	CMPST	Voltage Comparator Status ● 0b0: The voltage comparator comparison result flag bit is not set ● 0b1: The voltage comparator comparison result flag bit is set	RO
5:4	*Reserved*	-	-

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Bit	Name	Functional Description	Access
3	OSF	XTAL Stops Oscillating Flag Bit Set when EMB_STAT.OSST is 1. Clear 0 when EMB_STATCLR.OSFCLR writes 1.	RO
2	CMPF	CMP Control Flag Bit Set when EMB_STAT.CMPST is 1. Clear 0 when EMB_STATCLR.CMPFCLR writes 1.	RO
1:0	*Reserved*	-	-

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18.3.9 EMB Status Clear Register (EMB_STATCLR) (Group0)

Offset	Bit Position																													
0x10	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																					PORTINFCLR3	PORTINFCLR2	PORTINFCLR1	Reserved				OSFCLR	CMPFCLR	PWMSFCLR	Reserved
Access																						WO	WO	WO					WO	WO	WO	

Bit	Name	Functional Description	Access
31:11	*Reserved*	-	-
10	PORTINFCLR3	Reset EMB_STAT.PORTINF3 Write 1 to clear EMB_STAT.PORTINF3 to 0, write 0 has no effect	WO
9	PORTINFCLR2	Reset EMB_STAT.PORTINF2 Write 1 to clear EMB_STAT.PORTINF2 to 0, write 0 has no effect	WO
8	PORTINFCLR1	Reset EMB_STAT.PORTINF1 Write 1 to clear EMB_STAT.PORTINF1 to 0, write 0 has no effect	WO
7:4	*Reserved*	-	-
3	OSFCLR	Reset EMB_STAT.OSF Write 1 to clear EMB_STAT.OSF to 0 (when EMB_STAT.OSST=0), write 0 has no effect	WO
2	CMPFCLR	Reset EMB_STAT.CMPF Write 1 to clear EMB_STAT.CMPF to 0 (when EMB_STAT.CMPST=0), write 0 has no effect	WO
1	PWMSFCLR	Reset EMB_STAT.PWMSF Write 1 to clear EMB_STAT.PWMSF to 0 (when EMB_STAT.PWMST=0), write 0 has no effect	WO
0	*Reserved*	-	-

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18.3.10 EMB Status Clear Register (EMB_STATCLR) (Group1)

Offset	Bit Position																													
0x10	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																					PORTINFCLR3	PORTINFCLR2	PORTINFCLR1	Reserved				OSFCLR	CMPFCLR	Reserved	
Access																						WO	WO	WO					WO	WO		

Bit	Name	Functional Description	Access
31:11	*Reserved*	-	-
10	PORTINFCLR3	Reset EMB_STAT.PORTINF3 Write 1 to clear EMB_STAT.PORTINF3 to 0, write 0 has no effect	WO
9	PORTINFCLR2	Reset EMB_STAT.PORTINF2 Write 1 to clear EMB_STAT.PORTINF2 to 0, write 0 has no effect	WO
8	PORTINFCLR1	Reset EMB_STAT.PORTINF1 Write 1 to clear EMB_STAT.PORTINF1 to 0, write 0 has no effect	WO
7:4	*Reserved*	-	-
3	OSFCLR	Reset EMB_STAT.OSF Write 1 to clear EMB_STAT.OSF to 0 (when EMB_STAT.OSST=0), write 0 has no effect	WO
2	CMPFCLR	Reset EMB_STAT.CMPF Write 1 to clear EMB_STAT.CMPF to 0 (when EMB_STAT.CMPST=0), write 0 has no effect	WO
1:0	*Reserved*	-	-

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18.3.11 EMB Interrupt Enable Register (EMB_INTEN) (Group0)

Offset	Bit Position																													
0x14	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																					PORTININTEN3	PORTININTEN2	PORTININTEN1	Reserved				OSINTEN	CMPINTEN	PWMSINTEN	Reserved
Access																						RW	RW	RW					RW	RW	RW	

Bit	Name	Functional Description	Access
31:11	*Reserved*	-	-
10	PORTININTEN3	Port Input 3 Control Interrupt Enabled ● 0b0: Port input control does not generate interrupt ● 0b1: Port input control generates interrupt	RW
9	PORTININTEN2	Port Input 2 Control Interrupt Enabled ● 0b0: Port input control does not generate interrupt ● 0b1: Port input control generates interrupt	RW
8	PORTININTEN1	Port Input 1 Control Interrupt Enabled ● 0b0: Port input control does not generate interrupt ● 0b1: Port input control generates interrupt	RW
7:4	*Reserved*	-	-
3	OSINTEN	XTAL Stops Oscillating Control Interrupt Enabled ● 0b0: XTAL stops oscillating control does not generate interrupt ● 0b1: XTAL stops oscillating control generates interrupt	RW
2	CMPINTEN	CMP Comparison Result Control Interrupt Enabled ● 0b0: CMP comparison result control does not generate interrupt ● 0b1: CMP comparison result control generates interrupt	RW
1	PWMSINTEN	PWM Output In-phase Control Interrupt Enabled ● 0b0: PWM output in-phase control does not generate interrupt ● 0b1: PWM output in-phase control generates interrupt	RW
0	*Reserved*	-	-

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18.3.12 EMB Interrupt Enable Register (EMB_INTEN) (Group1)

Offset	Bit Position																													
0x14	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																					PORTININTEN3	PORTININTEN2	PORTININTEN1	Reserved				OSINTEN	CMPINTEN	Reserved	
Access																						RW	RW	RW					RW	RW		

Bit	Name	Functional Description	Access
31:11	*Reserved*	-	-
10	PORTININTEN3	Port Input 3 Control Interrupt Enabled ● 0b0: Port input control does not generate interrupt ● 0b1: Port input control generates interrupt	RW
9	PORTININTEN2	Port Input 2 Control Interrupt Enabled ● 0b0: Port input control does not generate interrupt ● 0b1: Port input control generates interrupt	RW
8	PORTININTEN1	Port Input 1 Control Interrupt Enabled ● 0b0: Port input control does not generate interrupt ● 0b1: Port input control generates interrupt	RW
7:4	*Reserved*	-	-
3	OSINTEN	XTAL Stops Oscillating Control Interrupt Enabled ● 0b0: XTAL stops oscillating control does not generate interrupt ● 0b1: XTAL stops oscillating control generates interrupt	RW
2	CMPINTEN	CMP Comparison Result Control Interrupt Enabled ● 0b0: CMP comparison result control does not generate interrupt ● 0b1: CMP comparison result control generates interrupt	RW
1:0	*Reserved*	-	-

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18.3.13 EMB Control PWM Output Release Select Register (EMB_RLSSEL) (Group0)

Offset	Bit Position																													
0x18	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																					PORTINRSEL3	PORTINRSEL2	PORTINRSEL1	Reserved				OSRSEL	CMPRSEL	PWMRSEL	Reserved
Access																						RW	RW	RW					RW	RW	RW	

Bit	Name	Functional Description	Access
31:11	*Reserved*	-	-
10	PORTINRSEL3	Port Input 3 Control Release Selection ● 0b0: Release PWM output control when EMB_STAT.PORTINF3=0 ● 0b1: Release PWM output control when EMB_STAT.PORTINST3=0	RW
9	PORTINRSEL2	Port Input 2 Control Release Selection ● 0b0: Release PWM output control when EMB_STAT.PORTINF2=0 ● 0b1: Release PWM output control when EMB_STAT.PORTINST2=0	RW
8	PORTINRSEL1	Port Input 1 Control Release Selection ● 0b0: Release PWM output control when EMB_STAT.PORTINF1=0 ● 0b1: Release PWM output control when EMB_STAT.PORTINST1=0	RW
7:4	*Reserved*	-	-
3	OSRSEL	XTAL Stops Oscillating Control Release Selection ● 0b0: Release PWM output control when EMB_STAT.OSF=0 ● 0b1: Release PWM output control when EMB_STAT.OSST=0	RW
2	CMPRSEL	CMP Comparison Result Control Release Selection ● 0b0: Release PWM output control when EMB_STAT.CMPF=0 ● 0b1: Release PWM output control when EMB_STAT.CMPST=0	RW
1	PWMRSEL	PWM Output Control Release Selection ● 0b0: Release PWM output control when EMB_STAT.PWMSF=0 ● 0b1: Release PWM output control when EMB_STAT.PWMST=0	RW
0	*Reserved*	-	-

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18.3.14 EMB Control PWM Output Release Select Register (EMB_RLSSEL) (Group1)

Offset	Bit Position																													
0x18	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																					PORTINRSEL3	PORTINRSEL2	PORTINRSEL1	Reserved				OSRSEL	CMPRSEL	Reserved	
Access																						RW	RW	RW					RW	RW		

Bit	Name	Functional Description	Access
31:11	*Reserved*	-	-
10	PORTINRSEL3	Port Input 3 Control Release Selection ● 0b0: Release PWM output control when EMB_STAT.PORTINF3=0 ● 0b1: Release PWM output control when EMB_STAT.PORTINST3=0	RW
9	PORTINRSEL2	Port Input 2 Control Release Selection ● 0b0: Release PWM output control when EMB_STAT.PORTINF2=0 ● 0b1: Release PWM output control when EMB_STAT.PORTINST2=0	RW
8	PORTINRSEL1	Port Input 1 Control Release Selection ● 0b0: Release PWM output control when EMB_STAT.PORTINF1=0 ● 0b1: Release PWM output control when EMB_STAT.PORTINST1=0	RW
7:4	*Reserved*	-	-
3	OSRSEL	XTAL Stops Oscillating Control Release Selection ● 0b0: Release PWM output control when EMB_STAT.OSF=0 ● 0b1: Release PWM output control when EMB_STAT.OSST=0	RW
2	CMPRSEL	CMP Comparison Result Control Release Selection ● 0b0: Release PWM output control when EMB_STAT.CMPF=0 ● 0b1: Release PWM output control when EMB_STAT.CMPST=0	RW
1:0	*Reserved*	-	-

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19 General Timer (TimerA)

19.1 Introduction

The General Timer A (TimerA) is a timer with a 16-bit counting width and 2/6-channel PWM output. The timer supports two waveform modes, triangle wave and sawtooth wave, and can generate various PWM waveforms (single-side aligned PWM, double-side symmetrical PWM); supports synchronous start of counter; the compare reference value register supports buffer function; supports cascading between units to achieve 32-bit counting; supports 2-phase quadrature encoding count and 3-phase quadrature encoding count. This product series is equipped with 5 TimerA units, Unit 1 (TimerA_1) to Unit 4 (TimerA_4) each have 2 channels of PWM output, Unit 5 (TimerA_5) has 6 channels of PWM output. The 5 units can achieve a maximum of 14 channels of PWM output in total.

19.2 Features

The basic functions and features of TimerA are shown in the table below:

Table 19-1 Basic Functions and Features of TimerA

Waveform mode	Sawtooth wave, triangular wave
Basic function	Up/Down-counting direction
	Synchronous startup counter
	Reference value buffer function
	32-bit cascading count
	Quadrature encoding count
	2/6 PWM output
	Compare match event output
Interrupt type	Compare match interrupt
	Period match interrupt

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19.3 Functional Description

19.3.1 TimerA Block Diagram

The basic block diagram of TimerA is shown in the figure. In the figure, "<t>" is the unit number, that is, "<t>" is 1-5. In the rest of this section, "<t>" refers to the unit number and will not be repeated here.

This series of products carries 5 units of TimerA, among which the bus clock and count clock of units 1 to 5 are both PCLK1 (in this case, the PCLK shown in the block diagram refers to PCLK1). The counting frequency division clock source of each unit and the sampling reference clock source of the port digital filter are the same as its bus clock and counting clock.

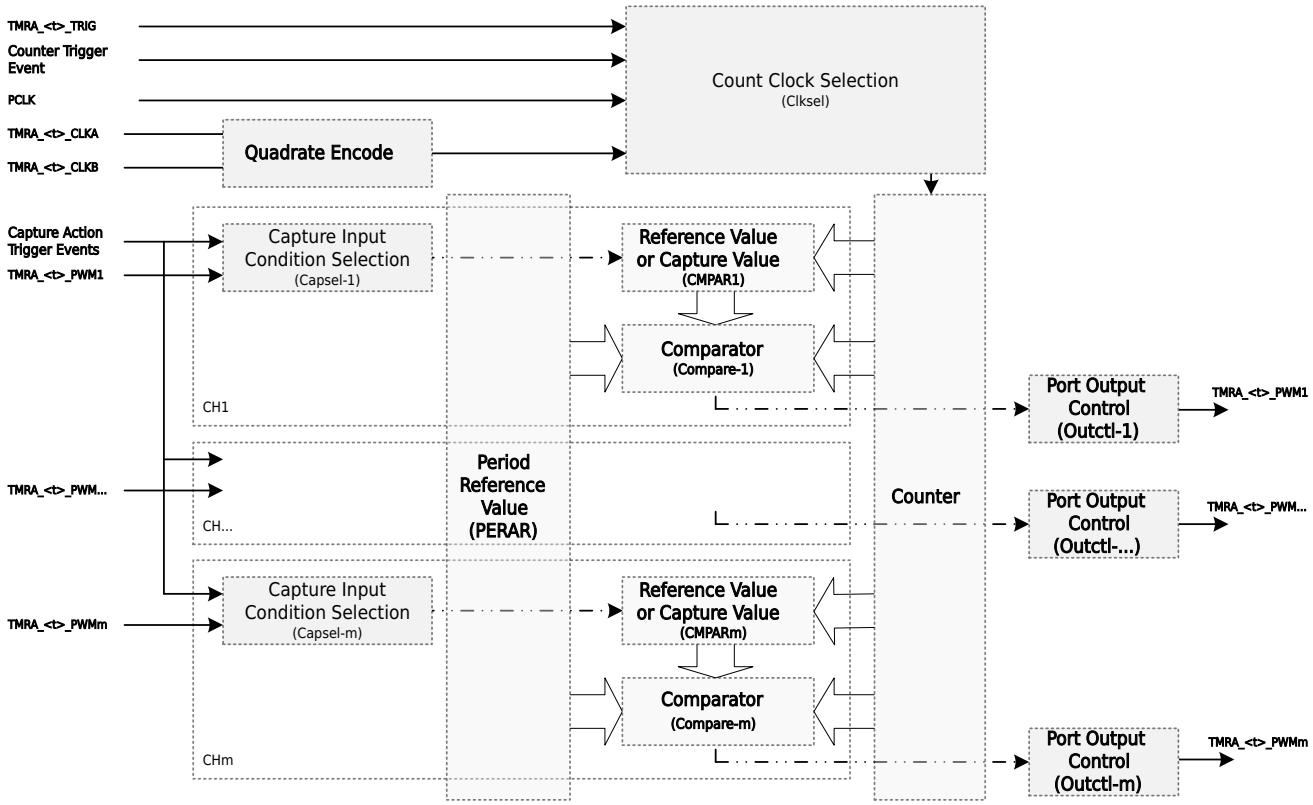

Figure 19-1 TimerA Basic Block Diagram

The following table lists the input and output ports of TimerA.

Table 19-2 TimerA Port List

Port Name	Direction	Function
TMRA_<t>_PWMm	Input/Output	Capture input event port or PWM output port (m=1-2/6)
TMRA_<t>_CLKA	Input	Quadrature encoder counting event input port
TMRA_<t>_CLKB		
TMRA_<t>_TRIG	Input	Hardware-triggered start, stop, clear event input port

19.3.2 Symmetric Units

TimerA unit 1 and unit 2 are symmetric units, as are unit 3 and unit 4, and so on. Symmetric units can be linked to achieve cascaded counting, synchronized start, and other functions, as described in the following sections.

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19.3.3 Basic Actions

19.3.3.1 Waveform Mode

TimerA has two basic counting wave modes: sawtooth wave mode and triangle wave mode. The basic waveforms of the two waveform modes are as follows:

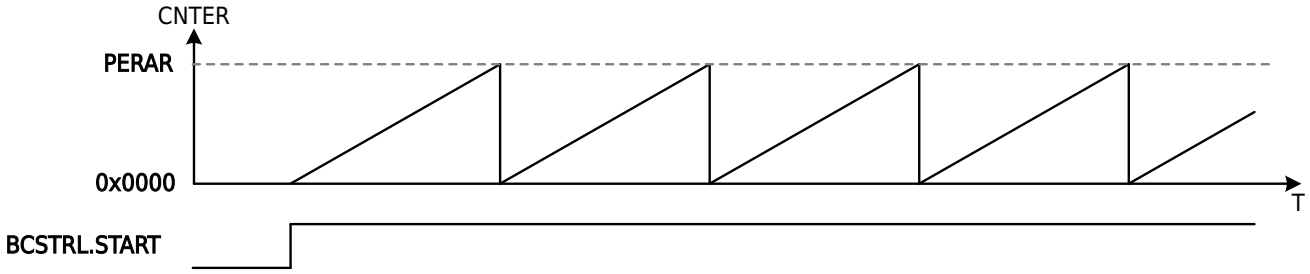

Figure 19-2 Sawtooth Waveform (Counting Up)

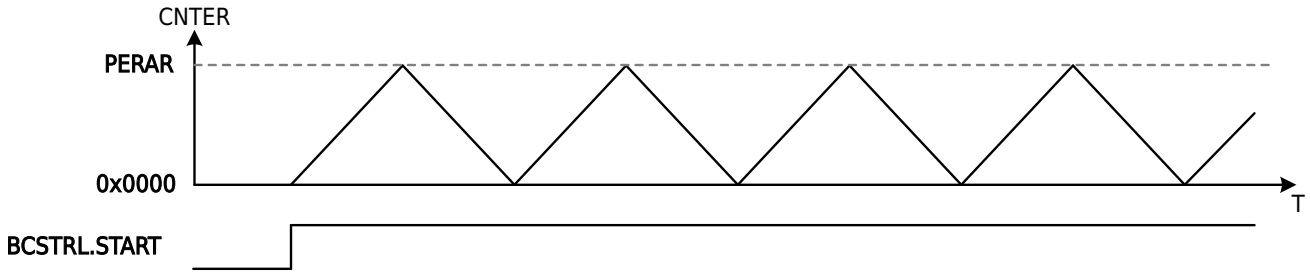

Figure 19-3 Triangle Waveform

19.3.3.2 Compare Output

Each TimerA unit contains 2/6 channels compare output (TMRA_<t>_PWMm), which can output a specified level when the count value matches the compare reference value. The TMRA_CMPARm registers correspond to the count compare reference value for the TMRA_<t>_PWMm output ports. When the timer count value equals TMRA_CMPARm, the TMRA_<t>_PWMm port outputs the specified level (m=1-2/6).

The output level of the TMRA_<t>_PWMm port at various timing events -- such as the start of counting, stop of counting, count compare match, and count period match -- can be configured using the STAC, STPC, CMPC, PERC, and FORC bits in PCONRm register (m=1-2/6). The diagram below illustrates an example of compare output action for Unit 1.

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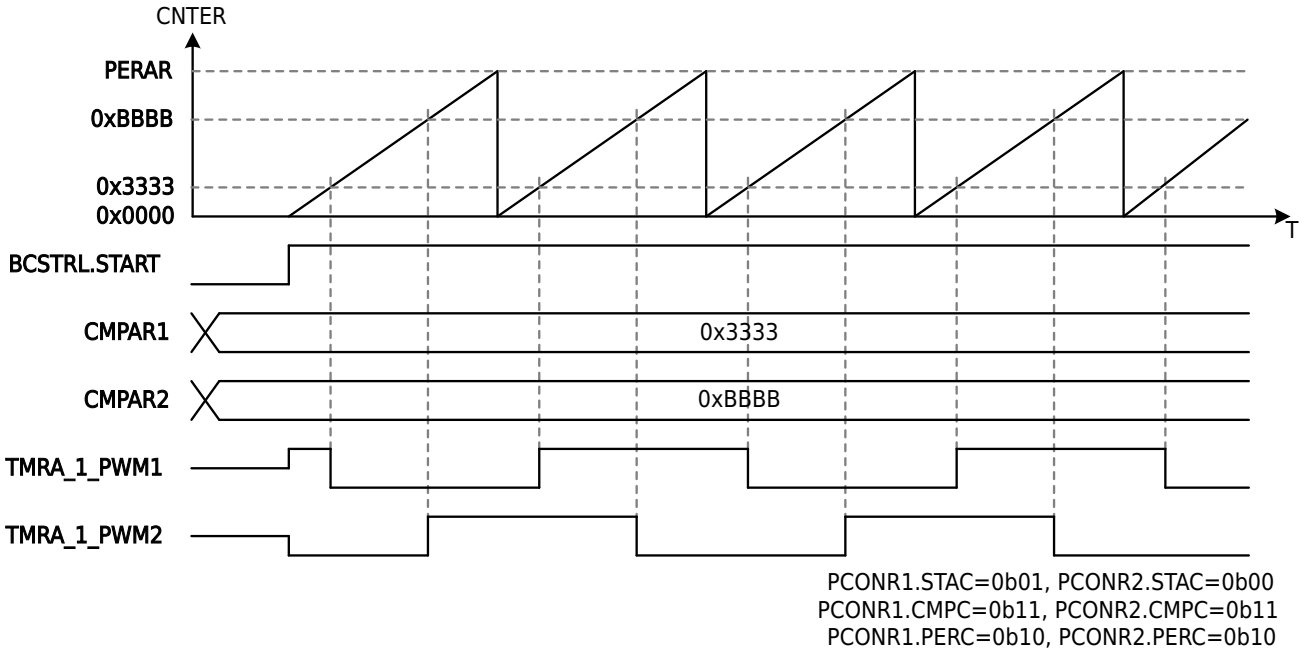

Figure 19-4 Compare Output Action

19.3.3.3 Capture Input

Each PWM output channel of every TimerA unit is equipped with a capture input function that stores the captured count value. When the CCONR.CAPMD bit in the Capture Control Register (CCONRm) is set to 1, the capture input function becomes active. At this point, when the corresponding capture input condition is selected and this condition is valid, the current count value is stored in the corresponding register (CMPARm) (m=1-2/6).

The capture input condition can select the internal capture action trigger event (selected by the TMRA_TRGSELx register, for the specific register content, see the "TimerA Hardware Trigger Event Selection Register (TMRA_TRGSELx) (x=0-1) " in the "Automatic Operation System (AOS) " chapter), TMRA_<t>_PWMm port input, etc. The specific condition selection can be set through the CCONRm.HICP bit (m=1-2/6).

The internal trigger event selection register is shared by all 5 units of TimerA, and the specific allocation is shown in the following table.

Table 19-3 TRGSEL Selection Relationship Table for Internal Trigger Events

TimerA Unit	Event Classification	Corresponding Selection Register
TimerA_1	Counter Trigger Events: TRGSEL selection events specified by HCONR, HCUPR, and HCDOR	TMRA_TRGSEL0
TimerA_2		TMRA_TRGSEL1
TimerA_3		TMRA_TRGSEL0
TimerA_4		TMRA_TRGSEL1
TimerA_5		TMRA_TRGSEL0
TimerA_1	Capture Action Trigger Events: TRGSEL selection events specified by CCONR	TMRA_TRGSEL1
TimerA_2		TMRA_TRGSEL0
TimerA_3		TMRA_TRGSEL1
TimerA_4		TMRA_TRGSEL0

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TimerA Unit	Event Classification	Corresponding Selection Register
TimerA_5	Capture Action Trigger Events: TRGSEL selection events specified by CCONR	TMRA_TRGSEL1

The following figure shows an example of the capture input action.

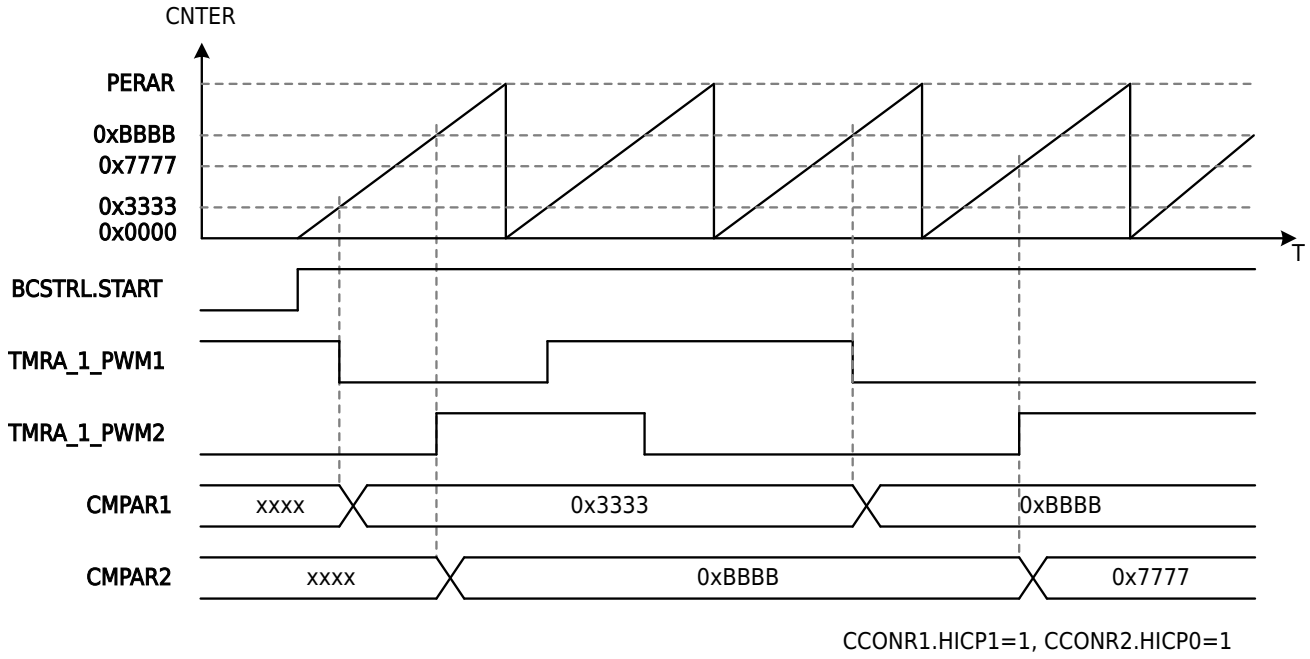

Figure 19-5 Capture Input Action

19.3.4 Clock Source Selection

The TimerA count clock can be selected from the following sources:

1. 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024 division of PCLK (configured by BCSTRL.CKDIV)
2. TMRA_<t>_TRIG port event input (configured by HCUPR.HCUPn or HCDOR.HCDOn) (n=8-9)
3. Internal counter trigger event input (configured by HCUPR.HCUP10 or HCDOR.HCDO10)
4. Count overflow or underflow event input for symmetric units (configured by HCUPR.HCUPn or HCDOR.HCDOn) (n=11-12)
5. TMRA_<t>_CLKA and TMRA_<t>_CLKB port quadrature encoder input (configured by HCUPR.HCUPn or HCDOR.HCDOn) (n=0-7)

When the clock source selection is set to 1, the timer operates in software counting mode. When set to others, the timer operates in hardware counting mode.

In hardware counting mode:

- Ensure that BCSTRL.CKDIV is 0.
- Each count clock source is independent and can be enabled or disabled individually.
- The software clock is automatically disabled.

19.3.5 Count Direction

The count direction of TimerA can be changed via software. The method of changing the counting direction may vary slightly depending on the selected waveform mode.

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19.3.5.1 Sawtooth Wave Count Direction

In sawtooth wave counting mode, the counting direction can be set either during the timer counting or when the counting is stopped. Once set, the direction changes immediately.

19.3.5.2 Triangle Wave Count Direction

In the triangle wave counting mode, the counting direction is set when counting stops. The direction setting is disabled when counting is in progress.

19.3.6 Digital Filtering

Each unit's TMRA_<t>_CLKA, TMRA_<t>_CLKB, TMRA_<t>_TRIG, TMRA_<t>_PWMm (when capturing input function) port inputs have digital filtering functions. The filter function of each port can be enabled and the filter clock can be selected by setting the corresponding bits of the FCONR register and the CCONRm register (m=1-2/6).

When the port level sampled by the filter sampling reference clock remains consistent for 3 consecutive times, that level is transmitted as a active level and transmitted to the internal block. Levels with fewer than 3 consistent samples are filtered as external noise and not transmitted to the internal block. The figure below shows an example of TMRA_1_CLKA port filtering action.

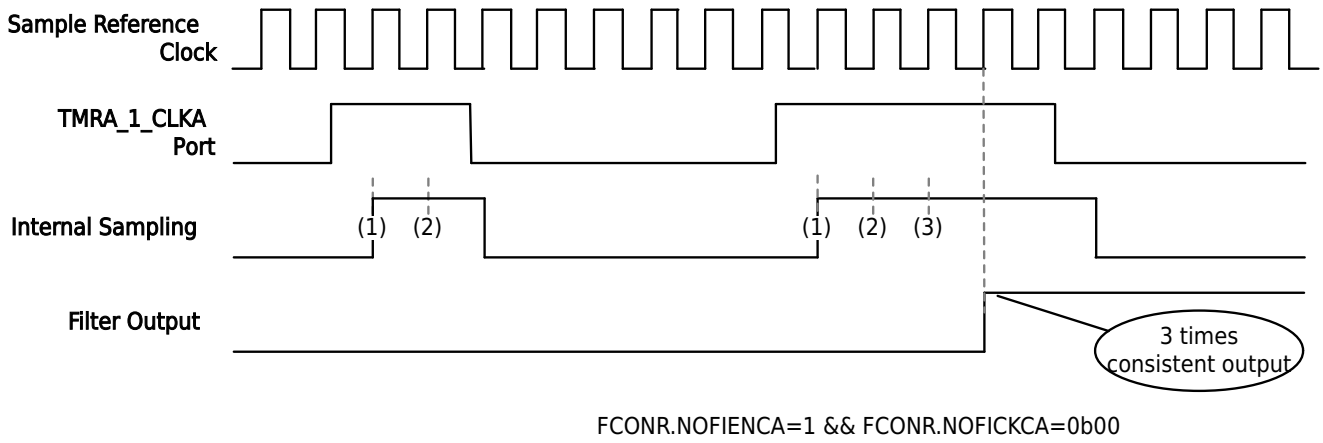

Figure 19-6 Filtering Function of Clock Input Port

19.3.7 Synchronous Starting

The symmetric units of TimerA can realize software synchronous start or hardware synchronous start, and the odd unit synchronously starts the even unit.

When the BCSTRL.SYNST bit of the even unit in the symmetric unit is set to 1, the synchronous start function of the even unit and the odd unit is enable. At this time, if the software sets the BCSTRL.START bit of the odd unit to 1, the counter of the synchronized even unit starts software synchronous counting; if the hardware sets any bit in HCONR.HSTA1-0 of the even unit to 1, and the corresponding hardware event occurs, the counter of the synchronized even unit starts hardware synchronous counting. When the hardware synchronous count start function is selected, the corresponding bits of HCONR.HSTA1-0 of the synchronized even unit must also be set to active.

The following figure shows an example of software synchronization startup when BCSTRL.SYNST=1 of unit 2 is set.

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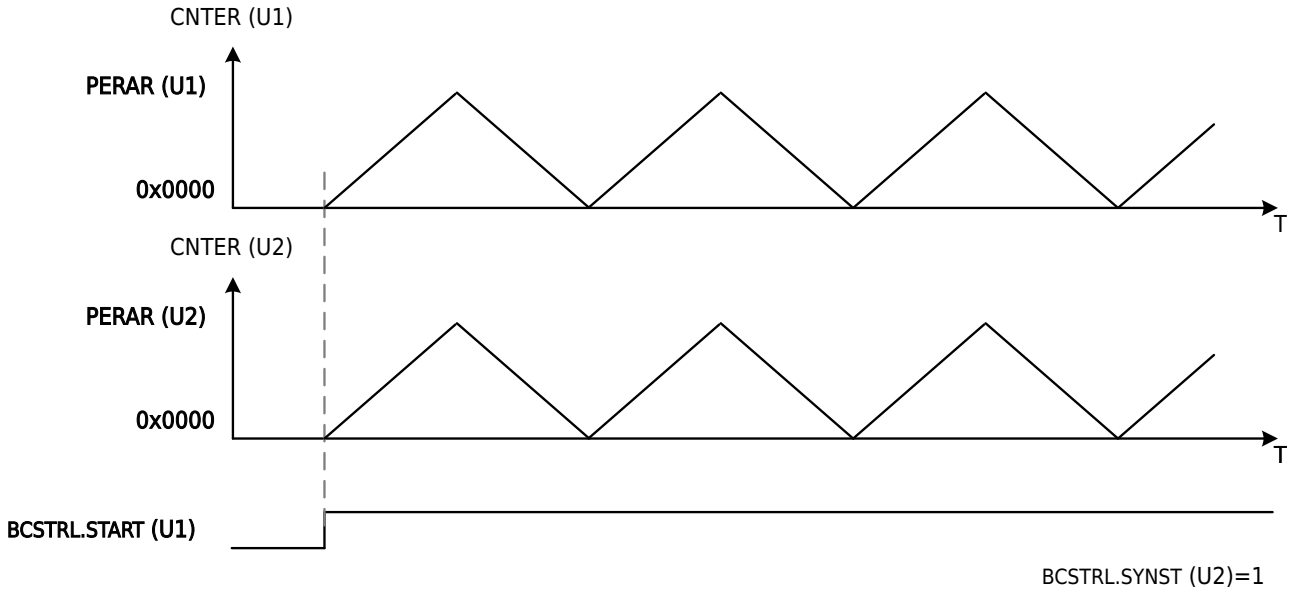

Figure 19-7 Software Synchronization Action

In addition, the product is equipped with a Counter Synchronization Enable Register TMR_SYNENR to synchronously start all the timers (including Timer0, Timer4, TimerA) carried by the product. For usage details and register descriptions, refer to the "General Timer (Timer0)" chapter.

19.3.8 Buffer Function

A total of 2/6 compare reference registers (CMPARm) (m=1-2/6) of TimerA can be used in pairs to implement the buffer function. That is, CMPAR2 is used as the buffer value of CMPAR1, CMPAR4 is used as the buffer value of CMPAR3, CMPAR6 is used as the buffer value of CMPAR5. The buffer control register (BCONRm) (m=1-3) controls the three groups of buffer functions respectively.

When the BCONRm.BEN (m=1-3) bit is set, the buffer function becomes active. When the counter reaches a certain time point, a buffer transmission occurs (CMPAR2/4/6->CMPAR1/3/5). The "Certain Time Point" includes the following situations:

1. In hardware counting mode, the counter reaches the overflow point (when HCUPR!=0), the underflow point (when HCDOR!=0), or a hardware clear action occurs for the counter.
2. In sawtooth counting mode (BCSTRL.MODE=0), the counter counts to the overflow point (BCSTRL.DIR=1) or underflow point (BCSTRL.DIR=0) or the hardware clears the counter.
3. In triangle wave counting mode (BCSTRL.MODE=1), count to peak point (BCSTRL.DIR=1 && BCONRm.BSE0=1) (m=1-3)
4. In triangle wave counting mode (BCSTRL.MODE=1), count to valley point (BCSTRL.DIR=0 && BCONRm.BSE1=1) (m=1-3)

When the BCONR1.BSEN bit is set, the buffer special function becomes active. When the CNTER of the symmetric unit is read, a buffer transmission occurs in the CMPAR of this unit (CMPAR2->CMPAR1).

Note

Only Unit 1-4 support buffer special function.

The figure below is a schematic diagram of buffer transmission in sawtooth mode.

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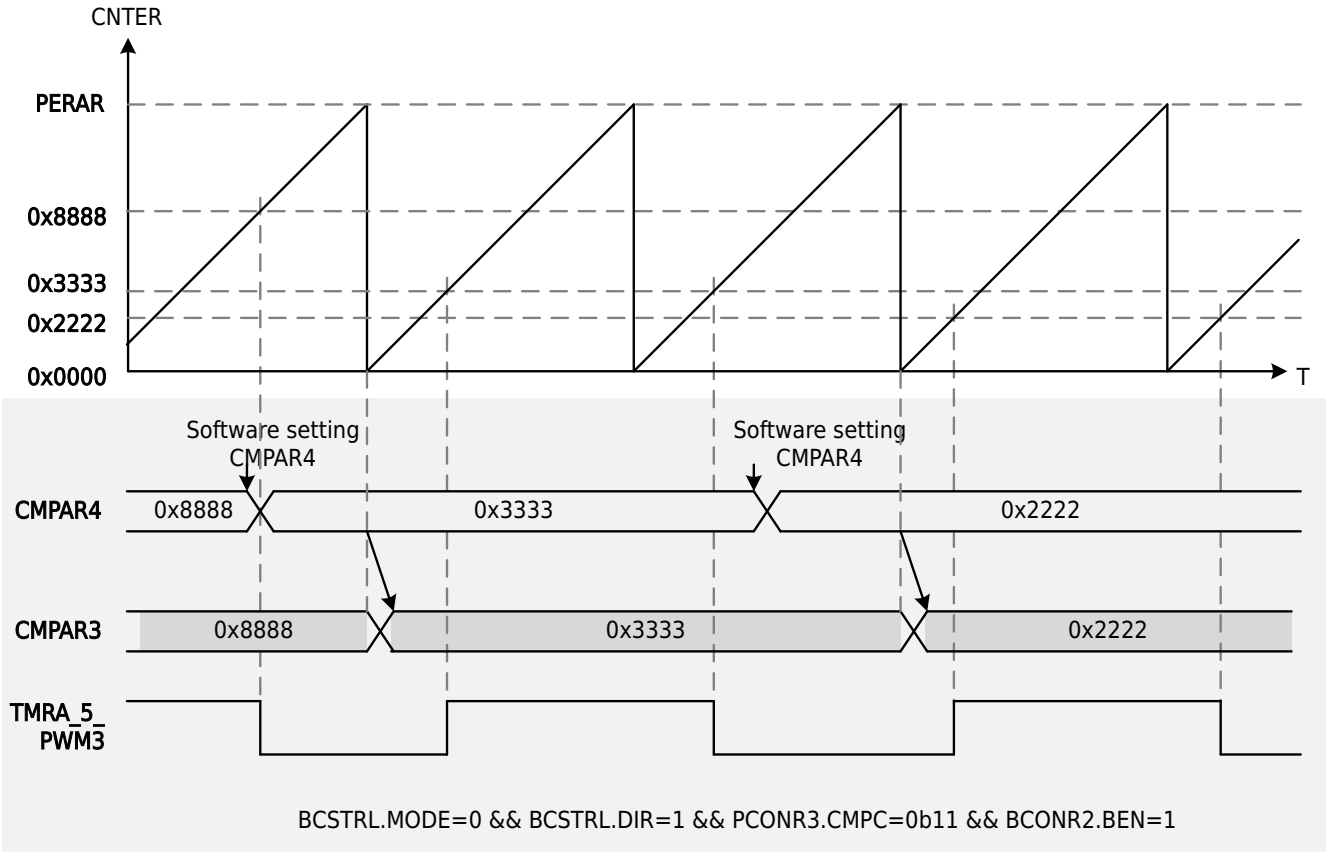

Figure 19-8 Buffer Action in Sawtooth Mode

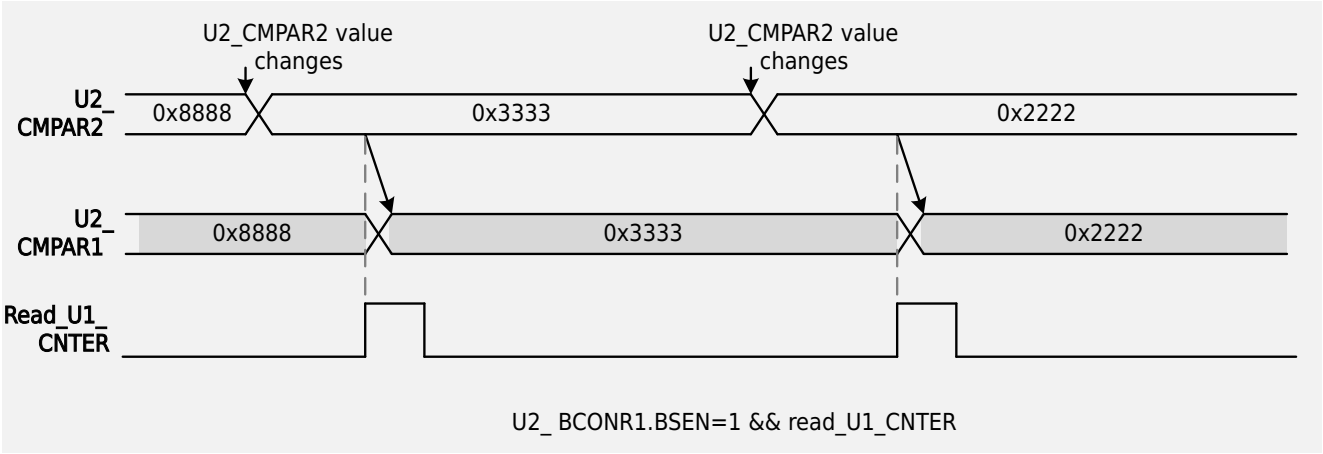

Figure 19-9 Buffer and Special Buffer Actions in Sawtooth Mode

19.3.9 Cascade Counting

As described in the "Clock Source Selection" section, when the clock source is set to 4, the counting clock of this unit is selected as the count overflow (count up or count down) event of the symmetric unit. This allows the two units to be cascade combined, creating a 32-bit counter. In cascaded counting, the CNTER register of the symmetric unit serves as the lower 16-bit counter, while the CNTER register of this unit serves as the upper 16-bit counter.

For example, in triangular up-counting mode (BCSTRL.MODE=1, BCSTRL.DIR=1), if unit 1 is configured to use PCLK as the counting clock and unit 2 is configured to use the overflow event of unit 1 as its counting clock source (TMRA_HCUPR.HCUP11=1 in unit 2), then starting the counters of unit 2 and unit 1 (start unit 2 first, then unit 1) enables cascaded counting. In this configuration, unit 1's CNTER serves

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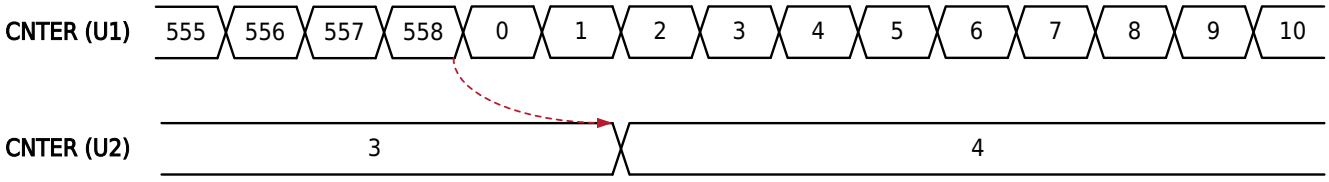
as the lower 16-bit counter, and unit 2's CNTER serves as the upper 16-bit counter. The figure below is a schematic diagram of the cascade counting of units 1 and 2.



PERAR=0x0558 (U1), HCUPR=0x0800 (U2)

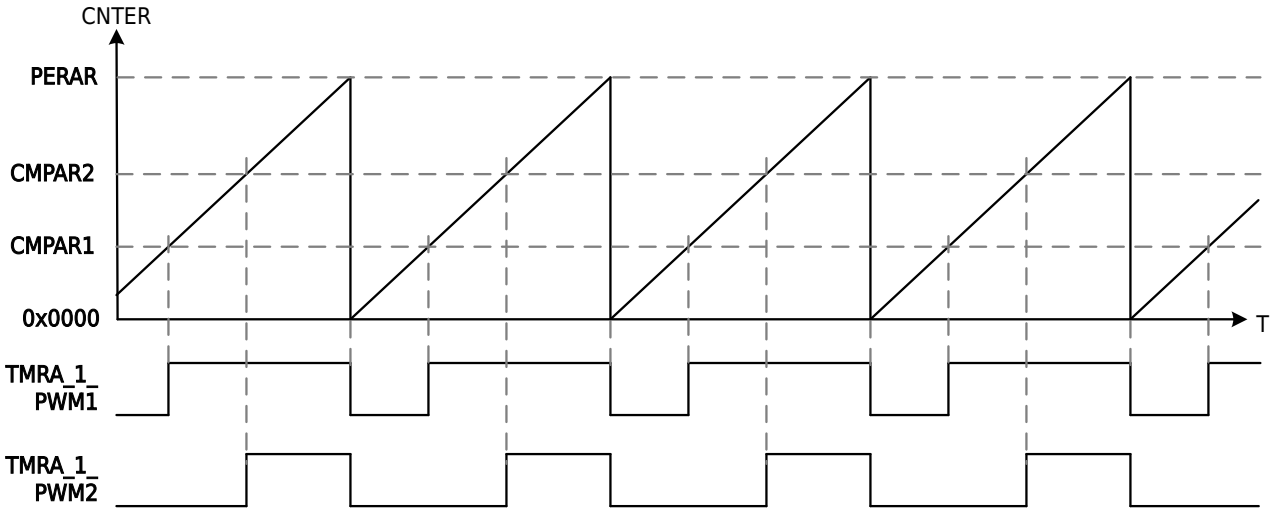
Figure 19-10 32-bit Cascade Counting Action

19.3.10 General PWM Output

19.3.10.1 Single-Side Aligned PWM Output

In sawtooth counting mode, each channel within a unit can be configured via various port control settings to achieve single-side aligned PWM output (aligned at the period match point). For example, by setting the output to toggle on compare match (PCONR.CMPC=0b11) and also to toggle on period match (PCONR.PERC=0b11), an edge-aligned PWM waveform can be generated within one counting period.

The figure below shows an example of single-side aligned PWM output waveform in sawtooth mode.



BCSTRL.MODE=0 && PCONRm.CMPC=0b11 && PCONRm.PERC=0b11 (m=1-2)

Figure 19-11 Example of Single-Side Aligned PWM Output

19.3.10.2 Double-Side Symmetric PWM Output

In triangle counting mode, each channel within a unit can be configured via various port control settings to achieve double-side symmetric PWM output, where the waveform is symmetrical around the counting peak point. Depending on the output relationship between channels, either independent PWM outputs or complementary PWM outputs can be realized.

The figure below shows an example of double-side symmetric PWM output waveforms for channels 1, 2, 3, and 4 in triangle mode. Among them, channels 1 and 2 can be used as a pair of complementary PWM outputs.

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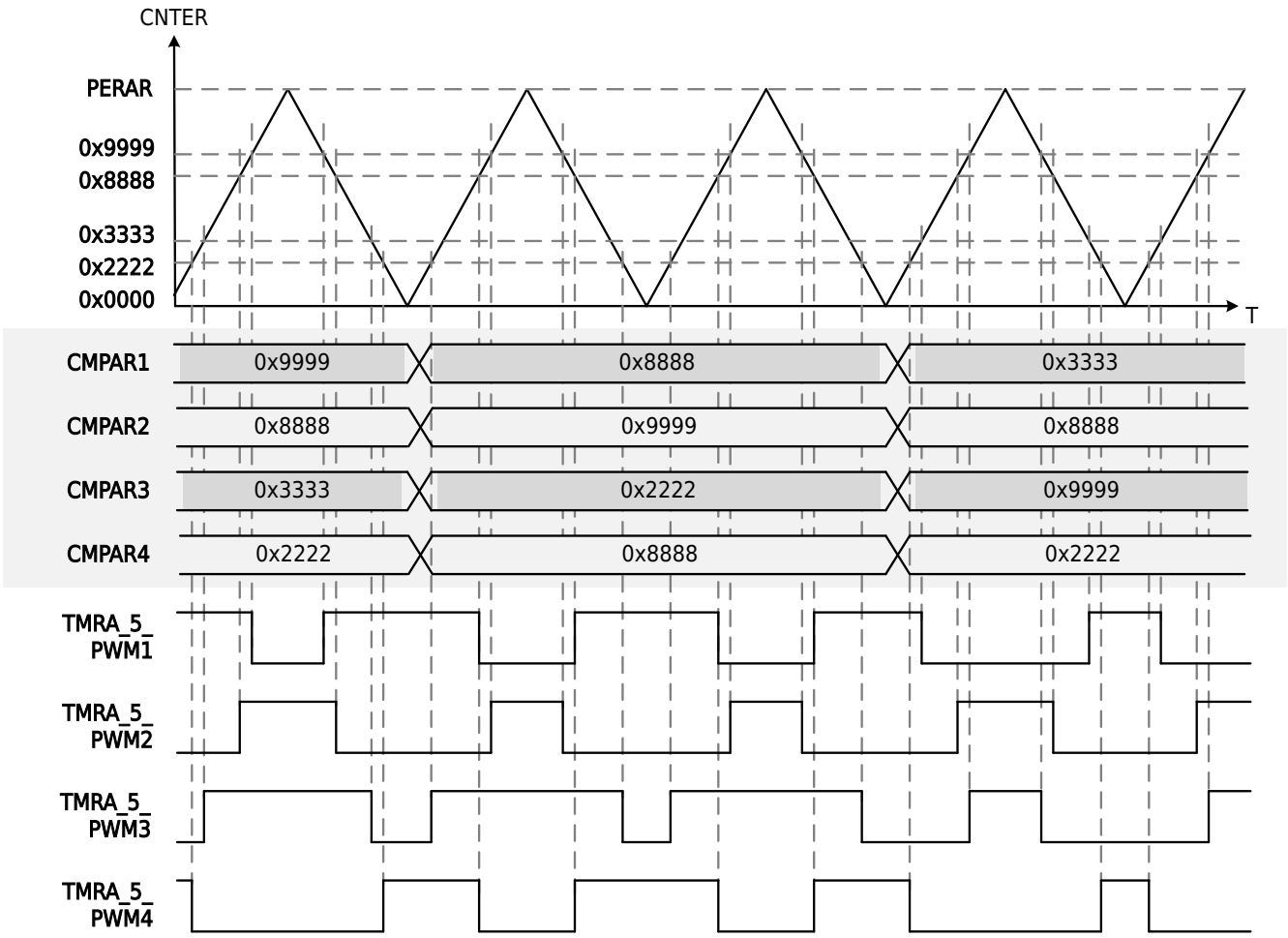

Figure 19-12 Example of Double-Side Symmetric PWM Output

19.3.11 Quadrature Encoding Counting

By considering the TMRA_<t>_CLKA input as AIN input, the TMRA_<t>_CLKB input as BIN input, and the TMRA_<t>_TRIG input as ZIN input, TimerA can implement quadrature encoding counting of three inputs.

The individual actions of AIN and BIN of each unit can realize the position counting mode; the combined actions of AIN, BIN and ZIN of two units can realize the revolution counting mode. The unit used for position counting is called the position counting unit, and the unit used for revolution counting is called the revolution counting unit. In the revolution counting mode, every two units are combined with each other (unit 1 and 2 are combined; unit 3 and 4 are combined), and the position counting unit and the revolution counting unit in the combination can be specified arbitrarily.

The counting condition enable of AIN and BIN is realized by setting the quadrature relationship between TMRA_<t>_CLKA and TMRA_<t>_CLKB in the HCUPR register and the HCDOR register; the input action of ZIN is realized by setting the clear enable bit of the HCONR register of the position counting unit to clear the position timer, and by setting HCUPR register of the revolution unit to count the revolution timer.

19.3.11.1 Position Counting Mode

The quadrature encoder position counting mode enables the implementation of basic counting, phase difference counting, and direction counting based on the input signals from AIN and BIN.

Basic Counting

Basic counting uses the input clock from either the AIN or BIN port to count.

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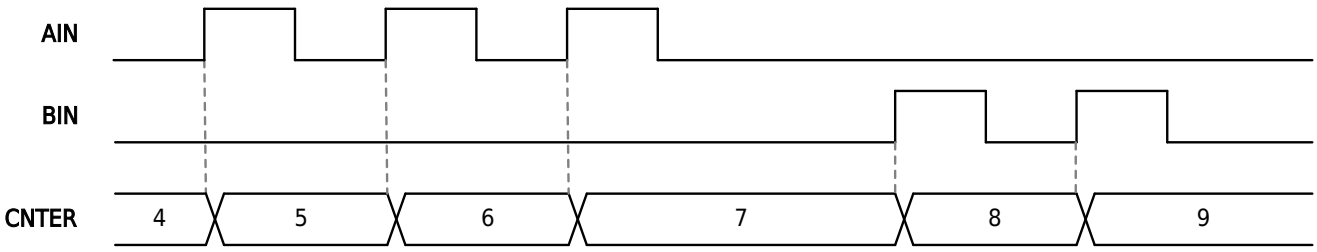
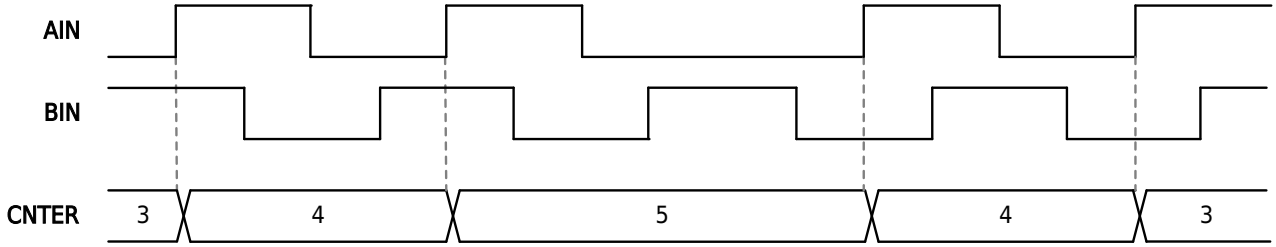


Figure 19-13 Position Mode-Basic Counting

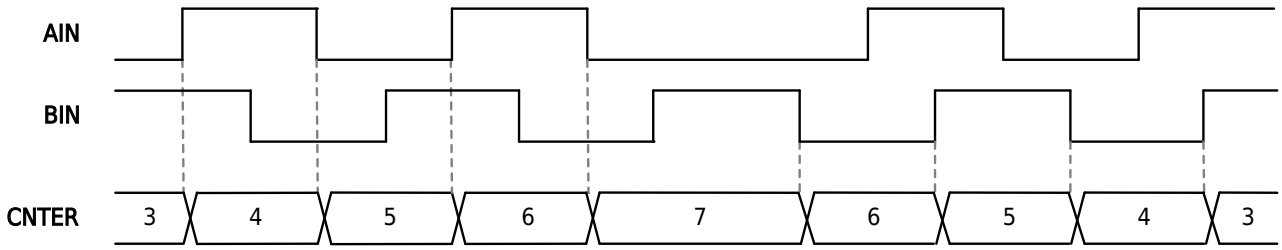
Phase Difference Counting

Phase difference counting operates based on the phase relationship between AIN and BIN. Depending on the configuration, the system can perform 1x counting, 2x counting, or 4x counting.



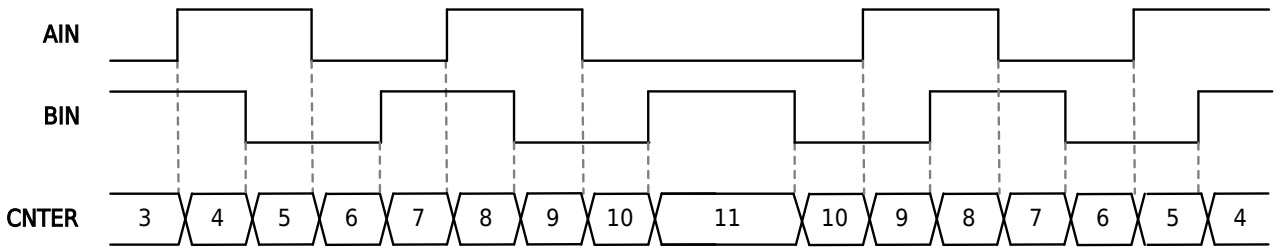
HCUPR.HCUP6=0b1 && HCDOR.HCDO4=0b1

Figure 19-14 Position Counting Mode-Phase Difference Counting (1x Counting)



HCUPR.HCUP6=HCUPR.HCUP5=0b1 && HCDOR.HCDO2=HCDOR.HCDO1=0b1

Figure 19-15 Position Counting Mode-Phase Difference Counting (2x Counting)



HCUPR.HCUP6=HCUPR.HCUP5=HCUPR.HCUP3=HCUPR.HCUP0=0b1
HCDOR.HCDO7=HCDOR.HCDO4=HCDOR.HCDO2=HCDOR.HCDO1=0b1

Figure 19-16 Position Counting Mode-Phase Difference Counting (4x Counting)

Direction Counting

Direction counting sets the AIN input as the direction control, and uses the BIN input as the counting clock.

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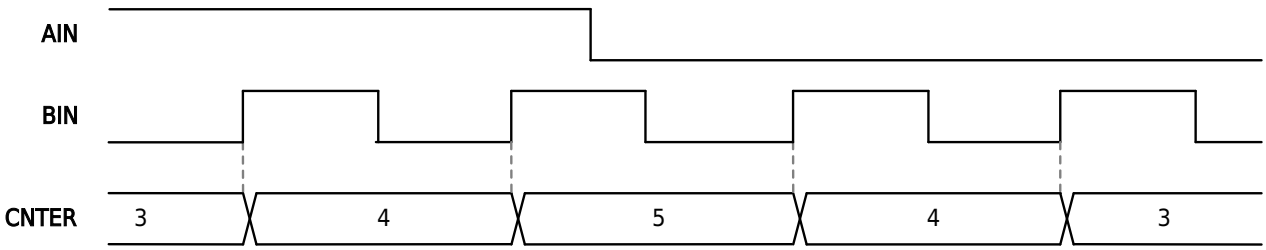

HCUPR.HCUP2=0b1 && HCDOR.HCDO0=0b1

Figure 19-17 Position Counting Mode-Direction Counting

19.3.11.2 Revolution Counting Mode

Quadrature encoding revolution mode refers to determining the revolution count by incorporating ZIN input events on the basis of AIN and BIN counting. In revolution counting mode, the Z phase count function, position overflow counting function, and mixed counting function can be implemented based on the counting method of the revolution timer.

Z-phase Counting

Z-phase counting refers to a counting operation in which the revolution counting unit performs counting based on the ZIN input, while the position counting unit is reset to zero.

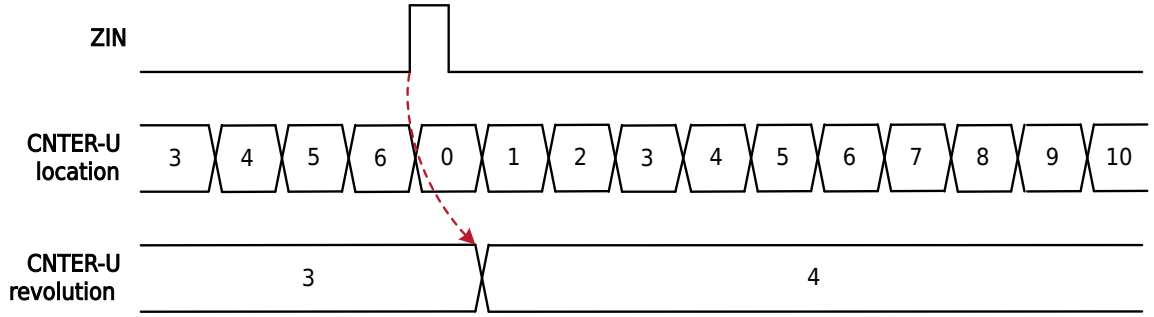

Figure 19-18 Revolution Counting Mode-Z-phase Counting

Position Overflow Counting

Position overflow counting refers to the situation where an overflow event is generated when the position counting unit's count overflows or underflows, thereby triggering the timer of the revolution counting unit to perform one count. (In this counting mode, the ZIN input does not trigger counting in the revolution counting unit or clear the position counting unit.)

The count up (count down) event Bits 12-11 of the HCUPR or HCDOR register of the revolution counting unit are enabled, and the overflow event of the position counting unit can trigger the revolution counting unit to count once.

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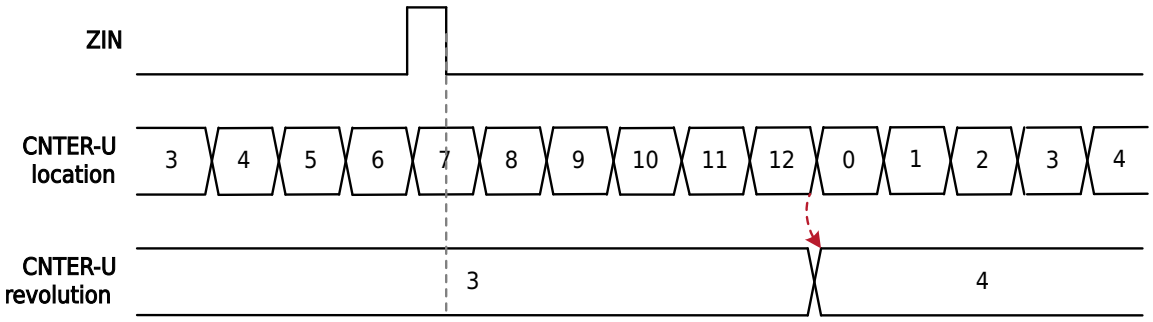

Figure 19-19 Revolution Counting Mode-Position Overflow Counting

Mixed Counting

Mixed counting refers to a combined counting method that integrates both Z-phase counting and position overflow counting. Its implementation method is also a combination of the above two counting methods.

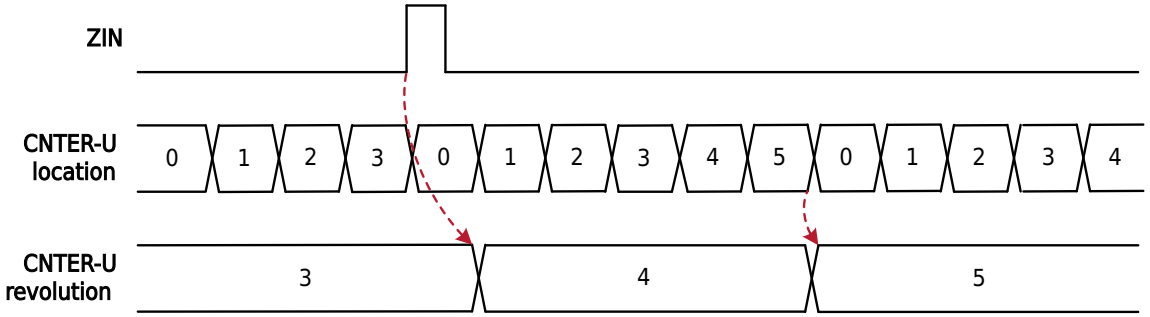

Figure 19-20 Revolution Counting Mode-Mixed Counting

19.3.12 Emergency Brake

Unit 5 features an emergency brake event interface that connects to the EMB event output from the EMB module. The gated abnormal condition events on this interface can be set from the EMB module. For detailed information, please refer to the relevant descriptions in the "Emergency Brake Module (EMB)" chapter.

During normal PWM output (when TMRA_PCONR6.OUTEN = 1) from the six PWM ports of Unit 5, if an EMB abnormal event from the EMB module is detected, the output state of each PWM port changes to a pre-configured state. That is, according to the settings of EPSCR.ESS1-6, the pre-set port state can be configured to output a high-impedance state, a low level, or a high level.

For example, if EPSCR.ESS1 is set to 0b01, and an EMB event occurs during normal output from the TIMA_5_PWM1 port of TimerA, the output of the TIMA_5_PWM1 port will change to a high-impedance state.

After the conditions triggering the EMB abnormal event become invalid, the user can clear the EMB abnormal event by writing to the EMB_STATCLR0 register.

19.3.13 Interrupt and Events

TimerA contains 3 interrupt outputs and 3 event outputs, which are 1 comparison match interrupt and event, 2 period match interrupts and events.

19.3.13.1 Comparison Match Interrupt and Event

When a comparison match occurs between the CMPARm register and the count value, the STFLR.CMPFm bit will be set to 1. At this time, if the ICONR.ITENm bit is set to 1, the corresponding interrupt request

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(TMRA_<t>_CMP) will be triggered; if the ECONR.ETENm bit is set to 1, the corresponding event request (TMRA_<t>_CMP) will be triggered (m=1-2/6).

When the capture input active condition selected by the CCONRm register occurs, the capture input action occurs. At this time, if the ICONR.ITENm bit is set to 1, the corresponding interrupt request (TMRA_<t>_CMP) will be triggered; if the ECONR.ETENm bit is set to 1, the corresponding event request (TMRA_<t>_CMP) will be triggered (m=1-2/6).

The comparison match interrupts and comparison match events of the 2/6 reference value within each unit are not output independently. The comparison match interrupts are summarized into an interrupt output to the interrupt module through "OR logic" (see the "Interrupt Controller (INTC) " chapter), and the comparison match events are summarized into an event output through "OR logic" to select trigger other modules.

19.3.13.2 Period Match Interrupt and Event

The sawtooth wave mode counts up to the overflow point, the sawtooth wave mode counts down to the underflow point, and the triangle wave mode counts to the valley point or peak point. The BCSTRH.OVFF or BCSTRH.UDFF bit will be set to 1. At this time, if the BCSTRH.ITENOVF or BCSTRH.ITENUDF bit is set to 1 to enable interrupts, the period match interrupt (TMRA_<t>_OVF and TMRA_<t>_UDF) can be triggered at the corresponding period point to be output to the interrupt module (INTC); the period match event has no corresponding enable bit control, and the period match event (TMRA_<t>_OVF and TMRA_<t>_UDF) output is triggered at the corresponding counting period point to select triggering other modules.

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19.4 Register Description

19.4.1 Register List

- TimerA_1 base address: 0x40015000
- TimerA_2 base address: 0x40015400
- TimerA_3 base address: 0x40015800
- TimerA_4 base address: 0x40015C00
- TimerA_5 base address: 0x40016000

Note

TimerA is the name of the timer, and TimerA_<t> (<t>: 1-5) is the timer unit.

Table 19-4 General Timer (TimerA) Register Offset

Offset	Register	Description	Width
0x0000	TMRA_CNTER	General Counter Value Register	16
0x0004	TMRA_PERAR	Period Reference Value Register	16
0x003C+0x4*m	TMRA_CMPARm	Compare Reference Value Register m (m=1-2/6)	16
0x0080	TMRA_BCSTRL	Basic Control and Status Register L	8
0x0081	TMRA_BCSTRH	Basic Control and Status Register H	8
0x0090	TMRA_ICONR	Interrupt Control Register	16
0x0094	TMRA_ECONR	Event Control Register	16
0x0098	TMRA_FCONR	Filter Control Register	16
0x009C	TMRA_STFLR	Status Flag Register	16
0x00B8+0x8*m	TMRA_BCONRm	Buffer Control Register m (m=1-3)	16
0x00FC+0x4*m	TMRA_CCONRm	Capture Control Register m (m=1-2/6)	16
0x013C+0x4*m	TMRA_PCONRm	Port Control Register m (m=1-2/6)	16
0x0084	TMRA_HCONR	Hardware Control Event Select Register	16
0x0088	TMRA_HCUPR	Hardware Count Up Event Select Register	16
0x008C	TMRA_HCDOR	Hardware Count Down Event Select Register	16
0x0180	TMRA_EPSCR	Emergency Port Status Control Register	16

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19.4.2 General Counter Value Register (TMRA_CNTER)

Offset	Bit Position															
0x0000	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	CNT															
Access	RW															

Bit	Name	Functional Description	Access
15:0	CNT	Count Value Current timer count value **Note** In the sawtooth up-counting mode, the initial value of CNT is set to 0. In the sawtooth down-counting mode, the initial value of CNT is set to the period value. In the triangular wave mode, the initial value of CNT is set to 1.	RW

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19.4.3 Period Reference Value Register (TMRA_PERAR)

Offset	Bit Position															
0x0004	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFFFF															
Name	PER															
Access	RW															

Bit	Name	Functional Description	Access
15:0	PER	Counting Period Value Set the counting period value for each counting period	RW

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19.4.4 Compare Reference Value Register (TMRA_CMPARm) (m=1-2/6)

Offset: 0x003C+0x4*m

Offset	Bit Position															
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFFFF															
Name	CMP															
Access	RW															

Bit	Name	Functional Description	Access
15:0	CMP	Count Compare Reference Value Set the compare reference value	RW

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19.4.5 Basic Control and Status Register L (TMRA_BCSTRL)

Offset	Bit Position							
0x0080	7	6	5	4	3	2	1	0
Reset	0x02							
Name	CKDIV				SYNST	MODE	DIR	START
Access	RW				RW	RW	RW	RW

Bit	Name	Functional Description	Access
7:4	CKDIV	Count Clock Selection ● 0b0000: PCLK ● 0b0001: PCLK/2 ● 0b0010: PCLK/4 ● 0b0011: PCLK/8 ● 0b0100: PCLK/16 ● 0b0101: PCLK/32 ● 0b0110: PCLK/64 ● 0b0111: PCLK/128 ● 0b1000: PCLK/256 ● 0b1001: PCLK/512 ● 0b1010: PCLK/1024 ● Others: Setting prohibited	RW
3	SYNST	Synchronous Start Enabled ● 0b0: Synchronous start between the even unit and the counting unit in the symmetric unit is disabled ● 0b1: Synchronous start between the even unit and the counting unit in the symmetric unit is enabled **Note** This setting has no effect for odd unit TimerA units in a symmetric unit or TimerA units without a symmetric unit; the bit will read as 0 in such cases.	RW
2	MODE	Counting Mode ● 0b0: Sawtooth wave mode ● 0b1: Triangle wave mode	RW
1	DIR	Count Direction ● 0b0: Counter count down ● 0b1: Counter count up **Note** In triangle wave mode, this bit indicates the counter direction status.	RW

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Bit	Name	Functional Description	Access
0	START	Timer Start ● 0b0: Timer disabled ● 0b1: Timer enabled **Note** ● This bit will automatically be cleared to 0 when the hardware stop condition is active. ● When the synchronous start function of the even unit in the symmetric unit is effective, the bit of the even unit will also be set after the software of the odd unit is started.	RW

Notice

1. For TimerA Units 1 to 5, the PCLK source is PCLK1.
2. In triangle wave mode, do not write to this register during timer operation.

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19.4.6 Basic Control and Status Register H (TMRA_BCSTRH)

Offset	Bit Position							
0x0081	7	6	5	4	3	2	1	0
Reset	0x00							
Name	UDFF	OVFF	ITENUDF	ITENOVF	Reserved			OVSTP
Access	RW	RW	RW	RW				RW

Bit	Name	Functional Description	Access
7	UDFF	Underflow Flag ● 0b0: No counter underflow occurred during down counting ● 0b1: Counter underflow occurred during down counting	RW
6	OVFF	Overflow Flag ● 0b0: No counter overflow occurred during up counting ● 0b1: Counter overflow occurred during up counting	RW
5	ITENUDF	Underflow Interrupt Enabled ● 0b0: Disable ● 0b1: Enable	RW
4	ITENOVF	Overflow Interrupt Enabled ● 0b0: Disable ● 0b1: Enable	RW
3:1	*Reserved*	-	-
0	OVSTP	Counting Overflow Stop Control ● 0b0: The counter continues counting after an overflow or underflow ● 0b1: The counter stops counting after an overflow or underflow **Note** The TMRA_CNTER register must be initialized before restarting the timer after an overflow stop.	RW

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19.4.7 Interrupt Control Register (TMRA_ICONR)

Offset	Bit Position															
0x0090	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved										ITEN6	ITEN5	ITEN4	ITEN3	ITEN2	ITEN1
Access											RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
15:6	*Reserved*	-	-
5	ITEN6	Count Match Interrupt Enable 6 Interrupt Condition: Triggered when the value of the CMPAR6 register matches the counter value (CNTER), or when an input capture occurs. ● 0b0: Disable interrupt output ● 0b1: Enable interrupt output **Note** Only valid for Unit 5.	RW
4	ITEN5	Count Match Interrupt Enable 5 Interrupt Condition: Triggered when the value of the CMPAR5 register matches the counter value (CNTER), or when an input capture occurs. ● 0b0: Disable interrupt output ● 0b1: Enable interrupt output **Note** Only valid for Unit 5.	RW
3	ITEN4	Count Match Interrupt Enable 4 Interrupt Condition: Triggered when the value of the CMPAR4 register matches the counter value (CNTER), or when an input capture occurs. ● 0b0: Disable interrupt output ● 0b1: Enable interrupt output **Note** Only valid for Unit 5.	RW

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Bit	Name	Functional Description	Access
2	ITEN3	Count Match Interrupt Enable 3 Interrupt Condition: Triggered when the value of the CMPAR3 register matches the counter value (CNTER), or when an input capture occurs. ● 0b0: Disable interrupt output ● 0b1: Enable interrupt output **Note** Only valid for Unit 5.	RW
1	ITEN2	Count Match Interrupt Enable 2 Interrupt Condition: Triggered when the value of the CMPAR2 register matches the counter value (CNTER), or when an input capture occurs. ● 0b0: Disable interrupt output ● 0b1: Enable interrupt output	RW
0	ITEN1	Count Match Interrupt Enable 1 Interrupt Condition: Triggered when the value of the CMPAR1 register matches the counter value (CNTER), or when an input capture occurs. ● 0b0: Disable interrupt output ● 0b1: Enable interrupt output	RW

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19.4.8 Event Control Register (TMRA_ECONR)

Offset	Bit Position															
0x0094	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved										ETEN6	ETEN5	ETEN4	ETEN3	ETEN2	ETEN1
Access											RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
15:6	*Reserved*	-	-
5	ETEN6	Count Match Events Enable 6 Events Condition: Triggered when the value of the CMPAR6 register matches the counter value (CNTER), or when an input capture occurs. ● 0b0: Disable event output ● 0b1: Enable event output **Note** Only valid for Unit 5.	RW
4	ETEN5	Count Match Events Enable 5 Events Condition: Triggered when the value of the CMPAR5 register matches the counter value (CNTER), or when an input capture occurs. ● 0b0: Disable event output ● 0b1: Enable event output **Note** Only valid for Unit 5.	RW
3	ETEN4	Count Match Events Enable 4 Events Condition: Triggered when the value of the CMPAR4 register matches the counter value (CNTER), or when an input capture occurs. ● 0b0: Disable event output ● 0b1: Enable event output **Note** Only valid for Unit 5.	RW

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Bit	Name	Functional Description	Access
2	ETEN3	Count Match Events Enable 3 Events Condition: Triggered when the value of the CMPAR3 register matches the counter value (CNTER), or when an input capture occurs. ● 0b0: Disable event output ● 0b1: Enable event output **Note** Only valid for Unit 5.	RW
1	ETEN2	Count Match Events Enable 2 Events Condition: Triggered when the value of the CMPAR2 register matches the counter value (CNTER), or when an input capture occurs. ● 0b0: Disable event output ● 0b1: Enable event output	RW
0	ETEN1	Count Match Events Enable 1 Events Condition: Triggered when the value of the CMPAR1 register matches the counter value (CNTER), or when an input capture occurs. ● 0b0: Disable event output ● 0b1: Enable event output	RW

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19.4.9 Filter Control Register (TMRA_FCONR)

Offset	Bit Position															
0x0098	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved	NOFICKCB		NOFIENCB	Reserved	NOFICKCA		NOFIENCA	Reserved					NOFICKTG		NOFIENTG
Access		RW		RW		RW		RW						RW		RW

Bit	Name	Functional Description	Access
15	*Reserved*	-	-
14:13	NOFICKCB	Filter Sampling Reference Clock Selection CB ● 0b00: PCLK ● 0b01: PCLK/4 ● 0b10: PCLK/16 ● 0b11: PCLK/64	RW
12	NOFIENCB	Capture Input Port Filter CB ● 0b0: Input filtering function for the TMRA_<t>_CLKB port is disabled ● 0b1: Input filtering function for the TMRA_<t>_CLKB port is enabled	RW
11	*Reserved*	-	-
10:9	NOFICKCA	Filter Sampling Reference Clock Selection CA ● 0b00: PCLK ● 0b01: PCLK/4 ● 0b10: PCLK/16 ● 0b11: PCLK/64	RW
8	NOFIENCA	Capture Input Port Filter CA ● 0b0: Input filtering function for the TMRA_<t>_CLKA port is disabled ● 0b1: Input filtering function for the TMRA_<t>_CLKA port is enabled	RW
7:3	*Reserved*	-	-
2:1	NOFICKTG	Filter Sampling Reference Clock Selection TG ● 0b00: PCLK ● 0b01: PCLK/4 ● 0b10: PCLK/16 ● 0b11: PCLK/64	RW

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Bit	Name	Functional Description	Access
0	NOFIENTG	Capture Input Port Filter TG ● 0b0: Input filtering function for the TMRA_<t>_TRIG port is disabled ● 0b1: Input filtering function for the TMRA_<t>_TRIG port is enabled	RW

Note

For TimerA Units 1 to 5, the PCLK source is PCLK1.

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19.4.10 Status Flag Register (TMRA_STFLR)

Offset	Bit Position															
0x009C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved		ICPF6	ICPF5	ICPF4	ICPF3	ICPF2	ICPF1	Reserved		CMPF6	CMPF5	CMPF4	CMPF3	CMPF2	CMPF1
Access			RW	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
15:14	*Reserved*	-	-
13	ICPF6	Repeat Capture Flag 6 Write 0 to clear the flag, write 1 has no effect Read: ● 0b0: No capture completion action has occurred after the CMPF6 flag was set to 1 ● 0b1: A capture completion action has occurred again after the CMPF6 flag was set to 1 **Note** Only valid for Unit 5.	RW
12	ICPF5	Repeat Capture Flag 5 Write 0 to clear the flag, write 1 has no effect Read: ● 0b0: No capture completion action has occurred after the CMPF5 flag was set to 1 ● 0b1: A capture completion action has occurred again after the CMPF5 flag was set to 1 **Note** Only valid for Unit 5.	RW
11	ICPF4	Repeat Capture Flag 4 Write 0 to clear the flag, write 1 has no effect Read: ● 0b0: No capture completion action has occurred after the CMPF4 flag was set to 1 ● 0b1: A capture completion action has occurred again after the CMPF4 flag was set to 1 **Note** Only valid for Unit 5.	RW

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Bit	Name	Functional Description	Access
10	ICPF3	Repeat Capture Flag 3 Write 0 to clear the flag, write 1 has no effect Read: ● 0b0: No capture completion action has occurred after the CMPF3 flag was set to 1 ● 0b1: A capture completion action has occurred again after the CMPF3 flag was set to 1 **Note** Only valid for Unit 5.	RW
9	ICPF2	Repeat Capture Flag 2 Write 0 to clear the flag, write 1 has no effect Read: ● 0b0: No capture completion action has occurred after the CMPF2 flag was set to 1 ● 0b1: A capture completion action has occurred again after the CMPF2 flag was set to 1	RW
8	ICPF1	Repeat Capture Flag 1 Write 0 to clear the flag, write 1 has no effect Read: ● 0b0: No capture completion action has occurred after the CMPF1 flag was set to 1 ● 0b1: A capture completion action has occurred again after the CMPF1 flag was set to 1	RW
7:6	*Reserved*	-	-
5	CMPF6	Count Match Flag 6 Write 0 to clear the flag, write 1 has no effect Read: ● 0b0: The value in the CMPAR6 register does not match the counter value, and no capture completion event has occurred ● 0b1: The value in the CMPAR6 register matches the counter value, or a capture completion event has occurred **Note** Only valid for Unit 5.	RW
4	CMPF5	Count Match Flag 5 Write 0 to clear the flag, write 1 has no effect Read: ● 0b0: The value in the CMPAR5 register does not match the counter value, and no capture completion event has occurred ● 0b1: The value in the CMPAR5 register matches the counter value, or a capture completion event has occurred **Note** Only valid for Unit 5.	RW

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Bit	Name	Functional Description	Access
3	CMPF4	Count Match Flag 4 Write 0 to clear the flag, write 1 has no effect Read: ● 0b0: The value in the CMPAR4 register does not match the counter value, and no capture completion event has occurred ● 0b1: The value in the CMPAR4 register matches the counter value, or a capture completion event has occurred **Note** Only valid for Unit 5.	RW
2	CMPF3	Count Match Flag 3 Write 0 to clear the flag, write 1 has no effect Read: ● 0b0: The value in the CMPAR3 register does not match the counter value, and no capture completion event has occurred ● 0b1: The value in the CMPAR3 register matches the counter value, or a capture completion event has occurred **Note** Only valid for Unit 5.	RW
1	CMPF2	Count Match Flag 2 Write 0 to clear the flag, write 1 has no effect Read: ● 0b0: The value in the CMPAR2 register does not match the counter value, and no capture completion event has occurred ● 0b1: The value in the CMPAR2 register matches the counter value, or a capture completion event has occurred	RW
0	CMPF1	Count Match Flag 1 Write 0 to clear the flag, write 1 has no effect Read: ● 0b0: The value in the CMPAR1 register does not match the counter value, and no capture completion event has occurred ● 0b1: The value in the CMPAR1 register matches the counter value, or a capture completion event has occurred	RW

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19.4.11 Buffer Control Register (TMRA_BCONRm) (m=1-3)

Offset: 0x00B8+0x8*m

Offset	Bit Position															
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved												BSEN	BSE1	BSE0	BEN
Access													RW	RW	RW	RW

Bit	Name	Functional Description	Access
15:4	*Reserved*	-	-
3	BSEN	Buffer Special Enabled ● 0b0: No buffer value transmission occurs when reading the CNTER register of the symmetric unit ● 0b1: Buffer value transmission occurs when reading the CNTER register of the symmetric unit, i.e., $CMPAR_{2m}$ -> $CMPAR_{2m-1}$ **Note** Only valid for Unit 1-4.	RW
2	BSE1	Triangle Wave Buffer Transmission Selection 1 ● 0b0: In triangle wave counting mode, the buffer value is not transmitted when the counter reaches the valley point ● 0b1: In triangle wave counting mode, the buffer value is transmitted when the counter reaches the valley point, that is: $CMPAR_{2m}$ -> $CMPAR_{2m-1}$ **Note** The configuration of this bit is enable only when BEN is 1.	RW
1	BSE0	Triangle Wave Buffer Transmission Selection 0 ● 0b0: In triangle wave counting mode, the buffer value is not transmitted when the counter reaches the peak point ● 0b1: In triangle wave counting mode, the buffer value is transmitted when the counter reaches the peak point, that is: $CMPAR_{2m}$ -> $CMPAR_{2m-1}$ **Note** The configuration of this bit is enable only when BEN is 1.	RW
0	BEN	Buffer Enabled ● 0b0: The buffer function for the $CMPAR_{2m-1}$ reference value is disabled ● 0b1: The buffer function for the $CMPAR_{2m-1}$ reference value is enabled	RW

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Note

- Please do not set both BEN and BSEN to 1 simultaneously.
- When BEN is 1 and BSE1 and BSE0 are both 0, in hardware counting mode or software counting sawtooth mode, when the count reaches the overflow point or underflow point or the hardware clear counter action occurs, the buffer value is transmitted.

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19.4.12 Capture Control Register (TMRA_CCONRm) (m=1-2/6)

Offset: 0x00FC+0x4*m

Offset	Bit Position															
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved	NOFICKCP		NOFIENCP	HICP6	HICP5	HICP4	HICP3	Reserved	HICP2	HICP1	HICP0	Reserved			CAPMD
Access		RW		RW	RW	RW	RW	RW		RW	RW	RW				RW

Bit	Name	Functional Description	Access
15	*Reserved*	-	-
14:13	NOFICKCP	Filter Sampling Reference Clock Selection CP ● 0b00: PCLK ● 0b01: PCLK/4 ● 0b10: PCLK/16 ● 0b11: PCLK/64	RW
12	NOFIENCP	Capture Input Port Filtering CP ● 0b0: TMRA_<t>_PWMm port input filter function is disabled ● 0b1: TMRA_<t>_PWMm port input filter function is enabled	RW
11	HICP6	Capture Input Condition Enable 6 ● 0b0: When the falling edge is sampled on the TMRA_<t>_XOR port, no capture input action occurs ● 0b1: When the falling edge is sampled on the TMRA_<t>_XOR port, a capture input action occurs **Note** This bit is only valid in the CCONR4 register of unit 5. That is, after this bit is enable and the corresponding event occurs, under the condition of CCONR4.CAPMD=1, the current counter value is captured and saved to CMPAR4, and STFLR.CMPF4 is set.	RW
10	HICP5	Capture Input Condition Enable 5 ● 0b0: When the rising edge is sampled on the TMRA_<t>_XOR port, no capture input action occurs ● 0b1: When the rising edge is sampled on the TMRA_<t>_XOR port, a capture input action occurs **Note** This bit is only valid in the CCONR4 register of unit 5. That is, after this bit is enable and the corresponding event occurs, under the condition of CCONR4.CAPMD=1, the current counter value is captured and saved to CMPAR4, and STFLR.CMPF4 is set.	RW

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Bit	Name	Functional Description	Access
9	HICP4	Capture Input Condition Enable 4 ● 0b0: When the falling edge is sampled on the TMRA_<t>_TRIG port input, no capture input action occurs ● 0b1: When the falling edge is sampled on the TMRA_<t>_TRIG port input, a capture input action occurs **Note** This bit is only valid in the CCONR3 register of unit 5. That is, after this bit is enable and the corresponding event occurs, under the condition of CCONR3.CAPMD=1, the current counter value is captured and saved to CMPAR3, and STFLR.CMPF3 is set.	RW
8	HICP3	Capture Input Condition Enable 3 ● 0b0: When the rising edge is sampled on the TMRA_<t>_TRIG port input, no capture input action occurs ● 0b1: When the rising edge is sampled on the TMRA_<t>_TRIG port input, a capture input action occurs **Note** This bit is only valid in the CCONR3 register of unit 5. That is, after this bit is enable and the corresponding event occurs, under the condition of CCONR3.CAPMD=1, the current counter value is captured and saved to CMPAR3, and STFLR.CMPF3 is set.	RW
7	*Reserved*	-	-
6	HICP2	Capture Input Condition Enable 2 ● 0b0: When the event specified in the TMRA_TRGSEL register occurs, no capture input action occurs ● 0b1: When the event specified in the TMRA_TRGSEL register occurs, a capture input action occurs **Note** For more information, please refer to "TimerA Hardware Trigger Event Selection Register (TMRA_TRGSELx) (x=0-1) " in "Automatic Operation System (AOS) ".	RW
5	HICP1	Capture Input Condition Enable 1 ● 0b0: When the falling edge is sampled on the TMRA_<t>_PWMm port input, no capture input action occurs ● 0b1: When the falling edge is sampled on the TMRA_<t>_PWMm port input, a capture input action occurs	RW
4	HICP0	Capture Input Condition Enable 0 ● 0b0: When the rising edge is sampled on the TMRA_<t>_PWMm port input, no capture input action occurs ● 0b1: When the rising edge is sampled on the TMRA_<t>_PWMm port input, a capture input action occurs	RW
3:1	*Reserved*	-	-
0	CAPMD	Function Mode Selection ● 0b0: Compare output function ● 0b1: Capture input function	RW

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Note

- For TimerA Units 1 to 5, the PCLK source is PCLK1.
- The TMRA_<t>_XOR signal is the signal obtained by performing an XOR operation on the quadrature inputs AIN and BIN of each unit.

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19.4.13 Port Control Register (TMRA_PCONRm) (m=1-2/6)

Offset: 0x013C+0x4*m

Offset	Bit Position															
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved			OUTEN	Reserved		FORC		PERC		CMPC		STPC		STAC	
Access				RW			RW		RW		RW		RW		RW	

Bit	Name	Functional Description	Access
15:13	*Reserved*	-	-
12	OUTEN	Output Enable ● 0b0: Output disabled for TMRA_<t>_PWMm port in PWM output function mode ● 0b1: Output enabled for TMRA_<t>_PWMm port in PWM output function mode	RW
11:10	*Reserved*	-	-
9:8	FORC	Forced Port Status Setting ● 0b0x: Not use forced port state setting ● 0b10: TMRA_<t>_PWMm port output will be set to low level at the beginning of next period ● 0b11: TMRA_<t>_PWMm port output will be set to high level at the beginning of next period **Note** The "next period" refers to the point when the counter reaches overflow or underflow point in hardware counting mode or sawtooth wave counting, or when the counter reaches trough point in triangular wave counting. This bit can be used to achieve control of PWM output duty cycle 0% or 100%.	RW

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Bit	Name	Functional Description	Access
7:6	PERC	Port Status Setting at Period Match ● 0b00: When the counter value equals the period value, the TMRA_<t>_PWMm output is set to low level. ● 0b01: When the counter value equals the period value, the TMRA_<t>_PWMm output is set to high level. ● 0b10: When the counter value equals the period value, the TMRA_<t>_PWMm output retains the previous state. ● 0b11: When the counter value equals the period value, the TMRA_<t>_PWMm output toggles. **Note** In sawtooth wave counting mode with up-counting, the period point is PERAR. In sawtooth wave counting mode with down-counting and triangle wave mode, the period point is zero.	RW
5:4	CMPC	Port Status Setting at Compare Match ● 0b00: When counter value equals CMPARn, the TMRA_<t>_PWMm output is set to low level. ● 0b01: When counter value equals CMPARn, the TMRA_<t>_PWMm output is set to high level. ● 0b10: When counter value equals CMPARn, the TMRA_<t>_PWMm output retains the previous state. ● 0b11: When counter value equals CMPARn, the TMRA_<t>_PWMm output toggles.	RW
3:2	STPC	Port Status Setting at Counting Stops ● 0b00: When counting stops, the TMRA_<t>_PWMm output is set to low level. ● 0b01: When counting stops, the TMRA_<t>_PWMm output is set to high level. ● 0b10: When counting stops, the TMRA_<t>_PWMm output retains the previous state. ● 0b11: When counting stops, the TMRA_<t>_PWMm output retains the previous state.	RW
1:0	STAC	Port Status Setting at Counting Starts ● 0b00: When counting starts, the TMRA_<t>_PWMm output is set to low level. ● 0b01: When counting starts, the TMRA_<t>_PWMm output is set to high level. ● 0b10: When counting starts, the TMRA_<t>_PWMm output retains the previous state. ● 0b11: When counting starts, the TMRA_<t>_PWMm output retains the previous state.	RW

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19.4.14 Hardware Control Event Select Register (TMRA_HCONR)

Offset	Bit Position															
0x0084	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	HCLE6	HCLE5	HCLE4	HCLE3	Reserved	HCLE2	HCLE1	HCLE0	Reserved	HSTP2	HSTP1	HSTP0	Reserved	HSTA2	HSTA1	HSTA0
Access	RW	RW	RW	RW		RW	RW	RW		RW	RW	RW		RW	RW	RW

Bit	Name	Functional Description	Access
15	HCLE6	Hardware Clear Condition 6 Condition: Falling edge is sampled on TMRA_5_PWM3 port ● 0b0: When the condition is met, hardware clear is disabled ● 0b1: When the condition is met, hardware clear is enabled	RW
14	HCLE5	Hardware Clear Condition 5 Condition: Rising edge is sampled on TMRA_5_PWM3 port ● 0b0: When the condition is met, hardware clear is disabled ● 0b1: When the condition is met, hardware clear is enabled	RW
13	HCLE4	Hardware Clear Condition 4 Condition: Falling edge is sampled on TRIG port of the symmetric unit ● 0b0: When the condition is met, hardware clear is disabled ● 0b1: When the condition is met, hardware clear is enabled	RW
12	HCLE3	Hardware Clear Condition 3 Condition: Rising edge is sampled on TRIG port of the symmetric unit ● 0b0: When the condition is met, hardware clear is disabled ● 0b1: When the condition is met, hardware clear is enabled	RW
11	*Reserved*	-	-
10	HCLE2	Hardware Clear Condition 2 Condition: The event specified in the TMRA_TRGSEL register occurs ● 0b0: When the condition is met, hardware clear is disabled ● 0b1: When the condition is met, hardware clear is enabled **Note** For more information, please refer to "TimerA Hardware Trigger Event Selection Register (TMRA_TRGSELx) (x=0-1) " in "Automatic Operation System (AOS) ".	RW
9	HCLE1	Hardware Clear Condition 1 Condition: Falling edge is sampled on TMRA_<t>_TRIG port ● 0b0: When the condition is met, hardware clear is disabled ● 0b1: When the condition is met, hardware clear is enabled	RW

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Bit	Name	Functional Description	Access
8	HCLE0	Hardware Clear Condition 0 Condition: Rising edge is sampled on TMRA_<t>_TRIG port ● 0b0: When the condition is met, hardware clear is disabled ● 0b1: When the condition is met, hardware clear is enabled	RW
7	*Reserved*	-	-
6	HSTP2	Hardware Stop Condition 2 Condition: The event specified in the TMRA_TRGSEL register occurs ● 0b0: When the condition is met, hardware stop is disabled ● 0b1: When the condition is met, hardware stop is enabled **Note** For more information, please refer to "TimerA Hardware Trigger Event Selection Register (TMRA_TRGSELx) (x=0-1) " in "Automatic Operation System (AOS) ".	RW
5	HSTP1	Hardware Stop Condition 1 Condition: Falling edge is sampled on TMRA_<t>_TRIG port ● 0b0: When the condition is met, hardware stop is disabled ● 0b1: When the condition is met, hardware stop is enabled	RW
4	HSTP0	Hardware Stop Condition 0 Condition: Rising edge is sampled on TMRA_<t>_TRIG port ● 0b0: When the condition is met, hardware stop is disabled ● 0b1: When the condition is met, hardware stop is enabled	RW
3	*Reserved*	-	-
2	HSTA2	Hardware Start Condition 2 Condition: The event specified in the TMRA_TRGSEL register occurs ● 0b0: When the condition is met, hardware start is disabled ● 0b1: When the condition is met, hardware start is enabled **Note** For more information, please refer to "TimerA Hardware Trigger Event Selection Register (TMRA_TRGSELx) (x=0-1) " in "Automatic Operation System (AOS) ".	RW
1	HSTA1	Hardware Start Condition 1 Conditions: 1. Falling edge is sampled on TMRA_<t>_TRIG port when the synchronization start function is disabled 2. Falling edge is sampled on TMRA_<t>_TRIG port of the symmetric unit when the synchronization start function is enabled (only even unit in the symmetric unit support) ● 0b0: When the condition is met, hardware start is disabled ● 0b1: When the condition is met, hardware start is enabled	RW

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Bit	Name	Functional Description	Access
0	HSTA0	Hardware Start Condition 0 Conditions: 1. Rising edge is sampled on TMRA_<t>_TRIG port when the synchronization start function is disabled 2. Rising edge is sampled on TMRA_<t>_TRIG port of the symmetric unit when the synchronization start function is enabled (only even unit in the symmetric unit support) ● 0b0: When the condition is met, hardware start is disabled ● 0b1: When the condition is met, hardware start is enabled	RW

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19.4.15 Hardware Count Up Event Select Register (TMRA_HCUPR)

Offset	Bit Position															
0x0088	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved			HCUP12	HCUP11	HCUP10	HCUP9	HCUP8	HCUP7	HCUP6	HCUP5	HCUP4	HCUP3	HCUP2	HCUP1	HCUP0
Access				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
15:13	*Reserved*	-	-
12	HCUP12	Hardware Count Up Condition 12 Condition: Count underflow occurs in the symmetric unit ● 0b0: When this condition is met, hardware count up is disabled. ● 0b1: When this condition is met, hardware count up is enabled.	RW
11	HCUP11	Hardware Count Up Condition 11 Condition: Count overflow occurs in the symmetric unit ● 0b0: When this condition is met, hardware count up is disabled. ● 0b1: When this condition is met, hardware count up is enabled.	RW
10	HCUP10	Hardware Count Up Condition 10 Condition: The event specified in the TMRA_TRGSEL register occurs ● 0b0: When this condition is met, hardware count up is disabled. ● 0b1: When this condition is met, hardware count up is enabled. **Note** For more information, please refer to "TimerA Hardware Trigger Event Selection Register (TMRA_TRGSELx) (x=0-1) " in "Automatic Operation System (AOS) ".	RW
9	HCUP9	Hardware Count Up Condition 9 Condition: Falling edge is sampled on the TMRA_<t>_TRIG port ● 0b0: When this condition is met, hardware count up is disabled. ● 0b1: When this condition is met, hardware count up is enabled.	RW
8	HCUP8	Hardware Count Up Condition 8 Condition: Rising edge is sampled on the TMRA_<t>_TRIG port ● 0b0: When this condition is met, hardware count up is disabled. ● 0b1: When this condition is met, hardware count up is enabled.	RW
7	HCUP7	Hardware Count Up Condition 7 Condition: When the TMRA_<t>_CLKB port is high level, the falling edge is sampled on the TMRA_<t>_CLKA port ● 0b0: When this condition is met, hardware count up is disabled. ● 0b1: When this condition is met, hardware count up is enabled.	RW

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Bit	Name	Functional Description	Access
6	HCUP6	Hardware Count Up Condition 6 Condition: When the TMRA_<t>_CLKB port is high level, the rising edge is sampled on the TMRA_<t>_CLKA port ● 0b0: When this condition is met, hardware count up is disabled. ● 0b1: When this condition is met, hardware count up is enabled.	RW
5	HCUP5	Hardware Count Up Condition 5 Condition: When the TMRA_<t>_CLKB port is low level, the falling edge is sampled on the TMRA_<t>_CLKA port ● 0b0: When this condition is met, hardware count up is disabled. ● 0b1: When this condition is met, hardware count up is enabled.	RW
4	HCUP4	Hardware Count Up Condition 4 Condition: When the TMRA_<t>_CLKB port is low level, the rising edge is sampled on the TMRA_<t>_CLKA port ● 0b0: When this condition is met, hardware count up is disabled. ● 0b1: When this condition is met, hardware count up is enabled.	RW
3	HCUP3	Hardware Count Up Condition 3 Condition: When the TMRA_<t>_CLKA port is high level, the falling edge is sampled on the TMRA_<t>_CLKB port ● 0b0: When this condition is met, hardware count up is disabled. ● 0b1: When this condition is met, hardware count up is enabled.	RW
2	HCUP2	Hardware Count Up Condition 2 Condition: When the TMRA_<t>_CLKA port is high level, the rising edge is sampled on the TMRA_<t>_CLKB port ● 0b0: When this condition is met, hardware count up is disabled. ● 0b1: When this condition is met, hardware count up is enabled.	RW
1	HCUP1	Hardware Count Up Condition 1 Condition: When the TMRA_<t>_CLKA port is low level, the falling edge is sampled on the TMRA_<t>_CLKB port ● 0b0: When this condition is met, hardware count up is disabled. ● 0b1: When this condition is met, hardware count up is enabled.	RW
0	HCUP0	Hardware Count Up Condition 0 Condition: When the TMRA_<t>_CLKA port is low level, the rising edge is sampled on the TMRA_<t>_CLKB port ● 0b0: When this condition is met, hardware count up is disabled. ● 0b1: When this condition is met, hardware count up is enabled.	RW

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19.4.16 Hardware Count Down Event Select Register (TMRA_HCDOR)

Offset	Bit Position															
0x008C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved			HCDO12	HCDO11	HCDO10	HCDO9	HCDO8	HCDO7	HCDO6	HCDO5	HCDO4	HCDO3	HCDO2	HCDO1	HCDO0
Access				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
15:13	*Reserved*	-	-
12	HCDO12	Hardware Count Down Condition 12 Condition: Count underflow occurs in the symmetric unit ● 0b0: Hardware count down is disabled when the condition is met. ● 0b1: Hardware count down is enabled when the condition is met.	RW
11	HCDO11	Hardware Count Down Condition 11 Condition: Count overflow occurs in the symmetric unit ● 0b0: Hardware count down is disabled when the condition is met. ● 0b1: Hardware count down is enabled when the condition is met.	RW
10	HCDO10	Hardware Count Down Condition 10 Condition: The event specified in the TMRA_TRGSEL register occurs ● 0b0: Hardware count down is disabled when the condition is met. ● 0b1: Hardware count down is enabled when the condition is met. **Note** For more information, please refer to "TimerA Hardware Trigger Event Selection Register (TMRA_TRGSELx) (x=0-1) " in "Automatic Operation System (AOS) ".	RW
9	HCDO9	Hardware Count Down Condition 9 Condition: Falling edge is sampled on the TMRA_<t>_TRIG port ● 0b0: Hardware count down is disabled when the condition is met. ● 0b1: Hardware count down is enabled when the condition is met.	RW
8	HCDO8	Hardware Count Down Condition 8 Condition: Rising edge is sampled on the TMRA_<t>_TRIG port ● 0b0: Hardware count down is disabled when the condition is met. ● 0b1: Hardware count down is enabled when the condition is met.	RW
7	HCDO7	Hardware Count Down Condition 7 Condition: When the TMRA_<t>_CLKB port is high level, the falling edge is sampled on the TMRA_<t>_CLKA port	RW

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Bit	Name	Functional Description	Access
7	HCDO7	● 0b0: Hardware count down is disabled when the condition is met. ● 0b1: Hardware count down is enabled when the condition is met.	RW
6	HCDO6	Hardware Count Down Condition 6 Condition: When the TMRA_<t>_CLKB port is high level, the rising edge is sampled on the TMRA_<t>_CLKA port ● 0b0: Hardware count down is disabled when the condition is met. ● 0b1: Hardware count down is enabled when the condition is met.	RW
5	HCDO5	Hardware Count Down Condition 5 Condition: When the TMRA_<t>_CLKB port is low level, the falling edge is sampled on the TMRA_<t>_CLKA port ● 0b0: Hardware count down is disabled when the condition is met. ● 0b1: Hardware count down is enabled when the condition is met.	RW
4	HCDO4	Hardware Count Down Condition 4 Condition: When the TMRA_<t>_CLKB port is low level, the rising edge is sampled on the TMRA_<t>_CLKA port ● 0b0: Hardware count down is disabled when the condition is met. ● 0b1: Hardware count down is enabled when the condition is met.	RW
3	HCDO3	Hardware Count Down Condition 3 Condition: When the TMRA_<t>_CLKA port is high level, the falling edge is sampled on the TMRA_<t>_CLKB port ● 0b0: Hardware count down is disabled when the condition is met. ● 0b1: Hardware count down is enabled when the condition is met.	RW
2	HCDO2	Hardware Count Down Condition 2 Condition: When the TMRA_<t>_CLKA port is high level, the rising edge is sampled on the TMRA_<t>_CLKB port ● 0b0: Hardware count down is disabled when the condition is met. ● 0b1: Hardware count down is enabled when the condition is met.	RW
1	HCDO1	Hardware Count Down Condition 1 Condition: When the TMRA_<t>_CLKA port is low level, the falling edge is sampled on the TMRA_<t>_CLKB port ● 0b0: Hardware count down is disabled when the condition is met. ● 0b1: Hardware count down is enabled when the condition is met.	RW
0	HCDO0	Hardware Count Down Condition 0 Condition: When the TMRA_<t>_CLKA port is low level, the rising edge is sampled on the TMRA_<t>_CLKB port ● 0b0: Hardware count down is disabled when the condition is met. ● 0b1: Hardware count down is enabled when the condition is met.	RW

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19.4.17 Emergency Port Status Control Register (TMRA_EPSCR)

Offset	Bit Position															
0x0180	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved				ESS6		ESS5		ESS4		ESS3		ESS2		ESS1	
Access					RW		RW		RW		RW		RW		RW	

Bit	Name	Functional Description	Access
15:12	*Reserved*	-	-
11:10	ESS6	TMRA_5_PWM6 Emergency Stop Status ● 0b00: When an EMB emergency brake event occurs, the TMRA_5_PWM6 port maintains normal output. ● 0b01: When an EMB emergency brake event occurs, the TMRA_5_PWM6 port output is set to Hi-z. ● 0b10: When an EMB emergency brake event occurs, the TMRA_5_PWM6 port output is set to a low level. ● 0b11: When an EMB emergency brake event occurs, the TMRA_5_PWM6 port output is set to a high level.	RW
9:8	ESS5	TMRA_5_PWM5 Emergency Stop Status ● 0b00: When an EMB emergency brake event occurs, the TMRA_5_PWM5 port maintains normal output. ● 0b01: When an EMB emergency brake event occurs, the TMRA_5_PWM5 port output is set to Hi-z. ● 0b10: When an EMB emergency brake event occurs, the TMRA_5_PWM5 port output is set to a low level. ● 0b11: When an EMB emergency brake event occurs, the TMRA_5_PWM5 port output is set to a high level.	RW
7:6	ESS4	TMRA_5_PWM4 Emergency Stop Status ● 0b00: When an EMB emergency brake event occurs, the TMRA_5_PWM4 port maintains normal output. ● 0b01: When an EMB emergency brake event occurs, the TMRA_5_PWM4 port output is set to Hi-z. ● 0b10: When an EMB emergency brake event occurs, the TMRA_5_PWM4 port output is set to a low level. ● 0b11: When an EMB emergency brake event occurs, the TMRA_5_PWM4 port output is set to a high level.	RW

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Bit	Name	Functional Description	Access
5:4	ESS3	TMRA_5_PWM3 Emergency Stop Status ● 0b00: When an EMB emergency brake event occurs, the TMRA_5_PWM3 port maintains normal output. ● 0b01: When an EMB emergency brake event occurs, the TMRA_5_PWM3 port output is set to Hi-z. ● 0b10: When an EMB emergency brake event occurs, the TMRA_5_PWM3 port output is set to a low level. ● 0b11: When an EMB emergency brake event occurs, the TMRA_5_PWM3 port output is set to a high level.	RW
3:2	ESS2	TMRA_5_PWM2 Emergency Stop Status ● 0b00: When an EMB emergency brake event occurs, the TMRA_5_PWM2 port maintains normal output. ● 0b01: When an EMB emergency brake event occurs, the TMRA_5_PWM2 port output is set to Hi-z. ● 0b10: When an EMB emergency brake event occurs, the TMRA_5_PWM2 port output is set to a low level. ● 0b11: When an EMB emergency brake event occurs, the TMRA_5_PWM2 port output is set to a high level.	RW
1:0	ESS1	TMRA_5_PWM1 Emergency Stop Status ● 0b00: When an EMB emergency brake event occurs, the TMRA_5_PWM1 port maintains normal output. ● 0b01: When an EMB emergency brake event occurs, the TMRA_5_PWM1 port output is set to Hi-z. ● 0b10: When an EMB emergency brake event occurs, the TMRA_5_PWM1 port output is set to a low level. ● 0b11: When an EMB emergency brake event occurs, the TMRA_5_PWM1 port output is set to a high level.	RW

Notice

The priority of this register in controlling the state of PWM ports is higher than that of the TMRA_PCONRm register.

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20 General Timer (Timer0)

20.1 Introduction

General Timer 0 (Timer0) is a basic timer that can realize synchronous counting and asynchronous counting. The timer contains two channels (CH-A and CH-B) that can generate compare match events and count overflow events during counting. This event can trigger an interrupt and can be used to trigger other module actions. This series of products is equipped with 2 units of Timer0.

20.2 Functional Description

20.2.1 Timer0 Block Diagram

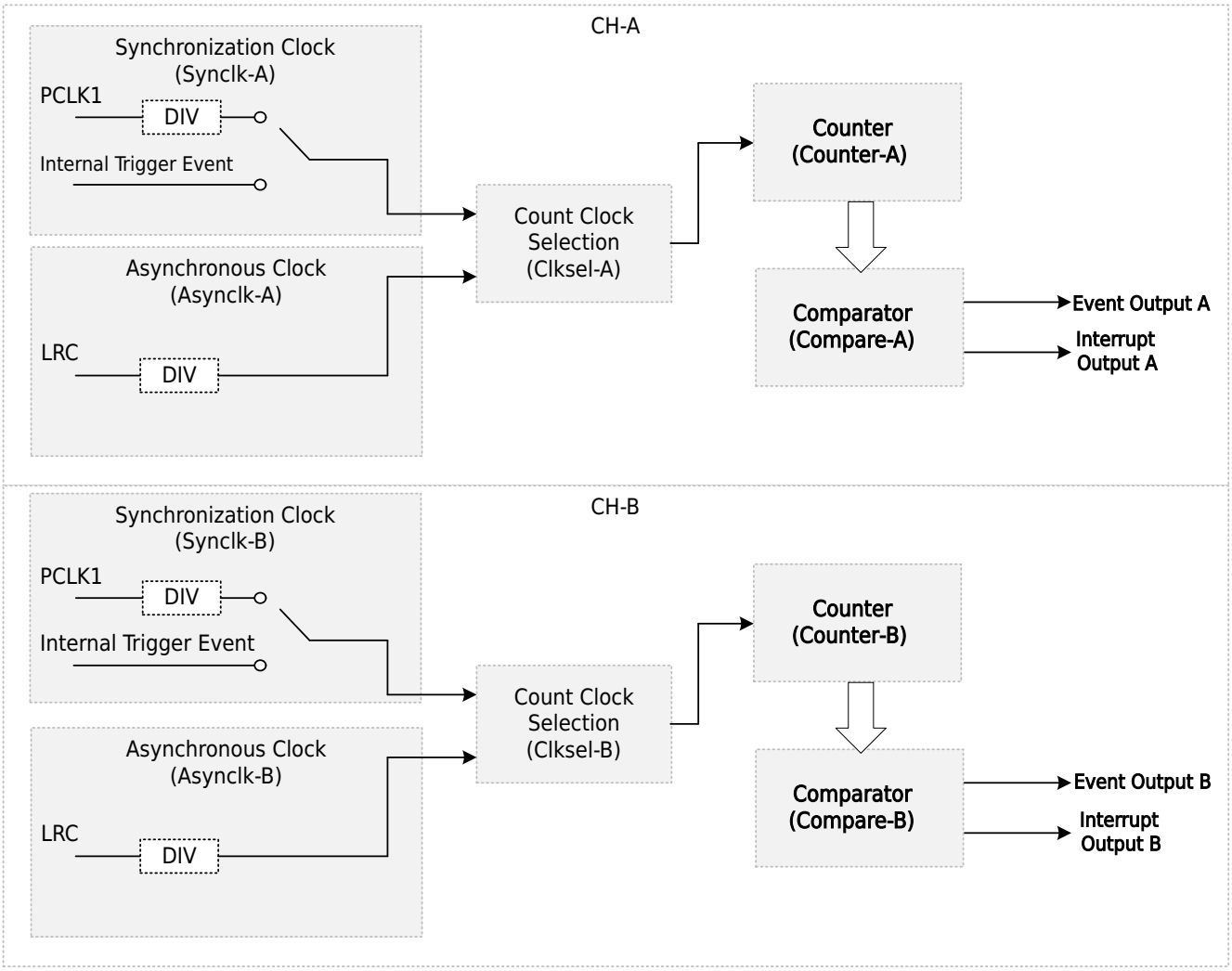

Figure 20-1 Timer0 Basic Block Diagram

20.2.2 Clock Source Selection

Timer0 can be counted either synchronously or asynchronously.

The synchronous counting mode refers to the synchronous timing relationship between the timer count clock and the bus access clock (register read/write operation clock). Asynchronous counting means that the timer count clock and bus access clock (register read/write operation clock) are non-synchronous timing relationships. The status of a timer, etc., may be changing when the register is read by asynchro-

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nous counting. Therefore, in the asynchronous counting mode, the register read operation must be implemented in the count stopped state.

Synchronous Count Clock Source

In synchronous counting mode (BCONR.SYNSA<B>=0), the clock source can have the following options (BCONR.SYNCLKA<B> setting) :

1. PCLK1 and PCLK1 divided by 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024 are used as synchronous count clocks (BCONR.SYNCLKA<B>=0 & BCONR.CKDIVA<B> settings);
2. An internal hardware trigger event input can serve as the synchronous count clock (BCONR.SYNCLKA<B>=1);

Asynchronous Count Clock Source

In asynchronous counting mode (BCONR.SYNSA<B>=1), the clock source is LRC. LRC and LRC divided by 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024 are used as asynchronous count clocks (BCONR.CKDIVA<B> settings).

20.2.3 Basic Counting

Each channel of Timer0 can set the reference count value, and generate a count compare match event when the count value is equal to the reference value.

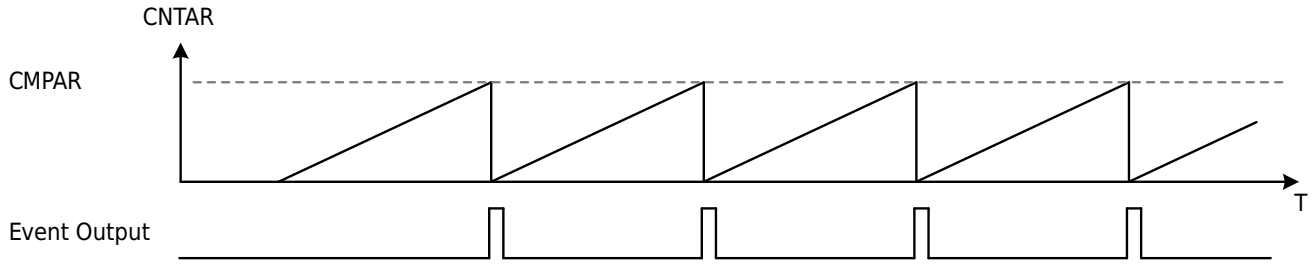

Figure 20-2 Timer0 Counting Timing Diagram

20.2.4 Hardware Triggering

Timer0 has two channels that share a common internal hardware trigger source. The timer's status (start, stop, reset) and capture input actions can be controlled through the relevant settings in the Basic Control Register (BCONR).

The source of this hardware trigger is selected by writing the corresponding trigger number into the Hardware Trigger Selection Register (TMR0_TRGSEL). For details on the register contents, refer to the "Automatic Operation System (AOS) " section, and for the specific event mappings, refer to the "Interrupt Controller (INTC) " section. When using the internal hardware trigger function, the AOS function control bit in Function Clock Control Register (CMU_FCG) must be enabled first.

20.2.5 Software Synchronization Start

The product is configured with a Count Synchronization Enable Register (TMR_SYNENR) to synchronize the start of the timers integrated in the product, as shown in the following table (where _* represents any unit of each TMR type, and TMR* represents each type of TMR). Setting multiple start bits in the TMR_SYNENR register enables multiple timers to start counting simultaneously. For the specific allocation of start bits, please refer to the "Count Synchronization Enable Register (TMR_SYNENR)".

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Notice

- When using the synchronous start function, ensure that the PCLK clock frequencies of the timers to be synchronized are identical and that the clocks (CMU_FCG) for the timers to be synchronized are enabled simultaneously.
- When using the synchronous start function, ensure that all timers to be synchronized are using the synchronous counting method.

Table 20-1 Counter and PWM Synchronous Start Status

Synchronous Start	TMR Unit	Counter Synchronization	PWM Synchronization
Same TMR Type	TMR0_1-2	✓	×
	TMRA_*	✓	✓
Different TMR Types	TMR0_*+TMR*	✓	×
	TMR4+TMRA_*	✓	×

20.2.6 Interrupt and Event

20.2.6.1 Interrupt

One Timer0 contains 4 interrupt outputs, namely, the count compare match interrupt or capture input interrupt of channel A and channel B, and the count overflow interrupt of channel A and channel B.

There are 2 reference value registers (CMPAR, CMPBR), which can be compared with the count value registers (CNTAR, CNTBR) respectively to generate comparison matching active signals. When the count compare matches, the STFLR.CMFA<B> bit in the Status Flag Register (STFLR) will be set to 1. At this time, if the BCONR.CMENA<B> bit of the Basic Control Register (BCONR) is set to enable interrupt, the corresponding interrupt request (TMR0_<t>_CMPn, <t>=1-2; n=A, B) will also be triggered.

When the internal hardware trigger input is used as the capture input condition, the corresponding capture input action can be generated. At this time, if the BCONR.CMENA<B> bit of the Basic Control Register (BCONR) is set to enable interrupt, the corresponding interrupt request (TMR0_<t>_CMPn, <t>=1-2; n=A, B) is triggered

When the count value register (CNTAR, CNTBR) counts to 0xFFFF, a count overflow event occurs. At this time, the STFLR.OVFA<B> bit in the Status Flag Register (STFLR) will be set to 1. If the BCONR.OVENA<B> bit of the Basic Control Register (BCONR) is set to enable interrupt, the corresponding interrupt request (TMR0_<t>_OVFn, <t>=1-2; n=A, B) will also be triggered.

When the asynchronous counting mode is selected, the compare match interrupt generated by the reference value register (CMPAR) of unit 1 can be used to wake up the system in Stop mode. Please refer to the relevant description in the "Interrupt Controller (INTC) " section.

20.2.6.2 Event

One Timer0 has four event outputs, namely, the count compare match events or capture input events of channel A and channel B, and the count overflow events of channel A and channel B.

When a count compare match, capture input action or count overflow occurs during the counting process, a corresponding event request (TMR0_<t>_CMPn or TMR0_<t>_OVFn, <t>=1-2, n=A, B) output signal will be generated, which can be used to select and trigger other modules.

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20.3 Register Description

20.3.1 Register List

- Timer0_1 base address: 0x40024000
- Timer0_2 base address: 0x40024400

Note

Timer0 is the name of the timer, and Timer0_<t> (<t>: 1-2) is the timer unit.

Table 20-2 General Timer (Timer0) Register Offset

Offset	Register	Description	Width
0x0000	TMR0_CNTAR	Counter Value Register A	32
0x0004	TMR0_CNTBR	Counter Value Register B	32
0x0008	TMR0_CMPAR	Compare Value Register A	32
0x000C	TMR0_CMPBR	Compare Value Register B	32
0x0010	TMR0_BCONR	Basic Control Register	32
0x0014	TMR0_STFLR	Status Flag Register	32

TMR_SYNENR base address: 0x40054C00

Table 20-3 TMR_SYNENR Register Offset

Offset	Register	Description	Width
0x14	TMR_SYNENR	Count Synchronization Enable Register	32

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20.3.2 Counter Value Register m (TMR0_CNTmR) (m=A/B)

Offset: 0x0000 (CNTAR), 0x0004 (CNTBR)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																						CNT									
Access																							RW									

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	CNT	Counter Value Current timer counter value **Note** Writing to this register is not disabled while counting is in progress.	RW

20.3.3 Compare Value Register m (TMR0_CMPmR) (m=A/B)

Offset: 0x0008 (CMPAR), 0x000C (CMPBR)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000FFFF																															
Name	Reserved																						CMP									
Access																							RW									

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	CMP	Reference Value Set the counting reference value to generate a compare match event	RW

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20.3.4 Basic Control Register (TMR0_BCONR)

Offset	Bit Position																													
0x0010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	HICPB	HCLEB	HSTPB	HSTAB	Reserved		SYNCLKB	SYNSB	CKDIVB				OVENB	CMENB	CAPMDB	CSTB	HICPA	HCLEA	HSTPA	HSTAA	Reserved		SYNCLKA	SYNSA	CKDIVA				OVENA	CMENA	CAPMDA	CSTA
Access	RW	RW	RW	RW			RW	RW	RW				RW	RW	RW	RW	RW	RW	RW	RW			RW	RW	RW				RW	RW	RW	RW

Bit	Name	Functional Description	Access
31	HICPB	Hardware Trigger Capture Input B Condition: Internal Hardware Trigger Event Active ● 0b0: Capture input is disabled when the condition matches ● 0b0: Capture input is enabled when the condition matches	RW
30	HCLEB	Hardware Trigger Clear B Condition: Internal Hardware Trigger Event Active ● 0b0: Timer clear operation is disabled when the condition matches ● 0b1: Timer clear operation is enabled when the condition matches	RW
29	HSTPB	Hardware Trigger Stop B Condition: Internal Hardware Trigger Event Active ● 0b0: Timer stop is disabled when the condition matches ● 0b1: Timer stop is enabled when the condition matches	RW
28	HSTAB	Hardware Trigger Start B Condition: Internal Hardware Trigger Event Active ● 0b0: Timer Start is disabled when the condition matches ● 0b1: Timer Start is enabled when the condition matches	RW
27:26	*Reserved*	-	-
25	SYNCLKB	Channel B Synchronous Counting Clock Source Selection ● 0b0: PCLK1 ● 0b1: Internal hardware triggering event	RW
24	SYNSB	Channel B Counting Mode Selection ● 0b0: Synchronous counting mode ● 0b1: Asynchronous counting mode	RW
23:20	CKDIVB	Channel B Count Clock Frequency Division Selection ● 0b0000: Clock source ● 0b0001: Clock source/2 ● 0b0010: Clock source/4 ● 0b0011: Clock source/8 ● 0b0100: Clock source/16 ● 0b0101: Clock source/32 ● 0b0110: Clock source/64	RW

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Bit	Name	Functional Description	Access
23:20	CKDIVB	● 0b0111: Clock source/128 ● 0b1000: Clock source/256 ● 0b1001: Clock source/512 ● 0b1010: Clock source/1024 ● Others: Setting prohibited **Note** The divided clock source can be various clock sources for asynchronous counting or PCLK1 for synchronous counting.	RW
19	OVENB	Count Overflow Interrupt Enable B Interrupt condition: count overflow, that is, count value (CNTBR)=0xFFFF ● 0b0: Disable interrupt ● 0b1: Enable interrupt	RW
18	CMENB	Count Match Interrupt Enable B Interrupt condition: When the CMPBR register is equal to the count value (CNTBR), or when a capture input event occurs ● 0b0: Disable interrupt ● 0b1: Enable interrupt	RW
17	CAPMDB	Function Mode Selection B ● 0b0: Compare output function ● 0b1: Capture input function	RW
16	CSTB	Channel B Timer ON ● 0b0: Channel B timer off ● 0b1: Channel B timer on **Note** This bit will automatically be set to 0 when the hardware trigger stop condition is enable.	RW
15	HICPA	Hardware Trigger Capture Input A Condition: Internal Hardware Trigger Event Active ● 0b0: Capture input is disabled when the condition matches ● 0b1: Capture input is enabled when the condition matches	RW
14	HCLEA	Hardware Trigger Clear A Condition: Internal Hardware Trigger Event Active ● 0b0: Timer clear operation is disabled when the condition matches ● 0b1: Timer clear operation is enabled when the condition matches	RW
13	HSTPA	Hardware Trigger Stop A Condition: Internal Hardware Trigger Event Active ● 0b0: Timer stop is disabled when the condition matches ● 0b1: Timer stop is enabled when the condition matches	RW

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Bit	Name	Functional Description	Access
12	HSTAA	Hardware Trigger Start A Condition: Internal Hardware Trigger Event Active ● 0b0: Timer start is disabled when the condition matches ● 0b1: Timer start is enabled when the condition matches	RW
11:10	*Reserved*	-	-
9	SYNCLKA	Channel A Synchronous Counting Clock Source Selection ● 0b0: PCLK1 ● 0b1: Internal hardware triggering event	RW
8	SYNSA	Channel A Counting Mode Selection ● 0b0: Synchronous counting mode ● 0b1: Asynchronous counting mode	RW
7:4	CKDIVA	Channel A Count Clock Frequency Division Selection ● 0b0000: Clock source ● 0b0001: Clock source/2 ● 0b0010: Clock source/4 ● 0b0011: Clock source/8 ● 0b0100: Clock source/16 ● 0b0101: Clock source/32 ● 0b0110: Clock source/64 ● 0b0111: Clock source/128 ● 0b1000: Clock source/256 ● 0b1001: Clock source/512 ● 0b1010: Clock source/1024 ● Others: Setting prohibited **Note** The divided clock source can be various clock sources for asynchronous counting or PCLK1 for synchronous counting.	RW
3	OVENA	Count Overflow Interrupt Enable A Interrupt condition: count overflow, that is, count value (CNTAR)=0xFFFF ● 0b0: Disable interrupt ● 0b1: Enable interrupt	RW
2	CMENA	Count Match Interrupt Enable A Interrupt condition: When the CMPAR register is equal to the count value (CNTAR), or when a capture input event occurs ● 0b0: Disable interrupt ● 0b1: Enable interrupt	RW
1	CAPMDA	Pattern Selection A ● 0b0: Compare output function ● 0b1: Capture input function	RW

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Bit	Name	Functional Description	Access
0	CSTA	Channel A Timer ON ● 0b0: Channel A timer OFF ● 0b1: Channel A timer ON **Note** This bit will automatically be set to 0 when the hardware trigger stop condition is enable.	RW

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20.3.5 Status Flag Register (TMR0_STFLR)

Offset	Bit Position																													
0x0014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x01000100																															
Name	Reserved							SYDB	Reserved					ICPB	OVFB	CMFB	Reserved							SYDA	Reserved					ICPA	OVFA	CMFA
Access								RO						RW	RW	RW								RO						RW	RW	RW

Bit	Name	Functional Description	Access
31:25	*Reserved*	-	-
24	SYDB	Synchronization Completion Flag B ● 0b0: B channel register is synchronizing during asynchronous counting ● 0b1: B channel register synchronization is completed during asynchronous counting	RO
23:19	*Reserved*	-	-
18	ICPB	Repeat Capture Flag B ● 0b0: No capture input occurred after the count match flag bit CMFB was set to 1 ● 0b1: A capture input occurred again after the count match flag bit CMFB was set to 1	RW
17	OVFB	Count Overflow Flag B ● 0b0: The count value (CNTBR) does not count to 0xFFFF ● 0b1: The count value (CNTBR) counts to 0xFFFF	RW
16	CMFB	Count Match Flag B ● 0b0: The value of the CMPBR register is not equal to the count value (CNTBR) and no capture input action occurs ● 0b1: The value of the CMPBR register is equal to the count value (CNTBR) or a capture input action occurs	RW
15:9	*Reserved*	-	-
8	SYDA	Synchronization Completion Flag A ● 0b0: A channel register is synchronizing during asynchronous counting ● 0b1: A channel register synchronization is completed during asynchronous counting	RO
7:3	*Reserved*	-	-
2	ICPA	Repeat Capture Flag A ● 0b0: No capture input occurred after the count match flag bit CMFA was set to 1 ● 0b1: A capture input occurred again after the count match flag bit CMFA was set to 1	RW

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Bit	Name	Functional Description	Access
1	OVFA	Count Overflow Flag A ● 0b0: The count value (CNTAR) does not count to 0xFFFF ● 0b1: The count value (CNTAR) counts to 0xFFFF	RW
0	CMFA	Count Match Flag A ● 0b0: The value of the CMPAR register is not equal to the count value (CNTAR) and no capture input action occurs ● 0b1: The value of the CMPAR register is equal to the count value (CNTAR) or a capture input action occurs	RW

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20.3.6 Count Synchronization Enable Register (TMR_SYNENR)

Offset	Bit Position																													
0x14	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved											TMRA_5	TMRA_4	TMRA_3	TMRA_2	TMRA_1	Reserved											TMR4	TMR0_1_B	TMR0_1_A	TMR0_2_B	TMR0_2_A
Access												RW	RW	RW	RW	RW												RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:21	*Reserved*	-	-
20	TMRA_5	TimerA_5 Software Start Enable Bit ● 0b0: TimerA unit 5 software start is disabled ● 0b1: TimerA unit 5 software start is enabled, and the timer starts counting **Note** Please use this function in synchronous counting mode.	RW
19	TMRA_4	TimerA_4 Software Start Enable Bit ● 0b0: TimerA unit 4 software start is disabled ● 0b1: TimerA unit 4 software start is enabled, and the timer starts counting **Note** Please use this function in synchronous counting mode.	RW
18	TMRA_3	TimerA_3 Software Start Enable Bit ● 0b0: TimerA unit 3 software start is disabled ● 0b1: TimerA unit 3 software start is enabled, and the timer starts counting **Note** Please use this function in synchronous counting mode.	RW
17	TMRA_2	TimerA_2 Software Start Enable Bit ● 0b0: TimerA unit 2 software start is disabled ● 0b1: TimerA unit 2 software start is enabled, and the timer starts counting **Note** Please use this function in synchronous counting mode.	RW

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Bit	Name	Functional Description	Access
16	TMRA_1	TimerA_1 Software Start Enable Bit ● 0b0: TimerA unit 1 software start is disabled ● 0b1: TimerA unit 1 software start is enabled, and the timer starts counting **Note** Please use this function in synchronous counting mode.	RW
15:5	*Reserved*	-	-
4	TMR4	Timer4 Software Start Enable Bit ● 0b0: Software start for Timer4 is disabled ● 0b1: Software start for Timer4 is enabled, and the timer starts counting	RW
3	TMR0_1_B	Timer0_1 Channel B Software Start Enable Bit ● 0b0: Software start for Timer0 unit 1 Channel B is disabled ● 0b1: Software start for Timer0 unit 1 Channel B is enabled, and the timer starts counting **Note** Please use this function in synchronous counting mode.	RW
2	TMR0_1_A	Timer0_1 Channel A Software Start Enable Bit ● 0b0: Software start for Timer0 unit 1 Channel A is disabled ● 0b1: Software start for Timer0 unit 1 Channel A is enabled, and the timer starts counting **Note** Please use this function in synchronous counting mode.	RW
1	TMR0_2_B	Timer0_2 Channel B Software Start Enable Bit ● 0b0: Software start for Timer0 unit 2 Channel B is disabled ● 0b1: Software start for Timer0 unit 2 Channel B is enabled, and the timer starts counting **Note** Please use this function in synchronous counting mode.	RW
0	TMR0_2_A	Timer0_2 Channel A Software Start Enable Bit ● 0b0: Software start for Timer0 unit 2 Channel A is disabled ● 0b1: Software start for Timer0 unit 2 Channel A is enabled, and the timer starts counting **Note** Please use this function in synchronous counting mode.	RW

Note

- Please do not use the count synchronization function in asynchronous counting mode for this timer.
- TMR_SYNENR is not controlled by the RMU_FRST register.

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20.4 Precautions

1. During asynchronous counting operation, first configure the asynchronous counting mode by setting the BCONR.SYNSA<B> bit, and then start Timer0.
2. When selecting asynchronous counting, when the count value (CNTA<B>R), reference value (CMPAA<B>R), start bit (BCONR.CSTA<B>), and status bit (STFLR.CMFA<B>, STFLR.OVFA<B>, STFLR.ICPA<B>) are modified, Timer0 will write the modified value into the corresponding register after 3 asynchronous counting clocks following the write action.
3. When selecting asynchronous counting, during consecutive write operations to the count value(CNTA<B>R), reference value (CMPA<B>R), start bit (BCONR.CSTA<B>), and status bits (STFLR.CMFA<B>, STFLR.OVFA<B>, STFLR.ICPA<B>), it is necessary to wait until the status bit (STFLR.SYDA<B>) is 1 before performing the next write operation to any of the aforementioned registers.
4. When selecting asynchronous counting, ensure that BCONR.SYNCLKA<B> is set to 0.
5. When writing to BCONR.CSTA<B>, do not simultaneously overwrite BCONR.SYNSA<B> (BCONR.SYNSA<B> must retain its current value); otherwise, BCONR.CSTA<B> cannot be written successfully.

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21 Watchdog Timer (WDT/SWDT)

21.1 Introduction

This product has two watchdog counters: one is a dedicated watchdog counter (SWDT) with an internal RC (32.768kHz) as its count clock source, and the other is a general-purpose watchdog counter (WDT) with PCLK3 as its count clock source. Both the dedicated watchdog and the general-purpose watchdog are 16-bit down counters used to monitor software faults caused by external interference or unforeseen logic conditions that cause the application to deviate from normal operation.

Both watchdogs support the window function. The window interval can be preset before the count starts, and when the count value is within the window interval, the counter can be refreshed and the count restarted.

21.2 Features

Table 21-1 Basic Features of Watchdog Timer

Count Clock	● SWDT: 1/16/32/64/128/256/2048 division of SWDTCLK ● WDT: 4/64/128/256/512/1024/2048/8192 division of PCLK3
Maximum Over-flow Time	● SWDT: 1.16 hours (SWDTCLK=32.768kHz) ● WDT: 10.7 seconds (PCLK3=50MHz)
Counting Mode	Decrement count
Window Function	Can set window interval, define the allowable interval of refresh action
Startup Mode	1. Hardware startup 2. Software startup
Stop Condition	1. Resetting 2. Underflow, refresh error occurs and then restart: ● In hardware startup mode, it starts automatically after a reset or interrupt request is output ● In software startup mode, set refresh register again
Interrupt/Reset Conditions	1. Count underflow 2. Refresh error

21.3 Functional Description

21.3.1 Start the Watchdog

Watchdog counter can be started in two ways: hardware startup mode and software startup mode.

The hardware startup mode refers to the setting of the watchdog counter (ICG0 register) read from the main flash memory area during startup, and the counter automatically starts counting. The software startup mode refers to the process where, after setting the control register, the refresh register is written to complete the refresh action, and the counter starts counting.

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21.3.2 Hardware Startup Mode

When the ICG0.WDTAUTS/SWDTAUTS is set to 0, it is the hardware startup mode. WDT/SWDT_CR settings are ignored in hardware startup mode.

In hardware start mode, the WDT/SWDT-related settings (counting clock, window setting value, counting period, etc.) in the ICG0 register are loaded into the WDT/SWDT module during the reset period. After the reset, the counter automatically starts counting according to the settings. The figure below shows a hardware start mode example.

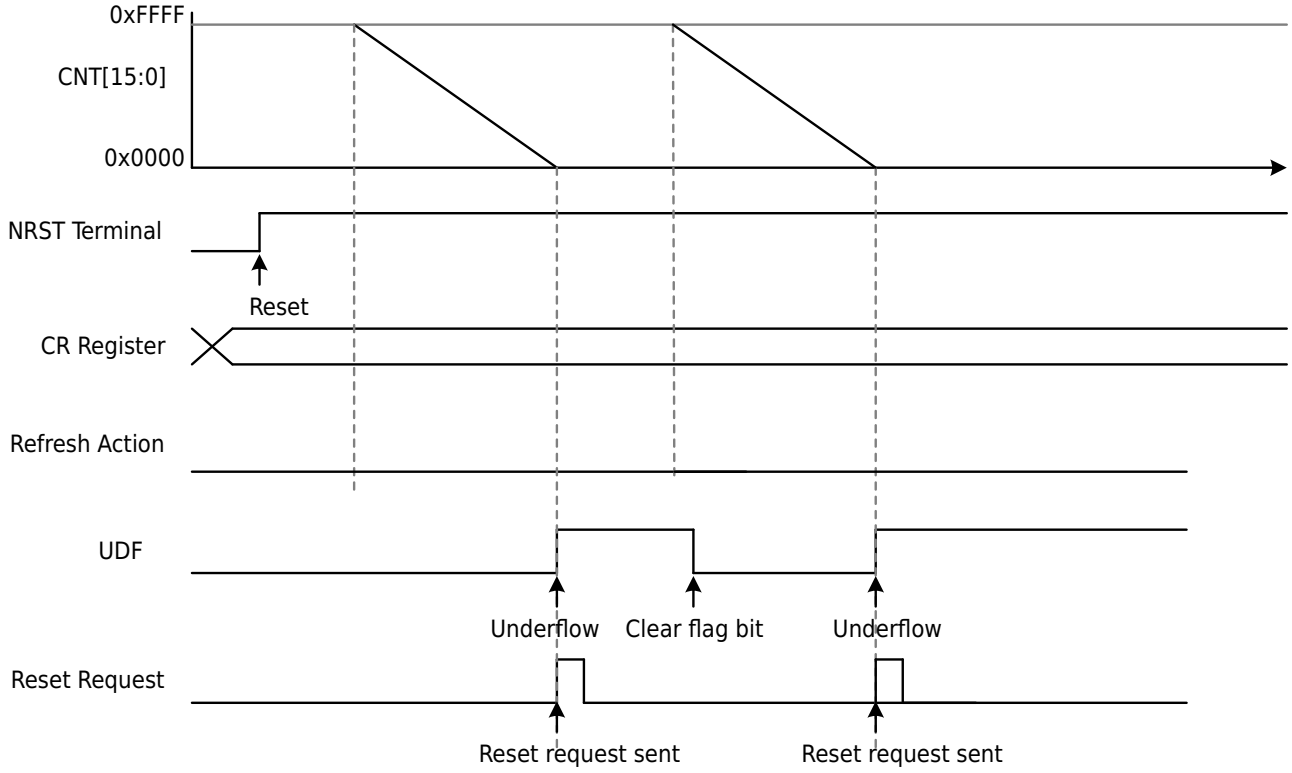

Figure 21-1 Hardware Startup Mode Example

21.3.3 Software Startup Mode

When the ICG0.WDTAUTS/SWDTAUTS is set to 1, WDT/SWDT is started via refresh register (software start mode). After reset, set the counting clock, window setting value, counting period, etc. in the WDT/SWDT_CR register, and then perform the refresh action, and the counter starts to count. WDT/SWDT_CR can be configured only once; subsequent writes are inactive. The figure below shows a software start mode example.

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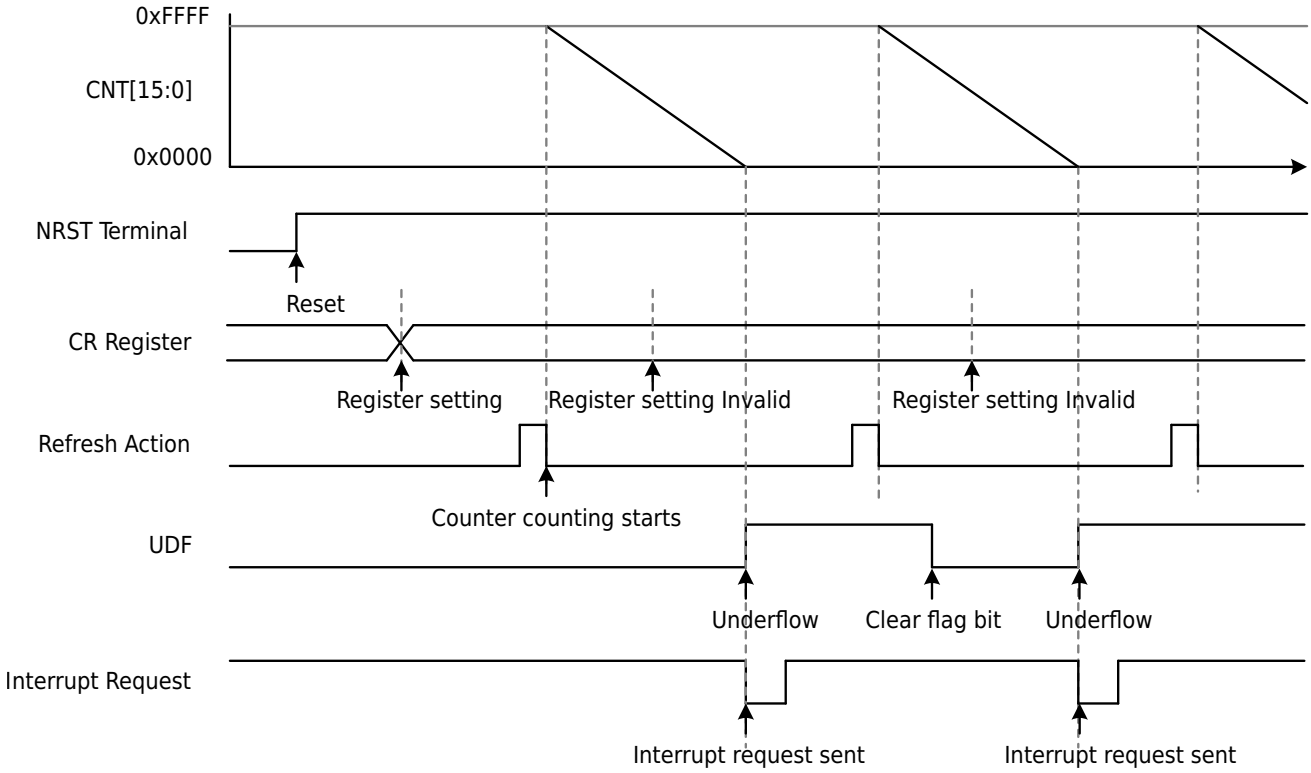

Figure 21-2 Software Startup Mode Example

21.3.4 Refresh Action

A refresh action (write 0x0123 followed by 0x3210 to WDT/SWDT_RR) starts (software start) or restarts the counter.

During the interval between writing 0x0123 and 0x3210 to the WDT/SWDT_RR register, other register accesses or reads do not affect the normal refresh action.

The figure below shows an operation example.

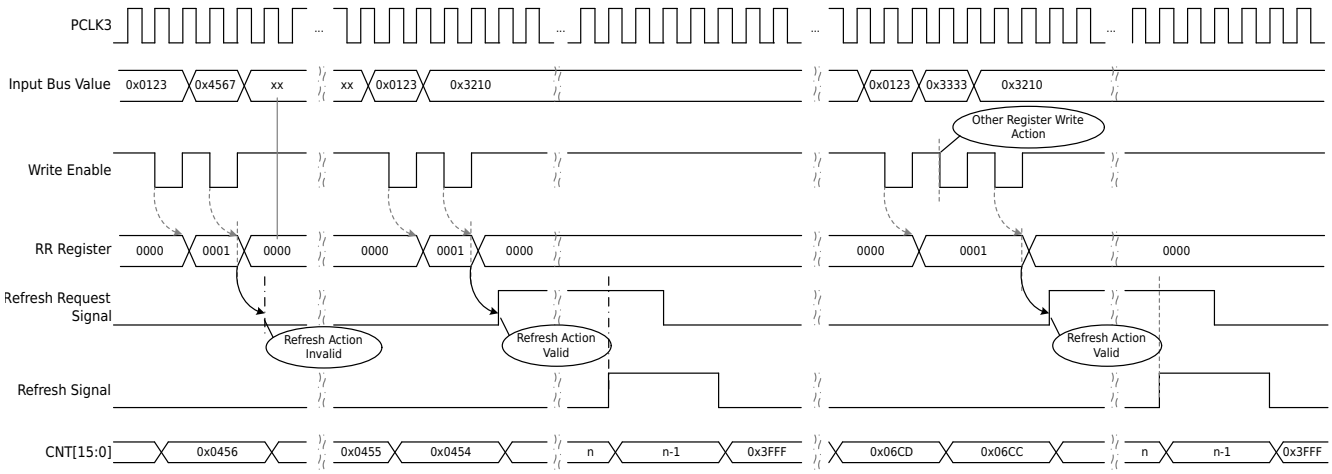

Figure 21-3 Examples of Various Refresh Action Sequences (action confirmation, refresh required signal falling edge, etc.)

Refresh action require 4 clock periods to update the counting. Therefore, complete the writing of the refresh register 4 count values in advance of refreshing the lower window and the underflow position. Check the status register for the count value.

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21.3.5 Flag Bit

Refresh error flag bit and underflow flag bit remain set if an interrupt is requested. Upon entering an interrupt, check the flag bit to identify the cause.

Clear the flag bit: Read "1" first, then write "0".

Note

Within a certain period of time when a refresh error or underflow error occurs, the clear operation of the flag bit has no effect. This period of time is: 1 counting period +2 SWDTCLK (SWDT module); 1 counting period +2 PCLK3 (WDT module).

When refreshing error flag bit and underflow flag bit, the counting of the hardware watchdog does not stop; while counting stops in software start mode. When writing "0" to the flag bit, the SWDT needs at most 3 SWDTCLK and 2 PCLK3 times before the register bit can be cleared to 0. It takes at most five PCLK3 times for the register bit of WDT to be cleared to 0. After clearing the flag bit, it is necessary to re-read the flag bit to confirm whether the clearing operation is successful.

Flag bit clearing procedures:

Step1. Read WDT/SWDT_SR to check the flag bit.

Step2. Write "0" to the flag bit set to "1".

Step3. Read WDT/SWDT_SR to confirm if the flag bit is cleared. Repeat Step 2 if the flag bit remains 1.

21.3.6 Interrupt/Reset

WDT/SWDT can trigger interrupt or reset requests upon counter underflow or refresh error. In hardware startup mode, generate an interrupt or a reset request depending on ICG0.WDTITS/SWDTITS bit. In software startup mode, set the WDT/SWDT_CR.ITS bit to select interrupt or reset request.

WDT/SWDT generates interrupt/reset requests under 2 conditions. One is that counter counts produce underflow; One is to perform a refresh action outside the refresh allowed interval, resulting in a refresh error.

21.3.7 Count Underflow

As shown in the following figure, underflow occurs when the counter decrements to 0.

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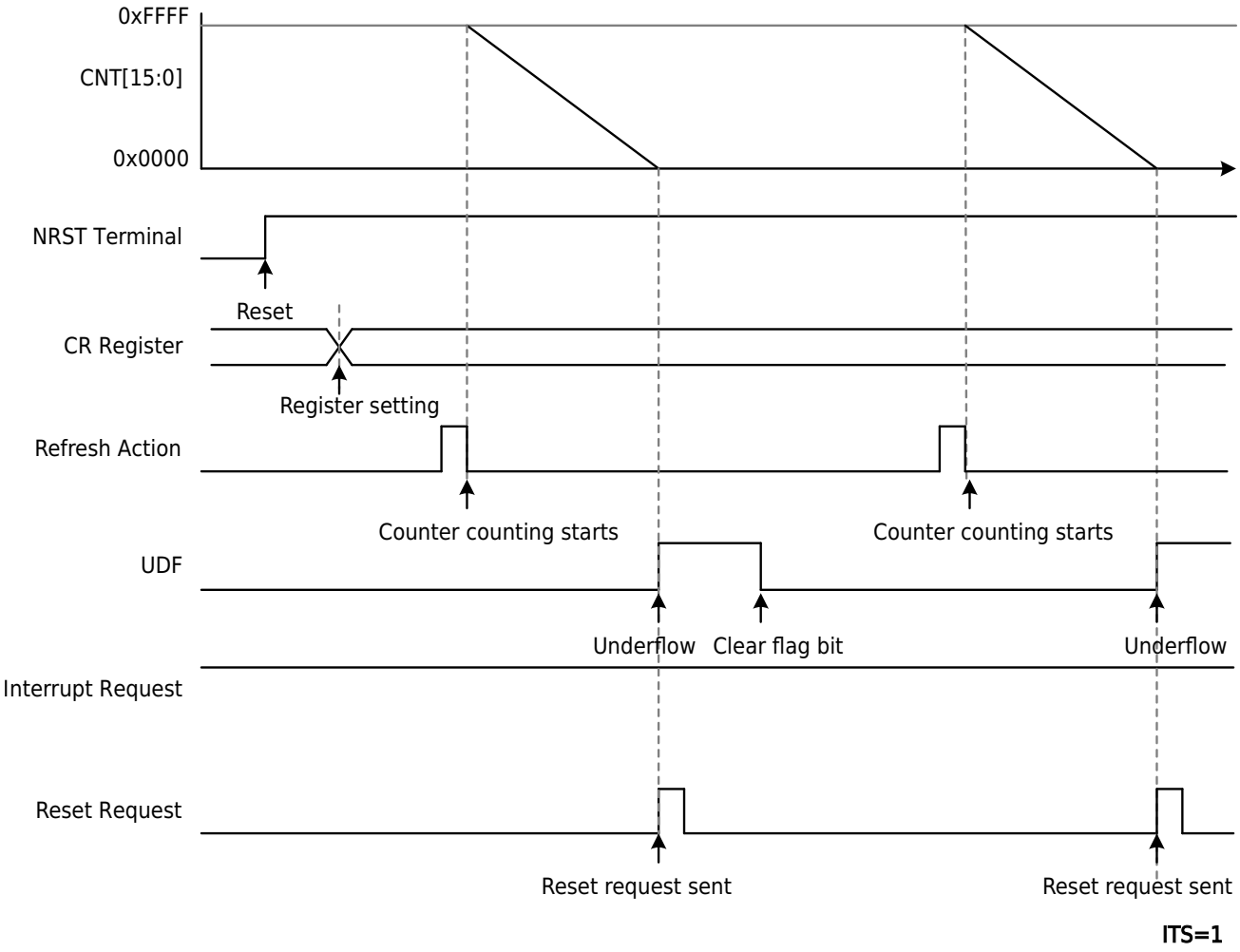

Figure 21-4 Counter Underflow Operation Example

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21.3.8 Refresh Error

After setting the window range, the counter is refreshed and re-counting only when the refresh action is performed within the window range. A refresh error occurs when the refresh action is performed outside the window range. The figure below shows a refresh operation example.

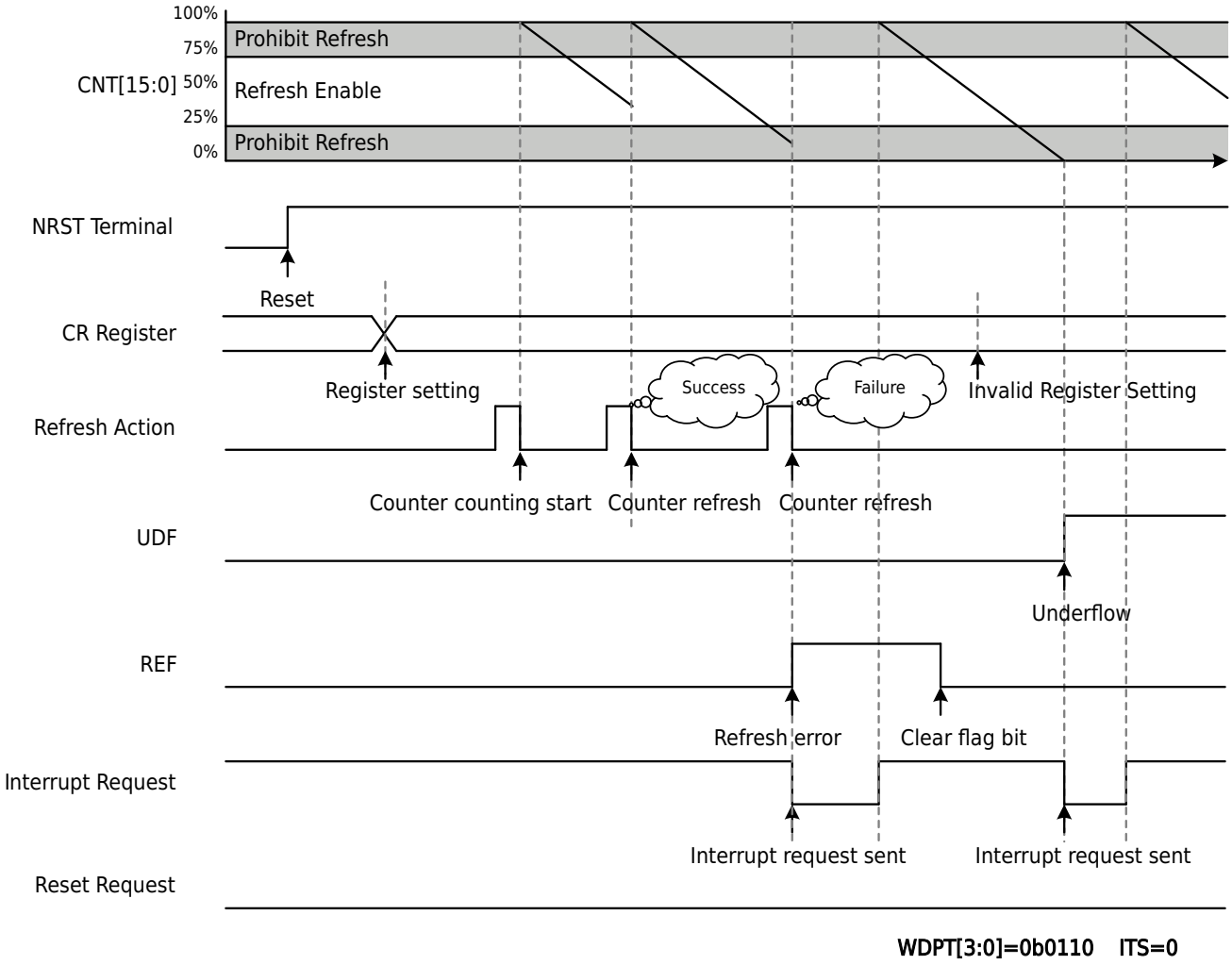

Figure 21-5 Counter Refresh Operation Example

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21.4 Register Description

21.4.1 Register List

WDT base address: 0x40049000

Table 21-2 Watchdog Timer (WDT) Register Offset

Offset	Register	Description	Width
0x00	WDT_CR	WDT Control Register	32
0x04	WDT_SR	WDT Status Register	32
0x08	WDT_RR	WDT Refresh Register	32

SWDT base address: 0x40049400

Table 21-3 Watchdog Timer (SWDT) Register Offset

Offset	Register	Description	Width
0x00	SWDT_CR	SWDT Control Register	32
0x04	SWDT_SR	SWDT Status Register	32
0x08	SWDT_RR	SWDT Refresh Register	32

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21.4.2 Control Register (SWDT_CR, WDT_CR)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x80010FF3																															
Name	ITS	Reserved														SLPOFF	Reserved				WDPT				CKS			Reserved		PERI		
Access	RW															RW					RW				RW					RW		

Bit	Name	Functional Description	Access
31	ITS	Refresh Error/Overflow Interrupt/Reset Selection ● 0b0: Interrupt request ● 0b1: Reset request	RW
30:17	*Reserved*	-	-
16	SLPOFF	WDT/SWDT Counting is Disabled in Low-power Modes WDT_CR: ● 0b0: Enable WDT counting in Sleep mode ● 0b1: Disable WDT counting in Sleep mode SWDT_CR: ● 0b0: Enable SWDT counting in Sleep/Stop mode ● 0b1: Disable SWDT counting in Sleep/Stop mode	RW
15:12	*Reserved*	-	-
11:8	WDPT	Refresh the Percentage of the Allowed Area Count Value ● 0b0000: 0%-100% ● 0b0001: 0%-25% ● 0b0010: 25%-50% ● 0b0011: 0%-50% ● 0b0100: 50%-75% ● 0b0101: 0%-25%, 50%-75% ● 0b0110: 25%-75% ● 0b0111: 0%-75% ● 0b1000: 75%-100% ● 0b1001: 0%-25%, 75%-100% ● 0b1010: 25%-50%, 75%-100% ● 0b1011: 0%-50%, 75%-100% ● 0b1100: 50%-100% ● 0b1101: 0%-25%, 50%-100% ● 0b1110: 25%-100% ● 0b1111: 0%-100%	RW
7:4	CKS	Count Clock WDT_CR: ● 0b0010: PCLK3/4 ● 0b0110: PCLK3/64	RW

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Bit	Name	Functional Description	Access
7:4	CKS	● 0b0111: PCLK3/128 ● 0b1000: PCLK3/256 ● 0b1001: PCLK3/512 ● 0b1010: PCLK3/1024 ● 0b1011: PCLK3/2048 ● 0b1101: PCLK3/8192 ● Others: Setting prohibited SWDT_CR: ● 0b0000: SWDTCLK ● 0b0100: SWDTCLK/16 ● 0b0101: SWDTCLK/32 ● 0b0110: SWDTCLK/64 ● 0b0111: SWDTCLK/128 ● 0b1000: SWDTCLK/256 ● 0b1011: SWDTCLK/2048 ● Others: Setting prohibited	RW
3:2	*Reserved*	-	-
1:0	PERI	Counting Period ● 0b00: 256 cycle ● 0b01: 4096 cycle ● 0b10: 16384 cycle ● 0b11: 65536 cycle	RW

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21.4.3 Status Register (SWDT_SR, WDT_SR)

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved														REF	UDF	CNT															
Access															RW	RW	RO															

Bit	Name	Functional Description	Access
31:18	*Reserved*	-	-
17	REF	Refresh Error Flag ● 0b0: No refresh error ● 0b1: Refresh error occurred After reading a value of 1 from this bit, writing 0 to it will clear this bit.	RW
16	UDF	Counting Underflow Mark ● 0b0: No counter underflow ● 0b1: Counter underflow occurred After reading a value of 1 from this bit, writing 0 to it will clear this bit.	RW
15:0	CNT	Count Value Counter current count	RO

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21.4.4 Refresh Register (SWDT_RR, WDT_RR)

Offset	Bit Position																													
0x08	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																RF															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	RF	Refresh Value Write 0x0123 and 0x3210 sequentially to complete the refresh. After writing 0x0123, the register reads as 0x00000001; in all other cases, it reads as 0x00000000.	RW

21.5 Precautions

During SWDT operation, the frequency of the clock PCLK3 must equal to or greater than 4 timers of counting clock frequency. That is, PCLK3 frequency ≥ counting clock frequency × 4.

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22 Hall Signal Processing Module (HALL)

22.1 Introduction

The Hall Signal Processing Module (HALL) features a 32-bit counting width and 3-channel HALL signal input. It supports digital filtering for the 3-channel HALL signal input.

22.2 Features

The basic functions and features of HALL are shown in the following table.

Table 22-1 HALL Basic Functions and Features

Basic Functions	Hall Signal Change Capture
	Software Write Trigger Hall Signal Change
	Hall Input Signal Digital Filtering
	Capture, Overflow Event Output
Interrupt Types	Capture Interrupt
	Overflow Interrupt

22.3 Functional Description

22.3.1 Functional Block Diagram

The HALL unit integrated in this product series uses PCLK1 as its bus clock and counting clock (in this context, PCLK shown in the block diagram refers to PCLK1). The counting divider clock source for each unit and the sampling reference clock source for port digital filtering are the same as its bus clock and counting clock.

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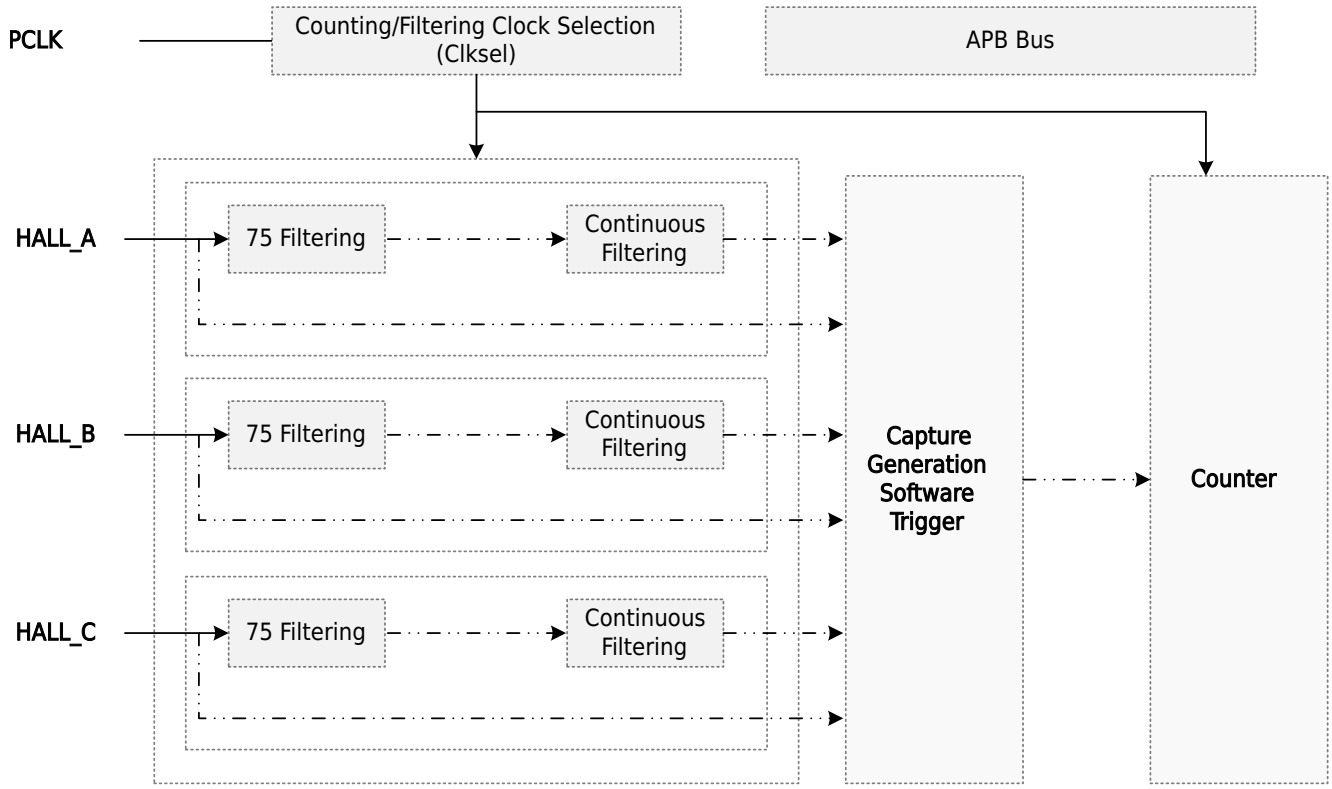

Figure 22-1 HALL Basic Block Diagram

The following table lists the input and output ports of the HALL signal processing module.

Table 22-2 HALL Port List

Port Name	Direction	Function
HALL_A	IN	Hall signal input port
HALL_B		
HALL_C		

22.3.2 Clock Source Selection

The HALL counting clock/filter clock can be selected from the following options:

- 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024 division of PCLK (HALL_CTLR.CKDIV sets both the counting clock and the filter clock simultaneously).

22.3.3 Capture Input

The capture module is used to measure the time between two HALL signal changes. Its core is a 32-bit counter. At a 120 MHz operating frequency, if the HALL clock is divided by 1024, it can record a maximum time width of approximately 36650 seconds, achieving a time resolution of 8.3333 ns.

HALL_CNTR starts counting from 0. When a HALL signal change occurs, the HALL_CNTR value at that moment is saved to the HALL_CAPR register, the filtered HALL signal at that moment is saved to HALL_INFR.FILDAT, and the raw HALL signal is saved to HALL_INFR.RAWDAT. If HALL_CTLR.ITENCHG is 1 at this time, a HALL signal change interrupt is generated, and HALL_CNTR restarts counting from 0.

When the counter value reaches HALL_THDR, if HALL_CTLR.ITENOVF is 1 at this time, a HALL counter overflow interrupt is generated, and the counter restarts counting from 0.

The following figure shows an example of the capture input action.

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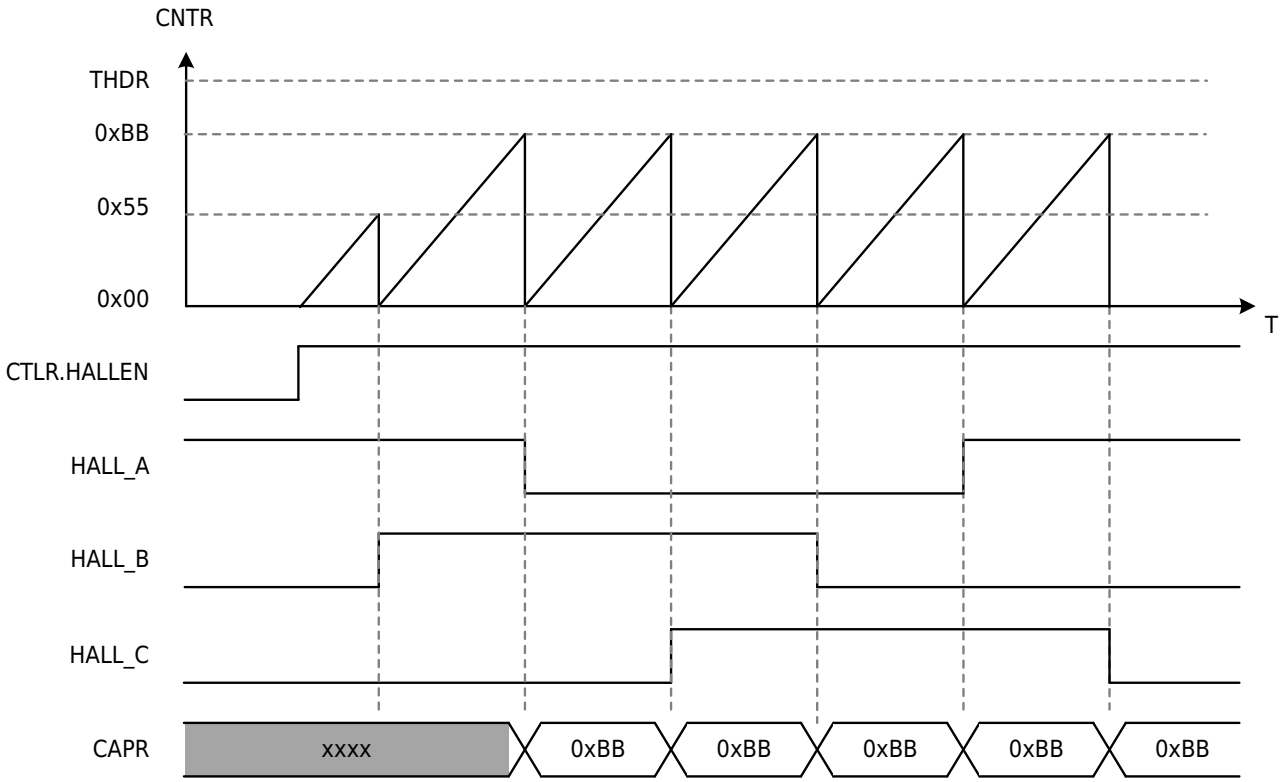

Figure 22-2 Capture Input Action

22.3.4 Digital Filtering

The HALL_A, HALL_B, and HALL_C port inputs of the module all have a digital filtering function. Enabling the port filtering function and selecting the filter clock can be achieved by setting the corresponding bits in the Filter Register (FILR) and the Control Register (CTLR).

The filtering includes two stages:

1. The first stage uses a 7-sample, 5-vote filter. That is, among 7 consecutive sampling points, if 5 or more are 1, the output is 1; if 5 or more are 0, the output is 0; otherwise, the output maintains the previous filter result.

   This is shown in the following figure.

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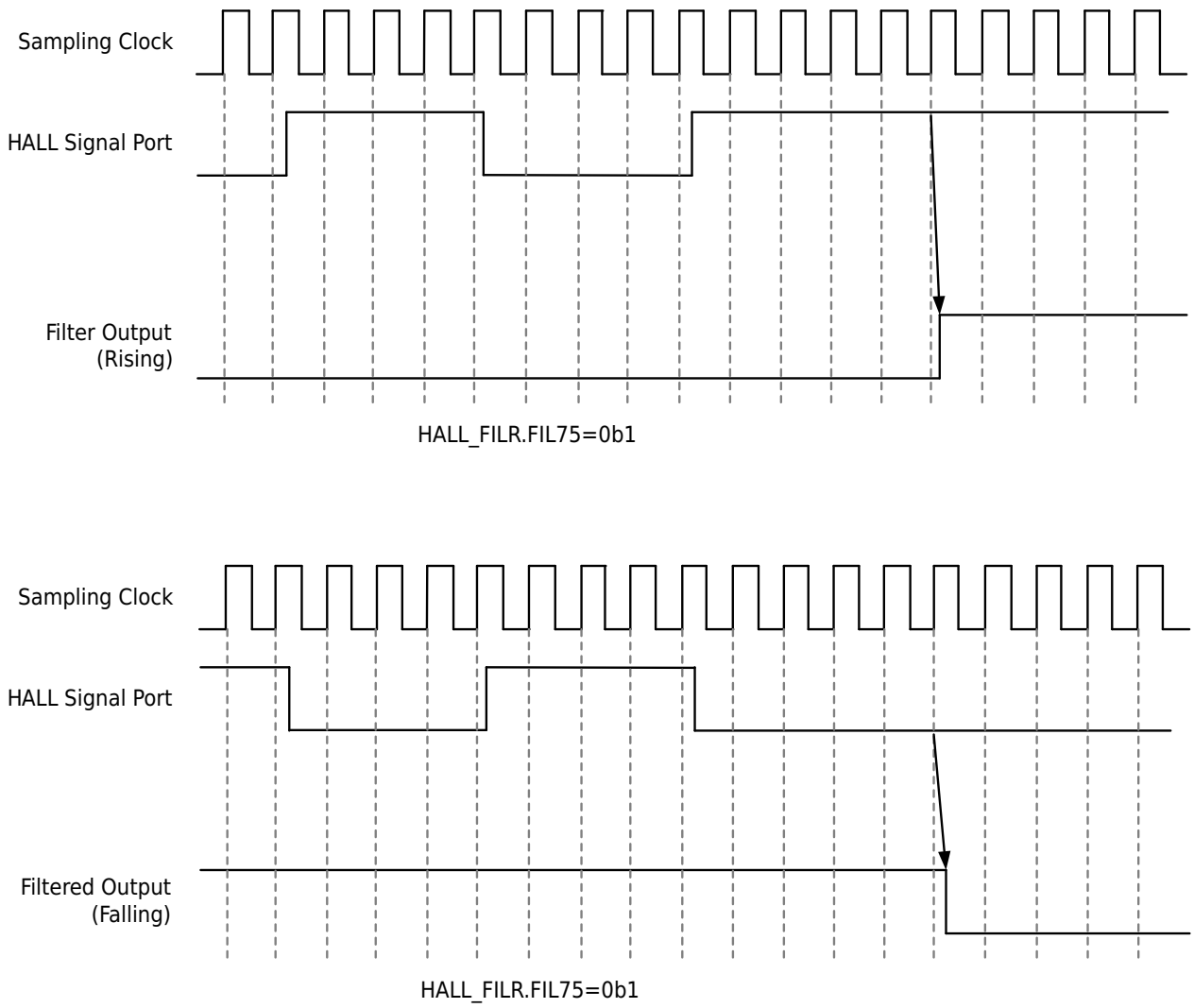

Figure 22-3 Input Port Filtering Function

2. The second stage uses continuous filtering. Among N consecutive sampling points, if all are 0, the output is 0; if all are 1, the output is 1; otherwise, the output maintains the previous filter result.

The register HALL_FILR.FIL75 is used to select whether to enable the first-stage filter. HALL_FILR.FILLEN is used to configure the second-stage filter depth, which is the number of consecutive samples. The maximum number of consecutive samples is 2^{15}. The filter time calculation formula is as follows:

$T_{fit} = T_{clk} * (HALL_FILR.FILLEN + 1)$

By accessing HALL_INFR.FILDATA, the filtered HALL signal can be captured; HALL_INFR.RAWDATA is the raw HALL input signal before filtering.

22.3.5 Interrupt

The HALL contains 2 interrupt outputs and 2 event outputs, which are 1 capture interrupt and event, and 1 overflow match interrupt and event.

22.3.5.1 Capture Interrupt and Event

When the HALL signal changes, the information register HALL_INFR.CHGF bit is set to 1. At this time, if the HALL_CTLR.ITENCHG bit is set to 1 to enable the interrupt, the corresponding interrupt request (HALL_CHGINT) is triggered and output to the interrupt module (INTC). The capture event does not have a corresponding enable bit control; it is triggered at the moment of the corresponding HALL signal change and outputs the capture event (HALL_CHGAOS) for selecting to trigger other modules.

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If both the HALL_CTLR.ITENSW bit and the HALL_CTLR.ITENCHG bit are set to 1, writing to the HALL_INFR.SWF bit by software can also trigger the interrupt request (HALL_CHGINT) to be output to the interrupt controller (INTC), while simultaneously outputting the capture event (HALL_CHGAOS) for selecting to trigger other modules.

22.3.5.2 Overflow Interrupt and Event

When the counter increments to the overflow point, the HALL_INFR.OVFF bit in the information register is set to 1. At this point, if the HALL_CTLR.ITENOVF bit is set to 1 to enable the interrupt, an overflow interrupt (HALL_OVFINT) is triggered at the corresponding overflow point and output to the interrupt module (INTC). The overflow event does not have a corresponding enable bit control; it triggers an overflow match event (HALL_OVFAOS) at the corresponding count overflow point, which is output for selecting to trigger other modules.

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22.4 Register Description

22.4.1 Register List

Base Address: 0x4001E800

Table 22-3 Hall Signal Processing Module (HALL) Register Offset

Offset	Register	Description	Width
0x0000	HALL_CTLR	Control Register	16
0x0004	HALL_FILR	Filter Register	32
0x0008	HALL_INFR	Information Register	32
0x0010	HALL_CAPR	Capture Register	32
0x0020	HALL_THDR	Threshold Register	32
0x0030	HALL_CNTR	Counter Register	32

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22.4.2 Count Register (HALL_CNTR)

Offset	Bit Position																													
0x0030	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	CNT																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	CNT	Count Value Specifies the current count value of the timer	RW

22.4.3 Threshold Register (HALL_THDR)

Offset	Bit Position																													
0x0020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFFFFFFFF																															
Name	THD																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	THD	Counting Threshold Value Specifies the counting threshold value	RW

22.4.4 Capture Register (HALL_CAPR)

Offset	Bit Position																													
0x0010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	CAP																															
Access	RO																															

Bit	Name	Functional Description	Access
31:0	CAP	Capture Value Reads the capture value	RO

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22.4.5 Control Register (HALL_CTLR)

Offset	Bit Position															
0x0000	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x3000															
Name	Reserved		SWCLR	CAPCLR	Reserved	ITENSW	ITENOVF	ITENCHG	CKDIV				Reserved			HALLEN
Access			RW	RW		RW	RW	RW	RW							RW

Bit	Name	Functional Description	Access
15:14	*Reserved*	-	-
13	SWCLR	Software-triggered Capture CNTR Clear Enable Bit ● 0b0: Disable ● 0b1: Enable **Note** When both ITENSW and SWCLR are 1, writing to the HALL_INFR.SWF bit by software triggers a HALL signal change and clears HALL_CNTR.	RW
12	CAPCLR	HALL Signal Change Capture CNTR Clear Enable Bit ● 0b0: Disable ● 0b1: Enable **Note** When CAPCLR is 1, HALL_CNTR is cleared whenever any of the HALL_A/B/C signals changes.	RW
11	*Reserved*	-	-
10	ITENSW	Software Write Triggers HALL Signal Change ● 0b0: Disable ● 0b1: Enable **Note** When ITENSW is 1, writing to the HALL_INFR.SWF bit by software triggers a HALL signal change.	RW
9	ITENOVF	Overflow Interrupt Enable ● 0b0: Disable ● 0b1: Enable	RW
8	ITENCHG	HALL Signal Change Interrupt Enable ● 0b0: Disable ● 0b1: Enable	RW

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Bit	Name	Functional Description	Access
7:4	CKDIV	Count Clock Selection ● 0b0000: PCLK ● 0b0001: PCLK/2 ● 0b0010: PCLK/4 ● 0b0011: PCLK/8 ● 0b0100: PCLK/16 ● 0b0101: PCLK/32 ● 0b0110: PCLK/64 ● 0b0111: PCLK/128 ● 0b1000: PCLK/256 ● 0b1001: PCLK/512 ● 0b1010: PCLK/1024	RW
3:1	*Reserved*	-	-
0	HALLEN	HALL Module Enable ● 0b0: Counting stopped ● 0b1: Counting enabled	RW

22.4.6 Filter Register (HALL_FILR)

Offset	Bit Position																													
0x0004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved															FIL75	Reserved	FILLEN														
Access																RW		RW														

Bit	Name	Functional Description	Access
31:17	*Reserved*	-	-
16	FIL75	75 Filter Enable ● 0b0: Disable ● 0b1: Enable	RW
15	*Reserved*	-	-
14:0	FILLEN	Continuous Filter Width If set to 0, the continuous filter function is not enabled.	RW

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22.4.7 Information Register (HALL_INFR)

Offset	Bit Position																													
0x0008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved													SWF	OVRFF	CHGF	Reserved					RAWDAT			Reserved				FILDAT			
Access														WO	RW	RW						RO							RO			

Bit	Name	Functional Description	Access
31:19	*Reserved*	-	-
18	SWF	Software Trigger HALL Signal Change When HALL_CTLR.ITENSW is 1, writing this bit by software can trigger a HALL signal change event; if HALL_CTLR.ITENCHG is also 1, it can also trigger a HALL signal change interrupt request.	WO
17	OVRFF	Counter Overflow Event Flag Write 0 to clear the flag, write 1 has no effect. Read: ● 0b0: Counter overflow event has not occurred. ● 0b1: Counter overflow event has occurred.	RW
16	CHGF	HALL Signal Change Event Flag Write 0 to clear the flag, write 1 has no effect. Read: ● 0b0: HALL signal change event has not occurred. ● 0b1: HALL signal change event has occurred.	RW
15:11	*Reserved*	-	-
10:8	RAWDAT	Raw HALL Signal Latches the 3-channel raw HALL signals when a HALL signal change occurs.	RO
7:3	*Reserved*	-	-
2:0	FILDAT	Filtered HALL Signal Latches the 3-channel filtered HALL signals when a HALL signal change occurs.	RO

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23 Universal Synchronous Asynchronous Receiver/Transmitter (USART)

23.1 Introduction

This product is equipped with 4 units of Universal Synchronous Asynchronous Receiver/Transmitter (USART) modules, which can flexibly exchange full-duplex data with external devices; the USART equipped in this product supports universal asynchronous serial communication interface (UART) , clock synchronous communication interface, smart card interface (ISO/IEC7816-3) and LIN communication interface. Support modem operation (CTS/RTS operation), multiprocessor operation, DE function, receive timeout function. USART1 supports the STOP mode wake-up function via the RX line.

23.2 Features

Function	Support Module			
	USART1	USART2	USART3	USART4
UART	✓	✓	✓	✓
Multiprocessor Communication	✓	✓	✓	✓
Clock Synchronization Communication	✓	✓	✓	✓
Wake-up from STOP Mode via RX Line	✓	-	-	-
Fractional Baud Rate	✓	✓	✓	✓
LIN	-	✓	✓	✓
Smart Card	✓	-	-	-
UART Receive Timeout Function	✓	✓	✓	✓
RS485 Driver Enable	✓	✓	✓	✓

USART Features

- Support full-duplex asynchronous communication and full-duplex clock synchronous communication
- Support LIN bus
- Support smart card interface (ISO/IEC7816-3)
- Transmitter and receiver have independent enable bits
- Built-in double buffer
- LSB/MSB optional
- Support modem operation (CTS/RTS)
- Transmission flag: transmit data register empty, transmit data complete, receive data register full, receive error flag, UART receive timeout flag, LIN wake-up signal detection flag, LIN interval segment detection flag, LIN synchronization segment detection flag, LIN bus error flag
- Support RS485 Driver Enable function

UART Features

- Data length programmable: 8 bits/9 bits
- Parity function configurable: odd parity/even parity/no parity
- Stop bit configurable: 1 bit/2 bits

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- Clock source optional: internal clock source (clock generated by internal baud rate generator) /external clock source (clock input from USARTn_CK pin)
- Receive error: parity error, frame error, overflow error
- Support for inter-processor communications
- Built-in digital filter
- Supports receiving data TIMEOUT function
- Unit 1 supports stop mode wake-up function
- Unit 2, 3, 4 supports 10/11-bit synchronization Break Field (BF) detection and 10/11/13/14-bit Break Field (BF) transmission
- Supports full-duplex/half-duplex communication mode

Clock Synchronization Mode Features

- Data length: 8 bits
- Receive error: overflow error
- Clock source: internal clock source (clock generated by internal baud rate generator) /external clock source (clock input by USARTn_CK pin)
- Supports full-duplex communication mode

Smart Card Interface Features

- Data length: 8 bits
- When a parity error is detected, it can automatically send out an error signal
- Support data retransmission

LIN Features

- Data length: 8 bits
- Supports wake-up signal detection
- Supports 10/11-bit synchronization Break Field (BF) detection
- Supports synchronization segment measurement, register records measurement value
- Supports 10/11/13/14-bit Break Field (BF) transmission
- Supports bus conflict detection
- Supports loop mode

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23.3 Functional Description

23.3.1 System Block Diagram

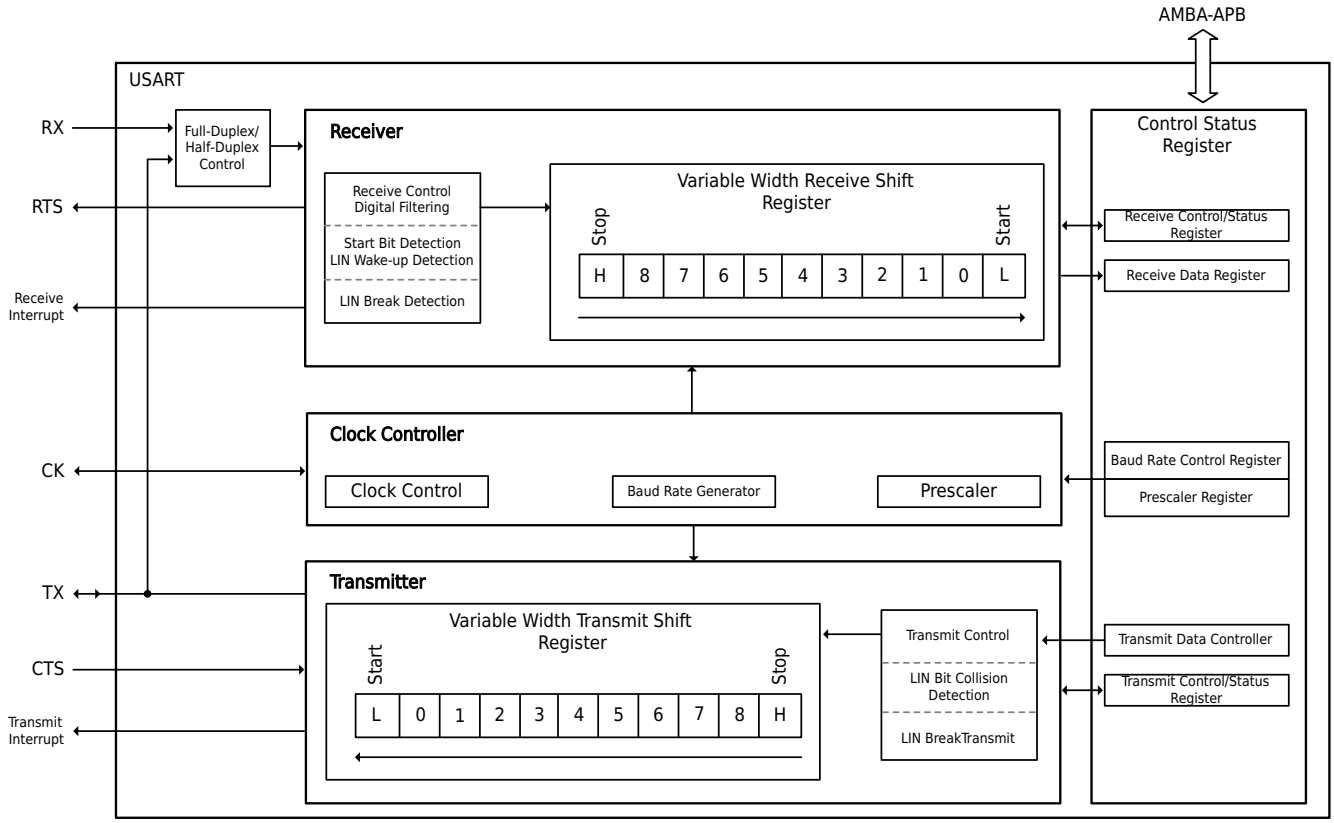

Figure 23-1 USART System Block Diagram

Table 23-2 USART pin description

Pin Name	Direction	Description
USARTn_CK	Input/Output	Clock
USARTn_TX	Input/Output	Transmit data pin Also used as receive data pin in half-duplex mode
USARTn_RX	Input	Receive data pin
USARTn_CTS	Input	Modem operation pin Clear send pin
USARTn_RTS/DE	Output	Modem operation pin Request send pin/Driver Enable pin

Note

The value of n is 1-4.

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23.3.2 UART Function

23.3.2.1 Clock

The UART can select either the clock generated by the internal baud rate generator (internal clock source) or the clock input from the USARTn_CK pin (external clock source) as the communication clock source.

Internal Clock Source

When USARTn_CR2.CLKC bit is set to 0b00 or 0b01, the clock source is selected as the internal clock source, i.e., the clock generated by the internal baud rate generator.

- When USARTn_CR2.CLKC=0b00, the USARTn_CK pin is not used as a clock pin and can function as a general-purpose IO.
- When USARTn_CR2.CLKC=0b01, the USARTn_CK pin outputs a clock with the same frequency as the communication baud rate.

When USARTn_PR.ULBREN is 0, the clock source of the internal baud rate generator is selected by the USARTn_PR.PSC bit setting as PCLK1, PCLK1/4, PCLK1/16, PCLK1/64. When USARTn_PR.ULBREN is 1, the ultra-low baud rate function is enabled, and the clock source of the internal baud rate generator is selected by the USARTn_PR.PSC bit setting as PCLK1/128, PCLK1/256, PCLK1/512, PCLK1/1024.

External Clock Source

When USARTn_CR2.CLKC bit is set to 0b10 or 0b11, the clock source is selected as the external clock input from the USARTn_CK pin. The input clock frequency is 16 times the baud rate (when USARTn_CR1.OVER8=0) or 8 times the baud rate (when USARTn_CR1.OVER8=1).

Maximum Baud Rate

When the internal clock source is selected, the baud rate generated by the internal baud rate generator is calculated using the following formula:

$$B = \frac{C}{8 \times (2 - OVER8) \times (DIV_Integer+1)}$$

Where:

- B: Baud rate, unit: Mbps
- C: When USARTn_PR.ULBREN is 0, the clock set by USARTn_PR.PSC bit (PCLK1, PCLK1/4, PCLK1/16, PCLK1/64), unit: MHz

  When USARTn_PR.ULBREN is 1, the clock set by USARTn_PR.PSC bit (PCLK1/128, PCLK1/256, PCLK1/512, PCLK1/1024), unit: MHz
- OVER8: USARTn_CR1.OVER8 setting value
- DIV_Integer: USARTn_BRR.DIV_Integer setting value

Maximum Baud Rate is PCLK1/8 (Mbps).

When using an External Clock Source, the maximum frequency requirement for the external input UART Clock is PCLK1/4 (MHz). Therefore, when the Clock Source is an external input clock:

- If USARTn_CR1.OVER8=0, the Maximum Baud Rate is PCLK1/64 (Mbps).
- If USARTn_CR1.OVER8=1, the Maximum Baud Rate is PCLK1/32 (Mbps).

Please note that in addition to the PCLK1-based calculation method described above for the maximum UART baud rate, you must also refer to the maximum communication baud rate specified in the "Electrical Specifications" chapter in the Datasheet.

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23.3.2.2 Data Format

A frame of data in UART mode consists of start bit, data bit, check bit, and stop bit.

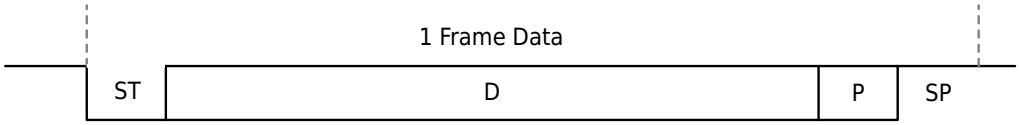

Figure 23-2 UART Data Format

- **Start Bit (ST) :** The start bit is always composed of one bit at low level.
- **Data Bit (D) :** The data bit can be configured as 8-bit or 9-bit.
- **Check Bit (P) :** The check bit can be configured as 1-bit even parity, 1-bit odd parity, or no check bit.
- **Stop Bit (SP) :** The stop bit is fixed at high level and can be configured as 1 bit or 2 bits.

23.3.2.3 Modem Operation

Modem operations include the CTS function and RTS function. When USARTn_CR3.RTSE=1, the RTS function is enabled. When USARTn_CR3.CTSE=1, the CTS function is enabled.

CTS Function

The CTS function controls data transmission via the input of the USARTn_CTS pin. Data can only be transmitted when the USARTn_CTS pin input is at low level. If the USARTn_CTS input transitions to high level during transmission, the ongoing data transmission is unaffected.

RTS Function

The RTS function outputs a low level through the USARTn_RTS pin to request the peer to transmit data.

The USARTn_RTS pin outputs a low level when all of the following conditions are met:

- Receive Enable (USARTn_CR1.RE=1) and not currently receiving data.
- No unread receive data is in the USARTn_RDR.RDR register.
- No reception errors occurred, including frame errors, parity errors, and overflow errors.

23.3.2.4 Transmitter

The transmitter can send 8-bit or 9-bit data, depending on the setting of the USARTn_CR1.M bit.

When USARTn_CR1.TE bit is set to 1, the data is serially output on the TX pin after writing transmit data. The corresponding clock pulses can be optionally output or not output on the USARTn_CK pin.

The sequence for transmitting data is: Start Bit -> Data Bit (MSB/LSB) -> Check Bit (if present) -> Stop Bit.

The transmit data register (TDR) and the internal transmit shift register form a double-buffered structure, enabling continuous data transmission.

When transmitting data via the transmit data register empty interrupt or DMA, to ensure transmission accuracy, only one data write can be performed per request.

Transmit Data Setting Procedure

Step1. Set the USARTn_CR1 register to its reset value;

Step2. Configure the pins required for UART operation;

Step3. Select the clock source via the USARTn_CR2.CLKC bit;

Step4. Configure the USARTn_CR1, USARTn_CR2, and USARTn_CR3 Registers;

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Step5. Set USARTn_PR to select the prescaler value, and configure the USARTn_BRR register for communication baud rate (no setting required when the clock source is an external clock source);

Step6. Enable the transmitter (USARTn_CR1.TE=1). If the transmit data register empty interrupt is required, set USARTn_CR1.TXEIE=1.

Step7. Wait for the transmit data register to be empty, write communication data to USARTn_TDR.TDR, data is transferred to the transmit shift register, transmission starts;

> **Note**
> When the CTS function is enabled, data is transferred to the transmit shift register and transmission starts when the USARTn_CTS input is at low level.

Step8. To continuously transmit data, repeat step7;

Step9. Check whether the transmission is complete by verifying the USARTn_SR.TC bit. For continuous data transmission using transmit interrupts, the last data can be written via the TI interrupt by setting USARTn_CR1.TXEIE to 0 and USARTn_CR1.TCIE to 1. A transmit completion interrupt will be generated after the last frame transmission ends.

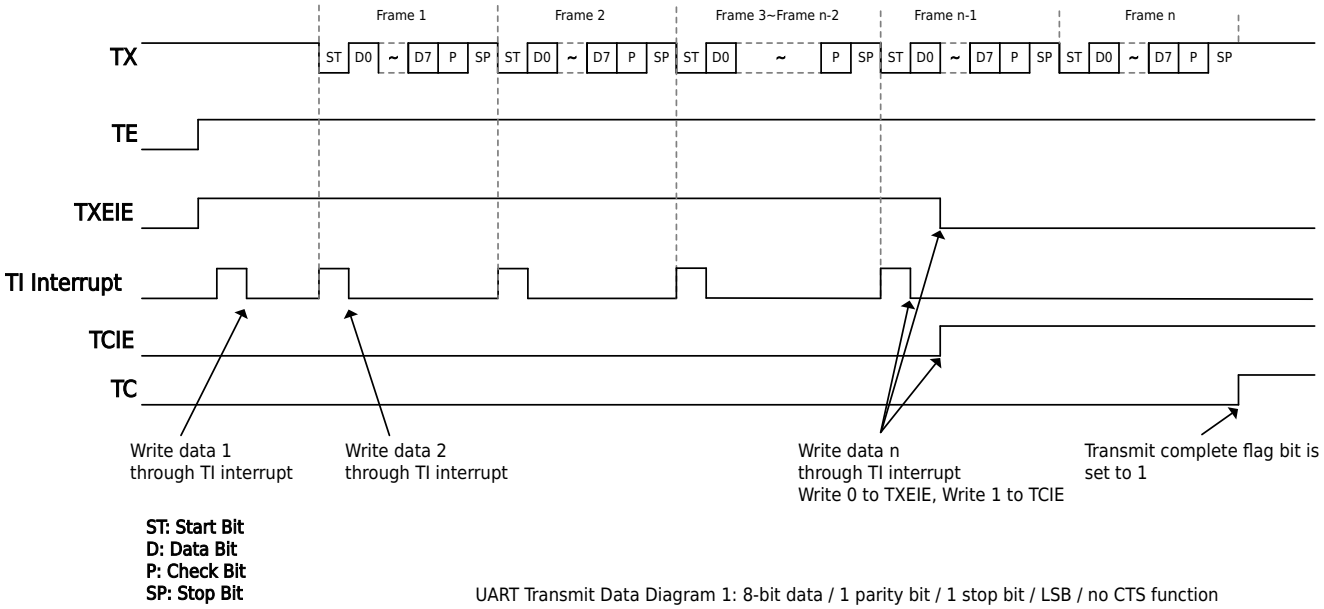

Figure 23-3 UART Transmit Data Diagram 1

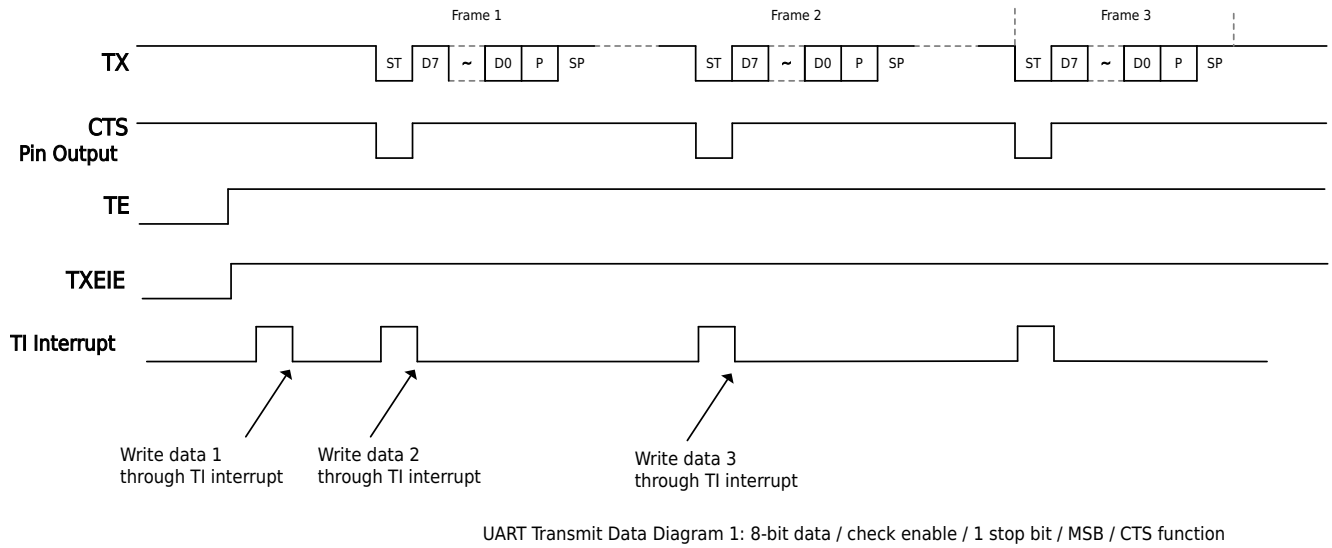

Figure 23-4 UART Transmit Data Diagram 2

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Transmitter Interrupt

In UART mode, the transmitter supports two interrupts: transmit data register empty interrupt (TI) and transmit completion interrupt (TCI).

- TXEIE=1, when the value of USARTn_TDR.TDR register is transferred to the transmit shift register, a TI interrupt is generated.
- TCIE=1, when the last bit of transmitted data is sent and the USARTn_TDR.TDR register is not updated, a TCI interrupt is generated.

23.3.2.5 Receiver

The receiver can receive 8-bit or 9-bit data, depending on the setting of the USARTn_CR1.M bit. After the receiver enable bit (USARTn_CR.RE) is set to 1 and the start bit is detected, the data on the RX pin is received into the receive shift register. Once a complete frame of data is received, the data is transferred from the receive shift register to the receive data register USARTn_RDR.RDR.

The sequence for receive data is: start bit -> data bit (MSB/LSB) -> check bit (present or absent) -> stop bit.

The receive data register USARTn_RDR.RDR and the internal receive shift register form a double-buffered structure, enabling continuous data reception.

When receiving data through the receive data register full interrupt or DMA, only one data read operation can be performed per request.

Start Bit Detection

Start bit detection can be configured for either low level or falling edge detection, determined by the USARTn_CR1.SBS bit. When USARTn_CR1.SBS=0, low level detection is selected; when USARTn_CR1.SBS=1, falling edge detection is selected.

Sampling and Reception Tolerance

Upon detecting a start condition (low level or falling edge), the USART synchronizes the receive data with the internal basic clock to initiate data reception.

Data sampling occurs at the center of the data. When USARTn_CR1.OVER8=0, sampling is performed on the 8th internal basic clock; when USARTn_MR.OVER8=1, sampling is performed on the 4th internal basic clock.

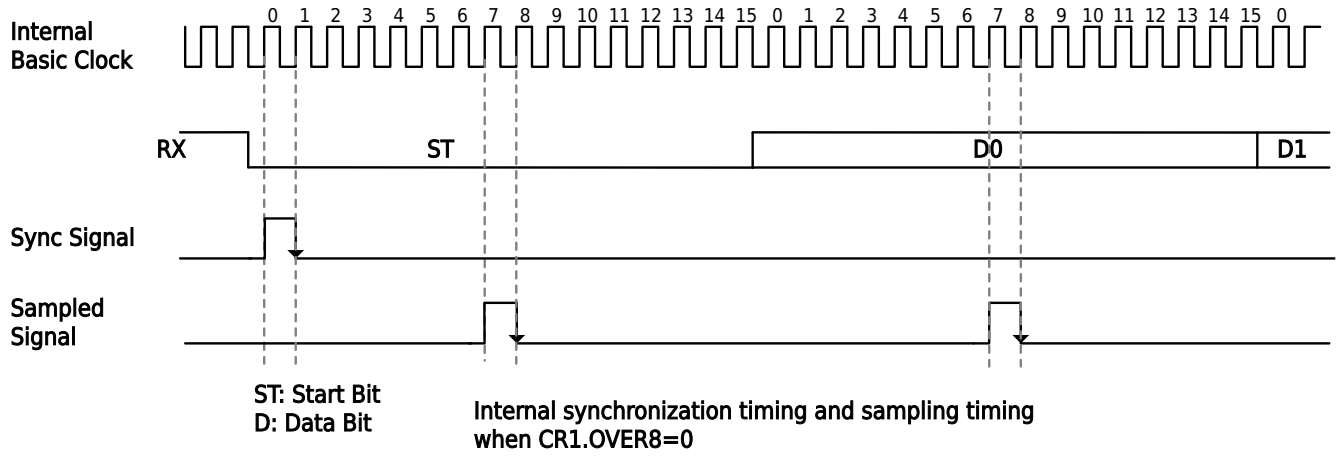

Figure 23-5 UART Internal Synchronization and Sample Timing

The UART asynchronous receiver can only operate normally when the total clock system deviation is less than the tolerance of the UART receiver. Factors affecting the total deviation include:

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- Deviation caused by transmitter error (including the deviation of the transmitter local oscillator)
- Error caused by baud rate quantization of the receiver
- Deviation of the receiver local oscillator
- Deviation caused by transmission line

For correct receive data, the maximum deviation value allowed by the UART asynchronous receiver depends on the following options:

- Frame Length (FL). FL is determined by the 8 or 9 data bits defined by the USARTn_CR1.M bit and the parity enable bit defined by the PCE bit.
- The oversampling ratio (8x or 16x) is defined by the USARTn_CR1.OVER8 bit.
- The USARTn_CR1.FBME bit defines whether to use fractional baud rate.

Table 23-3 Tolerance of UART Receiver

FL	DIV_Fraction is 0		DIV_Fraction is not 0	
	OVER8 bit=0	OVER8 bit=1	OVER8 bit=0	OVER8 bit=1
10	4.375%	3.75%	3.88%	3%
11	3.97%	3.41%	3.53%	2.73%
12	3.646%	3.125%	3.23%	2.5%

Note

Under special circumstances, when the RX pin receives continuous high level signals for the duration of FL, the data specified in the above table may vary slightly.

Receive Data Setting Procedure

Step1. Set the USARTn_CR1 register to its reset value;

Step2. Configure the pins required for UART operation;

Step3. Select the clock source via the USARTn_CR2.CLKC bit;

Step4. Configure the USARTn_CR1, USARTn_CR2, and USARTn_CR3 registers;

Step5. Set USARTn_PR to select the prescaler value, and configure the USARTn_BRR register for communication baud rate (no setting required when the clock source is an external clock source);

Step6. Enable the receiver (USARTn_CR1.RE=1). If receive interrupt is required, set USARTn_CR1.RIE=1.

Step7. Upon detecting the start bit, the receiver loads the data into the receive shift register and verifies the check bit and stop bit.

- When a parity error occurs, the received data is transferred to the USARTn_RDR.RDR register and the USARTn_SR.PE flag is set.
- When the stop bit is not at a high level, a frame error occurs. The received data is transferred to the USARTn_RDR.RDR register, and the USARTn_SR.FE flag is set.
- When an overflow error occurs, data is lost and the USARTn_SR.ORE flag is set.
- When no error occurs, the received data is transferred to the USARTn_RDR.RDR register, and the USARTn_SR.RXNE flag is set. By repeating 7 after reading the received data, continuous data reception can be achieved.

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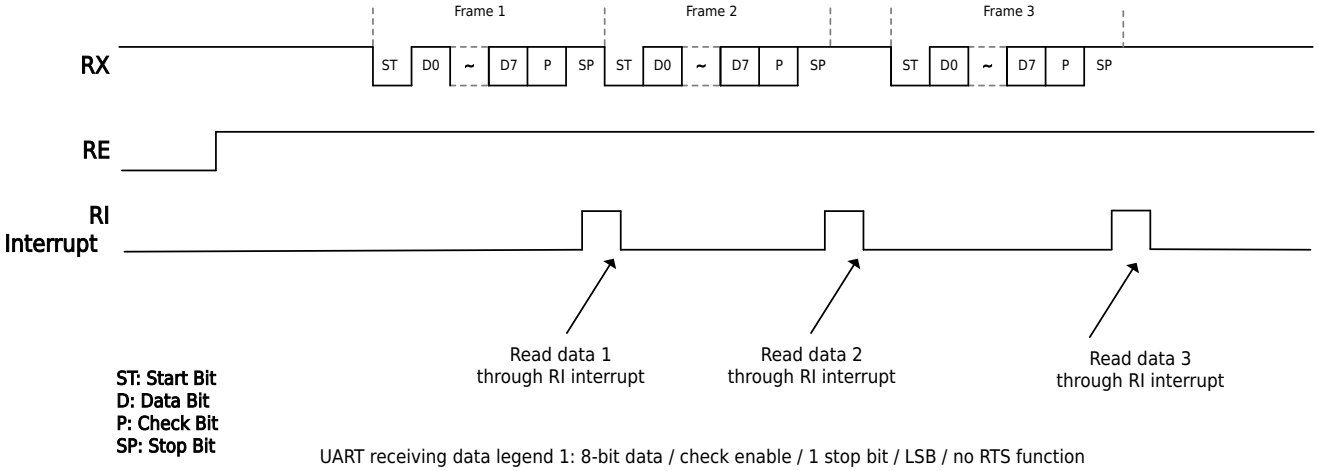
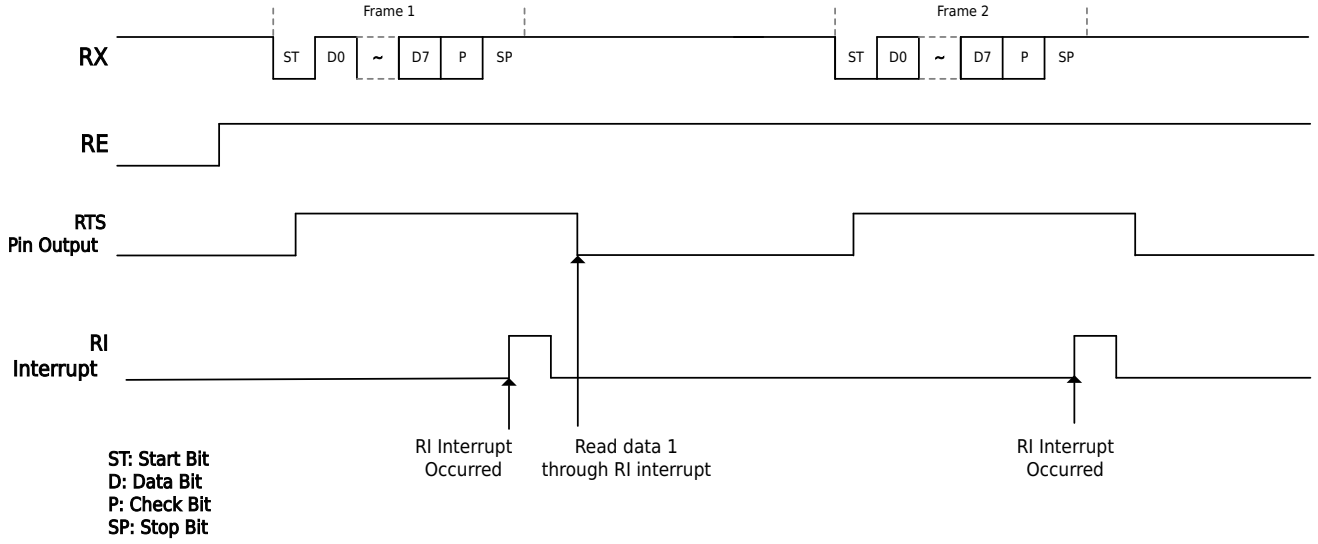


UART receiving data legend 1: 8-bit data / check enable / 1 stop bit / LSB / no RTS function

Figure 23-6 UART Receive Data Diagram 1



UART receiving data legend 2: 8-bit data / check enable / 1 stop bit / LSB / RTS function

Figure 23-7 UART Receive Data Diagram 2

Error Handling

During data reception, there are three types of receive errors: overflow error (USARTn_SR.ORE), parity error (USARTn_SR.PE), and frame error (USARTn_SR.FE). If any type of reception error occurs, data reception is disabled. To restart data reception, all error flags can be cleared by writing to the corresponding clear register. If the error is an overrun error, the error flag can be cleared by writing to the USARTn_CR1.CORE flag bit and performing a read operation on the USARTn_RDR.RDR register.

The condition for overflow error occurrence is when a new frame of data is received while the USARTn_RDR.RDR register value remains unread. Therefore, the previously received frame data should be read before the last bit of the current frame is received.

The condition for check error occurrence is when a parity check error happens.

The condition for frame error occurrence is when the stop bit is at low level. For 2-stop-bit cases, only the first stop bit is checked.

When an overflow error occurs, the received data is lost and no RI interrupt is generated.

When a parity error occurs, the received data is transferred to USARTn_RDR.RDR, and no RI interrupt is generated.

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When a frame error occurs, the received data is transferred to USARTn_RDR.RDR, and no RI interrupt is generated.

Receiver Interrupt

The UART Mode receiver supports two types of interrupts: receive data register full interrupt (RI) and error interrupt (EI).

- USARTn_CR1.RIE=1, when no receive error occurs and data is transferred from the receive shift register to the receive data register, an RI interrupt is generated.
- USARTn_CR1.RIE=1, when an overflow error, parity error, or frame error occurs during reception, an EI interrupt is generated.

23.3.2.6 UART Receive TIMEOUT Function

The TIMEOUT counter starts when the UART receive data stop bit is detected. If the next frame of receive data is not detected after the configured TIMEOUT period (set in units of receive bits), a TIMEOUT occurs. If USARTn_CR1.RE=1 at this time, the TIMEOUT status bit USARTn_SR.RTOF is set. If USARTn_CR1.RE=0, the USARTn_SR.RTOF bit will be set after USARTn_CR1.RE becomes 1.

TIMEOUT Function Setting Procedure

Step1. Set the USARTn_CR1 register to its reset value;

Step2. Configure the pins required for UART operation;

Step3. Select the clock source via the USARTn_CR2.CLKC bits (if the internal clock source is selected, set CR2.CLKC=0b01).

Step4. Configure the USARTn_CR1, USARTn_CR2, and USARTn_CR3 registers;

Step5. Set USARTn_PR to select the prescaler value, and configure the USARTn_BRR register for communication baud rate (no setting required when the clock source is an external clock source);

Step6. USARTn_CR1.RTOE=1. If interrupts are required, set USARTn_CR1.RTOIE=1.

Step7. Set USARTn_PR.RTOB to determine the TIMEOUT period;

Step8. Enable the receiver (USARTn_CR1.RE=1). If receive interrupt is required, set USARTn_CR1.RIE=1.

Step9. Upon detecting TIMEOUT, clear the USARTn_SR.RTOF bit by writing USARTn_CR1.CRTOF.

23.3.2.7 RX Line Wake-up Stop Mode Function

When the UART communication is idle, the system can enter stop mode to reduce current consumption. Without altering the UART PORT settings, UART Unit 1 can wake up the system from Stop mode via the RX line. The specific steps are as follows:

Step1. When UART communication is idle, set the USART_1_WUPI interrupt vector and enable the UART receive signal line wake-up stop mode function by setting the INTC_WKEN.RXWKEN bit.

Step2. The system enters stop mode;

Step3. When the system detects a falling edge on the RX line, it exits stop mode and disables this function in the USART_1_WUPI interrupt handler.

Please note that when the communication party needs to wake up the system, it should send a wake-up frame (recommended as 0x00). This data will not be received by UART and will not set the related flag. Additionally, the communication party must wait for the wake-up time required by the system stop mode before initiating UART communication data transmission.

UART RX line wake-up function can filter noise on the RX line. For details, refer to the USART1 Filter Control Register (USART1_NFC).

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23.3.2.8 UART Half-duplex Communication Mode

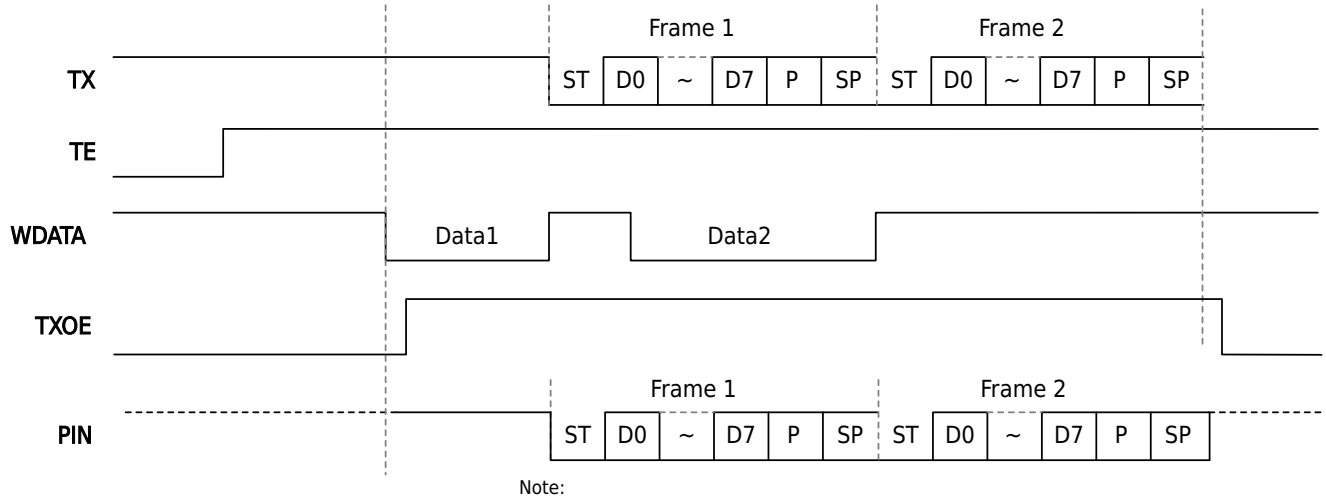
UART mode supports single-wire half-duplex operation. In UART mode, single-wire half-duplex mode is enabled by setting USARTn_CR3.HDSEL=1.

In single-wire half-duplex mode:

- The TX and RX lines are internally connected, and the RX pin is no longer used.
- When there is no data transmission and the TX function is disabled, the TX pin is in a released state. Therefore, when using the single-wire half-duplex mode, the TX line is pulled up to prevent floating input when no data is being transmitted.
- When there is no data transmission and the transmit function is enabled, the TX pin outputs a high level.

In addition, the half-duplex mode is similar to communication in normal UART mode. Please note that the transmission process will not be blocked by hardware. As long as data is written when USARTn_CR1.TE=1, the transmission will proceed. Therefore, conflicts on the line must be managed by software.

In half-duplex communication, to prevent the UART from receiving its own transmitted data, it is recommended to set USARTn_CR1.RE=0.



Note:
WDATA is the internal signal corresponding to USARTn_SR.TXE.
TXOE is the GPIO output enable signal. When it is 0, it means that the transmission is invalid.
PIN is GPIO output data signal.
TX is the transmit port signal of the USART module.

Figure 23-8 Half-Duplex Operation Timing

23.3.2.9 RS485 Driver Enable Function

UART mode supports Driver Enable mode, sharing the output signal with RTS. First configure USARTn_CR3.DEM to 1, then set USARTn_CR3.RTSE to 1.

By setting the USARTn_CR3.DEM to enable the driver function, users can activate external transceiver control through the DE (Driver Enable) signal. The assertion time programmed by the USARTn_CR3.DEA is the time between DE signal activation and the start of the START bit.

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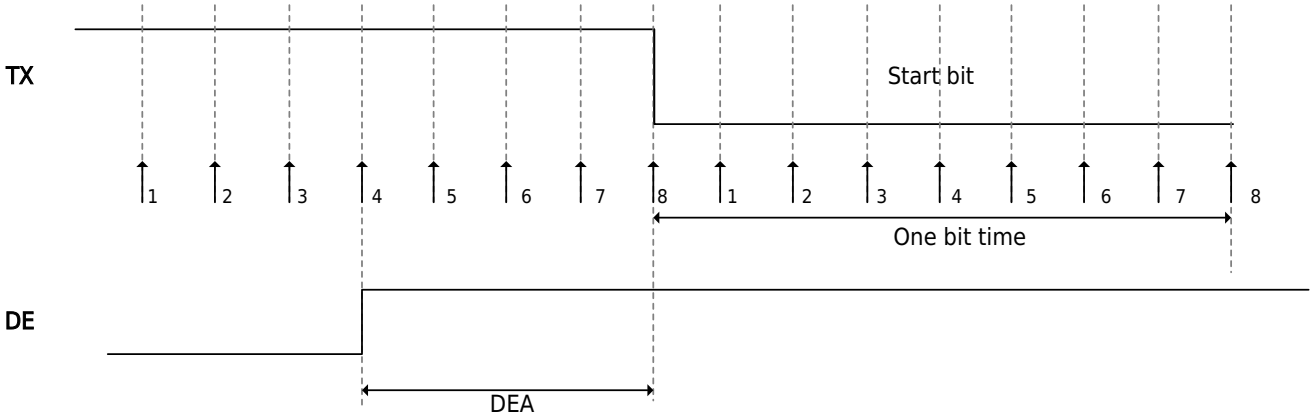

Figure 23-9 OVER8=1 DE Asserted

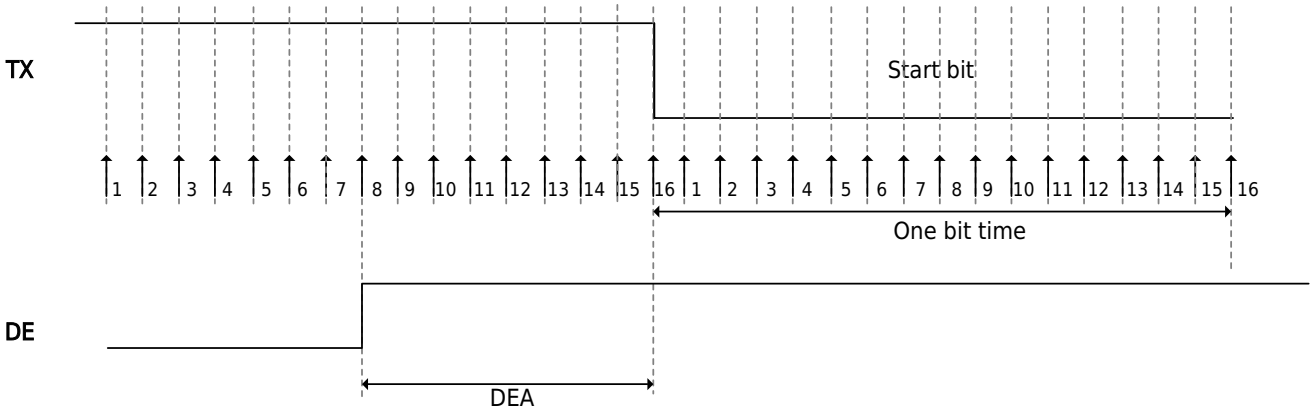

Figure 23-10 OVER8=0 DE Asserted

The de-assertion time programmed by the USARTn_CR3.DED is the duration between the end of the last stop bit and the DE signal deactivation. The polarity of the DE signal can be configured using the USARTn_CR3.DEP.

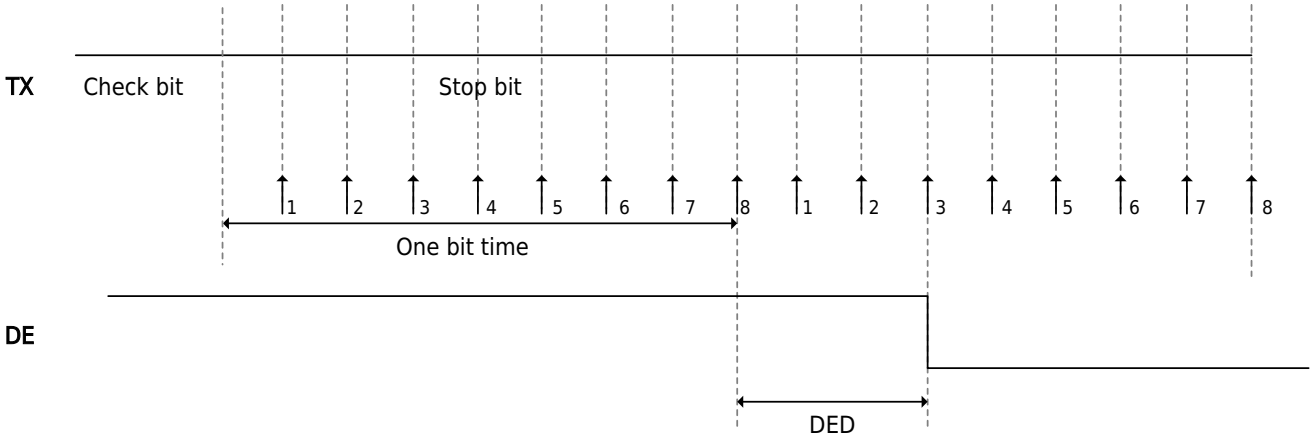

Figure 23-11 OVER8=1 DE De-assertion

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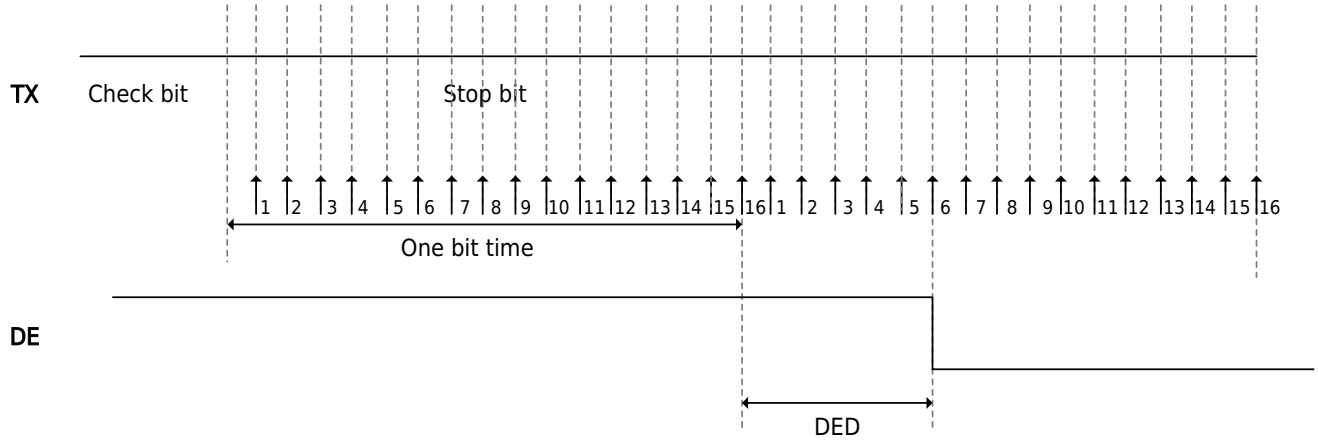

Figure 23-12 OVER8=0 DE De-assertion

23.3.2.10 Interrupt and Events

Table 23-4 UART Interrupt/Event Table

Function Name	Enable Bit (Interrupt only)	Flag Bit	Used as Event Source
Receive Error Interrupt	RIE	ORE, FE, PE	Enable
Receive Data Register Full Interrupt	RIE	RXNE	Enable
Transmit Data Register Empty Interrupt	TXEIE	TXE	Enable
Transmit Completion Interrupt	TCIE	TC	Enable
Transmit Completion Interrupt	TENDIE	TEND	Enable
TIMEOUT Interrupt	RTOIE	RTOF	Enable
RX Line Wake-up Stop Mode Interrupt	INTC_WKEN.RXWKEN	-	Disable

23.3.3 Multiprocessor Communication

23.3.3.1 Function Introduction

Multiprocessor communication mode refers to a communication method where multiple processors share a common communication line. The processors are divided into Transmit Stations and Receive Stations, with each Receive Station having its own unique ID. The types of data transmitted by the Transmit Station include Receive Station ID and communication data. By adding the MPB bit in the Data Format, it distinguishes whether the current transmission is the Receive Station ID or communication data. When the MPB bit is 0, the current frame contains communication data; when the MPB bit is 1, the current frame carries the Receive Station ID. All Receive Stations can receive the ID sent by the Transmit Station and compare it with their own ID. If they match, the Receive Data is accepted; otherwise, the station enters Silent Mode (neither receiving data nor setting related Receive Flags) until the next ID is received.

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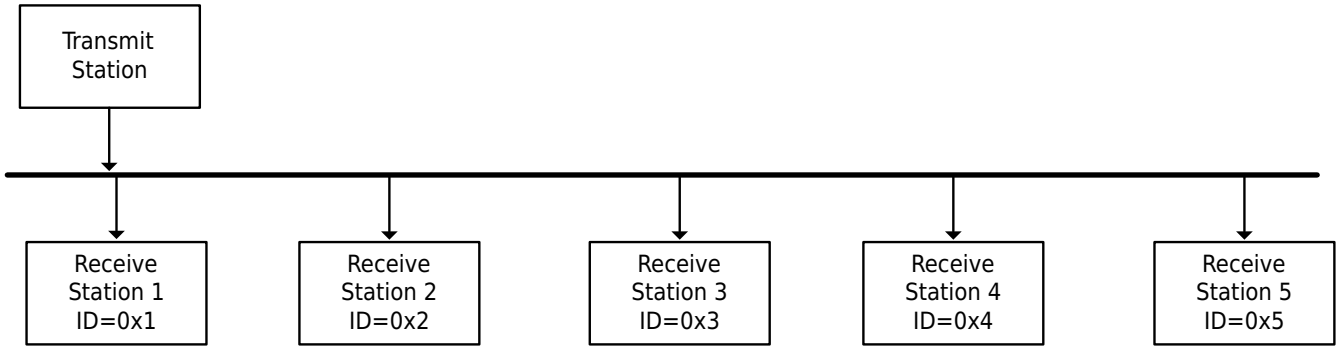

Figure 23-13 Multiprocessor Communication Legend

23.3.3.2 Data Format

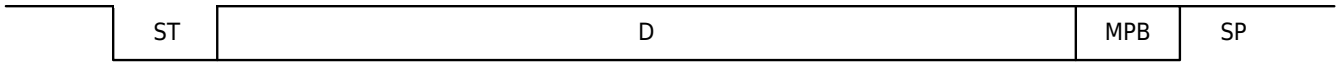

Figure 23-14 Multiprocessor Mode Data Format

- **Start Bit (ST) :** The start bit is always composed of one bit at low level.
- **Data Bit (D) :** The data bit can be configured as 8-bit or 9-bit.
- **Multiprocessor Bit (MPB) :** The multiprocessor bit can be configured to transmit communication data or send IDs.
- **Stop Bit (SP) :** The stop bit is fixed at high level and can be configured as 1 bit or 2 bits.

23.3.3.3 Action Description

In multiprocessor mode, the check bit has no effect, and the multiprocessor bit is added. Other functions such as clock and interrupt remain the same as in UART Mode.

Transmit Station Action

Step1. Set the USARTn_CR1 register to its reset value;

Step2. Set the required pins to be used;

Step3. Select the clock source via the USARTn_CR2.CLKC bit;

Step4. Configure the USARTn_CR1, USARTn_CR2, and USARTn_CR3 Registers;

Step5. Set USARTn_PR to select the prescaler value, and configure the USARTn_BRR register for communication baud rate (no setting required when the clock source is an external clock source);

Step6. Enable the transmitter (USARTn_CR1.TE=1). If the transmit data register empty interrupt is required, set USARTn_CR1.TXEIE=1.

Step7. Wait for the transmit data register to be empty, set USARTn_TDR.MPID bit to 1 (Transmit ID), write the ID value to USARTn_TDR, and transmit the ID.

Note

When the CTS function is enabled, data is transferred to the transmit shift register and transmission starts when the USARTn_CTS input is at low level.

Step8. Set USARTn_TDR.MPID bit to 0 (transmit data), write data to USARTn_TDR to transmit data;

Note

When the CTS function is enabled, data is transferred to the transmit shift register and transmission starts when the USARTn_CTS input is at low level.

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Step9. If continuous data transmission is required, repeat step 8. If the ID needs to be changed before transmitting data, repeat steps 7 and 8.

Step10. Check whether the transmission is complete by verifying the USARTn_SR.TC bit. For continuous data transmission using transmit interrupts, the last data can be written via the TI interrupt by setting USARTn_CR1.TXEIE to 0 and USARTn_CR1.TCIE to 1. A transmit completion interrupt will be generated after the last frame transmission ends.

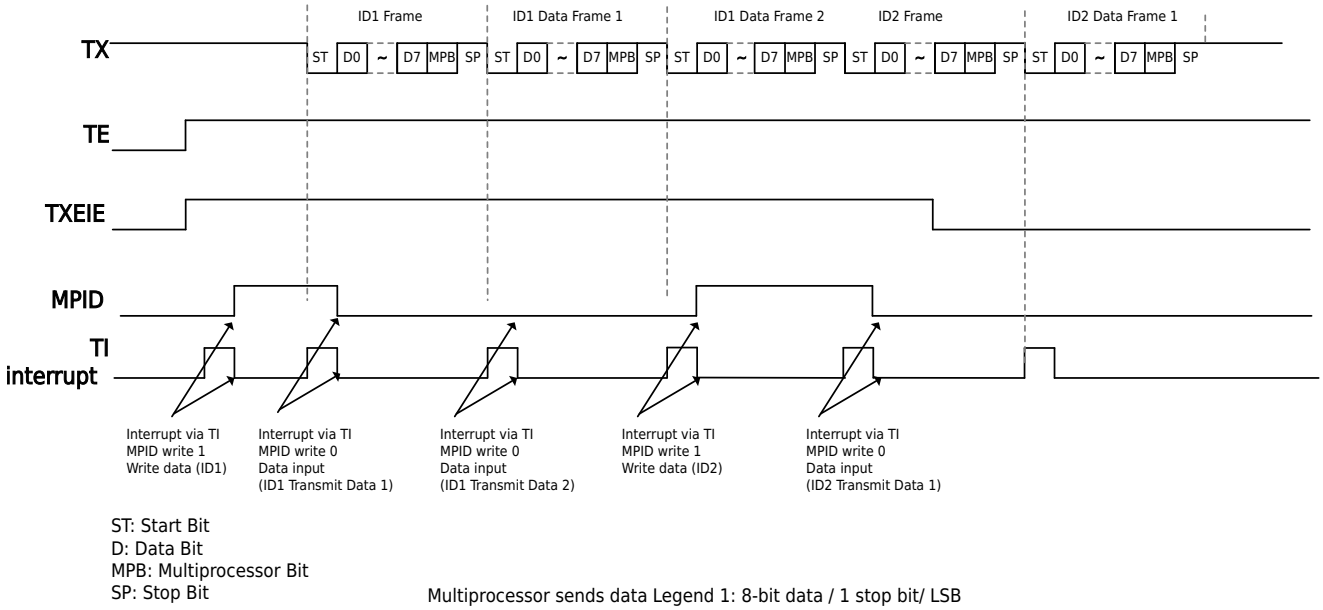

Figure 23-15 Multiprocessor Mode Transmit Data Diagram

Receive Station Action

In multiprocessor mode, the receive station must ensure it receives every ID data and compares it with its own ID. If they match, it receives the data; otherwise, it enters silent mode (neither receiving data nor setting receive-related flags) until the next ID data is received. This function is implemented via the USARTn_CR1.SLME bit.

When USARTn_CR1.SLME=0, receive data normally.

When USARTn_CR1.SLME=1, unless data with the MPB bit set to 1 (ID) is received, receive data is disabled, no RI interrupt occurs, and error flags FE and ORE are not set. When data with the MPB bit set to 1 (ID) is received, the USARTn_CR1.SLME bit is automatically cleared, enabling normal receive data and interrupt generation.

Action steps:

Step1. Set the USARTn_CR1 register to its reset value;

Step2. Set the required pins to be used;

Step3. Select the clock source via the USARTn_CR1.CLKC bit;

Step4. Configure the USARTn_CR1, USARTn_CR2, and USARTn_CR3 Registers;

Step5. Set USARTn_PR to select the prescaler value, and configure the USARTn_BRR register for communication baud rate (no setting required when the clock source is an external clock source);

Step6. USARTn_CR1.RE=1, USARTn_CR1.SLME=1 (waiting to receive ID). If using receive interrupt, set USARTn_CR1.RIE=1.

Step7. When the start bit is detected, the receiver loads the data into the receive shift register and checks the USARTn_SR.MPB bit.

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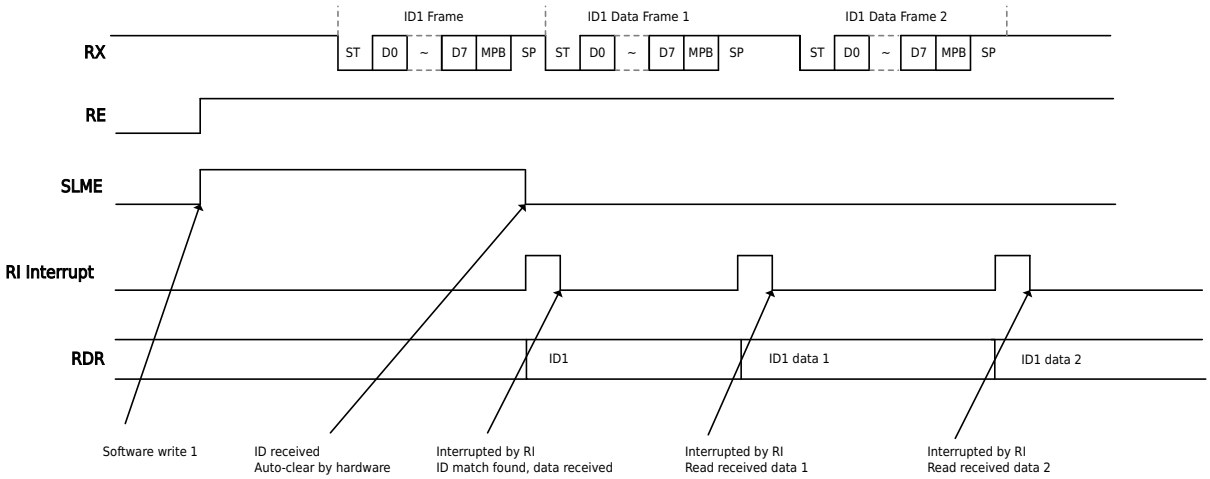
Step8. If USARTn_SR.MPB=1, the USARTn_CR1.SLME bit is automatically cleared, Receive Data normally, and the software compares the received ID with its own ID.

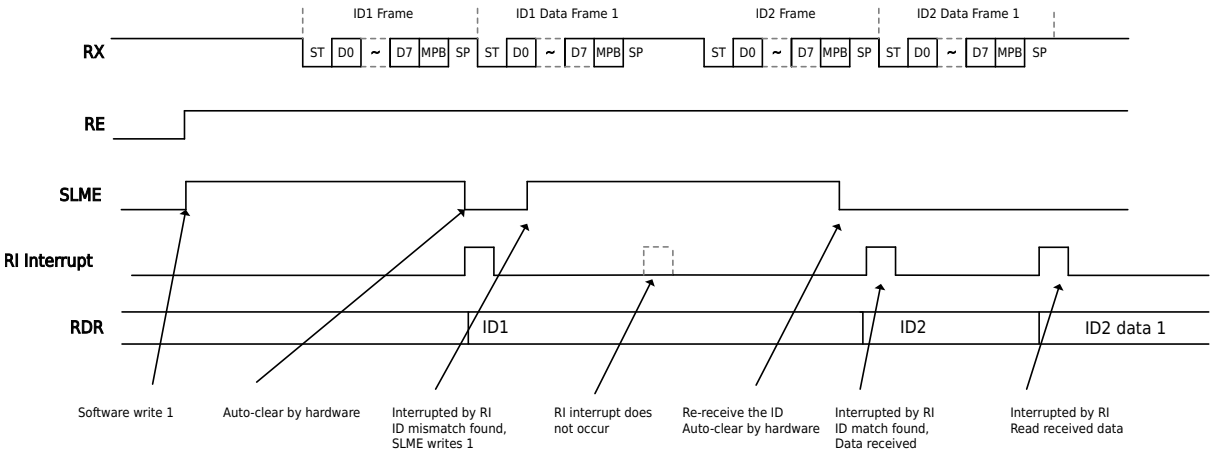
- If the ID matches, receive data normally, an interrupt occurs, and error detection is performed, which is the same as UART receive data.
- If the ID does not match, the software writes the USARTn_CR1.SLME bit to 1 again and repeats step 8.



ST: Start Bit
D: Data Bit
MPB: Multiprocessor Bit
SP: Stop Bit

Multiprocessor Data Receive Example 1: 8-bit data / 1 stop bit / LSB / ID match.

Figure 23-16 Multiprocessor Mode Receive Data Diagram 1



ST: Start Bit
D: Data Bit
MPB: Multiprocessor Bit
SP: Stop Bit

Multiprocessor Data Receive Example 2: 8-bit data / 1 stop bit / LSB / ID mismatch

Figure 23-17 Multiprocessor Mode Receive Data Diagram 2

23.3.3.4 Interrupt and Events

In multiprocessor mode, the interrupt handling is identical to UART mode except for the absence of parity errors.

Table 23-5 Multiprocessor Mode Interrupt/Event Table

Function Name	Enable Bit (Interrupt only)	Flag	Used as Event Source
Receive Error Interrupt	RIE	ORE, FE	Enable
Receive Data Register Full Interrupt	RIE	RXNE	Enable

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Function Name	Enable Bit (Interrupt only)	Flag	Used as Event Source
Transmit Data Register Empty Interrupt	TXEIE	TXE	Enable
Transmit Completion Interrupt	TCIE	TC	Enable
Transmit Completion Interrupt	TENDIE	TEND	Enable

23.3.4 UART-LIN

23.3.4.1 Function Introduction

LIN stands for Local Interconnect Network, a low-speed (1-20kbps) serial communication protocol designed to reduce automotive network costs.

23.3.4.2 LIN Data Format

A LIN frame consists of start bit + 8-bit data + 1 stop bit, with data transmitted and received in LSB format. The data behavior on the LIN Bus is as shown in the following figure.

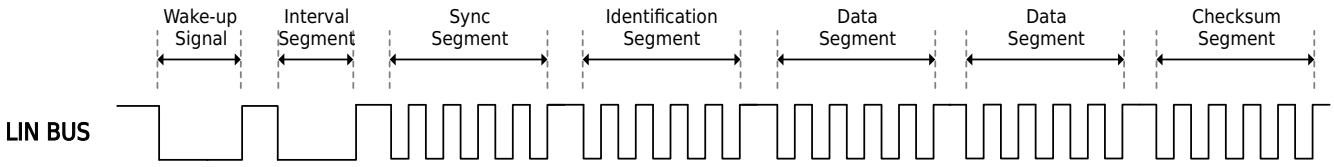

Figure 23-18 LIN Bus Data Behavior

23.3.4.3 LIN Transmit

Wake-up Signal Frame Transmit

Transmit the corresponding signal frame by transmitting data 0x80.

Interval Segment Transmit

The synchronous interval segment indicates the start of a frame. This product supports hardware transmission of the LIN interval segment.

The width of the low level in the LIN interval segment is determined by the USARTn_CR2.SBK register setting.

After the transmission of the wake-up frame is completed, the transmission of the interval segment will proceed.

- When USARTn_CR2.SBKM=0, writing 1 to USARTn_CR2.SBK will cause the hardware to automatically send out the interval segment.
- When USARTn_CR2.SBKM=1, after writing 1 to USARTn_CR2.SBK, writing data 0x00 to the transmit data register USARTn_TDR.TDR starts transmitting the interval segment.

After the interval segment transmission is completed, USARTn_CR2.SBK is automatically cleared.

Synchronization Segment Transmit

Transmit data 0x55 to achieve the transmission of the synchronization segment.

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Bus Error Detection

When USARTn_CR2.BEE=1, the USARTn_SR.BE flag is set if the hardware detects a mismatch between the data on the bus and the transmitted data. When USARTn_CR2.BEIE=1, the corresponding interrupt is generated.

23.3.4.4 LIN Receive

Wake-up Signal Frame Detection

When USARTn_CR2.WKUPE=1, the hardware automatically detects the wake-up signal. Upon detecting a low-level width on the RX line greater than or equal to 2.5 bit data widths (130μs at 19.2kbps), the USARTn_SR.WKUP flag is set. When USARTn_CR2.WKUPIE=1, the corresponding interrupt is generated. Upon detecting a wake-up signal frame, clear the USARTn_SR.WKUP flag and read the USARTn_RDR.RDR register.

The USARTn_CR2.WKUPE register should be set to 1 only when the system needs to wait for a wake-up signal; otherwise, it must be set to 0.

Synchronous Interval Segment Detection

This product supports hardware-based synchronous interval segment detection. When the low-level width on the communication line is greater than or equal to the value set in the USARTn_CR2.LBDL register and a break delimiter is detected, the USARTn_SR.LBD flag is set. When USARTn_CR2.LBDIE=1, the corresponding interrupt is generated.

Note that during synchronous interval segment detection, the USARTn_SR.FE flag will be set. While clearing the USARTn_SR.LBD flag, the USARTn_SR.FE flag must also be cleared, and the USARTn_RDR.RDR register should be read (the read value is 0x00).

Synchronization Segment Detection and Baud Rate Measurement

Upon detecting the interval segment, the hardware automatically measures the frequency of the synchronization segment. The clock for measuring the counter is set by the USARTn_PR.LBMPSC bit. The counter value is stored in the USARTn_LBMC register. The baud rate of the master node can be obtained by dividing the selected counter clock frequency by the value in the USARTn_LBMC register.

After the USARTn_LBMC register update is completed, the USARTn_SR.LBM flag bit will be set. When USARTn_CR2.LBMIE=1, the corresponding interrupt is generated.

Note that during synchronization segment detection, the USARTn_SR.FE flag may be set. When clearing the USARTn_SR.LBM flag, the USARTn_SR.FE flag also needs to be cleared; reading the USARTn_LBMC register must be performed after the synchronization segment reception is completed.

Do not enable the digital filter function during synchronization segment detection.

Receive Data Setting Procedure

Step1. Set the USARTn_CR1 register to its reset value;

Step2. Configure the pins required for UART operation;

Step3. Select the clock source via the USARTn_CR2.CLKC bit;

Step4. Configure the USARTn_CR1 (RE=1, RIE=0), USARTn_CR2, and USARTn_CR3 registers.

Step5. (Optional) wake-up signal frame detection:

a. Set USARTn_CR2.WKUPE=1 and wait for the wake-up signal;

b. Wake-up signal detected, USARTn_CR2.WKUPE=0, waiting for synchronization segment interval segment.

Step6. (Optional) synchronization segment interval field detection:

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a. Upon detecting the synchronous interval segment, clear the USARTn_SR.FE/LBD flag and verify that the received data is 0x00.

Step7. (Optional) Synchronization segment frequency measurement and communication baud rate calculation:

a. After completing the synchronization segment reception, read the USARTn_LBMC register to calculate the baud rate;
b. Clear the RE and TE bits in USARTn_CR1, and configure the correct baud rate via the USARTn_BRR and USARTn_PR registers;
c. Set USARTn_CR1.RE bit again;
d. Clear the USARTn_SR.FE/LBM flag and read the RDR register to enable normal data reception later;
e. If receive interrupts are required for later data reception, set USARTn_CR1.RIE=1.

Step8. Receive identification segment (process is the same as UART receive data process);

Step9. Receive Data (process is the same as UART receive data process);

Step10. Receive checksum (process is the same as UART receive data process).

23.3.4.5 Interrupt and Events

Table 23-6 LIN Interrupt/Event Table

Function Name	Enable Bit (Interrupt only)	Flag Bit	Used as Event Source
Error Interrupt	RIE	ORE, FE	Enable
	BEIE	BE	Enable
Wake-up Signal/Interval Segment/Synchronization Segment Detection Interrupt	WKUPIE	WKUP	Enable
	LBDIE	LBD	Enable
	LBMIE	LBM	Enable
Receive Data Register Full Interrupt	RIE	RXNE	Enable
Transmit Data Register Empty Interrupt	TXEIE	TXE	Enable
Transmit Completion Interrupt	TCIE	TC	Enable
Transmit Completion Interrupt	TENDIE	TEND	Enable

23.3.5 Smart Card

23.3.5.1 Connection Schematic Diagram

Supports the smart card communication protocol specified in ISO/IEC 7816-3. The figure below shows the connection schematic diagram for smart card mode.

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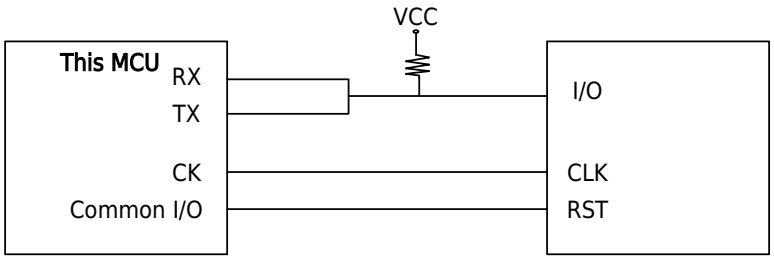

Figure 23-19 Smart Card Connection Schematic Diagram

23.3.5.2 Clock

Internal Clock Source

In smart card mode, only the clock generated by the internal baud rate generator can be used as the clock source.

The basic number of clock periods for 1-bit data transmission is determined by the USARTn_CR3.BCN setting.

The clock output in smart card mode is controlled by setting the USARTn_CR2.CLKC bit in the register.

Maximum Baud Rate

When the internal clock source is selected, the baud rate generated by the internal baud rate generator is calculated using the following formula:

$$B = \frac{C}{2 \times BCN \times (DIV_Integer+1)}$$

Where:

- B: Baud rate, unit: Mbps
- C: When USARTn_PR.ULBREN is 0, the clock set by USARTn_PR.PSC bit (PCLK1, PCLK1/4, PCLK1/16, PCLK1/64), unit: MHz

  When USARTn_PR.ULBREN is 1, the clock set by USARTn_PR.PSC bit (PCLK1/128, PCLK1/256, PCLK1/512, PCLK1/1024), unit: MHz
- DIV_Integer: USARTn_BRR.DIV_Integer setting value
- BCN: USARTn_CR3.BCN register setting value

When C is PCLK1, DIV_Integer=0, and BCN=0, the baud rate reaches the maximum baud rate of PCLK1/64 (Mbps).

Sampling and Reception Tolerance

Upon detecting the falling edge of RX, the USART synchronizes the receive data with the internal basic clock to initiate data reception. The receive data will be sampled at the center of the data.

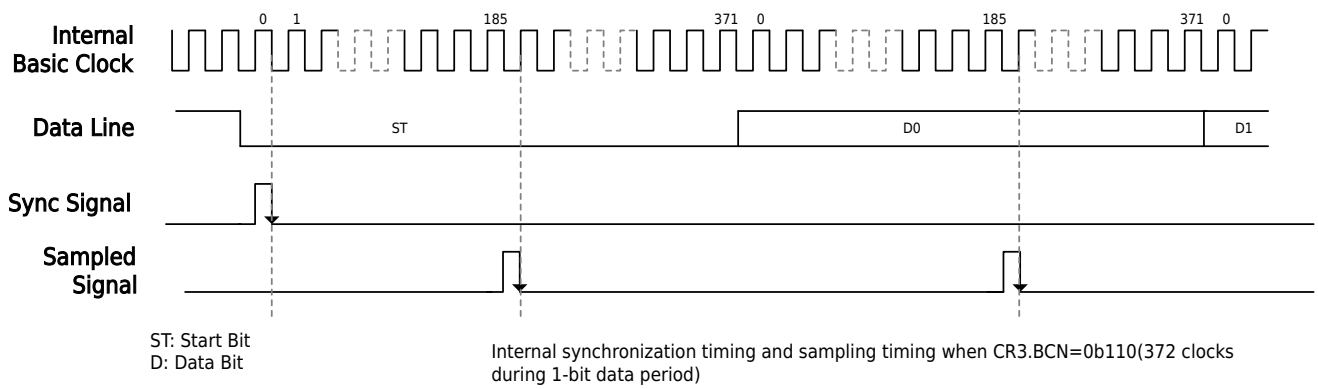

Figure 23-20 Smart Card Mode Synchronization Timing and Sample Timing Diagram

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Receive tolerance calculation formula:

$$RM = \{0.5 \times (1 - \frac{1}{BCN}) - 9.5CFD\} \times 100\%$$

Where:

- RM: Reception Margin
- BCN: Number of clocks required for 1 bit of data transmission (set by USARTn_CR3.BCN)
- CFD: Clock Frequency Deviation

23.3.5.3 Data Format

In smart card mode, a frame of data consists of start bit, data bit and check bit.

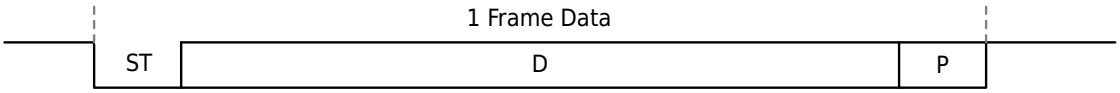

Figure 23-21 Smart Card Mode Data Format

- **Start Bit (ST) :** The start bit is always composed of one bit at low level.
- **Data Bit (D) :** The data bit is fixed as 8-bit data.
- **Check Bit (P) :** The check bit must be configured as 1-bit even parity.

23.3.5.4 Initialization Setup Procedure for Smart Cards

Step1. Configure the USARTn_CR1 register to the reset value;

Step2. Configure the required pins to be used;

Step3. Status register confirmed, USARTn_SR register setting is reset to default value;

Step4. Configure the USARTn_CR1, USARTn_CR2, and USARTn_CR3 Registers;

Step5. Set USARTn_PR to select the prescaler value, and configure the USARTn_BRR register for the communication baud rate.

Step6. USARTn_CR2.CLKC bits configure clock control;

Step7. Configuration of USARTn_CR1 register (TE, RE, RIE, TXEIE bits) : Except for self-test, do not simultaneously set both TE and RE to 1.

When switching from transmit mode to receive mode, or from receive mode to transmit mode, steps 1 to 7 above must be reconfigured.

23.3.5.5 Smart Card Mode Action Description

In smart card mode, the flag bit for the TI interrupt (transmit data empty interrupt) is the USARTn_SR.TC bit. A TI interrupt is generated when USARTn_SR.TC=1 and USARTn_CR1.TXEIE=1.

Function Overview

During data transmission, there must be a protection time of at least 2etu (Elementary Time Unit) between two frames (from the end of the check bit to the start of the next frame's start bit).

If an error signal from the receiver is detected during data transmission, the data will be automatically retransmitted after 2etu.

When a parity error occurs in the received data, a low-level error signal is transmitted for 1etu. The error signal is sent with a timing of 10.5 etu after the start of reception.

Transmission Instructions

After a frame of data is transmitted, if an error signal from the receiver is detected, USARTn_SR.FE is set to 1 (an error interrupt occurs if USARTn_CR1.RIE=1). The USARTn_SR.TC flag is not set, and the data is auto retransmitted. The USARTn_SR.FE bit must be cleared before receiving the next frame's check bit.

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After a frame of data is transmitted without errors, the USARTn_SR.TC flag is set, and a TI interrupt occurs when USARTn_CR1.TXEIE=1. Writing the data again enables continuous data transmission.

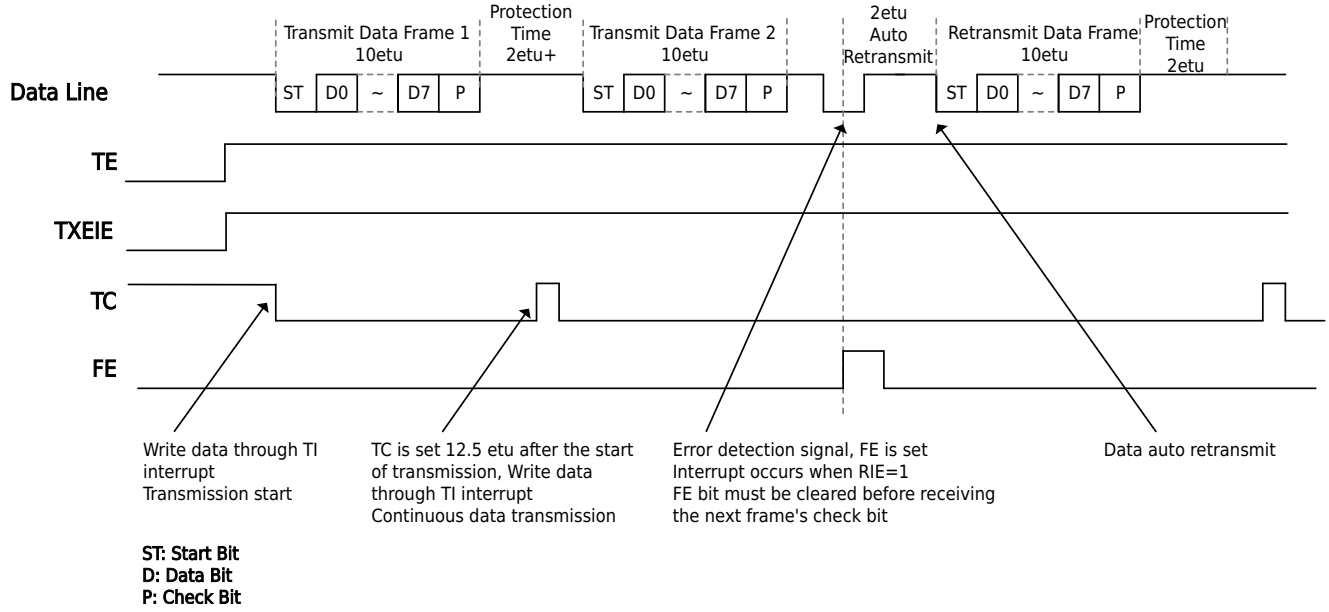

Figure 23-22 Smart Card Mode Transmit Data Diagram

Receive Instructions

When receiving data, if a parity error is detected, USARTn_SR.PE is set. When interrupt enable is active, an EI interrupt occurs. The USARTn_SR.PE bit must be cleared before receiving the next frame's check bit.

When a parity error occurs, a low level of 1etu is transmitted as the error signal, requesting the sender to retransmit the data.

Normal receive data, the received data can be read via RI Interrupt, continuous reception.

Detect overflow error when receiving data.

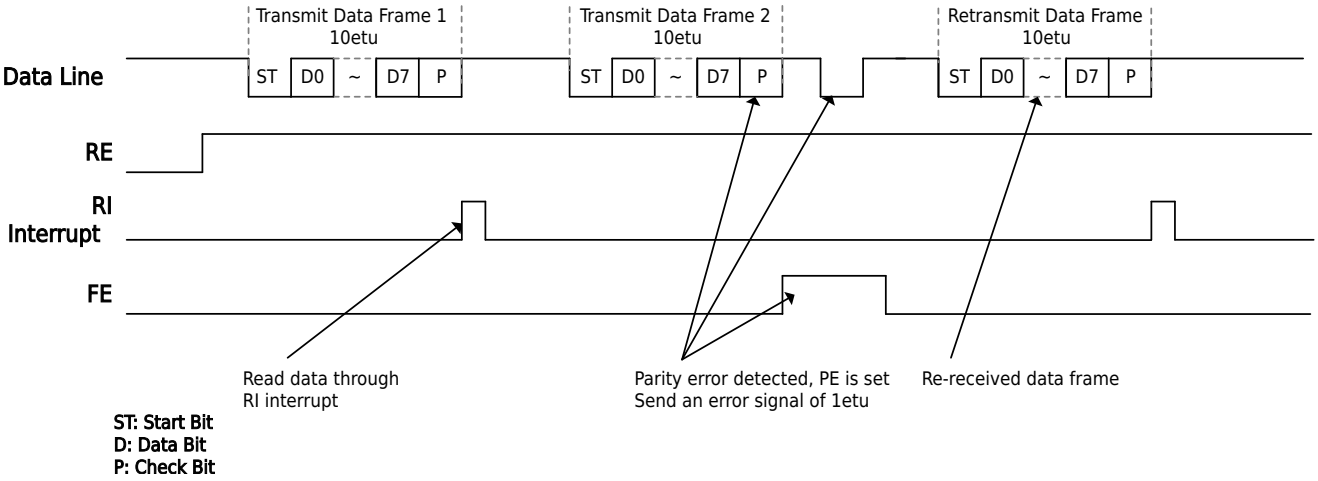

Figure 23-23 Smart Card Mode Receive Data Diagram

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23.3.5.6 Interrupt and Events

Table 23-7 Smart Card Mode Interrupt/Event Table

Function Name	Enable Bit (Interrupt only)	Flag Bit	Used as Event Source
Error Interrupt	RIE	ORE, PE, FE	Enable
Receive Data Full Interrupt	RIE	RXNE	Enable
Transmit Data Empty Interrupt	TXEIE	TC	Enable

23.3.6 Clock Synchronization Mode

23.3.6.1 Clock

The clock synchronization mode can select either the clock generated by the internal baud rate generator (internal clock source) or the clock input from the USARTn_CK pin (external clock source) as the communication clock source.

Internal Clock Source

The synchronization clock is output from the USARTn_CK pin. A frame of data outputs 8 clock pulses. When neither transmitting nor receiving data, the clock output remains fixed at high level.

External Clock Source

The external clock source inputs the clock from the USARTn_CK pin as the communication clock.

Maximum Baud Rate

When the internal clock source is selected, the baud rate generated by the internal baud rate generator is calculated using the following formula:

$$B = \frac{C}{4 \times (DIV_Integer+1)}$$

Where:

- B: Baud rate, unit: Mbps
- C: When USARTn_PR.ULBREN is 0, the clock set by USARTn_PR.PSC bit (PCLK1, PCLK1/4, PCLK1/16, PCLK1/64), unit: MHz

  When USARTn_PR.ULBREN is 1, the clock set by USARTn_PR.PSC bit (PCLK1/128, PCLK1/256, PCLK1/512, PCLK1/1024), unit: MHz
- DIV_Integer: USARTn_BRR.DIV_Integer setting value

When the internal clock source is selected and C is PCLK1 with DIV_Integer=1, the maximum baud rate is PCLK1/8 (Mbps).

Notice

In synchronous mode, setting DIV_Integer to 0 is prohibited.

When using an external clock source, the maximum frequency requirement for the external input clock is PCLK1/6 (MHz), so the maximum baud rate is PCLK1/6 (Mbps).

Please note that in synchronous mode, the maximum communication baud rate is not only determined by the PCLK1-based calculation method described above but also needs to refer to the maximum communication baud rate specified in the "Electrical Specifications" chapter of the Datasheet.

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23.3.6.2 Data Format

In clock synchronization mode, each frame of data consists of a fixed 8 bits. The transmission and reception of one frame requires 8 synchronization clock pulses. During data transmission, data is sent on the falling edge of the synchronization clock. During data reception, data is sampled on the rising edge of the synchronization clock.

The synchronization clock remains fixed at high level when there is no data transmission. After the last bit is transmitted, the communication line maintains the value of the last bit.

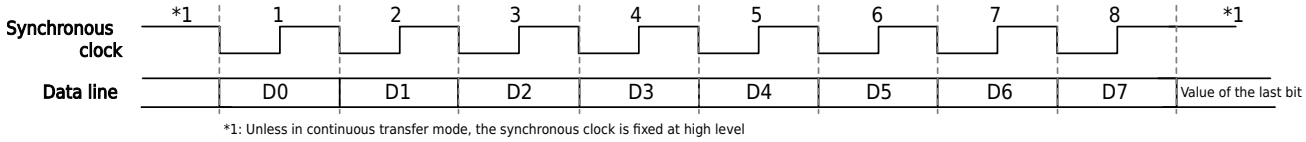

Figure 23-24 Clock Synchronization Mode Data Format

23.3.6.3 Modem Operation

Modem operations include the CTS function and RTS function. When USARTn_CR3.RTSE=1, the RTS function is enabled. When USARTn_CR3.CTSE=1, the CTS function is enabled.

CTS Function

The CTS function controls data transmission via the input of the USARTn_CTS pin. Data can only be transmitted when the USARTn_CTS pin input is at low level. If the USARTn_CTS input transitions to high level during transmission, the ongoing data transmission is unaffected.

RTS Function

The RTS function outputs a low level through the USARTn_RTS pin to request the peer to transmit data.

The USARTn_RTS pin outputs a low level when all of the following conditions are met:

- Receive enable (USARTn_CR1.RE=1) and not currently receiving data
- There is no unread data in the USARTn_RDR.RDR register (when USARTn_CR1.RE=1)
- USARTn_TDR.TDR update completed (when USARTn_CR1.TE=1)
- No receiving errors

If all the above conditions cannot be met at the same time, USARTn_RTS outputs a high level.

23.3.6.4 Transmitter

When USARTn_CR1.TE bit is set to 1, the data in the transmit shift register is serially output at the USARTn_TX pin, and the corresponding clock pulse is output at the USARTn_CK pin.

The transmit data register USARTn_TDR.TDR and the internal transmit shift register form a double buffer structure, which can transmit data continuously.

When transmitting data via the transmit data register empty interrupt or DMA, to ensure transmission accuracy, only one data write is enabled per request.

Transmit Data Setting Procedure

Step1. Configure USARTn_CR1, USARTn_SR1 registers to reset values;

Step2. Configure the required pins to be used;

Step3. Select the clock source via the USARTn_CR2.CLKC bit;

Step4. Configure the USARTn_CR1, USARTn_CR2, and USARTn_CR3 registers;

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Step5. Set USARTn_PR to select the prescaler value, and configure the USARTn_BRR register for communication baud rate (no setting required when the clock source is an external clock source);

Step6. Enable the transmitter (USARTn_CR1.TE=1). If the transmit data register empty interrupt is required, set USARTn_CR1.TXEIE=1.

Step7. Wait for the transmit data register to be empty, write communication data to USARTn_TDR.TDR, data is transferred to the transmit shift register, transmission starts;

> **Note**
> When the CTS function is enabled, data is transferred to the transmit shift register and transmission starts when the USARTn_CTS input is at low level.

Step8. To continuously transmit data, repeat step 7;

Step9. Check whether the transmission is complete by verifying the USARTn_SR.TC bit. For continuous data transmission using transmit interrupts, the last data can be written via the TI interrupt by setting USARTn_CR1.TXEIE to 0 and USARTn_CR1.TCIE to 1. A transmit completion interrupt will be generated after the last frame transmission ends.

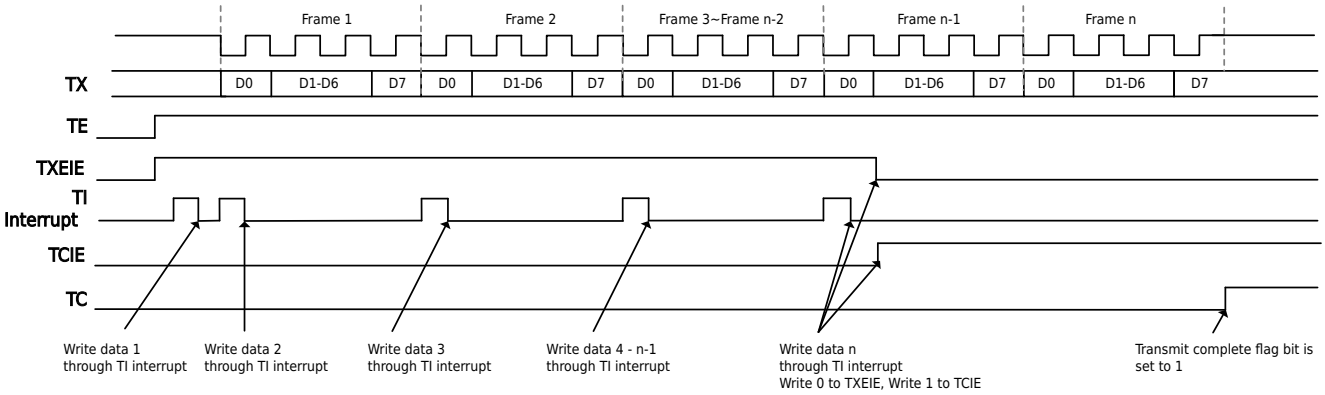

Figure 23-25 Data Transmission in Clock Synchronization Mode Diagram 1 (LSB/without CTS function)

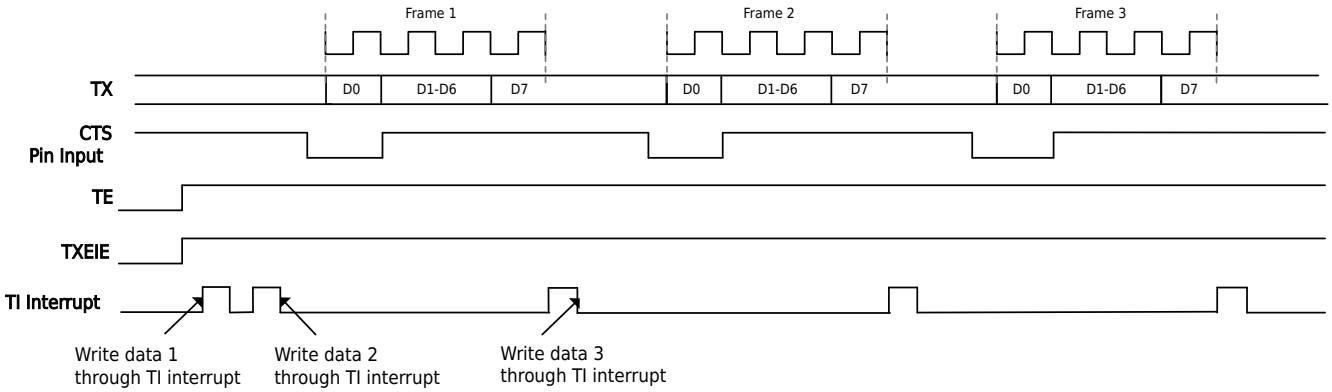

Figure 23-26 Data Transmission in Clock Synchronization Mode Diagram 2 (LSB/with CTS function)

Transmitter Interrupt

The clock synchronous mode transmitter supports two interrupts, the transmit data register empty interrupt TI and the transmit completion interrupt TCI.

- TXEIE=1, when the value of USARTn_TDR.TDR register is transferred to the transmit shift register, a TI interrupt is generated.
- TCIE=1, when the last bit of transmitted data is sent and the USARTn_TDR.TDR register is not updated, a TCI interrupt is generated.

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23.3.6.5 Receiver

Receive Data Setting Procedure

Step1. Configure USARTn_CR1, USARTn_SR registers to reset values;

Step2. Configure the required pins to be used;

Step3. Select the clock source via the USARTn_CR2.CLKC bit;

Step4. Configure the USARTn_CR1, USARTn_CR2, and USARTn_CR3 registers;

Step5. Set USARTn_PR to select the prescaler value, and configure the USARTn_BRR register for communication baud rate (no setting required when the clock source is an external clock source);

Step6. Enable the receiver (USARTn_CR1.RE=1). If receive interrupt is required, set USARTn_CR1.RIE=1.

> **Note**
> When using the RTS function, USARTn_RTS outputs a low level after RE=1.

Step7. Start receiving data in synchronization with the input synchronization clock or the internally generated synchronization clock, and receive data into the receive shift register.

- When an overflow error occurs, data is lost and the USARTn_SR.ORE flag is set;
- When no error occurs, the received data is transferred to the USARTn_RDR.RDR register, the USARTn_SR.RXNE flag is set, and the currently received data is read before the last bit of the next frame is received. Repeating step 7 can realize the continuous data reception function.

> **Note**
> When using the RTS function, USARTn_RTS outputs a low level after data is read.

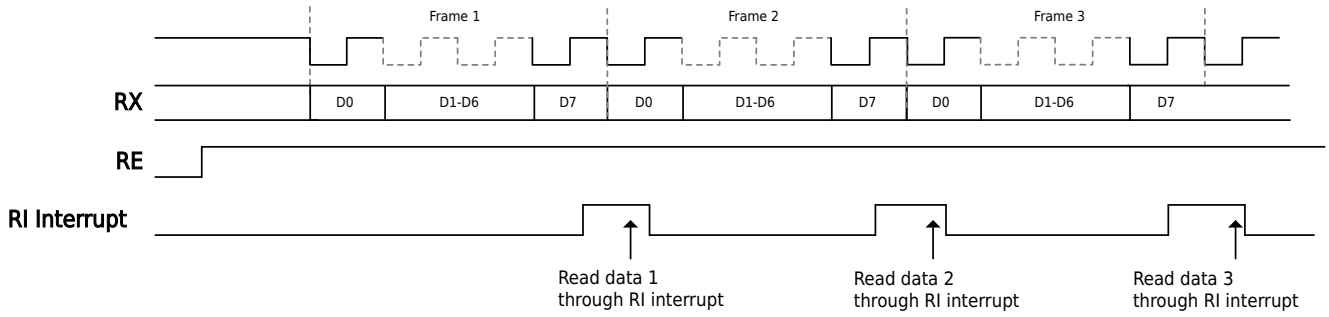

Figure 23-27 Data Reception in Clock Synchronization Mode Diagram 1 (LSB/without RTS function)

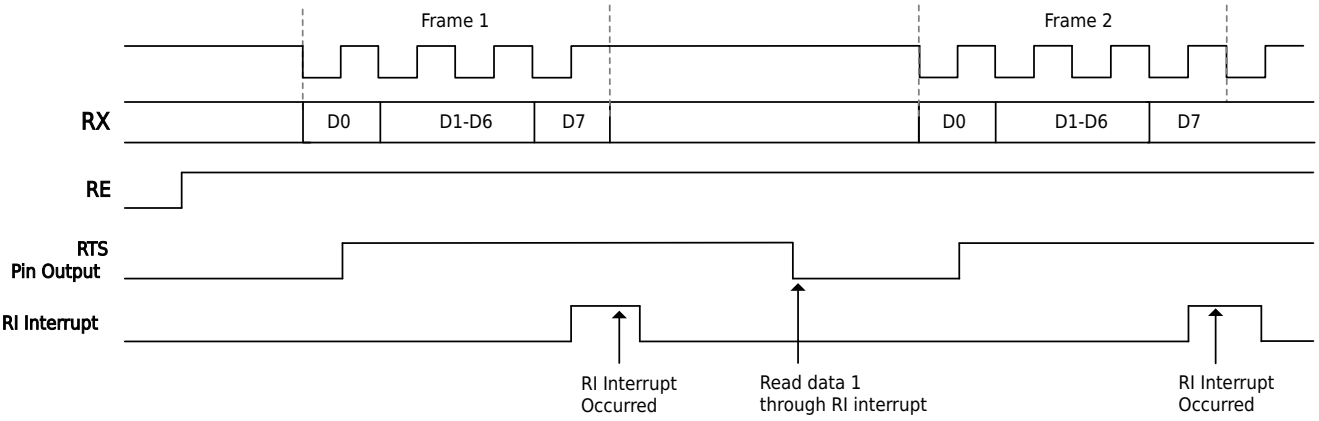

Figure 23-28 Data Reception in Clock Synchronization Mode Diagram 2 (LSB/with RTS function)

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Error Handling

When receiving data in clock synchronous mode, the reception error is an overflow error (USARTn_SR.ORE). When a reception error occurs, data transmission and reception are halted. Data transmission can be restarted by clearing the error flag, which is achieved by writing to the USARTn_CR1.CORE flag bit and performing a read operation on the USARTn_RDR.RDR register.

The condition for an overflow error is that new data is received without reading the USARTn_RDR.RDR value, so the data received in the previous frame should be read before the last bit of the current frame is received. When an overflow error occurs, the received data is lost and no RI interrupt is generated.

Receiver Interrupt

The clock synchronous mode receiver supports two interrupts, the receive data register full interrupt RI and the receive error interrupt EI.

- When RIE=1, when data is transferred from the receive shift register to the receive data register, an RI interrupt is generated.
- When RIE=1, when a receive error (such as an overflow error) occurs during reception, an EI interrupt is generated.

23.3.6.6 Simultaneous Transmission and Reception

The USART synchronous clock mode supports full-duplex operation, enabling simultaneous data transmission and reception. To perform simultaneous transmission and reception, a command must set RE, TE, RIE, and TXEIE to 1. Other configuration procedures are the same as those for the transmitter and receiver individually.

23.3.6.7 Interrupt and Events

Table 23-8 Interrupt/Event Table in Synchronous Clock Mode

Interrupt Name	Enable bit (Interrupt only)	Flag Bit	Used as Event Source
Receive Error Interrupt	RIE	ORE	Enable
Receive Data Register Full Interrupt	RIE	RXNE	Enable
Transmit Data Register Empty Interrupt	TXEIE	TXE	Enable
Transmit Completion Interrupt	TCIE	TC	Enable
Transmit Completion Interrupt	TENDIE	TEND	Enable

23.3.7 Digital Filter Function

When USARTn_CR1.NFE=1, the built-in digital filter function is enabled. The digital filter is only active in UART mode and can remove noise on the receive data line RX.

The built-in digital filter can filter out noise with a width less than 3/16 (USARTn_CR1.OVER8=0) or 3/8 width (USARTn_CR1.OVER8=1) of 1 bit.

When the fractional baud rate function is enabled (USARTn_CR1.FBME=1), the actual filtering capability should account for clock frequency errors introduced by fractional division. Refer to Table 23-21 : Baud Rate Calculation Formula (Fractional Baud Rate is Enable where FBME=1) for error calculation methods.

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When operating in LIN mode, enable the digital filtering function after the synchronization frame.

If the digital filter's clock stops and then starts again, the digital filter resumes operation from the state maintained when the clock stopped.

When USARTn_CR.TE=0 and USARTn_CR.RE=0, the Flip-Flop state inside the digital filter is reset to 1.

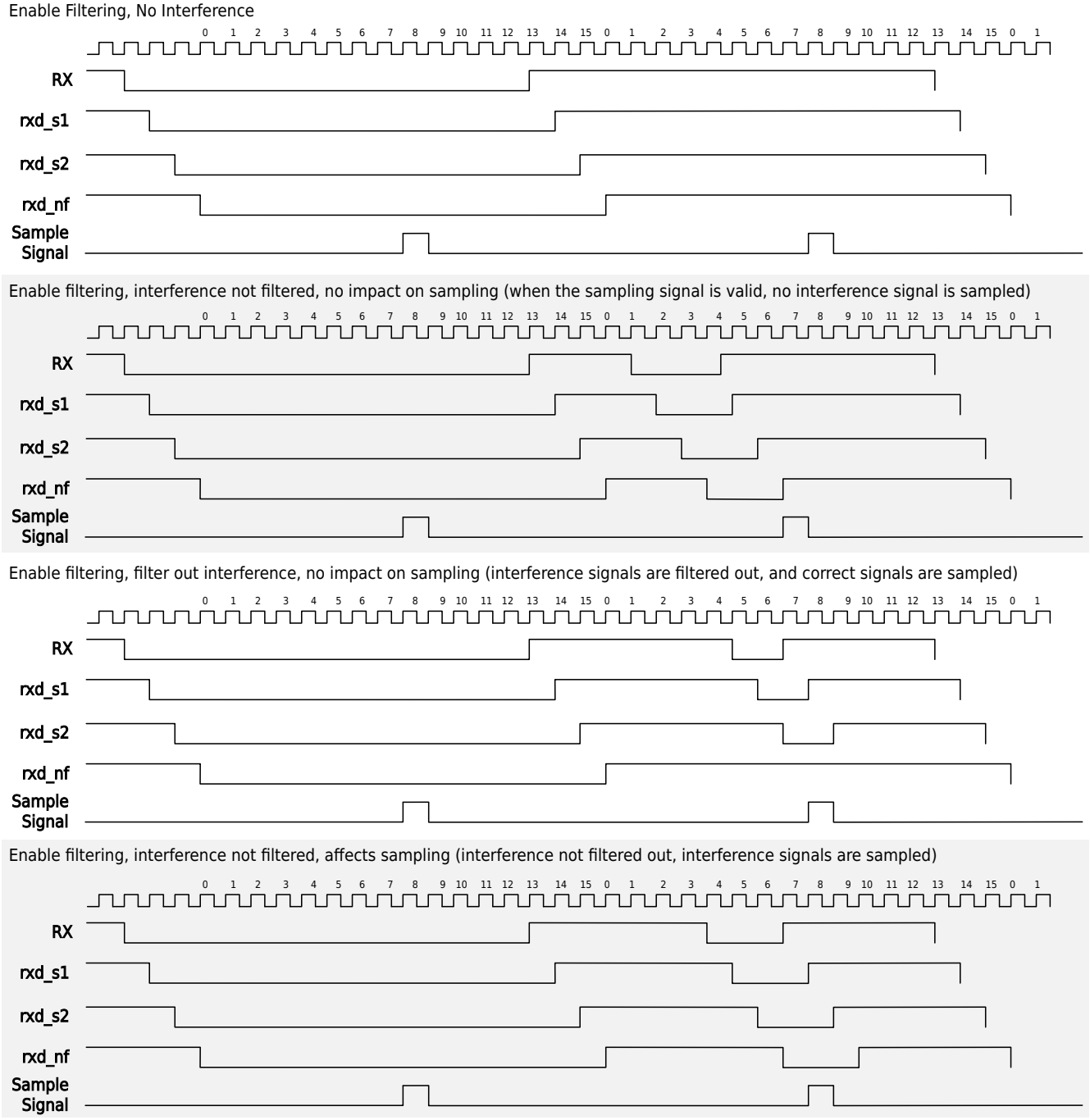

Figure 23-29 Digital Filter Function Diagram

- rxd_s1: internal signal RX delayed by 1 sampling clock
- rxd_s2: internal signal RX delayed by 2 sampling clocks
- rxd_nf: the actual sampled signal, determined by comparing the input signal RX, rxd_s1, and rxd_s2.

Enabling the NF (Noise Filter) function performs two delayed operations on the input RX signal, generating three signals in total. Only when the input signal matches both delayed signals can the internal module perform signal toggling.

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23.3.8 Interrupt

Table 23-9 USART Global Interrupt Summary Table

Interrupt Name	Symbol	Description
Error Interrupt	USART_n_EI n=1-4	UART/Multiprocessor/Smart Card/Clock Synchronization Mode Receive Error Interrupt LIN Error interrupt
Receive Data Register Full Interrupt	USART_n_RI n=1-4	UART/Multiprocessor/LIN/Smart Card/Clock Synchronization Mode Receive Data Register Full Interrupt LIN Error interrupt
Transmit Data Register Empty Interrupt	USART_n_TI n=1-4	UART/Multiprocessor/LIN/Smart Card/Clock Synchronization Mode Transmit Data Register Empty Interrupt
Transmit Completion Interrupt	USART_n_TCI n=1-4	UART/Multiprocessor/LIN/Smart Card/Clock Synchronization Mode Transmit Completion Interrupt (Writing transmit data to the Transmit Data Register clears the interrupt)
Transmit Completion Interrupt	USART_n_TENDI n=1-4	UART/Multiprocessor/LIN/Smart Card/Clock Synchronization Mode Transmit Completion Interrupt (Writing 1 to USARTn_CR1.CTEND bit or writing transmit data to Transmit Data Register clears the interrupt)
Wake-up Signal/Interval Segment/Synchronization Segment Detection Interrupt	USART_n_BRKWKPI n=2/3/4	LIN Wake-up Signal/Interval Segment /Synchronization Segment Detection Interrupt
UART Receive TIMEOUT Interrupt	USART_n_RTO n=1-4	UART Receive TIMEOUT Interrupt
RX Line Wake-up Stop Mode Interrupt	USART_1_WUPI	USART1 RX Line Wake-up Stop Mode Interrupt

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23.4 Register Description

This chapter provides a detailed description of the USART module control status and related registers. The function register bit is only valid when the corresponding function is configured for the channel; otherwise, it defaults to 0.

23.4.1 Register List

USART1_NFC base address: 0x40055400

Table 23-10 USART1 Filter Control Register Offset

Offset	Register	Description	Width
0x1C	USART1_NFC	USART1 Filter Control Register	32

- USART1 base address: 0x4001D000
- USART2 base address: 0x4001D400
- USART3 base address: 0x40021000
- USART4 base address: 0x40021400

Table 23-11 Universal Synchronous Asynchronous Receiver/Transmitter (USART) Register Offset

Offset	Register	Description	Width
0x00	USART_SR	Status Register	32
0x04	USART_TDR	Transmit Data Register	16
0x06	USART_RDR	Receive Data Register	16
0x08	USART_BRR	Baud Rate Register	32
0x0C	USART_CR1	Control Register 1	32
0x10	USART_CR2	Control Register 2	32
0x14	USART_CR3	Control Register 3	32
0x18	USART_PR	Prescaler Register	32
0x1C	USART_LBMC	LIN Baudrate Measuring Counter Register	32

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23.4.2 Status Register (USART_SR)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000000C0																															
Name	Reserved															MPB	Reserved			LBM	TEND	LBD	WKUP	RTOF	TXE	TC	RXNE	BE	ORE	Reserved	FE	PE
Access																RO				RO	RO	RO	RO	RO	RO	RO	RO	RO	RO		RO	RO

Bit	Name	Functional Description	Access
31:17	*Reserved*	-	-
16	MPB	Multiprocessor Bit Flag ● 0b0: Current receive data is communication data ● 0b1: Current receive data is ID **Note** The MPB bit is only valid in multiprocessor mode.	RO
15:13	*Reserved*	-	-
12	LBM	LIN Synchronization Segment Detection Flag Only valid in USART2/USART3/USART4: ● 0b0: Synchronization segment not detected ● 0b1: Synchronization segment detected LBM set condition: ● When a synchronization segment is detected and the LBMC register update is completed. LBM clear condition: ● Writing 1 to the USART_CR1.CLBM bit. **Note** RE=0 does not reset the LBM bit.	RO
11	TEND	Transmit Completion Flag ● 0b0: Transmit data in progress ● 0b1: Data transmission complete **UART Mode, Multiprocessor Mode, LIN Mode, Clock Synchronization Mode** ● TEND set condition: ▶ When the last bit of a frame is transmitted, the value in the transmit data register is not updated. ● TEND clear condition: ▶ When TE=1, write transmit data to the transmit data register. ▶ Write 1 to the USART_CR1.CTEND bit. **Smart Card Mode** ● TEND set condition:	RO

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Bit	Name	Functional Description	Access
11	TEND	▶ After the last byte of data is transmitted, FE becomes 0 after a specific time period, and the value in the transmit data register is not updated. The specific timing for TEND set is: 2.5 bit durations after the check bit is transmitted. ● TEND clear condition: ▶ When TE=1, write transmit data to the transmit data register. ▶ Write 1 to the USART_CR1.CTEND bit.	RO
10	LBD	LIN Interval Segment Detection Flag Only valid in USART2/USART3/USART4: ● 0b0: No interval segment detected ● 0b1: Interval segment detected LBD set condition: ● When CR2.WKUPE=0, a low level on the RX line is detected with a width greater than or equal to the width set by the USART_CR2.LBDL register, and a break delimiter is detected. LBD clear condition: ● Write 1 to the USART_CR1.CLBD bit. **Note** RE=0 does not reset the LBD bit.	RO
9	WKUP	LIN Wakeup Signal Detection Flag Only valid in USART2/USART3/USART4: ● 0b0: No Wakeup signal detected ● 0b1: Wakeup signal detected WKUP set condition: ● When USART_CR2.WKUPE=1, a low level on the RX line with a width greater than or equal to 2.5 bit durations (130μS at 19.2kbps) is detected. WKUP Clear condition: ● Write 1 to the USART_CR1.CWKUP bit. **Note** RE=0 does not reset the WKUP bit. After detecting the WKUP signal as 1, it indicates that this LIN node has exited Sleep mode. After setting register USART_CR2.WKUPE=0, perform subsequent operations such as interframe space detection.	RO

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Bit	Name	Functional Description	Access
8	RTOF	UART Receive TIMEOUT Flag Bit ● 0b0: No UART receive TIMEOUT ● 0b1: UART receive TIMEOUT occurred RTOF set condition: ● From the detection of the STOP bit of the last frame data, no new Receive Data is detected after the set time has elapsed. RTOF clear condition: ● Write 1 to the USART_CR1.CRTOF bit. **Note** RTOF is set to 1 by hardware, and is only set to 1 when both USART_CR1.RE=1 and USART_CR1.RTOE=1. When USART_CR1.RE=0, the TIMEOUT function is enabled, but RTOF is not set to 1.	RO
7	TXE	Transmit Data Register Empty Flag ● 0b0: Transmit data register is not empty, the hardware sets TXE to 0 ● 0b1: Transmit data register is empty, the hardware sets TXE to 1 **Note** The TXE bit is valid in UART/Clock synchronization mode/LIN Mode.	RO
6	TC	Transmit Completion Flag ● 0b0: Transmit data in progress ● 0b1: Data transmission complete **UART Mode, Multiprocessor Mode, LIN Mode, Clock Synchronization Mode** ● TC set condition: ▶ TE=0: Transmission Disabled ▶ When the last bit of a frame is transmitted, the value in the Transmit Data Register is not updated. ● TC clear condition: ▶ When TE=1, write transmit data to the transmit data register. **Smart Card Mode** ● TC set condition: ▶ TE=0: Transmission Disabled ▶ After the last byte of data is transmitted, FE=0 after a specific time period, and the value in the transmit data register is not updated. The specific timing for TC set is: 2.5 bit durations after the check bit is transmitted. ● TC clear condition: ▶ When TE=1, write transmit data to the transmit data register. **Note** When the TE bit changes from 0 to 1, TC remains at 1.	RO

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Bit	Name	Functional Description	Access
5	RXNE	Receive Data Register not Empty Flag ● 0b0: No data received ● 0b1: Ready to read received data The RXNE bit is set to 1 and cleared to 0 by hardware. The hardware sets RXNE to 1 when the Receive Data is ready to be read, and clears RXNE to 0 after the Receive Data is read.	RO
4	BE	LIN Bus Error Flag Only valid in USART2/USART3/USART4: ● 0b0: No bus error. ● 0b1: Bus error occurred BE set condition: ● During data transmission, a mismatch is detected between the bus data and the transmitted data at the 13/16 position of each bit (16-bit oversampling). BE clear condition: ● Write 1 to the USART_CR1.CBE bit. **Note** TE=0 does not reset the BE bit. When BE=1, after the ongoing data transmission is completed, no new data transmission will start. The software must clear the BE flag and restart the transmission action.	RO
3	ORE	Receive Overflow Error Flag ● 0b0: No receive overflow error ● 0b1: Receive overflow error occurred ORE set condition: ● New data frame received while the receive data register remains unread. ORE clear condition: ● Write 1 to the USART_CR1.CORE bit. **Note** RE=0 does not reset the ORE bit. Data received before ORE=1 will be retained, while data received when ORE=1 will be discarded. When ORE=1, it cannot continue to receive data, and transmit data is also prohibited in clock synchronization mode.	RO
2	*Reserved*	-	-

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Bit	Name	Functional Description	Access
1	FE	Receive Frame Error Flag ● 0b0: No receive frame error ● 0b1: Receive frame error occurred **UART Mode, Multiprocessor Mode, LIN Mode** ● FE set condition: ▶ The stop bit of the received data frame is at low level. For two stop bits, only the first stop bit is checked. ● FE clear condition: ▶ Write 1 to the USART_CR1.CFE bit. **Note** RE=0 does not reset the FE bit. When FE=1, the received data is retained but the RI interrupt does not occur. After FE=1, receive data is disabled. In LIN mode, this flag bit is generated upon receiving the interval segment and does not indicate a frame error; it is also generated when receiving the synchronization segment if the baud rate deviation is significant. **Smart Card Mode** ● FE set condition: ▶ Sampled low level error signal flag. ● FE clear condition: ▶ Write 1 to the USART_CR1.CFE bit. **Note** RE=0 does not reset the FE bit.	RO
0	PE	Receive Data Check Error Flag ● 0b0: No receive data parity error ● 0b1: Receive data parity error occurred PE set condition: ● A parity check error occurs when receiving data. PE clear condition: ● Write 1 to the USART_CR1.CPE bit. **Note** RE=0 does not reset the PE bit. When PE=1, the received data is retained but the RI interrupt does not occur. Receive data is disabled after PE=1 is set.	RO

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23.4.3 Transmit Data Register (USART_TDR)

Offset	Bit Position															
0x04	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x01FF															
Name	Reserved						MPID	TDR								
Access							RW	RW								

Bit	Name	Functional Description	Access
15:10	*Reserved*	-	-
9	MPID	Multiprocessor Mode ID Bit In multiprocessor mode, the selection bit for transmitting communication data or transmitting ID: ● 0b0: Transmit data ● 0b1: Transmit ID **Note** The MPID bit is only valid in multiprocessor mode and must be set to the reset value in other modes.	RW
8:0	TDR	Transmit Data Transmit Data Register **Note** The most significant bit TDR[8] is only valid in UART Mode when the data length is set to 9 bits.	RW

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23.4.4 Receive Data Register (USART_RDR)

Offset	Bit Position															
0x06	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000															
Name	Reserved								RDR							
Access									RO							

Bit	Name	Functional Description	Access
15:9	*Reserved*	-	-
8:0	RDR	Receiving Data Receive Data Register **Note** The most significant bit RDR[8] is only valid in UART Mode when the data length is set to 9 bits.	RO

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23.4.5 Baud Rate Register (USART_BRR)

Offset	Bit Position																													
0x08	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000FFFF																															
Name	Reserved																DIV_Integer								Reserved	DIV_Fraction						
Access																	RW									RW						

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:8	DIV_Integer	Integer Frequency Division **Note** This bit can only be set when TE=0 & RE=0 (transmit/receive disabled).	RW
7	*Reserved*	*Reads as 1, Write as 1*	-
6:0	DIV_Fraction	Fractional Frequency Division **Note** This bit can only be set when TE=0 & RE=0 (transmit/receive disabled), and the setting takes effect only when FBME=1.	RW

Table 23-20 Baud Rate Calculation Formula (Fractional Baud Rate is disable where FBME=0)

Mode	Baud Rate Calculation Formula	Error E Calculation Formula
UART Mode/ Multi-processor Mode	$B = \frac{C}{8 \times (2 - OVER8) \times (DIV_Integer+1)}$	$E = \left\{ \frac{C}{8 \times (2 - OVER8) \times (DIV_Integer+1) \times B} - 1 \right\} \times 100\%$
Clock Synchronization Mode	$B = \frac{C}{4 \times (DIV_Integer+1)}$	-
Smart Card Mode	$B = \frac{C}{2 \times BCN \times (DIV_Integer+1)}$	$E = \left\{ \frac{C}{2 \times BCN \times (DIV_Integer+1) \times B} - 1 \right\} \times 100\%$

Table 23-21 Baud Rate Calculation Formula (Fractional Baud Rate is Enable where FBME=1)

Mode	Baud Rate Calculation Formula	Calculation Formula for Error E (%)
UART Mode/ Multi-processor Mode	$B = \frac{C \times (128 + DIV_Fraction)}{8 \times (2 - OVER8) \times (DIV_Integer+1) \times 256}$	$E = \left\{ \frac{C \times (128 + DIV_Fraction)}{8 \times (2 - OVER8) \times (DIV_Integer+1) \times 256 \times B} - 1 \right\} \times 100\%$

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Mode	Baud Rate Calculation Formula	Calculation Formula for Error E (%)
Clock Synchro-nization Mode	$B = \frac{C \times (128 + DIV_Fraction)}{4 \times (DIV_Integer+1) \times 256}$	-
Smart Card Mode	$B = \frac{C \times (128 + DIV_Fraction)}{2 \times BCN \times (DIV_Integer+1) \times 256}$	$E = \left\{ \frac{C \times (128 + DIV_Fraction)}{2 \times BCN \times (DIV_Integer+1) \times 256 \times B} - 1 \right\} \times 100\%$

Where:

- B: Baud rate (Mbps)
- C: Clock (MHz) set by USART_PR.ULBREN and USART_PR.PSC bits
- BCN: USART_CR3.BCN register setting value

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23.4.6 Control Register 1 (USART_CR1)

Offset	Bit Position																													
0x0C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x80000000																															
Name	SBS	NFE	FBME	ML	Reserved	CLBM	CTEND	MS	CLBD	CWKUP	CBE	CRTOF	CORE	Reserved	CFE	CPE	OVER8	Reserved		M	Reserved	PCE	PS	TENDIE	TXEIE	TCIE	RIE	SLME	TE	RE	RTOIE	RTOE
Access	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW		RW	RW	RW			RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31	SBS	UART Mode Receive Data Start Bit Detection Mode Setting Bit In UART Mode, the start bit detection setting for receive data: ● 0b0: Start bit detection method is low level on RX pin ● 0b1: Start bit detection mode is falling edge on RX pin **Note** This bit must retain the reset value in non-UART Mode. This bit can only be set when TE=0 & RE=0 (transmit/receive disabled).	RW
30	NFE	Digital Filtering Enable Bit ● 0b0: Disable ● 0b1: Enable **Note** This bit must retain the reset value in Clock Synchronization Mode and synchronization frame detection of LIN Mode. This bit can only be set when TE=0 & RE=0 (transmit/receive disabled).	RW
29	FBME	Fractional Baud Rate Function Enabled ● 0b0: Disable ● 0b1: Enable **Note** This bit can only be set when TE=0 & RE=0 (transmit/receive disabled).	RW
28	ML	MSB/LSB Selection Bit In UART Mode/Clock Synchronization Mode/Smart Card Mode, MSB/LSB selection bit: ● 0b0: LSB mode ● 0b1: MSB mode **Note** This bit can only be set when TE=0 & RE=0 (transmit/receive disabled).	RW

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Bit	Name	Functional Description	Access
27	*Reserved*	-	-
26	CLBM	LBM Clear Bit Only valid in USART2/USART3/USART4: Write 1 to clear LBM flag, write 0 has no effect; read always returns 0.	RW
25	CTEND	TEND Clear Bit Write 1 to clear TEND flag, write 0 has no effect; read always returns 0.	RW
24	MS	Communication Mode Selection Bit ● 0b0: UART Mode ● 0b1: Clock synchronization mode **Note** This bit can only be set when TE=0 & RE=0 (transmit/receive disabled) . In Smart Card Mode, MS must be written to the reset value.	RW
23	CLBD	LBD Clear Bit Only valid in USART2/USART3/USART4: Write 1 to clear LBD flag, write 0 has no effect; read always returns 0.	RW
22	CWKUP	WKUP Clear Bit Only valid in USART2/USART3/USART4: Write 1 to clear WKUP flag, write 0 has no effect; read always returns 0.	RW
21	CBE	BE Clear Bit Only valid in USART2/USART3/USART4: Write 1 to clear BE flag, write 0 has no effect; read always returns 0.	RW
20	CRTOF	RTOF Clear Bit Write 1 to clear RTOF flag, write 0 has no effect; read always returns 0.	RW
19	CORE	ORE Flag Clear Bit Write 1 to clear ORE flag, write 0 has no effect; read always returns 0.	RW
18	*Reserved*	-	-
17	CFE	FE Flag Clear Bit Write 1 to clear FE flag, write 0 has no effect; read always returns 0.	RW
16	CPE	PE Flag Clear Bit Write 1 to clear PE flag, write 0 has no effect; read always returns 0.	RW

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Bit	Name	Functional Description	Access
15	OVER8	UART Oversampling Mode UART oversampling mode setting, i.e., the number of base clock periods during one bit data transmission: ● 0b0: 16 bits ● 0b1: 8 bits **Note** This bit must retain the reset value in Smart Card Mode/Clock Synchronization Mode. This bit can only be set when TE=0 & RE=0 (transmit/receive disabled).	RW
14:13	*Reserved*	-	-
12	M	Data Length Setting Bit In UART Mode, transmit/receive data length setting bit: ● 0b0: 8 bits ● 0b1: 9 bits **Note** This bit must retain the reset value in LIN Mode/Smart Card Mode/Clock Synchronization Mode. This bit can only be set when TE=0 & RE=0 (transmit/receive disabled).	RW
11	*Reserved*	-	-
10	PCE	Check Enable Bit In UART Mode, the parity check enable bit: ● 0b0: No check ● 0b1: Check **Note** This bit must retain the reset value in LIN Mode/Multiprocessor Communication Mode/Clock Synchronization Mode, and must be set to 1 in Smart Card Mode. This bit can only be set when TE=0 & RE=0 (transmit/receive disabled).	RW
9	PS	Check Bit In UART Mode, the parity check selection bit: ● 0b0: Even parity ● 0b1: Odd parity **Note** This bit is valid only when PCE=1. This bit must retain 0 in Smart Card Mode. This bit can only be set when TE=0 & RE=0 (transmit/receive disabled).	RW

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Bit	Name	Functional Description	Access
8	TENDIE	Transmit Completion Interrupt Enable Bit ● 0b0: TENDI interrupt request is disabled, no TENDI interrupt occurs ● 0b1: TENDI interrupt request is enabled, TENDI interrupt occurred	RW
7	TXEIE	Transmit Data Register Empty Interrupt Enable Bit ● 0b0: TI interrupt request is disabled, no TI interrupt occurs ● 0b1: TI interrupt request is enabled, TI interrupt occurred **Note** When TE=0 and TXEIE=1 is written, it is necessary to wait for the TI interrupt to occur when TE=1. When TE=1 and writing TXEIE=1, it is necessary to wait until SR.TC=1 before the write can be performed.	RW
6	TCIE	Transmit Completion Interrupt Enable Bit ● 0b0: TCI interrupt request is disabled, no TCI interrupt occurs ● 0b1: TCI interrupt request enable, TCI interrupt occurred **Note** Read is valid in non-Smart Card Mode, reads as 0 in Smart Card Mode.	RW
5	RIE	Receive Interrupt, Error Interrupt Enable Bit ● 0b0: Receive interrupt and error Interrupt requests are diabled; no RI and EI Interrupts occur ● 0b1: Receive interrupt and error interrupt requests are enabled, RI and EI interrupts occurred	RW
4	SLME	Silent Mode Enable Bit In multiprocessor operations, the silent mode enable bit: ● 0b0: Normal mode ● 0b1: Silent mode When SLME=1, communication data with MPB bit set to 0 will not be read from the Receive Shift Register to the Receive Data Register, and the error flags ORE and FE bits will not be set. When ID data with the MPB bit set to 1 is received, SLME is automatically cleared and starts the normal data reception action. **Note** This bit is only valid in UART Multiprocessor Communication Mode. In other modes, this bit must retain the reset value.	RW
3	TE	Transmitter Enable Bit ● 0b0: Transmitter disable ● 0b1: Transmitter enable **Note** In Clock Synchronization Mode, this bit can only be written as 1 when TE=0 & RE=0 (transmit/receive disabled).	RW

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Bit	Name	Functional Description	Access
2	RE	Receiver Enable Bit ● 0b0: Receiver disable ● 0b1: Receiver enable **Note** In Clock Synchronization Mode, this bit can only be written as 1 when TE=0 & RE=0 (transmit/receive disabled).	RW
1	RTOIE	UART TIMEOUT Interrupt Enable Bit ● 0b0: UART TIMEOUT interrupt request is disabled, no RTOI interrupt occurs ● 0b1: UART TIMEOUT interrupt request is enabled, RTOI interrupt occurred	RW
0	RTOE	UART TIMEOUT Function Enable Bit ● 0b0: UART TIMEOUT function disable ● 0b1: UART TIMEOUT function enable	RW

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23.4.7 Control Register 2 (USART_CR2)

Offset	Bit Position																													
0x10	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000600																															
Name	Reserved												LBMIE	Reserved	SBKM	SBK	UATSBKE	LINEN	STOP	CLKC	Reserved		WKUPE	SBKL		LBDL	LBDIE	BEE	BEIE	WKUPIE	MPE
Access													RW		RW	RW	RW	RW	RW	RW			RW	RW		RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:20	*Reserved*	-	-
19	LBMIE	LIN Synchronization Segment Interrupt Enable Bit Only valid in USART2/USART3/USART4: ● 0b0: LIN synchronization segment detection interrupt request is invalid; no interrupt occurs ● 0b1: LIN synchronization segment detection interrupt request is valid; an interrupt occurs **Note** This bit must retain the reset value in Non-UART-LIN mode.	RW
18	*Reserved*	-	-
17	SBKM	Interval Segment Transmission Mode Only valid in USART2/USART3/USART4: For specific settings, refer to the SBK bit description.	RW
16	SBK	Interval Segment Transmission Enable Bit Only valid in USART2/USART3/USART4	RW

SBK	SBKM	Interval segment transmission
0b0	0b0	Do not send interval segment
0b0	0b1	Do not send interval segment
0b1	0b0	Write 1 to SBK when TE=1, the interval segment is automatically transmitted. After transmission completes, SBK is automatically cleared.
0b1	0b1	Write data 0x00 to USART_TDR.TDR to start sending the interval segment. After transmission is complete, SBK is automatically cleared.

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Bit	Name	Functional Description	Access
15	UATSBKE	UART Mode Interval Segment Detection Enable Bit Only valid in USART2/USART3/USART4: ● 0b0: Disable interval segment detection in UART mode ● 0b1: Enable interval segment detection in UART mode **Note** This bit can only be set when TE=0 & RE=0 (transmit/receive disabled).	RW
14	LINEN	LIN Function Enabled Only valid in USART2/USART3/USART4: ● 0b0: Disable LIN Function ● 0b1: Enable LIN function **Note** This bit can only be set when TE=0 & RE=0 (transmit/receive disabled).	RW
13	STOP	Stop Bit Setting Bit In UART Mode, stop bit length setting bit: ● 0b0: 1 stop bit ● 0b1: 2 stop bits **Note** This bit must retain the reset value in LIN Mode/Smart Card Mode/ Clock Synchronization Mode. This bit can only be set when TE=0 & RE=0 (transmit/receive disabled).	RW

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Bit	Name	Functional Description	Access
12:11	CLKC	Clock Control Bit **UART Mode** ● 0b00: Clock source is the clock generated by the internal baud rate generator and doesnot output to the USARTn_CK pin. The USARTn_CK pin can be used as a general-purpose IO ● 0b01: Clock source is the clock generated by the internal baud rate generator and output to the USARTn_CK pin. The output clock frequency equals the baud rate ● 0b10/0b11: Clock source is external input clock, the input clock frequency is 16 times the baud rate (USART_CR1.OVER8=0) or 8 times the baud rate (USART_CR1.OVER8=1) **Clock Synchronization Mode** ● 0b00/0b01: Clock source is the clock generated by the internal baud rate generator and output to the USARTn_CK pin ● 0b10/0b11: Clock source is external input clock, the input clock frequency equals baud rate **Smart Card Mode** ● 0b00: Clock source is the clock generated by the internal baud rate generator and doesnot output to the USARTn_CK pin. The USARTn_CK pin can be used as a general-purpose IO ● 0b01: Clock source is the clock generated by the internal baud rate generator and output to the USARTn_CK pin ● 0b10/0b11: Setting prohibited **Note** This bit can only be set when TE=0 & RE=0 (transmit/receive disabled). When both TE and RE are cleared to 0, the clock output on the USARTn_CK pin is disabled.	RW
10:9	*Reserved*	*All bits read as 1, Write as 1*	-
8	WKUPE	LIN Wake-up Signal Detection Enable Bit Only valid in USART2/USART3/USART4: ● 0b0: Disable wake-up signal detection ● 0b1: Enable wake-up signal detection **Note** Set WKUPE to 1 only when the system requires wake-up signal detection. After detecting the wake-up signal, software must clear WKUPE.	RW
7:6	SBKL	LIN Interval Segment Low Level Width Setting Bit Only valid in USART2/USART3/USART4: ● 0b00: 10 bits ● 0b01: 11 bits ● 0b10: 13 bits ● 0b11: 14 bits	RW

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Bit	Name	Functional Description	Access
7:6	SBKL	**Note** This bit must retain the reset value when UATSBKE=0 in non-UART-LIN Mode. This bit can only be set when TE=0 & RE=0 (transmit/receive disabled).	RW
5	LBDL	LIN Interval Segment Low Level Width Detection Threshold Setting Bit Only valid in USART2/USART3/USART4: ● 0b0: ≥ 10 bits ● 0b1: ≥ 11 bits **Note** This bit must retain the reset value when UATSBKE=0 in non-UART-LIN Mode. This bit can only be set when TE=0 & RE=0 (transmit/receive disabled).	RW
4	LBDIE	LIN Interval Segment Detection Interrupt Enable Bit Only valid in USART2/USART3/USART4: ● 0b0: LIN interval segment detection interrupt request is disable, no interrupt occurs ● 0b1: LIN interval segment detection interrupt request is enable, an interrupt occurred **Note** This bit must retain the reset value in non-UART-LIN Mode.	RW
3	BEE	LIN Bus Error Detection Function Enable Bit Only valid in USART2/USART3/USART4: ● 0b0: Disable LIN bus error function detection function ● 0b1: Enable LIN bus error function detection function **Note** This bit must retain the reset value when UATSBKE=0 in non-UART-LIN Mode. This bit can only be set when TE=0 & RE=0 (transmit/receive disabled).	RW
2	BEIE	LIN Bus Error Interrupt Enable Bit Only valid in USART2/USART3/USART4: ● 0b0: LIN bus error interrupt request is disabled, no interrupt occurs ● 0b1: LIN bus error interrupt request is enabled, an interrupt occurred **Note** This bit must retain the reset value in non-UART-LIN Mode.	RW

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Bit	Name	Functional Description	Access
1	WKUPIE	LIN Wake-up Signal Detection Interrupt Enable Bit Only valid in USART2/USART3/USART4: ● 0b0: LIN Wake-up signal detection interrupt request is disabled, no interrupt occurs ● 0b1: LIN Wake-up signal detection interrupt request is enabled, an interrupt has occurred **Note** This bit must retain the reset value in non-UART-LIN Mode.	RW
0	MPE	Multiprocessor Function Enable Bit In UART Mode, the multiprocessor function enable bit: ● 0b0: Disable ● 0b1: Enable **Note** This bit must retain the reset value in non-UART Mode. This bit can only be set when TE=0 & RE=0 (transmit/receive disabled).	RW

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23.4.8 Control Register 3 (USART_CR3)

Offset	Bit Position																													
0x14	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	DEP	DEM	Reserved	DEA				Reserved	BCN			Reserved					TDS	DED					CTSE	RTSE	Reserved		SCEN	LOOP	HDSEL	Reserved		
Access	RW	RW		RW					RW								RW	RW					RW	RW			RW	RW	RW			

Bit	Name	Functional Description	Access
31	DEP	DE Function Polarity Driver enable polarity mode: ● 0b0: DE signal is high when USART is in IDLE state ● 0b1: DE signal is low when USART is in IDLE state When USART TE or RE is enabled, this bit field cannot be written.	RW
30	DEM	DE Function Enabled Enable driver enable mode. This bit is used to activate external transceiver control via the DE signal. ● 0b0: DE function disable ● 0b1: DE function enable When USART TE or RE is enabled, writing to this bit field is prohibited.	RW
29	*Reserved*	-	-
28:25	DEA	DE Assertion Enable Time These bits define the time between DE (Driver Enable) signal activation and the start bit, expressed in sample time units (1/8 or 1/16 bit time), configured by the OVER8 bit: maximum configurable value is 0x7 when OVER8 is set to 1, and 0xF when OVER8 is set to 0. Minimum configuration is 0. When configured as 0, the DE signal occurs simultaneously with the start bit; when configured as 0x7 or 0xF, the DE signal occurs 7 or 15 time units before the start bit. When USART TE or RE is enabled, writing to this bit field is prohibited.	RW
24	*Reserved*	-	-
23:21	BCN	Basic Clock Count In Smart Card Mode, set the number of basic clock periods for 1 Bit data transmission: ● 0b000: 32 ● 0b001: 64 ● 0b010: Setting prohibited ● 0b011: 128 ● 0b100: Setting prohibited ● 0b101: 256 ● 0b110: 372	RW

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<table>
<tr><th>Bit</th><th>Name</th><th>Functional Description</th><th>Access</th></tr>
<tr><td>23:21</td><td>BCN</td><td>● 0b111: Setting prohibited
Note
This bit must retain the reset value in non-Smart Card Mode.
This bit can only be set when TE=0 & RE=0 (transmit/receive disabled).
USART2/USART3/USART4 does not support this function. Read always returns 0.</td><td>RW</td></tr>
<tr><td>20:16</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>15:14</td><td>TDS</td><td>TX State when TE is Disabled
Condition: The pin is configured for TX function and TE=0
● 0b00: When the above condition is met, the TX pin output is Hi-Z
● 0b01: When the above condition is met, the TX pin output is Hi-Z
● 0b10: When the above condition is met, the TX pin output is fixed at low level
● 0b11: When the above condition is met, the TX pin output is fixed at high level
Table 23-29 Port Status Truth Table
<table>
<tr><th>TE</th><th>TDS[1]</th><th>TDS[0]</th><th>TX Pin</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>Normal serial data output</td></tr>
<tr><td>0</td><td>0</td><td>x</td><td>Output Hi-Z</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Output low level</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Output high level</td></tr>
</table>
Note
This bit must retain the reset value in Smart Card Mode, Half-duplex Mode.</td><td>RW</td></tr>
<tr><td>13:10</td><td>DED</td><td>DE Assertion Cancellation Time
These bits define the interval between the end of the last stop bit in the transmitted message and the deactivation of the DE (Driver Enable) signal. It is expressed in sample time units (1/8 or 1/16 bit time), configured by the OVER8 bit: maximum configurable value is 0x7 when OVER8 is set to 1, and 0xF when OVER8 is set to 0.
Minimum configurable value is 0. When configured as 0, the DE signal transition occurs 2 time units after the end bit completes; when configured as 0x7 or 0xF, the DE signal occurs 9 or 17 time units after the end bit completes.
When USART TE or RE is enabled, writing to this bit field is prohibited.</td><td>RW</td></tr>
</table>

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Bit	Name	Functional Description	Access
9	CTSE	CTS Function Enable Bit ● 0b0: CTS function disable ● 0b1: CTS function enable **Note** This bit can only be set when TE=0 & RE=0 (transmit/receive disabled).	RW
8	RTSE	RTS Function Enable Bit ● 0b0: RTS function disable ● 0b1: RTS function enable **Note** This bit can only be set when TE=0 & RE=0 (transmit/receive disabled).	RW
7:6	*Reserved*	-	-
5	SCEN	Smart Card Mode Enable Bit ● 0b0: Disable Smart Card Mode ● 0b1: Enable Smart Card Mode **Note** This bit must retain the reset value in non-Smart Card Mode. This bit can only be set when TE=0 & RE=0 (transmit/receive disabled). USART2/USART3/USART4 does not support this function. Read always returns 0.	RW
4	LOOP	LIN Loop Mode Enable Bit Only valid in USART2/USART3/USART4: ● 0b0: Normal Mode ● 0b1: Loop Mode **Note** This bit can only be set when TE=0 & RE=0 (transmit/receive disabled).	RW
3	HDSEL	UART Single-wire Half-duplex Mode Enable Bit ● 0b0: UART full-duplex mode ● 0b1: UART half-duplex mode **Note** This bit can only be set when TE=0 & RE=0 (transmit/receive disabled).	RW
2:0	*Reserved*	-	-

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23.4.9 Prescaler Register (USART_PR)

Offset	Bit Position																													
0x18	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																				RTOB				Reserved				ULBREN	LBMPSC		PSC
Access																					RW								RW	RW		RW

Bit	Name	Functional Description	Access
31:12	*Reserved*	-	-
11:8	RTOB	UART TIMEOUT Length Setting Bits Specifies the timeout length when the UART TIMEOUT function is enabled: (The unit of setting is the number of received bits) ● 0b0000-0b0100: 15 bits ● 0b0101: 31 bits ● 0b0110: 63 bits ● 0b0111: 127 bits ● 0b1000: 255 bits ● 0b1001: 511 bits ● 0b1010: 1023 bits ● 0b1011: 2047 bits ● 0b1100: 4095 bits ● 0b1101: 8191 bits ● 0b1110: 16383 bits ● 0b1111: 32767 bits **Note** This bit can only be set when TE=0 & RE=0.	RW
7:5	*Reserved*	-	-
4	ULBREN	Ultra-low Baud Rate Enable Bit When using the internal clock source, the ultra-low baud rate function enable bit: ● 0b0: Ultra-low baud rate function disable ● 0b1: Ultra-low baud rate function enable And the prescaler division value is determined by PSC as follows: ● 0b00: PCLK1/128 ● 0b01: PCLK1/256 ● 0b10; PCLK1/512 ● 0b11: PCLK1/1024 **Note** This bit can only be set when TE=0 & RE=0.	RW

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Bit	Name	Functional Description	Access
3:2	LBMPSC	LIN Baud Rate Measurement Counter Clock Source Selection Only valid in USART2/USART3/USART4: ● 0b00: PCLK1 ● 0b01: PCLK1/2 ● 0b10: PCLK1/4 ● 0b11: PCLK1/8 **Note** This bit can only be set when TE=0 & RE=0.	RW
1:0	PSC	Prescaler Value When using the internal clock source, the prescaler division ratio selection bit: ● 0b00: PCLK1 ● 0b01: PCLK1/4 ● 0b10: PCLK1/16 ● 0b11: PCLK1/64 **Note** This bit can only be set when TE=0 & RE=0.	RW

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23.4.10 LIN Baudrate Measuring Counter Register (USART_LBMC)

Offset	Bit Position																													
0x1C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																LBMC															
Access																	RO															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	LBMC	LIN Baud Rate Measurement Result Counter Only valid in USART2/USART3/USART4: LIN slave node uses the clock source selected by the USART_PR.LBMPSC register to measure the frequency of the synchronization segment transmitted by the master node. The measured LIN communication baud rate is obtained by dividing the count clock frequency selected by USART_PR.LBMPSC by the value of LBMC. **Note** The value of LBMC is meaningful only after being read upon completion of the synchronization segment.	RO

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23.4.11 USART1 Filter Control Register (USART1_NFC)

Offset	Bit Position																													
0x1C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																													USART1_NFE	USART1_NFS	
Access																														RW	RW	

Bit	Name	Functional Description	Access
31:3	*Reserved*	-	-
2	USART1_NFE	USART1 Filter Enable Control Controls the analog filter on the RX line in STOP mode: ● 0b0: Analog filter disable ● 0b1: Analog filter enable. For the filter range, refer to the setting of USART1_NFS.	RW
1:0	USART1_NFS	USART1 Filter Frequency Range Setting Controls the filtering range of the analog filter on the RX line in STOP mode: ● 0b00: Filter width gear 1 ● 0b01: Filter width gear 2 ● 0b10: Filter width gear 3 ● 0b11: Filter width gear 4 For specific values of each setting, please refer to the relevant description in the "Electrical Specifications - Operating conditions - RX Filtering Characteristics in USART1 STOP Mode" chapter of the Datasheet.	RW

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23.5 Precautions

23.5.1 UART Precautions

Transmitter

When the transmitter is disabled in UART mode (USARTn_CR1.TE=0), the TX pin can be used as a general-purpose I/O, allowing output value and direction configuration. If the output is 0, it will cause a frame error on the receiver side, thereby triggering an interrupt in data transmission. If the output is 1, the receiver cannot detect the start bit, thus preventing data transmission from starting.

Receiver

In UART mode, when a frame error occurs, software can detect whether the subsequent RX line is at a low level to determine if the sender intends to interrupt the transmission.

If the start bit detection mode for receive data is set to low level detection, continuing to receive all low level data after clearing the error flag will cause the receive error to occur again.

23.5.2 Clock Synchronous Mode Precautions

1. When using an external input clock for data transmission, the USARTn_TDR.TDR register must be updated before the clock is applied. After writing data to the register, the clock input must be delayed by at least one bit time.
2. When transmitting data continuously, the next frame must be updated before the last bit of the current frame is transmitted.

23.5.3 Other Precautions

To prevent the TX communication line from entering Hi-Z state when transmission is disabled, the following methods can be adopted:

- Communication line pull-up;
- Before the end of data transmission and before USARTn_CR1.TE=0, configure the TX pin as a general-purpose IO output.
- Before transmitting data starts, after USARTn_CR1.TE=1, configure the IO as TX function.
- Fix the USARTn_TX output pin to a preset value by configuring USARTn_CR3.TDS.

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24 Inter-Integrated Circuit (I2C)

24.1 Introduction

I2C (Inter-Integrated Circuit) used as an interface between the microcontroller and the I2C serial bus. Provide multi-master mode function, which can control the protocol and arbitration of all I2C buses. Standard mode and fast mode are supported. SMBus is also supported.

24.2 Features

- I2C bus mode and SMBUS bus mode are optional. Master mode and slave mode are optional. Automatically ensure various preparation times, hold times, and bus idle times corresponding to the transfer rate
- Standard mode up to 100kbps, fast mode up to 400kbps
- The start condition, restart condition, and stop condition are automatically generated, and the start condition, restart condition, and stop condition of the bus can be detected
- Supports up to 128 slave mode addresses. Supports 7-bit address format and 10-bit address format. Broadcast call address, SMBus host address, SMBus device default address, SMBus alarm address can be detected
- Answer bits can be automatically determined when sent. Answer bits can be automatically sent when reception
- Handshake function
- Arbitration function
- Timeout function, can detect SCL clock stop for a long time
- SCL input and SDA input have built-in digital filters that are programmable to filter
- Communication error, receive data full, send data empty, one frame send end, address match unanimously interrupt
- 2-stage transmit FIFO and 2-stage receive FIFO

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24.3 Functional Description

24.3.1 I2C System Block Diagram

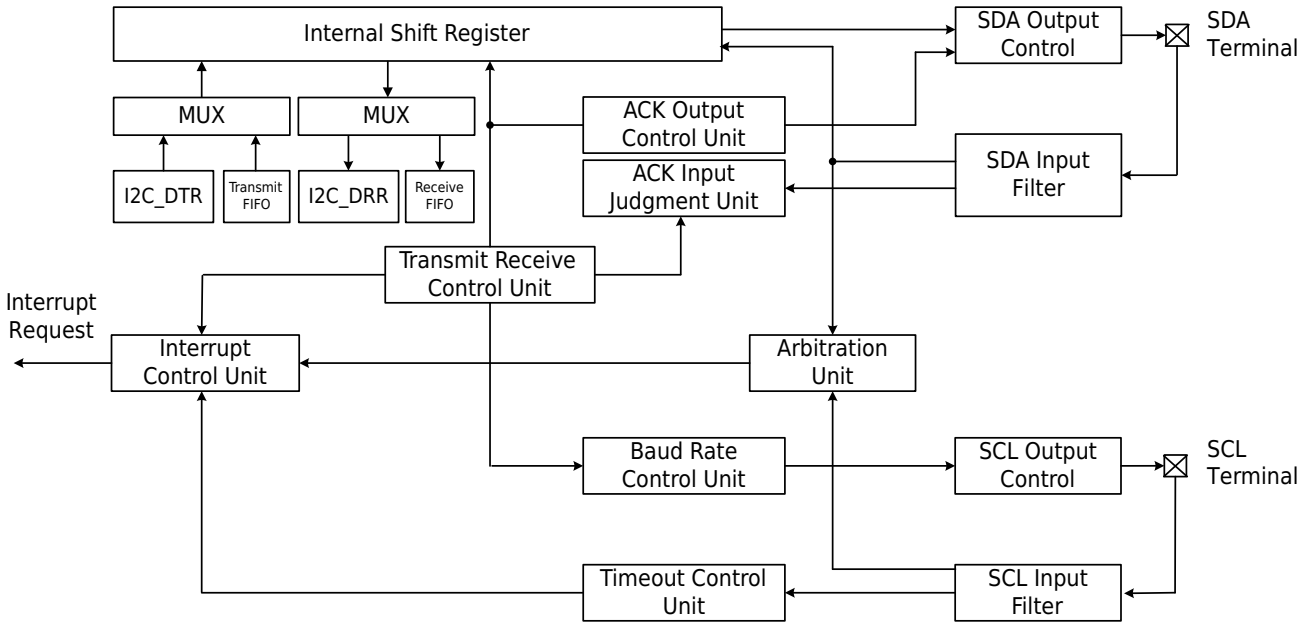

Figure 24-1 I2C System Block Diagram

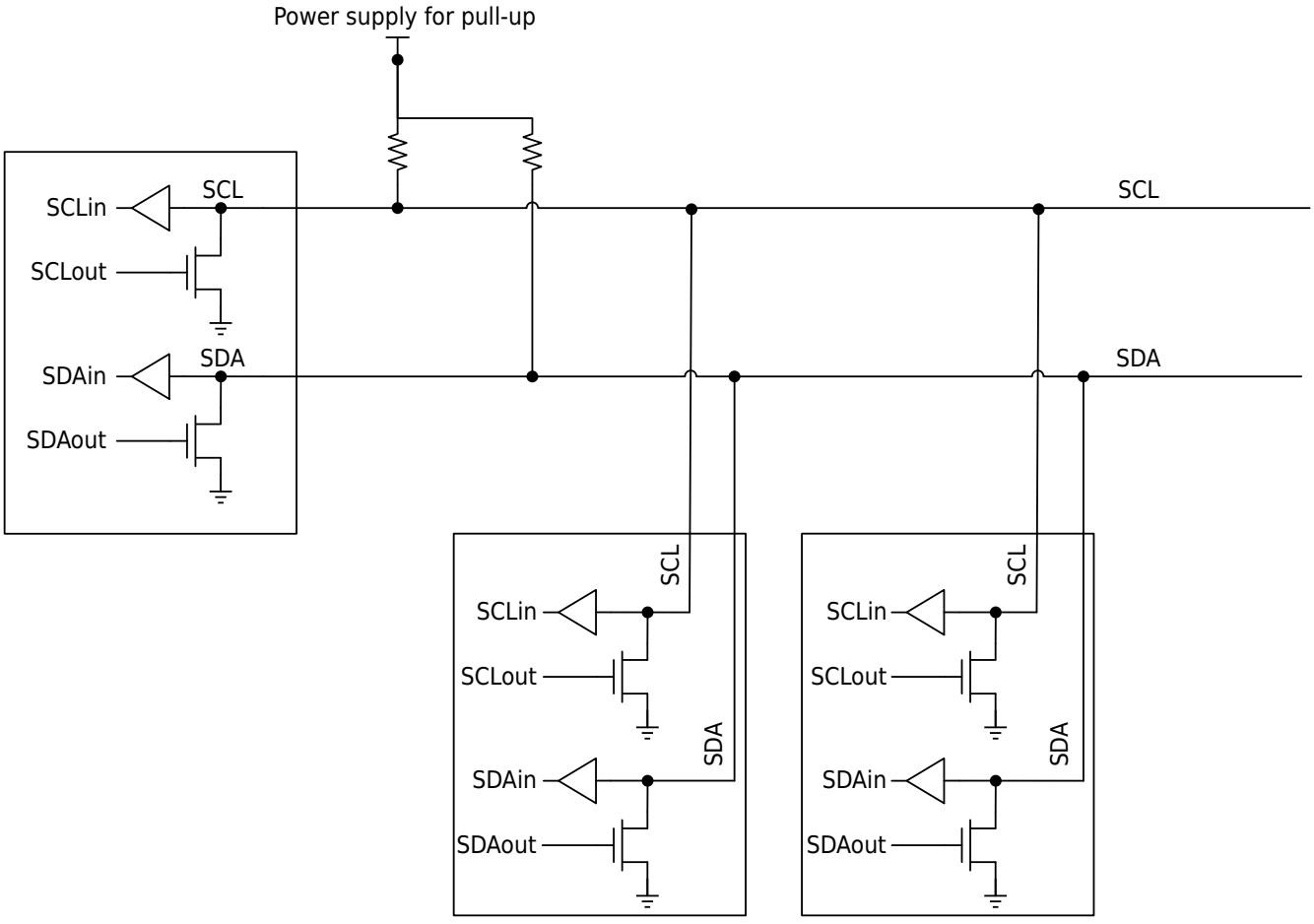

Figure 24-2 Example of I2C Bus Structure

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Table 24-1 Input/Output Pin

Pin Name	Input/Output	Function
SCL	Input/Output	Input/output pin of serial clock
SDA	Input/Output	Input/output pin of serial data

When the I2C bus is selected, please set the SCL/SDA input level to the Schmitt level (compatible with the CMOS level). When the SMBus is selected, please set the SCL/SDA input level to the CMOS level. For specific configuration details, please refer to the relevant description of the PCRxy.CINSEL bit in the "General-Purpose IO (GPIO)" chapter .

24.3.2 I2C Protocol

24.3.2.1 Data Transmission

I2C bus consists of a clock line (SCL) and a data line (SDA). All connection devices must be drain open output. The SCL and SDA lines are connected to external pull-up resistors, and the resistance value depends on the system application.

In general, a complete communication process consists of the following four parts:

1. Start Condition
2. Address Transmission
3. Data Transmission
4. Stop Condition

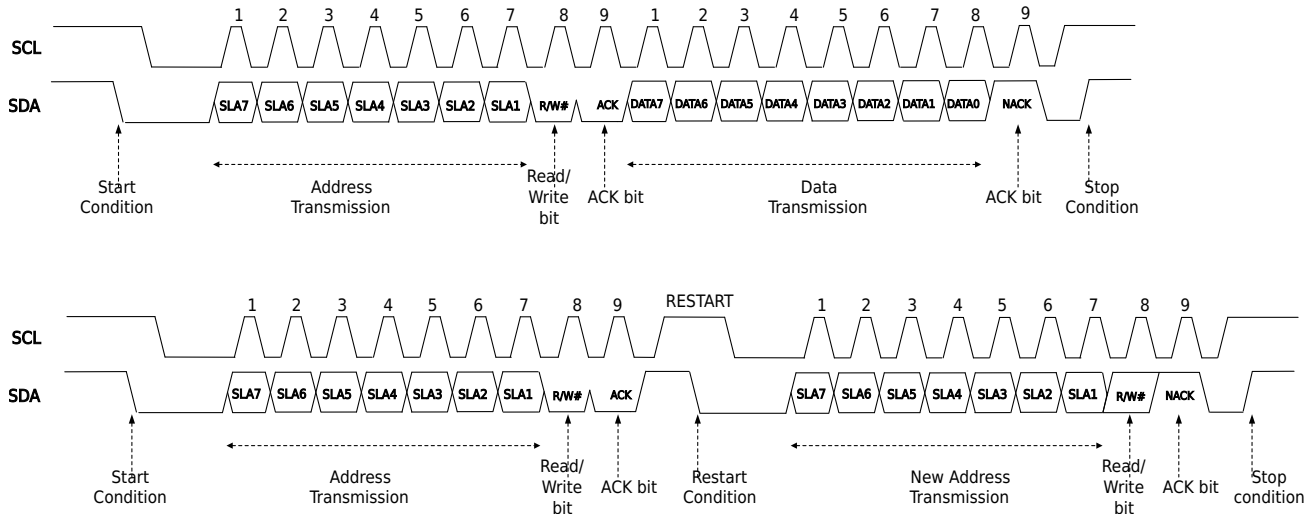

Figure 24-3 I2C Bus Timing Diagram

Start Condition

When the master on the bus does not drive the bus, the bus enters the idle state. Both SCL and SDA are high level. Devices on the bus in idle state can start the communication by sending the start condition.

If the START position is set to 1 in the I2C_SR.BUSY flag of 0 (bus is idle), the start condition is issued. If a start condition is detected, the I2C_SR.BUSY flag and I2C_SR.STARTF flag are automatically set to 1 and the START bit is automatically set to 0. At this point, if the status of the SDA signal sent in the START bit 1 is the same as that of the SDA line, and the start condition is detected, it is considered that the start condition is correctly issued by the START bit, and the I2C_SR.MSL bit and I2C_SR.TRA bit are automatically set to 1 and then changed to the master send mode. In addition, I2C_SR.TEMPTYF

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automatically changes to 1 because the TRA bit is 1. Next write the slave address to the I2C_DTR register and send the address.

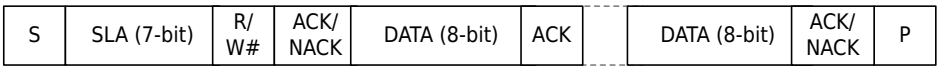
Address Transmission

The frame after the start condition or restart condition is an address frame that specifies the object address for master communication. The specified slave is always enable until the stop condition is sent.

The top 7 bits of the address frame are the slave addresses. The eighth bit of the address frame determines the direction of the data frame.

1. The 7-bit addressing mode is shown in the following figure [7-bit address format]
   Master send mode, master send address frame 8th bit is 0;
   Master receive mode, master send address frame 8th bit is 1.
2. The 10-bit addressing mode is shown in the following figure [10-bit address format]
   Master send mode, master first frame send header sequence (0b11110XX0, where XX represents the top two digits of the 10-bit address), then the second frame send the low eight-bit slave address.
   Master receive mode, master first frame send header sequence(0b11110XX0, where XX represents the top two digits of the 10-bit address), and then the second frame send the low eight-bit slave address. Next, a restart condition is sent, and then a frame header sequence is sent (0b11110XX1, where XX represents the top two digits of the 10-bit address).

7-bit Address Format



10-bit Address Format

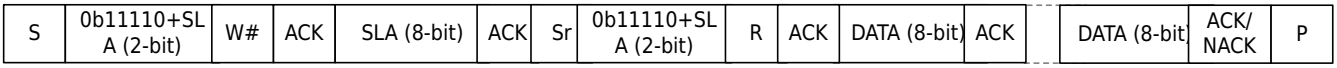


Figure 24-4 Data Format of I2C Bus

- S: Indicates the start condition
- SLA: Indicates the slave address
- R/W#: Indicates the direction of transmission and reception. Send data from slave to master when R/W# is 1; When R/W# is 0 the data is sent from the master to the slave.
- Sr: Indicates the restart condition
- DATA: Indicates the data sent and received
- P: Indicates the stop condition

Data Transmission

After address matching is consistent, the master on the bus transmits data frame by frame according to the direction defined by R/W.

The data transmitted after all address frames are treated as data frames. Even a low 8-bit address in a 10-bit address format is considered a data frame.

The length of the data frame is 8 bits. The low-level SDA of the SCL changes, the high-level SDA of the SCL remains, and a bit of data is sent per clock period. The 9th clock after the data frame is an answer bit and is a handshake signal from the receiver to the transmitter.

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If data is received from the slave on the bus and does not respond to the master in the 9th clock period, the slave must send NACK. If the master receives data on the bus, NACK is sent in the 9th period, the slave receives NACK, and data is stopped from the slave.

Whether the master or the slave sends NACK, the data transfer terminates. The master can do any of the following:

1. Transmit stop condition to release bus;
2. Send the restart condition to start a new communication.

- Master transmitting data

  In master transmit mode, the master outputs SCL clock and transmits data, the slave receives data and returns an answer. The sequence of master sending data is shown in the following figure.

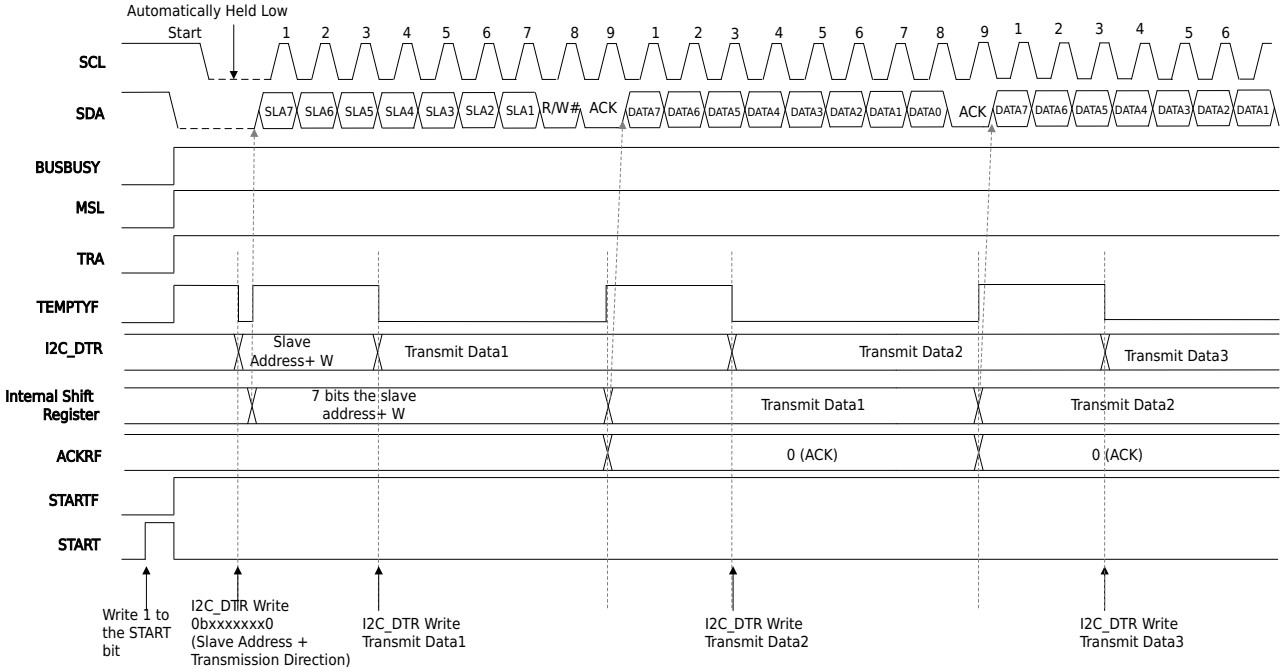

Figure 24-5 Sequence Diagram of Master Transmitting Data in 7-bit Address Format (Example)

- Master receiving data

  In master receiving mode, the master outputs an SCL clock, receives slave data, and returns an answer. The running sequence of receiving data by the master is shown in the following figure.

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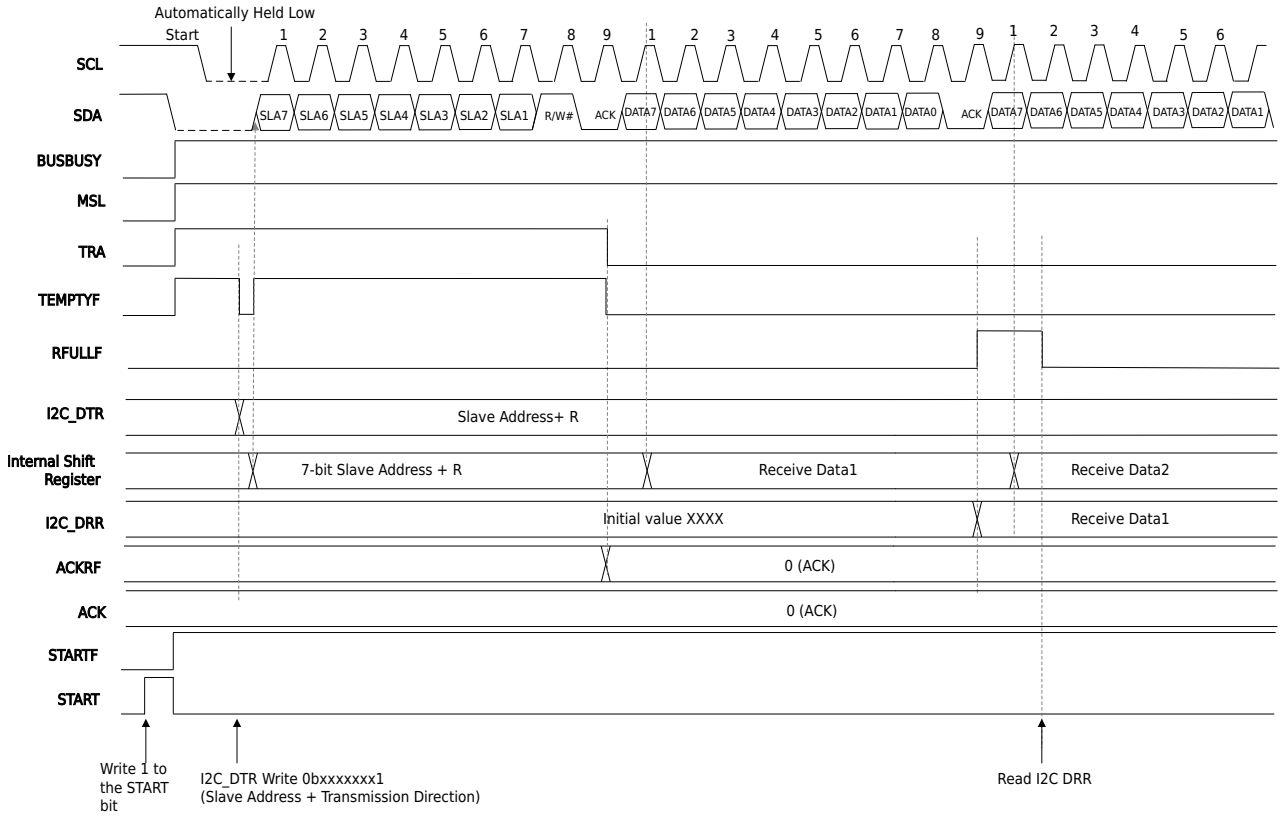

Figure 24-6 Sequence Diagram of Master Receiving Data in 7-bit Address Format (Example)

- Slave transmitting data

  In slave send mode, the SCL clock from the master is received. This product sends data for the slave and receives a reply from the master. The sequence of data sent from the slave is shown in the following figure.

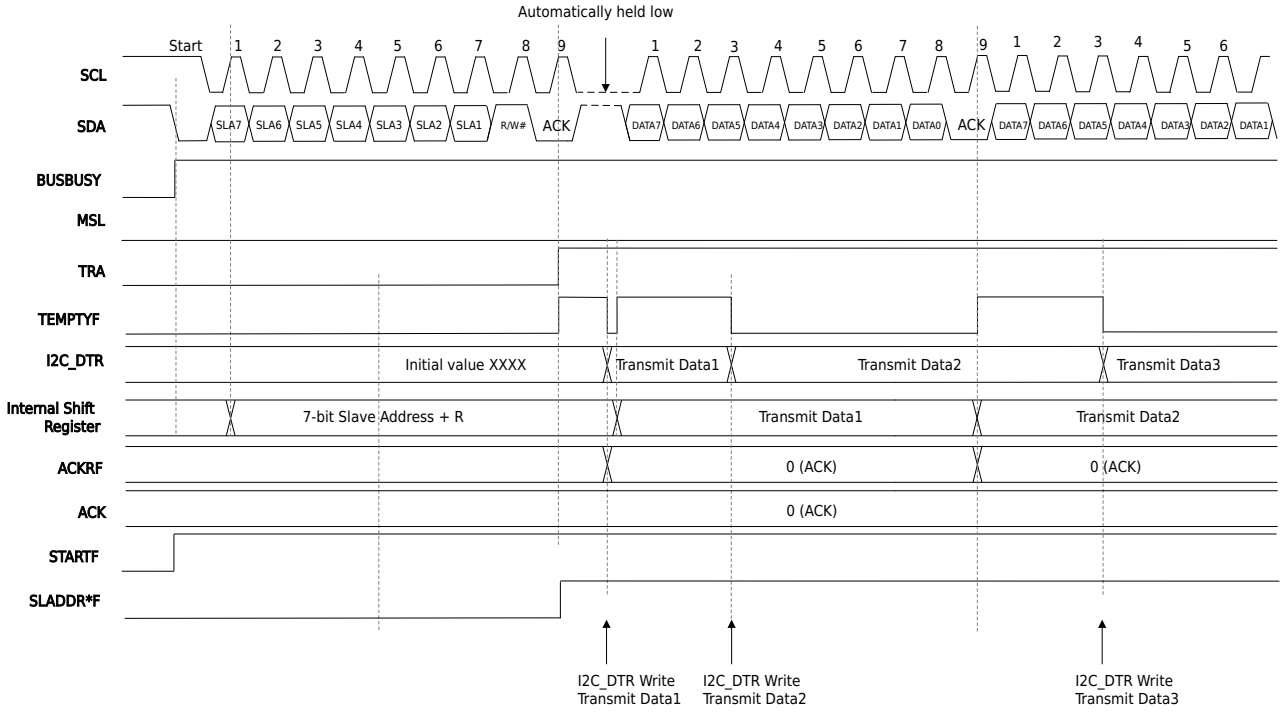

Figure 24-7 Sequence Diagram of Slave Transmitting Mode in 7-bit Address Format (Example)

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- Slave receiving data

  In slave receiving mode, the SCL clock and data from the master are received, and the response is returned after receiving the data. The sequence of data received from the slave is shown in the following figure.

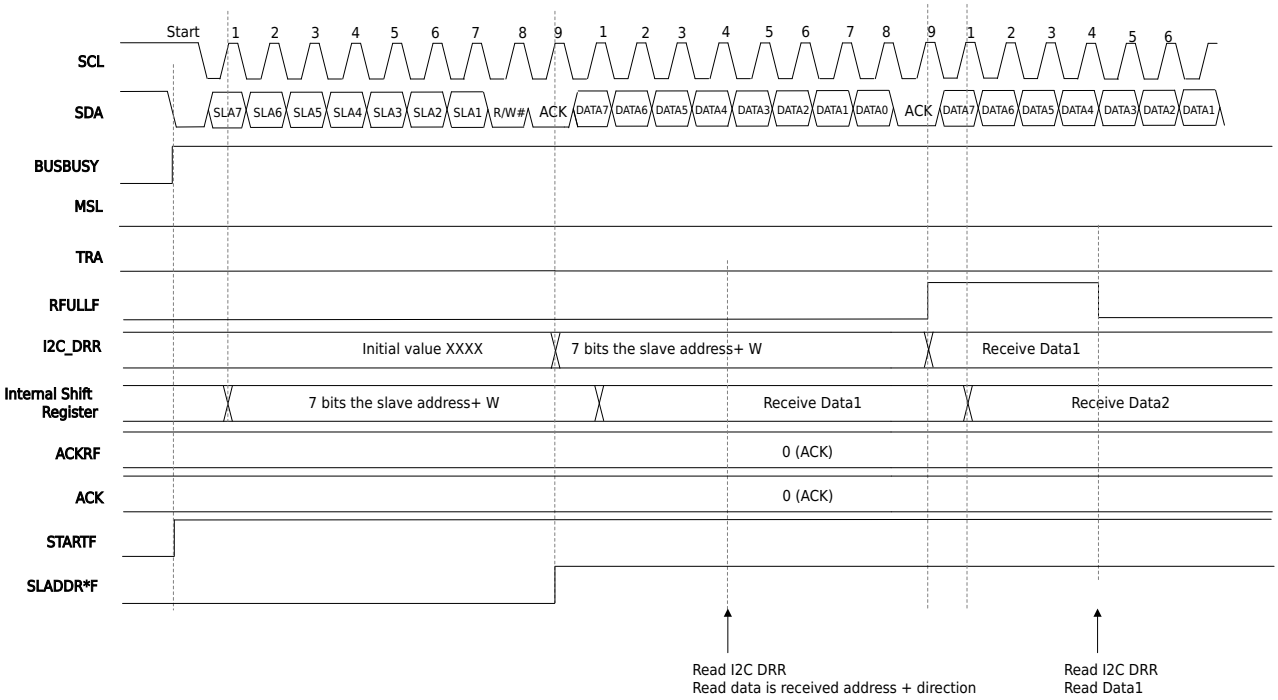

Figure 24-8 Sequence Diagram of Slave Receiving Data in 7-bit Address Format (Example)

Stop Condition

A stop condition is sent via the I2C_CR1.STOP bit.

When the I2C_SR.BUSY flag is 1 (bus is busy) and the I2C_SR.MSL bit is 1 (master mode), the STOP bit is set to 1 to issue a stop condition.

Restart Condition

A restart condition is generated via the I2C_CR1.RSTART bit.

When the I2C_SR.BUSY flag is 1 (bus is busy) and the I2C_SR.MSL bit is 1 (master mode), the RSTART bit is set to 1 to generate a restart condition.

Using the restart condition, the master can switch transmit/receive modes without releasing BUS authority. Communication can also be established with another slave without releasing BUS authority.

24.3.2.2 SCL Clock Synchronization

When using the I2C bus in multi-master mode, there is a possibility that the SCL clock may conflict due to competition with other masters. If the SCL clock conflicts, the master needs to synchronize with the SCL clock and synchronize the SCL clock bit by bit. When the rising edge of the SCL line is detected and the high level set by I2C_CCR.SHIGHW register is counted, if the SCL line is lowered due to the SCL clock output of other masters, the increment count of the high level width is stopped when the falling edge of the SCL line is detected, and the increment count of the low level width set by I2C_CCR.SLOWW is started while the SCL line is driven to low level. When the counting of the low-level width ends, the low-level drive of the SCL line is terminated and the SCL line is released. At this time, if the low level width of the SCL clock of other masters is greater than the low-level width set by SLOWW, the low-level width of the SCL clock is prolonged. When other masters end the low-level output, release the SCL line

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and the SCL clock rises. Therefore, in case of SCL clock output conflict, the high level width of SCL clock synchronizes with short clock, and the low level width synchronizes with long clock.

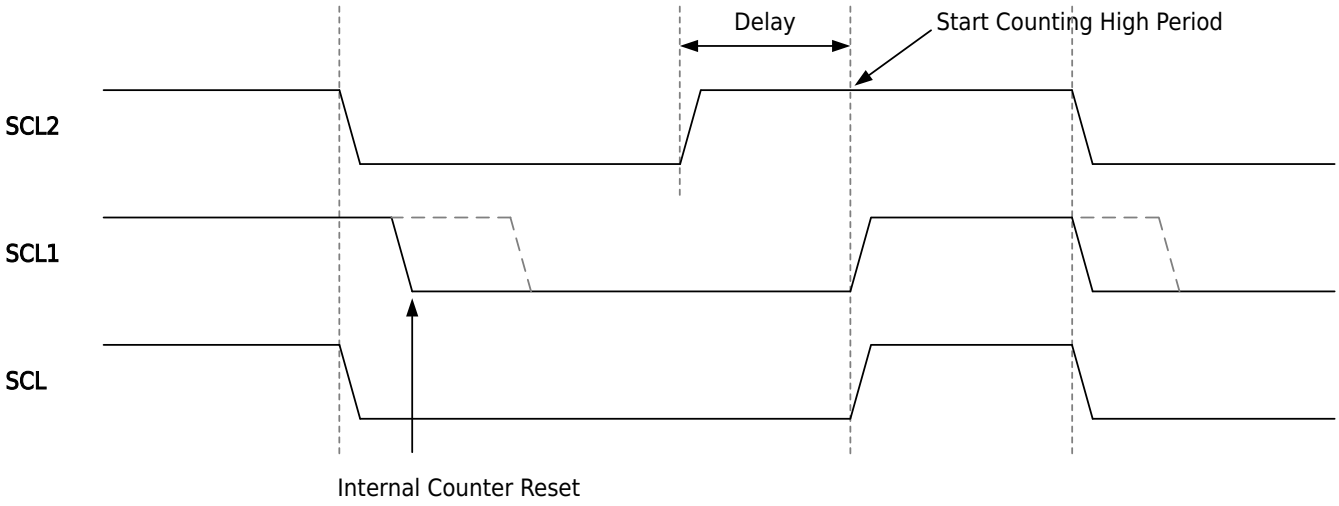

Figure 24-9 SCL Synchronous Timing

24.3.2.3 Arbitration

I2C bus is a real multi-master bus that allows multiple masters to connect.

If two or more masters try to control the bus at the same time, the SCL clock synchronization process determines the bus clock. The low period of the bus clock depends on the longest low-level clock and the high period depends on the shortest high-level clock. The results of arbitration are determined by the data collected at high levels. When the SDA output sent is a high-level output (the SDA pin is in a high impedance state) and the SDA line is detected to be at a low-level, arbitration fails. The I2C_SR.AROLF bit will be set to "1" by hardware. If a master arbitration fails, it is immediately transferred to the slave receiving mode. At this point, if the slave addresses matches, including broadcast addresses, the slave mode continues to run.

24.3.2.4 Handshake

The handshake is realized by SCL clock synchronization mechanism during data transfer. After transmitting a frame of data (including ACK bits), the slave maintains the SCL clock line at low level. In this case, the low level of the SCL clock causes the master to enter the waiting state until the SCL line is released by the slave.

Slave Transmitting Mode

In the transmitting mode (I2C_SR.TRA bit=1), if the internal shift register is empty and the transmitting data (I2C_DTR register) is not written, the SCL line is automatically kept low in the low level interval between the 9th clock and the 1st clock of the next transmission. The action timing is shown in the figure below.

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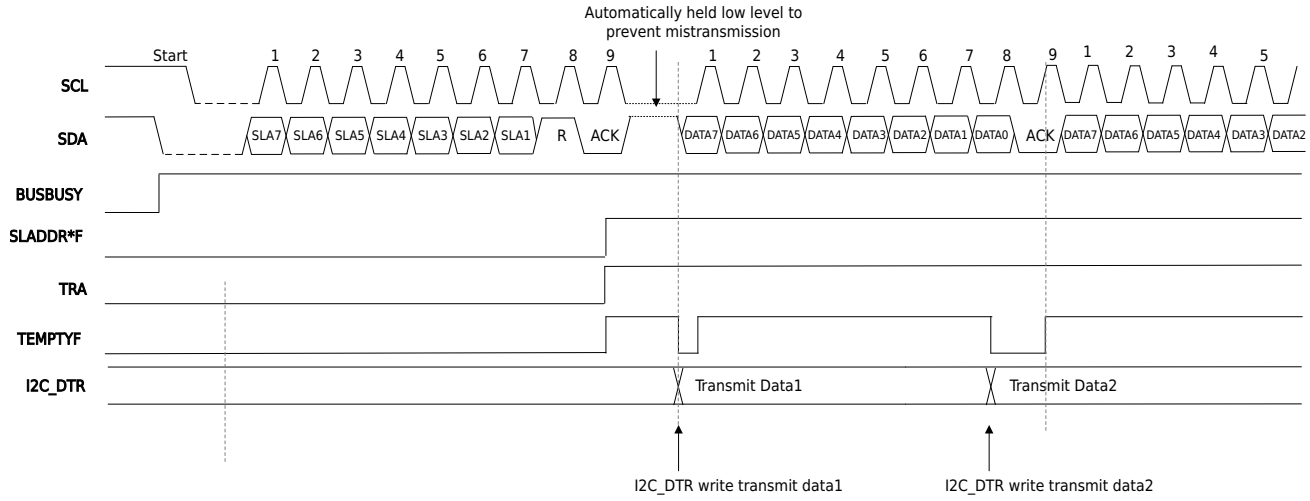

Figure 24-10 Transmitting Timing Diagram of Slave (1)

After the I2C_SR.NACKF flag is changed to 1 or the last sent data is written to the I2C_DTR register when I2C_CR4.NACKTRA_CLREN=0, wait until the I2C_SR.TENDF flag changes to 1 while the I2C_SR.TEMPTYF flag is 1. When the I2C_SR.NACKF flag or TENDF flag is 1, keep the SCL line low after the ninth clock drops. At this point, the communication must be ended by reading I2C_DRR register, thereby releasing the SCL line.

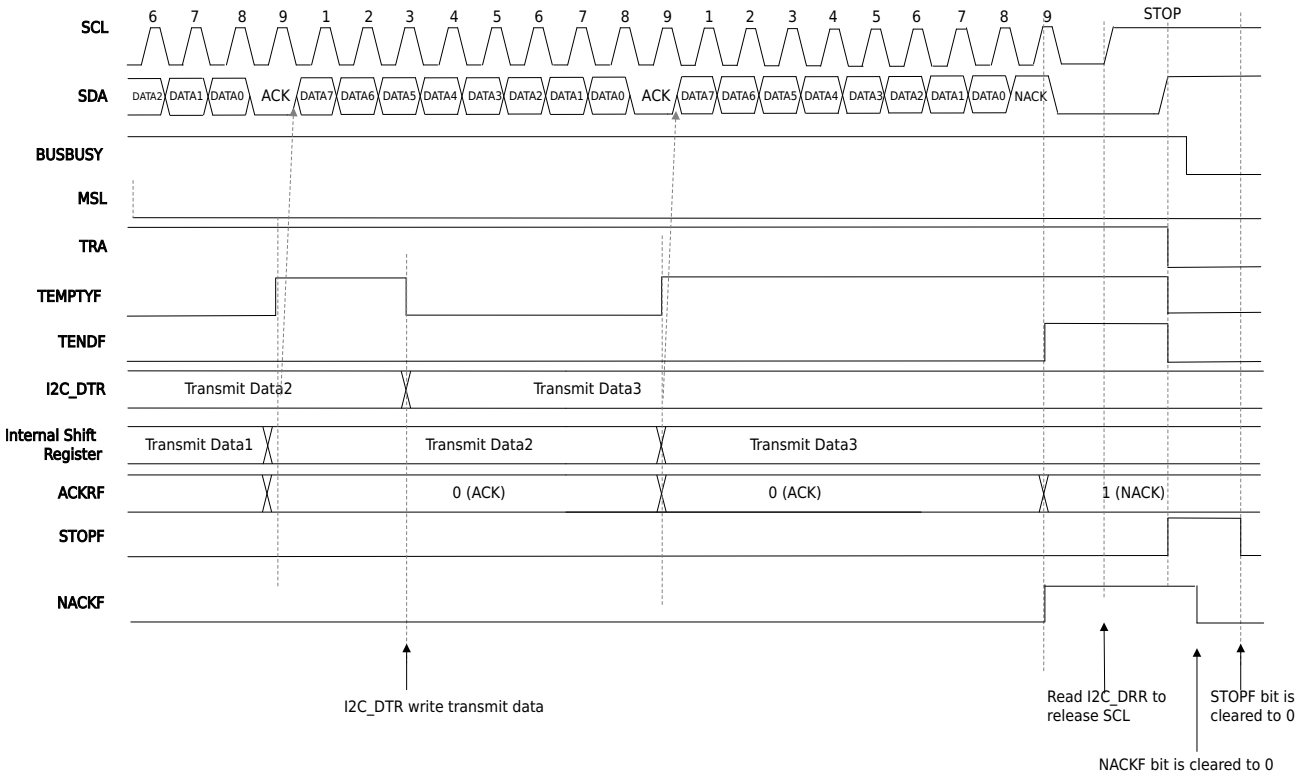

Figure 24-11 Transmitting Timing Diagram of Slave (2)

Slave Receiving Mode

If a response processing delay occurs in receiving mode (I2C_SR.TRA bit=0) and when the received data is full (I2C_SR.RFULLF flag=1) due to the delay of at least one transmission frame read received data (I2C_DRR register), etc., the SCL line is automatically maintained low between the 8th SCL and the 9th SCL clock, as shown in the following figure.

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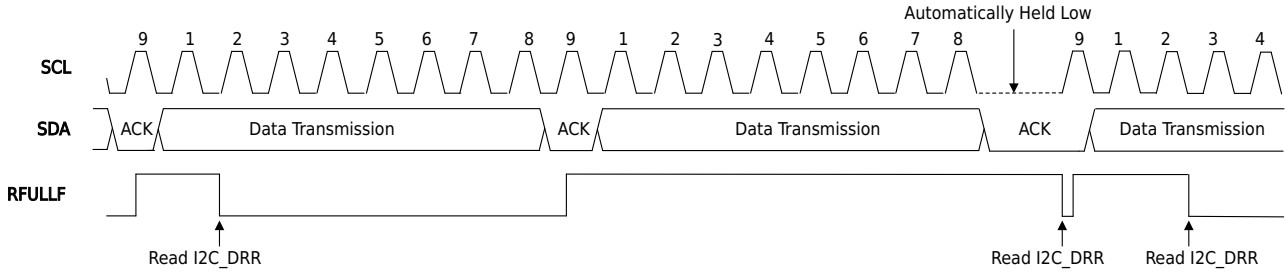

Figure 24-12 Slave Receiving Timing Diagram

Fast ACK/NACK

In SMBUS communication, the data packet error code (PEC) of SMBUS is calculated or the received data is checked using the built-in CRC operator. During a PEC code check, transmits an ACK or NACK based on matching in the last byte. This requires the SCL to be kept low at the falling edge of the eighth clock of the last byte of the received SCL. This satisfies the software processing time. The software writes I2C_CR1.ACK bit to remove SCL low level according to the calculation results. Fast ACK/NACK is controlled through I2C_CR3.FACKEN bit, action sequence is shown in the following figure.

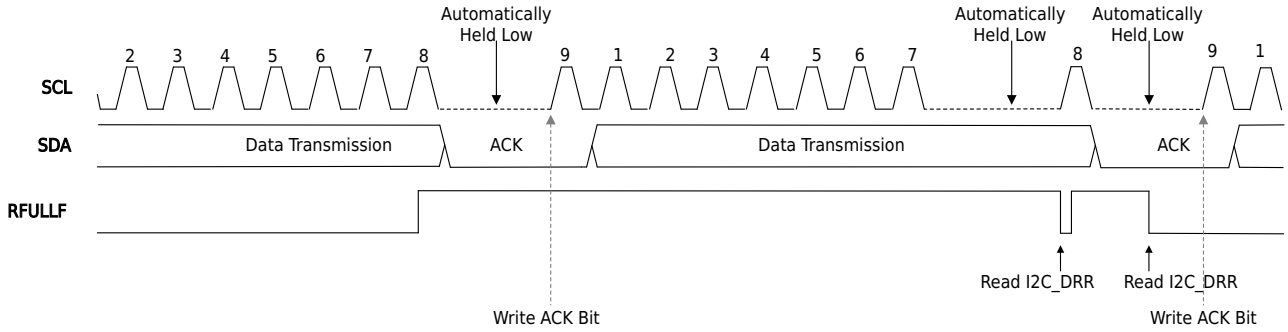

Figure 24-13 Fast ACK/NACK Timing Diagram

24.3.3 Address Matching

As a slave, two kinds of addresses other than broadcast address and master notification address can be set, and 7-bit address or 10-bit address format can be set for slave address.

24.3.3.1 Slave Address Matching

The I2C bus can set two kinds of slave addresses, and has corresponding slave address detection functions. When SLADDR1EN and SLADDR0EN are "1", the slave addresses set by I2C_SLR1 and I2C_SLR0 register can be detected.

If the set slave address matching is consistent, the corresponding SLADDR1F and SLADDR0F are set to 1 at the rising edge of the 9th clock of the SCL clock, and then the I2C_SR.RFULLF flag or the I2C_SR.TEMPTYF flag is set to 1 according to the subsequent R/W# bit. As a result, either receiving full interrupt or sending empty interrupt can be generated, and can determine which slave address is specified by confirming the I2C_SR.SLADDR1F, SLADDR0F flags.

The timings of I2C_SR.SLADDR1F/SLADDR0F flags changing to 1 are shown in the figure below.

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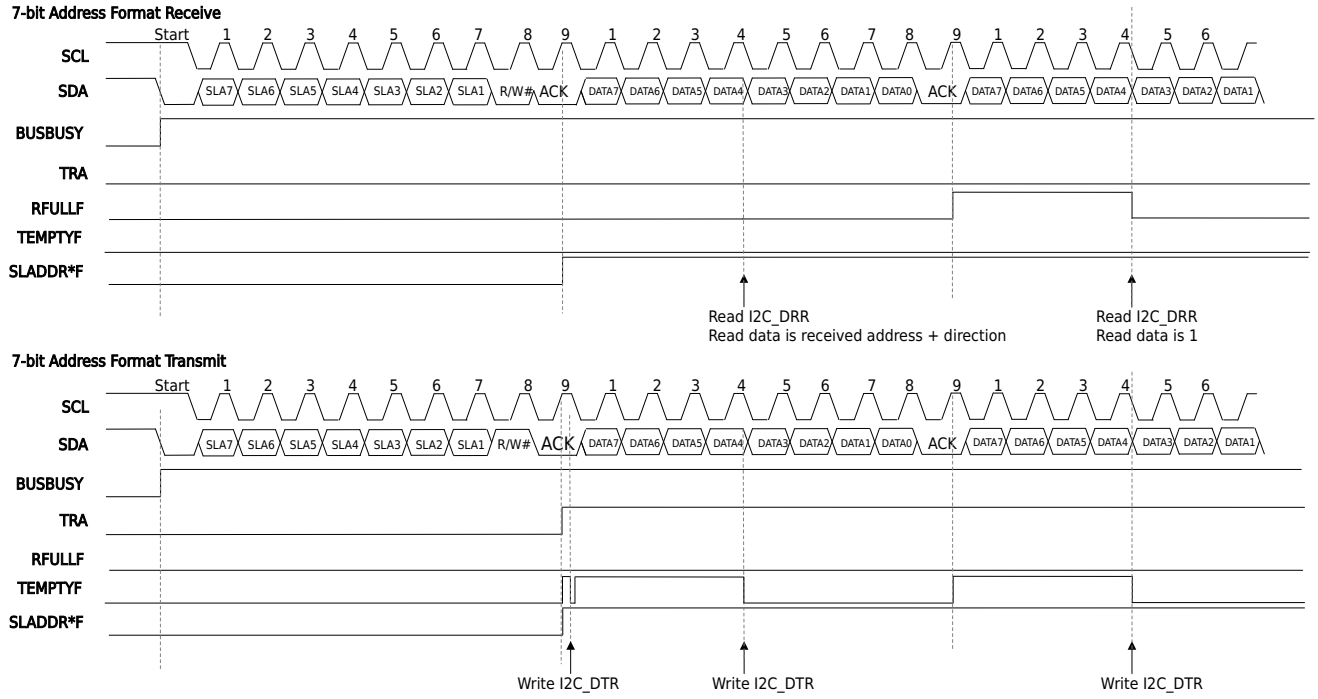

Figure 24-14 Timing when Selecting 7-bit Address Format

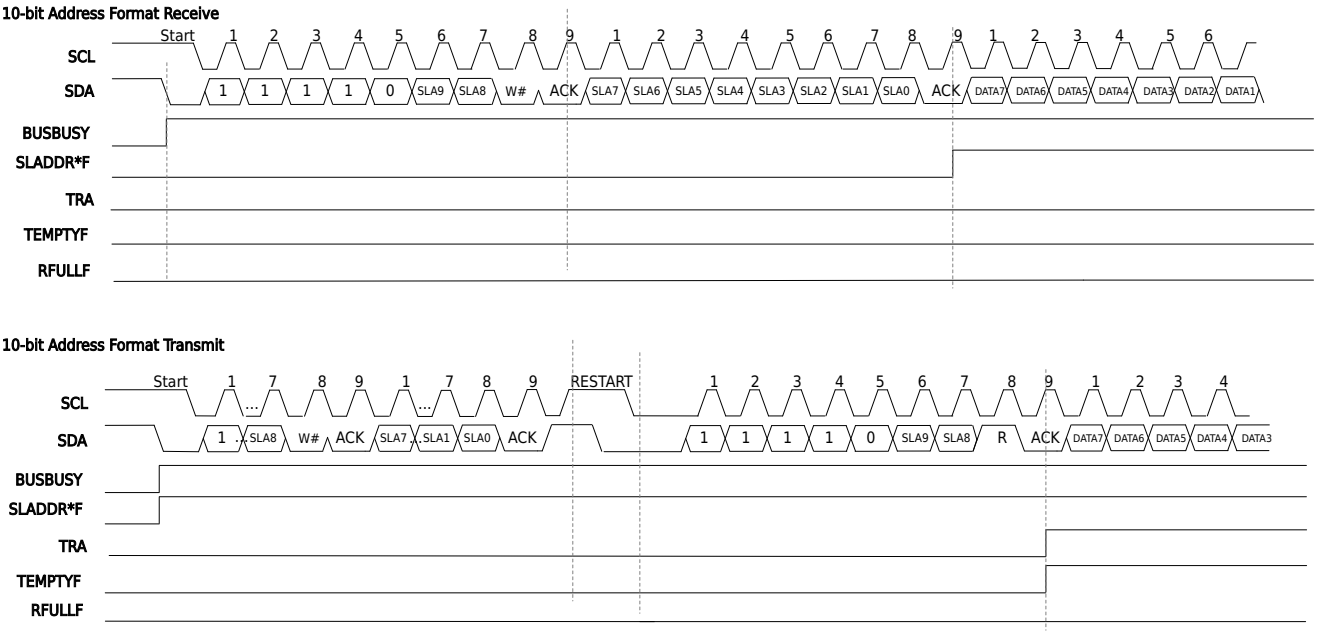

Figure 24-15 Timing when Selecting 10-bit Address Format

24.3.3.2 Broadcast Address Matching

When I2C_CR1.GCEN bit is 1, the broadcast address can be detected (0b0000000+0[W]).

But after the start condition or restart condition, the address is 0b0000000+1[R] (Start byte), which is considered the slave address of All "0" and not the broadcast address.

If the broadcast address is matched, the I2C_SR.GENCALLF flag is set to 1 at the rising edge of the 9th clock of SCL clock.

The operation after the broadcast address matches is the same as the ordinary slave receiving operation.

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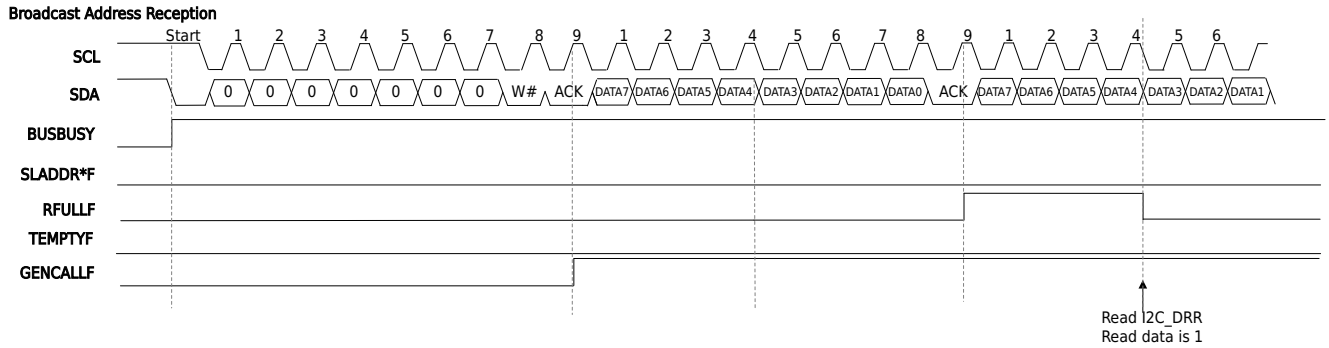

Figure 24-16 Broadcast Address Matching Timing Diagram

24.3.3.3 SMBus Master Address Matching

This product has the master address detection function when SMBus runs. If the I2C_CR1.SMBHOSTEN bit is set to 1 when the I2C_CR1.SMBUS bit is 1, the master address (0b0001000) can be detected in slave receive mode (I2C_SR.MSL=0 and I2C_SR.TRA=0).

If the SMBUS master address is detected, the I2C_SR.SMBHOSTF flag is set to 1 at the rising edge of the 9th clock of SCL clock.

Even if the bit following the SMBUS master address (0b0001000) is the Rd bit (R/W# bit receives 1), the SMBUS master address can be detected. The running of SMBUS master address detection is the same as that of normal slave mode.

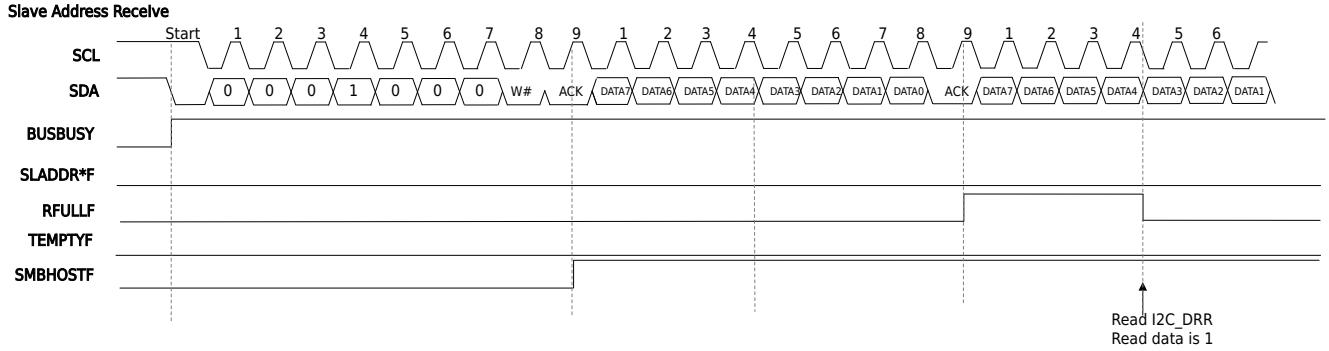

Figure 24-17 SMBus Master Address Matching Timing Diagram

24.3.3.4 SMBus Alarm Response Address Matching

This product has the function of alarm response address detection when SMBus is running. If the I2C_CR1.SMBALRTEN bit is set to 1 when the I2C_CR1.SMBUS bit is 1, the SMBUS alarm response address (0b0001100) can be detected in slave receive mode (I2C_SR.MSL=0 and I2C_SR.TRA=0).

If the SMBUS alarm response address is detected, the I2C_SR.SMBALRTF flag is set to 1 at the rising edge of the 9th clock of the SCL clock.

The operation of SMBUS alarm response address detection is the same as that of normal slave mode.

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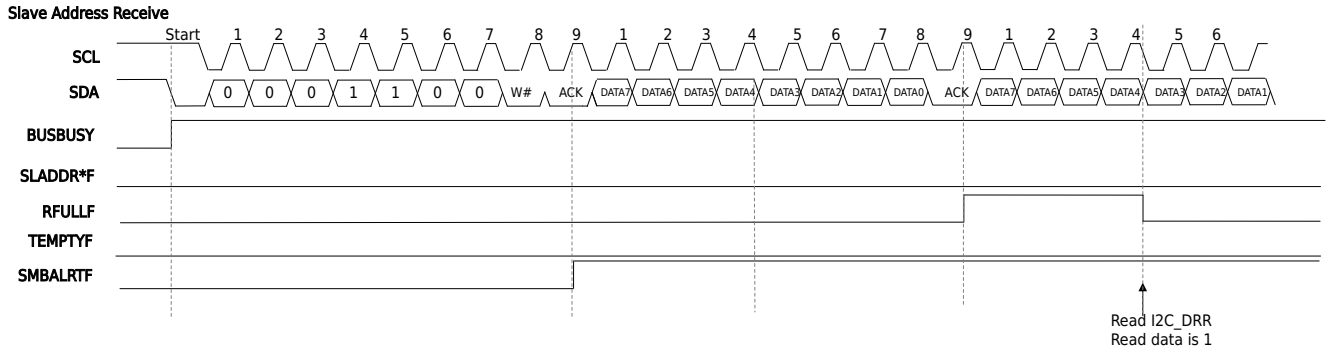

Figure 24-18 SMBus Alarm Response Address Matching Timing Diagram

24.3.3.5 SMBus Default Address Matching

This product has the default address detection function when SMBus runs. If the I2C_CR1.SMBDEFAULTEN bit is set to 1 when the I2C_CR1.SMBUS bit is 1, the SMBUS default address (0b1100001) can be detected in slave receive mode (I2C_SR.MSL=0 and I2C_SR.TRA=0).

If the SMBUS default address is detected, the I2C_SR.SMBDEFAULTF flag is set to 1 on the rising edge of the 9th clock of SCL clock.

The SMBUS default address detection runs the same as the normal slave mode.

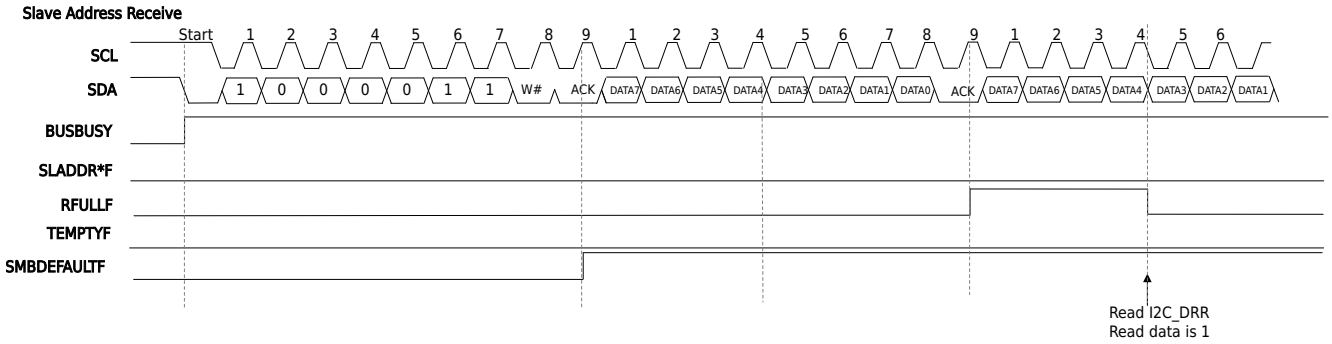

Figure 24-19 SMBus Default Address Timing Diagram

24.3.4 SMBus Action

This I2C interface can perform communication based on SMBus (Ver.2.0). When performing SMBus communication, I2C_CR1.SMBUS bit must be set to 1. The transmission speed must be set within the SMBus specification range of 10kbps to 100kbps by setting the I2C_CCR register.

24.3.4.1 SMBus Timeout Measurement

SCL Level Timeout Measurement

When working in slave mode, after the address match is consistent, it is detected that the low level or high level of the SCL line is fixed for more than a certain time, and the abnormal state of the bus is detected.

When working in the master mode, after the start condition is generated, it is detected that the low level or high level of SCL is fixed for more than a certain time, and the abnormal state of the bus is detected.

The timeout detection function monitors the state of the SCL line, and counts the time of high level or low level through the internal counter. If the SCL line changes (rising/falling), the internal counter is reset, otherwise it continues to count. If the internal counter counts up to the I2C_SLTR.TOUTHIGH/I2C_SLTR.TOUTLOW set value while the SCL line does not change, a timeout is detected and an abnormal state of the bus is notified.

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For the counting of the internal counter, it can select whether to count at the low level or high level of the SCL line by setting the I2C_CR3.HTMOUT and I2C_CR3.LTMOUT bits, or to count at both low and high levels. If both the I2C_CR3.HTMOUT and I2C_CR3.LTMOUT bits are set to 0, no internal counting will be performed.

Timeout Measurement of Slave

The slave device of SMBus communication needs to measure the interval shown below (timeout interval: $T_{LOW:SEXT}$):

- Interval from start condition to stop condition

When timeout is measured by the slave device, use the start condition to detect interrupt and stop condition to detect interrupt, and use the chip timer to measure the time from detection to start condition to detection to stop condition. This timeout measurement time must be within the SMBus specification clock low level accumulation time [slave device] $T_{LOW:SEXT}$: 25ms (max).

If the timer measures longer than the timeout of the SMBus specification clock low level detection $T_{TIMEOUT}$: 25ms (min), the slave needs to release the bus.

Timeout Measurement of Master

The main control device of SMBus communication needs to measure the interval shown below (timeout interval: $T_{LOW:MEXT}$):

- Interval from start condition to answer bit
- Interval from answer to next answer
- Interval from answer bit to stop condition

When the master performs timeout measurement, use the start condition to detect interrupt, stop condition to detect interrupt, send end interrupt or receive data full interrupt, and use the chip timer to measure the time between intervals. The timeout time must be within the accumulated time [master] $T_{LOW:MEXT}$: 10ms (max) of the clock low level in the SMBus specification, and the cumulative result of all $T_{LOW:MEXT}$ from the start condition to the stop condition must be within $T_{LOW:SEXT}$: 25ms (max).

If the time measured by the timer exceeds the cumulative time of the clock low level in the SMBus specification [master device] $T_{LOW:MEXT}$: 10ms (max), or the cumulative result of each measurement time exceeds the timeout of the clock low level detection in the SMBus specification $T_{TIMEOUT}$: 25ms (min), the master needs to terminate the processing. When sending a master, it must immediately abort the transmitting (write I2C_DTR register). Abort the master transaction by transmitting a stop condition.

24.3.4.2 Packet Error Code (PEC)

In communication, use the CPU to calculate the CRC, transmits the packet error code (PEC) of the SMBus, or checks the received data.

24.3.5 Reset

It has the function of resetting the communication module. There are two types of reset, one is communication reset: all registers inside I2C and internal state reset; the other is internal state reset: I2C_SR (including BUSY bit), internal shift register and internal state machine are reset.

After reset, the I2C_CR1.SWRST bit must be set to 0.

Because any kind of reset will remove the output state of the SCL pin /SDA pin and change it to a high-impedance state, it can also be used to remove the unexpected shutdown state of the bus.

The reset in the slave mode causes disparity with the master device, so try to avoid using it.

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Notice

During reset (I2C_CR1.PE=0 and I2C_CR1.SWRST=1), the bus status such as the start condition cannot be monitored.

24.3.6 Programmable Digital Filtering

The status of SCL pin and SDA pin is taken internally via analog filter circuit and digital filter. A block diagram of the digital filter circuit is shown below.

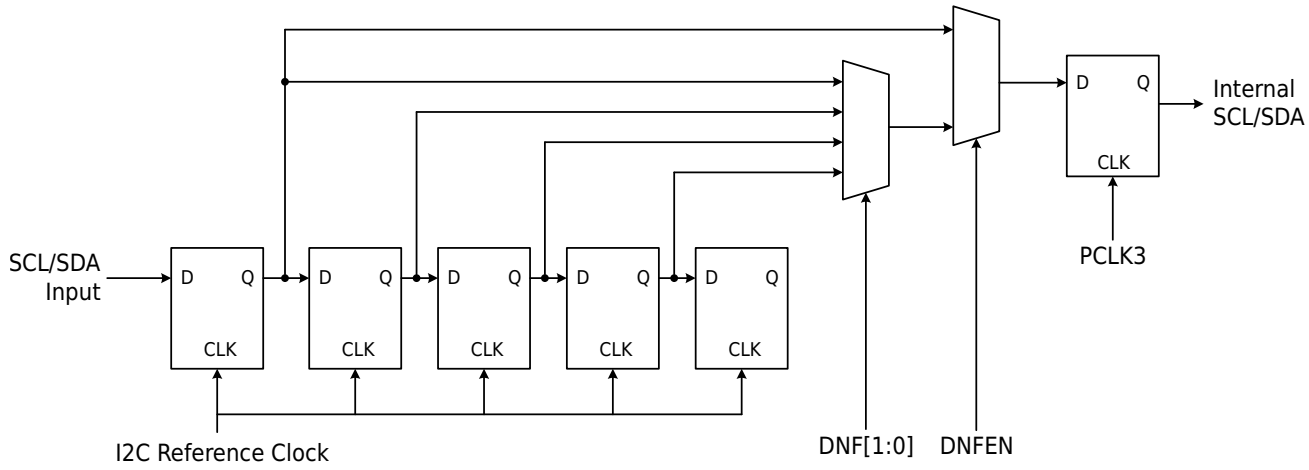

Figure 24-20 Digital Filtering Circuit Block Diagram

The internal digital filter circuit is composed of a four-segment series-connected trigger circuit and matching detection circuit.

The number of active segments of the digital filter is selected through the I2C_FLTR.DNF bit. According to the selected active segment number, the noise elimination capability is 1- 4 I2C periods.

The input signal of the SCL pin (or the input signal of the SDA pin) is sampled on the falling edge of the I2C internal clock. If the output of the trigger circuit with the number of active segments set by the I2C_FLTR.DNF bit all matches, the level is used as the internal signal to transmit, otherwise it keeps the original value.

24.3.7 Interrupt and Event

I2C has four interrupts and event outputs for triggering the activation of other peripheral circuits for user selection. Including: the occurrence of communication errors/events (arbitration failure detection, NACK detection, timeout detection, start condition detection, stop condition detection), end of receiving, transmitting data empty, end of transmitting.

The interrupt list is as follows.

Table 24-2 Interrupt List

Name	Interrupt Source	Interrupt Flag	Interrupt Condition
I2C_EEI	Communication Error/Communication Event	ARLOF	ARLOF=1&ARLOIE=1
		SLADDR0F	SLADDR0F=1&SLADDR0IE=1
		SLADDR1F	SLADDR1F=1&SLADDR1IE=1
		SMBALRTF	SMBALRTF=1&SMBALRTIE=1
		SMBHOSTF	SMBHOSTF=1&SMBHOSTFIE=1

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Name	Interrupt Source	Interrupt Flag	Interrupt Condition
I2C_EEI	Communication Error/Communication Event	SMBDEFAULTF	SMBDEFAULTF=1&SMBDEFAULTIE=1
		GENCALLF	GENCALLF=1&GENCALLIE=1
		NACKF	NACKF=1&NACKIE=1
		TMOUTF	TMOUTF=1&TMOUTIE=1
		STARTF	STARTF=1&STARTIE=1
		STOPF	STOPF=1&STOPIE=1
I2C_RXI	Receive Data Full	RFULLF	RFULLF=1&RFULLIE=1&-FEN
	Receive FIFO Data is not Empty	RFREQF	RFREQF=1&RFREQIE=1&FEN
I2C_TXI	Transmit Data Empty	TEMPTYF	TEMPTYF=1&TEMPTYIE=1
I2C_TEI	End of Transmit	TENDF	TENDF=1&TENDIE=1

The following table shows the output of the event signal.

Table 24-3 Event Signal Output List

Name	Event Source	Event Conditions
I2C_EEI	Communication Error/Communication Event	ARLOF=1
		SLADDR0F=1
		SLADDR1F=1
		SMBALRTF=1
		SMBHOSTF=1
		SMBDEFAULTF=1
		GENCALLF=1
		NACKF=1
		TMOUTF=1
		STARTF=1
		STOPF=1
I2C_RXI	Receive Data Full	RFULLF=1
I2C_TXI	Transmit Data Empty	TEMPTYF=1
I2C_TEI	End of Transmit	TENDF=1

24.4 Operation Example

24.4.1 I2C Initialization Process

When start transmitting or receiving data, it must follow the steps below to initialize:

Step1. I2C_CR1.PE bit is set to 0;

Step2. Set I2C_CR1.SWRST to 1, communication reset;

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Step3. I2C_CR1.PE bit set to 1, internal state reset;

Step4. Set slave address format and address;

Step5. Set baud rate;

Step6. Set control register function and interrupt as needed;

Step7. I2C_CR1.SWRST bit is set to 0 to cancel internal state reset;

Step8. The initialization ends. Can transmit and receive data.

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24.5 Register Description

24.5.1 Register List

Base address: 0x4004E000

Table 24-4 Inter-Integrated Circuit (I2C) Register Offset

Offset	Register	Description	Width
0x00	I2C_CR1	I2C Control Register 1	32
0x04	I2C_CR2	I2C Control Register 2	32
0x08	I2C_CR3	I2C Control Register 3	32
0x0C	I2C_CR4	I2C Control Register 4	32
0x10	I2C_SLR0	I2C Slave Address Register 0	32
0x14	I2C_SLR1	I2C Slave Address Register 1	32
0x18	I2C_SLTR	I2C SCL Level Timeout Control Register	32
0x1C	I2C_SR	I2C Status Register	32
0x20	I2C_CLR	I2C Status Clear Register	32
0x24	I2C_DTR	I2C Data Transmit Register	8
0x28	I2C_DRR	I2C Data Receive Register	8
0x2C	I2C_CCR	I2C Clock Control Register	32
0x30	I2C_FLTR	I2C Filter Control Register	32
0x34	I2C_FSTR	I2C FIFO Status Register	32
0x38	I2C_SLVADRR	I2C Slave Address Receive Register	32

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24.5.2 I2C Control Register 1 (I2C_CR1)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000040																															
Name	Reserved																SWRST	Reserved				ACK	STOP	START	RESTART	GCEN	Reserved	SMBHOSTEN	SMBDEFAULTEN	SMBALRTEN	SMBUS	PE
Access																	RW					RW	RW	RW	RW	RW		RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15	SWRST	Software Reset ● 0b0: Release reset ● 0b1: Software reset By combining with the PE bit, select internal status reset or communication reset: SWRST / PE / Reset Content 0b1 / 0b0 / Communication reset: reset all registers and internal status of I2C 0b1 / 0b1 / Internal status reset: I2C_SR (including BUSY bit), internal shift register and internal status machine are reset	RW
14:11	*Reserved*	-	-
10	ACK	Send Answer ● 0b0: The answer bit sends "0" (sends ACK) ● 0b1: The answer bit sends "1" (sends NACK)	RW
9	STOP	Stop Condition Generation Bit ● 0b0: No stop condition is generated ● 0b1: Generate stop condition This bit can be set and cleared by software. Hardware clear condition: ● Stop condition detected ● Failure to arbitrate ● Start condition detected ● Communication reset	RW

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Bit	Name	Functional Description	Access
8	START	Start Condition Generating Bit ● 0b0: No start condition generated ● 0b1: Start condition generated This bit can be set and cleared by software. Hardware clear condition: ● Start condition detected ● Failure of arbitration ● Communication reset	RW
7	RESTART	Repeated Start Condition Generating Bit ● 0b0: No repeated start condition generated ● 0b1: Repeated start condition generated This bit can be set and cleared by software. Hardware clear condition: ● Start condition detected ● Failure of arbitration ● Communication reset	RW
6	GCEN	Broadcast Call Enabled ● 0b0: Broadcast address detection disabled ● 0b1: Broadcast address detection enabled	RW
5	*Reserved*	-	-
4	SMBHOSTEN	Allow Matching of SMBUS Master Address Bit ● 0b0: SMBUS master address match disabled ● 0b1: SMBUS master address match enabled	RW
3	SMBDEFAULTEN	Allow Matching of SMBUS Default Address Bit ● 0b0: SMBUS default address match disabled ● 0b1: SMBUS default address match enabled	RW
2	SMBALRTEN	Allow Matching of SMBUS Alarm Response Address Bit ● 0b0: SMBUS alarm response address match disabled ● 0b1: SMBUS alarm response address match enabled	RW
1	SMBUS	SMBUS/I2C Bus Mode Selection Bit ● 0b0: I2C bus mode ● 0b1: SMBUS mode	RW
0	PE	I2C Function Enabled By combining with the SWRST bit, select internal status reset or communication reset: ● 0b0: I2C function disabled ● 0b1: I2C function enabled	RW

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24.5.3 I2C Control Register 2 (I2C_CR2)

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved								SMBALRTIE	SMBHOSTIE	SMBDEFAULTIE	GENCALLIE	Reserved					TMOUTIE	Reserved	NACKIE	RFREQIE	Reserved	ARLOIE	Reserved	TEMPTYIE	RFULLIE	Reserved	STOPIE	TENDIE	SLADDR1IE	SLADDR0IE	STARTIE
Access									RW	RW	RW	RW						RW		RW	RW		RW		RW	RW		RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:24	*Reserved*	-	-
23	SMBALRTIE	SMBUS Alarm Response Address Matching Consistent Interrupt Enabled ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW
22	SMBHOSTIE	SMBUS Master Address Matching Consistent Interrupt Enabled ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW
21	SMBDEFAULTIE	SMBUS Default Address Matching Consistent Interrupt Enabled ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW
20	GENCALLIE	Broadcast Call Address Matching Consistent Interrupt Enabled ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW
19:15	*Reserved*	-	-
14	TMOUTIE	Timeout Interrupt Enabled ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW
13	*Reserved*	-	-
12	NACKIE	NACK Interrupt Enabled ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW
11	RFREQIE	FIFO Receive Request Interrupt Enabled ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW
10	*Reserved*	-	-
9	ARLOIE	Arbitration Failure Interrupt Enabled ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW

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Bit	Name	Functional Description	Access
8	*Reserved*	-	-
7	TEMPTYIE	Transmit Data Empty Interrupt Enabled ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW
6	RFULLIE	Receive Data Full Interrupt Enabled ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW
5	*Reserved*	-	-
4	STOPIE	Stop Condition Interrupt Enabled ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW
3	TENDIE	Send a Frame of Data End Interrupt Enabled ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW
2	SLADDR1IE	Slave Address 1 Match Consistent Interrupt Enabled ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW
1	SLADDR0IE	Slave Address 0 Match Consistent Interrupt Enabled ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW
0	STARTIE	Start Condition/Repeated Start Condition Interrupt Enabled ● 0b0: Interrupt disabled ● 0b1: Interrupt enabled	RW

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24.5.4 I2C Control Register 3 (I2C_CR3)

Offset	Bit Position																													
0x08	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000006																															
Name	Reserved																								FACKEN	Reserved				HTMOUT	LTMOUT	TMOUTEN
Access																									RW					RW	RW	RW

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7	FACKEN	Time Point Selection of RFULLF Flag Bit Set ● 0b0: When the 9th clock of SCL clock rises, the RFULLF flag is "1" (at the falling edge of the 8th clock, the SCL line does not remain at a low level) ● 0b1: When the 8th clock of SCL clock rises, the RFULLF flag is "1" (at the falling edge of the 8th clock, the SCL line remains at a low level) **Note** Remove the held low level by writing the ACK bit.	RW
6:3	*Reserved*	-	-
2	HTMOUT	High Level Timeout Detection Enabled ● 0b0: Timeout detection disabled when SCL is high level ● 0b1: Timeout detection enabled when SCL is high level	RW
1	LTMOUT	Low Level Timeout Detection Enabled ● 0b0: Timeout detection disabled when SCL is low level ● 0b1: Timeout detection enabled when SCL is low level	RW
0	TMOUTEN	Timeout Function Enable Bit ● 0b0: SCL level timeout detection function disabled ● 0b1: SCL level timeout detection function enabled	RW

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24.5.5 I2C Control Register 4 (I2C_CR4)

Offset	Bit Position																													
0x0C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00301B07																															
Name	Reserved												SDADLY				Reserved			BUSFREE_CLREN	NACKTRA_CLREN	BUSWAIT	Reserved									
Access													RW							RW	RW	RW										

Bit	Name	Functional Description	Access
31:22	*Reserved*	-	-
21:20	*Reserved*	*All bits read as 1, Write as 1*	-
19:16	SDADLY	SDA Output Delay Counter ● 0b0000: No output delay ● 0b0001: 1 I2C reference clock period ● 0b0010: 2 I2C reference clock periods ● ..... ● 0b1111: 15 I2C reference clock periods	RW
15:13	*Reserved*	-	-
12	BUSFREE_CLREN	Bus End Status Clear Bit ● 0b0: Disable the I2C bus STOP flag to clear the SMBALRTF, SMBHOSTF, SMBDEFAULTF, GENCALLF, MSL, TENDF, SLADDR1F, SLADDR0F, and STARTF bits in the I2C_SLVADRR slave receive address register and the I2C_SR status register. ● 0b1: Enable the I2C bus STOP flag to clear the SMBALRTF, SMBHOSTF, SMBDEFAULTF, GENCALLF, MSL, TENDF, SLADDR1F, SLADDR0F, and STARTF bits in the I2C_SLVADRR slave receive address register and the I2C_SR status register.	RW
11	NACKTRA_CLREN	Slave Transit Clear Enable ● 0b0: Slave does not clear the I2C_SR.TRA bit after receiving NACK ● 0b1: Slave clears the I2C_SR.TRA bit after receiving NACK	RW

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Bit	Name	Functional Description	Access
10	BUSWAIT	Bus Wait Bit ● 0b0: When I2C_DRR is full and the internal shift register is empty, it does not maintain a low level between the 9th clock and the 1st clock of the next transmission, and continues to receive the next data ● 0b1: When I2C_DRR is full and the internal shift register is empty, it maintains a low level between the 9th clock and the 1st clock of the next transmission. The low level is released by reading the I2C_DRR register.	RW
9:8	*Reserved*	*All bits read as 1, Write as 1*	-
7:3	*Reserved*	-	-
2:0	*Reserved*	*All bits read as 1, Write as 1*	-

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24.5.6 I2C Slave Address Register 0 (I2C_SLR0)

Offset	Bit Position																													
0x10	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00001000																															
Name	Reserved					MASK0EN	MSLADDR0										ADDRMOD0	Reserved		SLADDR0EN	Reserved		SLADDR0								
Access						RW	RW										RW			RW			RW								

Bit	Name	Functional Description	Access
31:27	*Reserved*	-	-
26	MASK0EN	Slave Address 0 Mask Enable Bit ● 0b0: The slave address register 0 mask setting disabled ● 0b1: The slave address register 0 mask setting enabled	RW
25:24	MSLADDR0[9:8]	10-bit Slave Address High Mask Address Set the high mask address of the slave address 0: ● When MASK0EN=0, the mask set by MSLADDR0[9:8] is invalid. ● When MASK0EN=1, the mask set by MSLADDR0[9:8] is valid. Its valid range is positively correlated with the value set by ADDRMOD0, namely: ▶ When ADDRMOD0=0, MSLADDR0[9:8] bits disabled; ▶ When ADDRMOD0=1, MSLADDR0[9:8] is the mask address of the upper two bits of the 10-bit slave address.	RW
23:16	MSLADDR0[7:0]	7-bit Address/10-bit Address Low Mask Address Set the low mask address of the slave address 0: ● When MASK0EN=0, the mask set by MSLADDR0[7:0] is invalid. ● When MASK0EN=1, the mask set by MSLADDR0[7:0] is valid. Its valid range is positively correlated with the value set by ADDRMOD0, namely: ▶ When ADDRMOD0=0, MSLADDR0[7:1] is the 7-bit slave address mask, and MSLADDR0[0] bit is disabled; ▶ When ADDRMOD0=1, MSLADDR0[7:0] is the lower 8-bit address mask of the 10-bit slave address.	RW
15	ADDRMOD0	7-bit/10-bit Address Format Selection Bit ● 0b0: Select 7-bit address format ● 0b1: Select 10-bit address format	RW
14:13	*Reserved*	-	-
12	SLADDR0EN	Slave Address 0 Enabled Bit ● 0b0: Slave address register 0 setting value disabled ● 0b1: Slave address register 0 setting value enabled	RW
11:10	*Reserved*	-	-

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Bit	Name	Functional Description	Access
9:8	SLADDR0[9:8]	High Bit of a 10-bit Slave Address Set the slave address: ● When ADDRMOD0=0, the SLADDR0[9:8] setting is invalid; ● When ADDRMOD0=1, SLADDR0[9:8] is the upper two bits of the 10-bit slave address.	RW
7:0	SLADDR0[7:0]	Lower Bits of 7-bit Address/10-bit Address Set the slave address: ● When ADDRMOD0=0, SLADDR0[7:1] is the 7-bit slave address, and SLADDR0[0] is invalid; ● When ADDRMOD0=1, SLADDR0 [7:0] is the lower 8 bits of the 10-bit slave address.	RW

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24.5.7 I2C Slave Address Register 1 (I2C_SLR1)

Offset	Bit Position																													
0x14	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved					MASK1EN	MSLADDR1										ADDRMOD1	Reserved		SLADDR1EN	Reserved		SLADDR1									
Access						RW	RW										RW			RW			RW								

Bit	Name	Functional Description	Access
31:27	*Reserved*	-	-
26	MASK1EN	Slave Address 1 Mask Enable Bit ● 0b0: The slave address register 1 mask setting disabled ● 0b1: The slave address register 1 mask setting enabled	RW
25:24	MSLADDR1[9:8]	10-bit Slave Address High Mask Address Set the high mask address of the slave address 1: ● When MASK1EN=0, the mask set by MSLADDR1[9:8] is invalid. ● When MASK1EN=1, the mask set by MSLADDR1[9:8] is valid. Its valid range is positively correlated with the value set by ADDR-MOD 1, namely: ▶ When ADDRMOD1=0, MSLADDR1[9:8] bits disabled; ▶ When ADDRMOD1=1, MSLADDR1[9:8] is the mask address of the upper two bits of the 10-bit slave address.	RW
23:16	MSLADDR1[7:0]	7-bit Address/10-bit Address Low Mask Address Set the low mask address of the slave address 1: ● When MASK1EN=0, the mask set by MSLADDR1[7:0] is invalid. ● When MASK1EN=1, the mask set by MSLADDR1[7:0] is valid. Its valid range is positively correlated with the value set by ADDR-MOD1, namely: ▶ When ADDRMOD1=0, MSLADDR1[7:1] is the 7-bit slave address mask, and MSLADDR1[0] bit is invalid; ▶ When ADDRMOD1= 1, MSLADDR1[7:0] is the low 8-bit address mask of the 10-bit slave address.	RW
15	ADDRMOD1	7-bit/10-bit Address Format Selection Bit ● 0b0: Select 7-bit address format ● 0b1: Select 10-bit address format	RW
14:13	*Reserved*	-	-
12	SLADDR1EN	Slave Address 1 Enable Bit ● 0b0: Slave address register 1 setting value disabled ● 0b1: Slave address register 1 setting value enabled	RW
11:10	*Reserved*	-	-

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Bit	Name	Functional Description	Access
9:8	SLADDR1[9:8]	High Bit of a 10-bit Slave Address Set the slave address: ● When ADDRMOD1=0, the SLADDR1[9:8] setting is invalid; ● When ADDRMOD1=1, the SLADDR1[9:8] is the upper two bits of the 10-bit slave address.	RW
7:0	SLADDR1[7:0]	Low Bits of 7-bit Address/10-bit Address Set the slave address: ● When ADDRMOD1=0, SLADDR1[7:1] is the 7-bit slave address, and SLADDR1[0] is invalid; ● When ADDRMOD1=1, SLADDR1[7:0] is the low 8 bits of the 10-bit slave address.	RW

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24.5.8 I2C SCL Level Timeout Control Register (I2C_SLTR)

Offset	Bit Position																													
0x18	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFFFFFFFF																															
Name	TOUTHIGH																TOUTLOW															
Access	RW																RW															

Bit	Name	Functional Description	Access
31:16	TOUTHIGH	SCL High Level Timeout Period SCL high level timeout time=TOUTHIGH*I2C reference clock period	RW
15:0	TOUTLOW	SCL Low Level Timeout Period SCL low level timeout time=TOUTLOW*I2C reference clock period	RW

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24.5.9 I2C Status Register (I2C_SR)

Offset	Bit Position																														
0x1C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x05000000																															
Name	RFREQ	Reserved	TFST		RFFULL	RFEMPTY	TFFULL	TFEMPTY	SMBALRTF	SMBHOSTF	SMBDEFAULTF	GENCALLF	Reserved	TRA	BUSY	MSL	Reserved	TMOUTF	Reserved	NACKF	Reserved	ACKRF	ARLOF	Reserved	TEMPTYF	RFULLF	Reserved	STOPF	TENDF	SLADDR1F	SLADDR0F	STARTF
Access	RO		RO		RO	RO	RO	RO	RO	RO	RO	RO		RW	RO	RW		RO		RO		RO	RO		RO	RO		RO	RO	RO	RO	RO

Bit	Name	Functional Description	Access
31	RFREQ	Receive FIFO Request Flag Bit ● 0b0: Current receive FIFO without enable data ● 0b1: Current receive FIFO with enable data	RO
30	*Reserved*	-	-
29:28	TFST	Transmit FIFO Status Flag Bit ● 0b00: Current transmit FIFO is empty ● 0b01: Current transmit FIFO with 1 Byte enable data ● 0b10: Current transmit FIFO with 2 Bytes enable data ● 0b11: Reserved	RO
27	RFFULL	Receive FIFO Full Flag Bit ● 0b0: Current receive FIFO not full ● 0b1: Current receive FIFO full	RO
26	RFEMPTY	Receive FIFO Empty Flag Bit ● 0b0: Current receive FIFO not empty ● 0b1: Current receive FIFO empty	RO
25	TFFULL	Transmit FIFO Full Flag Bit ● 0b0: Current transmit FIFO not full ● 0b1: Current transmit FIFO full	RO
24	TFEMPTY	Transmit FIFO Empty Flag Bit ● 0b0: Current transmit FIFO not empty ● 0b1: Current transmit FIFO is empty	RO
23	SMBALRTF	SMBUS Alarm Response Address Matching Consistent Flag Bit ● 0b0: SMBUS alarm response address not matched ● 0b1: Master address detected Set condition: ● Received address matches 0b0001100 Clear condition: ● SMBALRTFCLR writes "1" ● Stop condition detected ● Communication reset ● Internal state reset	RO

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<table>
<tr><th>Bit</th><th>Name</th><th>Functional Description</th><th>Access</th></tr>
<tr><td>22</td><td>SMBHOSTF</td><td>SMBUS Master Address Matching Consistent Flag Bit
● 0b0: No match to SMBUS master address
● 0b1: Match to SMBUS master address
Set condition:
● Received address matches 0b0001000
Clear condition:
● SMBHOSTFCLR writes "1"
● Stop condition detected
● Communication reset
● Internal state reset</td><td>RO</td></tr>
<tr><td>21</td><td>SMBDEFAULTF</td><td>SMBUS Default Address Matching Consistent Flag Bit
● 0b0: No match with the SMBUS default address.
● 0b1: A match with the SMBUS default address.
Set condition:
● Received address matches 0b1100001
Clear condition:
● SMBDEFAULTFCLR Write "1"
● Stop condition detected
● Communication reset
● Internal state reset</td><td>RO</td></tr>
<tr><td>20</td><td>GENCALLF</td><td>Broadcast Call Address Matching Consistent Flag Bit
● 0b0: No match with the broadcast call address.
● 0b1: A match with the broadcast call address.
Set condition:
● The received slave address matches the broadcast call address (All "0")
Clear condition:
● GENCALLFCLR write "1"
● Stop condition detected
● Communication reset
● Internal state reset</td><td>RO</td></tr>
<tr><td>19</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>18</td><td>TRA</td><td>Transmit Receive Selection Bit
● 0b0: Receive data
● 0b1: Transmit data
The operating mode of I2C is represented by a combination of MSL bits:
<table><tr><th>MSL</th><th>TRA</th><th>I2C operating mode</th></tr><tr><td>0b0</td><td>0b0</td><td>Slave receive mode</td></tr><tr><td>0b0</td><td>0b1</td><td>Slave transmit mode</td></tr><tr><td>0b1</td><td>0b0</td><td>Master receive mode</td></tr><tr><td>0b1</td><td>0b1</td><td>Master transmit mode</td></tr></table>
This bit can be set and cleared by software.
Hardware set condition:
● Start condition detected</td><td>RW</td></tr>
</table>

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Bit	Name	Functional Description	Access
18	TRA	● In master mode, the transmitted RW bit is 0 ● In slave mode, the address matches and the received RW bit is 1 Hardware clear condition: ● Stop condition detected ● In master mode, the transmitted RW bit is 1 ● In slave mode, the address matches and the received RW bit is 0 ● Communication reset ● Internal state reset	RW
17	BUSY	Bus Busy Flag Bit ● 0b0: Idle state, no communication on the bus ● 0b1: Occupied state, the bus is communicating Set condition: ● Start condition detected on bus Clear condition: ● Bus stop condition detected ● Communication reset	RO
16	MSL	Master-slave Selection Bit ● 0b0: Slave mode ● 0b1: Master mode The operating mode of I2C is represented by a combination of TRA bits. This bit can be set and cleared by software. Hardware set conditions: ● Start condition detected when START bit is 1 Hardware clear condition ● Stop condition detected ● Failure to arbitrate ● Communication reset ● Internal state reset	RW
15	*Reserved*	-	-
14	TMOUTF	Timeout Flag Bit ● 0b0: SCL level timeout not detected ● 0b1: SCL level timeout Set condition: ● During the period set by I2C_SLTR, SCL is not inverted Clear condition: ● TMOUTFCLR writes "1" ● Communication reset ● Internal state reset	RO
13	*Reserved*	-	-

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Bit	Name	Functional Description	Access
12	NACKF	NACK Flag Bit ● 0b0: NACK not received ● 0b1: NACK received Set condition: ● Receive NACK in transmit mode Clear condition: ● NACKFCLR writes "1" ● Communication reset ● Internal state reset	RO
11	*Reserved*	-	-
10	ACKRF	Receive Acknowledge Bit ● 0b0: The received acknowledge bit is "0" (receive ACK) ● 0b1: The received acknowledge bit is "1" (receive NACK) Set condition: ● Receive NACK in transmit mode Clear condition: ● Receive ACK in transmit mode ● Communication reset ● Internal state reset	RO
9	ARLOF	Arbitration Failure Flag Bit ● 0b0: No arbitration failure occurred ● 0b1: Arbitration failure Set condition: ● Failure to arbitrate Clear condition: ● ARLOFCLR writes "1" ● Communication reset ● Internal state reset	RO
8	*Reserved*	-	-
7	TEMPTYF	Transmit Data Empty Flag Bit ● 0b0: I2C_DTR register full ● 0b1: I2C_DTR register empty Set condition: ● I2C_DTR data is transferred to the internal shift register ● TRA bit set to 1 Clear condition: ● Write I2C_DTR ● TRA bit clear 0 ● Communication reset ● Internal state reset	RO

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Bit	Name	Functional Description	Access
6	RFULLF	Receive Data Full Flag Bit ● 0b0: I2C_DRR register empty ● 0b1: I2C_DRR register full Set condition: ● The received data is transferred from the internal shift register to I2C_DRR Clear condition: ● Read I2C_DRR ● RFULLFCLR writes "1" ● Communication reset ● Internal state reset	RO
5	*Reserved*	-	-
4	STOPF	Stop Condition Flag Bit ● 0b0: No STOP condition has been detected on the bus. ● 0b1: A STOP condition has been detected on the bus. Set condition: ● Stop condition detected Clear condition: ● STOPFCLR writes "1" ● Communication reset ● Internal state reset	RO
3	TENDF	Transmit Data End Flag Bit ● 0b0: The internal shift register is still transmitting data. ● 0b1: The internal shift register has finished transmitting data. Set condition: ● Under the condition of TEMPTYF=1, the 9th rising edge of SCL is "1" Clear condition: ● Stop condition detected ● Write I2C_DTR ● TENDFCLR writes "1" ● Communication reset ● Internal state reset	RO
2	SLADDR1F	Slave Address Register 1 Matching Consistent Mark Bit ● 0b0: No consistent address was detected in the slave address register 1. ● 0b1: A consistent address is detected in the slave address register 1. Set condition: ● When I2C_SLR1.ADDRMOD1=0, the received slave address is matched with the I2C_SLR1.SLADDR1[7:1]. ● When I2C_SLR1.ADDRMOD1=1, the first byte address of the received 10-bit slave address matches 0b11110+I2C_SLR1.SLADDR1[9:8] and the second byte address matches I2C_SLR1.SLADDR1[7:0] Clear condition: ● Stop condition detected ● SLADDR1FCLR writes "1"	RO

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Bit	Name	Functional Description	Access
2	SLADDR1F	● Communication reset ● Internal state reset	RO
1	SLADDR0F	Slave Address Register 0 Matching Consistent Mark Bit ● 0b0: No consistent address was detected in the slave address register 0. ● 0b1: A consistent address is detected in the slave address register 0. Set condition: ● When I2C_SLR0.ADDRMOD0=0, the received slave address is compared with the I2C_SLR0.SLADDR0[7:1]. ● When I2C_SLR0.ADDRMOD0=1, the first byte address of the received 10-bit slave address matches 0b11110 + I2C_SLR0.SLADDR0 [9: 8] and the second byte address matches I2C_SL0.SLADDR0 [7: 0] Clear condition: ● Stop condition detected ● SLADDR0FCLR writes "1" ● Communication reset ● Internal state reset	RO
0	STARTF	Start Condition/Restart Condition Flag Bit ● 0b0: Bus not detected starting condition ● 0b1: Bus detected starting condition Set condition: ● Start condition detected Clear condition: ● Stop condition detected ● STARTFCLR writes "1" ● Communication reset ● Internal state reset	RO

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24.5.10 I2C Status Clear Register (I2C_CLR)

Offset	Bit Position																													
0x20	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved								SMBALRTFCLR	SMBHOSTFCLR	SMBDEFAULTFCLR	GENCALLFCLR	Reserved					TMOUTFCLR	Reserved	NACKFCLR	Reserved	RFREQCLR	ARLOFCLR	Reserved		RFULLFCLR	Reserved	STOPFCLR	TENDFCLR	SLADDR1FCLR	SLADDR0FCLR	STARTFCLR
Access									WO	WO	WO	WO						WO		WO		WO	WO			WO		WO	WO	WO	WO	WO

Bit	Name	Functional Description	Access
31:24	*Reserved*	-	-
23	SMBALRTFCLR	SMBUS Alarm Response Address Matching Consistent Flag Clear Write 1 to clear the SMBALRTF flag bit, write 0 has no effect	WO
22	SMBHOSTFCLR	SMBUS Master Address Matching Consistent Flag Clear Write 1 to clear the SMBHOSTF flag bit, write 0 has no effect	WO
21	SMBDEFAULTFCLR	SMBUS Default Address Matching Consistent Flag Clear Write 1 to clear the SMBDEFAULTF flag bit, write 0 has no effect	WO
20	GENCALLFCLR	Broadcast Call Address Matching Flag Clear Write 1 to clear the GENCALLF flag bit, write 0 has no effect	WO
19:15	*Reserved*	-	-
14	TMOUTFCLR	Timeout Flag Clear Write 1 to clear the TMOUTF flag bit, write 0 has no effect	WO
13	*Reserved*	-	-
12	NACKFCLR	NACK Flag Clear Write 1 to clear the NACKF flag bit, write 0 has no effect	WO
11	*Reserved*	-	-
10	RFREQCLR	Receive FIFO Data Request Flag Clear Write 1 to clear the RFREQF flag bit, write 0 has no effect	WO
9	ARLOFCLR	Arbitration Lost Flag Clear Write 1 to clear the ARLOF flag bit, write 0 has no effect	WO
8:7	*Reserved*	-	-
6	RFULLFCLR	Receive Data Full Flag Clear Write 1 to clear the RFULLF flag bit, write 0 has no effect	WO

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Bit	Name	Functional Description	Access
5	*Reserved*	-	-
4	STOPFCLR	Stop Condition Flag Clear Write 1 to clear the STOPF flag bit, write 0 has no effect	WO
3	TENDFCLR	Transmit Data End Flag Clear Write 1 to clear the TENDF flag bit, write 0 has no effect	WO
2	SLADDR1FCLR	Slave Address Register 1 Matching Consistent Flag Clear Write 1 to clear the SLADDR1F flag bit, write 0 has no effect	WO
1	SLADDR0FCLR	Slave Address Register 0 Matching Consistent Flag Clear Write 1 to clear the SLADDR0F flag bit, write 0 has no effect	WO
0	STARTFCLR	Start Condition/Restart Condition Flag Clear Write 1 to clear the STARTF flag bit, write 0 has no effect	WO

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24.5.11 I2C Data Transmit Register (I2C_DTR)

Offset	Bit Position							
0x24	7	6	5	4	3	2	1	0
Reset	0xFF							
Name	DT							
Access	RW							

Bit	Name	Functional Description	Access
7:0	DT	Transmit Data If the internal shift register is empty, the data written to the I2C_DTR register will be transferred to the internal shift register. In transmit mode, the data transmission to the SDA line begins	RW

The internal shift register and the I2C_DTR register form a double-buffered structure. During the data transmission of the internal shift register, if data is written in advance to the I2C_DTR register, continuous data transmission can be achieved.

The I2C_DTR register is readable and writable. Write I2C_DTR register only once when the transmit data is empty interrupt request occurs.

When the I2C operates in FIFO mode, accessing the I2C_DTR register address allows direct access to the transmit FIFO. If the current TEMPTYF flag is enabled, a write operation to the I2C_DTR register address writes the current bus data into the transmit FIFO. When the transmit FIFO is enabled and the I2C is enabled to transmit, data from the transmit FIFO is transferred to the internal shift register, and data transmission to the SDA line begins.

The selection of the transmit data source is determined by the FEN bit in the FIFO Status Register (I2C_FSTR) in I2C :

- When FEN is 1, the path from the external data bus to the FIFO and from the FIFO to the internal shift register is selected.
- When FEN is 0, the path from the external data bus to the I2C_DTR register and from the I2C_DTR register to the internal shift register is selected.

By default, the non-FIFO mode is selected.

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24.5.12 I2C Data Receive Register (I2C_DRR)

Offset	Bit Position							
0x28	7	6	5	4	3	2	1	0
Reset	0x00							
Name	DR							
Access	RO							

Bit	Name	Functional Description	Access
7:0	DR	Receive Data If a frame of data is received, the received data can be transferred from the internal shift register to the I2C_DRR register, and then into the next data receiving state	RO

The internal shift register and the I2C_DRR register form a double-buffered structure. During data reception in the internal shift register, if the data in the I2C_DRR register is read, continuous data reception can be achieved.

Do not write to I2C_DRR register. Read I2C_DRR register only once when the receive data full interrupt request occurs.

When the I2C_SR.RFULLF flag is set to 1 and the data in the I2C_DRR register is not read before the next data is received, the SCL clock will be automatically held low after the 7th or 8th falling edge during data reception (refer to the slave receive timing diagram and the fast ACK/NACK timing diagram), until the data in the I2C_DRR register is read.

When the I2C operates in FIFO mode, accessing the I2C_DRR register address directly accesses the receive FIFO:

- If one frame of data is received, the received data will be transferred from the internal shift register to the receive FIFO. Once the receive FIFO has received active data, an RFREQ request status signal will be asserted. At this point, a read operation to the I2C_DRR register address directly accesses the data in the receive FIFO.
- When the I2C_SR.RFULLF flag is set to 1 (i.e., the receive FIFO has stored 2 bytes of data and FIFO is full), and if the data in the receive FIFO is not read before the next data is received, the SCL clock will be automatically held low after the 7th or 8th falling edge of the received data, until the data in the receive FIFO is read.

The receive data path of the I2C is selected through the FEN bit in the I2C FIFO Status Register (I2C_FSTR) :

- When FEN is 1, the data path from the internal shift register to the receive FIFO and from the receive FIFO to the data bus is selected.
- When FEN is 0, the data path from the internal shift register to the I2C_DRR register and from the I2C_DRR register to the data bus is selected.

By default, the non-FIFO mode is selected.

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24.5.13 I2C Clock Control Register (I2C_CCR)

Offset	Bit Position																													
0x2C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00001F1F																															
Name	Reserved																	CKDIV			SHIGHW							SLOWW			
Access																		RW			RW							RW			

Bit	Name	Functional Description	Access
31:19	*Reserved*	-	-
18:16	CKDIV	Setting Bit of I2C Reference Clock Frequency ● 0b000: I2C Reference Clock Frequency=PCLK3 ● 0b001: I2C Reference Clock Frequency=PCLK3/2 ● 0b010: I2C Reference Clock Frequency=PCLK3/4 ● 0b011: I2C Reference Clock Frequency=PCLK3/8 ● 0b100: I2C Reference Clock Frequency=PCLK3/16 ● 0b101: I2C Reference Clock Frequency=PCLK3/32 ● 0b110: I2C Reference Clock Frequency=PCLK3/64 ● 0b111: I2C Reference Clock Frequency=PCLK3/128	RW
15:8	SHIGHW	Set SCL High Level Width Bit Setting the high level width of SCL clock	RW
7:0	SLOWW	Set SCL Low Level Width Bit Setting the low level width of SCL clock	RW

The baud rate is calculated as follows:

I2C_FLTR.DNFEN	I2C_CCR.CKDIV	Baud rate
0b0	0b000	$B = \frac{1}{\frac{(SHIGHW + 3) + (SLOWW + 3)}{\Phi I2C} + t_R + t_F}$
0b1	0b000	$B = \frac{1}{\frac{(SHIGHW + 3 + DNF) + (SLOWW + 3 + DNF)}{\Phi I2C} + t_R + t_F}$
0b0	Non-0	$B = \frac{1}{\frac{(SHIGHW + 2) + (SLOWW + 2)}{\Phi I2C} + t_R + t_F}$
0b1	Non-0	$B = \frac{1}{\frac{(SHIGHW + 2 + DNF) + (SLOWW + 2 + DNF)}{\Phi I2C} + t_R + t_F}$

Where:

- B: Baud rate, unit: Mbps
- ΦI2C: I2C reference clock frequency, unit: MHz
- DNF: Digital filter capability, set by the I2C_FLTR.DNF register

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- t_R: Rise time of the SCL line, unit: ns
- t_F: Fall time of the SCL line, unit: ns

Note

- In master mode, SHIGHW is used to set the high level width of the SCL clock. The setting has no effect in slave mode.
- In master mode, SLOWW is used to set the low level width of the SCL clock. In slave mode, the set value must be greater than the data setup time ($t_{SU;DAT}$), which is 250ns for standard mode and 100ns for fast mode.
- The rise time (t_R) and fall time (t_F) of the SCL line depend on the total bus capacitance (C_b) and pull-up resistance (R_p). For detailed information, refer to the I2C bus specification.

24.5.14 I2C Filter Control Register (I2C_FLTR)

Offset	Bit Position																													
0x30	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000010																															
Name	Reserved																										ANFEN	DNFEN	Reserved		DNF	
Access																											RW	RW			RW	

Bit	Name	Functional Description	Access
31:6	*Reserved*	-	-
5	ANFEN	Analog Filtering Function Allowed Bit ● 0b0: Analog filter function disabled ● 0b1: Analog filter function enabled	RW
4	DNFEN	Digital Filtering Function Allowed Bit ● 0b0: Digital filter function disabled ● 0b1: Digital filter function enabled	RW
3:2	*Reserved*	-	-
1:0	DNF	Selection of Filtering Capabilities for Digital Filters ● 0b00: Filtering capability 1 I2C reference clock period ● 0b01: Filtering capability 2 I2C reference clock periods ● 0b10: Filtering capability 3 I2C reference clock periods ● 0b11: Filtering capability 4 I2C reference clock periods	RW

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24.5.15 I2C FIFO Status Register (I2C_FSTR)

Offset	Bit Position																													
0x34	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								RFST		TFST		NACK_TFFLUSH	RFFLUSH	TFFLUSH	FEN
Access																									RO		RO		RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7:6	RFST	Receive FIFO Status Bit ● 0b00: FIFO empty ● 0b01: FIFO half full ● 0b10: FIFO full ● 0b11: Reserved	RO
5:4	TFST	Transmit FIFO Status Bit ● 0b00: FIFO empty ● 0b01: FIFO half empty ● 0b10: FIFO full ● 0b11: Reserved	RO
3	NACK_TFFLUSH	NACK Resets Transmit FIFO ● 0b0: Do not execute TFIFO FLUSH after receiving NACK in slave mode ● 0b1: Execute TFIFO FLUSH after receiving NACK in slave mode	RW
2	RFFLUSH	RX FIFO Pointer Reset ● 0b0: Write disabled ● 0b1: Reset RX FIFO pointer	RW
1	TFFLUSH	TX FIFO Pointer Reset ● 0b0: Write disabled ● 0b1: Reset TX FIFO pointer	RW
0	FEN	FIFO Function Enable Bit ● 0b0: FIFO function disabled ● 0b1: FIFO function enabled	RW

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24.5.16 I2C Slave Address Receive Register (I2C_SLVADRR)

Offset	Bit Position																													
0x38	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																						SLVADR									
Access																							RO									

Bit	Name	Functional Description	Access
31:10	*Reserved*	-	-
9:0	SLVADR	Slave Address Receive Register SLVADR[6:0]: 7-bit slave receive address SLVADR[9:0]: 10-bit slave receive address	RO

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25 Serial Peripheral Interface (SPI)

25.1 Introduction

This product is equipped with 1-channel serial peripheral interface SPI, supports high-speed full-duplex serial synchronous transmission, and facilitates data exchange with peripheral devices. Users can set the range of 3/4-wire, master/slave and baud rate as required.

25.2 Features

Table 25-1 SPI Main Features

Essentials	Description
Serial Communication Function	● Supporting 4-wire SPI mode and 3-wire clock synchronization mode ● Supports full-duplex synchronous communication mode and transmit-only communication mode ● Polarity and phase of adjustable communication clock SCK
Data Format	● Selectable data shift order: MSB start/LSB start ● Selectable data width: 4/5/6/7/8/9/10/11/12/13/14/15/16/20/24/32 bits ● A maximum of 4 frames width of 32-bit data can be transmitted or received at a single time
Baud Rate	● The baud rate can be adjusted by the built-in special baud rate generator in master mode. The baud rate ranges from 2 to 256 frequency division of PCLK1. ● Maximum baud rate allowed in slave mode is 6 frequency division of PCLK1
Data Buffer	● With 16-byte data buffer ● Supports double buffering
Error Monitoring	● Mode fault error monitoring ● Data overload error monitoring ● Data underload error monitoring ● Parity error monitoring
Chip Selection Signal Control	● Each channel is configured with 4 chip-selected signal line ● The relative timing relationship between the chip select signal and the communication clock can be adjusted ● The inactive time of the chip select signal between two consecutive communications can be adjusted ● Polarity adjustable
Transmission Control in Master Mode	● Start transmission by writing data to the data register ● Communication auto suspend function

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Essentials	Description
Interrupt	● Receive buffer is full ● Transmit buffer is empty ● SPI error (mode/overload/underload/parity) ● SPI vacant ● Transmit complete (event source only)
Low Power Control	● Configurable module stop
Other Functions	● SPI initialization function

Note

When the communication auto-suspend feature is used in master receive mode, overload errors will not occur because the communication clock stops. Refer to "Overload Error" for more information.

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25.3 Functional Description

25.3.1 System Block Diagram

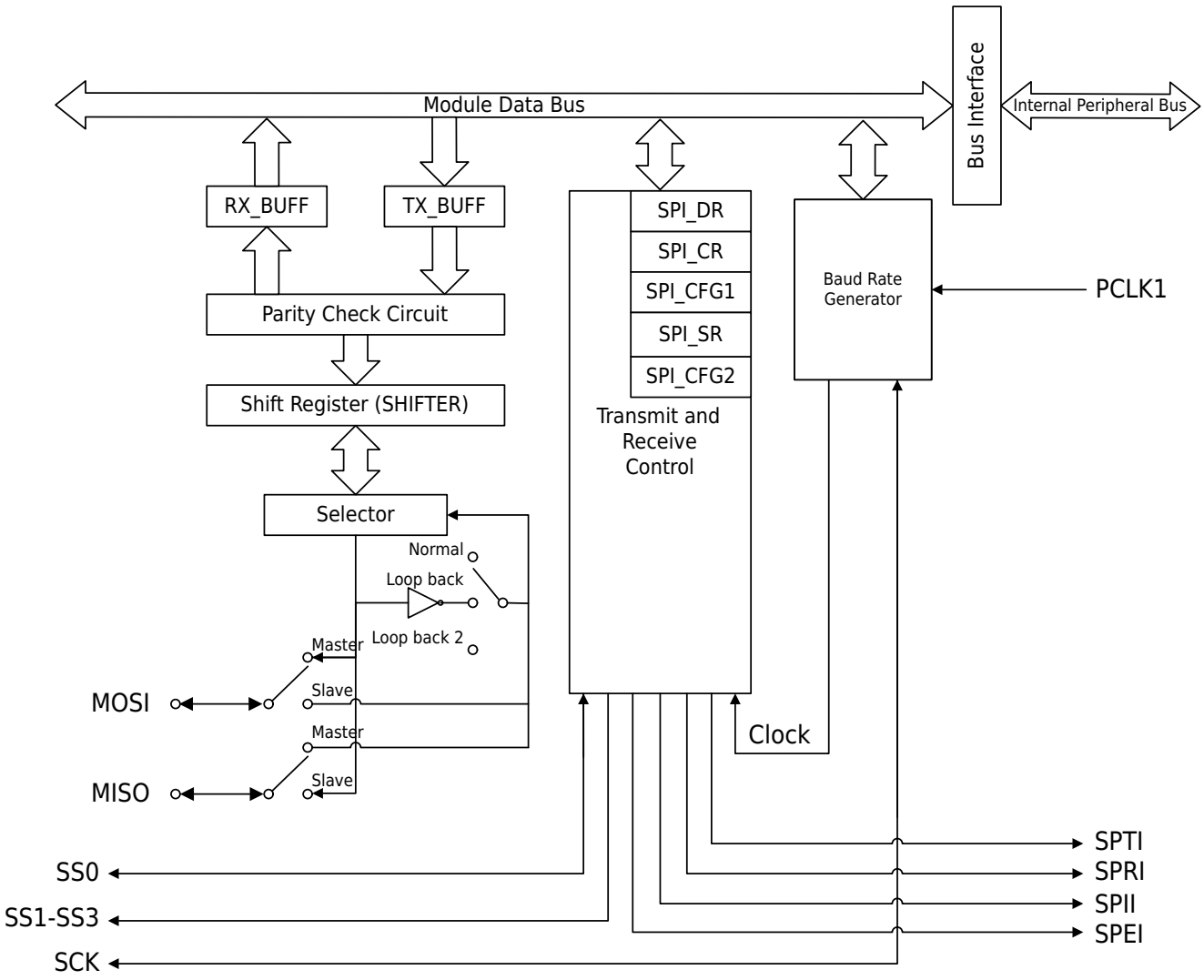

Figure 25-1 SPI System Block Diagram

Table 25-2 Pin Description

Pin Name	Port direction	Function
SCK	Input/ Output	Communication clock pin
MOSI	Input/ Output	Master data transmission pin
MISO	Input/ Output	Slave data transmission pin
SS0	Input/ Output	Slave select input/output pin
SS1	Output	Slave select output pin
SS2	Output	Slave select output pin

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Pin Name	Port direction	Function
SS3	Output	Slave select output pin

25.3.2 SPI Action System Description

25.3.2.1 Pin Status in Master Mode

When SPI works in master mode, the status of each pin is shown below.

Table 25-3 SPI Pin Status Description in Master Mode

Mode		Pin Name	Pin Status
SPI Action (SPIMDS=0)	Master Mode (MSTR=1, MODFE=0)	SCK	Output
		SS0-SS3	Output
		MOSI	Output
		MISO	Input
Clock Synchronization Operation (SPIMDS=1)	Master Mode (MSTR=1)	SCK	Output
		SS0-SS3 (not used)	Hi-Z (available as general I/O)
		MOSI	Output
		MISO	Input

Note

Please set the pin input type to CMOS input and the output type to high drive mode. For related settings, please refer to "Register-General Control Register (PCRxy) " in the "General-Purpose IO (GPIO) " chapter.

25.3.2.2 Pin Status in Slave Mode

When SPI works in slave mode, the status of each pin is shown below.

Table 25-4 SPI Pin Status Description in Slave Mode

Mode		Pin Name	Pin Status
SPI Action (SPIMDS=0)	Slave Mode (MSTR=0, MODFE=0)	SCK	Input
		SS0	Input
		SS1- SS3 (not used)	Hi-Z (available as general I/O)
		MOSI	Input
		MISO	Output/Hi-Z
Clock Synchronization Operation (SPIMDS=1)	Slave Mode (MSTR=0)	SCK	Input
		SS0-SS3 (not used)	Hi-Z (available as general I/O)
		MOSI	Input
		MISO	Output

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Note

Please set the pin input type to CMOS input and the output type to high drive mode. For related settings, please refer to "Register-General Control Register (PCRxy) " in the "General-Purpose IO (GPIO) " chapter.

25.3.2.3 SPI System Connection Examples

Master Mode

In the master-multi-slave mode SPI system architecture, the master drives SCK, MOSI, and SS0-SS3. In SPI slave equipment 0-3, the slave equipment drives the MISO when the SS input of a slave computer is a active level.

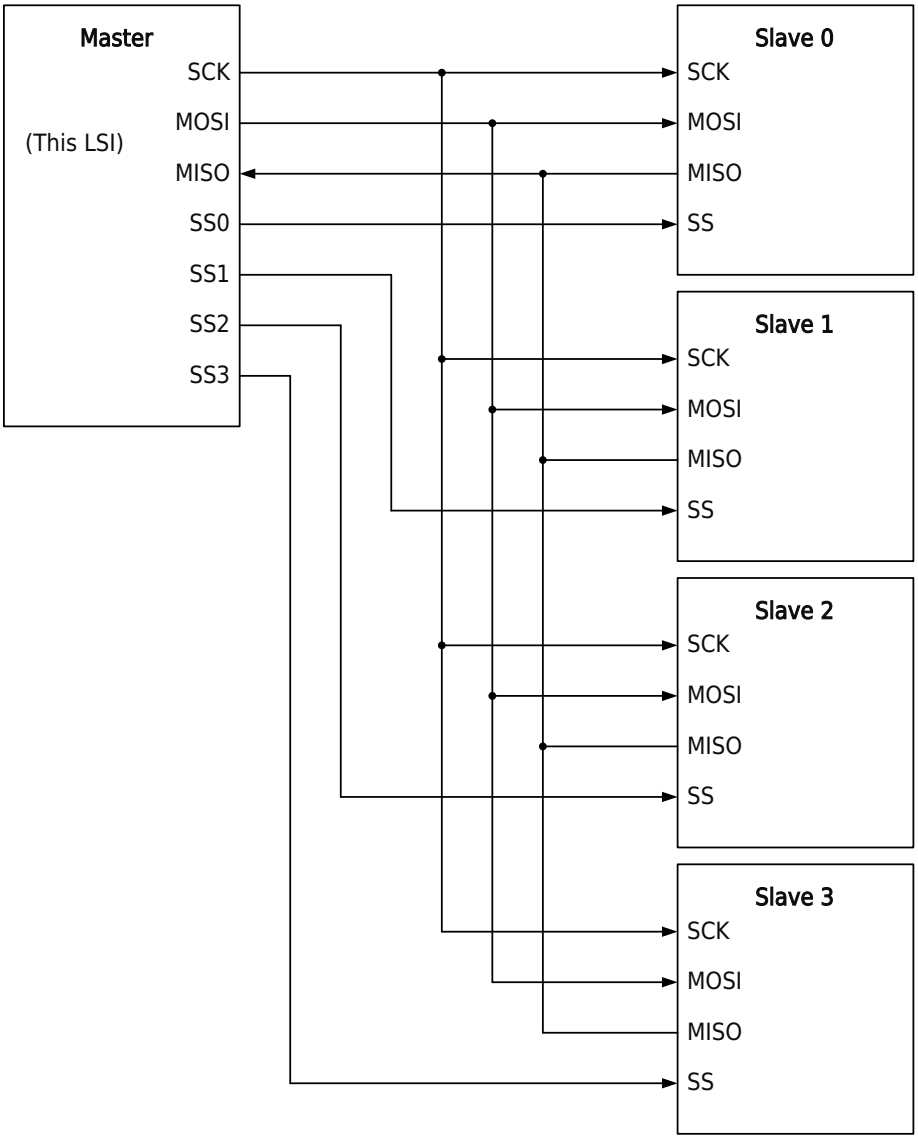

Figure 25-2 Master Mode Structure

Clock Synchronization Operation

In the SPI system structure used for clock synchronous operation, the master device drives SCK and MOSI, and the slave device drives MISO. SS pins are not used.

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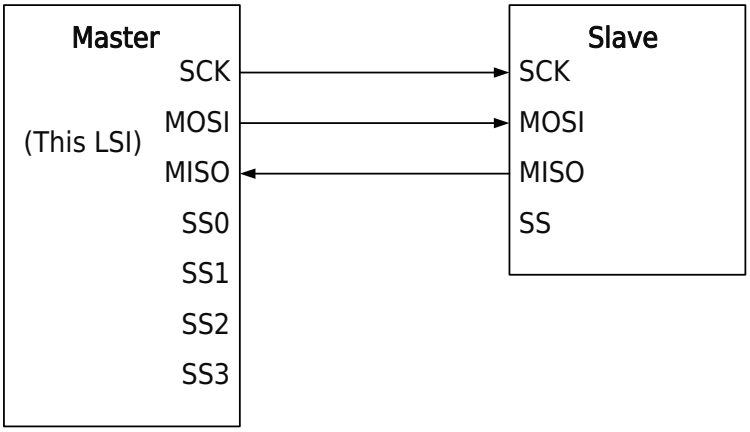

Figure 25-3 Three-wire Clock Synchronization Operation

25.3.3 Data Communication Description

25.3.3.1 Baud Rate

In master mode, SPI clock is provided by internal baud rate generator. In slave mode, the clock is input to the SCK pin.

Baud rate depends on SPI_CFG2.MBR bit setting. The calculation method is shown in the following formula:

$$\text{Baud Rate} = \frac{f_{PCLK1}}{2^{N+1} \times (M+1)}$$

Where:

- N: SPI_CFG2.MBR bit setting value, the range is from 0-3;
- M: SPI_CFG1.CLKDIV bit setting value, the range is from 0-15.

Table 25-5 Bit Speed of Some Set Values

MBR Bit Setting Value (N)	CLKDIV Bit Setting Value (M)	Frequency Dividing Ratio	Baud Rate			
			PCLK1=5MHz	PCLK1=10MHz	PCLK1=20MHz	PCLK1=40MHz
0	0	2	2.50Mbps	5.00Mbps	10.0Mbps	20.0Mbps
0	1	4	1.25Mbps	2.50Mbps	5.00Mbps	10.0Mbps
0	3	8	625kbps	1.25Mbps	2.50Mbps	5.00Mbps
0	7	16	313kbps	625kbps	1.25Mbps	2.50Mbps
0	15	32	156kbps	313kbps	625kbps	1.25Mbps
1	15	64	78kbps	156kbps	313kbps	625kbps
2	15	128	39kbps	78kbps	156kbps	313kbps
3	15	256	20kbps	39kbps	78kbps	156kbps

25.3.3.2 Data Format

The data format of SPI depends on the setting value of SPI_CFG2 register and SPI_CR.PAE bit setting value. SPI treats the data of a certain length starting from the LSB bit in the data register SPI_DR (the data length is set by the SPI_CFG2.DSIZE) as the transfer object, regardless of the MSB/LSB shift order.

SPI_CFG2.DSIZE determines the bit width of the data. The bit width range is 4-32 bits. SPI_CR.PAE determines the last bit of the data. When PAE is 1, the last bit is used as the parity bit. When it is 0, it is the lowest bit of the data itself.

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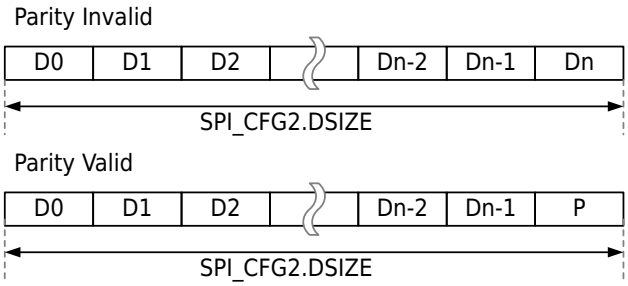

Figure 25-4 Data Format

When sending SPI data, the transmitted data first enters the transmit buffer (TX_BUFF), and then the data in the TX_BUFF is copied to the SHIFTER register. The SHIFTER sequentially outputs the data. During SPI data reception, data is sequentially shifted in from the SHIFTER. Once the shifting is complete, the data in the SHIFTER is copied to the receive buffer (RX_BUFF).

During data transmission, there are four situations according to the settings of the shift order control bit SPI_CFG2.LSBF and the parity control bit SPI_CR.PAE:

- **MSB Transmitted First, Parity Invalid**

  During transmitting, data D31-D0 is copied sequentially from TX_BUFF to the SHIFTER and shifted out from the highest bit of the SHIFTER in the sequence of D31-D0.

  During receiving, data D31-D0 is shifted in from the least significant bit of the SHIFTER and copied to RX_BUFF after all bits have been received.

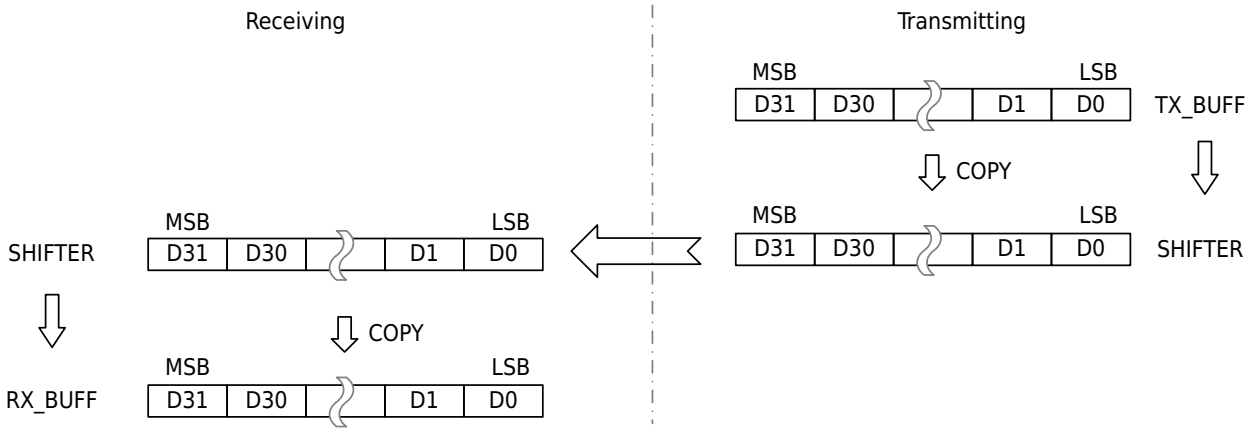

Figure 25-5 MSB Transmitted First, Parity Invalid

- **LSB Transmitted First, Parity Invalid**

  During transmitting, D31-D0 is copied from TX_BUFF to SHIFTER in the sequence of D0-D31, and shifted out from the highest bit of the SHIFTER in the sequence of D0-D31.

  During receiving, data D0-D31 is moved in from the lowest bit of SHIFTER, and then copied from SHIFTER to RX_BUFF in the order D31-D0 after all data is moved in.

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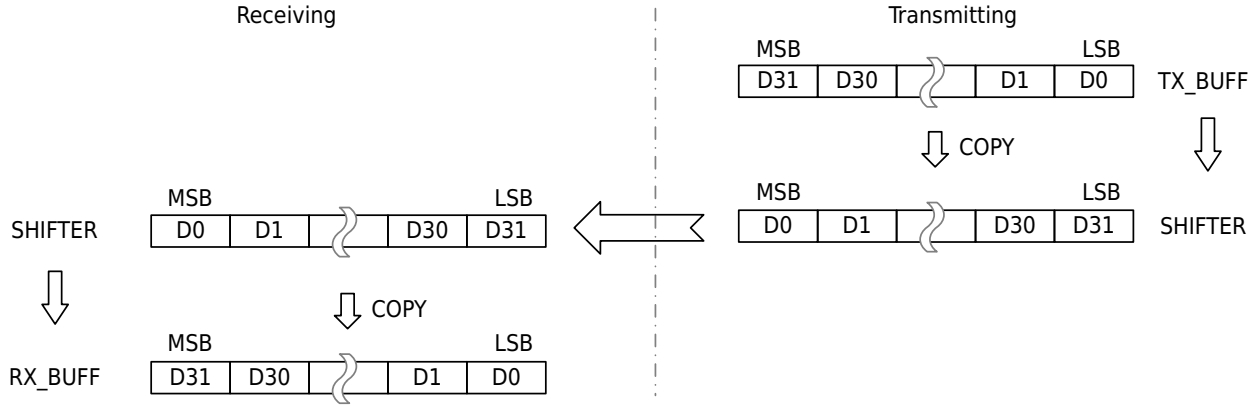

Figure 25-6 LSB Transmitted First, Parity Invalid

- **MSB Transmitted First, Parity Valid**

  During transmitting, the value of parity bit P is calculated according to the value of D31-D1, then D0 is replaced by P, copied to SHIFTER according to the order of D31-D1, P, and shifted out from the highest bit of the SHIFTER in the sequence of D31-P.

  During receiving, the data D31-P moves in from the lowest bit of SHIFTER, and parity is performed when the data is copied to SHIFTER. Finally, copy the data to RX_BUFF.

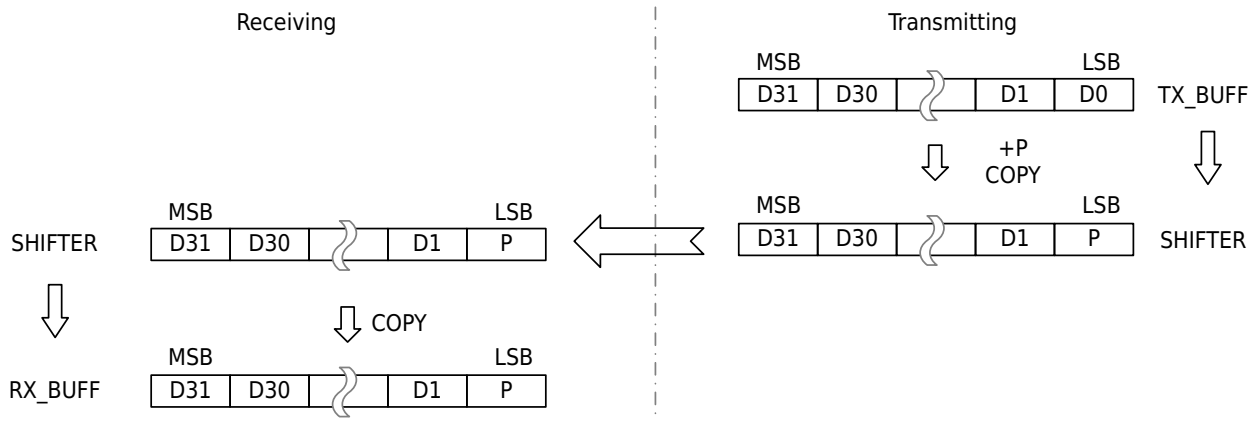

Figure 25-7 MSB Transmitted First, Parity Valid

- **LSB Transmitted First, Parity Valid**

  During transmitting, the value of parity bit P is calculated according to the value of D30-D0, and then P is used instead of D31, which is copied from TX_BUFF to SHIFTER in the sequence of D0-P and shifted out from the highest bit of the SHIFTER in the sequence of D0-P.

  During receiving, the data D0-P moves in from the lowest bit of SHIFTER, and parity is performed when the data is copied to SHIFTER. The data D0-P is rearranged at the time of replication and copied to RX_BUFF in the sequence of P-D0.

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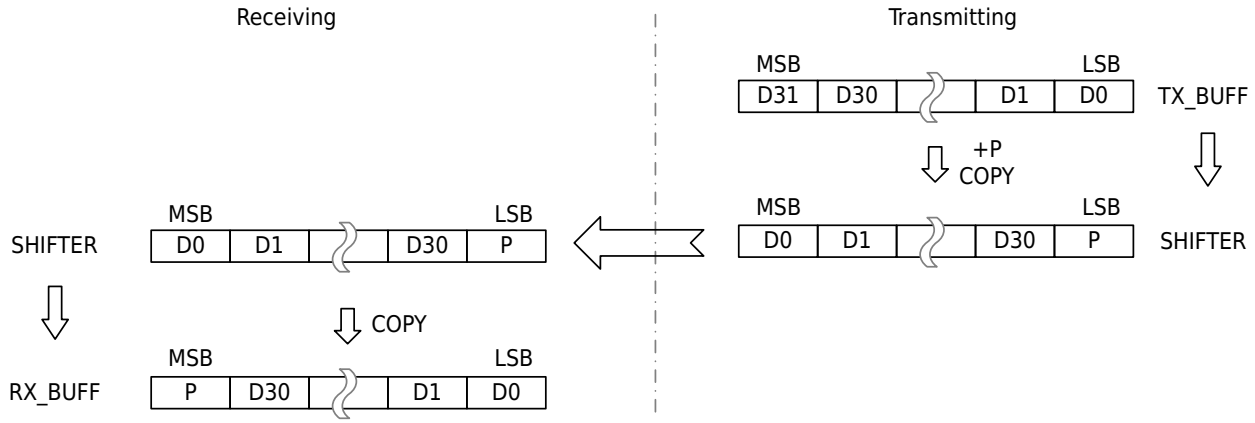

Figure 25-8 LSB Transmitted First, Parity Valid

25.3.3.3 Transfer Format

CPHA=0

When the SPI_CFG2.CPHA bit is 0, SPI samples data on the odd edges of SCK and updates data on the even edges. The figure below is the SPI transmission timing diagram when CPHA=0. When the input level of the SSi signal becomes a active level, MOSI/MISO starts to update the transmission data. After the SSi signal becomes active for the first time on the edge of the first SCK signal, the data is sampled once per SCK period. MOSI/MISO signals are updated at 1/2 SCK periods after each sampling. The set value of CPOL bit does not affect the running time of SCK signal, but only affects the polarity of signal.

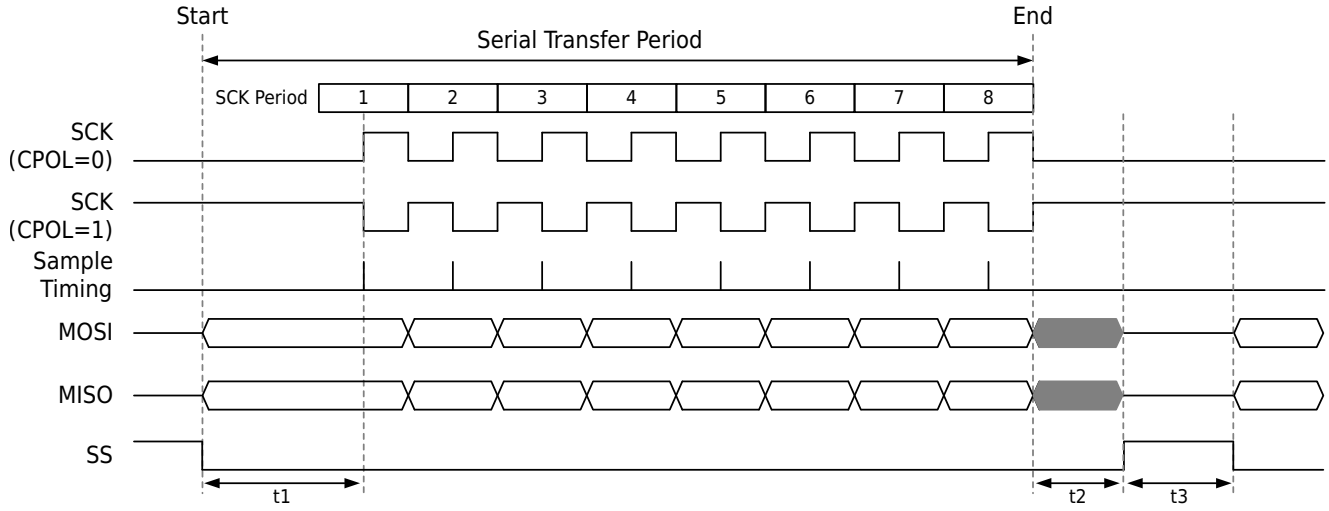

Figure 25-9 Data Transmission Format Diagram (CPHA=0)

In the above figure, t1 represents the interval from the SS signal being active to the SCK oscillation (SCK delay time, which can be controlled by setting SPI_CFG1.MSSI and SPI_CFG2.MSSIE), t2 represents the interval from the SCK oscillation stopping to the SS signal becoming inactive (SS inactive delay time, which can be controlled by setting SPI_CFG1.MSSDL and SPI_CFG2.MSSDLE), and t3 represents the minimum waiting time from the end of serial transmission to the start of the next transmission (the next access delay, which can be controlled by setting SPI_CFG1.MIDI and SPI_CFG2.MIDIE). t1, t2 and t3 are controlled by the master device on the SPI system. For details, see "Master Action in SPI Operation Mode".

CPHA=1

When SPI_CFG2.CPHA bit is "1", SPI updates the data at the odd edge of SCK and samples the data at the even edge. The figure below is the SPI transmission timing diagram when CPHA=1. MOSI/MISO starts

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to transmit data updates at the edge of the first SCK signal after the SSi signal becomes active. After this, data is updated every SCK period. Data is sampled at 1/2 SCK periods after each update. The set value of the SPI_CFG2.CPOL bit does not affect the timing of the operation of the SCK signal but only affects the polarity of the signal.

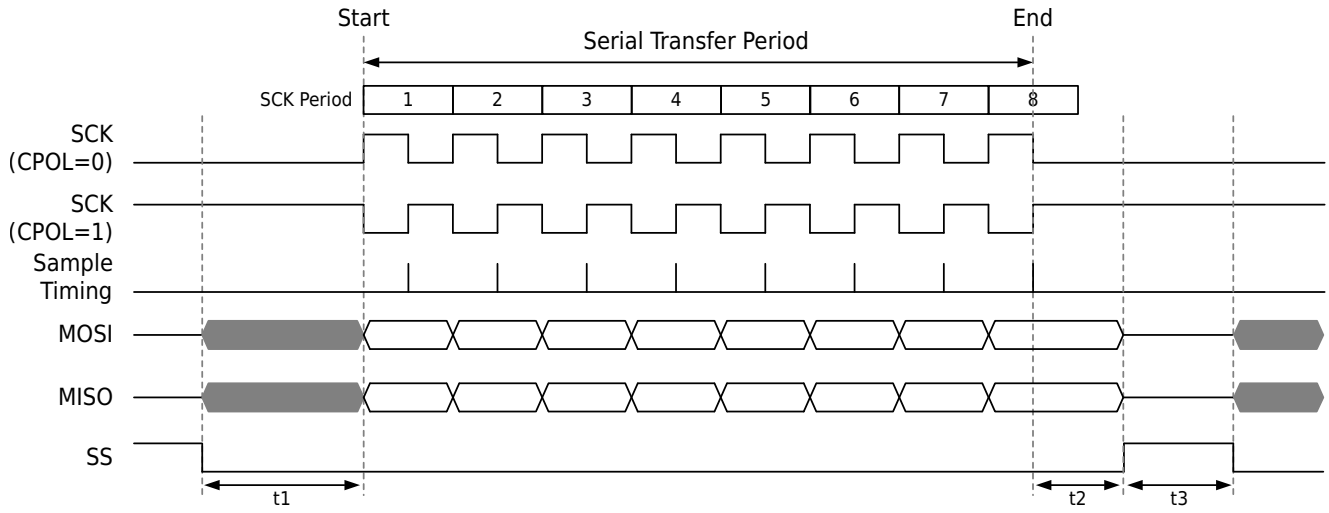

Figure 25-10 Data Transmission Format Diagram (CPHA=1)

t1, t2, t3 are the same as when the CPHA bit is 0.

25.3.3.4 Communication Method

This SPI supports full-duplex synchronous serial communication mode, transmit-only communication mode, which can be selected through the SPI_CR.TXMDS.

Full-duplex Synchronous Serial Communication Mode

When the SPI_CR.TXMDS bit is set to 0, the SPI operates in full-duplex synchronous serial communication mode. As shown in the figure below, the SPI_CFG1.FTHLV bit is 0b00, the SPI_CFG2.CPHA bit is 1 and the SPI_CFG2.CPOL bit is 0, and the SPI performs 8-bit serial transmission.

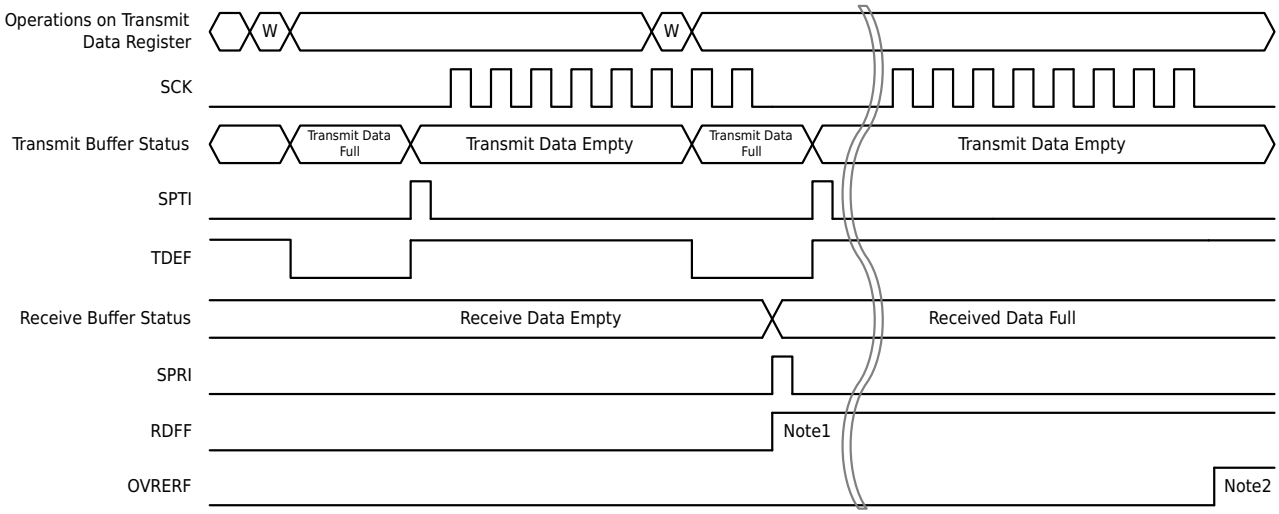

Figure 25-11 Full-duplex Synchronous Serial Communication

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Note

1. When the serial transmission ends, if the receive buffer is empty, SPI will copy the received data from the SHIFTER register to the receive buffer, the receive buffer full flag RDFF is set to 1, and a receive data full interrupt request SPRI is generated.
2. When the serial transmission ends, if the receive buffer still holds the data received last time and has not been read by the system, the SPI will set the data overload flag OVRERF to 1, the data reception will be inactive, and the data in the receive SHIFTER register will be discarded.

Transmit-only Communication Mode

When the SPI_CR.TXMDS bit is set to 1, the SPI operates in transmit-only communication mode. As shown in the figure below, the SPI_CFG1.FTHLV bit is 0b00, the SPI_CFG2.CPHA bit is 1 and the SPI_CFG2.CPOL bit is 0, and the SPI performs 8-bit serial transmission.

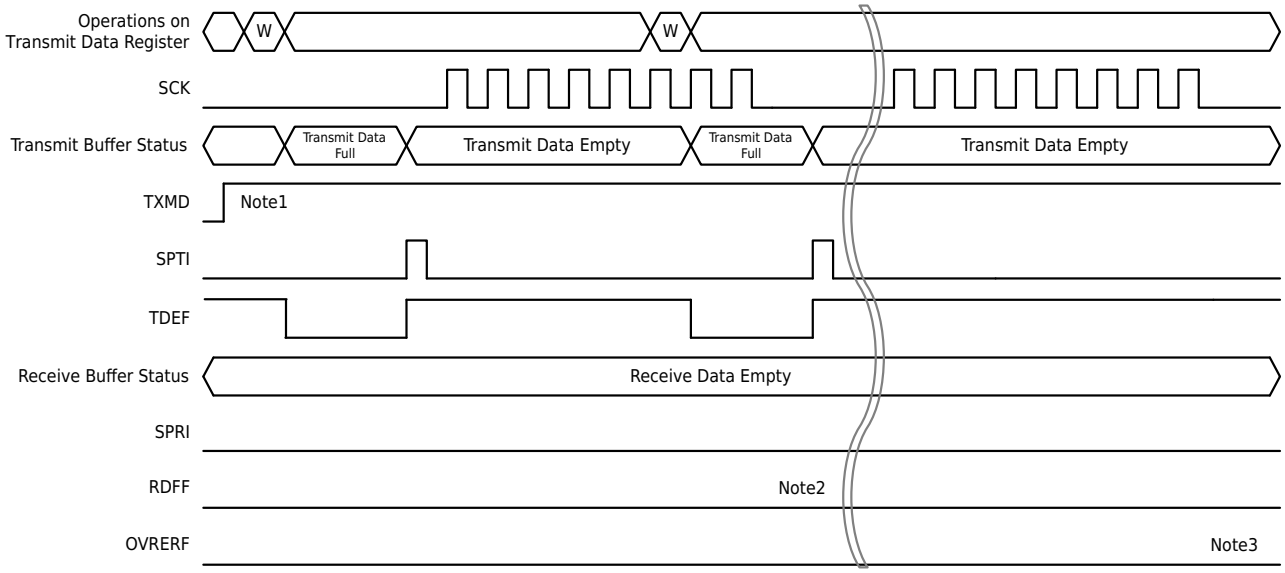

Figure 25-12 Transmit-only Communication

Note

1. Before setting up the transmit-only communication mode, make sure that there is no unread data in the receive buffer (RDFF=0) and no data overload error (OVRERF=0).
2. In the transmit-only communication mode, when the serial transmission ends, no data will be received even if the receive buffer is empty, and RDFF will always remain 0.
3. In the transmit-only communication mode, since the receive buffer is always empty, no data overload error will occur and the OVRERF flag will always remain 0.

25.3.3.5 Communication Interval Time

Communication Interval Time Under Normal Communication Setting

When the SPI_CFG1.CTMDS bit is set to 0, the SPI uses normal communication setting. The interval time between two consecutive communications can be set by SPI_CFG1.MIDI and SPI_CFG2.MIDIE. The minimum interval time is 1*SCK+2*PCLK1. As shown in the figure below, the SPI_CFG2.CPHA bit is 1 and the SPI_CFG2.CPOL bit is 0, and the SPI performs serial transmission.

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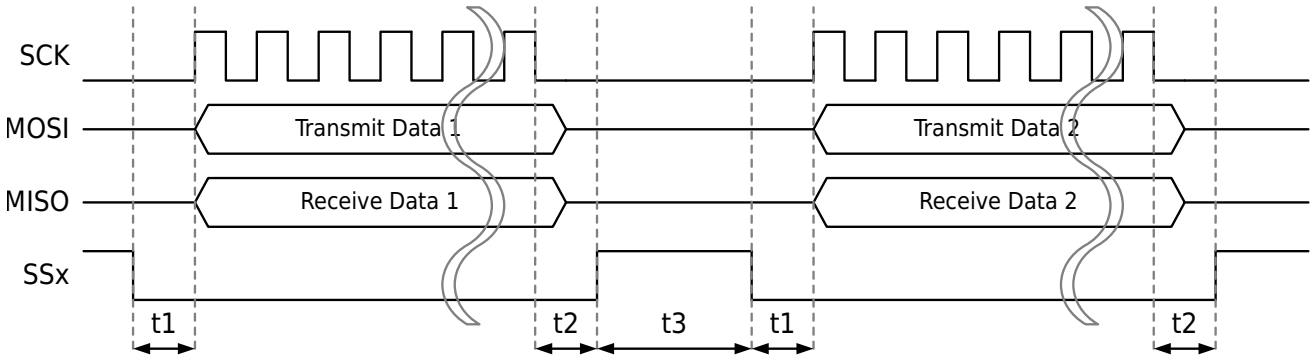

Figure 25-13 Normal Communication

In the above figure, t1 represents the time interval from the active SS signal to the first edge of SCK (SCK delay time, which can be controlled by setting SPI_CFG1.MSSI and SPI_CFG2.MSSIE), t2 represents the time interval from the last edge of SCK to the inactive SS signal (SS inactive delay time, which can be controlled by setting SPI_CFG1.MSSDL and SPI_CFG2.MSSDLE), and t3 represents the minimum waiting time from the end of this transmission to the beginning of the next transmission (the next access data delay, which can be controlled by setting SPI_CFG1.MIDI and SPI_CFG2.MIDIE).

Note

When the communication rate is 2 divided by PCLK1 (SPI_CFG2.MBR=0b00 and SPI_CFG1.CLKDIV=0b0000), please configure t3 to 2*SCK+2*PCLK1 or above, that is, SPI_CFG2.MIDIE=1 and SPI_CFG1.MIDI=0x1-0x7.

Communication Interval Time Under Continuous Communication Setting

When the SPI_CFG1.CTMDS bit is set to 1, the SPI uses the continuous communication setting. Completely continuous and uninterrupted data communication can be achieved. As shown in the figure below, the SPI_CFG2.CPHA bit is 1 and the SPI_CFG2.CPOL bit is 0, and the SPI performs serial transmission.

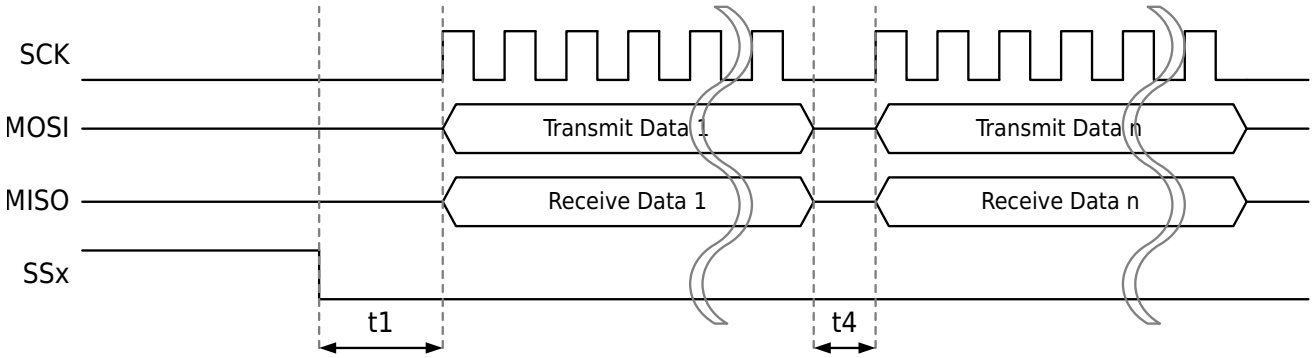

Figure 25-14 Continuous Communication

In the above figure, t1 represents the time interval from the activeity of the SS signal to the first edge of SCK (SCK delay time, which can be controlled by setting SPI_CFG1.MSSI and SPI_CFG2.MSSIE), and t4 represents the time interval between each transmission, which can be controlled by setting SPI_CFG1.MSSI and SPI_CFG2.MSSIE. The relationship between t1 and t4 is defined as t4=t1-1*SCK.

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Note

- In continuous communication mode, if the master has no new data written into the transmit buffer, it will enter a pause state, SCK stops outputting, and the SS signal remains active, waiting for new transmit data to be written into the transmit buffer before continuing to transmit the next frame of data.
- In continuous communication mode, if the slave has no new data written into the transmit buffer, an underload error will occur and SPI_SR.MODFERF and SPI_SR.UDRERF will be set to 1. For detailed description, see "Underload Error".
- For continuous communication in clock synchronization mode, if the transmission format with CPHA=0 is used, ensure that the data is written before CPHA is set to 0.
- When using the transmission format of CPHA=0, the slave needs to write new data to the transmit buffer before the previous frame of data is sent. Otherwise, no matter whether the master starts the communication of the next frame of data, the slave will have an underload error.
- In continuous communication mode, the time interval between the last SCK of the previous frame of data and the first SCK of the next frame of data can also be adjusted through MSSI.

25.3.4 Operating Instructions

25.3.4.1 Operational Mode Overview

This SPI supports 4-wire SPI mode and 3-wire clock synchronization mode. Serial communication can be performed as a master or slave in each operating mode. Set the SPI_CR.MSTR and SPI_CR.SPIMDS bits to set the SPI mode. The relationship between the SPI mode and the SPI_CR register setting and the overview of each mode are shown in the following table.

Table 25-6 SPI Mode and Register Setting Relationship

Mode	Master (SPI Operation)	Slave (SPI Operation)	Master (Clock Synchronous Operation)	Slave (Clock Synchronous Operation)
MSTR bit setting	1	0	1	0
SPIMDS bit setting	0	0	1	1
SCK signal	Output	Input	Output	Input
MOSI signal	Output	Input	Output	Input
MISO signal	Input	Output/Hi-Z	Input	Output
SS0 signal	Output	Input	Hi-Z (not used)	Hi-Z (not used)
SS1-SS3 signal	Output	Hi-Z	Hi-Z (not used)	Hi-Z (not used)
SS polarity change function	Yes	Yes	-	-
Maximum transmission rate	PCLK1/2	PCLK1/6	PCLK1/2	PCLK1/6
Clock source	Internal baud rate generator	SCK input	Internal baud rate generator	SCK input
Clock polarity	2 species	2 species	2 species	2 species
Clock phase	2 species	2 species	2 species	2 species[*3]
Start transfer bit	MSB/LSB	MSB/LSB	MSB/LSB	MSB/LSB

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Mode	Master (SPI Operation)	Slave (SPI Operation)	Master (Clock Synchronous Operation)	Slave (Clock Synchronous Operation)
Transmission data length	4-32 bits	4-32 bits	4-32 bits	4-32 bits
SCK delay control	Yes	No	Yes	No
SS inactive delay control	Yes	No	Yes	No
Next access delay control	Yes	No	Yes	No
Transport start method	Write transmit buffer by transmit buffer empty interrupt request	SS input active or SCK clock edge	Write transmit buffer by transmit buffer empty interrupt request	SCK oscillation
Mode failure error	No	Yes	No	Yes
Transmit buffer empty detection	Yes	Yes	Yes	Yes
Receive buffer full detection	Yes*1	Yes*1	Yes*1	Yes*1
Overload error detection	Yes*1	Yes*1	Yes*1	Yes*1
Parity error detection	Yes*1 *2	Yes*1 *2	Yes*1 *2	Yes*1 *2
Underload error detection	No	Yes	No	Yes

Note

1. When the SPI_CR.TXMDS bit is 1, the receive buffer full detection, overload error detection, and parity error detection are not performed.
2. When the SPI_CR.PAE bit is 0, parity error detection is not performed.
3. When the SPI_CFGR2.CPHA bit is 0, it is only active in continuous transmission mode. For specific setting steps, please refer to "Slave Action in Clock Synchronous Operation Mode".

25.3.4.2 Master Action in SPI Operation Mode

Action Description as Master

When the SPI data transmit buffer (TX_BUFF) is empty (SPI_SR.TDEF is 1), write the data of the frame length set by the SPI_CFG1.FTHLV to the SPI_DR register, SPI will update the SPI_DR data to TX_BUFF. If the SHIFTER register is empty, SPI copies the TX_BUFF data to the SHIFTER register to start serial transmission.

When transmit data is copied to SHIFTER, SPI will change SHIFTER state to full state; When serial delivery is over, change to empty. The status of SHIFTER cannot be read.

After the SPI has generated the final SCK edge required for the last sampling timing, the current serial transmission concludes. The completion time is independent of the SPI_CFG2.CPHA bit. When the

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receive buffer (RX_BUFF) is empty, SPI copies the data from SHIFTER to RX_BUFF after serial delivery, which can be read by the SPI_DR register.

The final sampling timing depends on the bit length of the transmit data, and the SPI data length of the master mode depends on SPI_CFG2.DSIZE. The polarity of the SS output pin depends on the set value of SPI_CFG1 register. For details about the SPI transfer format, see "Transfer Format".

Initialization of SPI Master Mode

Step1. Set the SPI_CFG1 register, including the setting of the baud rate, the setting of the number of frames used, the setting of various delay times, etc.;

Step2. Set the SPI_CFG2 register, including SS level setting, data shift sequence setting, various delay allow bit setting, data format and clock polarity phase setting, etc.;

Step3. If you need to use interrupt, set the interrupt register of the system;

Step4. If you need to use DMA, set the relevant register for DMA;

Step5. Set the input/output pin;

Step6. Set the SPI_CR register, including the mode and operation mode settings, self-diagnosis function settings, parity check settings, etc.;

Step7. Confirm the setting of SPI_CR register;

Step8. Clear various flag bits;

Step9. Set the interrupt permission bit;

Step10. Set the SPI_CR.SPE bit to 1 and the action starts.

25.3.4.3 Slave Action in SPI Operation Mode

Action Description as Slave

When the SPI_CFG2.CPHA bit is 0, if SPI detects that the SS0 input signal becomes active, it needs to start to output the signal to MISO to drive the active data. Therefore, when the CPHA bit is 0, the SS0 input signal level is changed from inactive to active as a trigger signal that starts serial transmission.

When the CPHA bit is 1, if SPI detects the original SCK edge when the SS0 input signal is at an active level, it needs to start to drive active data to the MISO output signal. Therefore, when the CPHA bit is 1, the first SCK edge of the SS0 signal in the active state is considered as the trigger signal that starts serial transmission.

If SPI detects the start of serial delivery in the SHIFTER empty state, it changes SHIFTER to full state and cannot transfer data from TX_BUFF to SHIFTER during serial delivery. If SHIFTER is full before starting serial transfer, SPI keeps SHIFTER full.

If SPI detects the SCK edge of the last sampling sequence, the current serial transmission concludes. The completion time is independent of the SPI_CFG2.CPHA bit. When RX_BUFF is empty, SPI copies the data from SHIFTER to RX_BUFF after serial delivery. The data can be read by accessing SPI_DR. SPI changes SHIFTER to an empty state after serial delivery, independent of the state of RX_BUFF.

During serial delivery, a mode fault error occurs if SPI detects that the SS0 input signal is disabled.

The final sampling timing depends on the bit length of the transmit data, and the SPI data length depends on SPI_CFG2.DSIZE. The polarity of SS0 input signal depends on SPI_CFG1.SS0PV bit setting. For details about the SPI transfer format, see "Transfer Format".

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Note

When the SPI_CFG2.CPHA bit is 0, the SS0 input signal level is changed from inactive to active as a trigger signal to start serial transmission. Since the SS0 input signal is fixed in a slave mode, SPI will not start serial transmission normally. Therefore, in the structure where the SS0 input signal is fixed to the active state, the CPHA bit must be set to 1 in order to send and receive the SPI in the slave mode normally. If you need to set the CPHA bit to 0, you cannot fix the SS0 input signal.

Initialization of SPI Slave Mode

Step1. Set the SPI_CFG1 register, mainly including the setting of the number of frames used;

Step2. Set the SPI_CFG2 register, including transmission rate, data format and clock polarity phase setting;

Step3. If you need to use interrupt, set the interrupt register of the system;

Step4. If you need to use DMA, set the relevant register for DMA;

Step5. Set the input/output pin;

Step6. Set the SPI_CR register, including the mode and operation mode settings, self-diagnosis function settings, parity check settings, etc.;

Step7. Confirm the setting of SPI_CR register;

Step8. Clear various flag bits;

Step9. Set the interrupt permission bit;

Step10. Set the SPI_CR.SPE bit to 1 and the action starts.

25.3.4.4 Master Action in Clock Synchronous Operation Mode

When the SPI_CR.SPIMDS bit is 1, the SPI is in clock synchronous operation mode. When operating in this mode, SPI only uses the 3 pins SCK, MOSI and MISO for communication, and the SSi pin is released for normal I/O functions.

Although the SSi pins are not used in the clock synchronous operation mode, the internal operation of the module is the same as the SPI mode of operation.

Action Description as Master

When the SPI data transmit buffer (TX_BUFF) is empty (SPI_SR.TDEF is 1), write the data with the frame length set by the SPI_CFG1.FTHLV to the SPI_DR register, SPI will update the SPI_DR data to TX_BUFF. If the SHIFTER register is empty, SPI copies the TX_BUFF data to the SHIFTER register to start serial transmission.

When transmit data is copied to SHIFTER, SPI will change SHIFTER state to full state; When serial delivery is over, change to empty. The status of SHIFTER cannot be read.

After the SPI has generated the final SCK edge required for the last sampling timing, the current serial transmission concludes. The completion time is independent of the SPI_CFG2.CPHA bit. When the receive buffer (RX_BUFF) is empty, SPI copies the data from SHIFTER to RX_BUFF after serial delivery, which can be read by the SPI_DR register.

The final sampling timing depends on the bit length of the transmit data, and the SPI data length of the master mode depends on SPI_CFG2.DSIZE. For details about the SPI transfer format, see "Transfer Format".

Master Initialization in Clock Synchronous Operation Mode

Step1. Set the SPI_CFG1 register, including the setting of the baud rate, the setting of the number of frames used, the setting of various delay times, etc.;

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Step2. Set the SPI_CFG2 register, including the data shift sequence setting, the setting of the allowable bit of various delays, the setting of the data format and the clock polarity phase, etc.;

Step3. If you need to use interrupt, set the interrupt register of the system;

Step4. If you need to use DMA, set the relevant register for DMA;

Step5. Set the input/output pin;

Step6. Set the SPI_CR register, including the mode and operation mode settings, self-diagnosis function settings, parity check settings, etc.;

Step7. Confirm the setting of SPI_CR register;

Step8. Clear various flag bits;

Step9. Set the interrupt permission bit;

Step10. Set the SPI_CR.SPE bit to 1 and the action starts.

25.3.4.5 Slave Action in Clock Synchronous Operation Mode

Action Description as Slave

When the SPI_CFG2.CPHA bit is 0, the SPI needs to detect that the SS0 input signal becomes an active level as a trigger signal to start serial communication. Since the SS0 pin is not used in the clock synchronous operation mode, the following sequence must be followed for normal communication:

Step1. Set up communication and set the SPI_CR.SPE to 1;

Step2. Set SPI_CFG2.CPHA to 1;

Step3. Set SPI_CFG1.CTMDS to 1;

Step4. Write transmit data to SPI_DR;

Step5. Set SPI_CFG2.CPHA to 0;

Step6. Waiting for the master clock to start communicating.

When the CPHA bit is 1, if SPI detects the original SCK edge when the SS0 input signal is at an active level, it needs to start to drive active data to the MISO output signal. Since the SS0 pin is not used in the clock synchronous mode of operation, when the CPHA bit is 1, the first SCK edge is considered as the trigger signal to start the serial transmission.

If SPI detects the start of serial delivery in the SHIFTER empty state, it changes SHIFTER to full state and cannot transfer data from TX_BUFF to SHIFTER during serial delivery. If SHIFTER is full before starting serial transfer, SPI keeps SHIFTER full.

If SPI detects the SCK edge of the last sampling sequence, the current serial transmission concludes. When RX_BUFF is empty, SPI copies the data from SHIFTER to RX_BUFF after serial delivery. The data can be read by accessing SPI_DR. SPI changes SHIFTER to an empty state after serial delivery, independent of the state of RX_BUFF.

The final sampling timing depends on the bit length of the transmitted data, and the data length of the SPI in slave mode depends on SPI_CFG2.DSIZE.

Slave Initialization in Clock Synchronous Operation Mode

Step1. Set the SPI_CFG1 register, mainly including the setting of the number of frames used;

Step2. Set the SPI_CFG2 register, including transmission rate, data format and clock polarity phase setting, etc.;

Step3. If you need to use interrupt, set the interrupt register of the system;

Step4. If you need to use DMA, set the relevant register for DMA;

Step5. Set the input/output pin;

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Step6. Set the SPI_CR register, including the mode and operation mode settings, self-diagnosis function settings, parity check settings, etc.;

Step7. Confirm the setting of SPI_CR register;

Step8. Clear various flag bits;

Step9. Set the interrupt permission bit;

Step10. Set the SPI_CR.SPE bit to 1 and the action starts.

25.3.4.6 Processing Flow of Several SPI Actions

SPI Data Transmission Process as Master

Step1. Wait for the interrupt of the data transmit buffer being empty or confirm that the data transmit buffer is in an empty state by polling;

Step2. Writes the transmit data to SPI_DR register;

Step3. Repeat steps 1 and 2 until the final data is transmitted;

Step4. Reset the allowable bit TXIE of transmit data register empty interrupt, and set the allowable bit IDIE of SPI idle state interrupt to 1;

Step5. The hardware generates an SPI idle state interrupt;

Step6. Set SPE to 0, stop SPI, and reset IDIE.

Data Reception Process

Step1. Wait for the full interrupt of the data receive buffer register or confirm by polling that the data receive buffer register is full;

Step2. Read data from the receive buffer register by accessing SPI_DR;

Step3. Repeat steps 1 and 2 until the last received data is read;

Step4. Clears the RXIE bit for the full interrupt of the data receive buffer register.

Communication Error Process

Step1. Wait for the communication error interrupt or confirm that the communication error flag bit (MODFERF/OVERRF/UDRERF/PERF) is set to 1 by polling;

Step2. Verify SS0 status and troubleshoot mode errors;

Step3. Clear SPE and stop SPI;

Step4. Identify the types of communication errors by error flag bits and handle them;

Step5. Clear the error flag bit;

Step6. Start SPI and restart the communication.

25.3.5 Self-diagnosis of Parity

Parity check circuit is composed of parity check bits for transmitting data and error detection part for receiving data. You can use the self-diagnosis function to diagnose the fault of the parity circuit as shown in the following figure.

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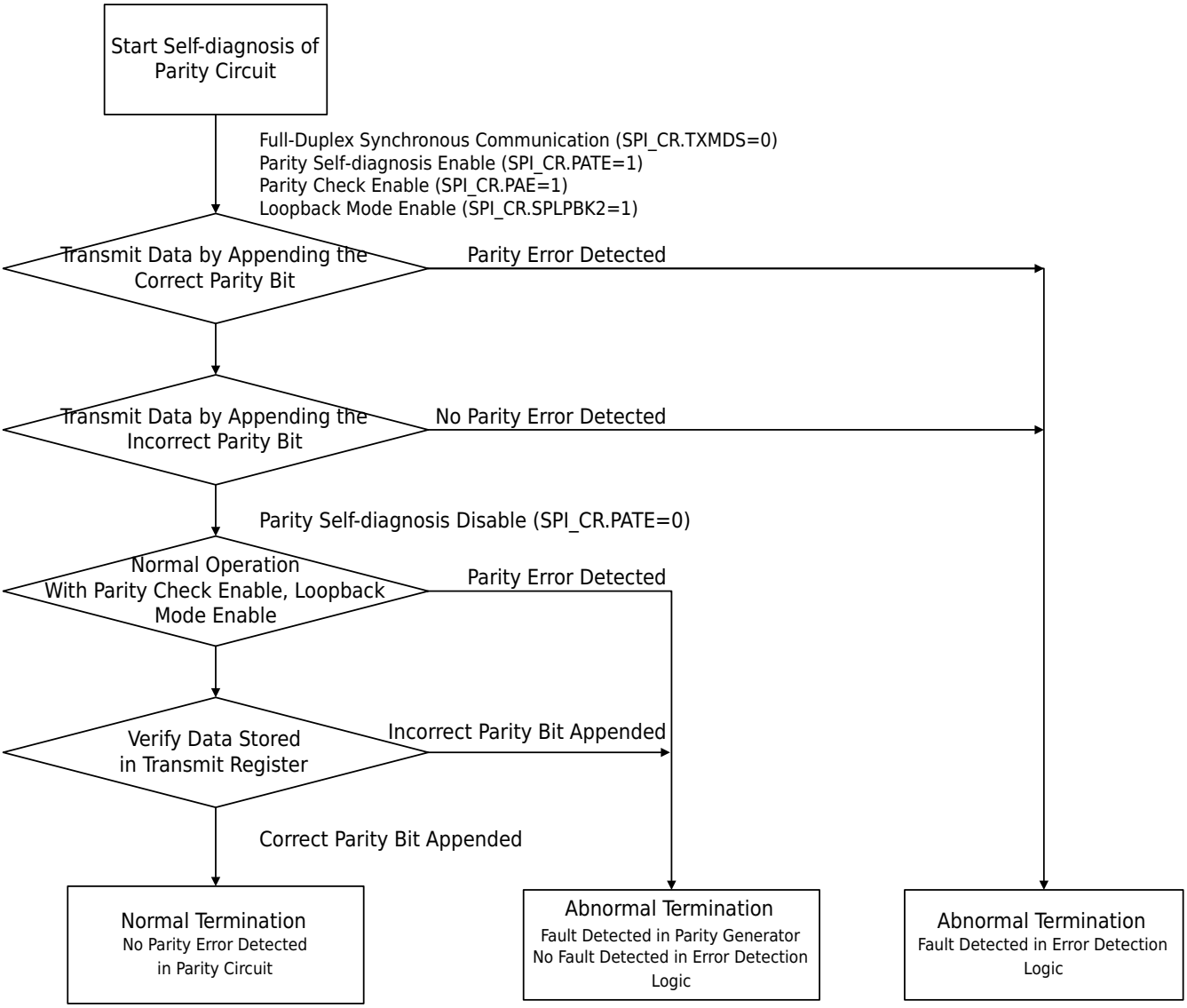

Figure 25-15 Parity Check Process

25.3.6 Error Detection

25.3.6.1 Error Detection Overview

In the normal SPI serial transmission, the system writes the data serially to SPI_DR register and obtains the data serially received by reading SPI_DR register. However, due to the status of the transmit/receive buffer and the SPI at the start/end of serial delivery, abnormal delivery may occur in some cases. When an abnormal transfer occurs, SPI detects this transfer as an underload error, an overload error, a parity error, or a mode fault error. The correspondence between abnormal transmission and SPI error detection is shown in the following table.

Table 25-7 Error Detection Correspondence Table

SN	Occurrence Condition	SPI Operation	Detect Errors
①	Write SPI_DR register in full transmit buffer	Hold transmit buffer content	No
		Write data loss	
②	Read SPI_DR register when receive buffer is empty	Output last serial received data	No

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SN	Occurrence Condition	SPI Operation	Detect Errors
③	In slave mode, serial delivery begins without data being transferred to the SHIFTER register	Aborting serial transmission	Underload Error
		Loss of sending and receiving data	
		Stop driving MISO output signal	
		Stop SPI function	
④	Slave mode: The active level width of the SS0 pin does not reach the time required for data transmission	Abort transmission	Mode Error
		Loss of sending and receiving data	
		Stop SPI function	
⑤	A new frame is received again in full receive buffer	Hold receive buffer content	Overload Error
		Loss of received data	
⑥	Error parity bits are received in full-duplex synchronous serial communication and the parity function is active	Parity error flag is valid	Parity Error

In case ① described, SPI does not detect errors. To prevent data omissions during data write to SPI_DR register, data must be written to SPI_DR register by an empty interrupt of the transmit buffer. Similarly in case ②, SPI does not detect errors. To prevent unrelated data from being read, SPI_DR data read must be done by a full interrupt request of receive register.

25.3.6.2 Underload Error

When the MSTR bit is 0, the SPI operates in the slave state. If the SPE is set to 1, the transmission data is not ready before the SS0 pin receives a active level, and the SPI has an underload error, SPI_SR.MODFERF and SPI_SR.UDRERF will be set to 1.

When an underload error is detected, SPI will stop driving signal output, and SPI_CR.SPE is set to 0.

Monitoring of underload errors can be done by accessing SPI_SR register directly, or by using SPI error interrupt to read SPI_SR. If you do not use the error interrupt, use the polling method to monitor for unloaded errors.

When SPI_SR.MODFERF is 1, the system disables writing 1 to SPE bits. To set SPI_CR.SPE to 1 to enable the SPI function, the MODFERF flag must be cleared to 0 first.

25.3.6.3 Mode Error

When SPI is in master mode, please do not set SPI_CR.MODFE to 1. In slave mode, when the SSi active level width does not reach the time required for data transmission, a mode fault occurs, SPI_SR.MODFERF is set to 1, and SPI_CR.SPE is set to 0. When transmission is required, set SPI_CR.SPE to 1 after clearing SPI_SR.MODFREF.

25.3.6.4 Overload Error

SPI_SR.OVRERF flag is set to 1 (Overload error occurred) if serial delivery is ended when receive buffer is full. Since SPI does not copy the data of the SHIFTER register to the receive buffer in the case of the OVRERF flag is 1, the receive buffer stores the received data before the error occurs. The OVRERF flag only can be written to 0 after the SPI_SR register is read when the OVRERF flag is 1.

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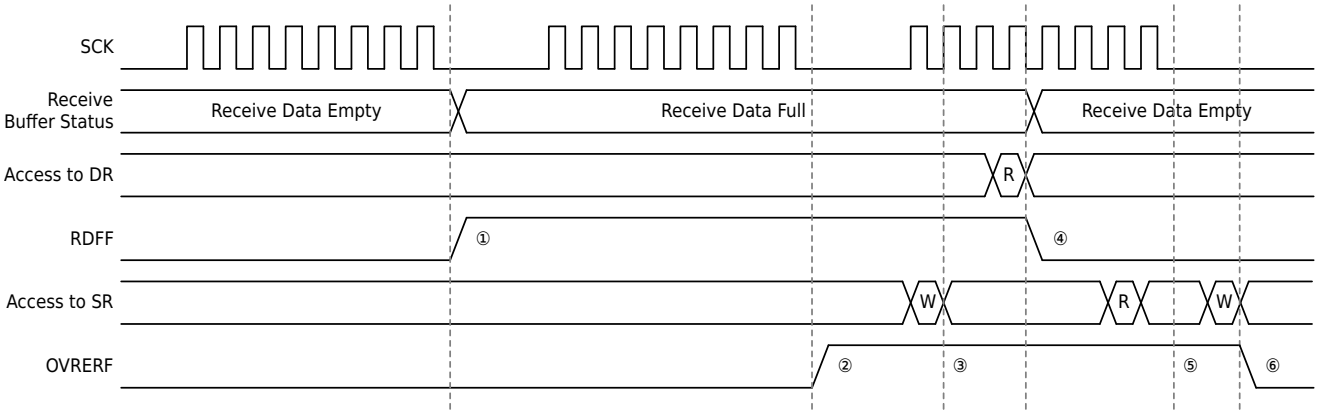

Figure 25-16 Overload Error Pocessing

The following describes the operation content of the flags in the sequence shown in ①-⑥ in the figure:

① When the receive buffer is empty, the serial transmission ends, the SPI operates normally, the data of the SHIFTER register is copied to the receive buffer, and the RDFF flag is set to 1.

② At the end of the serial transfer with the receive buffer full, the SPI detects an overload error and sets the OVRERF flag to 1. SPI will not copy the data of the SHIFTER register to the receive buffer. Even when the PAE bit is 1, a parity error is not detected.

③ Clear the OVRERF flag.

④ Read access to SPI_DR register allows the SPI to read the data in the receive buffer. The RDFF flag becomes 0. Even if the receive buffer status is empty at this time, the OVRERF flag will not become 0.

⑤ When the serial transmission ends when the OVRERF flag is 1 (overload error), the SPI will not copy the data of the SHIFTER register to the receive buffer, nor will it generate a receive buffer full interrupt, and the RDFF flag will remain at 0. Even if the PAE bit is 1, no parity error is detected. In the state where an overload error occurs, if the serial transmission ends without copying the received data from the SHIFTER register to the receive buffer, the SPI judges that the SHIFTER register is in an empty state and allows data to be transferred from the transmit buffer to the SHIFTER register.

⑥ Normal reception operation can only be performed after the OVRERF flag changes to 0.

Monitoring overload errors can be done by accessing the SPI_SR register directly or using the SPI error interrupt to access the SPI_SR register. When performing serial transmission, the occurrence of overload errors must be detected as early as possible by methods such as reading the SPI_SR register immediately after reading the SPI_DR register.

In master mode, if the communication automatic suspend function is enabled (set the SPI_CR.CSUSPE bit to 1), the SPI will suspend the communication clock in the last sampling period before the overload error occurs. At this time, since the SHIFTER register has not completed the reception of the last bit, the SPI remains in the normal communication state and the overload error will not occur. The receive buffer can be read during the communication clock pause. After reading, the receive buffer status becomes empty, and the SPI restarts the communication clock to complete the reception of the last bit of data.

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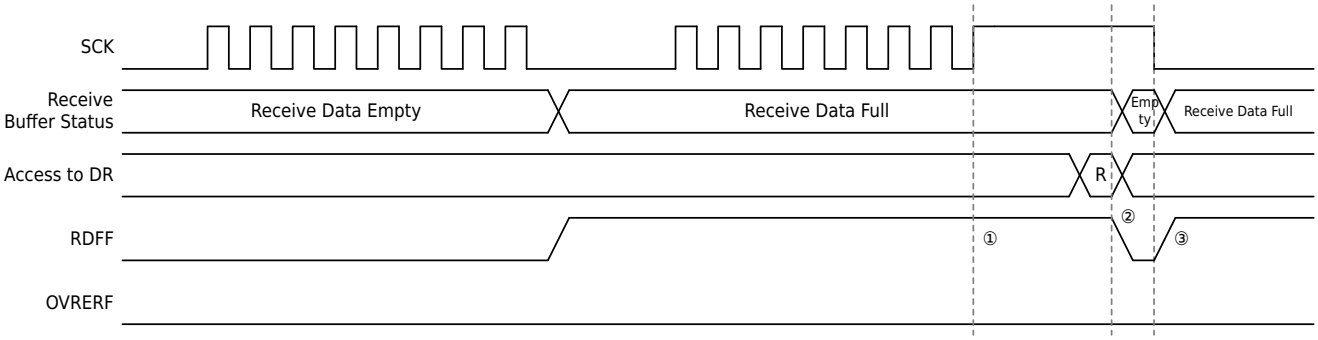

Figure 25-17 Schematic Diagram of Action when Clock Automatic Stop Function Enabled (CPHA=1)

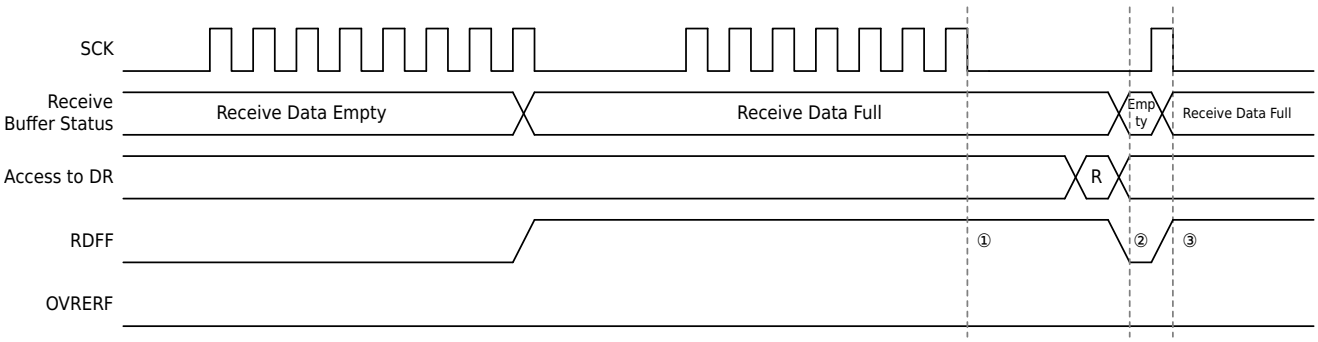

Figure 25-18 Schematic Diagram of Action when Clock Automatic Stop Function Enabled (CPHA=0)

The following describes the running contents of the flags in the time product family shown in figures ①-③:

① When the receive buffer is full, the SPI pauses the communication clock before the last bit of data is received. No overload error will occur at this time.

② After reading the data in the receive buffer by accessing SPI_DR, the receive buffer becomes empty, the RDFF flag is cleared, and the SPI restarts the communication clock to complete the last bit of data communication.

③ The last bit of data communication is completed, the receive buffer register becomes full again, the RDFF flag is set to 1, and the received data can be read by accessing SPI_DR.

25.3.6.5 Parity Error

When the SPI_CR.TXMDS bit is 0 and the SPI_CR.PAE bit is 1, the SPI will perform a parity check at the end of full-duplex synchronous serial communication. When SPI detects a parity error in the received data, set the SPI_SR.PERF flag to 1. In the SPI_SR.OVRERF bit 1 state, the received data is not checked for parity errors because SPI does not copy the data of the SHIFTER register to the receive buffer. The PERF flag only can be written to 0 after the SPI_SR register is read when the PERF flag is 1.

The following figure shows an example of the OVRERF flag and the PERF flag in action. In the example in the figure, the SPI performs 8-bit serial transmission of full-duplex synchronous serial communication when the SPI_CR.TXMDS bit is 0 and the SPI_CR.PAE bit is 1.

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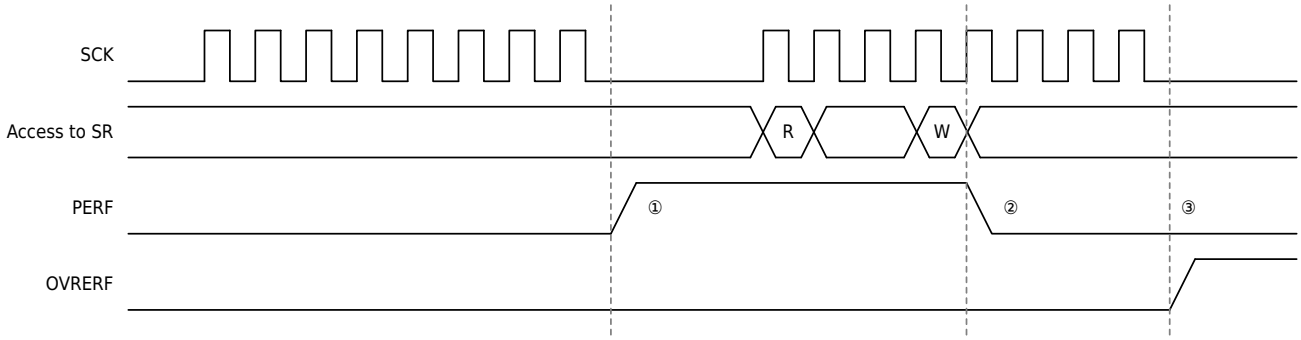

Figure 25-19 Parity Error

The following describes the running contents of the flags in the timing sequence shown in figures ① to ③:

① SPI did not detect an overload error and serial delivery ended normally. SPI copies the data of the SHIFTER register to the receive buffer. At this time, SPI performs parity check on the received data. If a parity error is detected, the PERF flag is set to 1.

② Clear the RERF flag.

③ SPI detects an overload error. At this time, SPI does not copy the data of the SHIFTER register to the receiving buffer, SPI does not perform parity check on the data, and no parity check error occurs.

Monitoring parity errors can be done by accessing the SPI_SR register directly or using the SPI error interrupt to access the SPI_SR register. When performing serial transmission, the occurrence of parity errors must be detected as early as possible by methods such as reading the SPI_SR register.

25.3.7 SPI Initialization

Write operation or mode fault error detection is used to clear SPE bit, which can inactiveate SPI functions and initialize some SPI functions. If a system reset occurs or the function reset register RMU_FRST0 is used, all SPI functions are initialized.

Initialization by Clear SPE Bit

When the SPI_CR.SPE bit is set to 0, the SPI performs the following initialization operations:

- Abort in-progress serial delivery.
- If in slave state, stop driving the output signal (the state changes to Hi-Z).
- SPI internal state is initialized.
- Clear transmit buffer, set SPI_SR.TDEF to 1.

SPI control bits are not initialized by clear SPE bit. As a result, SPI can be started in the same transmission mode as before initialization, as long as SPE is relocated to 1.

Clearing SPE bit does not initialize error flag bits and sequence states. Thus, even after the SPE is cleared, it is possible to confirm the occurrence of errors during SPI transfer by reading the data of the receive buffer.

Clearing SPE bit clears the transmit buffer and sets the SPI_SR.TDEF to 1. Therefore, if the SPI_CR.TXIE bit is set to 1 after initialization, an SPI transmit buffer empty interrupt will be generated. To avoid this interrupt, you must clear the SPE bit to 0 while setting the TXIE bit to 0.

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Initialization by Reset

Initialization by system reset or using the function reset register RMU_FRST0 will initialize all SPI control bits, status bits and data registers. For the contents of the system reset and function reset registers, please refer to the relevant description in the "Reset Module Unit (RMU)" chapter.

25.3.8 Interrupt and Events

The SPI receive buffer full, transmit buffer empty, mode fault (overload, underload, parity error) and SPI idle can be used as interrupt sources or internal trigger sources. Transmission completion can only be used as an internal trigger source.

The interrupt of overload, underload and parity errors is integrated into the SPI error interrupt SPEI, so the actual interrupt source needs to be judged by the flag. The specific description of SPI interrupt/internal trigger source is shown in the following table. Once the condition is met, the corresponding interrupt/internal trigger request is generated. For receive buffer full and transmit buffer empty interrupt sources, data transmission changes buffer status to clear.

Table 25-8 SPI Interrupt Source and Trigger Source Description

Interrupt/Internal Trigger Source	Abbreviation	Interrupt Source	Internal Trigger Source	Condition
Receive buffer full	SPI_SPRI	√	√	When the receive buffer becomes full while the SPI_CR.RXIE bit is 1
Transmit buffer empty	SPI_SPTI	√	√	When the transmit buffer becomes empty while the SPI_CR.TXIE bit is 1
SPI errors (overload, underload, parity errors)	SPI_SPEI	√	√	When the SPI_CR.EIE bit is 1, the SPI_SR.OVRERF, SPI_SR.PERF or SPI_SR.MODFERF and SPI_SR.UDRERF flags become 1.
SPI idle	SPI_SPII	√	√	When the SPI_CR.IDIE bit is 1: ● Master mode: Data transmissions is completed or SPI_CR.SPE is written from 1 to 0. ● Slave mode: SPI_CR.SPE is written from 1 to 0.
Data transmission completed	SPI_SPEND	-	√	● Master mode: Data transmission completed. ● Slave mode: Four-wire, when the SSL pin is at an inactive level; three-wire, when the SCK pin clock reaches the number of clocks required for data transmission

The user can write the vectors that can be used as trigger sources in the above table into different trigger object registers to implement various event trigger functions. For the vectors corresponding to the above event trigger sources, please refer to the "Interrupt Event List" in the "Interrupt Controller (INTC) " chapter.

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25.4 Register Description

25.4.1 Register List

Base address: 0x4001C000

Table 25-9 Serial Peripheral Interface (SPI) Register Offset

Offset	Register	Description	Width
0x00	SPI_DR	SPI Data Register	32
0x04	SPI_CR	SPI Control Register	32
0x0C	SPI_CFG1	SPI Config Register 1	32
0x14	SPI_SR	SPI Status Register	32
0x18	SPI_CFG2	SPI Config Register 2	32

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25.4.2 SPI Data Register (SPI_DR)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	SPD																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	SPD	Serial Data SPI data storage	RW

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25.4.3 SPI Control Register (SPI_CR)

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																PAE	PAOE	PATE	MODFE	IDIE	RXIE	TXIE	EIE	CSUSPE	SPE	SPLPBK2	SPLPBK	MSTR	Reserved	TXMDS	SPIMDS
Access																	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15	PAE	Parity Enabled ● 0b0: Transmit data without parity bit, receive data without parity check ● 0b1: Transmit data with parity bit, receive data with parity check (SPI_CR.TXMDS=0); Transmit data with parity bit, receive data without parity check (SPI_CR.TXMDS=1)	RW
14	PAOE	Parity Mode Selection ● 0b0: Select even check for sending and receiving ● 0b1: Select odd check for sending and receiving	RW
13	PATE	Parity Self-diagnosis ● 0b0: Parity self-diagnosis function inactive ● 0b1: Parity self-diagnosis function active	RW
12	MODFE	Mode Fault Error Detection Enabled ● 0b0: Disable mode fault error detection ● 0b1: Enable mode fault error detection	RW
11	IDIE	SPI Idle Interrupt Enabled ● 0b0: Disable generation of idle interrupt requests ● 0b1: Enable generation of idle interrupt requests	RW
10	RXIE	SPI Receive Interrupt Enabled ● 0b0: Disable generation of SPI receive interrupt requests ● 0b1: Enable generation of SPI receive interrupt requests	RW
9	TXIE	SPI Transmit Interrupt Enabled ● 0b0: Disable generation of SPI transmit interrupt requests ● 0b1: Enable generation of SPI transmit interrupt requests	RW
8	EIE	SPI Error Interrupt Enabled ● 0b0: Disable generation of SPI error interrupt requests ● 0b1: Enable generation of SPI error interrupt requests	RW
7	CSUSPE	Communication Auto Suspend Function Enabled ● 0b0: Communication auto suspend function inactive ● 0b1: Communication auto suspend function active	RW

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Bit	Name	Functional Description	Access
6	SPE	SPI Function Enabled ● 0b0: SPI function disabled ● 0b1: SPI function enabled	RW
5	SPLPBK2	SPI Loop 2-bit ● 0b0: Normal mode ● 0b1: Loopback mode (transmit data=receive data)	RW
4	SPLPBK	SPI Loopback Position ● 0b0: Normal mode ● 0b1: Loopback mode (inverted phase of transmit data=received data)	RW
3	MSTR	SPI Master-slave Mode Selection ● 0b0: Slave mode ● 0b1: Master mode	RW
2	*Reserved*	-	-
1	TXMDS	Communication Mode Selection ● 0b0: Full-duplex synchronous serial communication ● 0b1: Transmit serial communication only	RW
0	SPIMDS	SPI Mode Selection ● 0b0: SPI operation (4-wire) ● 0b1: Clock synchronous operation (3-wire)	RW

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25.4.4 SPI Config Register 1 (SPI_CFG1)

Offset	Bit Position																													
0x0C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000010																															
Name	Reserved	MIDI			Reserved	MSSDL			Reserved	MSSI			Reserved				CLKDIV				SS3PV	SS2PV	SS1PV	SS0PV	Reserved	SPRDTD	Reserved			CTMDS	FTHLV	
Access		RW				RW				RW							RW				RW	RW	RW	RW		RW				RW	RW	

Bit	Name	Functional Description	Access
31	*Reserved*	-	-
30:28	MIDI	Master Next Access Data Interval Idle Time Setting Bit ● 0b000: 1 SCK + 2 PCLK1s ● 0b001: 2 SCKs + 2 PCLK1s ● 0b010: 3 SCKs + 2 PCLK1s ● 0b011: 4 SCKs + 2 PCLK1s ● 0b100: 5 SCKs + 2 PCLK1s ● 0b101: 6 SCKs + 2 PCLK1s ● 0b110: 7 SCKs + 2 PCLK1s ● 0b111: 8 SCKs + 2 PCLK1s	RW
27	*Reserved*	-	-
26:24	MSSDL	Master SS Inactive Delay Setting Bit ● 0b000: 1 SCK ● 0b001: 2 SCKs ● …… ● 0b110: 7 SCKs ● 0b111: 8 SCKs	RW
23	*Reserved*	-	-
22:20	MSSI	Master SS Idle Time Setting Bit ● 0b000: 1 SCK ● 0b001: 2 SCKs ● …… ● 0b110: 7 SCKs ● 0b111: 8 SCKs	RW
19:16	*Reserved*	-	-
15:12	CLKDIV	Communication Reference Clock Selection Bit ● 0000: PCLK1/2 ● 0001: PCLK1/4 ● 0010: PCLK1/6 ● 0011: PCLK1/8 ● 0100: PCLK1/10 ● 0101: PCLK1/12 ● 0110: PCLK1/14	RW

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Bit	Name	Functional Description	Access
15:12	CLKDIV	● 0111: PCLK1/16 ● 1000: PCLK1/18 ● 1001: PCLK1/20 ● 1010: PCLK1/22 ● 1011: PCLK1/24 ● 1100: PCLK1/26 ● 1101: PCLK1/28 ● 1110: PCLK1/30 ● 1111: PCLK1/32	RW
11	SS3PV	Polarity Setting of SS3 Signal ● 0b0: Low level active ● 0b1: High level active	RW
10	SS2PV	Polarity Setting of SS2 Signal ● 0b0: Low level active ● 0b1: High level active	RW
9	SS1PV	Polarity Setting of SS1 Signal ● 0b0: Low level active ● 0b1: High level active	RW
8	SS0PV	Polarity Setting of SS0 Signal ● 0b0: Low level active ● 0b1: High level active	RW
7	*Reserved*	-	-
6	SPRDTD	Data Register Read Target Selection ● 0b0: SPI_DR read receive buffer ● 0b1: SPI_DR read transmit buffer (Can only be read when TDEF=1)	RW
5	*Reserved*	-	-
4	*Reserved*	*Reads as 1, Write as 1*	-
3	*Reserved*	-	-
2	CTMDS	Continuous Communication Mode Selection ● 0b0: Normal communication mode ● 0b1: Continuous communication mode	RW
1:0	FTHLV	Frames Setting Bit ● 0b00: 1 frame ● 0b01: 2 frames ● 0b10: 3 frames ● 0b11: 4 frames	RW

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25.4.5 SPI Status Register (SPI_SR)

Offset	Bit Position																													
0x14	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000020																															
Name	Reserved																								RDFF	FMIDLF	TDEF	UDRERF	PERF	MODFERF	IDLNF	OVRERF
Access																									RO	RO	RO	RW	RW	RW	RO	RW

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7	RDFF	Receive Buffer Full Flag Hardware set and clear ● 0b0: The receive buffer is not full ● 0b1: The receive buffer is full	RO
6	FMIDLF	IDLE Status Flag of Master in Continuous Mode Hardware set and clear ● 0b0: Continuous mode master is in normal operation state ● 0b1: Continuous mode master is in idle state	RO
5	TDEF	Transmit Buffer Empty Flag Hardware set and clear ● 0b0: Data present in transmit buffer ● 0b1: No data present in the transmit buffer	RO
4	UDRERF	Underload Error Flag Hardware set; read this bit as 1 and then write 0 to clear the status bit ● 0b0: No underload error occurred ● 0b1: Underload error occurred (MODFERF=1) **Note** When MODFERF=0, this bit will be initialized.	RW
3	PERF	Parity Error Flag Hardware set; read this bit as 1 and then write 0 to clear the status bit ● 0b0: No parity error occurred ● 0b1: Parity error occurred	RW
2	MODFERF	Mode Fault Error Flag Hardware set; read this bit as 1 and then write 0 to clear the status bit ● 0b0: No mode fault error occurred ● 0b1: Mode fault error occurred	RW

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Bit	Name	Functional Description	Access
1	IDLNF	SPI Idle Flag Hardware set and clear ● 0b0: SPI is in idle state ● 0b1: SPI is in transmission state	RO
0	OVRERF	Overload Error Flag Hardware set; read this bit as 1 and then write 0 to clear the status bit ● 0b0: No overload error occurred ● 0b1: Overload error occurred	RW

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25.4.6 SPI Config Register 2 (SPI_CFG2)

Offset	Bit Position																													
0x18	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000F1D																															
Name	Reserved																MSSIE	MSSDLE	MIDIE	LSBF	DSIZE				SSA	Reserved	MBR			CPOL	CPHA	
Access																	RW	RW	RW	RW	RW				RW		RW			RW	RW	

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15	MSSIE	SCK Delay Enabled ● 0b0: SCK delay is 1 SCK period ● 0b1: SCK delay is the value set by MSSI	RW
14	MSSDLE	SS Invalid Delay Enabled ● 0b0: SS invalid delay is 1 SCK ● 0b1: SS invalid delay is the value set by MSSDL	RW
13	MIDIE	SPI Next Access Delay Enabled ● 0b0: The next access delay is 1 SCK+2 PCLK1 ● 0b1: The next access delay is the value set by MIDI	RW
12	LSBF	SPI LSB First Bit ● 0b0: MSB first ● 0b1: LSB first	RW
11:8	DSIZE	SPI Data Length Setting Bit ● 0b0000: 4 bits ● 0b0001: 5 bits ● 0b0010: 6 bits ● 0b0011: 7 bits ● 0b0100: 8 bits ● 0b0101: 9 bits ● 0b0110: 10 bits ● 0b0111: 11 bits ● 0b1000: 12 bits ● 0b1001: 13 bits ● 0b1010: 14 bits ● 0b1011: 15 bits ● 0b1100: 16 bits ● 0b1101: 20 bits ● 0b1110: 24 bits ● 0b1111: 32 bits	RW

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Bit	Name	Functional Description	Access
7:5	SSA	SS Signal Enabled Setting Bit ● 0b000: SS0 ● 0b001: SS1 ● 0b010: SS2 ● 0b011: SS3 ● Others: Setting prohibited	RW
4	*Reserved*	*Reads as 1, Write as 1*	-
3:2	MBR	Bit Rate Frequency Division Setting Bit ● 0b00: Select the reference communication clock ● 0b01: Select the 2-division of the reference communication clock ● 0b10: Select the 4-division of the base communication clock ● 0b11: Select the 8-division of the base communication clock	RW
1	CPOL	SCK Polarity Setting Bit ● 0b0: SCK is low level when idle ● 0b1: SCK is high level when idle	RW
0	CPHA	SCK Phase Setting Bit ● 0b0: Data sampling at odd edges, changing at even edges ● 0b1: Data changing at odd edges, sampling at even edges	RW

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26 CRC Operation (CRC)

26.1 Introduction

In many applications, CRC algorithms are required to verify the integrity and correctness of data. Especially in data transmission, CRC checking is widely used. This module can use 11 algorithms, including CRC16/CCITT, CRC16/CCITT-FALSE, CRC16/XMODE, CRC16/IBM, CRC16/MAXIM, CRC16/USB, CRC16/MODBUS, CRC16/X25, CRC32, CRC32/MPEG-2 and CRC64, to calculate and check the data.

26.2 Functional Description

26.2.1 Function Block Diagram

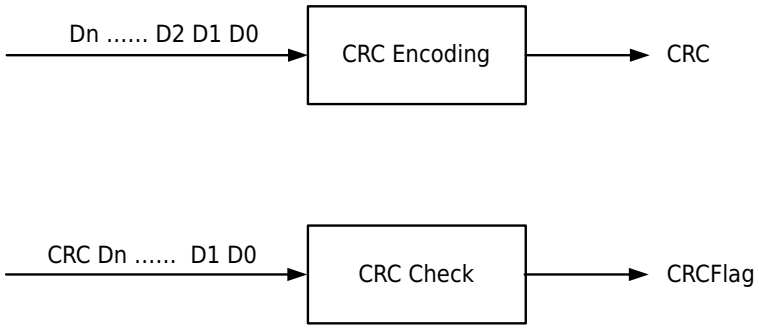

Figure 26-1 CRC Application Diagram

26.2.2 CRC Parameter Model

The CRC algorithm of this module complies with the definition of ISO/IEC13239, using 16-bit, 32-bit, and 64-bit CRC respectively. The corresponding parameter models for each CRC algorithm are shown in the table below.

Table 26-1 CRC Parameter Model

CRC Algorithm Name	Polynomial Formula	Initial Value	Result XOR Value	Input Inversion	Output Inversion
CRC16/IBM	$X^{16}+X^{15}+X^{2}+1$	0x0000	0x0000	Yes	Yes
CRC16/MAXIM	$X^{16}+X^{15}+X^{2}+1$	0x0000	0xFFFF	Yes	Yes
CRC16/USB	$X^{16}+X^{15}+X^{2}+1$	0xFFFF	0xFFFF	Yes	Yes
CRC16/MODBUS	$X^{16}+X^{15}+X^{2}+1$	0xFFFF	0x0000	Yes	Yes
CRC16/CCITT	$X^{16}+X^{12}+X^{5}+1$	0x0000	0x0000	Yes	Yes
CRC16/CCITT-FALSE	$X^{16}+X^{12}+X^{5}+1$	0xFFFF	0x0000	No	No
CRC16/X25	$X^{16}+X^{12}+X^{5}+1$	0xFFFF	0xFFFF	Yes	Yes
CRC16/XMODEM	$X^{16}+X^{12}+X^{5}+1$	0x0000	0x0000	No	No
CRC32	$X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$	0xFFFFFFFF	0xFFFFFFFF	Yes	Yes

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CRC Algorithm Name	Polynomial Formula	Initial Value	Result XOR Value	Input Inversion	Output Inversion
CRC32/MPEG-2	$X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$	0xFFFFFFFF	0x00000000	No	No
CRC64	$X^{64}+X^{4}+X^{3}+X+1$	0xFFFFFFFFFFFFFFFF	0xFFFFFFFFFFFFFFFF	Yes	Yes

The functions of this module include:

- CRC encoding and CRC check
- 3 bit width access methods: 8-bit, 16-bit, 32-bit:
  - Example of input data with 8-bit bit width: 0x00, 0x11, 0x22, 0x33, 0x44, 0x55, 0x66, 0x77;
  - Example of input data with 16-bit bit width: 0x1100, 0x3322, 0x5544, 0x7766;
  - Example of input data with 32-bit bit width: 0x33221100, 0x77665544.

26.2.3 CRC16 Encoding Mode

CRC encoding is the process of encoding the original data to calculate its CRC value. The operating procedures are as follows:

1. Write 0b0 to CRC_CR.CR and write corresponding data to CRC_CR.SELECT, selecting the corresponding CRC16 specification algorithm.
2. Initialize CRC calculation by writing 0x0000 or 0xFFFF to CRC_RESLT1[15:0] according to the CRC parameter model.
3. Organize the original data to be encoded into 8-bit/16-bit/32-bit formats and write them into CRC_DAT register sequentially.

   Note
   When writing the CRC value in 8-bit format, write the low bits first and then the high bits.

4. Read CRC_RESLT1[15:0] to obtain the 16-bit CRC encoded value.

26.2.4 CRC16 Check Mode

The check mode can verify whether the encoded data has been tampered. The operating procedures are as follows:

1. Write 0b0 to CRC_CR.CR and write corresponding data to CRC_CR.SELECT, selecting the corresponding CRC16 specification algorithm.
2. Initialize CRC calculation by writing 0x0000 or 0xFFFF to CRC_RESLT1[15:0] according to the CRC parameter model.
3. Write the encoded data into CRC_DAT register sequentially in 8-bit, 16-bit, or 32-bit organization.

   Note
   When writing the CRC value in 8-bit format, write the low bits first and then the high bits.

4. Write the check code into the CRC_DAT register with a 16-bit bit width.

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Note

For CRC16/CCITT-FALSE and CRC16/XMODEM, the check code needs to be swapped between the high 8 bits and low 8 bits.

For example: 0x1234-> 0x3412

5. Read the value of CRC_CR.FLAG. A value of 1 indicates check success, and a value of 0 indicates check failure.

26.2.5 CRC32 Encoding Mode

CRC encoding is the process of encoding the original data to calculate its CRC value. The operating procedures are as follows:

1. Write 0b1 to CRC_CR.CR and write corresponding data to CRC_CR.SELECT, selecting the corresponding CRC32 specification algorithm.
2. Write 0xFFFFFFFF to CRC_RESLT1[31:0] to initialize CRC calculation.
3. Organize the original data to be encoded into 8-bit/16-bit/32-bit formats and write them into CRC_DAT register sequentially.

Note

When writing the CRC value in 8-bit format, write the low bits first and then the high bits.

4. Read CRC_RESLT1[31:0] to obtain the 32-bit CRC encoded value.

26.2.6 CRC32 Check Mode

The check mode can verify whether the encoded data has been tampered with. The operating procedures are as follows:

1. Write 0b1 to CRC_CR.CR and write corresponding data to CRC_CR.SELECT, selecting the corresponding CRC32 specification algorithm.
2. Write 0xFFFFFFFF to CRC_RESLT1[31:0] to initialize CRC calculation.
3. Write the encoded data into CRC_DAT register sequentially in 8-bit, 16-bit, or 32-bit organization.

Note

When writing the CRC value in 8-bit format, write the low bits first and then the high bits.

4. Write the check code into the CRC_DAT register in 8-bit, 16-bit, or 32-bit organization.

Note

For CRC32/MPEG-2, during check, the high 16 bits and low 16 bits need to be swapped, and within each 16-bit section, the high 8 bits and low 8 bits also need to be swapped.

For example: 0x12345678->0x78563412

5. Read the value of CRC_CR.FLAG. A value of 1 indicates check success, and a value of 0 indicates check failure.

26.2.7 CRC64 Encoding Mode

CRC encoding is the process of encoding the original data to calculate its CRC value. The operating procedures are as follows:

1. Write 0b1 to CRC_CR.CR and write corresponding data to CRC_CR.SELECT, selecting the corresponding CRC64 specification algorithm.

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2. Write 0xFFFFFFFF to CRC_RESLT1[31:0] and CRC_RESLT2[31:0] to initialize CRC calculation.
3. Organize the original data to be encoded into 8-bit/16-bit/32-bit formats and write them into CRC_DAT register sequentially.

> **Note**
> When writing the CRC value in 8-bit format, write the low bits first and then the high bits.

4. Read CRC_RESLT1[31:0] and CRC_RESLT2[31:0] to obtain the 64-bit CRC encoded value.

> **Note**
> CRC64_DATA= {CRC_RESLT2[31:0], CRC_RESLT1[31:0]}.

26.2.8 CRC64 Check Mode

The check mode can verify whether the encoded data has been tampered. The operating procedures are as follows:

1. Write 0b1 to CRC_CR.CR and write corresponding data to CRC_CR.SELECT, selecting the corresponding CRC64 specification algorithm.
2. Write 0xFFFFFFFF to CRC_RESLT1[31:0] and CRC_RESLT2[31:0] to initialize CRC calculation.
3. Write the encoded data into CRC_DAT register sequentially in 8-bit, 16-bit, or 32-bit organization.

> **Note**
> When writing the CRC value in 8-bit format, write the low bits first and then the high bits.

4. Write the check code into the CRC_DAT register in 8-bit, 16-bit, or 32-bit organization.
5. Read the CRC_CR.FLAG register. A value of 1 indicates check success, and a value of 0 indicates check failure.

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26.3 Register Description

26.3.1 Register List

Base address: 0x40050400

Table 26-2 CRC Operation (CRC) Register Offset

Offset	Register	Description	Width
0x00	CRC_CR	CRC Control Register	32
0x04	CRC_RESLT1	CRC Result Register 1	32
0x08	CRC_RESLT2	CRC Result Register 2	32
0x80-0xFC	CRC_DAT	CRC Data Register	32

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26.3.2 Control Register (CRC_CR)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000001																															
Name	Reserved																											SELECT			FLAG	CR
Access																												RW			RO	RW

Bit	Name	Functional Description	Access
31:5	*Reserved*	-	-
4:2	SELECT	CRC Selection Bit **When CR=0b0, Bit4-2 correspond to CRC algorithm selection:** ● 0b000: CRC16/X25 ● 0b001: CRC16/CCITT ● 0b010: CRC16/CCITT-FALSE ● 0b011: CRC16/XMODEM ● 0b100: CRC16/IBM ● 0b101: CRC16/MAXIM ● 0b110: CRC16/USB ● 0b111: CRC16/MODBUS **When CR=0b1, Bit4-2 correspond to CRC algorithm selection:** ● 0b000: CRC32 ● 0b001: CRC32/MPEG-2 ● 0b010: CRC64 ● Others: Setting prohibited	RW
1	FLAG	Check Result Bit ● 0b0: Current check error ● 0b1: Current check correct	RO
0	CR	Operational Control Bit ● 0b0: CRC16 ● 0b1: CRC32/CRC64	RW

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26.3.3 Result Register 1 (CRC_RESLT1)

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	RESULT1																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	RESULT1	Result bit ● When CRC16 is selected, use RESULT1[15:0]. ● When CRC32 is selected, use RESULT1[31:0]. ● When selecting CRC64, CRC_RESLT1 and CRC_RESLT2 are used jointly. CRC_RESLT1.RESULT1[31:0] corresponds to CRC result Bit31-Bit0; CRC_RESLT2.RESULT2[31:0] corresponds to CRC result Bit63-Bit32	RW

26.3.4 Result Register 2 (CRC_RESLT2)

Offset	Bit Position																													
0x08	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	RESULT2																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	RESULT2	Result bit When selecting CRC64, CRC_RESLT1 and CRC_RESLT2 are used jointly: ● CRC_RESLT1.RESULT1[31:0] corresponds to CRC result Bit31-Bit0 ● CRC_RESLT2.RESULT2[31:0] corresponds to CRC result Bit63-Bit32	RW

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26.3.5 Data Register (CRC_DAT)

Offset	Bit Position																													
0x80-0xFC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	CRC_DAT																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	CRC_DAT	Data for operation Write the data to be operated on; reads always as 0.	RW

Note

CRC_DAT register is at the 0x80 offset from the CRC base address. The 0x84-0xFC offset from the base address are the mapping addresses of the CRC_DAT register, with the same access and operation permissions as the CRC_DAT register.

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27 Data Computing Unit (DCU)

27.1 Introduction

The Data Computing Unit (DCU) is a simple data processing block that does not rely on the CPU. Each DCU unit has three data registers capable of performing addition, subtraction, comparison, and window comparison functions on two data values. This product is equipped with 1 DCU unit.

27.2 Features

- Supports 4 types of data processing: addition, subtraction, comparison of 2 data values, and window comparison of 3 data values.
- Addition and subtraction operations are performed on data in the DATA0 and DATA1 registers, with results stored in DATA0. Simultaneously, the result is automatically halved, and the halved result is stored in DATA1.
- Addition and subtraction can be triggered by writing to the register or by events from other peripheral circuits.
- In comparison mode, two data values can be compared between DATA0 and DATA1 registers, as well as between DATA0 and DATA2 registers. Interrupt and flag bits can be generated when the comparison results meet the conditions of greater than, less than, or equal to.
- Compare mode can also be used for window comparison by setting DATA1 and DATA2 as the upper and lower limits of the window, and judging whether DATA0 is within or outside the window based on the comparison results between DATA0 and DATA1, and DATA0 and DATA2.
- Operations can be triggered by events from other peripheral circuits, and various interrupts and event signals can be generated based on the operation results. When other peripheral circuits with hardware trigger start function select DCU as the trigger source, the DCU generates an event signal to start the peripheral circuit's action.

27.3 Functional Description

27.3.1 Addition Mode

The addition mode calculates the sum of DATA0 and DATA1, where DATA0 is used as the summand and DATA1 is used as the addend. Each write to the DATA1 register performs a DATA0 + DATA1 addition operation, with the result stored in DATA0 and the result divided by 2 stored in DATA2. An interrupt and flag bit are generated when the result of DATA0 + DATA1 is greater than 0xFF (8-bit mode) or 0xFFFF (16-bit mode) or 0xFFFFFFFF (32-bit mode).

Application example of addition mode:

Step1. Set the DCU_CTL control register to addition mode with a data width of 16-bit;

Step2. Select the interrupt generation condition in the DCU_INTEVTSEL register;

Step3. Write 0xFF00 and 0x55 to DATA0 and DATA1, respectively. The calculation result is 0xFF55, which is saved in DATA0, and 0xFF55/2 is saved in DATA2;

Step4. Continue writing 0xFF to DATA1. At this point, the calculation result (0xFF55 + 0xFF > 0xFFFF) overflows, generating a result flag. Reading the flag register DCU_FLAG obtains the result flag;

Step5. Write to the flag reset register DCU_FLAGCLR to clear the flag bit.

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27.3.2 Subtraction Mode

The subtraction mode calculates the difference between DATA0 and DATA1, where DATA0 acts as the minuend and DATA1 acts as the subtrahend. Each write to the DATA1 register performs a DATA0-DATA1 subtraction operation. The subtraction result is stored in DATA0, and the result divided by 2 is stored in DATA2. An interrupt and flag bit are generated when the DATA0-DATA1 result is less than 0x0 (in 8-bit, 16-bit, or 32-bit mode).

27.3.3 Hardware Trigger Start Mode

The DCU can trigger and start operations according to events generated by peripheral circuits. When using hardware trigger start mode, first enable the peripheral circuit trigger function in the function clock control register (CMU_FCG). Each DCU unit can independently select trigger start signals from other peripheral circuit, when select start signals, writing the peripheral circuit source number in the trigger source selection register (DCU_TRGSEL). For details of the registers, please refer to the Automatic Operation System (AOS). When the peripheral circuit event occurs, the event signal is input to the DCU to trigger the DCU start operation.

Hardware trigger start mode includes trigger plus mode and trigger minus mode:

- In trigger plus mode, each event trigger initiates a DATA0+DATA1 addition. The result is stored in DATA0, and the result divided by 2 is stored in DATA2. If the result exceeds 0xFF (8-bit mode), 0xFFFF (16-bit mode), or 0xFFFFFFFF (32-bit mode), the flag bit is set and an interrupt is generated.
- In trigger minus mode, each trigger initiates a DATA0-DATA1 subtraction. The result is stored in DATA0, and the result divided by 2 is stored in DATA2. When the result of DATA0-DATA1 is less than 0x0 (in 8-bit, 16-bit, and 32-bit mode), the flag bit is set and an interrupt is generated.

Example application of hardware trigger start mode:

Step1. The control register DCU_CTL selects the trigger plus mode, with a data width of 8-bit;

Step2. The interrupt condition selection register DCU_INTEVTSEL selects the operation conditions;

Step3. Write 0x00 and 0x56 to DATA0 and DATA1 respectively;

Step4. Write the event number in the trigger source selection register DCU_TRGSEL;

Step5. Make the selected peripheral circuit action and generate events, the DCU is triggered to perform an addition operation. The result is 0x56 and saved in DATA0, and 0x56 divided by 2 is saved in DATA2;

Step6. After three consecutive triggers, the calculation result overflows, generating a result flag. Reading the flag register DCU_FLAG obtains the result flag;

Step7. Write to the flag reset register DCU_FLAGCLR to clear the flag bit.

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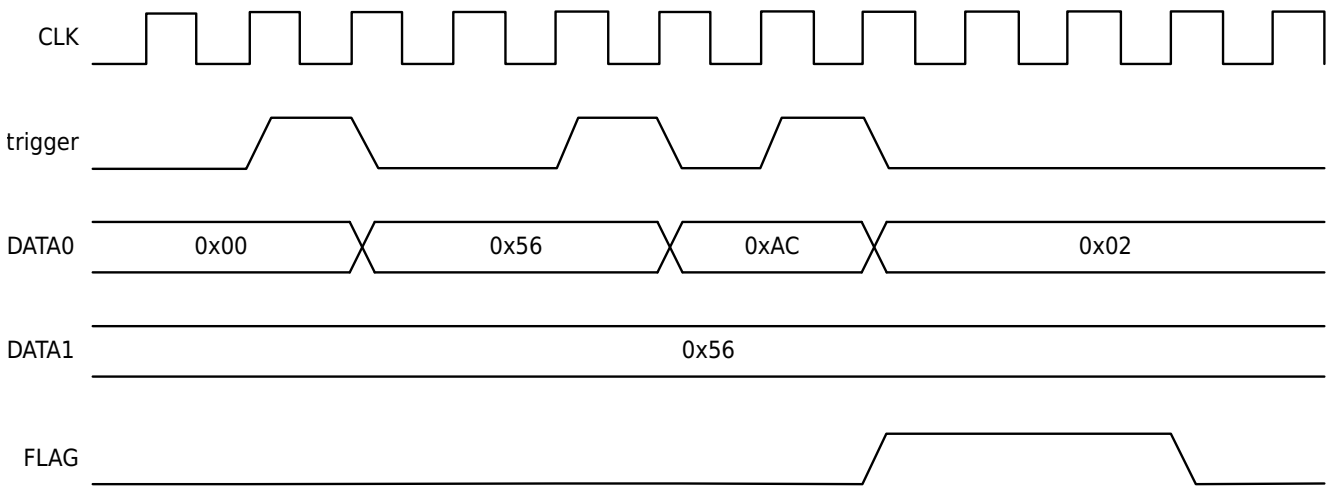

Figure 27-1 Hardware Trigger Start Schematic Diagram

27.3.4 Comparative Mode

Comparing the size of DATA0 and DATA1 and DATA0 and DATA2, it can select when DATA0 is greater than DATA1, DATA0 is less than DATA1, DATA0 is equal to DATA1 and when DATA0 is greater than DATA2, DATA0 is less than DATA2, DATA0 is equal to DATA2, generate a flag and generate an interrupt. In the comparative mode, it can choose the conditions for data comparison, compare after writing DATA0 or write any data register.

Comparative mode application example:

Step1. Select comparative mode in the control register DCU_CTL, with data width of 16-bit. Start comparison after writing to DATA0;

Step2. In the interrupt condition selection register DCU_INTEVTSEL, select to generate a flag when DATA0>DATA1;

Step3. Write 0xBBBB and 0xAAAA to DATA1 and DATA0 respectively. Since DATA0>DATA1 is not satisfied, no flag is generated;

Step4. Write 0x8888 to DATA1. Although DATA0>DATA1 is now satisfied, since it's set to start comparison after writing to DATA0, no flag is generated;

Step5. After writing 0x9999 to DATA0, the flag generation condition is met, and a flag is generated;

Step6. Write to the flag reset register DCU_FLAGCLR to clear the flag bit.

27.3.5 Interrupt and Event

DCU has various interrupts and event outputs for triggering other peripheral circuits for user selection. The control of interrupts and event outputs is managed by the interrupt and event register (DCU_INTEVTSEL). When an event signal needs to be output, users need to set the corresponding control bit in the interrupt and event register (DCU_INTEVTSEL) to active. DCU unit outputs a DCU event signal, DCU in the event list. When a corresponding event needs to generate an interrupt, users need to set the corresponding control bit in the interrupt and event register (DCU_INTEVTSEL) to active, and simultaneously set the DCU_CTL.INTEN bit in the control register to 1. DCU unit outputs a DCU interrupt signal, DCU in the interrupt list.

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27.4 Register Description

27.4.1 Register List

Base address: 0x40052000

Table 27-1 Data Computing Unit (DCU) Register Offset

Offset	Register	Description	Width
0x00	DCU_CTL	DCU Control Register	32
0x04	DCU_FLAG	DCU Flag Register	32
0x08+0x04*x	DCU_DATAx	DCU Data Register x (x=0-2)	32
0x14	DCU_FLAGCLR	DCU Flag Clear Register	32
0x18	DCU_INTEVTSEL	DCU Interrupt and Event Source Select Register	32

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27.4.2 DCU Control Register (DCU_CTL)

This register is used to configure the action mode of DCU.

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x80000000																															
Name	INTEN	Reserved																						COMPTRG	Reserved			DATASIZE		MODE		
Access	RW																							RW				RW		RW		

Bit	Name	Functional Description	Access
31	INTEN	Interrupt Enable ● 0b0: Disable ● 0b1: Enable	RW
30:9	*Reserved*	-	-
8	COMPTRG	Comparative Mode Trigger Timing ● 0b0: Compare after writing to DATA0 ● 0b1: Compare after writing to DATA0, DATA1, or DATA2	RW
7:5	*Reserved*	-	-
4:3	DATASIZE	Addition/Subtraction Mode, Comparative Mode Data Size ● 0b00: 8-bit ● 0b01: 16-bit ● 0b10: 32-bit ● 0b11: Setting prohibited	RW
2:0	MODE	Action Mode ● 0b000: DCU inactive ● 0b001: Addition mode, operation performed after data is written to the DATA1 register ● 0b010: Subtraction mode, operation performed after data is written to the DATA1 register ● 0b011: Hardware trigger addition mode, addition operation triggered by other peripheral circuits ● 0b100: Hardware trigger subtraction mode, subtraction operation triggered by other peripheral circuits ● 0b101: Comparative mode ● Others: Setting prohibited	RW

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27.4.3 DCU Flag Register

This register generates the DCU result identifier.

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																									FLAG_GT1	FLAG_EQ1	FLAG_LS1	FLAG_GT2	FLAG_EQ2	FLAG_LS2	FLAG_OP
Access																										RO	RO	RO	RO	RO	RO	RO

Bit	Name	Functional Description	Access
31:7	*Reserved*	-	-
6	FLAG_GT1	Greater Than Flag Bit 1 In comparison mode, the flag is set when DATA0 > DATA1, and the flag is cleared when the DCU_FLAGCLR.CLR_GT1 bit is written with 1.	RO
5	FLAG_EQ1	Equal Flag Bit 1 In comparative mode, when DATA0=DATA1, the bit is set. It is cleared when the DCU_FLAGCLR.CLR_EQ1 bit is written as 1.	RO
4	FLAG_LS1	Less Than Flag Bit 1 In comparative mode, when DATA0<DATA1, the bit is set. It is cleared when the DCU_FLAGCLR.CLR_LS1 bit is written as 1.	RO
3	FLAG_GT2	Greater Than Flag Bit 2 In comparison mode, the flag is set when DATA0 > DATA2, and the flag is cleared when the DCU_FLAGCLR.CLR_GT2 bit is written with 1.	RO
2	FLAG_EQ2	Equal Flag Bit 2 In comparative mode, when DATA0=DATA2, the bit is set. It is cleared when the DCU_FLAGCLR.CLR_EQ2 bit is written as 1.	RO
1	FLAG_LS2	Less Than Flag Bit 2 In comparative mode, when DATA0<DATA2, the bit is set. It is cleared when the DCU_FLAGCLR.CLR_LS2 bit is written as 1.	RO
0	FLAG_OP	Operation Flag Bit In addition/subtraction and trigger addition/trigger subtraction modes, when addition produces an overflow or subtraction produces an underflow, the bit is set. It is cleared when the DCU_FLAGCLR.CLR_OP bit is written as 1.	RO

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27.4.4 DCU Data Register (DCU_DATAx) (x=0-2)

The functions of each data register in different modes are as follows:

Mode Functions	DATA0	DATA1	DATA2
Addition mode	Summand/Result	Addend	Halving result
Trigger addition mode	Summand/Result	Addend	Halving result
Subtraction mode	Minuend/Result	Subtrahend	Halving result
Trigger subtraction mode	Minuend/Result	Subtrahend	Halving result
Compare mode	Compared object	Compare object 1	Compare object 2
Compare mode (window compare)	Compared object	Window upper limit	Window lower limit

Offset: 0x08+0x04*x

Addition/Subtraction Mode, Trigger Addition/Subtraction Mode, Comparative Mode

This register is used to store operation data.

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	DAT																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	DAT	Operation Data Store operation data, the actual number of bits used depends on DCU_CTL.DATASIZE setting: ● When DCU_CTL.DATASIZE=0b00, DATA[7:0] are valid data; ● When DCU_CTL.DATASIZE=0b01, DATA[15:0] are valid data; ● When DCU_CTL.DATASIZE=0b10, DATA[31:0] are valid data.	RW

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27.4.5 DCU Flag Clear Register (DCU_FLAGCLR)

This register is used to clear the DCU result identifier.

Offset	Bit Position																													
0x14	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																									CLR_GT1	CLR_EQ1	CLR_LS1	CLR_GT2	CLR_EQ2	CLR_LS2	CLR_OP
Access																										WO	WO	WO	WO	WO	WO	WO

Bit	Name	Description	Access
31:7	*Reserved*	-	-
6	CLR_GT1	Clear Greater Than Flag Bit 1 Write 1 to clear the DCU_FLAG.FLAG_GT1 bit, write 0 has no effect.	WO
5	CLR_EQ1	Clear Equals Flag Bit 1 Write 1 to clear the DCU_FLAG.FLAG_EQ1 bit, write 0 has no effect.	WO
4	CLR_LS1	Clear Less Than Flag Bit 1 Write 1 to clear the DCU_FLAG.FLAG_LS1 bit, write 0 has no effect.	WO
3	CLR_GT2	Clear Greater Than Flag Bit 2 Write 1 to clear the DCU_FLAG.FLAG_GT2 bit, write 0 has no effect.	WO
2	CLR_EQ2	Clear Equals Flag Bit 2 Write 1 to clear the DCU_FLAG.FLAG_EQ2 bit, write 0 has no effect.	WO
1	CLR_LS2	Clear Less Than Flag Bit 2 Write 1 to clear the DCU_FLAG.FLAG_LS2 bit, write 0 has no effect.	WO
0	CLR_OP	Clear Operation Flag Bit Write 1 to clear the DCU_FLAG.FLAG_OP bit, write 0 has no effect.	WO

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27.4.6 DCU Interrupt and Event Source Select Register (DCU_INTEVTSEL)

This register can select under what conditions DCU generates interrupts and outputs event signals.

Offset	Bit Position																													
0x18	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																							SEL_WIN		SEL_GT1	SEL_EQ1	SEL_LS1	SEL_GT2	SEL_EQ2	SEL_LS2	SEL_OP
Access																								RW		RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:9	*Reserved*	-	-
8:7	SEL_WIN	Window Compare Condition Selection In comparative mode, when the window comparison condition set by SEL_WIN is met, an interrupt is generated and an event output signal is output. When SEL_WIN is set active, no interrupt and no event output signal will be generated when other comparison conditions are met: ● 0b00: No window comparison interrupt is generated and no event output signal is output. Under this setting, other interrupt and event signal generation conditions are selected by Bit1-Bit6 of this register ● 0b01: When DATA0 data is within the window, an interrupt is generated and an event signal is output, i.e., DATA2≤DATA0≤DATA1 ● 0b10: When DATA0 data is outside the window, an interrupt is generated and an event signal is output, i.e., DATA0>DATA1 or DATA0<DATA2 ● 0b11: In comparative mode, no interrupt and no event signal is generated	RW
6	SEL_GT1	Greater Than Condition Selection 1 ● 0b0: In comparative mode with SEL_WIN=0b00, when DATA0>DATA1, no interrupt is generated and no event signal is output ● 0b1: In comparative mode with SEL_WIN=0b00, an interrupt and output event signal will be generated when DATA0 > DATA1. **Note** When SEL_WIN≠0b00, this bit setting has no effect.	RW

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Bit	Name	Functional Description	Access
5	SEL_EQ1	Equal Condition Selection 1 ● 0b0: In comparative mode with SEL_WIN=0b00, no interrupt and no event output is generated when DATA0=DATA1 ● 0b1: In comparative mode with SEL_WIN=0b00, an interrupt and output event signal will be generated when DATA0=DATA1. **Note** When SEL_WIN≠0b00, this bit setting has no effect.	RW
4	SEL_LS1	Less Than Condition Selection 1 ● 0b0: In comparative mode with SEL_WIN=0b00, no interrupt and no event output is generated when DATA0<DATA1 ● 0b1: In comparative mode with SEL_WIN=0b00, an interrupt and event output are generated when DATA0<DATA1 **Note** When SEL_WIN≠0b00, this bit setting has no effect.	RW
3	SEL_GT2	Greater Than Condition Selection 2 ● 0b0: In comparative mode with SEL_WIN=0b00, when DATA0>DATA2, no interrupt is generated and no event signal is output ● 0b1: In comparative mode with SEL_WIN=0b00, an interrupt and output event signal will be generated when DATA0 > DATA2. **Note** When SEL_WIN≠0b00, this bit setting has no effect.	RW
2	SEL_EQ2	Equal Condition Selection 2 ● 0b0: In comparative mode with SEL_WIN=0b00, no interrupt and no event output is generated when DATA0=DATA2 ● 0b1: In comparative mode with SEL_WIN=0b00, an interrupt and output event signal will be generated when DATA0=DATA2. **Note** When SEL_WIN≠0b00, this bit setting has no effect.	RW
1	SEL_LS2	Less Than Condition Selection 2 ● 0b0: In comparative mode with SEL_WIN=0b00, no interrupt and no event output is generated when DATA0<DATA2 ● 0b1: In comparative mode with SEL_WIN=0b00, an interrupt and event output are generated when DATA0<DATA2 **Note** When SEL_WIN≠0b00, this bit setting has no effect.	RW
0	SEL_OP	Operation Condition Selection ● 0b0: In addition/subtraction modes, no interrupt and no event output is generated on arithmetic overflow/underflow ● 0b1: In addition/subtraction modes, an interrupt and event output are generated on arithmetic overflow/underflow	RW

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28 Math Arithmetical Unit (MAU)

28.1 Introduction

The Math Arithmetical Unit (MAU) is a hardware-accelerated computing module that includes three types of operations: square root, sine, and arctangent. It supports square root, sine, and arctangent operations for fixed-point numbers. The sine function supports an operation precision of $360°/2^{12}$.

28.2 Functional Description

28.2.1 Square Root Operation

The square root operation supports 32-bit fixed-point input and outputs a 32-bit fixed-point result. The execution period varies depending on the input data value.

Operating Procedures

When the interrupt is disabled (MAU_CSR.INTEN=0), the square root operation follows the steps below. When the interrupt is enabled, users may customize the process by adding interrupt handling:

Step1. Write the radicand (number to be square-rooted) into MAU_DTR0 register;

Step2. Set the MAU_CSR.START bit to 1 to trigger the operation;

Step3. The MAU_CSR.BUSY bit will be set during computation. When the calculation is complete, this bit is automatically cleared; Wait until the BUSY bit is cleared, indicating the computation has completed;

Step4. Read the result from MAU_RTR0 register;

Step5. Repeat steps 1-4 as needed.

In step 3, after setting the MAU_CSR.START bit, the BUSY bit rises and remains high for 8 to 16 calculation clock periods, then automatically goes to 0, with the calculation time varying depending on the input data size. Users can monitor this bit to track computation status. When using the square root operation module, users can flexibly judge the current operation status according to the changes of this bit.

Result Handling

The result of the square root operation is a 32-bit value. The least significant bit is rounded to the nearest integer using the "round half up" method.

For example: Input=0x0000000C → Output=0x00000003; Input=0x0000000D → Output=0x00000004.

Fixed-Point Number Processing

When using fixed-point decimal input and needing consistent formatting between input and output, users can configure the MAU_CSR.SHIFT bit to adjust the output accordingly.

For example, when using the Q14.2 format for fixed-point arithmetic, you can set MAU_CSR.SHIFT=1 so that the output results also follow the Q14.2 format. The fixed-point number 6.25 (0x00000019 in Q14.2 format) has an output result of 5 (0x00000005) before shifting, and a result of 2.5 (0x0000000A in Q14.2 format) after shifting 1 bit.

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Note

When the exponent data written to MAU_DTR0 is greater than 0xFFFF0000, the maximum value of MAU_CSR.SHIFT can be set to 15; when the exponent data written to MAU_DTR0 is less than or equal to 0xFFFF0000, the maximum value of MAU_CSR.SHIFT can be set to 16.

28.2.2 Sine Operation

The sine operation supports 12-bit data input and the operation result is a 16-bit signed number output. The 12-bit data input represents the rectangular coordinate system angle to be calculated; in the 16-bit data output, the highest bit represents the positive or negative sign of the result, the data format is in Q15 format.

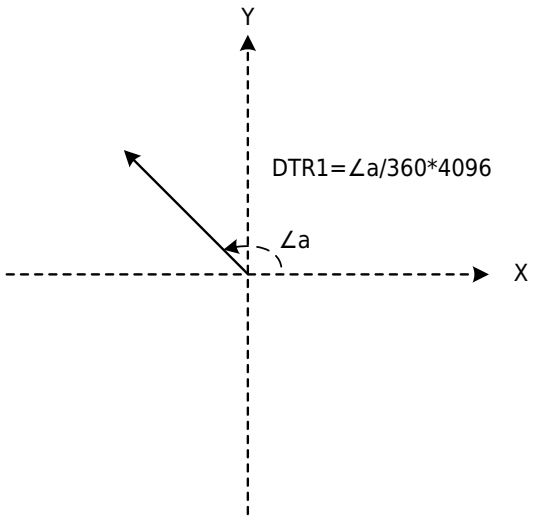

Figure 28-1 Schematic Diagram Of Sine Operation Angle Value

Operating Procedures

The operation flow of sine operation is as follows:

Step1. Write the angle value in MAU_DTR1 register; the input range of the angle value is 0° to 360° (excluding 360°). It needs to be converted to a value within the range of 0 to 4095 before being written into MAU_DTR1. The conversion formula is: (angle value / 90) * 1024;

Step2. After 1 period, read the operation result from MAU_RTR1 register;

Step3. Repeat the above steps 1-2.

28.2.3 Arctangent Operation

The arctangent operation is a lookup table calculation. The input is a 12-bit tangent value (signed number in Q10 format, input data range is [-1, +1]), and the output is a 16-bit radian value (signed number in Q15 format).

The input tangent value range is [-1, +1]. Software needs to process the tangent value (x) / output radian value:

- When the tangent value x is within [-1, +1], convert the tangent value x to a fixed-point number in Q10 format, write this value to the MAU_ATAN_DIN register, and read the MAU_ATAN_DOUT register to obtain the arctangent value (radians) of x.
- When the value of the tangent value x is greater than 1, the following formula must be used for conversion:

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$\arctan(x) + \arctan(\frac{1}{x}) = \frac{\pi}{2}$

When the value of the tangent value x is less than -1, the following formula must be used for conversion:

$\arctan(x) + \arctan(\frac{1}{x}) = -\frac{\pi}{2}$

Conversion process: Take the reciprocal of the tangent value to get 1/x, convert 1/x to a fixed-point number in Q10 format, write this value to the MAU_ATAN_DIN register, read the MAU_ATAN_DOUT register to obtain the arctangent of 1/x, and then use the above formula for mathematical calculation to obtain the arctangent value (radians) of x.

Operation Flow

The operation flow for the arctangent calculation is as follows:

Step1. Write the processed tangent value to the Arctangent Input Register (MAU_ATAN_DIN).

Step2. Read the operation result from the Arctangent Output Register (MAU_ATAN_DOUT).

Step3. Repeat steps 1 to 2.

28.2.4 Interrupt and Event Output

Interrupt Output

After each square root operation is completed, a corresponding operation completion event will be generated. If the interrupt control bit is enabled (MAU_CSR.INTEN=1), the corresponding interrupt request signal (MAU_SQRT) will also be generated.

Event Output

After each square root operation is completed, a corresponding operation completion event will be generated, and the corresponding event request signal (MAU_SQRT) will also be output, which can be used to select and trigger other modules.

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28.3 Register Description

28.3.1 Register List

Base address: 0x40054800

Table 28-1 Math Unit (MAU) Register Offset

Offset	Register	Description	Width
0x0000	MAU_CSR	Control Status Register	32
0x0004	MAU_DTR0	Data Input Register 0	32
0x000C	MAU_RTR0	Result Output Register 0	32
0x001C	MAU_DTR1	Data Input Register 1	32
0x0020	MAU_RTR1	Result Output Register 1	32
0x0024	MAU_ATAN_DIN	Arctan Data Input Register	32
0x0028	MAU_ATAN_DOUT	Arctan Data Output Register	32

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28.3.2 Control State Register (MAU_CSR)

Offset	Bit Position																													
0x0000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																			SHIFT					Reserved				BUSY	Reserved	INTEN	START
Access																				RW									RO		RW	RW

Bit	Name	Functional Description	Access
31:13	*Reserved*	-	-
12:8	SHIFT	Shift the Square Root Result ● 0b00000: The result is output without shifted ● 0b00001: The result is output with shifted left by 1 bit ● 0b00010: The result is output with shifted left by 2 bit ● ..... ● 0b10000: The result is output with shifted left by 16 bit ● Others: Setting prohibited	RW
7:4	*Reserved*	-	-
3	BUSY	Square Root Operation Status ● 0b0: The square root operation has not started or is completed ● 0b1: Square root operation in progress	RO
2	*Reserved*	-	-
1	INTEN	Square Root Interrupt Enable ● 0b0: No interrupt will be generated after the square root operation is completed ● 0b1: An interrupt is generated after the square root operation is completed	RW
0	START	Square Root Operation Starts Write 1 starts the square root operation (generating a START request internally), write 0 has no effect; read always returns 0.	RW

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28.3.3 Data Input Register 0 (MAU_DTR0)

Offset	Bit Position																													
0x0004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	SQRT_DIN																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	SQRT_DIN	Radicand Input of the number to be squared	RW

28.3.4 Result Output Register 0 (MAU_RTR0)

Offset	Bit Position																													
0x000C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	SQRT_DOUT																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	SQRT_DOUT	Square Root Result Square root result output	RW

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28.3.5 Data Input Register 1 (MAU_DTR1)

Offset	Bit Position																													
0x001C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																				SIN_DIN											
Access																					RW											

Bit	Name	Functional Description	Access
31:12	*Reserved*	-	-
11:0	SIN_DIN	Angle Setting Angle input in Cartesian coordinate system	RW

28.3.6 Result Output Register 1 (MAU_RTR1)

Offset	Bit Position																													
0x0020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								SIN_DOUT							
Access																									RW							

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	SIN_DOUT	Sine Operation Result Sine operation result output, signed number in Q15 format	RW

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28.3.7 Arctan Data Input Register (MAU_ATAN_DIN)

Offset	Bit Position																													
0x0024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																				ATAN_DIN											
Access																					RW											

Bit	Name	Functional Description	Access
31:12	*Reserved*	-	-
11:0	ATAN_DIN	Tangent Value Specifies the tangent value input, signed number in Q10 format	RW

28.3.8 Arctan Data Output Register (MAU_ATAN_DOUT)

Offset	Bit Position																													
0x0028	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								ATAN_DOUT							
Access																									RW							

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	ATAN_DOUT	Arctangent Operation Result Specifies the arctangent operation result output, a signed number in Q15 format, representing the radian value.	RW

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29 Debug Controller (DBGC)

29.1 Introduction

This MCU's core is Cortex-M4, which includes hardware for advanced debugging functions. Using these debugging functions, the core can be stopped when fetching instructions (instruction breakpoint) or accessing data (data breakpoint). When the core is stopped, the internal state of the core and the external state of the system can be queried. After the query completes, the kernel and system are restored and program execution is restored.

Debugging interface supported:

- Serial debug trace interface SWD
- Single-wire serial debug interface TOOL0

29.2 Functional Description

29.2.1 Function Block Diagram

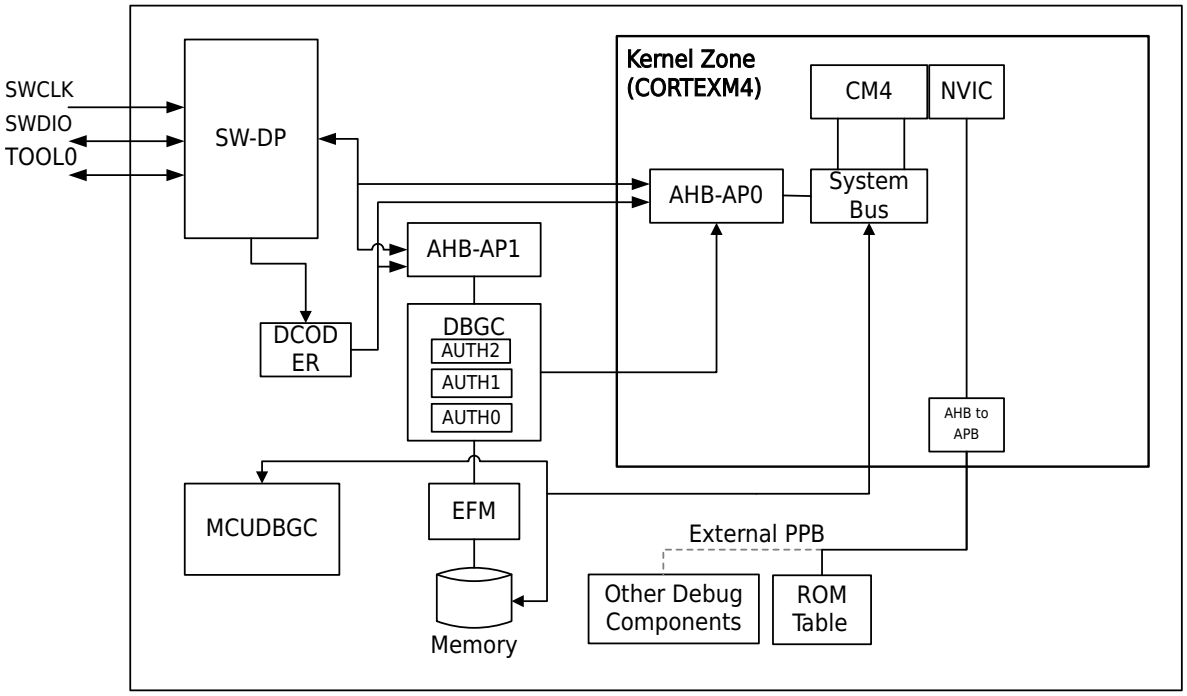

Figure 29-1 Debug Control System Block Diagram

The ARM Cortex-M4 core provides integrated on-chip debugging support. It includes:

- SW-DP: SWD debug port
- AHB-AP: AHB access port
- FPB: Flash instruction breakpoint
- Flexible debugging pin assignment

Note

For more information on the debugging functions supported by the ARM Cortex-M4 core, see the "Cortex-M4F-r0p1 Technical Reference Manual" and "CoreSight Design Kit r0p1 Technical Reference Manual".

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29.2.2 Reference Documentation

This product references the following ARM technical documentation:

- Cortex M4 Technical Reference Manual r0p1
- Arm Debug Interface Architecture Specification version 5
- CoreSight Components Technical Reference Manual version 1.0

29.2.3 SWDand TOOL0 Debug Ports

The MCU core integrates a Serial Wire Debug Port (SW-DP) and a single-wire debug interface TOOL0. The SW-DP is an ARM standard CoreSight debug port with a SW-DP (2-pin) interface. TOOL0 is a single-wire debug interface with only a (1-pin) TOOL0 interface. The default interface is the two-wire SWD (clock + data).

To switch from two-wire SWD to single-wire TOOL0 debugging, connect the single-wire debugger to the TOOL0 port and the chip reset pin (NRST). Then, using the configuration sequence issued by the single-wire debugger, single-wire TOOL0 debugging can be performed.

To switch from single-wire TOOL0 debugging back to two-wire SWD, reset the chip by power cycling, and it will revert to the default two-wire SWD debug mode.

29.2.4 Pin Arrangement and Debug Port Pins

Depending on the MCU package, there are different active pin counts. Therefore, some pin-related functions may vary from package to package.

Debug Port Pins

The MCU's 2 general-purpose I/O pins can be used as SW-DP interface pins, and 1 pin (MD) can be used as a TOOL0 interface pin. All packages provide these pins.

Table 29-1 Debug Port Pins

Pin Name	Debug Port		MCU Pin Assignment
	Type	Debug Assignment	
SWCLK	I	SWD Serial Clock	PB1
SWDIO	I/O	SWD Serial Wire Data Input/Output	PB2
TOOL0	I/O	TOOL0 Single-Wire Data Input/Output	MD

Flexible Pin Assignment

After reset (power-on or pin reset), all 2 pins used for SW-DP are assigned as dedicated pins, available for immediate use by the debug tool (note that trace outputs are not assigned unless explicitly programmed by the debug tool). However, the MCU can disable part or all of the SW-DP port, thereby releasing the associated pins for use as GPIO.

After reset (power-on or pin reset), TOOL0 defaults to debug pins, available for immediate use by the debug tool. However, when no debugger is connected, the MCU can disable the pin debug function, thereby releasing the associated pins.

For the configuration to disable the debug port pin function, refer to the "Special Control Register (PSPCR)" in the "General-Purpose I/O (GPIO) " chapter.

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Table 29-2 Flexible Pin Assignment

Available Debug Ports	Assigned Pins		
	SWCLK	SWDIO	TOOL0
Two-wire SW-DP Debug	√	√	Released
Single-wire TOOL0 Debug	Released	Released	√
Disable SW-DP and Disable TOOL0	Can be released	Can be released	Can be released

Internal Pull-ups on Pins

To avoid floating IO levels, the MCU has built-in internal pull-up resistors on the debug pins:

- TOOL0: Internal pull-up
- SWDIO: Internal pull-up
- SWCLK: Internal pull-up

In the absence of a connected debugger, user software can release debug IO for use as general-purpose I/O ports by setting the GPIO special control register. Since the internal pull-up is a weak pull-up of <100kΩ, it is recommended to use an external pull-up of 10kΩ.

29.2.5 SW Debug Port-SW Protocol Overview

The synchronous serial protocol uses two pins:

- SWCLK: Clock from master to slave
- SWDIO: Bidirectional

LSB is ahead when transferring data.

For SWCLK and SWDIO, it is recommended to use a 10kΩ pull-up on the circuit board.

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29.3 Register Description

29.3.1 Register List

Base address: 0xE0042000

Table 29-3 Debug Controller (DBGC) Register Offset

Offset	Register	Description	Width	Access Host
0x001C	DBGC_MCUDBGCSTAT	DBG Status Register	32	CPU(1)
0x0020	DBGC_MCUSTPCTL	Peripheral Debug Stop Control Register	32	CPU(1)
0x0030	DBGC_FCRCCR0	FCRC Control Register 0	32	Debug IDE
0x0034	DBGC_FCRCCR1	FCRC Control Register 1	32	Debug IDE
0x0038	DBGC_FCRCDOR	FCRC Date Output Register	32	Debug IDE
0x003C	DBGC_FCRCREF	FCRC Reference Register	32	Debug IDE
0x0018	DBGC_FMCCTL	FLASH Control Register	32	Debug IDE

Note

1. Register bits are located in the PPB region and can only be accessed by the CPU in privileged mode.

29.3.2 DBG Status Register (DBGC_MCUDBGCSTAT)

DBG debugs power-on status check register.

Offset	Bit Position																													
0x001C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																														CDBGPWRUPACK	CDBGPWRUPREQ
Access																															RW	RW

Bit	Name	Functional Description	Access
31:2	*Reserved*	-	-
1	CDBGPWRUPACK	Debugger Power-on Feedback ● 0b0: No feedback ● 0b1: Debug power-on feedback	RW
0	CDBGPWRUPREQ	Debugger Power-on Request ● 0b0: No power-on request ● 0b1: Power-on request	RW

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29.3.3 Peripheral Debug Stop Control Register (DBGC_MCUSTPCTL)

The peripheral module pauses control when the CPU is in the debug state.

Offset	Bit Position																													
0x0020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000003B																															
Name	Reserved																HALLSTP	TMRA5STP	TMRA4STP	TMRA3STP	TMRA2STP	TMRA1STP	Reserved	TMR4STP	TMR02STP	TMR01STP	PVD2STP	PVD1STP	PVD0STP	Reserved	WDTSTP	SWDTSTP
Access																	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW		RW	RW

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15	HALLSTP	HALL Count Pause Signal ● 0b0: Counter continues counting even when the core is stopped ● 0b1: Counter pauses counting when the core is stopped	RW
14	TMRA5STP	TimerA_5 Count Pause Signal ● 0b0: Counter continues counting even when the core is stopped ● 0b1: Counter pauses counting when the core is stopped	RW
13	TMRA4STP	TimerA_4 Count Pause Signal ● 0b0: Counter continues counting even when the core is stopped ● 0b1: Counter pauses counting when the core is stopped	RW
12	TMRA3STP	TimerA_3 Count Pause Signal ● 0b0: Counter continues counting even when the core is stopped ● 0b1: Counter pauses counting when the core is stopped	RW
11	TMRA2STP	TimerA_2 Count Pause Signal ● 0b0: Counter continues counting even when the core is stopped ● 0b1: Counter pauses counting when the core is stopped	RW
10	TMRA1STP	TimerA_1 Count Pause Signal ● 0b0: Counter continues counting even when the core is stopped ● 0b1: Counter pauses counting when the core is stopped	RW
9	*Reserved*	-	-
8	TMR4STP	Timer4 Count Pause Signal ● 0b0: Counter continues counting even when the core is stopped ● 0b1: Counter pauses counting when the core is stopped	RW
7	TMR02STP	Timer0_2 Count Pause Signal ● 0b0: Counter continues counting even when the core is stopped ● 0b1: Counter pauses counting when the core is stopped	RW
6	TMR01STP	Timer0_1 Count Pause Signal ● 0b0: Counter continues counting even when the core is stopped ● 0b1: Counter pauses counting when the core is stopped	RW

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Bit	Name	Functional Description	Access
5	PVD2STP	PVD2 Pause Signal ● 0b0: PVD2 interrupt application or reset occurs even when the core is stopped ● 0b1: PVD2 interrupt application or reset is masked when the core is stopped	RW
4	PVD1STP	PVD1 Pause Signal ● 0b0: PVD1 interrupt application or reset occurs even when the core is stopped ● 0b1: PVD1 interrupt application or reset is masked when the core is stopped	RW
3	PVD0STP	PVD0 Pause Signal ● 0b0: BOR interrupt application or reset occurs even when the core is stopped ● 0b1: BOR interrupt application or reset is masked when the core is stopped **Note** PVD0 is used as BOR reset.	RW
2	*Reserved*	-	-
1	WDTSTP	WDT Count Pause Signal ● 0b0: Counter continues counting even when the core is stopped ● 0b1: Counter pauses counting when the core is stopped	RW
0	SWDTSTP	SWDT Count Pause Signal ● 0b0: Counter continues counting even when the core is stopped ● 0b1: Counter pauses counting when the core is stopped	RW

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29.3.4 FCRC Control Register 0 (DBGC_FCRCCR0)

Select the Flash CRC operation.

Offset	Bit Position																													
0x0030	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								FCRCDORCLR	Reserved				FCRCERR	FCRCACK	FCRCREQ
Access																									RW					RW	RW	RW

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7	FCRCDORCLR	CRC Result Clearing ● 0b0: Do not clear the CRC calculation result ● 0b1: Clear the CRC calculation result	RW
6:3	*Reserved*	-	-
2	FCRCERR	CRC Request Error Write 0 clears the flag; write 1 has no effect. Read: ● 0b0: No error flag ● 0b1: CRC request error **Notice** Initiating a CRC calculation request while the CPU is running will return a CRC request error.	RW
1	FCRCACK	CRC Calculation End Flag Write 0 clears the flag; write 1 has no effect. Read: ● 0b0: No end flag ● 0b1: CRC calculation ended	RW
0	FCRCREQ	CRC Calculation Request ● 0b0: No request ● 0b1: CRC calculation request **Notice** This bit is automatically cleared by hardware after the CRC calculation is completed or an error occurs.	RW

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29.3.5 FCRC Control Register 1 (DBGC_FCRCCR1)

Select the Flash CRC check sector. If sectors 0 and 1 are selected for the check, then FCRCCR1=0x00010000.

Offset	Bit Position																													
0x0034	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	FCRCER																FCRCSR														
Access	RW																RW														

Bit	Name	Functional Description	Access
31:16	FCRCER	CRC Calculation Start Sector ● 0x0: sector 0 ● 0x1: Sector1 ● 0x2: Sector2 ● ... ● 0xFF: Sector255 ● Others: Setting prohibited **Note** Ensure that FCRCER ≥ FCRCSR; otherwise, an FCRC request error occurs.	RW
15:0	FCRCSR	CRC Calculation Start Sector ● 0x0: Sector0 ● 0x1: Sector1 ● 0x2: Sector2 ● ... ● 0xFF: Sector255 ● Others: Setting prohibited	RW

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29.3.6 FCRC Result Register (DBGC_FCRCDOR)

Reads back the FCRC calculation result. This register is cleared to zero after each system reset.

Offset	Bit Position																													
0x0038	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	DOR																															
Access	RO																															

Bit	Name	Functional Description	Access
31:0	DOR	FCRC calculation result	RO

29.3.7 FCRC Reference Value Register (DBGC_FCRCREF)

Read back the FCRC reference value stored in the FLASH address ICG4 (i.e., 0x00020010-0x00020013).

Offset	Bit Position																													
0x003C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	REF																															
Access	RO																															

Bit	Name	Functional Description	Access
31:0	REF	FCRC Reference Value	RO

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29.3.8 FLASH Control Register (DBGC_FMCCTL)

Offset	Bit Position																													
0x0018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved													PCROPERSERR	PCROPERSACK	PCROPERSREQ	Reserved															
Access														RW	RW	RW																

Bit	Name	Functional Description	Access
31:19	*Reserved*	-	-
18	PCROPER-SERR	PCROP Release Error Flag Write 0 to clear the flag, write 1 has no effect. Read: ● 0b0: No release error flag generated ● 0b1: Release error flag generated	RW
17	PCROPER-SACK	PCROP Release Completion Flag Write 0 to clear the flag, write 1 has no effect ● 0b0: No release completion flag generated ● 0b1: Release completion flag generated	RW
16	PCROPERS-REQ	PCROP Release Request ● 0b0: No release request initiated ● 0b1: Release request initiated	RW
15:0	*Reserved*	-	-

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A Glossary

Terminology	Full Name	description
Byte	-	Bytes, 8-bit data
Half Word	-	Half word, 16-bit data
Word	-	Words, 32-bit data
Double Word	-	Double word, 64 -bit data.
IAP	-	It refers to reprogram the MCU's Flash during the running of a user program (programming in the application).
ICP	-	It means that the MCU's Flash of the MCU can be programmed by using JTAG protocol, SWD protocol or bootstrap program when the device is installed on the user application circuit board (in-circuit/online programming).
AHB	Advanced High-performance Bus	Advanced High-Performance Bus
APB	Advanced Peripheral Bus	Advanced peripheral bus
DMA	Direct Memory Access	Direct memory access
TIM/TMR	-	Timer

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Revision History

Revision/Date	Changes
Rev1.00 Jul. 24, 2026	First official release.

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