XIAOHUA SEMICONDUCTOR

HC32L16x Series

32-bit ARM® Cortex®-M0+ Microcontroller

Reference Manual

Rev1.30

August 2026

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Preface

Bit/Bit Field

A register contains a bit (one bit wide) or a bit field (multiple bit width), and the bit field is usually described as [y:x], starting from the x bit and ending at the y bit. Unless otherwise specified, decimal numbers are used in the bit field.

It is not recommended to use unspecified fields; otherwise, unpredictable consequences may be caused.

Register Address

The address of each register can be obtained by the base address of the system address division and the offset address of the register (see the "Register List" of each module for details).

Access Type

The following abbreviations are used for register description:

Access Type	Description
RW	Readable and writable.
RO	Read only. Writes are ignored.
WO	Write only. Read value undefined.
RWA	Readable and writable. Writable only when unlocked or in safe mode.
RWC	Readable and writable. Writing any value clears this bit.
RC	Read only. Writes are ignored. This bit is cleared automatically after reading.
RS	Read only. Writes are ignored. This bit is set automatically after reading.

Number Format

- 0x prefix is used for hexadecimal numbers
- 0b prefix is used for binary numbers
- Numbers without prefix are in decimal representation

Reserved (Res.)

Registers and bit fields marked with *Reserved* are reserved for future use. These should be written to their reset value unless otherwise stated in the Register Description. The read value of Reserved bit may be different in different devices or features.

Reset Value (Reset)

The reset value indicates the value after the register is reset. Registers need to be initialized and reset before use; otherwise, unpredictable consequences may be caused.

Peripheral Availability Description

For HC32L16x Series 32-bit ARM® Cortex®-M0+ Microcontroller supported peripherals and their numbers, refer to the corresponding "Datasheet".

Security Statement

There may be potential security problems due to the use of a certain function or protocol, which need to be declared to remind users and avoid security risks.

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1 Product Introduction

HC32L16x Series is an ultra-low power consumption MCU with a wide operating voltage range designed to extend the battery life of portable measurement systems. Integrates a 12-bit 1Msps high-precision SARADC, one 12-bit DAC, comparator, operational amplifier (OPA), built-in high-performance PWM timer, LCD display, multiple UART interfaces, SPI, I2C, and other communication peripherals. Includes AES and TRNG information security modules, offering high integration, high noise immunity, high reliability, and ultra-low power consumption. This product adopts the Cortex-M0+ core and is combined with the mature Keil & IAR debugging and development software, supporting C language, assembly language and assembly instructions.

Typical Applications of Ultra-low Power MCU

Main application scenarios include:

- Sensor applications, IoT applications
- Smart meters, wireless modules, thermostats, electronic shelf labels
- Intelligent transportation, alarm systems
- Smart home, medical devices

About This Manual

This manual describes the chip's functionalities, operational guidelines, and usage methods. For detailed chip specifications, refer to the corresponding "Datasheet".

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2 Storage and Architectures

2.1 Overview

System consists of the following parts:

- 2 AHB bus Master:
  - Cortex-M0+
  - DMA controller
- Multiple AHB bus Slaves:
  - Flash Memory
  - SRAM Memory
  - AHB to APB Bridge 0 includes all APB0 interface peripherals
  - AHB to APB Bridge 1 includes all APB1 interface peripherals
  - AHB peripherals

The entire system bus structure is realized by multi-level AHB-lite bus interconnection.

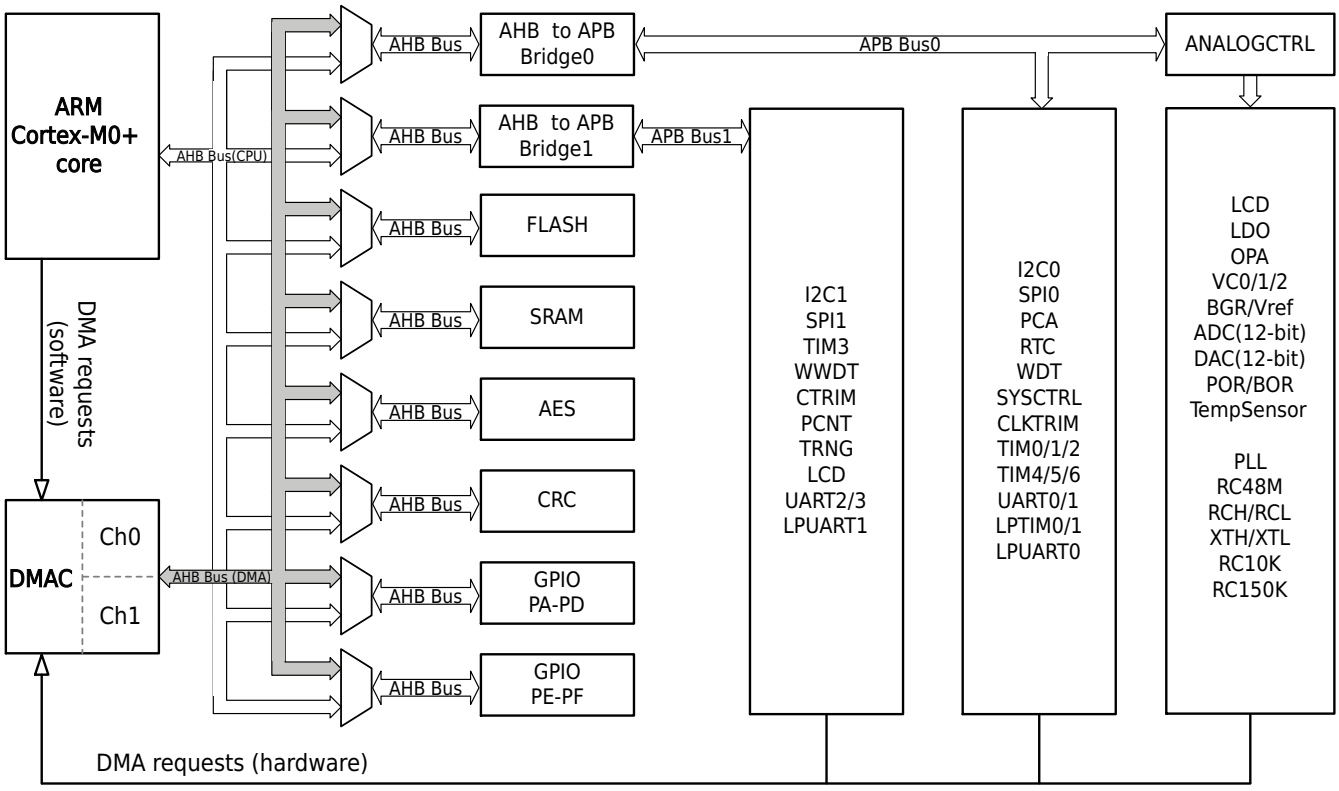

Figure 2-1 System Architecture Schematic Diagram

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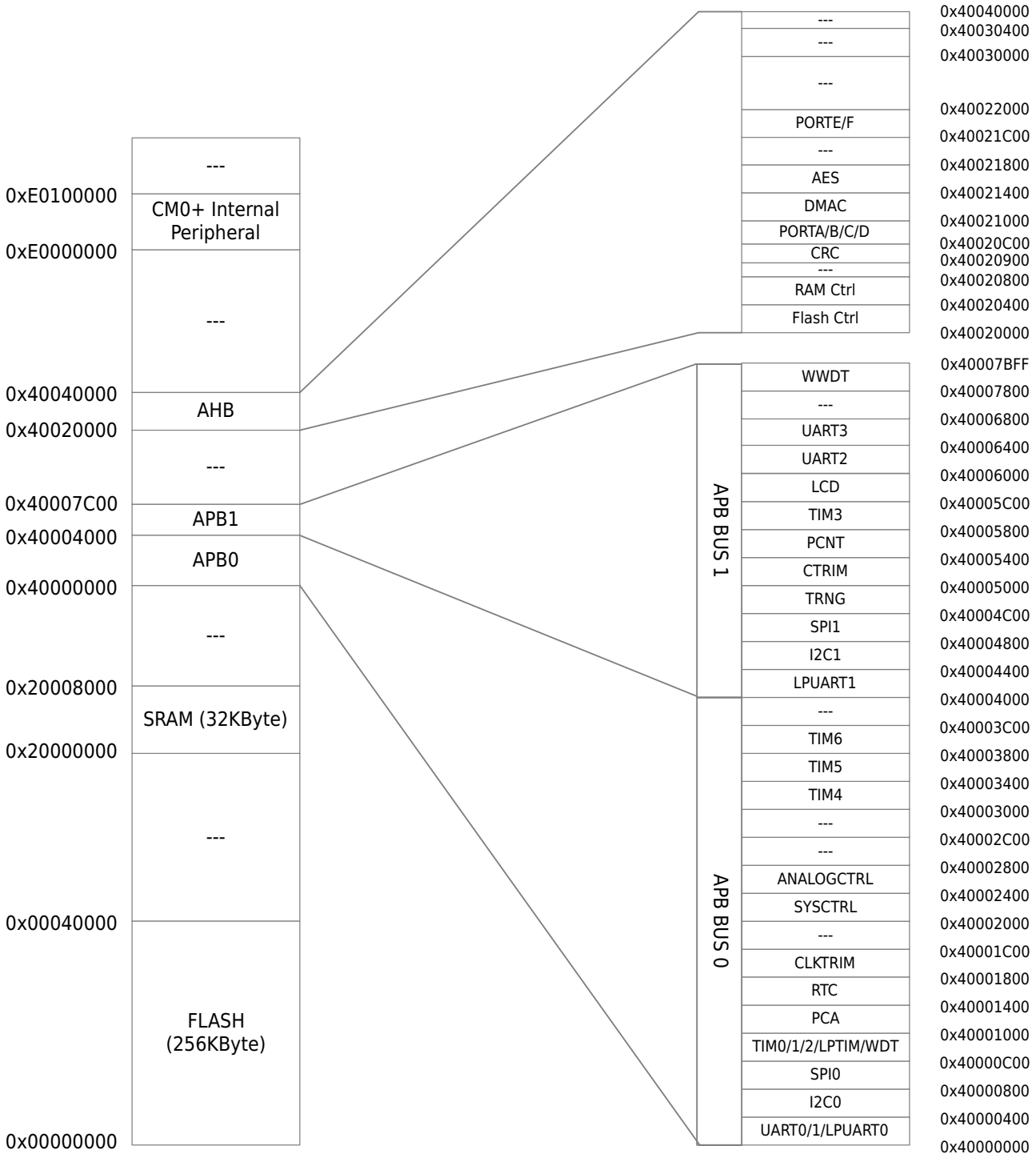
2.2 System Address Division

System of address region division:



Note

PORTA/B/C/D and PORTE/F modules use two separate address spaces.

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2.3 Memory and Module Address Assignment

Memory/Module	Address	Size	Description
FLASH	0x00000000-0x0001FFFF	128KByte	-
	0x00000000-0x0003FFFF	256KByte	-
Reserved	0x00010000-0x1FFFFFFF	-	-
SRAM	0x20000000-0x20003FFF	16KByte	-
	0x20000000-0x20007FFF	32KByte	-
Reserved	0x20002000-0x3FFFFFFF	-	-
UART0	0x40000000-0x400000FF	256Byte	-
UART1	0x40000100-0x400001FF	256Byte	-
LPUART0	0x40000200-0x400002FF	256Byte	-
Reserved	0x40000300-0x400003FF	-	-
I2C0	0x40000400-0x400007FF	1KByte	-
SPI0	0x40000800-0x40000BFF	1KByte	-
TIM0	0x40000C00-0x40000CFF	256Byte	-
TIM1	0x40000D00-0x40000DFF	256Byte	-
TIM2	0x40000E00-0x40000EFF	256Byte	-
LPTIM0/1	0x40000F00-0x40000F7F	128Byte	-
WDT	0x40000F80-0x40000FFF	128Byte	-
PCA	0x40001000-0x400013FF	1KByte	-
RTC	0x40001400-0x400017FF	1KByte	-
CLKTRIM	0x40001800-0x40001BFF	1KByte	-
Reserved	0x40001C00-0x40001FFF	-	-
SYSCTRL	0x40002000-0x400023FF	1KByte	-
ANALOGCTRL	0x40002400-0x400027FF	1KByte	ADC/DAC/VC/LVD/OPA
Reserved	0x40002800-0x40002BFF	1KByte	-
Reserved	0x40002C00-0x40002FFF	1KByte	-
TIM4	0x40003000-0x400033FF	1KByte	-
TIM5	0x40003400-0x400037FF	1KByte	-
TIM6	0x40003800-0x40003BFF	1KByte	-
Reserved	0x40003C00-0x40003FFF	-	-
LPUART1	0x40004000-0x400043FF	1KByte	-
I2C1	0x40004400-0x400047FF	1KByte	-
SPI1	0x40004800-0x40004BFF	1KByte	-
TRNG	0x40004C00-0x40004FFF	1KByte	-

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Memory/Module	Address	Size	Description
CTRIM	0x40005000-0x400053FF	1KByte	-
PCNT	0x40005400-0x400057FF	1KByte	-
TIM3	0x40005800-0x40005BFF	1KByte	-
LCD	0x40005C00-0x40005FFF	1KByte	-
UART2	0x40006000-0x400063FF	1KByte	-
UART3	0x40006400-0x400067FF	1KByte	-
Reserved	0x40006800-0x400077FF	-	-
WWDT	0x40007800-0x40007BFF	1KByte	-
Reserved	0x40007C00-0x4001FFFF	-	-
FLASH-CTRL	0x40020000-0x400203FF	1KByte	-
RAM-CTRL	0x40020400-0x400207FF	1KByte	-
Reserved	0x40020800-0x400208FF	256Byte	-
CRC	0x40020900-0x40020BFF	768Byte	-
PORTA/B/C/D	0x40020C00-0x40020FFF	1KByte	-
DMAC	0x40021000-0x400213FF	1KByte	-
AES	0x40021400-0x400217FF	1KByte	-
Reserved	0x40021800-0x40021BFF	1KByte	-
PORTE/F	0x40021C00-0x40021FFF	1KByte	-

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3 Operating Mode

3.1 Overview

This product can realize 3 working modes under the control of the power management module. The operable modules and their power consumption differ across working modes.

This product has the following working modes:

1. Active Mode: CPU running, peripheral functional modules running.
2. Sleep mode: CPU halted, peripheral functional modules running.
3. DeepSleep mode: CPU halted, high-speed clock modules disabled.

3.2 Working Mode Switching

The product can be freely switched among 3 working modes when it is working. In Active mode, executing specific instructions can transition the device into Sleep mode or DeepSleep mode. Wake-up from Sleep or DeepSleep mode via an interrupt and return to Active mode.

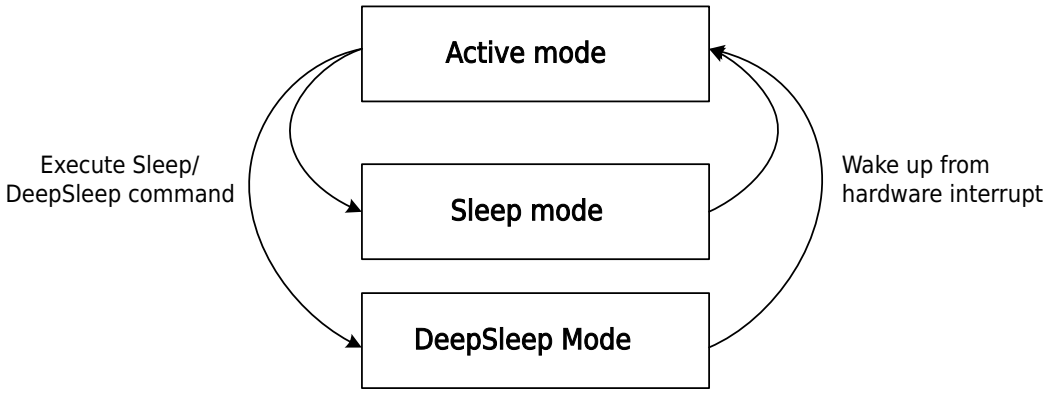

Figure 3-1 Working Mode State Transition Diagram

In various working modes, the interrupts that the CPU can respond type are as follows:

NVIC Interrupt Input	External Interrupt Source	Active Mode	Sleep mode	DeepSleep mode
Interrupt #0	PORTA	✓	✓	✓
Interrupt #1	PORTB	✓	✓	✓
Interrupt #2	PORTC/E	✓	✓	✓
Interrupt #3	PORTD/F	✓	✓	✓
Interrupt #4	DMAC	✓	✓	×
Interrupt #5	TIM3	✓	✓	×
Interrupt #6	UART0/2	✓	✓	×
Interrupt #7	UART1/3	✓	✓	×
Interrupt #8	LPUART0	✓	✓	✓
Interrupt #9	LPUART1	✓	✓	✓

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NVIC Interrupt Input	External Interrupt Source	Active Mode	Sleep mode	DeepSleep mode
Interrupt #10	SPI0	✓	✓	×
Interrupt #11	SPI1	✓	✓	×
Interrupt #12	I2C0	✓	✓	×
Interrupt #13	I2C1	✓	✓	×
Interrupt #14	TIM0	✓	✓	×
Interrupt #15	TIM1	✓	✓	×
Interrupt #16	TIM2	✓	✓	×
Interrupt #17	LPTIM0/1	✓	✓	✓
Interrupt #18	TIM4	✓	✓	×
Interrupt #19	TIM5	✓	✓	×
Interrupt #20	TIM6	✓	✓	×
Interrupt #21	PCA/WWDT	✓	✓	×
Interrupt #22	WDT	✓	✓	✓
Interrupt #23	RTC	✓	✓	✓
Interrupt #24	ADC/DAC	✓	✓	×
Interrupt #25	PCNT	✓	✓	✓
Interrupt #26	VC0	✓	✓	✓
Interrupt #27	VC1/2	✓	✓	✓
Interrupt #28	LVD	✓	✓	✓
Interrupt #29	LCD	✓	✓	✓
Interrupt #30	FLASH/RAM	✓	✓	×
Interrupt #31	CLKTRIM/CTRIM	✓	✓	✓

In different working mode, the reset types system can respond following to:

Table 3-2 Reset Type Response Capabilities in Different Operational Mode

Number	Reset Source	Active Mode	Sleep Mode	DeepSleep Mode
[0]	Power-on/Brown-out Reset (POR)	✓	✓	✓
[1]	External Reset Pin Reset	✓	✓	✓
[2]	LVD Reset	✓	✓	✓
[3]	WDT Reset	✓	✓	✓

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Number	Reset Source	Active Mode	Sleep Mode	DeepSleep Mode
[4]	WWDT Reset	✓	✓	×
[5]	PCA Reset	✓	✓	×
[6]	Cortex-M0+ LOCKUP Hardware Reset	✓	×	×
[7]	Cortex-M0+ SYSRESETREQ Software Reset	✓	×	×

3.3 Active Mode

The MCU is in the Active mode after system is reset at power-on, or after waking up from various low power consumptions. Various low-power modes are available to conserve power when the CPU is not required to continue running, such as while waiting for an external event. Users need to select an optimal low-power mode based on the lowest power consumption, fastest startup time, and available wake-up sources.

In Active mode, several ways to reduce chip power consumption in run mode:

1. In Active mode, the speed of any system clock (HCLK, PCLK) can be reduced by programming the prescaler registers (SYSCTRL0.HCLK_PRS, SYSCTRL0.PCLK_PRS). The prescaler can also be used to slow down the clocks to peripherals before entering Sleep mode.
2. In Active mode, disable the clocks of unused peripherals (PERI_CLKENx) to reduce power consumption.
3. Turn off the clocks of unused peripheral clock (PERI_CLKENx) before executing WFI instructions.
4. In certain scenarios, low-power mode can be used instead of Active mode, as this product features extremely short wake-up time that can still meet system real-time response requirements.

3.4 Sleep Mode

Executing the WFI instruction enters Sleep mode. In Sleep mode, the CPU halted, but the clock module, system clock, NVIC interrupt processing and peripheral functional modules can still work.

When the system enters the sleep state, the port state will not be changed. Before entering the sleep state, the IO state can be changed as needed.

Enter Sleep Mode

Enter sleep state by executing WFI instruction. There are two options available for selecting the Sleep mode entry mechanism based on value of the SLEEPONEXIT bit in the system control register of Cortex-M0+:

- SLEEP-NOW: If the SLEEPONEXIT bit is cleared, the MCU enters Sleep mode immediately when WFE is executed.
- SLEEP-ON-EXIT: If the SLEEPONEXIT bit is set, the MCU enters Sleep mode immediately when the system exits from the lowest priority interrupt handler.

Exit Sleep Mode

If the WFI instruction is executed to enter the Sleep mode, any peripheral interrupt responded by the as the high-priority nested vector interrupt controller can wake up the system from the Sleep mode.

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Precautions

- The position of SLEEPONEXIT is 1, and the interrupt will automatically enter Sleep after execution, and the program does not need to write __wfi();
- SLEEPONEXIT bit is cleared to 0, main() executes __wfi() and enters Sleep, interrupt triggers and executes the interrupt program and returns to main(), then executes WFI instruction and enters Sleep. Wait for a subsequent interrupt to fire.
- The SLEEPONEXIT bit does not affect the execution of the __wfi() instruction. SLEEPONEXIT = 0: main() executes __wfi() and enters Sleep, interrupt triggers and executes the interrupt program and returns to main(), and then continues to execute;
- If Sleep is entered in an interrupt, only interrupts with a priority higher than this interrupt can wake up, and the high priority is executed first, and then the low priority is executed; interrupts with a priority lower than or equal to this interrupt cannot wake up.
- For details on entering and waking up from Sleep mode via WFE (Wait For Event) instruction, refer to the Cortex-M0+ relevant technical manual.

3.5 DeepSleep Mode

Using SLEEPDEEP with the WFI instruction enables entry into DeepSleep mode. In DeepSleep mode, the CPU halted, the high-speed clock is disabled, the low-speed clock can be configured to remain active or not, certain low-power peripheral modules may be selectively enabled, while the NVIC interrupt handling remains functional.

- When the system (Using high-speed clock) enters DeepSleep mode, the high-speed clock is automatically disabled, and the low-speed clock remains in the state before entering DeepSleep.
- The system (Using low-speed clock) enters the DeepSleep mode, the low-speed clock is not automatically disabled and maintains its operation. Only ARM Cortex-M0+ is not running, other modules are running.
- When the system clock is switched, all clocks will not be automatically disabled, and the corresponding clocks need to be disabled or enabled by software according to power consumption and system requirements.
- When the system enters the DeepSleep mode, it will not change the port state. Before entering the DeepSleep mode, change the IO state as needed.

Enter DeepSleep Mode

First set the SLEEPDEEP bit of Cortex-M0+ in the system control register, and enter the DeepSleep mode by executing the WFI instruction. Depending on the value of the SLEEPONEXIT bit in the system control register, there are two options for selecting the DeepSleep mode entry mechanism:

- SLEEP-NOW: If the SLEEPONEXIT bit is cleared, the MCU enters DeepSleep mode immediately when WFI is executed.
- SLEEP-ON-EXIT: If the SLEEPONEXIT bit is set, the MCU enters DeepSleep mode immediately when the system exits from the lowest priority interrupt handler.

Exit DeepSleep Mode

If the WFI instruction is executed to enter DeepSleep mode, any peripheral interrupt that is responded to by the high priority nested vector interrupt controller (operable under DeepSleep peripheral module interrupt) can wake up the system from DeepSleep mode.

For wake-up configuration, refer to the "Interrupt Wakeup Control" section in the "System Controller (SYSCRTL)" chapter.

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Precautions

- The position of SLEEPONEXIT is 1, and the interrupt will automatically enter DeepSleep after execution, and the program does not need to write __wfi();
- SLEEPONEXIT bit is cleared to 0, main() executes __wfi() and enters DeepSleep, interrupt triggers and executes the interrupt program and returns to main(), then executes WFI instruction and enters DeepSleep. Wait for a subsequent interrupt to fire.
- The SLEEPONEXIT bit does not affect the execution of the __wfi() instruction. SLEEPONEXIT = 0: main() executes __wfi() and enters DeepSleep, interrupt triggers and executes the interrupt program and returns to main(), and then continues to execute.
- If DeepSleep is entered in an interrupt, only interrupts with a priority higher than this interrupt can wake up, and the high priority is executed first, and then the low priority is executed; interrupts with a priority lower than or equal to this interrupt cannot wake up.
- For details on entering and waking up from DeepSleep mode via WFE (Wait For Event) instruction, refer to the Cortex-M0+ relevant technical manual.

3.6 Functional/Module Working Status

The comparison of the working status of the functional/modules in the three working modes is shown in the table below:

Table 3-3 Peripheral Working Status Table in Each Mode

Functional/Module	Active Mode	Sleep Mode	DeepSleep Mode
Cortex-M0+	✓	×	×
XTH	✓	✓	×
XTL	✓	✓	✓
RCH	✓	✓	×
RC48M	✓	✓	×
RCL	✓	✓	✓
PLL	✓	✓	×
RESET	✓	✓	✓
GPIO	✓	✓	✓
I2C0/1	✓	✓	×
SPI0/1	✓	✓	×
CLKTRIM	✓	✓	✓(1)
CTRIM	✓	✓	✓(1)
FLASH	✓	✓	×
RAM	✓	✓	×
DMAC	✓	✓	×
TIM0/1/2/3	✓	✓	×
LPTIM0/1	✓	✓	✓(1)
PCA	✓	✓	×
TIM4/5/6	✓	✓	×
RTC	✓	✓	✓
WDT	✓	✓	✓
WWDT	✓	✓	×
PCNT	✓	✓	✓
UART0/1/2/3	✓	✓	×

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Functional/Module	Active Mode	Sleep Mode	DeepSleep Mode
LPUART0/1	✓	✓	✓(1)
CRC	✓	✓	×
TRNG	✓	✓	×
AES	✓	✓	×
LCD	✓	✓	✓
ADC	✓	✓	×
DAC	✓	✓	×
VC0/1/2	✓	✓	✓
LVD	✓	✓	✓
OPA	✓	✓	×
SWD	✓	✓	×
POR/BOR	✓	✓	✓

Notice

1. When the working clock is PCLK, wakeup from DeepSleep mode is not supported.

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3.7 Register Description

3.7.1 System Control Register (SCB_SCR) (Cortex-M0+ Core System Control Register)

Base address: 0xE000ED10

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																											SEVONPEND	RESERVED	SLEEPDEEP	SLEEPONEXIT	RESERVED
Access																												RW		RW	RW	

Bit	Name	Functional Description	Access
31:5	*Reserved*	-	-
4	SEVONPEND	Interrupt Pending Flag ● 0b1: A new event is generated upon each interrupt pending. If WFE is used to enter Sleep or DeepSleep mode, this event can wake up the processor	RW
3	*Reserved*	-	-
2	SLEEPDEEP	Sleep Mode Selection ● 0b0: Executing WFI or WFE enters Sleep mode ● 0b1: Executing WFI or WFE enters DeepSleep mode	RW
1	SLEEPONEXIT	Auto-Sleep Mark ● 0b0: This feature disabled ● 0b1: When exiting exception handling and returning to thread mode, the processor automatically enters Sleep or DeepSleep mode (WFI)	RW
0	*Reserved*	-	-

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4 SYSCTRL

4.1 System Clock Introduction

The clock control module primarily provides system clock, peripheral clock, and peripheral reset control functions.

This product provides the following different clock sources as the system clock:

- RC48M - Internal high-speed RC clock (output frequency: 4-48 MHz)
- RCH - Internal high-speed RC clock (output frequency:4-24MHz)
- RCL - Internal low-speed RC clock (configurable to 38.4 kHz or 32.768 kHz)
- XTH - External high-speed crystal oscillator clock
- XTL - External low-speed crystal oscillator clock
- PLL - Phase-locked loop clock

Note

1. When switching the system clock source, please follow the procedure strictly. See the System Clock Switching section for details.
2. XTL can not be connected to the crystal oscillator, and directly input the 32.768kHz clock signal from the PC14 pin. XTH can not be connected to the crystal oscillator, and directly input the 4-32MHz clock signal from the PF00 pin.

This product also contains the following two auxiliary clocks:

- RC10K - Internal 10kHz clock, for WDT and CLKTRIM modules
- RC150K - Internal 150kHz clock, for LVD and VC modules.

4.1.1 Clock Architecture Diagram

The clock architecture of this product is shown as follows:

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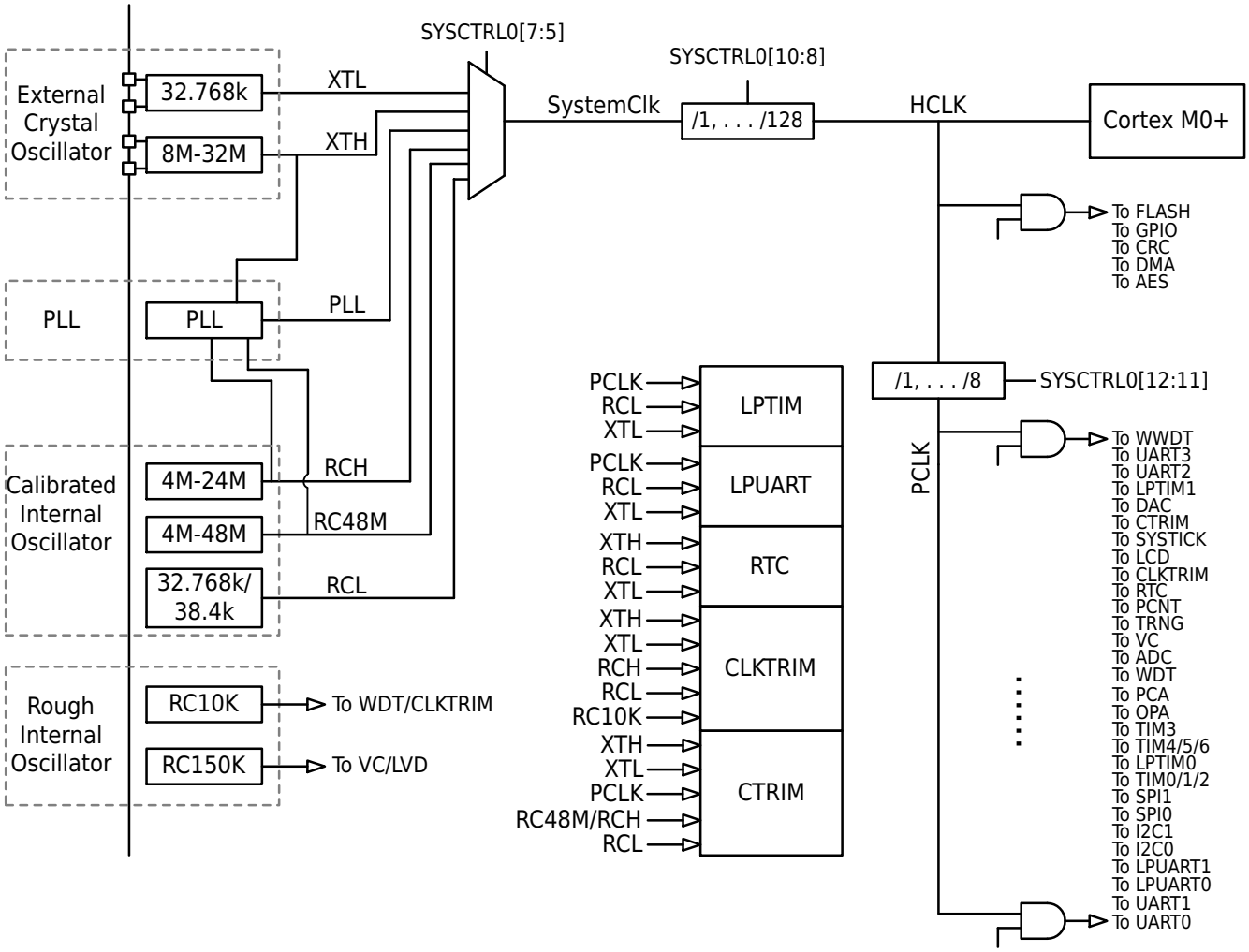

Figure 4-1 Clock Architecture Diagram

4.1.2 Clock Types

4.1.2.1 RCH

RCH is an internal high-speed clock oscillator with configurable and calibratable frequency. It is also the default clock source used after chip power-up or reset, with a frequency of 4 MHz; this high-speed clock automatically shuts down when the system enters DeepSleep mode.

The output frequency of RCH can be adjusted by changing the value of the register RCH_CR[10:0]. The register value increases by 1, then the output frequency of RCH will increase by about 0.2%, and the total adjustment range is 4-24MHz. 5 frequencies of 4MHz, 8MHz, 16MHz, 22.12MHz and 24MHz have been pre-adjusted before leaving the factory; if other frequencies are required, please manually adjust the value of this register.

For instructions on changing the RCH clock source frequency, please refer to the relevant description in chapter System Clock Switching.

The internal high-speed clock requires a short time from start up to stabilization. In order to respond to interrupts quickly in DeepSleep mode, it is recommended to switch the system clock source to RCH before entering DeepSleep mode.

4.1.2.2 RC48M

RC48M is an internal high-speed clock oscillator with configurable and calibratable frequency. The clock frequency can be configured through the RC48M_CR register. Four preset calibrated frequency configu-

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ration values—4MHz, 6MHz, 32MHz and 48MHz before leaving the factory can be directly loaded for use; it can also adjust the calibration value in this register to change to other frequencies or achieve higher-precision calibration according to actual needs.

When the system enters DeepSleep mode, this high-speed clock will be automatically turned off. It cannot be used as a wake-up clock, before entering DeepSleep mode, the system clock needs to be switched to RCH or SYSCTRL0.WAKEUP_BYRCH must be set to 1.

For instructions on changing the RC48M clock source frequency, please refer to the chapter System Clock Switching.

4.1.2.3 RCL

RCL is an internal low-speed clock with configurable and calibratable frequency.

The clock frequency can be configured through RCL_CR register, two preset calibrated frequency configuration values before leaving the factory: 32.768kHz and 38.4kHz, which can be directly loaded for use; it can also adjust the calibration value in this register to change to other frequencies or achieve higher-precision calibration according to actual needs.

When the system enters DeepSleep mode, this clock will not be automatically turned off, and the ultra-low power peripheral module can choose RCL as its clock.

4.1.2.4 XTL

XTL external low-speed crystal oscillator clock requires an external 32.768kHz low-power crystal oscillator, which has ultra-high precision and ultra-low power. When the system enters DeepSleep mode, this clock will not shut down automatically. Peripheral modules operating in ultra-low power mode can select XTL as their clock.

XTL supports an external active clock as input, allowing the input of a 32.768kHz clock signal directly from the PC14 pin without connecting a crystal. The method for inputting an active clock signal from PC14 is as follows:

- Configure the PC14 pin as a GPIO input;
- Configure the XTL stable time XTL_CR.STARTUP;
- Set SYSCTRL1.EXTL_EN to 1;
- Wait for the XTL stable flag to be set XTL_CR.STABLE.

Notice

The crystal, its matching capacitors, and the external clock source signal must comply with the requirements for the low-speed external clock XTL specified in the Electrical Specifications chapter of the Datasheet.

4.1.2.5 XTH

The external high-speed crystal oscillator clock requires an external high-speed crystal with a frequency of 8-32MHz. When the system enters DeepSleep mode, this clock will shut down automatically.

XTH supports an external active clock as input, allowing the input of a 4-32MHz clock signal directly from the PF00 pin without connecting a crystal. The method for inputting an clock signal from PF00 is as follows:

- Configure the PF00 pin as a GPIO input;
- Configure the XTH stable time XTH_CR.STARTUP;
- Set SYSCTRL1.EXTH_EN to 1;
- Wait for the XTH stable flag to be set XTH_CR.STABLE.

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Notice

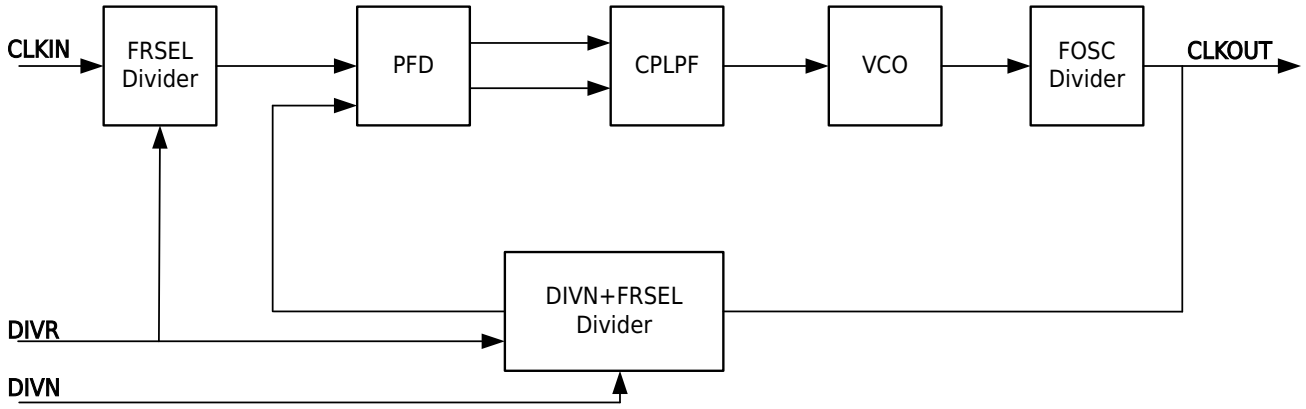
The crystal, its matching capacitors, and the external clock source signal must comply with the requirements for the high-speed external clock XTH specified in the Electrical Specifications section of the Datasheet.

4.1.2.6 PLL

Built-in PLL supports 8-48M clock output. The reference clock sources for the PLL are: RC48M, RCH, XTH crystal oscillator clock, and PF00 pin input clock.

The PLL consumes relatively high power during operation. Before entering DeepSleep mode, configure the system clock to RCH and disable the PLL and BGR, reconfigure the system clock to PLL upon wake-up.

PLL architecture diagram is as follows:



Its output frequency CLKOUT=DIVN×CLKIN, where CLKIN is the reference clock signal before the pre-divider FRSEL, and CLKOUT is the PLL output frequency signal after division by FOSC. Depending on the different output frequency and input frequency range, users need to select the corresponding FOSC, FRSEL, and DIVN values according to the contents of the PLL Control Register.

For example, if the input frequency comes from a 16MHz crystal oscillator circuit, then FRSEL=0b10. If the output frequency is 48MHz, then FOSC=0b1xx. 48MHz = 3 × 16 MHz, thus calculating DIVN = 0x3.

4.1.3 Clock Start Process

All of the above clock sources require a startup stabilization time. Taking XTH as example to illustrate the process of the clock startup and stabilization.

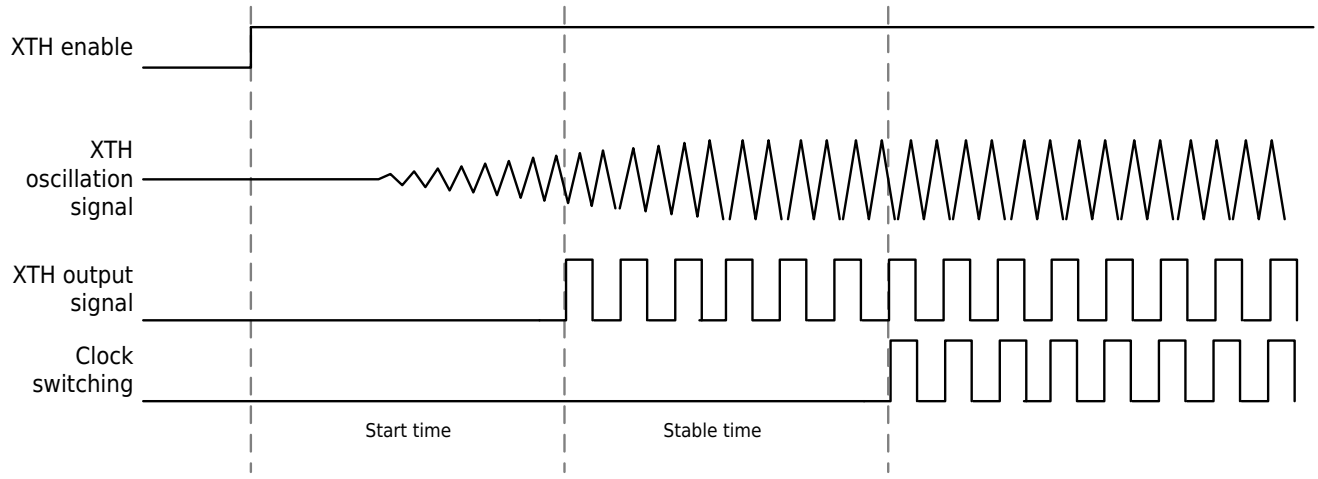


Figure 4-3 Crystal Oscillator Clock Startup Diagram

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4.2 System Clock Switching

4.2.1 System Clock Switching Introduction

The clock source of the system clock can be switched through SYSCTRL0.CLKSW among RCH, RCL, XTH, XTL, PLL, RC48M. When switching, any two of the clock sources RCH, RCL, XTH, XTL, and RC48M can be switched between each other; PLL can only be switched with RCH, RC48M, and XTH. The clock switching operation must be performed according to clock switching processes described below, otherwise abnormalities may occur.

The system clock source can be used as HCLK after system division, an appropriate frequency division value can be configured via SYSCTRL0.HCLK_PRS.

When switching the clock, FLASH_CR.WAIT must be configured accordingly based on the current and target HCLK frequencies.

- When HCLK≤24MHz, FLASH_CR.WAIT should be set to 0.
- When HCLK>24MHz, FLASH_CR.WAIT should be set to 1;

Note

For detailed instructions on setting FLASH_CR.WAIT, please refer to the chapter "FLASH Controller (FLASH)".

4.2.2 Switching Process

4.2.2.1 Standard Clock Switching Process

Procedure

Step1. If the new clock source requires an external pin, set the pin to the appropriate mode.

Note

An analog pin is required when connecting to an external crystal oscillator; GPIO input is required and the external clock input is enabled when connecting to an external clock input.

Step2. Configure the oscillation parameters of the new clock source.

Step3. Enable the oscillator of the new clock source.

Step4. If the frequency of the new clock source is higher than that of the previous one, configure the FLASH_CR.WAIT before switching, based on the new clock source frequency, following the procedure described in the chapter FLASH Controller.

Step5. Wait for the new clock source to output a stable frequency.

Step6. Configure SYSCTRL0.CLKSW to select the source of the system clock as the new clock source.

Step7. If the frequency of the new clock source is lower than that of the previous one, configure the FLASH_CR.WAIT after switching, based on the new clock source frequency, following the procedure described in the chapter FLASH Controller.

Step8. Turn off clock sources that are no longer in use.

4.2.2.2 RCH Switching Process between Different Oscillation Frequencies

Procedure

Write the factory-preset TRIM value to RCH_CR[10:0] to adjust the target output frequency of RCH.

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4.2.3 Examples of Switching

4.2.3.1 Example of Switching from Other Clocks to XTL

Procedure

Step1. Set PCADS.14 and PCADS.15 to 1, configure PC14/PC15 pins as analog ports.

Step2. Configure the parameters in the XTL_CR register according to the features of the crystal and the system.

Step3. Write 0x5A5A and 0xA5A5 to SYSCTRL2 register in sequence to enable register rewriting.

Step4. Set SYSCTRL0.XTL_EN to 1 to enable the crystal oscillator circuit.

Step5. Query and wait for the XTL_CR.STABLE flag to become 1, and the crystal oscillator outputs a stable clock.

Step6. Write 0x5A5A and 0xA5A5 to SYSCTRL2 register in sequence to enable register rewriting.

Step7. Set SYSCTRL0.CLKSW to 3, switch the system clock to XTL.

Step8. See the chapter FLASH Controller to set FLASH_CR.WAIT to 0.

Step9. Write 0x5A5A and 0xA5A5 to SYSCTRL2 register in sequence to enable register rewriting.

Step10. Turn off the clock source that is no longer used.

4.2.3.2 Example of Switching from Other Clocks to XTH

Procedure

Step1. Set PFADS.0 and PFADS.1 to 1, configure PF00/PF01 pin as analog ports.

Step2. Configure XTH_CR[3:0] according to the features of the crystal oscillator.

Step3. Set XTH_CR.STARTUP to 3, then choose the longest crystal oscillator stable time.

Step4. Write 0x5A5A and 0xA5A5 to SYSCTRL2 register in sequence to enable register rewriting.

Step5. Set SYSCTRL0.XTH_EN to 1, then enable the crystal oscillator circuit.

Step6. According to the higher frequency of the current clock and XTH, configure FLASH_CR.WAIT according to Flash Controller.

Step7. Query and wait for the XTH_CR.STABLE flag to become 1, the software delays for more than 10ms, and the oscillator outputs a stable clock.

Step8. Write 0x5A5A and 0xA5A5 to SYSCTRL2 register in sequence to enable register rewriting.

Step9. Set SYSCTRL0.CLKSW to 1, switch the system clock to XTH.

Step10. According to the frequency of XTH, configure FLASH_CR.WAIT in terms of Flash Controller.

Step11. Write 0x5A5A and 0xA5A5 to SYSCTRL2 register in sequence to enable register rewriting.

Step12. Turn off the clock source that is no longer used.

4.2.3.3 Example of Switching from Other Clocks to RCL

Procedure

Step1. Configure RCL_CR.TRIM and RCL_CR.STARTUP.

Step2. Write 0x5A5A and 0xA5A5 to SYSCTRL2 register in sequence to enable register rewriting.

Step3. Set SYSCTRL0.RCL_EN to 1 to enable the RCL oscillation circuit.

Step4. Query and wait for RCL_CR.STABLE flag to become 1, and the RCL outputs a stable clock.

Step5. Write 0x5A5A and 0xA5A5 to SYSCTRL2 register in sequence to enable register rewriting.

Step6. Set SYSCTRL0.CLKSW to 2, switch the system clock to RCL.

Step7. See the chapter FLASH Controller to set FLASH_CR.WAIT to 0.

Step8. Write 0x5A5A and 0xA5A5 to SYSCTRL2 register in sequence to enable register rewriting.

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Step9. Turn off the clock source that is no longer used.

4.2.3.4 Example of Switching from Other Clocks to RCH

Procedure

Step1. Configure RCH_CR.TRIM.

Step2. Write 0x5A5A and 0xA5A5 to SYSCTRL2 register in sequence to enable register rewriting.

Step3. Set SYSCTRL0.RCH_EN to 1 to enable the RCH oscillation circuit.

Step4. Query and wait for RCH_CR.STABLE flag to become 1, and the RCH outputs a stable clock.

Step5. Write 0x5A5A and 0xA5A5 to SYSCTRL2 register in sequence to enable register rewriting.

Step6. Set SYSCTRL0.CLKSW to 0, switch the system clock to RCH.

Step7. See the chapter FLASH Controller to set FLASH_CR.WAIT to 0.

Step8. Write 0x5A5A and 0xA5A5 to SYSCTRL2 register in sequence to enable register rewriting.

Step9. Turn off the clock source that is no longer used.

4.2.3.5 Example of Switching from Other Clocks to RC48M

Procedure

Step1. According to the higher frequency between the current clock and the RC48M clock to be configured, configure FLASH_CR.WAIT following the procedure described in chapter FLASH Controller.

Step2. Write the preset value to the RC48M_CR register to configure the desired clock frequency.

Step3. Write 0x5A5A and 0xA5A5 to SYSCTRL2 register in sequence to enable register rewriting.

Step4. Set SYSCTRL0.RC48M_EN to 1, enable RC48M oscillation circuit.

Step5. Query and wait for RC48M_CR.STABLE flag to become 1, RC48M outputs a stable clock.

Step6. Write 0x5A5A and 0xA5A5 to SYSCTRL2 register in sequence to enable register rewriting.

Step7. Set SYSCTRL0.CLKSW to 5, switch the system clock to RC48M.

Step8. According to the frequency of RC48M, configure FLASH_CR.WAIT according to the procedures in chapter Flash Controller.

Step9. Write 0x5A5A and 0xA5A5 to SYSCTRL2 register in sequence to enable register rewriting.

Step10. Turn off the clock source that is no longer used.

4.2.3.6 Example of Switching between PLL and RCH, the Reference Clock is RCH

Context

> **Notice**
> RCH_CR.TRIM must not be changed during switching.

Procedure

- Switch from RCH to PLL

  Step1. Enable the BGR and delay the $T_{stable(BGR)}$ period (refer to the "Electrical Specifications - Operating Conditions - Internal Reference Voltage" section in the Datasheet for the specific value), then wait for the BGR to start up and stabilize.

  Step2. Set PLL_CR.REFSEL to 3 select the PLL clock source as RCH.

  Step3. Configure PLL_CR.FRSEL according to the RCH frequency.

  Step4. According to the PLL output frequency, configure PLL_CR.DIVN and PLL_CR.FOSC.

  Step5. Set PLL_CR.STARTUP to 7, then choose the longest PLL stable time.

  Step6. Write 0x5A5A and 0xA5A5 to SYSCTRL2 register in sequence to enable register rewriting.

  Step7. Set SYSCTRL0.PLL_EN to 1 to enable the PLL oscillation circuit.

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Step8. Configure FLASH_CR.WAIT based on the PLL output frequency in terms of FLASH Controller.

Step9. Query and wait for PLL_CR.STABLE flag to become 1, and the PLL outputs a stable clock.

Step10. Write 0x5A5A and 0xA5A5 to SYSCTRL2 register in sequence to enable register rewriting.

Step11. Set SYSCTRL0.CLKSW to 4, switch the system clock to PLL.

- Switch from PLL to RCH

Step1. Write 0x5A5A and 0xA5A5 to SYSCTRL2 register in sequence to enable register rewriting.

Step2. Set SYSCTRL0.CLKSW to 0,switch the system clock to RCH.

Step3. Set FLASH_CR.WAIT to 0 in terms of FLASH Controller.

Step4. Write 0x5A5A and 0xA5A5 to SYSCTRL2 register in sequence to enable register rewriting.

Step5. Set SYSCTRL0.PLL_EN to 0, turn off PLL.

Step6. Decide whether to disable the BGR based on the actual usage of other modules (such as ADC, etc.).

4.2.3.7 Example of Switching between PLL and XTH, the Reference Clock is XTH

Procedure

- Switch from XTH to PLL

Step1. Enable the BGR and delay the $T_{stable(BGR)}$ period (refer to the "Electrical Specifications - Operating Conditions - Internal Reference Voltage" section in the Datasheet for the specific value), then wait for the BGR to start up and stabilize.

Step2. Set PLL_CR.REFSEL to 0, select the PLL clock source as XTH.

Step3. According to XTH frequency, configure PLL_CR.FRSEL.

Step4. Configure PLL_CR.DIVN and PLL_CR.FOSC according to the PLL output frequency.

Step5. Set PLL_CR.STARTUP to 7, then choose the longest PLL stable time.

Step6. Write 0x5A5A and 0xA5A5 to the SYSCTRL2 register in sequence to enable register rewriting.

Step7. Set SYSCTRL0.PLL_EN to 1 to enable the PLL oscillation circuit.

Step8. Configure FLASH_CR.WAIT based on the PLL output frequency in terms of FLASH Controller.

Step9. Query and wait for the PLL_CR.STABLE flag to become 1, and the PLL outputs a stable clock.

Step10. Write 0x5A5A and 0xA5A5 to the SYSCTRL2 register in sequence to enable register rewriting.

Step11. Set SYSCTRL0.CLKSW to 4, switch the system clock to PLL.

- Switch from PLL to XTH

Step1. Write 0x5A5A and 0xA5A5 to SYSCTRL2 register in sequence to enable register rewriting.

Step2. Set SYSCTRL0.CLKSW to 1, switch the system clock to XTH.

Step3. According to the frequency of XTH, configure FLASH_CR.WAIT in terms of Flash Controller.

Step4. Write 0x5A5A and 0xA5A5 to the SYSCTRL2 register in sequence to enable register rewriting.

Step5. Set SYSCTRL0.PLL_EN to 0, turn off PLL.

Step6. Decide whether to disable the BGR based on the actual usage of other modules (such as ADC, etc.).

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4.2.4 Clock Switching Diagram

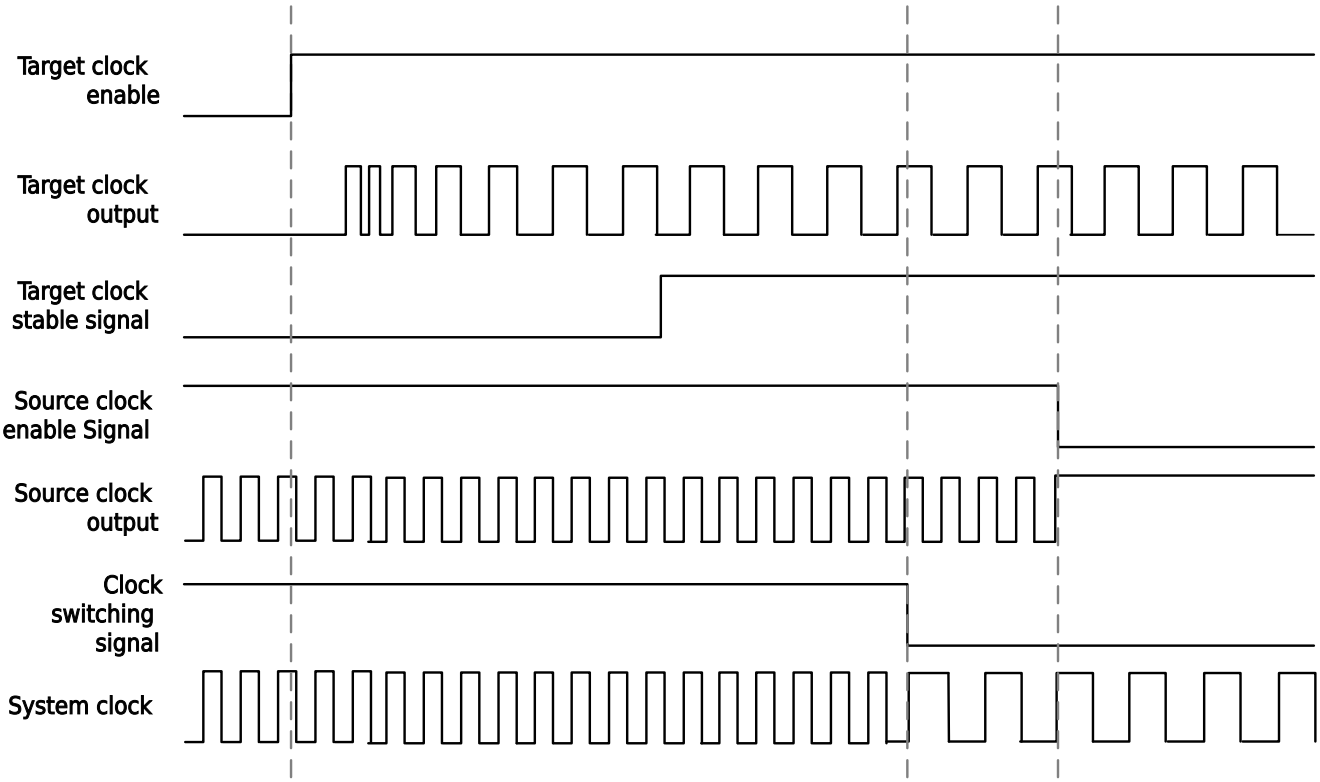

Figure 4-4 Clock Switching Diagram

4.3 Clock Calibration Module

This product integrates an internal clock calibration circuit CLKTRIM and CTRIM modules. For more information, see the relevant chapter descriptions.

4.4 Interrupt Wakeup Control

When the processor executes the WFI instruction to enter the Sleep/DeepSleep state, it will stop executing instructions. When an interrupt request (higher priority) occurs during Sleep/DeepSleep and needs to be serviced, the processor is woken up.

The behavior of the processor in the Sleep/DeepSleep state when receiving an interrupt request is shown in the following table:

PRIMASK Status	WFI Behavior	Wakeup	ISR Execution
0	IRQ Priority > Current Class	Y	Y
0	IRQ Priority≤ Current Class	N	N
1	IRQ Priority > Current Class	Y	N
1	IRQ Priority≤ Current Class	N	N

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4.4.1 Executing Interrupt Service after Waking from DeepSleep mode

Procedure

Step1. Enable the NVIC corresponding to the module that needs to wake up the processor.

Step2. Enable the interrupt corresponding to the module that needs to wake up the processor.

Step3. Set SCB->SCR.SLEEPDEEP to 1.

Step4. Execute WFI instruction enter the DeepSleep mode.

Step5. The system enters the DeepSleep mode and waits for the interrupt to wake up, and executes the interrupt service program after waking up.

Examples

```
SCB->SCR |= 0x00000004u;
while(1)
{
  __asm("WFI");
}
```

4.4.2 Interrupt Service Not Executed after Waking from DeepSleep mode

Procedure

Step1. Enable the NVIC corresponding to the module that needs to wake up the processor.

Step2. Enable the interrupt corresponding to the module that needs to wake up the processor.

Step3. Set PRIMASK to 1.

Step4. Set SCB->SCR.SLEEPDEEP to 1.

Step5. Execute WFI instruction enter the DeepSleep mode.

Step6. The system enters the DeepSleep mode and waits for the interrupt to wake up, and executes the next instruction after waking up;

Step7. Clear interrupt flag, clear interrupt pending status.

Step8. Execute user-defined operations.

Examples

```
__asm("CPSID I");//Set PRIMASK
SCB->SCR |= 0x00000004u;
while(1)
{
  __asm("WFI");
  ...//Clear the interrupt flag of the wake-up interrupt
  ...//Clear the interrupt pending status of the wake-up interrupt
  ...//Perform user-defined operation
}
```


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4.4.3 Using Sleep-on-exit Feature

Context

Sleep-on-exit is ideal for interrupt-driven applications. When this feature is enabled, the processor enters Sleep/DeepSleep mode whenever exception handling is completed and returns to thread mode. With the sleep-on-exit feature, the processor can be in Sleep/DeepSleep mode as much as possible.

Cortex-M0+ take use of the sleep-on-exit feature to enter Sleep/DeepSleep. This situation is similar to the effect of executing WFI immediately after executing an abnormal exit. Attention: in order to avoid the need to push the stack when entering an exception next time, the processor will not perform the process of popping the stack.

Procedure

Step1. Enable the NVIC corresponding to the module that needs to wake up the processor.

Step2. Enable the interrupt corresponding to the module that needs to wake up the processor.

Step3. Set SCB->SCR.SLEEPDEEP to 1.

Step4. Set SCB->SCR.SLEEPONEXIT to 1.

Step5. Execute WFI instruction enter the DeepSleep mode.

Step6. The system enters the DeepSleep mode and waits for the interrupt to wake up, and executes the interrupt service subroutine after waking up.

Step7. Automatically enters DeepSleep mode when exiting interrupt service.

Examples

```
SCB->SCR |= 0x00000004u;
SCB->SCR |= 0x00000002u;
while(1)
{
  __asm("WFI");
}
```

4.5 Reset Control

4.5.1 Reset Controller Overview

This product has 8 reset signal sources, each of which can make the CPU run again. Most registers will be reset to reset values, and the program will start executing from the reset vector.

- Digital area power-on and power-off reset POR
- External Reset PAD, low level is reset signal
- WWDT reset
- WDT reset
- PCA reset
- LVD low voltage reset
- Cortex-M0+ SYSRESETREQ software reset
- Cortex-M0+ LOCKUP hardware reset

Each reset source is indicated by a corresponding reset flag. Reset flags are set by hardware and need to be cleared by user software. When the chip is reset, if RESET_FLAG.POR15V or RESET_FLAG.POR5V is 1, it is a **power-on reset**. When **power-on a reset**, the user program should clear the RESET_FLAG register

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to zero. Then, the reset source can be determined by the relevant bits of RESET_FLAG during the next reset.

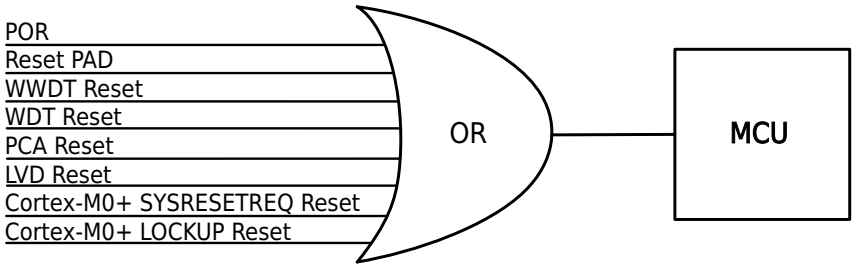

Figure 4-5 Reset Source Diagram

4.5.2 Reset Function

4.5.2.1 Power-on and Power-off Reset POR

This product has two power supply areas: VCC area and VCAP area. All analog modules and IO work in the VCC area; other modules work in the VCAP area.

- When the VCC area is powered on, when the VCC voltage is lower than the POR threshold voltage, POR5V signal is generated; when the VCC area is powered off, when the VCC voltage is lower than the BOR threshold voltage, POR5V signal is generated.
- When the VCAP area is powered on, when the VCAP voltage is lower than the POR threshold voltage, POR15V signal is generated; when the VCAP area is powered off, when the VCAP voltage is lower than the BOR threshold voltage, POR15V signal is generated.

Both the POR5V signal and the POR15V signal will reset the chip's registers to the initialization state.

4.5.2.2 External Reset Pin Reset

A system reset is generated when the external reset pin detects a low level. The reset pin has a built-in pull-up resistor and integrates a glitch filter circuit. The glitch filter circuit filters out glitches shorter than a certain time width. Therefore, the low-level signal applied to the reset pin must exceed this time width to ensure a reliable reset of the chip. For specific timing parameters, see the RESETB Pin Features section under the chapter "Electrical Specifications" in the Datasheet.

4.5.2.3 Watchdog Reset

For watchdog reset, refer to the relevant introductions in the chapters "Watchdog Timer (WDT)" and "Window Watchdog (WWDT)".

4.5.2.4 PCA Reset

For PCA reset, see the relevant introduction in the Programmable Count Array (PCA) chapter.

4.5.2.5 LVD Low Voltage Reset

For LVD low voltage reset, refer to the relevant introduction in the "Low Voltage Detector (LVD)" chapter.

4.5.2.6 Cortex-M0+ SYSRESETREQ Reset

Cortex-M0+ software reset.

4.5.2.7 Cortex-M0+ LOCKUP Reset

When Cortex-M0+ encounters a serious exception, it will stop its own PC pointer at the current address and lock it, and reset the entire CORE area after a delay of several clock cycles. This reset function is enabled when SYSCTRL1.LOCKUP_EN is set to 1.

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4.6 Register Description

4.6.1 Register List

Base address: 0x40002000

Table 4-2 System Controller (SYSCTRL) Register Offset

Offset	Register	Description	Width
0x00	SYSCTRL0	System Control Register 0	32
0x04	SYSCTRL1	System Control Register 1	32
0x08	SYSCTRL2	System Control Register 2	32
0x54	RC48M_CR	RC48M Control Register	32
0x0C	RCH_CR	RCH Control Register	32
0x10	XTH_CR	XTH Control Register	32
0x14	RCL_CR	RCL Control Register	32
0x18	XTL_CR	XTL Control Register	32
0x3C	PLL_CR	PLL Control Register	32
0x1C	RESET_FLAG	Reset Flag Register	32
0x20	PERI_CLKEN0	Peripheral Module Clock Control Register 0	32
0x24	PERI_CLKEN1	Peripheral Module Clock Control Register 1	32
0x28	PERI_RESET0	Peripheral Module Reset Control Register 0	32
0x2C	PERI_RESET1	Peripheral Module Reset Control Register 1	32
0x38	DEBUG_ACTIVE	Peripheral Debug Function Enable Register	32

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4.6.2 System Control Register 0 (SYSCTRL0)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000001																															
Name	Reserved																WAKEUP_BYRCH	Reserved	RC48M_EN	PCLK_PRS		HCLK_PRS		CLKSW		PLL_EN	XTL_EN	RCL_EN	XTH_EN	RCH_EN	
Access																	RW		RW	RW		RW		RW		RW	RW	RW	RW	RW	

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15	WAKE-UP_BYRCH	System clock source control bit after wake-up ● 0b0: After waking up from DeepSleep mode, the system clock source remains unchanged. ● 0b1: After waking up from DeepSleep mode, the system clock source switches to RCH, and the original clock source remains enabled.	RW
14	*Reserved*	-	-
13	RC48M_EN	Internal high-speed clock RC48M enable signal ● 0b0: Disable ● 0b1: Enable **Notice** Before enabling the RC48M clock each time, the RC48M_CR register parameters must be fully loaded as specified in RC48M_CR Control Register; otherwise, the RC48M clock may not operate correctly. **Note** When the system enters DeepSleep, this high-speed clock will be automatically turned off.	RW
12:11	PCLK_PRS	PCLK clock source selection ● 0b00: HCLK ● 0b01: HCLK/2 ● 0b10: HCLK/4 ● 0b11: HCLK/8	RW
10:8	HCLK_PRS	HCLK system frequency division selection ● 0b000: SystemClk ● 0b001: SystemClk/2 ● 0b010: SystemClk/4 ● 0b011: SystemClk/8 ● 0b100: SystemClk/16 ● 0b101: SystemClk/32	RW

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Bit	Name	Functional Description	Access
10:8	HCLK_PRS	● 0b110: SystemClk/64 ● 0b111: SystemClk/128	RW
7:5	CLKSW	SystemClk clock source selection ● 0b000: RCH ● 0b001: XTH ● 0b010: RCL ● 0b011: XTL ● 0b100: PLL ● 0b101: RC48M	RW
4	PLL_EN	PLL enable control ● 0b0: Disable ● 0b1: Enable **Note** PLL can only be enabled after BGR is enabled and stable.	RW
3	XTL_EN	External low-speed crystal oscillator XTL enable control ● 0b0: Disable ● 0b1: Enable **Note** PC14 and PC15 need to be set as analog ports.	RW
2	RCL_EN	Internal low-speed clock RCL enable control ● 0b0: Disable ● 0b1: Enable	RW
1	XTH_EN	External high-speed crystal oscillator XTH enable control ● 0b0: Disable ● 0b1: Enable **Note** PF00, PF01 need to be set as analog ports. When the system enters DeepSleep, this high-speed clock will be automatically turned off.	RW
0	RCH_EN	Internal high-speed clockRCH enable control ● 0b0: Disable ● 0b1: Enable **Note** When the system enters DeepSleep, this high-speed clock will be automatically turned off.	RW

Note

Every time you rewrite the value of SYSCTRL0 or SYSCTRL1, you need to write 0x5A5A and 0xA5A5 to SYSCTRL2 in sequence. Such steps can effectively prevent misoperation of SYSCTRL0 or SYSCTRL1 register.

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4.6.3 System Control Register 1 (SYSCTRL1)

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000008																															
Name	Reserved																				RTC_FREQ_ADJUST			SWD_USE_IO	Reserved		LOCKUP_EN	RTC_LPW	Reserved		XTL_ALWAYS_ON	EXTL_EN	EXTH_EN	Reserved
Access																					RW			RW			RW	RW			RW	RW	RW	

Bit	Name	Functional Description	Access
31:12	*Reserved*	-	-
11:9	RTC_FREQ_ADJUST	RTC high-speed clock compensation clock frequency selection ● 0b000: 4M ● 0b001: 6M ● 0b010: 8M ● 0b011: 12M ● 0b100: 16M ● 0b101: 20M ● 0b110: 24M ● 0b111: 32M	RW
8	SWD_USE_IO	SWD port function configuration ● 0b0: SWD port ● 0b1: GPIO port	RW
7	*Reserved*	-	-
6	LOCKUP_EN	Cortex-M0+ LockUp enable ● 0b0: Disable ● 0b1: Enable **Note** After enabling, the CPU will reset the MCU when it reads an invalid command, which can enhance system reliability.	RW
5	RTC_LPW	RTC module low power control ● 0b0: Disable ● 0b1: Enable **Note** After enabling, the RTC module enters low-power mode, and writing to the RTC calendar time register is prohibited. Writes to its registers will not be synchronized; synchronization occurs only after exiting low-power mode, during which timing may be lost.	RW

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Bit	Name	Functional Description	Access
4	*Reserved*	-	-
3	XTL_AL-WAYS_ON	XTL enable permission control ● 0b0: SYSCTRL0.XTL_EN can be set and cleared. ● 0b1: SYSCTRL0.XTL_EN can only be set.	RW
2	EXTL_EN	External XTL clock source control ● 0b0: XTL is generated by a crystal. ● 0b1: XTL clock source is input from PC14 **Note** When using PC14 input clock, it is necessary to set SYSCTRL0.XTL_EN to 0.	RW
1	EXTH_EN	External XTH clock source control ● 0b0: XTH is generated by a crystal. ● 0b1: XTH clock source is input from PF00 **Note** When using PF00 input clock: 1. SYSCTRL0.XTH_EN must be set to 0. 2. SYSCTRL0.WAKEUP_BYRCH must be set to 1; otherwise, abnormal current consumption may occur in low-power mode.	RW
0	*Reserved*	-	-

Note

Every time you rewrite the value of SYSCTRL0 or SYSCTRL1, you need to write 0x5A5A and 0xA5A5 to SYSCTRL2 in sequence. Such steps can effectively prevent misoperation of SYSCTRL0 or SYSCTRL1 registers.

4.6.4 System Control Register 2 (SYSCTRL2)

Offset	Bit Position																													
0x08	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								SYSCTRL2							
Access																									WO							

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-

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Bit	Name	Functional Description	Access
15:0	SYSCTRL2	SYSCTL0 register and SYSCTRL1 protection control register Write 0x5A5A first to SYSCTRL2, and then write 0xA5A5 to start the write operation to SYSCTRL0 and SYSCTRL1 register. As long as the write operation is performed to SYSCTRL0 or SYSCTRL1 register, this protection bit automatically recovery to the protection state. Subsequent write operations to SYSCTRL0 or SYSCTRL1 require repeating the previous steps.	WO

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4.6.5 RC48M Control Register (RC48M_CR)

Offset	Bit Position																													
0x54	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x08000080																															
Name	STABLE	Reserved			TCTRIM			Reserved							FSEL		TRIMC								TRIMF					Reserved		
Access	RO				RW										RW		RW								RW							

Bit	Name	Functional Description	Access
31	STABLE	RC48M clock stable flag bit ● 0b0: RC48M is not stable and cannot be used by internal circuits. ● 0b1: RC48M is stable and can be used by internal circuits.	RO
30:28	*Reserved*	-	-
27:24	TCTRIM	Oscillation frequency temperature coefficient TRIM This bit does not support independent configuration. For configuration details, refer to the instructions.	RW
23:18	*Reserved*	-	-
17:16	FSEL	Operating frequency selection This bit does not require independent configuration. For parameter selection, refer to the instructions. ● 0b00: 4MHz ● 0b01: 6MHz ● 0b10: 32MHz ● 0b11: 48MHz	RW
15:8	TRIMC	Coarse adjustment of clock frequency Parameter selection details are provided in the instructions.	RW
7:2	TRIMF	Clock frequency fine tuning Parameter selection details are provided in the instructions.	RW
1:0	*Reserved*	-	-

Note

RC48M clock frequency adjustment: changing the value of this register allows you to adjust the output frequency of RC48M.

The Flash already contains several sets of calibration values and configuration parameters. By reading all the data from the specified addresses in Flash and writing them into the entire RC48M_CR register, you can obtain an accurate frequency.

- 48MHz calibration value address: 0x00101B04 - 0x00101B07
- 32MHz calibration value address: 0x00101B0C - 0x00101B0F
- 6MHz calibration value address: 0x00101B10 - 0x00101B13
- 4MHz calibration value address: 0x00101B14 - 0x00101B17

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4.6.6 RCH Control Register (RCH_CR)

Offset	Bit Position																													
0x0C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000126																															
Name	Reserved																				STABLE	TRIM									
Access																					RO	RW									

Bit	Name	Functional Description	Access
31:12	*Reserved*	-	-
11	STABLE	RCH clock stable flag bit ● 0b0: RCH is not stable and cannot be used by internal circuits. ● 0b1: RCH is stable and can be used by internal circuits.	RO
10:0	TRIM	Clock frequency adjustment Modify the value of this register to adjust the output frequency of the RCH. The register value increases by 1, then the output frequency of RCH will increase by about 0.2%, and the total adjustment range is 4-24 MHz. 5 groups of frequency calibration values have been saved in Flash, and the precise frequency can be obtained by reading out the calibration values in Flash and writing them into RCH_CR.TRIM. ● 24MHz calibration value address: 0x00101BE0-0x00101BE1 ● 22.12MHz calibration value address: 0x00101BE2-0x00101BE3 ● 16MHz calibration value address: 0x00101BE4-0x00101BE5 ● 8MHz calibration value address: 0x00101BE6-0x00101BE7 ● 4MHz calibration value address: 0x00101BE8-0x00101BE9	RW

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4.6.7 XTH Control Register (XTH_CR)

Offset	Bit Position																													
0x10	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000022																															
Name	Reserved																									STABLE	STARTUP		XTH_FSEL		DRIVER	
Access																										RO	RW		RW		RW	

Bit	Name	Functional Description	Access
31:7	*Reserved*	-	-
6	STABLE	External high-speed crystal oscillator stable flag bit ● 0b0: XTH is not stable and cannot be used by internal circuits. ● 0b1: XTH is stable and can be used by internal circuits. **Note** In order to increase system reliability, after querying this flag, the software needs to delay more than 10ms before switching the system clock to XTH.	RO
5:4	STARTUP	External high-speed crystal oscillator stable time selection ● 0b00: 256 cycles ● 0b01: 1024 cycles ● 0b10: 4096 cycles ● 0b11: 16384 cycles (Recommended value) **Notice** It is highly recommended to set the stable time of XTH to 0b11. If the XTH stable time is insufficient, the system will not work stably when performing clock switching or waking up from DeepSleep.	RW
3:2	XTH_FSEL	External crystal oscillator operating frequency selection ● 0b00: 8M ● 0b01: 8M-16M ● 0b10: 16M-24M ● 0b11: 24M-32M	RW

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Bit	Name	Functional Description	Access
1:0	DRIVER	External crystal oscillator driving capability selection ● 0b00: Weakest driving capability ● 0b01: Weaker driving capability ● 0b10: Stronger driving capability (Recommended value) ● 0b11: Strongest driving capability **Note** It is necessary to select an appropriate driving capability according to the characteristics of the crystal oscillator, the load capacitance and the parasitic parameters of the circuit board. The greater the driving capability, the greater the power consumption; the weaker the driving capability, the smaller the power consumption.	RW

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4.6.8 RCL Control Register (RCL_CR)

Offset	Bit Position																													
0x14	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000033F																															
Name	Reserved																			STABLE	STARTUP		TRIM									
Access																				RO	RW		RW									

Bit	Name	Functional Description	Access
31:13	*Reserved*	-	-
12	STABLE	Internal low-speed clock RCL stable flag ● 0b0: RCL is not stable and cannot be used by internal circuits. ● 0b1: RCL is stable and can be used by internal circuits.	RO
11:10	STARTUP	Internal low-speed clock RCL stable time selection ● 0b00: 4 cycles ● 0b01: 16 cycles ● 0b10: 64 cycles ● 0b11: 256 cycles	RW
9:0	TRIM	Internal low-speed clock frequency adjustment 2 sets of frequency calibration values are stored in Flash. The precise frequency can be obtained by reading out the calibration value in Flash and writing it into RCL_CR.TRIM. ● 38.4kHz calibration value address: 0x00101BDC-0x00101BDD ● 32.768kHz calibration value address: 0x00101BDE-0x00101BDF	RW

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4.6.9 XTL Control Register (XTL_CR)

Offset	Bit Position																													
0x18	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000022																															
Name	Reserved																									STABLE	STARTUP		AMP_SEL		DRIVER	
Access																										RO	RW		RW		RW	

Bit	Name	Functional Description	Access
31:7	*Reserved*	-	-
6	STABLE	External low-speed crystal oscillator stable flag bit ● 0b0: XTL is not stable and cannot be used by internal circuits. ● 0b1: XTL is stable and can be used by internal circuits.	RO
5:4	STARTUP	External low-speed crystal oscillator stable time selection ● 0b00: 256 cycles ● 0b01: 1024 cycles ● 0b10: 4096 cycles ● 0b11: 16384 cycles (Recommended value)	RW
3:2	AMP_SEL	XTL crystal oscillation amplitude adjustment ● 0b00: minimum amplitude ● 0b01: normal amplitude ● 0b10: larger amplitude (Recommended value) ● 0b11: maximum amplitude	RW
1:0	DRIVER	XTL crystal oscillator driving capability selection ● 0b00: Setting prohibited ● 0b01: Setting prohibited ● 0b10: Stronger driving capability (Recommended value) ● 0b11: Strongest driving capability **Note** It is necessary to select an appropriate driving capability according to the characteristics of the crystal oscillator, the load capacitance and the parasitic parameters of the circuit board. The greater the driving capability, the greater the power consumption; the weaker the driving capability, the smaller the power consumption.	RW

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4.6.10 PLL Control Register (PLL_CR)

Offset	Bit Position																													
0x3C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00010B0F																															
Name	Reserved													STABLE	STARTUP		FRSEL		LFSEL		IBSEL		DIVN					FOSC		REFSEL		
Access														RO	RW		RW		RW		RW		RW					RW		RW		

Bit	Name	Functional Description	Access
31:19	*Reserved*	-	-
18	STABLE	PLL stable flag ● 0b0: PLL is not stable ● 0b1: PLL is stable	RO
17:15	STARTUP	PLL stable time selection ● 0b000: 128 PLL cycles ● 0b001: 256 PLL cycles ● 0b010: 512 PLL cycles ● 0b011: 1024 PLL cycles ● 0b100: 2048 PLL cycles ● 0b101: 4096 PLL cycles ● 0b110: 8192 PLL cycles ● 0b111: 16384 PLL cycles	RW
14:13	FRSEL	PLL input frequency selection Configure as follows according to the input clock frequency of the PLL: ● 0b00: 4M-6M ● 0b01: 6M-12M ● 0b10: 12M-20M ● 0b11: 20M-24M	RW
12:11	LFSEL	PLL filter control bit Must retain the default value	RW
10:9	IBSEL	PLL bias current selection Must retain the default value	RW
8:5	DIVN	PLL output clock frequency multiplier factor The multiple of the PLL output frequency to the input frequency: Output frequency = DIVN × Input frequency, where DIVN ranges from 0x2 to 0xC.	RW

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Bit	Name	Functional Description	Access
4:2	FOSC	PLL output frequency range selection Configure as follows according to the output clock frequency of the PLL: ● 0b000: 8M-12M ● 0b001: 12M-18M ● 0b010: 18M-24M ● 0b011: 24M-36M ● 0b1xx: 36M-48M	RW
1:0	REFSEL	Input clock selection ● 0b00: Clock generated by XTH crystal oscillator ● 0b01: Clock input from pin PF00 for XTH (see External high-speed crystal oscillator clock XTH) ● 0b10: RC48M clock ● 0b11: RCH clock	RW

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4.6.11 Reset Flag Register (RESET_FLAG)

Note

The reset value is 0x03 at power-on reset. After the program determines the reset source, it should clear the register so that it can determine the reset source the next time a reset occurs.

Offset	Bit Position																													
0x1C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000003																															
Name	Reserved																							WWDT	RSTB	SYSREQ	LOCKUP	PCA	WDT	LVD	POR15V	POR5V
Access																								RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:9	*Reserved*	-	-
8	WWDT	WWDT reset flag Write 0 to clear flag, write 1 has no effect Read: ● 0b0: No reset occurred ● 0b1: Reset occurred	RW
7	RSTB	RESETB port reset flag Write 0 to clear flag, write 1 has no effect Read: ● 0b0: No reset occurred ● 0b1: Reset occurred	RW
6	SYSREQ	Cotrex-M0+ CPU software reset flag Write 0 to clear flag, write 1 has no effect Read: ● 0b0: No reset occurred ● 0b1: Reset occurred	RW
5	LOCKUP	Cotrex-M0+ CPU Lockup reset flag Write 0 to clear flag, write 1 has no effect Read: ● 0b0: No reset occurred ● 0b1: Reset occurred	RW
4	PCA	PCA reset flag Write 0 to clear flag, write 1 has no effect Read: ● 0b0: No reset occurred ● 0b1: Reset occurred	RW

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Bit	Name	Functional Description	Access
3	WDT	WDT reset flag Write 0 to clear flag, write 1 has no effect Read: ● 0b0: No reset occurred ● 0b1: Reset occurred	RW
2	LVD	LVD reset flag Write 0 to clear flag, write 1 has no effect Read: ● 0b0: No reset occurred ● 0b1: Reset occurred	RW
1	POR15V	VCAP domain reset flag Write 0 to clear flag, write 1 has no effect Read: ● 0b0: No reset occurred ● 0b1: Reset occurred	RW
0	POR5V	VCC power domain reset flag Write 0 to clear flag, write 1 has no effect Read: ● 0b0: No reset occurred ● 0b1: Reset occurred	RW

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4.6.12 Peripheral Module Clock Control Register 0 (PERI_CLKEN0)

Offset	Bit Position																													
0x20	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x80800000																															
Name	FLASH	Reserved	DMA	GPIO	AES	CRC	Reserved	TICK	Reserved	LCD	TRIM	RTC	PCNT	TRNG	VC	ADC	WDT	PCA	OPA	Reserved	TIM3	ADVTIM	LPTIM0	BASETIM	SPI1	SPI0	I2C1	I2C0	LPUART1	LPUART0	UART1	UART0
Access	RW		RW	RW	RW	RW		RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31	FLASH	FLASH controller module clock enable After closing, the FLASH configuration registers cannot be written, and the programs in the FLASH can still run. ● 0b0: Disable ● 0b1: Enable	RW
30	*Reserved*	-	-
29	DMA	DMAC module clock enable ● 0b0: Disable ● 0b1: Enable	RW
28	GPIO	GPIO module clock enable ● 0b0: Disable ● 0b1: Enable	RW
27	AES	AES module clock enable ● 0b0: Disable ● 0b1: Enable	RW
26	CRC	CRC module clock enable ● 0b0: Disable ● 0b1: Enable	RW
25	*Reserved*	-	-
24	TICK	SysTick timer reference clock enable ● 0b0: Disable ● 0b1: Enable	RW
23	*Reserved*	-	-
22	LCD	LCD module clock enable ● 0b0: Disable ● 0b1: Enable	RW
21	TRIM	CLKTRIM module clock enable ● 0b0: Disable ● 0b1: Enable	RW

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Bit	Name	Functional Description	Access
20	RTC	RTC module clock enable ● 0b0: Disable ● 0b1: Enable	RW
19	PCNT	PCNT module clock enable ● 0b0: Disable ● 0b1: Enable	RW
18	TRNG	TRNG module clock enable ● 0b0: Disable ● 0b1: Enable	RW
17	VC	VC, LVD module clock enable ● 0b0: Disable ● 0b1: Enable	RW
16	ADC	ADC, BGR module clock enable ● 0b0: Disable ● 0b1: Enable	RW
15	WDT	WDT module clock enable ● 0b0: Disable ● 0b1: Enable	RW
14	PCA	PCA module clock enable ● 0b0: Disable ● 0b1: Enable	RW
13	OPA	OPA module clock enable ● 0b0: Disable ● 0b1: Enable	RW
12	*Reserved*	-	-
11	TIM3	TIM3 module clock enable ● 0b0: Disable ● 0b1: Enable	RW
10	ADVTIM	TIM4/5/6 module clock enable ● 0b0: Disable ● 0b1: Enable	RW
9	LPTIM0	LPTIM0 module clock enable ● 0b0: Disable ● 0b1: Enable	RW
8	BASETIM	TIM0/1/2 module clock enable ● 0b0: Disable ● 0b1: Enable	RW
7	SPI1	SPI1 module clock enable ● 0b0: Disable ● 0b1: Enable	RW

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Bit	Name	Functional Description	Access
6	SPI0	SPI0 module clock enable ● 0b0: Disable ● 0b1: Enable	RW
5	I2C1	I2C1 module clock enable ● 0b0: Disable ● 0b1: Enable	RW
4	I2C0	I2C0 module clock enable ● 0b0: Disable ● 0b1: Enable	RW
3	LPUART1	LPUART1 module clock enable ● 0b0: Disable ● 0b1: Enable	RW
2	LPUART0	LPUART0 module clock enable ● 0b0: Disable ● 0b1: Enable	RW
1	UART1	UART1 module clock enable ● 0b0: Disable ● 0b1: Enable	RW
0	UART0	UART0 module clock enable ● 0b0: Disable ● 0b1: Enable	RW

Note

The above peripherals must have their corresponding control bits set to enable before use.

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4.6.13 Peripheral Module Clock Control Register 1 (PERI_CLKEN1)

Offset	Bit Position																													
0x24	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																					WWDT	UART3	UART2	Reserved			LPTIM1	DAC	CTRIM	Reserved	
Access																						RW	RW	RW				RW	RW	RW		

Bit	Name	Functional Description	Access
31:11	*Reserved*	-	-
10	WWDT	WWDT module clock enable ● 0b0: Disable ● 0b1: Enable	RW
9	UART3	UART3 module clock enable ● 0b0: Disable ● 0b1: Enable	RW
8	UART2	UART2 module clock enable ● 0b0: Disable ● 0b1: Enable	RW
7:5	*Reserved*	-	-
4	LPTIM1	LPTIM1 module clock enable ● 0b0: Disable ● 0b1: Enable	RW
3	DAC	DAC module clock enable ● 0b0: Disable ● 0b1: Enable	RW
2	CTRIM	CTRIM module clock enable ● 0b0: Disable ● 0b1: Enable	RW
1:0	*Reserved*	-	-

Note

The above peripherals must have their corresponding control bits set to enable before use.

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4.6.14 Peripheral Module Reset Control Register 0 (PERI_RESET0)

Offset	Bit Position																													
0x28	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x7F7F6FFF																															
Name	Reserved		DMA	GPIO	AES	CRC	Reserved			LCD	TRIM	RTC	PCNT	TRNG	VC	ADC	Reserved	PCA	OPA	Reserved	TIM3	ADVTIM	LPTIM0	BASETIM	SPI1	SPI0	I2C1	I2C0	LPUART1	LPUART0	UART1	UART0
Access			RW	RW	RW	RW				RW	RW	RW	RW	RW	RW	RW		RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:30	*Reserved*	-	-
29	DMA	DMAC module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
28	GPIO	GPIO module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
27	AES	AES module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
26	CRC	CRC module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
25:23	*Reserved*	-	-
22	LCD	LCD module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
21	TRIM	CLKTRIM module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
20	RTC	RTC module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
19	PCNT	PCNT module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
18	TRNG	TRNG module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW

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Bit	Name	Functional Description	Access
17	VC	VC module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
16	ADC	ADC, BGR module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
15	*Reserved*	-	-
14	PCA	PCA module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
13	OPA	OPA module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
12	*Reserved*	-	-
11	TIM3	TIM3 module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
10	ADVTIM	TIM456 module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
9	LPTIM0	LPTIM0 module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
8	BASETIM	TIM0/1/2 module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
7	SPI1	SPI1 module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
6	SPI0	SPI0 module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
5	I2C1	I2C1 module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
4	I2C0	I2C0 module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
3	LPUART1	LPUART1 module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW

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Bit	Name	Functional Description	Access
2	LPUART0	LPUART0 module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
1	UART1	UART1 module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
0	UART0	UART0 module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW

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4.6.15 Peripheral Module Reset Control Register 1 (PERI_RESET1)

Offset	Bit Position																													
0x2C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000071C																															
Name	Reserved																					WWDT	UART3	UART2	Reserved			LPTIM1	DAC	CTRIM	Reserved	
Access																						RW	RW	RW				RW	RW	RW		

Bit	Name	Functional Description	Access
31:11	*Reserved*	-	-
10	WWDT	WWDT module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
9	UART3	UART3 module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
8	UART2	UART2 module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
7:5	*Reserved*	-	-
4	LPTIM1	LPTIM1 module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
3	DAC	DAC module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
2	CTRIM	CTRIM module reset enable ● 0b0: In reset state ● 0b1: Normal working status	RW
1:0	*Reserved*	-	-

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4.6.16 Peripheral Debug Function Enable Register (DEBUG_ACTIVE)

Note

This register setting is effective only in SWD debug mode.

Offset	Bit Position																													
0x38	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00003FFF																															
Name	Reserved																		WWDT	LPTIM1	TIM3	Reserved	RTC	WDT	PCA	TIM6	TIM5	TIM4	LPTIM0	TIM2	TIM1	TIM0
Access																			RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:14	*Reserved*	-	-
13	WWDT	WWDT counting function configuration in SWD debug interface ● 0b0: Normal counting ● 0b1: Stop counting	RW
12	LPTIM1	Configuration of LpTimer1 counting function under SWD debug interface ● 0b0: Normal counting ● 0b1: Stop counting	RW
11	TIM3	Configuration of Timer3 counting function under SWD debug interface ● 0b0: Normal counting ● 0b1: Stop counting	RW
10	*Reserved*	-	-
9	RTC	Configuration of RTC counting function under SWD debug interface ● 0b0: Normal counting ● 0b1: Stop counting	RW
8	WDT	Configuration of WDT counting function under SWD debug interface ● 0b0: Normal counting ● 0b1: Stop counting	RW
7	PCA	Configuration of PCA counting function under SWD debug interface ● 0b0: Normal counting ● 0b1: Stop counting	RW
6	TIM6	Configuration of Timer6 counting function under SWD debug interface ● 0b0: Normal counting ● 0b1: Stop counting	RW

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Bit	Name	Functional Description	Access
5	TIM5	Configuration of Timer5 counting function under SWD debug interface ● 0b0: Normal counting ● 0b1: Stop counting	RW
4	TIM4	Configuration of Timer4 counting function under SWD debug interface ● 0b0: Normal counting ● 0b1: Stop counting	RW
3	LPTIM0	Configuration of LPTIM0 counting function under SWD debug interface ● 0b0: Normal counting ● 0b1: Stop counting	RW
2	TIM2	Configuration of Timer2 counting function under SWD debug interface ● 0b0: Normal counting ● 0b1: Stop counting	RW
1	TIM1	Configuration of Timer1 counting function under SWD debug interface ● 0b0: Normal counting ● 0b1: Stop counting	RW
0	TIM0	Configuration of Timer0 counting function under SWD debug interface ● 0b0: Normal counting ● 0b1: Stop counting	RW

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5 NVIC

5.1 Introduction

The Cortex-M0+ processor is internally equipped with a Nested Vector Interrupt Controller (NVIC), which supports up to 32 Interrupt Request (IRQ) inputs and 1 Non Maskable Interrupt (NMI) input (not used in this system). Meanwhile, the processor supports multiple internal exceptions.

Each exception source has a separate exception number, each exception type is assigned a corresponding priority. Some exception priorities are fixed, while others are programmable, as detailed in the table below.

Table 5-1 Cortex-M0+ Processor Interrupt List

Exception Number	Exception Type	Priority	Description
1	Reset	-3 (highest)	Reset
2	NMI	-2	Non-maskable interrupt (not used in this system)
3	Hardware error	-1	Error handling exception
4-10	Reserved	-	-
11	SVC	Programmable	Invoke the hypervisor through the SVC command
12-13	Reserved	-	-
14	PendSV	Programmable	Pendable requests for system services
15	SysTick	Programmable	SysTick timer
16	Interrupt #0	Programmable	External interrupt #0
17	Interrupt #1	Programmable	External interrupt #1
...	...	...	...
47	Interrupt #31	Programmable	External interrupt #31

This chapter only introduces the processor's 32 external interrupt requests (interrupt #0-interrupt #31). For internal exceptions, see the relevant core documentation and reference guides. In addition, this chapter only discusses the interrupt handling mechanism of the NVIC in the processor core, and does not address the interrupt generation mechanisms of peripheral modules.

5.2 Functional Description

5.2.1 Interrupt Priority

Each external interrupt corresponds to a priority register, each priority is 2 bits wide, and uses the highest two bits of the interrupt priority register, and each register occupies 1 byte (8 bits). Under this setting, the available priorities are 0x00 (highest), 0x40, 0x80 and 0xC0 (lowest).

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Used		Not used, read as 0					

When multiple interrupts occur during processor execution:

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- Preemption occurs if the processor is servicing an interrupt and a higher-priority interrupt is triggered. The running interrupt processing will be pended and the new interrupt will be executed instead. This process is usually called interrupt nesting. After the new interrupt is executed, the previous interrupt processing will continue and return to the program thread after it finishes.
- If the priority of the currently executing interrupt is higher than or equal to that of the new interrupt, the new interrupt will wait and enter the pending state. Once the current interrupt handler completes execution, the processor resumes by servicing the pending interrupt.
- If two interrupts occur at the same time and they have the same priority, the interrupt with the lower interrupt number will be serviced first. For example, if interrupt #0 and interrupt #1 are both enabled, have the same priority, and are triggered at the same time, interrupt #0 will be serviced first.

5.2.2 Interrupt Digraph

When the Cortex-M0+ processor is about to handle an interrupt service request, it must first determine the starting address of the exception handler. The required information is called the vector table, as illustrated in the figure below. The vector table is stored at the beginning of the memory space and contains the exception (interrupt) vectors of the exceptions (interrupts) available in the system, as well as the initial value of the main stack pointer (MSP).

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Memory address		Exception number
0x000000BC	Interrupt vector #31	47
...	...	...
0x0000004C	Interrupt vector #3	19
0x00000048	Interrupt vector #2	18
0x00000044	Interrupt vector #1	17
0x00000040	Interrupt vector #0	16
0x0000003C	SysTick vector	15
0x00000038	PendSV vector	14
0x00000034	Reserved	13
0x00000030	Reserved	12
0x0000002C	SVC vector	11
0x00000028	Reserved	10
0x00000024	Reserved	9
0x00000020	Reserved	8
0x0000001C	Reserved	7
0x00000018	Reserved	6
0x00000014	Reserved	5
0x00000010	Reserved	4
0x0000000C	Hardware Fault Exception	3
0x00000008	NMI vector	2
0x00000004	Reset vector	1
0x00000000	Initial Value of MSP	0

Figure 5-1 Interrupt Vector Table

The storage order of the interrupt vector is consistent with the interrupt number. Since each vector is 1 word (4 bytes), the address of the interrupt vector is the interrupt number multiplied by 4, and each interrupt vector is the starting address of the interrupt processing.

5.2.3 Interrupt Input and Pending Behavior

In the NVIC module of the Cortex-M0+ processor, each interrupt input corresponds to a pending state register, and each register has only 1 bit, which is used to save the interrupt request, regardless of whether the request has been confirmed. When the processor starts servicing the interrupt, the hardware will automatically clear the pending status bit.

The peripherals of this system use level-triggered interrupt output. When an interrupt event occurs, the interrupt signal will be confirmed because the peripheral is connected to the NVIC. This signal remains high until the processor executes the interrupt service and clears the peripheral's interrupt signal. Inside the NVIC, when an interrupt is detected, the pending state of the interrupt will be set, and when the

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processor receives the interrupt and starts executing the interrupt service routine, the pending state will be cleared. The handling process is illustrated in the following figure:

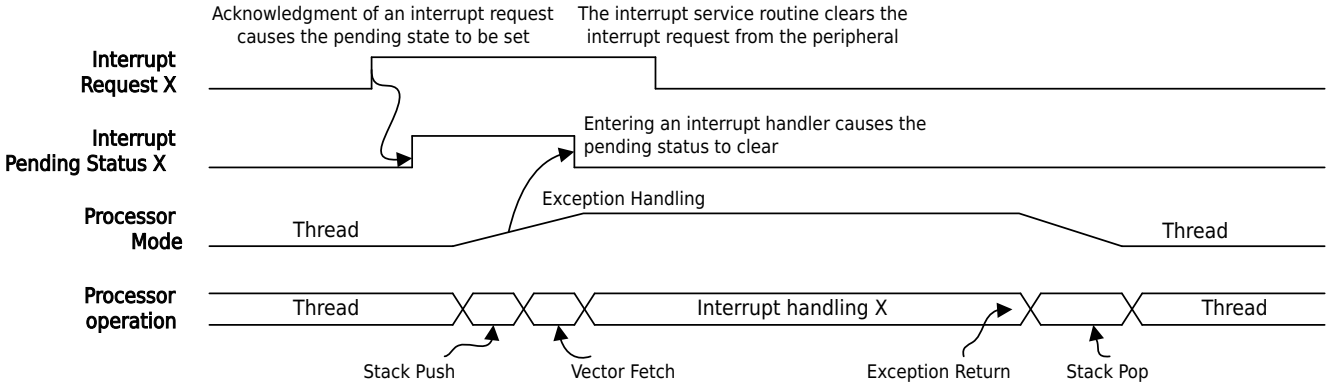

Figure 5-2 Interrupt Active and Pending States

If the interrupt request is not executed immediately and is cleared by software before being acknowledged, the processor will ignore the request and does not perform interrupt processing. When configuring a peripheral, the pending interrupt state can be cleared by writing to the NVIC_ICPR register, thereby removing any interrupt requests generated by the peripheral prior to its configuration.

If the peripheral is still holding an interrupt request when software clears the pending state, the pending state is also generated immediately. The handling process is illustrated in the following figure:

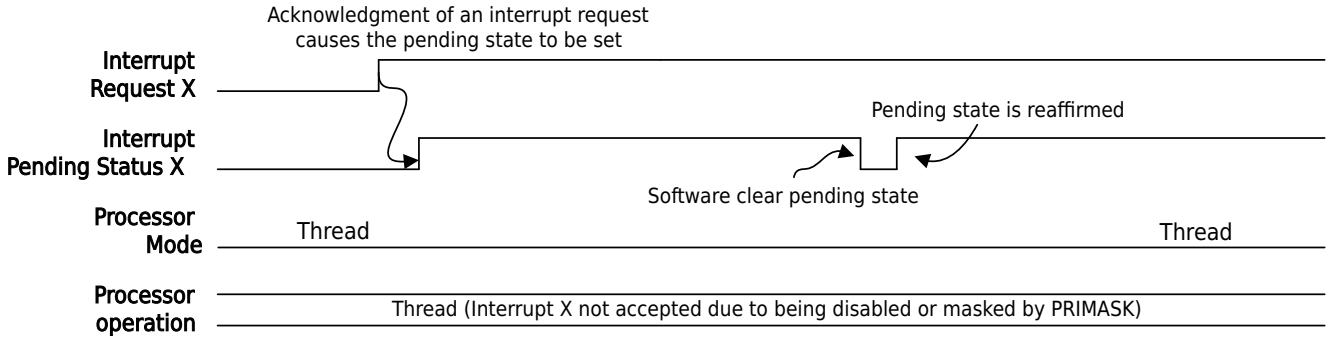

Figure 5-3 Interrupt Pending State is Cleared and Then Reasserted

If the interrupt request generated by the peripheral is not cleared when the exception is handled, the pending state will be activated again after the exception returns, so that the interrupt service routine will be executed again. The handling process is illustrated in the following figure:

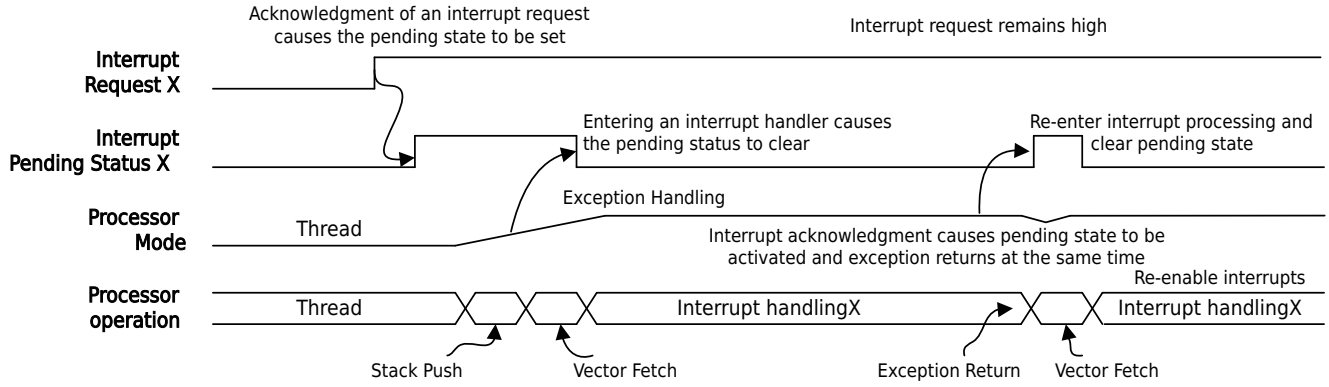

Figure 5-4 When the Interrupt Exits, If the Interrupt Request Remains High, It Will Cause the Interrupt Processing to Be Executed Again

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If a peripheral interrupt request occurs during the execution of the interrupt service routine, the request will be regarded as a new interrupt request, and after this interrupt exits, the interrupt service program will be executed again. The handling process is illustrated in the following figure:

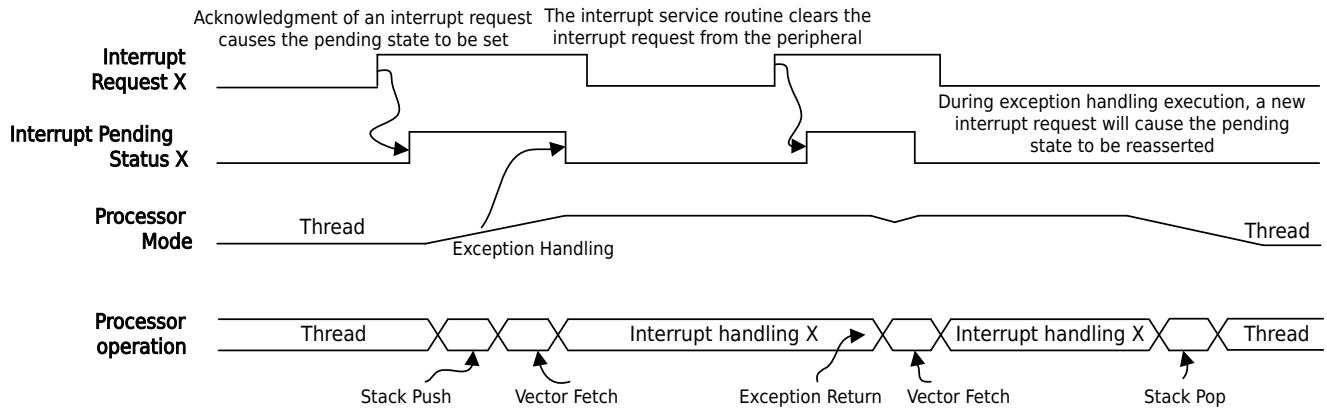

Figure 5-5 Interrupt Pending Interrupts Generated During Interrupt Processing Can Also Be Acknowledged

5.2.4 Interrupt Waiting

Typically, the interrupt waiting of the NVIC is 16 cycles. This wait time starts from the processor clock cycle when the interrupt is acknowledged, and ends when the interrupt handler starts executing. Computing interrupt waiting requires the following prerequisites:

- The interrupt is enabled and not masked by PRIMASK or any other currently executing exception handler.
- The memory system does not have any wait states. Bus transfers are used for interrupt processing, stack push, vector fetches, or instruction fetches at the start of interrupt processing. If the memory system needs to wait, the wait states generated when bus transfers occur may delay interrupts.

The following situations may cause different interrupt waiting:

- The end of the interrupt is chained. If another interrupt request is generated when the interrupt returns, the processor will skip the process of popping and pushing the stack, thus reducing the interrupt waiting time.
- Delayed arrival. If an interrupt occurs, another low-priority interrupt is being pushed to the stack. Due to the existence of the delayed arrival mechanism, the high-priority interrupt will be executed first, which will also reduce the waiting time of the high-priority interrupt.

5.2.5 Interrupt Source

Because the NVIC of the Cortex-M0+ processor supports up to 32 external interrupts, and in this system, there are more than 32 external interrupt sources, some external interrupts are multiplexed on the same NVIC interrupt input, and NMI (Non-Maskable Interrupt) did not use. The corresponding relationship between all external interrupt sources of this system and NVIC interrupt input is shown in the following table:

NVIC Interrupt Input	External Interrupt Source	Active Mode	Sleep mode	DeepSleep mode
Interrupt #0	PORTA	✓	✓	✓
Interrupt #1	PORTB	✓	✓	✓
Interrupt #2	PORTC/E	✓	✓	✓

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NVIC Interrupt Input	External Interrupt Source	Active Mode	Sleep mode	DeepSleep mode
Interrupt #3	PORTD/F	✓	✓	✓
Interrupt #4	DMAC	✓	✓	×
Interrupt #5	TIM3	✓	✓	×
Interrupt #6	UART0/2	✓	✓	×
Interrupt #7	UART1/3	✓	✓	×
Interrupt #8	LPUART0	✓	✓	✓
Interrupt #9	LPUART1	✓	✓	✓
Interrupt #10	SPI0	✓	✓	×
Interrupt #11	SPI1	✓	✓	×
Interrupt #12	I2C0	✓	✓	×
Interrupt #13	I2C1	✓	✓	×
Interrupt #14	TIM0	✓	✓	×
Interrupt #15	TIM1	✓	✓	×
Interrupt #16	TIM2	✓	✓	×
Interrupt #17	LPTIM0/1	✓	✓	✓
Interrupt #18	TIM4	✓	✓	×
Interrupt #19	TIM5	✓	✓	×
Interrupt #20	TIM6	✓	✓	×
Interrupt #21	PCA/WWDT	✓	✓	×
Interrupt #22	WDT	✓	✓	✓
Interrupt #23	RTC	✓	✓	✓
Interrupt #24	ADC/DAC	✓	✓	×
Interrupt #25	PCNT	✓	✓	✓
Interrupt #26	VC0	✓	✓	✓
Interrupt #27	VC1/2	✓	✓	✓
Interrupt #28	LVD	✓	✓	✓
Interrupt #29	LCD	✓	✓	✓
Interrupt #30	FLASH/RAM	✓	✓	×
Interrupt #31	CLKTRIM/CTRIM	✓	✓	✓

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Notice

1. Since some module interrupts are multiplexed for the same IRQ interrupt source, when the CPU enters the interrupt operation, it must first determine which module generated the interrupt, and then perform the corresponding interrupt operation.

5.2.6 Interrupt Structure Diagram

The interrupt structure diagram of this system is shown in the block diagram below. Please note the following:

- The respective interrupt enables of the peripheral interrupt sources are not marked in the figure, and only the logic block diagram of the interrupt signal after the peripheral interrupt is generated is included here.
- IRQ has more than one peripheral interrupt input multiplexing, and the interrupt flag bits of these peripherals must be read separately to determine which peripheral interrupt it is.
- If a peripheral interrupt source is asserted with a high-level signal, the corresponding bit in the NVIC interrupt pending state set register (NVIC_ISPR) will be set regardless of whether the interrupt is enabled in the NVIC interrupt enable set register (NVIC_ISER), indicating that an interrupt has been generated by the peripheral.
- Only when the interrupt enable register NVIC_ISER is set, the corresponding interrupt IRQ will respond to the processor and execute the corresponding interrupt program.
- In the interrupt program, the high-level interrupt signal of the peripheral interrupt source must be cleared, and the interrupt pending register NVIC_ISPR is automatically cleared by the hardware.
- The interrupt priority registers NVIC_IPR0-NVIC_IPR7 set the priority of 32 interrupt sources, 0b00 has the highest priority, and 0b11 has the lowest priority. When the priority is the same, the priority is determined by the interrupt number, and the smaller the number, the higher the priority.

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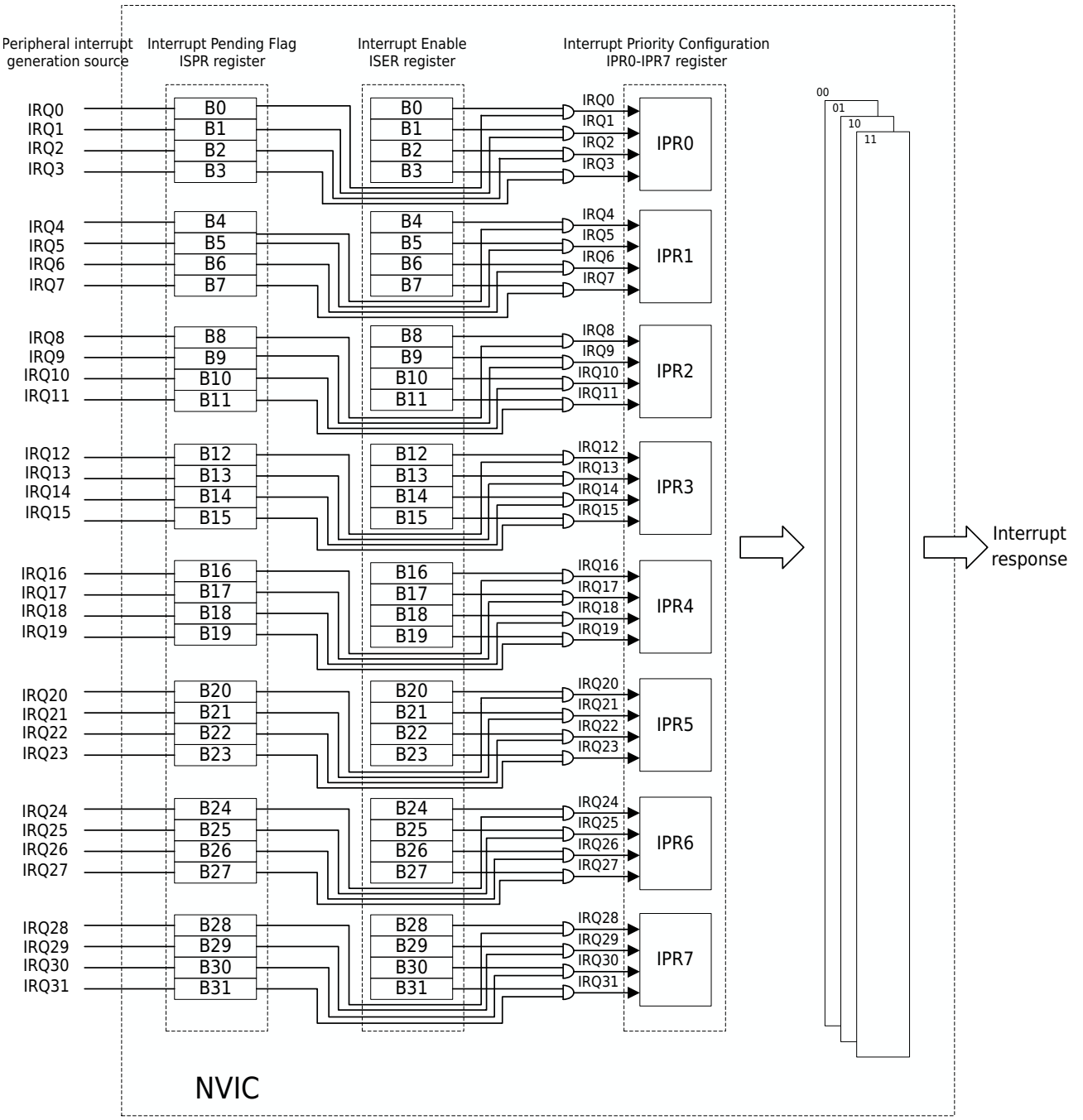

Figure 5-6 Interrupt Structure Diagram

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5.3 Operation Example

5.3.1 External Interrupt Enable

Each peripheral module has its own interrupt enable register. When an interrupt operation is required, the peripheral's own interrupt enable must be enabled first. The operation of this enable bit is not discussed in this chapter, please refer to the chapter descriptions of the corresponding peripheral modules.

5.3.2 NVIC Interrupt Enable and Clear Enable

The Cortex-M0+ processor supports up to 32 interrupt sources, and each interrupt source corresponds to an interrupt enable bit and a clear-enable bit, forming a 32-bit interrupt enable set register (NVIC_ISER) and a 32-bit interrupt enable clear register (NVIC_ICER). If you want to enable a particular interrupt, set the corresponding bit in the NVIC_ISER register to 1. If you want to clear a particular interrupt, set the corresponding bit in the NVIC_ICER register to 1.

The interrupt enable and clear-enable operations mentioned here apply only to the NVIC processor. Whether an interrupt is generated by each peripheral is determined by the peripheral's own interrupt control registers and is unrelated to NVIC_ISER and NVIC_ICER.

5.3.3 NVIC Interrupt Pending and Clear Pending

If an interrupt occurs but cannot be handled immediately, the interrupt request will be pending. The pending state is kept in a register and will remain valid as long as the processor's current priority has not been lowered enough to handle the pending request and the pending state has not been cleared manually.

When the processor starts to enter the interrupt service, the hardware will automatically cause the clearing of the pending state.

You can access or modify the interrupt pending state by manipulating the interrupt pending state set rigister (NVIC_ISPR) and interrupt pending state clear register (NVIC_ICPR). The interrupt pending state register allows software to trigger interrupts.

5.3.4 NVIC Interrupt Priority

Setting the NVIC_IPR0-NVIC_IPR7 registers determines the priority of IRQ0-IRQ31. The programming of the interrupt priority register should be done before the interrupt is enabled, which is usually done at the beginning of the program. Changing the interrupt priority after the interrupt is enabled should be avoided, the results of this situation are unpredictable and are not supported by the Cortex-M0+ processor.

5.3.5 NVIC Interrupt Mask

Some time-sensitive applications need to disable all interrupts in a short period of time, which can be realized by using the interrupt mask register PRIMASK. Only 1 bit of the special register PRIMASK is valid, and it defaults to 0 after reset. When this register is 0, all interrupts and exceptions are enabled; when set to 1, only NMI (not supported by this system) and hardware error exceptions are enabled. In fact, when PRIMASK is set to 1, the current priority of the processor is reduced to 0 (highest programmable priority).

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PRIMASK register can be programmed in a variety of ways. Using assembly language, the MSR instruction can be used to set and clear the PRIMASK register. If using C language and CMSIS device driver library, users can use the following functions to set and clear PRIMASK.

```
void_enable_irq(void);  //Clear PRIMASK
void_disable_irq(void); //Set PRIMASK
```


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5.4 Register Description

5.4.1 Register List

Base address: 0xE000E000

Table 5-4 Interrupt Controller (NVIC) Register Offset Address

Offset	Register	Description	Width
0x100	NVIC_ISER	Interrupt Enable Set Register	32
0x180	NVIC_ICER	Interrupt Enable Clear Register	32
0x200	NVIC_ISPR	Interrupt Pending State Set Register	32
0x280	NVIC_ICPR	Interrupt Pending State Clear Register	32
0x400	NVIC_IPR0	Interrupt #0- Interrupt #3 Priority Registers	32
0x404	NVIC_IPR1	Interrupt #4- Interrupt #7 Priority Registers	32
0x408	NVIC_IPR2	Interrupt #8- Interrupt #11 Priority Registers	32
0x40C	NVIC_IPR3	Interrupt #12- Interrupt #15 Priority Registers	32
0x410	NVIC_IPR4	Interrupt #16- Interrupt #19 Priority Registers	32
0x414	NVIC_IPR5	Interrupt #20- Interrupt #23 Priority Registers	32
0x418	NVIC_IPR6	Interrupt #24- Interrupt #27 Priority Registers	32
0x41C	NVIC_IPR7	Interrupt #28- Interrupt #31 Priority Registers	32
-	PRIMASK	Interrupt Mask Special Register	32

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5.4.2 Interrupt Enable Set Register (NVIC_ISER)

Offset	Bit Position																													
0x100	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	SETENA																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	SETENA	Interrupt Enable Set Flag Set enable interrupt #0 to interrupt #31 ● bit 0: IRQ0 ● bit 1: IRQ1 ● bit 2: IRQ2 ● ... ● bit 31: IRQ31 **Note** Each bit: writing 1 is set, writing 0 has no effect.	RW

5.4.3 Interrupt Enable Clear Register (NVIC_ICER)

Offset	Bit Position																													
0x180	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	CLRENA																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	CLRENA	Interrupt Clear-Enable Clear-enable interrupt #0 to interrupt #31 ● bit 0: IRQ0 ● bit 1: IRQ1 ● bit 2: IRQ2 ● ... ● bit 31: IRQ31 **Note** Each bit: write 1 to clear flag, write 0 has no effect. .	RW

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5.4.4 Interrupt Pending State Set Register (NVIC_ISPR)

Offset	Bit Position																													
0x200	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	SETPEND																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	SETPEND	Interrupt Pending State Set Flag Set the pending state of interrupt #0 to interrupt #31 ● bit 0: IRQ0 ● bit 1: IRQ1 ● bit 2: IRQ2 ● ... ● bit 31: IRQ31 **Note** Each bit: write 1 is set, writing 0 has no effect.	RW

5.4.5 Interrupt Pending State Clear Register (NVIC_ICPR)

Offset	Bit Position																													
0x280	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	CLRPEND																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	CLRPEND	Interrupt Pending State Clear Clear the pending state of interrupt #0 to interrupt #31 ● bit 0: IRQ0 ● bit 1: IRQ1 ● bit 2: IRQ2 ● ... ● bit 31: IRQ31 **Note** Each bit: write 1 to clear flag, write 0 has no effect.	RW

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5.4.6 Interrupt Priority Register (NVIC_IPR0)

Offset	Bit Position																													
0x400	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	IPR0																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	IPR0	Priority of Interrupt #0 to Interrupt #3 The corresponding bits for each interrupt priority are as follows: ● [31:30]: Priority of interrupt #3 ● [23:22]: Priority of interrupt #2 ● [15:14]: Priority of interrupt #1 ● [7:6]: Priority of interrupt #0 In the above configuration, a setting of 0b00 indicates the highest priority, whereas 0b11 indicates the lowest priority. Since the other bits are unused, configuring them has no effect and read always returns 0.	RW

5.4.7 Interrupt Priority Register (NVIC_IPR1)

Offset	Bit Position																													
0x404	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	IPR1																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	IPR1	Priority of Interrupt #4 to Interrupt #7 The corresponding bits for each interrupt priority are as follows: ● [31:30]: Priority of interrupt #7 ● [23:22]: Priority of interrupt #6 ● [15:14]: Priority of interrupt #5 ● [7:6]: Priority of interrupt #4 In the above configuration, a setting of 0b00 indicates the highest priority, whereas 0b11 indicates the lowest priority. Since the other bits are unused, configuring them has no effect and read always returns 0.	RW

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5.4.8 Interrupt Priority Register (NVIC_IPR2)

Offset	Bit Position																													
0x408	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	IPR2																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	IPR2	Priority of Interrupt #8 to Interrupt #11 The corresponding bits for each interrupt priority are as follows: ● [31:30]: Priority of interrupt #11 ● [23:22]: Priority of interrupt #10 ● [15:14]: Priority of interrupt #9 ● [7:6]: Priority of interrupt #8 In the above configuration, a setting of 0b00 indicates the highest priority, whereas 0b11 indicates the lowest priority. Since the other bits are unused, configuring them has no effect and read always returns 0.	RW

5.4.9 Interrupt Priority Register (NVIC_IPR3)

Offset	Bit Position																													
0x40C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	IPR3																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	IPR3	Priority of Interrupt #12 to Interrupt #15 The corresponding bits for each interrupt priority are as follows: ● [31:30]: Priority of interrupt #15 ● [23:22]: Priority of interrupt #14 ● [15:14]: Priority of interrupt #13 ● [7:6]: Priority of interrupt #12 In the above configuration, a setting of 0b00 indicates the highest priority, whereas 0b11 indicates the lowest priority. Since the other bits are unused, configuring them has no effect and read always returns 0.	RW

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5.4.10 Interrupt Priority Register (NVIC_IPR4)

Offset	Bit Position																													
0x410	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	IPR4																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	IPR4	Priority of Interrupt #16 to Interrupt #19 The corresponding bits for each interrupt priority are as follows: ● [31:30]: Priority of interrupt #19 ● [23:22]: Priority of interrupt #18 ● [15:14]: Priority of interrupt #17 ● [7:6]: Priority of interrupt #16 In the above configuration, a setting of 0b00 indicates the highest priority, whereas 0b11 indicates the lowest priority. Since the other bits are unused, configuring them has no effect and read always returns 0.	RW

5.4.11 Interrupt Priority Register (NVIC_IPR5)

Offset	Bit Position																													
0x414	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	IPR5																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	IPR5	Priority of Interrupt #20 to Interrupt #23 The corresponding bits for each interrupt priority are as follows: ● [31:30]: Priority of interrupt #23 ● [23:22]: Priority of interrupt #22 ● [15:14]: Priority of interrupt #21 ● [7:6]: Priority of interrupt #20 In the above configuration, a setting of 0b00 indicates the highest priority, whereas 0b11 indicates the lowest priority. Since the other bits are unused, configuring them has no effect and read always returns 0.	RW

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5.4.12 Interrupt Priority Register (NVIC_IPR6)

Offset	Bit Position																													
0x418	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	IPR6																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	IPR6	Priority of Interrupt #24 to Interrupt #27 The corresponding bits for each interrupt priority are as follows: ● [31:30]: Priority of interrupt #27 ● [23:22]: Priority of interrupt #26 ● [15:14]: Priority of interrupt #25 ● [7:6]: Priority of interrupt #24 In the above configuration, a setting of 0b00 indicates the highest priority, whereas 0b11 indicates the lowest priority. Since the other bits are unused, configuring them has no effect and read always returns 0.	RW

5.4.13 Interrupt Priority Register (NVIC_IPR7)

Offset	Bit Position																													
0x41C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	IPR7																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	IPR7	Priority of Interrupt #28 to Interrupt #31 The corresponding bits for each interrupt priority are as follows: ● [31:30]: Priority of interrupt #31 ● [23:22]: Priority of interrupt #30 ● [15:14]: Priority of interrupt #29 ● [7:6]: Priority of interrupt #28 In the above configuration, a setting of 0b00 indicates the highest priority, whereas 0b11 indicates the lowest priority. Since the other bits are unused, configuring them has no effect and read always returns 0.	RW

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5.4.14 Interrupt Mask Special Register (PRIMASK)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																															PRIMASK
Access																																RW

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-
0	PRIMASK	Interrupt mask flag Typically used in time-critical application scenarios. The special register can be accessed through MSR and MRS special register operation instructions, and can also be accessed by changing the processor state instruction CPS. ● 0b0: All interrupts and exceptions are in the enabled state. ● 0b1: Only the NMI and hardware error exceptions are enabled.	RW

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6 GPIO

6.1 Introduction

This series supports up to 72 digital general-purpose input/output ports . The input and output signals of the analog module ADC/VC/LVD/LCD, and the input and output signals of various functional modules (such as SPI/UART/I2C/Timer, etc.) can be multiplexed with digital general-purpose input and output ports.

Each port can be configured as internal pull-up/pull-down input, floating input, push-pull output, open-drain output, two levels driving capability output. After the digital port is configured as an analog port, the digital function is isolated, "1" and "0" cannot be output, and the result of reading the port input value register by the CPU is "0".

When each digital port is configured as an input, it can provide an external interrupt. The interrupt type can be configured as high-level trigger, low-level trigger, rising edge trigger, and falling edge trigger. Query the interrupt flag bit of Px_STAT[n] can know the corresponding interrupt trigger port. In addition, each digital port interrupt can wake up the chip from Sleep mode/DeepSleep mode to Active mode.

After the chip is reset, the port is a floating input, the purpose is to prevent abnormal actions on external devices when the chip is abnormally reset. However, in order to avoid the leakage caused by floating input, the user should configure the port accordingly after the chip is started (configured as internal pull-up/pull -down input or output).

6.2 Features

The general-purpose I/O supports the following features:

- Port input value/output value register supports FAST IO/AHB bus read and write
- Other registers support AHB bus interface read and write
- Analog function pins/digital common pins/digital function pins are multiplexed
- Support pull-up/pull-down/two levels driving/open drain output function selection
- Support interrupt in Active mode/Sleep mode/DeepSleep mode
- Support high level/low level/rising edge/falling edge trigger interrupt
- Support bit set, bit clear, bit set clear function

Note

For the introduction of FAST IO, please refer to "ARM Cortex-M0+_IntegrationAndImplementationManual.pdf".

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6.3 Functional Description

6.3.1 Port Configuration Function

Each port can be configured as an analog port or a digital port through the configuration register (**PxADS**) according to system requirements. When PxADS is 1, the port is configured as an analog port, and when PxADS is 0, the port is configured as a digital port.

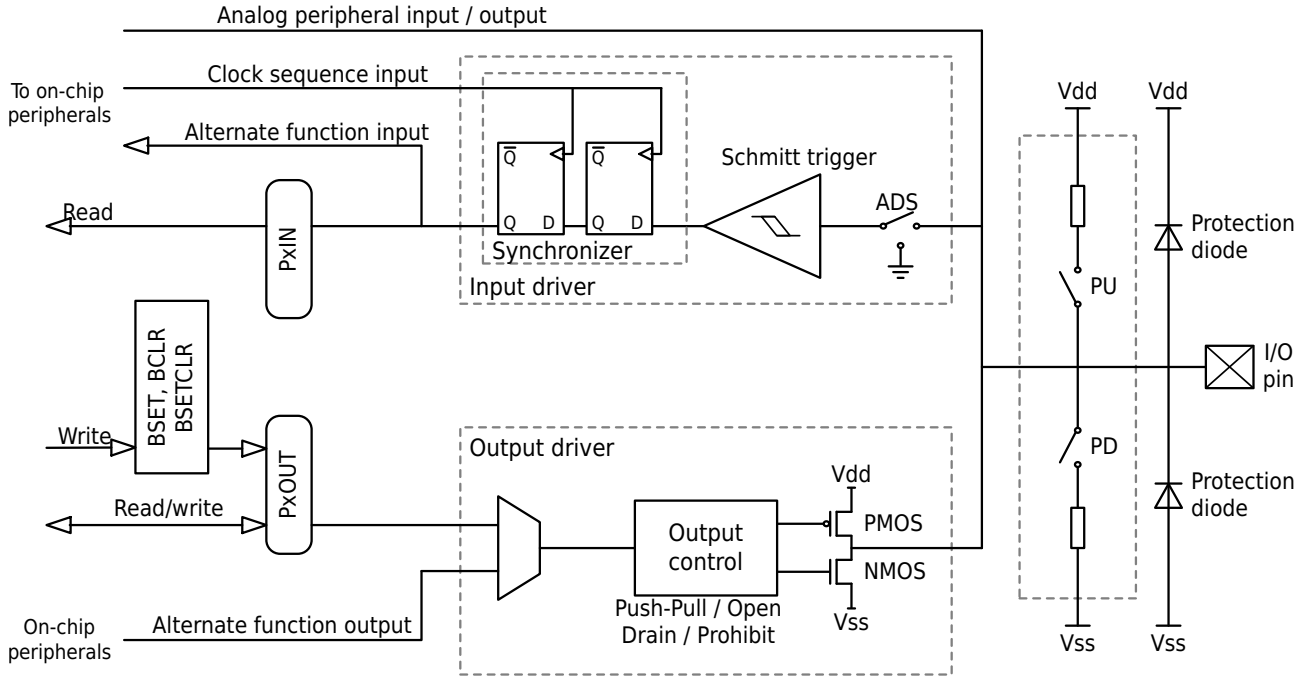

Figure 6-1 Port Circuit Diagram

Note

The output/input data register (PxOUT/PxIN) supports AHB/FAST IO bus access, other registers support AHB bus access.

When the port is configured as a digital port, it can accept digital general-purpose input and output signals (set the Pxy_SEL register to 0), and accept the input and output signals of various functional modules (such as SPI, UART, I2C, Timer, ect.) through the configuration register Pxy_SEL, for details, refer to the port digital multiplexing function module.

The corresponding registers can also be configured to achieve the following features:

- Internal pull-up (PxPU)/pull-down (PxPD)

  The pull-up register (PxPU) and the pull-down register (PxPD) correspond to the port pull-up enable and port pull-down enable respectively. When the corresponding bit is 1, set the corresponding bit pin pull-up/pull-down enable, When it is 0, the pull-up/pull-down of the corresponding bit pin is prohibited.

- Two levels driving output (PxDR)

  The driving capability can be changed through the PxDR register. When PxDR is 1, it is low driving capability, and when PxDR is 0, it is high driving capability.

- Open-drain output (PxOD)

  Set the pin output state through the PxOD register. When PxOD is '1', the port open-drain output is enabled, and when it is '0', the port push-pull output is enabled. When the open-drain pin is not

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connected to an external pull-up resistor, it can only output low level. If it needs to output high level at the same time, a pull-up resistor is required.

- Direction selection (PxDIR)

  Used to set the direction of the port pin. When PxDIR is 0, the port is output, and when PxDIR is 1, the port is input.

- Input level status (PxIN)

  The synchronized pin level can be obtained by reading the PxIN register. When PxIN is 1, the pin is high level, and when PxIN is 0, the pin is low level.

- Output high and low level selection (PxOUT)

  When the port pin is configured as an output, if PxOUT is 1, the port pin output is high level, if PxOUT is 0, the output is low level.

- Bit set (PxBSET), bit cleared (PxBCLR), bit set cleared (PxBSETCLR)

  Bit set and bit cleared are applicable to setting the bit that the user wants to change to obtain the corresponding value without changing the value of other bits. When a bit is set, the corresponding value is set to 1, and when a bit is cleared, the corresponding value is set to 0.

Note

The above features are invalid when configured as an analog port.

The relationship between port states and register configuration is as follows:

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Table 6-1 Port Status Truth Table

IO State	IO Direction	PxADS	PxDIR	PxOUT	PxIN	PxBSET	PxBCLR	PxBSETCLR	PxPU	PxPD	PxOD	PxDR	Pxy_SEL
Simulation	Input/Output	1	W	W	0	W	W	W	W	W	W	W	W
Floating	Input	0	1	W	X	W	W	W	0	0	W	W	0
Pull-down	Input	0	1	W	0	W	W	W	0	1	W	W	0
Pull-up	Input	0	1	W	1	W	W	W	1	0	W	W	0
Pull-up	Input	0	1	W	1	W	W	W	1	1	W	W	0
1	Input	0	1	W	1	W	W	W	W	W	W	W	0
0	Input	0	1	W	0	W	W	W	W	W	W	W	0
1	Output	0	0	1	1	0	0	0	W	W	0	W	0
0	Output	0	0	0	0	0	0	0	W	W	0	W	0
1	Output	0	0	W	1	1	0	0	W	W	0	W	0
0	Output	0	0	W	0	0	1	0	W	W	0	W	0
1 (SET)	Output	0	0	W	1 (SET)	0	0	1	W	W	0	W	0
0 (CLR)	Output	0	0	W	0 (CLR)	0	0	1	W	W	0	W	0
0	Output	0	0	0	0	0	0	0	W	W	1	W	0
Z	Output	0	0	1	X	0	0	0	0	0	1	W	0
0	Output	0	0	1	0	0	0	0	0	1	1	W	0
1	Output	0	0	1	1	0	0	0	1	0	1	W	0
1	Output	0	0	1	1	0	0	0	1	1	1	W	0
0-Logic low, 1-Logic high, W-Whatever 0 or 1, X-unknow state, Z-high impedance													

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6.3.2 Port Write

The port input value/output value register (PxIN/PxOUT) supports reading and writing of the AHB bus and the FAST IO bus (controlled by the register GPIO_CTRL2.AHB_SEL bit), and only supports reading and writing of the AHB bus for other registers. For these two different buses, the system clock (HCLK) has different processing cycles for these two buses. The following two figures show the fastest timing for two bus port flipping:

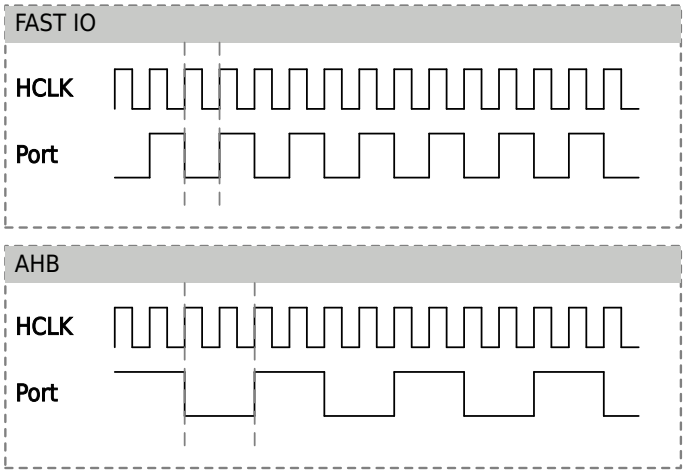

Figure 6-2 AHB/FASTIO Bus Port Changes with System Clock

For the AHB bus, every two HCLK cycles, the IO is flipped once, and for the FAST IO bus, every HCLK cycle, the IO is flipped once.

6.3.3 Port Read

Each port can get the port pin level by reading the PxIN register. As Port Circuit Diagram shown, each bit of the PxIN register and the latch in front of it form a synchronizer to avoid the signal instability caused by the pin level change in a short time when the system clock state changes, but it also introduces delay. The synchronization diagram for reading port pin data is as follows:

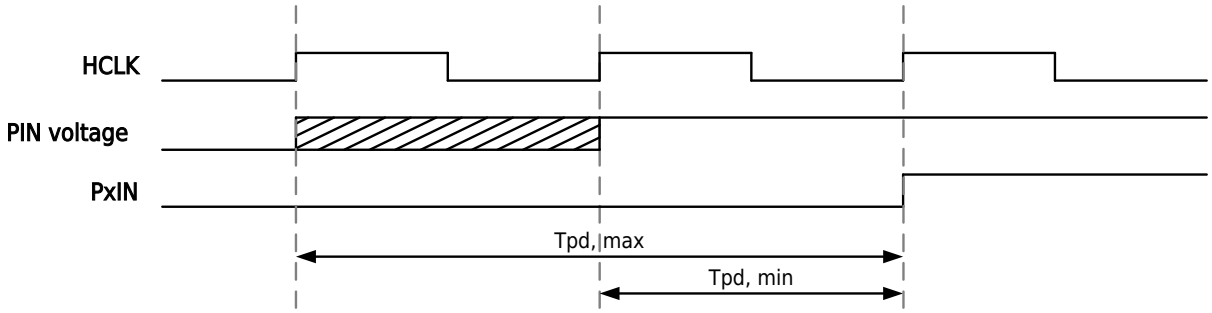

Figure 6-3 Port Pin Data Read Synchronization Diagram

During the clock period after the rising edge of the system clock, the pin level signal will be latched in the internal register, as shown in the shaded part, after the next rising edge of the system clock, the stable pin level signal can be read. Then, when the rising edge of the system clock, the data is latched into the PxIN register. The signal replacement delay Tpd is 1-2 system clocks.

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Note

Handling of unconnected pins: If there are unconnected pins during use, in order to avoid floating current consumption caused by pins not having a certain level in other digital input enable modes, it is recommended to assign a certain level to the pin.

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6.3.4 Port Digital Multiplexing Function

Port digital multiplexing is one of the main functions of the general-purpose I/O. Through the configuration register, the port can be flexibly configured as a digital general-purpose port/digital function port.

The Pxy_SEL register is used for digital general-purpose port/digital function port switching, and each port can be independently configured as a functional port required by the system.

Table 6-2 Port Multiplexing Table

AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA00	UART1_CTS	LPUART1_TXD	TIM0_ETR	VC0_OUT	TIM1_CHA	TIM3_ETR	TIM0_CHA
PA01	UART1_RTS	LPUART1_RXD	TIM0_CHB	TIM1_ETR	TIM1_CHB	HCLK_OUT	SPI1_MOSI
PA02	UART1_TXD	TIM0_CHA	VC1_OUT	TIM1_CHA	TIM2_CHA	PCLK_OUT	SPI1_MISO
PA03	UART1_RXD	TIM0_GATE	TIM1_CHB	TIM2_CHB	SPI1_CS	TIM3_CH1A	TIM5_CHA
PA04	SPI0_CS	UART1_TXD	PCA_CH4	TIM2_ETR	TIM5_CHA	LVD_OUT	TIM3_CH2B
PA05	SPI0_SCK	TIM0_ETR	PCA_ECI	TIM0_CHA	TIM5_CHB	XTL_OUT	XTH_OUT
PA06	SPI0_MISO	PCA_CH0	TIM3_BK	TIM1_CHA	VC0_OUT	TIM3_GATE	LPUART0_CTS
PA07	SPI0_MOSI	PCA_CH1	HCLK_OUT	TIM3_CH0B	TIM2_CHA	VC1_OUT	TIM4_CHB
PA08	UART0_TXD	TIM3_CH0A	CTRIM_ETRTOG	-	TIM1_GATE	TIM4_CHA	TIM3_BK
PA09	UART0_TXD	TIM3_CH1A	TIM0_BK	I2C0_SCL	-	HCLK_OUT	TIM5_CHA
PA10	UART0_RXD	TIM3_CH2A	TIM2_BK	I2C0_SDA	TIM2_GATE	PCLK_OUT	TIM6_CHA
PA11	UART0_CTS	TIM3_GATE	I2C1_SCL	-	VC0_OUT	SPI0_MISO	TIM4_CHB
PA12	UART0_RTS	TIM3_ETR	I2C1_SDA	-	VC1_OUT	SPI0_MOSI	PCNT_S0
PA13	IR_OUT	UART0_RXD	LVD_OUT	TIM3_ETR	RTC_1HZ	PCNT_S1	VC2_OUT
PA14	UART1_TXD	UART0_TXD	TIM3_CH2A	LVD_OUT	RCH_OUT	RCL_OUT	PLL_OUT
PA15	SPI0_CS	UART1_RXD	LPUART1_RTS	TIM0_ETR	TIM0_CHA	TIM3_CH1A	-
PB00	PCA_CH2	TIM3_CH1B	LPUART0_TXD	TIM5_CHB	RCH_OUT	RCL_OUT	PLL_OUT
PB01	PCA_CH3	PCLK_OUT	TIM3_CH2B	TIM6_CHB	LPUART0_RTS	VC2_OUT	TCLK_OUT
PB02	LPTIM0_TOG	PCA_ECI	LPUART1_TXD	TIM4_CHA	TIM1_BK	TIM0_BK	TIM2_BK
PB03	SPI0_SCK	TIM0_CHB	TIM1_GATE	TIM3_CH0A	LPTIM0_GATE	XTL_OUT	XTH_OUT
PB04	SPI0_MISO	PCA_CH0	TIM2_BK	UART0_CTS	TIM2_GATE	TIM3_CH0B	LPTIM0_ETR
PB05	SPI0_MOSI	-	TIM1_BK	PCA_CH1	LPTIM0_GATE	PCNT_S0	UART0_RTS
PB06	I2C0_SCL	UART0_TXD	TIM1_CHB	TIM0_CHA	LPTIM0_ETR	TIM3_CH0A	LPTIM0_TOG

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AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB07	I2C0_SDA	UART0_RXD	TIM2_CHB	LPUART1_CTS	TIM0_CHB	LPTIM0_TOGN	PCNT_S1
PB08	I2C0_SCL	TIM1_CHA	-	TIM2_CHA	TIM0_GATE	TIM3_CH2A	UART0_TXD
PB09	I2C0_SDA	IR_OUT	SPI1_CS	TIM2_CHA	-	TIM2_CHB	UART0_RXD
PB10	I2C1_SCL	SPI1_SCK	TIM1_CHA	LPUART0_TXD	TIM3_CH1A	LPUART1_RTS	UART1_RTS
PB11	I2C1_SDA	TIM1_CHB	LPUART0_RXD	TIM2_GATE	TIM6_CHA	LPUART1_CTS	UART1_CTS
PB12	SPI1_CS	TIM3_BK	LPUART0_TXD	TIM0_BK	-	LPUART0_RTS	TIM6_CHA
PB13	SPI1_SCK	I2C1_SCL	TIM3_CH0B	LPUART0_CTS	TIM1_CHA	TIM1_GATE	TIM6_CHB
PB14	SPI1_MISO	I2C1_SDA	TIM3_CH1B	TIM0_CHA	RTC_1HZ	LPUART0_RTS	TIM1_BK
PB15	SPI1_MOSI	TIM3_CH2B	TIM0_CHB	TIM0_GATE	-	-	LPUART1_RXD
PC00	LPTIM0_GATE	PCNT_S0	UART1_CTS	UART2_RTS	-	-	-
PC01	LPTIM0_TOG	TIM5_CHB	UART1_RTS	PCNT_S0FO	-	UART2_CTS	-
PC02	SPI1_MISO	LPTIM0_TOGN	PCNT_S1	UART2_RXD	-	-	-
PC03	SPI1_MOSI	LPTIM0_ETR	LPTIM0_TOGN	PCNT_S1FO	UART2_TXD	-	-
PC04	LPUART0_TXD	TIM2_ETR	IR_OUT	VC2_OUT	-	-	-
PC05	LPUART0_RXD	TIM6_CHB	PCA_CH4	-	-	-	-
PC06	PCA_CH0	TIM4_CHA	TIM2_CHA	LPTIM1_GATE	-	UART3_RXD	-
PC07	PCA_CH1	TIM5_CHA	TIM2_CHB	LPTIM1_ETR	-	UART3_TXD	-
PC08	PCA_CH2	TIM6_CHA	TIM2_ETR	LPTIM1_TOG	-	UART3_CTS	-
PC09	PCA_CH3	TIM4_CHB	TIM1_ETR	LPTIM1_TOGN	-	UART3_RTS	-
PC10	LPUART1_TXD	LPUART0_TXD	PCA_CH2	-	-	-	-
PC11	LPUART1_RXD	LPUART0_RXD	PCA_CH3	PCNT_S0FO	-	-	-
PC12	LPUART0_TXD	LPUART1_TXD	PCA_CH4	PCNT_S1FO	-	-	-
PC13	-	RTC_1HZ	TIM3_CH1B	-	-	-	-
PC14	-	-	-	-	-	-	-
PC15	-	-	-	-	-	-	-
PD00	-	SPI1_CS	-	-	-	-	-
PD01	-	SPI1_SCK	-	-	-	-	-
PD02	PCA_ECI	LPUART0_RTS	TIM1_ETR	-	-	-	-
PD03	UART1_CTS	SPI1_MISO	LPTIM1_TOG	-	-	-	-
PD04	UART1_RTS	SPI1_MOSI	LPTIM1_TOGN	-	-	-	-
PD08	LPUART0_TXD	-	-	-	-	-	-

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AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD09	LPUART0_RXD	-	-	-	-	-	-
PD10	LPUART0_TXD	-	-	-	-	-	-
PD11	LPUART0_CTS	-	-	-	-	-	-
PE02	PCA_ECI	-	-	-	-	-	-
PE03	PCA_CH0	-	-	-	-	-	-
PE04	PCA_CH1	-	-	-	-	-	-
PE05	PCA_CH2	-	-	-	-	-	-
PE11	TIM3_CH1A	-	-	-	-	-	-
PE12	TIM3_CH2B	SPI0_CS	UART3_CTS	-	-	-	-
PE13	TIM3_CH2A	SPI0_SCK	UART3_RTS	-	-	-	-
PE14	TIM3_CH0B	SPI0_MISO	UART3_RXD	-	-	-	-
PF00	I2C0_SDA	CTRIM_ETRTOG	UART1_TXD	-	-	-	-
PF01	I2C0_SCL	TIM4_CHB	UART1_RXD	-	-	-	-
PF04	-	-	-	-	-	-	-
PF05	-	-	-	-	-	-	-
PF06	I2C1_SCL	LPUART1_CTS	UART0_CTS	-	-	-	-
PF07	I2C1_SDA	LPUART1_RTS	UART0_RTS	-	-	-	-
PF11	-	-	-	-	-	-	-

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6.3.5 Port Interrupt Function

Each digital general-purpose port can be interrupted by an external signal source. The external signal source can be four types of signals: high level/low level/rising edge/falling edge, and the corresponding interrupt enable registers are High Level Interrupts Enable Register (PxHIE)/Low Level Interrupt Enable Register (PxLIE)/Rising Edge Interrupt Enable Register (PxRIE)/Falling Edge Interrupt Enable Register (PxFIE). When an interrupt is triggered, it can be determined which port triggered the interrupt by querying the Interrupt Status Register (Px_STAT), and the corresponding interrupt status flag bit can be cleared by clearing the Interrupt Clear Register (Px_ICLR).

6.4 Operation Example

6.4.1 Port Multiplexing Configured as Analog Port Operation Flow

Procedure

Set the register PxADS[n] to 1.

6.4.2 Port Multiplexing Configured as Digital Universal Port Operation Flow

Procedure

Step1. Set the register PxADS[n] to 0.

Step2. Set the register Pxy_SEL to 0.

Step3. Set the register PxDIR[n] to 1: the port direction is input, and the CPU can read the port status PxIN[n].

Step4. Set the register PxDIR[n] to 0: the port direction is output.

Step5. Set the register PxOUT[n] to 1: the port outputs a high level.

Step6. Set the register PxOUT[n] to 0: the port outputs a low level.

6.4.3 Port Multiplexing Configured as Digital Function Port Operation Flow

Procedure

Step1. Set the register PxADS[n] to 0.

Step2. According to the system requirement, set the register Pxy_SEL to 1-7, for specific configurations,refer to the Port Multiplexing Table.

Step3. According to the system requirement, set the register PxDIR[n].

Step4. According to the system requirement, set the register PxPU[n]/PxPD[n]/PxOD[n].

6.4.4 Port Multiplexing Configured as Debug Test Port Operation Flow

Context

For specific operations, please refer to the relevant introduction in the "SWD Debugging Interface" chapter.

6.4.5 Port Multiplexing Configured as Infrared Output Signal Operation Flow

Context

Ports PA13, PB09, PC04 can modulate the internal clock signal with a frequency of 38.4kHz into infrared signal output.

Note

Carrier output is only generated when operating with the 38.4kHz RCL clock enabled.

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Procedure

Step1. Set register PAADS[13]/PBADS[9]/PCADS[4] to 0.

Step2. Set register PA13_SEL = 1/PB09_SEL = 2/PC04_SEL = 3.

Step3. Set register PADIR[13] = 0/PBDIR[9] = 0/PCDIR[4] = 0, port direction is output.

Step4. Set the register GPIO_CTRL1[14] to select the output polarity of the infrared signal.

Step5. Set register PAOUT[13] = 1/PBOUT[9] = 1/PCOUT[4] = 1, select the gated infrared signal output.

6.4.6 Port High Level Interrupt Operation Flow

Procedure

Step1. Set the register PxADS[n] to 0.

Step2. Set the register Pxy_SEL to 0.

Step3. Set the register PxDIR[n] to 1.

Step4. Set the register PxHIE[n] to 1.

Step5. Read the register Px_STAT[n] after the interrupt is triggered.

Step6. Set the register Px_ICLR[n] to 0 to clear the register Px_STAT[n].

6.4.7 Port Low Level Interrupt Operation Flow

Procedure

Step1. Set the register PxADS[n] to 0.

Step2. Set the register Pxy_SEL to 0.

Step3. Set the register PxDIR[n] to 1.

Step4. Set the register PxLIE[n] to 1.

Step5. Read the register Px_STAT[n] after the interrupt is triggered.

Step6. Set the register Px_ICLR[n] to 0 to clear the register Px_STAT[n].

6.4.8 Port Rising Edge Interrupt Operation Flow

Procedure

Step1. Set the register PxADS[n] to 0.

Step2. Set the register Pxy_SEL to 0.

Step3. Set the register PxDIR[n] to 1.

Step4. Set the register PxRIE[n] to 1.

Step5. Read the register Px_STAT[n] after the interrupt is triggered.

Step6. Set the register Px_ICLR[n] to 0 to clear the register Px_STAT[n].

6.4.9 Port Falling Edge Interrupt Operation Flow

Procedure

Step1. Set the register PxADS[n] to 0.

Step2. Set the register Pxy_SEL to 0.

Step3. Set the register PxDIR[n] to 1.

Step4. Set the register PxFIE[n] to 1.

Step5. Read the register Px_STAT[n] after the interrupt is triggered.

Step6. Set the register Px_ICLR[n] to 0 to clear the register Px_STAT[n].

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6.4.10 Port Pull-Up Enable Configuration Operation Flow

Procedure

Set the register PxPU[n] to 1.

6.4.11 Port Pull-Down Enable Configuration Operation Flow

Context

When PxPU[n] and PxPD[n] are set to 1 at the same time, PxPU[n] has higher priority and PxPD[n] is invalid.

Procedure

Step1. Set the register PxPU[n] to 0.

Step2. Set the register PxPD[n] to 1.

6.4.12 Port Enhancement Driver Configuration Operation Flow

Procedure

Set the register PxDR[n] to 0.

6.4.13 Port Open-Drain Output Configuration Operation Flow

Procedure

Set the register PxOD[n] to 1.

6.4.14 Port Bit Setting Operation Flow

Procedure

Set the register PxBSET[n] to 1.

6.4.15 Port Bit Clearing Operation Flow

Procedure

Set the register PxBCLR[n] to 1.

6.4.16 Port Bit Setting and Clearing Operation Flow

Procedure

Set the register PxBSETCLR[n] to 1.

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6.5 Register Description

6.5.1 Register List

Base address: 0x40020C00

Table 6-3 General-Purpose I/O (GPIO) Register Offset

Offset	Register	Description
0x00+0x4*y	PAy_SEL	Port PAy Function Configuration Register (y=0-15)
0x40+0x4*y	PBy_SEL	Port PBy Function Configuration Register (y=0-15)
0x80+0x4*y	PCy_SEL	Port PCy Function Configuration Register (y=0-15)
0xC0+0x4*y	PDy_SEL	Port PDy Function Configuration Register (y=0-4, 8-11)
0x100	PADIR	Port PA Input/Output Configuration Register
0x104	PAIN	Port PA Input Value Register
0x108	PAOUT	Port PA Output Value Configuration Register
0x10C	PAADS	Port PA Digital-to-Analog Configuration Register
0x110	PABSET	Port PA Bit Set Register
0x114	PABCLR	Port PA Bit Clear Register
0x118	PABSETCLR	Port PA Bit Set Clear Register
0x11C	PADR	Port PA Driving Capability Configuration Register
0x120	PAPU	Port PA Pull-Up Enable Configuration Register
0x124	PAPD	Port PA Pull-Down Enable Configuration Register
0x12C	PAOD	Port PA Open-Drain Output Configuration Register
0x130	PAHIE	Port PA High Level Interrupt Enable Configuration Register
0x134	PALIE	Port PA Low Level Interrupt Enable Configuration Register
0x138	PARIE	Port PA Rising Edge Interrupt Enable Configuration Register
0x13C	PAFIE	Port PA Falling Edge Interrupt Enable Configuration Register
0x200	PA_STAT	Port PA Interrupt Status Register
0x210	PA_ICLR	Port PA Interrupt Clear Register
0x140	PBDIR	Port PB Input and Output Configuration Register
0x144	PBIN	Port PB Input Value Register

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Offset	Register	Description
0x148	PBOUT	Port PB Output Value Configuration Register
0x14C	PBADS	Port PB Digital-to-Analog Configuration Register
0x150	PBBSET	Port PB Bit Set Register
0x154	PBBCLR	Port PB Bit Clear Register
0x158	PBBSETCLR	Port PB Bit Set Clear Register
0x15C	PBDR	Port PB Driving Capability Configuration Register
0x160	PBPU	Port PB Pull-Up Enable Configuration Register
0x164	PBPD	Port PB Pull-Down Enable Configuration Register
0x16C	PBOD	Port PB Open-Drain Output Configuration Register
0x170	PBHIE	Port PB High Level Interrupt Enable Configuration Register
0x174	PBLIE	Port PB Low Level Interrupt Enable Configuration Register
0x178	PBRIE	Port PB Rising Edge Interrupt Enable Configuration Register
0x17C	PBFIE	Port PB Falling Edge Interrupt Enable Configuration Register
0x240	PB_STAT	Port PB Interrupt Status Register
0x250	PB_ICLR	Port PB Interrupt Clear Register
0x180	PCDIR	Port PC Input and Output Configuration Register
0x184	PCIN	Port PC Input Value Register
0x188	PCOUT	Port PC Output Value Configuration Register
0x18C	PCADS	Port PC Digital-to-Analog Configuration Register
0x190	PCBSET	Port PC Bit Set Register
0x194	PCBCLR	Port PC Bit Clear Register
0x198	PCBSETCLR	Port PC Bit Set Clear Register
0x19C	PCDR	Port PC Driving Capability Configuration Register
0x1A0	PCPU	Port PC Pull-Up Enable Configuration Register
0x1A4	PCPD	Port PC Pull-Down Enable Configuration Register
0x1AC	PCOD	Port PC Open-Drain Output Configuration Register
0x1B0	PCHIE	Port PC High Level Interrupt Enable Configuration Register

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Offset	Register	Description
0x1B4	PCLIE	Port PC Low Level Interrupt Enable Configuration Register
0x1B8	PCRIE	Port PC Rising Edge Interrupt Enable Configuration Register
0x1BC	PCFIE	Port PC Falling Edge Interrupt Enable Configuration Register
0x280	PC_STAT	Port PC Interrupt Status Register
0x290	PC_ICLR	Port PC Interrupt Clear Register
0x1C0	PDDIR	Port PD Input and Output Configuration Register
0x1C4	PDIN	Port PD Input Value Register
0x1C8	PDOUT	Port PD Output Value Configuration Register
0x1CC	PDADS	Port PD Digital-to-Analog Configuration Register
0x1D0	PDBSET	Port PD Bit Set Register
0x1D4	PDBCLR	Port PD Bit Clear Register
0x1D8	PDBSETCLR	Port PD Bit Set Clear Register
0x1DC	PDDR	Port PD Driving Capability Configuration Register
0x1E0	PDPU	Port PD Pull-Up Enable Configuration Register
0x1E4	PDPD	Port PD Pull-Down Enable Configuration Register
0x1EC	PDOD	Port PD Open-Drain Output Configuration Register
0x1F0	PDHIE	Port PD High Level Interrupt Enable Configuration Register
0x1F4	PDLIE	Port PD Low Level Interrupt Enable Configuration Register
0x1F8	PDRIE	Port PD Rising Edge Interrupt Enable Configuration Register
0x1FC	PDFIE	Port PD Falling Edge Interrupt Enable Configuration Register
0x2C0	PD_STAT	Port PD Interrupt Status Register
0x2D0	PD_ICLR	Port PD Interrupt Clear Register
0x304	GPIO_CTRL1	Port Alternate Function Configuration Register 1
0x308	GPIO_CTRL2	Port Alternate Function Configuration Register 2
0x30C	GPIO_TIMGS	Port Auxiliary Function Timer Gate Selection
0x310	GPIO_TIMES	Port Auxiliary Function Timer ETR selection
0x314	GPIO_TIMCPS	Port Auxiliary Function Timer Capture Input selection

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Offset	Register	Description
0x318	GPIO_PCAS	Port Auxiliary Function PCA Capture Selection
0x31C	GPIO_PCNT	Port Auxiliary Function PCNT Input selection
0x1000+0x4*y	PEy_SEL	Port PEy Function Configuration Register (y=2-5, 11-14)
0x1040+0x4*y	PFy_SEL	Port PFy Function Configuration Register (y=0-1, 4-7, 11)
0x1100	PEDIR	Port PE Input and Output Configuration Register
0x1104	PEIN	Port PE Input Value Register
0x1108	PEOUT	Port PE Output Value Configuration Register
0x110C	PEADS	Port PE Digital-to-Analog Configuration Register
0x1110	PEBSET	Port PE Bit Set Register
0x1114	PEBCLR	Port PE Bit Clear Register
0x1118	PEBSETCLR	Port PE Bit Set Clear Register
0x111C	PEDR	Port PE Driving Capability Configuration Register
0x1120	PEPU	Port PE Pull-Up Enable Configuration Register
0x1124	PEPD	Port PE Pull-Down Enable Configuration Register
0x112C	PEOD	Port PE Open-Drain Output Configuration Register
0x1130	PEHIE	Port PE High Level Interrupt Enable Configuration Register
0x1134	PELIE	Port PE Low Level Interrupt Enable Configuration Register
0x1138	PERIE	Port PE Rising Edge Interrupt Enable Configuration Register
0x113C	PEFIE	Port PE Falling Edge Interrupt Enable Configuration Register
0x1200	PE_STAT	Port PE Interrupt Status Register
0x1210	PE_ICLR	Port PE Interrupt Clear Register
0x1140	PFDIR	Port PF Input and Output Configuration Register
0x1144	PFIN	Port PF Input Value Register
0x1148	PFOUT	Port PF Output Value Configuration Register
0x114C	PFADS	Port PF Digital-to-Analog Configuration Register
0x1150	PFBSET	Port PF Bit Set Register
0x1154	PFBCLR	Port PF Bit Clear Register

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Offset	Register	Description
0x1158	PFBSETCLR	Port PF Bit Set Clear Register
0x115C	PFDR	Port PF Driving Capability Configuration Register
0x1160	PFPU	Port PF Pull-Up Enable Configuration Register
0x1164	PFPD	Port PF Pull-Down Enable Configuration Register
0x116C	PFOD	Port PF Open-Drain Output Configuration Register
0x1170	PFHIE	Port PF High Level Interrupt Enable Configuration Register
0x1174	PFLIE	Port PF Low Level Interrupt Enable Configuration Register
0x1178	PFRIE	Port PF Rising Edge Interrupt Enable Configuration Register
0x117C	PFFIE	Port PF Falling Edge Interrupt Enable Configuration Register
0x1240	PF_STAT	Port PF Interrupt Status Register
0x1250	PF_ICLR	Port PF Interrupt Clear Register

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6.5.2 Port General Register

6.5.2.1 Port Px Input/Output Configuration Register (PxDIR) (x =A to F)

Offset: 0x100 (PA), 0x140 (PB), 0x180 (PC), 0x1C0 (PD), 0x1100 (PE), 0x1140 (PF)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000FFFF																															
Name	Reserved																PxDIR															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	PxDIR	Port Px input/output configuration register Corresponding to Px15-Px00: ● 0b0: Configured as output ● 0b1: Configured as input **Note** Each bit corresponds to one port, please refrain from configuring non-existent ports, for example: PxDIR[15] corresponds to port Px15.	RW

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6.5.2.2 Port Px Input Value Register (PxIN) (x =A to F)

Offset: 0x104 (PA), 0x144 (PB), 0x184 (PC), 0x1C4 (PD), 0x1104 (PE), 0x1144 (PF)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	-																															
Name	Reserved																PxIN															
Access																	RO															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	PxIN	Port Px input value register Corresponding to Px15-Px00: ● 0b0: Input low level ● 0b1: Input high level **Note** Each bit corresponds to one port, please refrain from configuring non-existent ports.	RO

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6.5.2.3 Port Px Output Value Configuration Register (PxOUT) (x=A to F)

Offset: 0x108 (PA), 0x148 (PB), 0x188 (PC), 0x1C8 (PD), 0x1108 (PE), 0x1148 (PF)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	Reserved																PxOUT															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	PxOUT	Port Px output value register Corresponding to Px15-Px00: ● 0b0: Output low level ● 0b1: Output high level, if it is configured as an open-drain output, an external pull-up resistor is required to pull it high **Note** Each bit corresponds to one port, please refrain from configuring non-existent ports.	RW

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6.5.2.4 Port Px Digital-to-Analog Configuration Register (PxADS) (x=A to F)

Offset: 0x10C (PA), 0x14C (PB), 0x18C (PC), 0x1CC (PD), 0x110C (PE), 0x114C (PF)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																PxADS															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	PxADS	Port Px digital-to-analog configuration register Corresponding to Px15-Px00: ● 0b0: Configured as a digital port ● 0b1: Configured as an analog port **Note** Each bit corresponds to one port, please refrain from configuring non-existent ports.	RW

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6.5.2.5 Port Px Bit Set Register (PxBSET) (x=A to F)

Offset: 0x110 (PA), 0x150 (PB), 0x190 (PC), 0x1D0 (PD), 0x1110 (PE), 0x1150 (PF)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																PxBSET															
Access																	WO															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	PxBSET	Port Px bit set register Corresponding to Px15-Px00, writing 1 sets the bit, writing 0 has no effect on the port state. **Note** Each bit corresponds to one port, please refrain from configuring non-existent ports.	WO

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6.5.2.6 Port Px Bit Clear Register (PxBCLR) (x=A to F)

Offset: 0x114 (PA), 0x154 (PB), 0x194 (PC), 0x1D4 (PD), 0x1114 (PE), 0x1154 (PF)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																PxBCLR															
Access																	WO															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	PxBCLR	Port Px bit clear register Corresponding to Px15-Px00, writing 1 clears the bit, writing 0 has no effect on the port state. **Note** Each bit corresponds to one port, please refrain from configuring non-existent ports.	WO

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6.5.2.7 Port Px Bit Set Clear Register (PxBSETCLR) (x=A to F)

Offset: 0x118 (PA), 0x158 (PB), 0x198 (PC), 0x1D8 (PD), 0x1118 (PE), 0x1158 (PF)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	PxBSET																PxBCLR															
Access	WO																WO															

Bit	Name	Functional Description	Access
31:16	PxBSET	Port Px bit set register Corresponding to Px15-Px00, writing 1 sets the bit, writing 0 has no effect on the port state. **Note** Each bit corresponds to one port, please refrain from configuring non-existent ports.	WO
15:0	PxBCLR	Port Px bit clear register Corresponding to Px15-Px00, writing 1 clears the bit, writing 0 has no effect on the port state. **Note** Each bit corresponds to one port, please refrain from configuring non-existent ports.	WO

Note

When the same bit of PxBSET and PxBCLR is both set to 1, PxBCLR has higher priority, the port is cleared.

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6.5.2.8 Port Px Pull-Up Enable Configuration Register (PxPU) (x=A to F)

Offset: 0x120 (PA), 0x160 (PB), 0x1A0 (PC), 0x1E0 (PD), 0x1120 (PE), 0x1160 (PF)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																PxPU															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	PxPU	Port Px pull-up enable configuration register Corresponding to Px15-Px00: ● 0b0: Disable ● 0b1: Enable **Note** Each bit corresponds to one port, please refrain from configuring non-existent ports.	RW

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6.5.2.9 Port Px Driving Capability Configuration Register (PxDR) (x=A to F)

Offset: 0x11C (PA), 0x15C (PB), 0x19C (PC), 0x1DC (PD), 0x111C (PE), 0x115C (PF)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																PxDR															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	PxDR	Port Px driving capability configuration register Corresponding to Px15-Px00: ● 0b0: High driving capability ● 0b1: Low driving capability **Note** Each bit corresponds to one port, please refrain from configuring non-existent ports.	RW

6.5.2.10 Port Px Pull-Down Enable Configuration Register (PxPD) (x=A to F)

Offset: 0x124 (PA), 0x164 (PB), 0x1A4 (PC), 0x1E4 (PD), 0x1124 (PE), 0x1164 (PF)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																PxPD															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	PxPD	Port Px pull-down enable configuration register Corresponding to Px15-Px00: ● 0b0: Disable ● 0b1: Enable **Note** Each bit corresponds to one port, please refrain from configuring non-existent ports.	RW

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6.5.2.11 Port Px Open-Drain Output Configuration Register (PxOD) (x=A to F)

Offset: 0x12C (PA), 0x16C (PB), 0x1AC (PC), 0x1EC (PD), 0x112C (PE), 0x116C (PF)

xOffset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																PxOD															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	PxOD	Port Px open-drain output configuration register Corresponding to Px15-Px00: ● 0b0: Set the port output mode to push-pull output ● 0b1: Set the port output mode to open-drain output **Note** Each bit corresponds to one port, please refrain from configuring non-existent ports.	RW

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6.5.2.12 Port Px High Level Interrupt Enable Configuration Register (PxHIE) (x=A to F)

Offset: 0x130 (PA), 0x170 (PB), 0x1B0 (PC), 0x1F0 (PD), 0x1130 (PE), 0x1170 (PF)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																PxHIE															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	PxHIE	Port Px high level interrupt enable configuration register Corresponding to Px15-Px00: ● 0b0: Disable ● 0b1: Enable **Note** Each bit corresponds to one port, please refrain from configuring non-existent ports.	RW

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6.5.2.13 Port Px Low Level Interrupt Enable Configuration Register (PxLIE) (x=A to F)

Offset: 0x134 (PA), 0x174 (PB), 0x1B4 (PC), 0x1F4 (PD), 0x1134 (PE), 0x1174 (PF)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																PxLIE															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	PxLIE	Port Px low level interrupt enable configuration register Corresponding to Px15-Px00: ● 0b0: Disable ● 0b1: Enable **Note** Each bit corresponds to one port, please refrain from configuring non-existent ports.	RW

6.5.2.14 Port Px Rising Edge Interrupt Enable Configuration Register (PxRIE) (x=A to F)

Offset: 0x138 (PA), 0x178 (PB), 0x1B8 (PC), 0x1F8 (PD), 0x1138 (PE), 0x1178 (PF)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																PxRIE															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	PxRIE	Port Px rising edge interrupt enable configuration register Corresponding to Px15-Px00: ● 0b0: Disable ● 0b1: Enable **Note** Each bit corresponds to one port, please refrain from configuring non-existent ports.	RW

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6.5.2.15 Port Px Falling Edge Interrupt Enable Configuration Register (PxFIE) (x=A to F)

Offset: 0x13C (PA), 0x17C (PB), 0x1BC (PC), 0x1FC (PD), 0x113C (PE), 0x117C (PF)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																PxFIE															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	PxFIE	Port Px falling edge interrupt enable configuration register Corresponding to Px15-Px00: ● 0b0: Disable ● 0b1: Enable **Note** Each bit corresponds to one port, please refrain from configuring non-existent ports.	RW

6.5.2.16 Port Px Interrupt Status Register (Px_STAT) (x=A to F)

Offset: 0x200 (PA), 0x240 (PB), 0x280 (PC), 0x2C0 (PD), 0x1200 (PE), 0x1240 (PF)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																Px_STAT															
Access																	RO															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	Px_STAT	Port Px interrupt status register Corresponding to Px15-Px00: ● 0b0: No interrupt trigger ● 0b1: Interrupt trigger **Note** Each bit corresponds to one port, please refrain from configuring non-existent ports.	RO

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6.5.2.17 Port Px Interrupt Clear Register (Px_ICLR) (x=A to F)

Offset: 0x210 (PA), 0x250 (PB), 0x290 (PC), 0x2D0 (PD), 0x1210 (PE), 0x1250 (PF)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000FFFF																															
Name	Reserved																Px_ICLR															
Access																	WO															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	Px_ICLR	Port Px interrupt clear register Corresponding to Px15-Px00, write 0 to clear flag, write 1 has no effect; read always returns 1. **Note** Each bit corresponds to one port, please refrain from configuring non-existent ports.	WO

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6.5.3 Port Auxiliary Register

6.5.3.1 Port Auxiliary Function Configuration Register 1 (GPIO_CTRL1)

Offset	Bit Position																													
0x304	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																	IR_POL	HCLK_EN	PCLK_EN	HCLK_SEL		PCLK_SEL		NSS0_SEL				EXT_CLK_SEL			
Access																		RW	RW	RW	RW		RW		RW				RW			

Bit	Name	Functional Description	Access
31:15	*Reserved*	-	-
14	IR_POL	IR output polarity selection ● 0b0: Forward output ● 0b1: Inverted output	RW
13	HCLK_EN	HCLK output gating ● 0b0: Gating ● 0b1: Output	RW
12	PCLK_EN	PCLK output gating ● 0b0: Gating ● 0b1: Output	RW
11:10	HCLK_SEL	HCLK output frequency division selection ● 0b00: HCLK ● 0b01: HCLK/2 ● 0b10: HCLK/4 ● 0b11: HCLK/8	RW
9:8	PCLK_SEL	PCLK output frequency division selection ● 0b00: PCLK ● 0b01: PCLK/2 ● 0b10: PCLK/4 ● 0b11: PCLK/8	RW
7:4	NSS0_SEL	SPI0NSS signal source selection ● 0b0000: High level ● 0b0001: PA03 ● 0b0010: PA04 ● 0b0011: PA06 ● 0b0100: PA08 ● 0b0101: PA09 ● 0b0110: PA12 ● 0b0111: PA15 ● 0b1000: PB01	RW

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Bit	Name	Functional Description	Access
7:4	NSS0_SEL	● 0b1001: PB02 ● 0b1010: PB05 ● 0b1011: PB06 ● 0b1100: PB09 ● 0b1101: PB10 ● 0b1110: PB12 ● 0b1111: PB14	RW
3:0	EXT_CLK_SEL	External clock signal source selection ● 0b0000: High level ● 0b0001: PA03 ● 0b0010: PA04 ● 0b0011: PA06 ● 0b0100: PA08 ● 0b0101: PA09 ● 0b0110: PA12 ● 0b0111: PA15 ● 0b1000: PB01 ● 0b1001: PB02 ● 0b1010: PB05 ● 0b1011: PB06 ● 0b1100: PB09 ● 0b1101: PB10 ● 0b1110: PB12 ● 0b1111: PB14	RW

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6.5.3.2 Port Auxiliary Function Configuration Register 2 (GPIO_CTRL2)

Offset	Bit Position																													
0x308	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																AHB_SEL	Reserved							TCLK_DIV		TCLK_SEL		NSS1_SEL			
Access																	RW								RW		RW		RW			

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15	AHB_SEL	AHB bus access mode ● 0b0: Use the FASTIO bus to access PxIN, PxOUT registers ● 0b1: Use the AHB bus to access PxIN, PxOUT registers	RW
14:8	*Reserved*	-	-
7:6	TCLK_DIV	TCLK output frequency division selection ● 0b00: TCLK ● 0b01: TCLK/2 ● 0b10: TCLK/4 ● 0b11: TCLK/8	RW
5:4	TCLK_SEL	TCLK output signal source selection ● 0b00: Setting prohibited ● 0b01: RCH ● 0b10: XTH ● 0b11: PLL	RW
3:0	NSS1_SEL	SPI1NSS signal source selection ● 0b0000: High level ● 0b0001: PA03 ● 0b0010: PA04 ● 0b0011: PA06 ● 0b0100: PA08 ● 0b0101: PA09 ● 0b0110: PA12 ● 0b0111: PA15 ● 0b1000: PB01 ● 0b1001: PB02 ● 0b1010: PB05 ● 0b1011: PB06 ● 0b1100: PB09 ● 0b1101: PB10 ● 0b1110: PB12 ● 0b1111: PB14	RW

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6.5.3.3 Port Auxiliary Function Timer Gate Selection (GPIO_TIMGS)

Offset	Bit Position																													
0x30C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																	LPTIM0_G			TIM3_G			TIM2_G			TIM1_G			TIM0_G		
Access																		RW			RW			RW			RW			RW		

Bit	Name	Functional Description	Access
31:15	*Reserved*	-	-
14:12	LPTIM0_G	LPTIM0 timer GATE input selection Parameter selection details (See Table Below)	RW
11:9	TIM3_G	TIM3 timer GATE input selection Parameter selection details (See Table Below)	RW
8:6	TIM2_G	TIM2 timer GATE input selection Parameter selection details (See Table Below)	RW
5:3	TIM1_G	TIM1 timer GATE input selection Parameter selection details (See Table Below)	RW
2:0	TIM0_G	TIM0 timer GATE input selection Parameter selection details (See Table Below)	RW

Value	LPTIM0_G	TIM3_G	TIM2_G	TIM1_G	TIM0_G
0b000	Pxy_SEL	Pxy_SEL	Pxy_SEL	Pxy_SEL	Pxy_SEL
0b001	LPUART0_RXD	UART0_RXD	UART0_RXD	LPUART0_RXD	UART0_RXD
0b010	LPUART1_RXD	UART1_RXD	UART1_RXD	LPUART1_RXD	UART1_RXD
0b011	VC0_OUT	LPUART0	VC0_OUT	VC0_OUT	VC0_OUT
0b100	VC1_OUT	LPUART1	VC1_OUT	VC1_OUT	VC1_OUT
0b101	PB03	VC0_OUT	PA10	PA08	PA03
0b110	PB05	PA06	PB04	PB03	PB08
0b111	PC00	PA11	PB11	PB13	PB15

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6.5.3.4 Port Auxiliary Function Timer ETR Selection (GPIO_TIMES)

Offset	Bit Position																													
0x310	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																				LPTIM0_E			TIM3_E			TIM2_E			TIM1_E			TIM0_E		
Access																					RW			RW			RW			RW			RW		

Bit	Name	Functional Description	Access
31:15	*Reserved*	-	-
14:12	LPTIM0_E	LPTimer0 timer ETR input selection Parameter selection details (See Table Below)	RW
11:9	TIM3_E	TIM3 timer ETR input selection Parameter selection details (See Table Below)	RW
8:6	TIM2_E	TIM2 timer ETR input selection Parameter selection details (See Table Below)	RW
5:3	TIM1_E	TIM1 timer ETR input selection Parameter selection details (See Table Below)	RW
2:0	TIM0_E	TIM0 timer ETR input selection Parameter selection details (See Table Below)	RW

Value	LPTIM0_E	TIM3_E	TIM2_E	TIM1_E	TIM0_E
0b000	Pxy_SEL	Pxy_SEL	Pxy_SEL	Pxy_SEL	Pxy_SEL
0b001	PCNT_S0	UART0_RXD	LPUART0_RXD	UART0_RXD	LPUART0_RXD
0b010	LVD_OUT	UART1_RXD	LPUART1_RXD	UART1_RXD	LPUART1_RXD
0b011	VC0_OUT	VC1_OUT	VC0_OUT	VC1_OUT	VC0_OUT
0b100	VC1_OUT	PCNT_S0	PCNT_S1	LVD_OUT	LVD_OUT
0b101	PB04	PA00	PA04	PA01	PA00
0b110	PB06	PA12	PC04	PC09	PA05
0b111	PC03	PA13	PC08	PD02	PA15

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6.5.3.5 Port Auxiliary Function Timer Capture Input Selection (GPIO_TIMCPS)

Offset	Bit Position																													
0x314	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																		TIM3_CB			TIM3_CA			TIM2_CA			TIM1_CA			TIM0_CA		
Access																			RW			RW			RW			RW			RW		

Bit	Name	Functional Description	Access
31:15	*Reserved*	-	-
14:12	TIM3_CB	TIM3 timer CH0B input selection Parameter selection details (See Table Below)	RW
11:9	TIM3_CA	TIM3 timer CH0A input selection Parameter selection details (See Table Below)	RW
8:6	TIM2_CA	TIM2 timer CHA input selection Parameter selection details (See Table Below)	RW
5:3	TIM1_CA	TIM1 timer CHA input selection Parameter selection details (See Table Below)	RW
2:0	TIM0_CA	TIM0 timer CHA input selection Parameter selection details (See Table Below)	RW

Value	TIM3_CB	TIM3_CA	TIM2_CA	TIM1_CA	TIM0_CA
0b000	Pxy_SEL	Pxy_SEL	Pxy_SEL	Pxy_SEL	Pxy_SEL
0b001	UART0_RXD	LPUART1_RXD	LPUART0_RXD	UART1_RXD	UART0_RXD
0b010	UART1_RXD	LPUART0_RXD	VC0_OUT	PA00	PA00
0b011	PCNT_S1	PCNT_S0	PA02	PA02	PA02
0b100	VC1_OUT	VC0_OUT	PA07	PA06	PA05
0b101	PA07	PA08	PB08	PB08	PA15
0b110	PB04	PB03	PB09	PB10	PB06
0b111	PB13	PB06	PC06	PB13	PB14

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6.5.3.6 Port Auxiliary Function PCA Capture Selection (GPIO_PCAS)

Offset	Bit Position																													
0x318	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																				LPTIM1_E			LPTIM1_G			PCA_ECI			PCA_CH0		
Access																					RW			RW			RW			RW		

Bit	Name	Functional Description	Access
31:12	*Reserved*	-	-
11:9	LPTIM1_E	LPTIM1 timer ETR input selection Parameter selection details (See Table Below)	RW
8:6	LPTIM1_G	LPTIM1 timer GATE input selection Parameter selection details (See Table Below)	RW
5:3	PCA_ECI	PCA ECI clock input selection Parameter selection details (See Table Below)	RW
2:0	PCA_CH0	PCA CH0 capture port input selection Parameter selection details (See Table Below)	RW

Value	LPTIM1_E	LPTIM1_G	PCA_ECI	PCA_CH0
0b000	Pxy_SEL	Pxy_SEL	Pxy_SEL	Pxy_SEL
0b001	UART1	UART0	PCNT_S1	PCNT_S0
0b010	LPUART1_RXD	LPUART0_RXD	LVD_OUT	PCNT_S1
0b011	VC0_OUT	VC1_OUT	VC0_OUT	LVD_OUT
0b100	VC2_OUT	VC2_OUT	VC1_OUT	VC1_OUT
0b101	LPTIM0_TOG	PD5	PA05	PA06
0b110	PE8	PE7	PB02	PB04
0b111	PC7	PC6	PD02	PC06

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6.5.3.7 Port Auxiliary Function PCNT Pulse Input Selection (GPIO_PCNT)

Offset	Bit Position																													
0x31C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																												PCNT_S1		PCNT_S0	
Access																													RW		RW	

Bit	Name	Functional Description	Access
31:4	*Reserved*	-	-
3:2	PCNT_S1	PCNT_S1 input selection ● 0b00: Pxy_SEL ● 0b01: VC0_OUT ● 0b10: VC1_OUT ● 0b11: VC2_OUT	RW
1:0	PCNT_S0	PCNT_S0 input selection ● 0b00: Pxy_SEL ● 0b01: VC0_OUT ● 0b10: VC1_OUT ● 0b11: VC2_OUT	RW

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6.5.4 Port Function Selection Register

6.5.4.1 Port Pxy Function Configuration Register (Pxy_SEL) (x =A to F)

Offset: 0x00+0x4*y (PA) (y= 0-15);

0x40+0x4*y (PB)(y=0-15);

0x80+0x4*y (PC)(y=0-15);

0xC0+0x4*y (PD)(y=0-4, 8-11);

0x1000+0x4*y (PE)(y=2-5, 11-14);

0x1040+0x4*y (PF)(y=0-1, 4-7, 11).

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																														SEL	
Access																															RW	

Bit	Name	Functional Description	Access
31:3	*Reserved*	-	-
2:0	SEL	Port Pxy function selection ● 0b000: GPIO ● 0b001: AF1 ● 0b010: AF2 ● 0b011: AF3 ● 0b100: AF4 ● 0b101: AF5 ● 0b110: AF6 ● 0b111: AF7 **Note** For the specific functions of AF1-AF7 please refer to the "Port Digital Multiplexing Function".	RW

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7 I2C

7.1 Introduction

Inter-Integrated Circuit Bus (I2C) is a two-wire bidirectional synchronous serial bus, which uses a clock line and a data line to transmit information between two devices connected to the bus, providing a simple and efficient method for data exchange between devices. Each device connected to the bus has a unique address, and any device can be used as both a master and a slave, but only one master is allowed at the same time. I2C standard is a real multi-master bus with a conflict detection mechanism and an arbitration mechanism. It can use the arbitration mechanism to avoid data conflicts and protect data when multiple masters request control of the bus at the same time.

I2C bus controller can meet various specifications of the I2C bus and support all transmission modes communicating with the I2C bus. The I2C logic can handle the transfer of bytes autonomously. It can keep track of the serial transfer, and there is a status register (I2C_STAT) that can reflect the status of the I2C bus controller and the I2C bus.

7.2 Features

I2C controller supports the following features:

- Support 4 working modes of master sending/receiving and slave sending/receiving
- Support 3 operating rates: Standard (100kbps)/Fast (400kbps)/Fast enhanced (1Mbps)
- Support 7-bit addressing function
- Support noise filtering function
- Support 3 slave addresses
- Support broadcast address
- Support interrupt status query function

7.3 Protocol Description

The I2C bus transfers information using the SCL (serial clock bus) and SDA (serial data bus) that connect devices. The master outputs a serial clock signal on the SCL line, and the data is transmitted on the SDA line, and each byte is transmitted (the highest bit MSB starts to be transmitted), followed by an acknowledge bit. One SCL clock pulse transfers one data bit.

7.3.1 Data Transmission on the I2C Bus

Usually the standard I2C transmission protocol consists of four parts: start (S) or repeated start signal (Sr), slave address and read and write bits, transmission data, and stop signal (P).

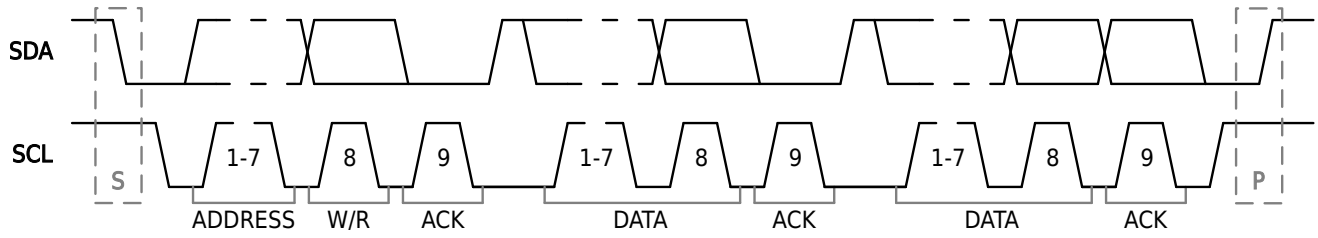

Figure 7-1 I2C Transmission Protocol

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- Start signal, repeated start signal, stop signal

  Start signal: When the bus is in an idle state (the SCL and SDA lines are high at the same time), a signal from high to low appears on the SDA line, indicating that a start signal is generated.

  Repeated start signal: A repeated start signal occurs when there is no stop signal between two start signals. This method is used by a master to communicate with another slave or the same slave with a different transfer direction (for example: from writing to the device to reading from the device) without releasing the bus.

  Stop signal: When the SCL line is high, a low-to-high signal appears on the SDA line, which is generated a stop signal. The master sends a stop signal to the bus to end the data transfer.

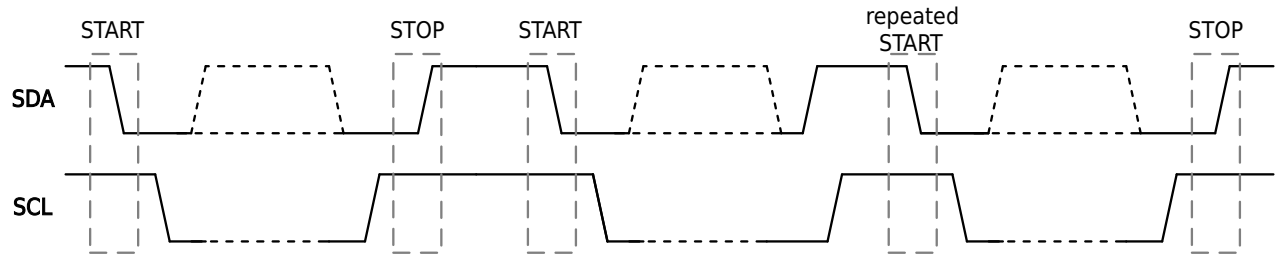

Figure 7-2 START, Repeated START and STOP

- Slave address and read/write bits

  When the start signal is generated, the master immediately transmits the first byte of data: 7-bit slave address + read/write bits, the read/write bits control the data transmission direction of the slave (0: write; 1: read). The addressed slave device will pull SDA low before the rising edge of the 9th SCL clock cycle as an acknowledgment (ACK).

- Transfer data

  During data transfer, one SCL clock pulse transfers one data bit, and the SDA line can only change when SCL is low.

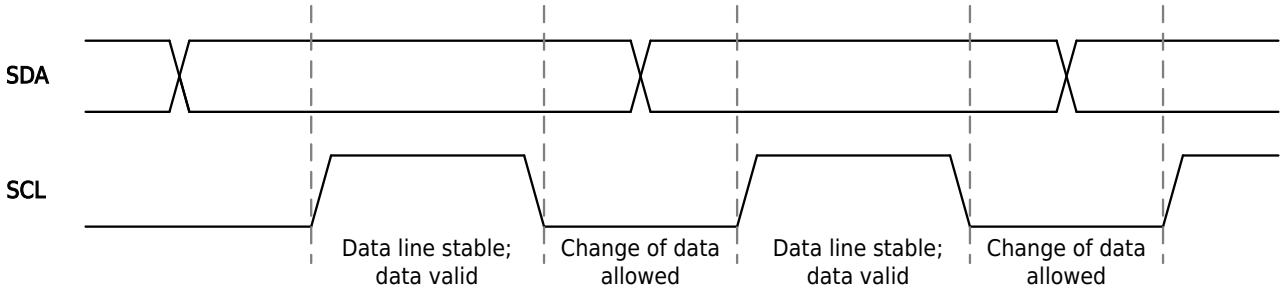

Figure 7-3 Bit Transfer on I2C Bus

7.3.2 Acknowledgment Signal on the I2C Bus

After transmitting each byte, the sending device releases control of SDA at the start of the 9th SCL clock cycle, while the receiving device generates an acknowledgment signal before the rising edge of that same SCL cycle. There are two types of acknowledgment bits:

- ACK: A low level signal. The receiving device pulls SDA low before the rising edge of the 9th SCL cycle and maintains it stable low throughout the high phase of this cycle. This signal indicates successful data reception by the receiver.
- NACK: A high level signal. The receiving device refrains from driving SDA during the 9th SCL cycle, leaving SDA persistently high. When the master acts as a transmitter and the slave generates a negative acknowledgment signal (NACK), the master may either generate a stop signal to terminate

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transmission or issue a repeated start signal to initiate a new transfer. When the master acts as a receiver and generates NACK, the slave releases control of SDA. The master then generates either a stop or repeated start signal.

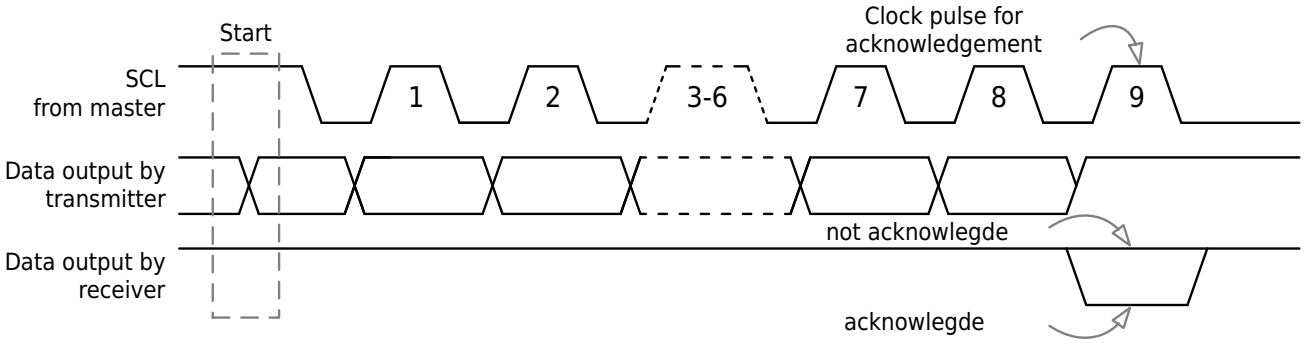

Figure 7-4 Acknowledgment Signal on I2C Bus

7.3.3 Arbitration on the I2C Bus

Arbitration on the I2C bus is divided into two parts:

- Synchronization on SCL line (clock synchronization)

  Since the I2C bus has the logic function of "AND", as long as one node on the SCL line sends a low level, the bus will show a low level. The bus can only behave as a high level when all nodes are sending a high level. Therefore, the clock low time is determined by the device with the longest clock low level period, and the clock high time is determined by the device with the shortest clock high level period. Due to the characteristics of I2C, when multiple nodes send clock signals at the same time, a unified clock signal is represented on the bus.

  When a slave can receive a byte of data at a higher rate but requires additional time to process it, the slave may suspend bus transmission by pulling SCL low after receiving the data and returning an ACK. The master then enters a wait state until the slave completes processing and releases SCL, after which the master proceeds with the next byte transfer. This slave clock stretching mechanism is implemented by controlling the I2C_CR.SI bit. Upon receiving data, I2C_CR.SI is automatically set to 1 by hardware, causing SCL to be held low by the slave. After processing the data, the slave clears I2C_CR.SI to release SCL.

- Arbitration on SDA line

  The arbitration on the SDA line is also due to the logical function of the "AND" of the I2C bus. After the master sends data, it decides whether to exit the competition by comparing the data on the bus. The master that loses the arbitration immediately switches to the unaddressed slave state to ensure that it can be addressed by the master that wins the arbitration. A master that loses arbitration continues to output clock pulses (on SCL) until the current serial byte has been sent. This principle can ensure that the I2C bus will not lose data when multiple masters attempt to control the bus.

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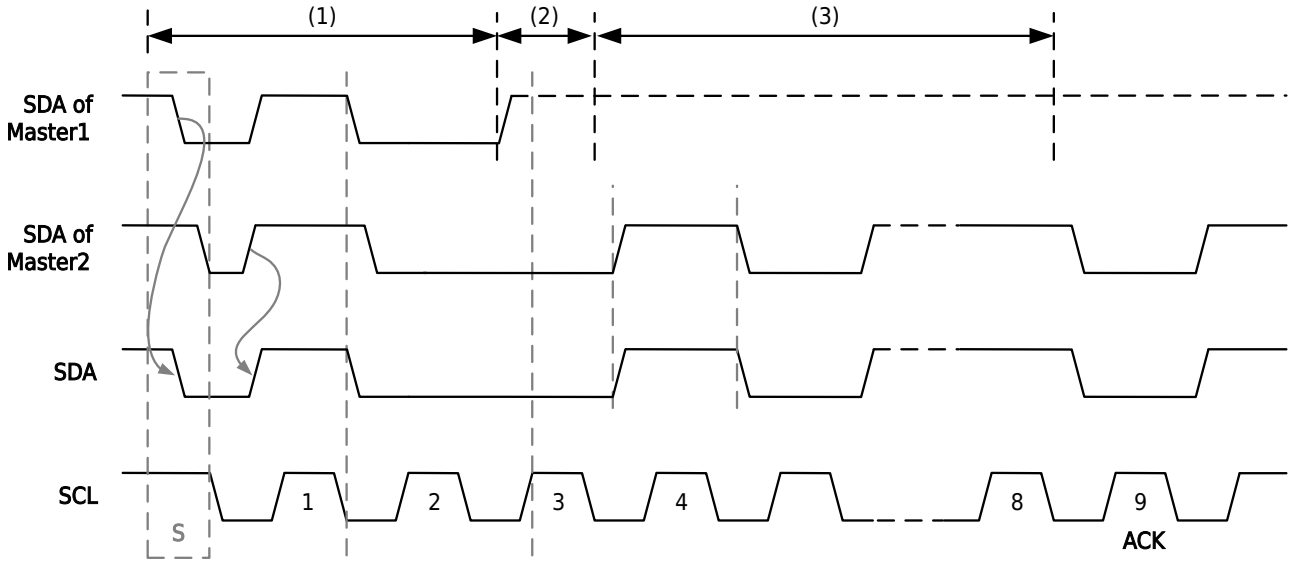

Figure 7-5 Arbitration on the I2C Bus

In the diagram above, the arbitration-triggering process is handled as follows:

- First, after transmitting the start signal, both Master 1 and Master 2 simultaneously transmit serial data.
- Second, during the low phase of the third SCL cycle, Master 1 transmits logic '1' while Master 2 transmits logic '0'. The logic '0' from Master 2 pulls SDA low, overriding the logic '1' of Master 1, thereby causing arbitration loss in Master 1 and transitioning it to an unaddressed slave mode.
- Third, after losing arbitration and entering the unaddressed slave mode, Master 1 continues clock pulse generation until completion of the current byte transmission, but ceases clock pulse generation for subsequent bytes. After Master 2 wins arbitratoin, subsequent data transfer on SDA is initiated by Master 2.

7.4 Functional Description

The I2C bus uses two wires to transfer information between devices connected to the bus SCL (serial clock line) and SDA (serial data line). Filtering logic can filter glitches on the data bus to protect data integrity. Since there are only non-directional ports, I2C requires that the pins used be configured as open-drain outputs. Each device connected to the bus can be addressed by a specific address. The I2C standard is a true multi-master bus with a collision detection mechanism and an arbitration mechanism. It prevents data collisions when two or more masters start transmitting data at the same time. I2C bus can be queried in the status register.

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7.4.1 Function Block Diagram

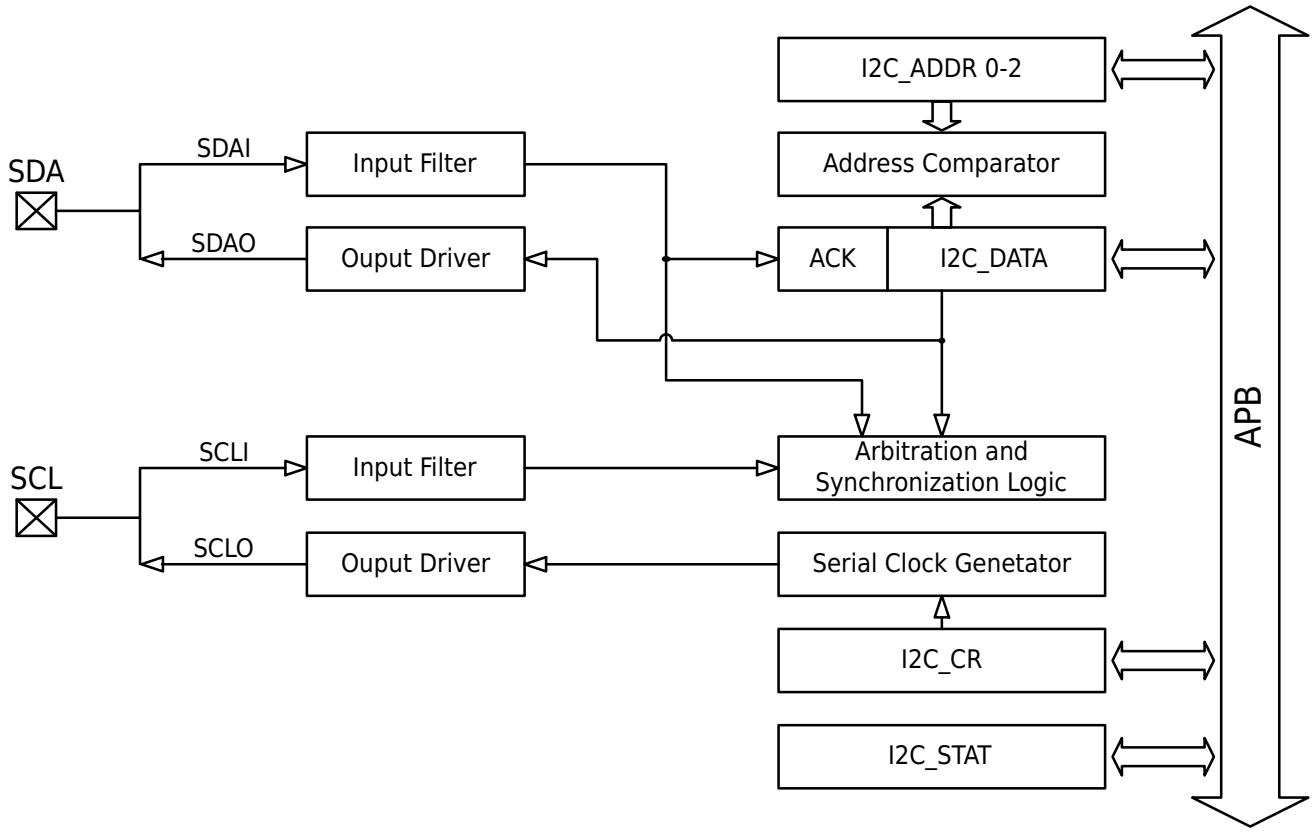

Figure 7-6 I2C Function Block Diagram

7.4.2 Serial Clock Generator

The serial clock generator uses an 8-bit counter as the baud rate generator. The frequency relationship between the SCL signal and the PCLK signal is $f_{SCL}= f_{PCLK}/8/(I2C\_TM+1)$, where I2C_TM should be greater than 0.

The following table lists the output frequency value of SCL signal when PCLK frequency is combined with I2C_TM.

Table 7-1 I2C Clock Signal Baud Rate

PCLK (kHz)	I2C_TM						
	1	2	3	4	5	6	7
1000	62	41	31	25	20	17	15
2000	125	83	62	50	41	35	31
4000	250	166	125	100	83	71	62
6000	375	250	187	150	125	107	93
8000	500	333	250	200	166	142	125
10000	625	416	312	250	208	178	156
12000	750	500	375	300	250	214	187
14000	875	583	437	350	291	250	218
16000	1000	666	500	400	333	285	250

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7.4.3 Input Filter

The input signal is synchronous with PCLK, and the spike pulse signal lower than the period of PCLK will be filtered out. By adjusting the value of I2C_CR.H1M, the intensity of filtering can be changed.

- When used as the master, if the value of I2C_TM is less than or equal to 9, I2C_CR.H1M should be set to 1 to make simple filtering; if the value of I2C_TM is greater than 9, I2C_CR.H1M should be set to 0 to make advanced filtering.
- When used as a slave, if the ratio of PCLK to SCL frequency is less than or equal to 30, I2C_CR.H1M should be set to 1 to make simple filtering; if the ratio of PCLK to SCL frequency is greater than 30, I2C_CR.H1M should be set to 0 to make advanced filtering.

7.4.4 Address Comparator

The I2C address comparator compares the received 7-bit address with the three slave addresses. According to the configuration of I2C_ADDR0.GC register, when the GC configuration is 0, the high 7 bits of the first received 8-bit byte are compared with the 7-bit Addr value of the I2C_ADDRx register. When the GC configuration is 1, the high 7 bits of the first received 8-bit byte are compared with the broadcast address (0x00). If any one is the same, the I2C_CR.SI bit will be set to 1 and an interrupt request will be generated. Query the I2C_MATCH register to obtain the matching address as the serial number.

7.4.5 Acknowledgement Flag Bit

I2C_CR.AA is the acknowledgement control bit. When the AA bit is 1, the I2C module responds with an acknowledgement signal (ACK) after receiving the data; when the AA bit is 0, the I2C module responds with a non-acknowledgement signal (NACK) after receiving the data.

7.4.6 Interrupt Generator

I2C_CR.SI is an interrupt flag. Whenever the value of the status register (I2C_STAT) changes (except for 0xF8), the SI flag will be set to 1. When an interrupt is generated, the status of the I2C bus can be obtained by querying the status register (I2C_STAT) to determine the actual source of the interrupt. In order to proceed to the next step, the SI flag must be cleared by software.

7.4.7 Operating Mode

The I2C component supports 8-bit bidirectional data transmission. The transmission rate can reach 100kbps in standard mode, 400kbps in fast mode, and 1Mbps in fast enhanced mode. It can operate in four modes: master sending mode, master receiving mode, slave receiving mode, and slave sending mode. There is also a special mode, broadcast call mode, which operates in a similar way to slave receive mode.

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- Master sending mode

  The master sends multiple bytes to the slave, and the master generates a clock, so it is necessary to fill in the set value in I2C_TM. I2C_CR.STA needs to be set to 1 in master sending mode. When the bus is free, the master initiates a start bit START. I2C_CR.SI is set to 1 if successful. Next, write the slave address and write bit (SLA+W) into I2C_DATA, and after clearing the SI bit, SLA+W is sent on the bus. After the master sends the SLA+W and receives the acknowledge signal (ACK) from the slave machine, the SI is set to 1. The data is then sent according to the user-defined format. After all the data is sent, set I2C_CR.STO to 1, clear the SI bit and send a STOP signal, or send a repeated start signal for a new round of data transmission.

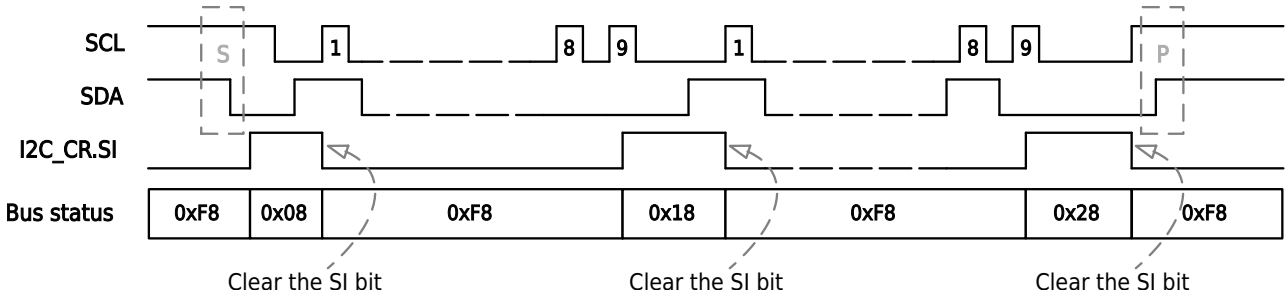

Figure 7-7 Data Synchronization Diagram of Master Sending Mode

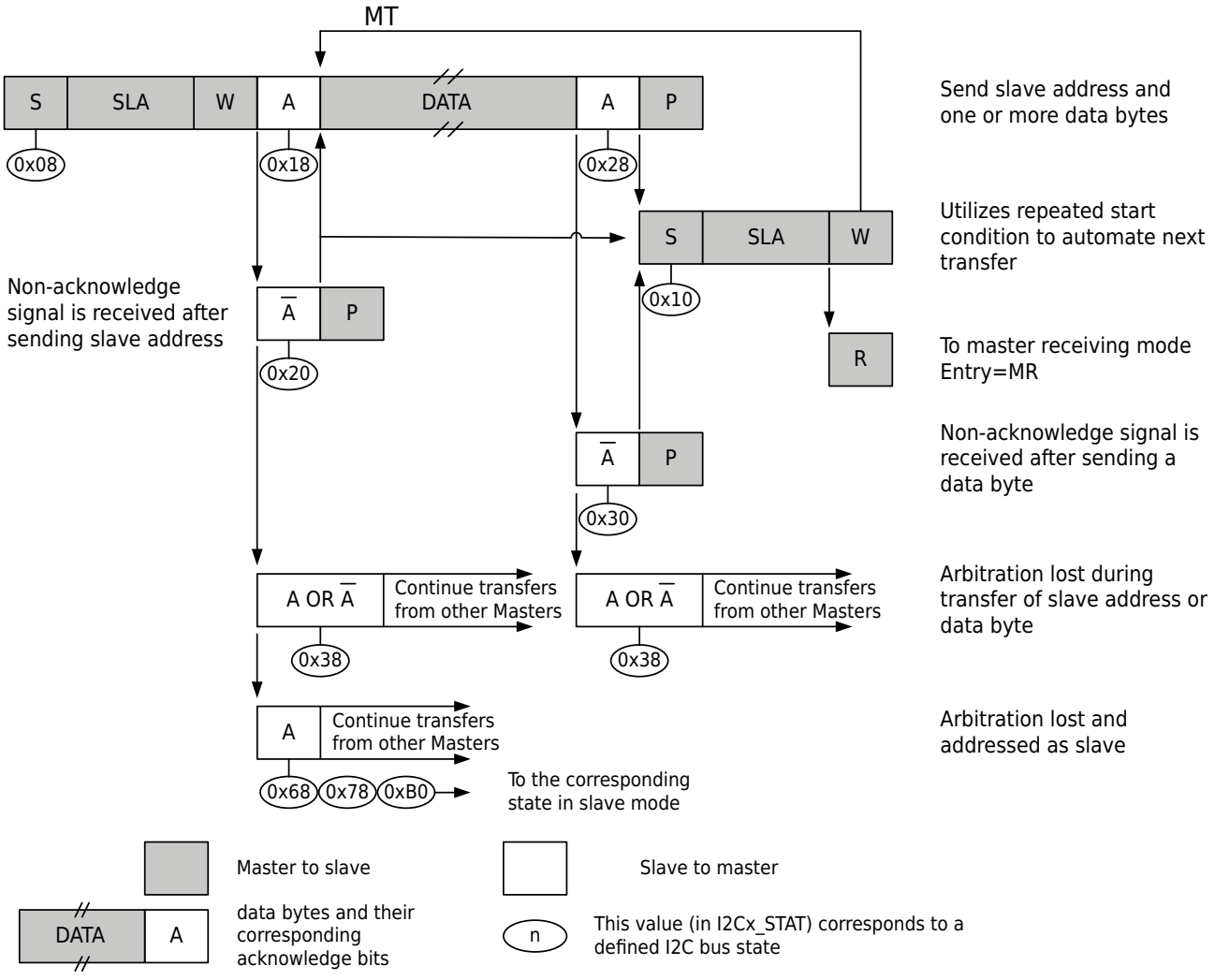

Figure 7-8 I2C Master Sending State Diagram

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- Master receiving mode

  In master receiving mode, the data is transferred from the slave. The initialization setting is the same as the master sending mode, after the master sends the start bit, I2C_DATA should be written into the slave address and " read bit " (SLA+R). After receiving the acknowledge signal (ACK) from the slave device, I2C_CR.SI is set to 1. After SI is cleared to 0, the master starts to receive data from the slave. If I2C_CR.AA is 1, the master responds with an acknowledge signal (ACK) after receiving the data; if it is 0, the master responds with a non-acknowledge signal (NACK). After that, the master can send a stop signal or repeat the start signal to begin the next round of data transmission.

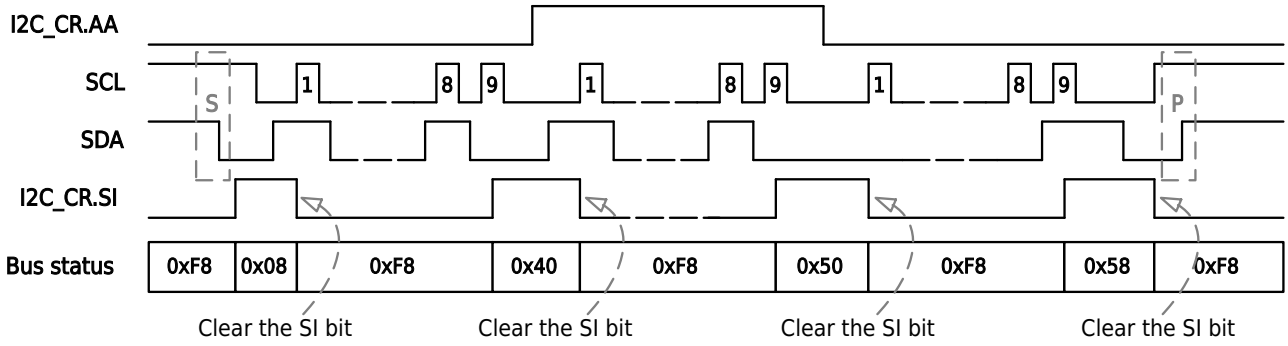

Figure 7-9 Data Synchronization Diagram of Master Receiving Mode

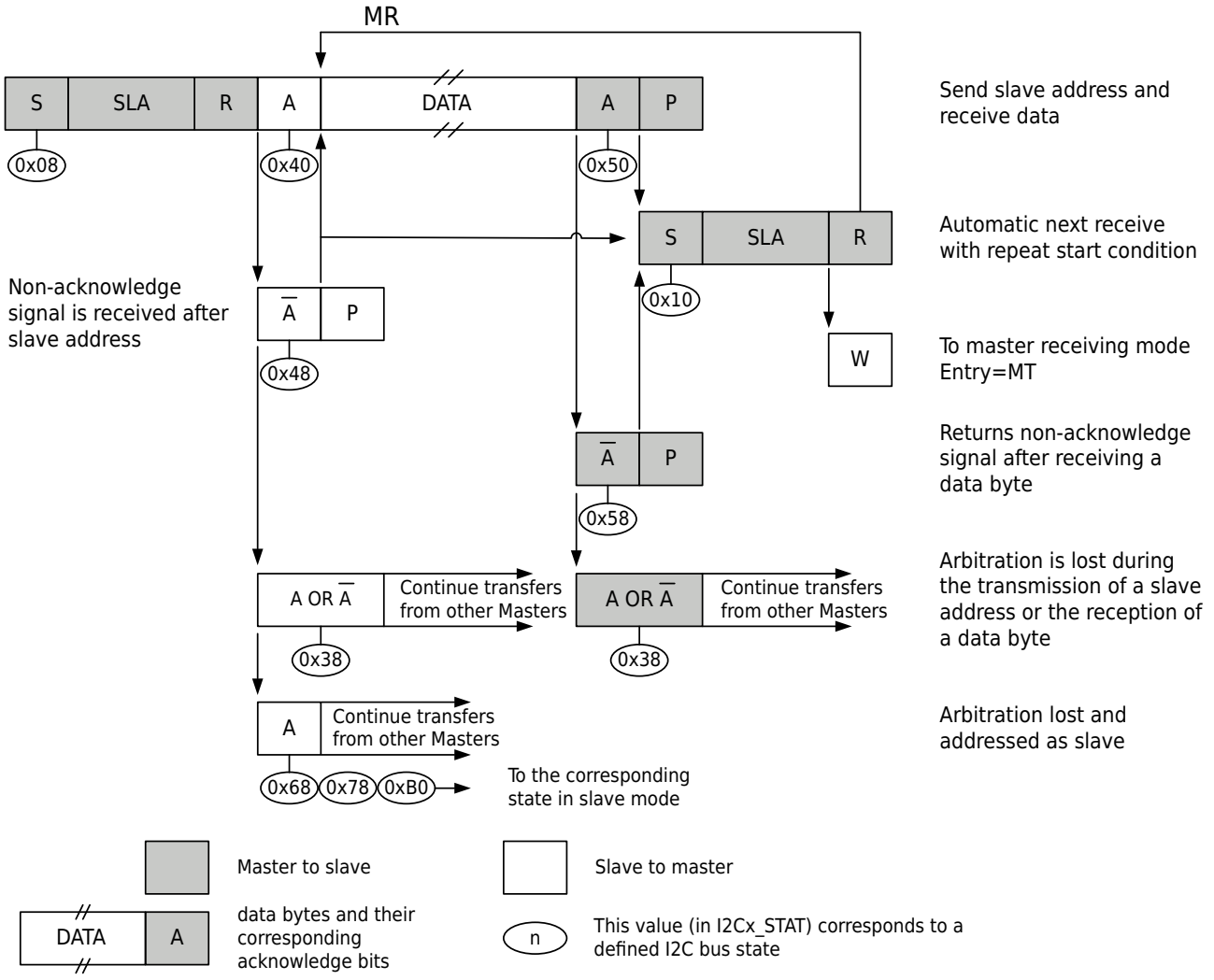

Figure 7-10 I2C Master Receiving State Diagram

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- Slave receiving mode

  In slave receiving mode, the slave receives data from the master. Before the transmission starts, I2C_ADDRx should be written to the slave address, and I2C_CR.AA is set to 1 to respond to the addressing of the master. After the above initialization, the slave enters idle mode and waits for a "write" signal (SLA+W). If the master arbitration fails, it will directly enter the mode where the unaddressed slave receives data.

  When the slave is addressed by the "write" signal SLA+W, the SI bit needs to be cleared to receive data from the master. If during the transmission process I2C_CR.AA = 0, the slave device will send a non-acknowledge signal (NACK) after receiving the next byte. The slave device will also switch to an unaddressed slave mode, terminate the connection with the master, stop receiving data, and keep the I2C_DATA as the data it previously received. Slave address recognition can be restored by setting AA, which means that the AA bit temporarily detaches the I2C module from the I2C bus.

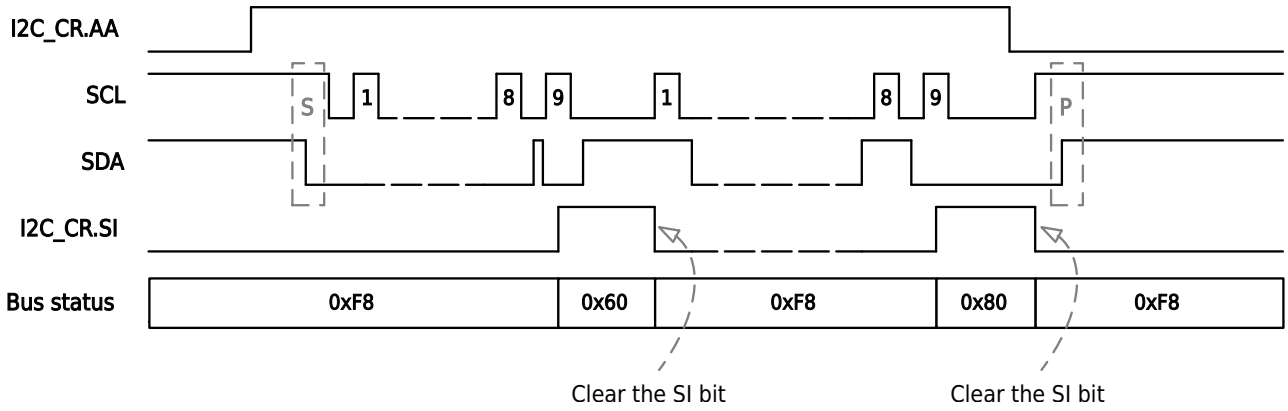

Figure 7-11 Slave Receiving Mode Data Synchronization Diagram

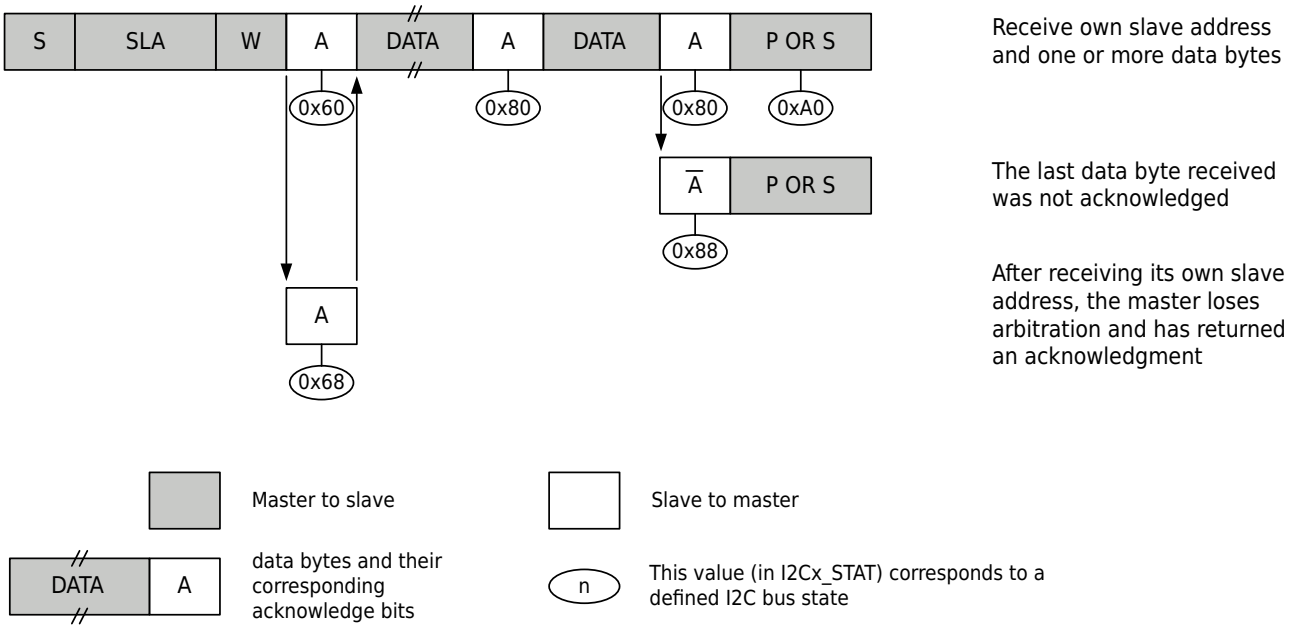

Figure 7-12 Slave Receiving State Diagram

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- Slave sending mode

  In the slave sending mode, the data is sent from the slave to the master. After initializing the I2C_ADDRx and I2C_CR.AA values, the device waits until its own address is addressed by the "read" signal (SLA+R). If the master arbitration fails, it can also enter the mode where the unaddressed slave devices send data.

  When the slave is addressed by the "read" signal SLA+R, it needs to clear SI to send data to the master. Usually, the master will send an acknowledgement signal (ACK) after receiving each byte of data.

  If the I2C_CR.AA register of the master is cleared during the transmission process, the slave will stop sending data and release SDA, and will change itself to an unaddressed slave.

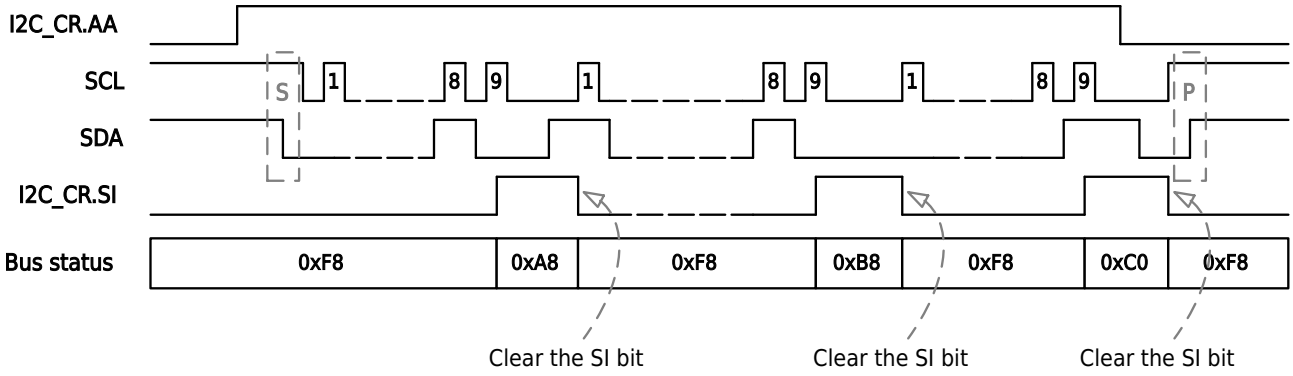

Figure 7-13 Slave Sending Mode Data Synchronization Diagram

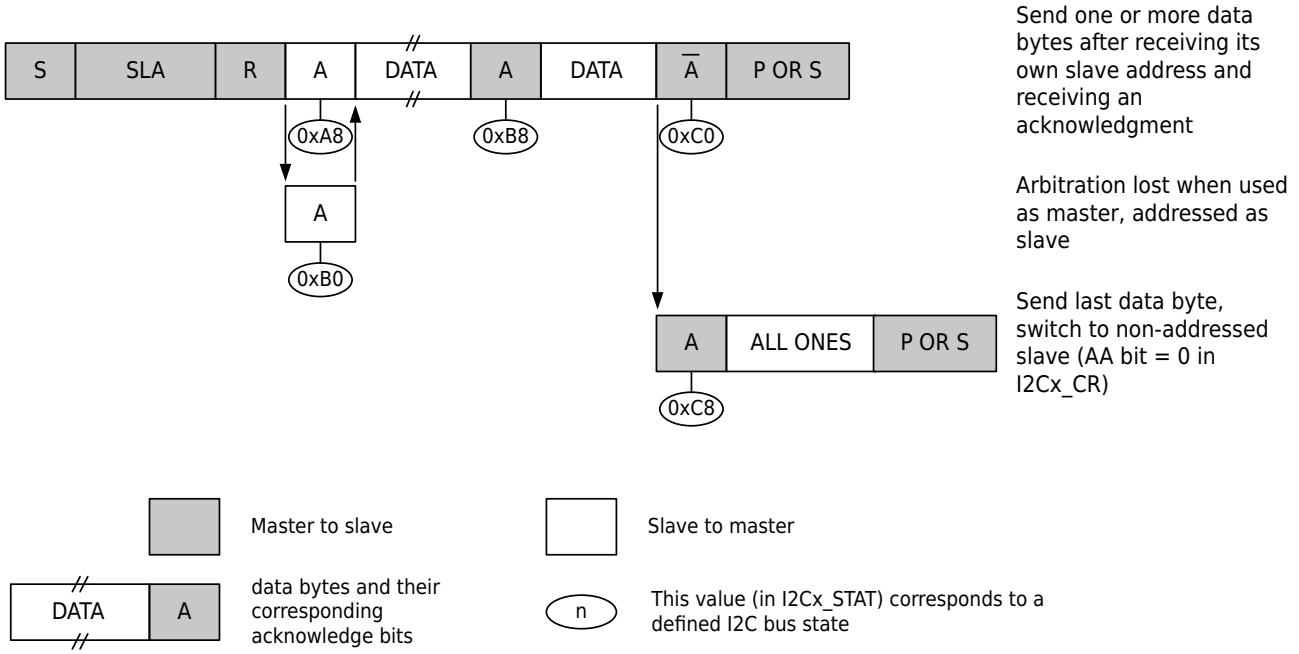

Figure 7-14 I2C Slave Sending State Diagram

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- Broadcast call mode

  Broadcast call mode is a special slave receiving mode, The addressing mode is 0x00, and the slave address and reading and writing are both 0. When both I2C_ADDR0.GC and I2C_CR.AA are set to 1, the broadcast call receiving mode is enabled. In this mode, the I2C_STAT value is different from the normal slave receiving mode I2C_STAT value. Arbitration failure may also enter broadcast call mode.

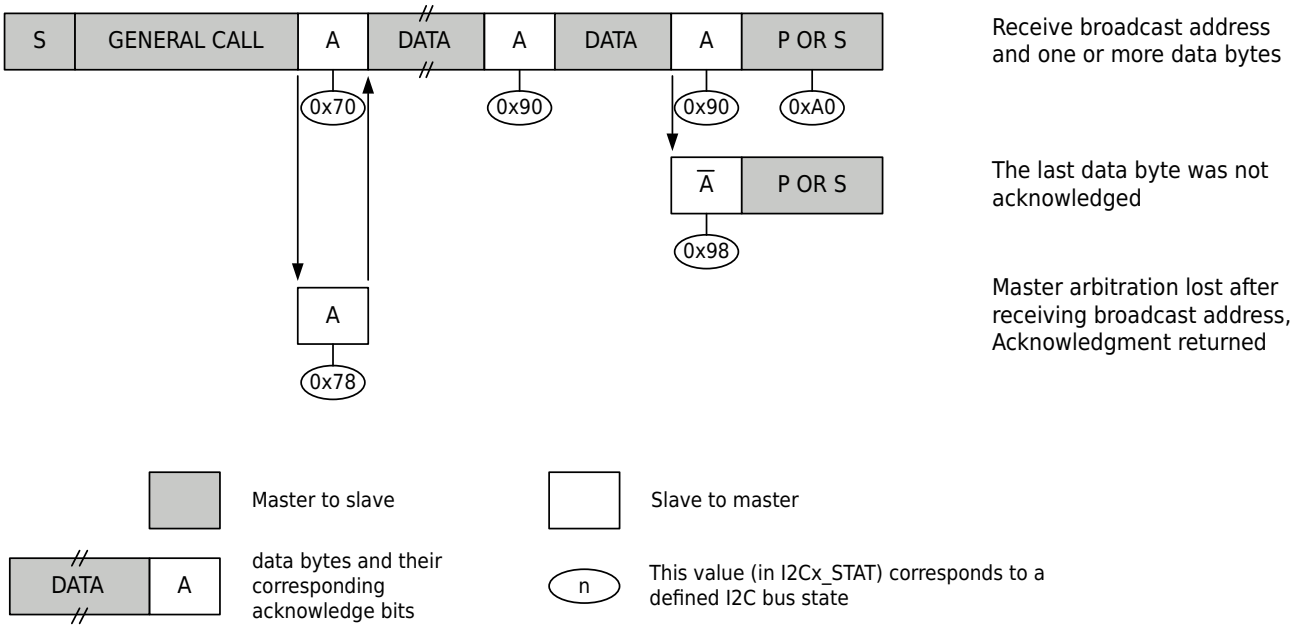

Figure 7-15 I2C Broadcast Call State Diagram

7.4.8 Status Code Expression

There are two special states in the I2C status register:

- 0xF8: This status code indicates that no relevant information is available, because the serial interrupt flag"SI" has not been set. This condition occurs between other states and before the I2C module has started to perform a serial transfer.
- 0x00: This status code indicates that a bus error occurred during I2C serial transmission. A bus error occurs when a START or STOP condition occurs at an illegal position in a format frame. These illegal locations refer to address bytes, data bytes, or acknowledge bits during serial transfers. When external disturbances affect the internal I2C block signals, bus errors can also occur. SI is set when a bus error occurs.

Table 7-2 I2C Status Code Expression

Status Code	Description
Master Sending Mode	
0x08	Start condition sent
0x10	Repeated start condition sent
0x18	SLA+W sent, ACK received
0x20	SLA+W sent, NACK received
0x28	Data in I2C_DATA has been sent, ACK has been received
0x30	Data in I2C_DATA has been sent, NACK has been received
0x38	Loss of Arbitration when SLA+ reads or writes data bytes

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Status Code	Description
Master Receiving Mode	
0x08	Start condition sent
0x10	Repeated start condition sent
0x38	Loss of arbitration in NACK (that is, the master detects that SDA has been pulled low by another device when responding with ACK)
0x40	SLA+R sent, ACK received
0x48	SLA+R sent, NACK received
0x50	Data byte has been received, ACK has been returned
0x58	Data byte has been received, NACK has been returned
Slave Receiving Mode	
0x60	Has received its own SLA+W and returned ACK
0x68	When the master is in SLA+ read and write lost arbitration, has received its own SLA+W, and has returned ACK
0x80	The previous addressing used its own slave address, received data bytes, and returned ACK
0x88	The previous addressing used its own slave address, received data bytes, and returned NACK
0xA0	During static addressing, when the stop condition or the repeated start condition is received.
Slave Sending Mode	
0xA8	Received its own SLA+R and returned ACK
0xB0	When the master loses arbitration, has received its own SLA+R, and has returned ACK
0xB8	Data sent, ACK received
0xC0	Data bytes sent, NACK received
0xC8	Loaded data bytes have been sent, ACK has been received
Broadcast Call Mode	
0x70	Received broadcast address (0x00), returned ACK
0x78	When the master is in SLA+ read and write lost arbitration, the broadcast address has been received, and ACK has been returned
0x90	The previous addressing used the broadcast address, data bytes have been received, and ACK has been returned
0x98	The previous addressing used the broadcast address, data bytes have been received, and NACK has been returned
0xA0	During static addressing, when the stop condition or the repeated start condition is received.
Other Miscellaneous Status	

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Status Code	Description
0xF8	No relevant status information available, SI=0
0x00	A bus error occurs during transmission, or external interference causes I2C to enter an undefined state

7.5 Operation Example

7.5.1 Master Sending Example

Procedure

Step1. Refer to the relevant description of the port digital multiplexing function in the "General-Purpose I/O (GPIO)" chapter. Map SCL and SDA to the required pins; and configure the SCL and SDA pins to the open-drain output mode.

Step2. Set SYSCTRL module register PERI_CLKEN0.I2Cx to 1 to enable the I2C working clock.

Step3. Write 0 and 1 to SYSCTRL module register PERI_RESET0.I2Cx in sequence to reset the I2C module.

Step4. Configure I2C_TM, so that the clock rate of SCL meets the application requirements.

Step5. Set I2C_TMRUN to 1 to enable the SCL clock generator.

Step6. Set I2C_CR.ENS to 1 to enable the I2C module.

Step7. Set I2C_CR.STA to 1, the bus tries to send the Start signal.

Step8. Wait for I2C_CR.SI to become 1 the Start signal has been sent to the bus, set I2C_CR.STA to 0.

Step9. Query I2C_STAT, if the register value is 0x08 or 0x10, continue to the next step, otherwise, perform error handling.

Step10. Write SLA+W to I2C_DATA, set I2C_CR.SI to 0 and send SLA+W.

Step11. Wait for I2C_CR.SI to become 1, SLA+W has been sent to the bus.

Step12. Query I2C_STAT, if the register value is 0x18, proceed to the next step. Otherwise, perform error handling.

Step13. Write the data to be sent to I2C_DATA, set I2C_CR.SI to 0, and send the data.

Step14. Wait for I2C_CR.SI to become 1, the data has been sent to the bus.

Step15. Query I2C_STAT, if the register value is 0x28, proceed to the next step. Otherwise, perform error handling.

Step16. If the data to be sent is not completed, then jump to step13 to continue execution.

Step17. Set I2C_CR.STO to 1, set I2C_CR.SI to 0, and the bus tries to send a Stop signal.

7.5.2 Master Receiving Example

Procedure

Step1. Refer to the relevant description of the port digital multiplexing function in the "General-Purpose I/O (GPIO)" chapter. Map SCL and SDA to the required pins; and configure the SCL and SDA pins to the open-drain output mode.

Step2. Set SYSCTRL module register PERI_CLKEN0.I2Cx to 1 to enable the I2C working clock.

Step3. Write 0 and 1 to SYSCTRL module register PERI_RESET0.I2Cx in sequence to reset the I2C module.

Step4. Configure I2C_TM, so that the clock rate of SCL meets the application requirements.

Step5. Set I2C_TMRUN to 1 to enable the SCL clock generator.

Step6. Set I2C_CR.ENS to 1 to enable the I2C module.

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Step7. Set I2C_CR.STA to 1, the bus tries to send the Start signal.

Step8. Wait for I2C_CR.SI to become 1, the Start signal has been sent to the bus, set I2C_CR.STA to 0.

Step9. Query I2C_STAT. If the register value is 0x08 or 0x10, continue to the next step, otherwise perform error handling.

Step10. Write SLA+R to I2C_DATA, set I2C_CR.SI to 0, and send SLA+R.

Step11. Wait for I2C_CR.SI to become 1, SLA+R has been sent to the bus.

Step12. Query I2C_STAT, if the register value is 0x40, continue to the next step, otherwise, perform error handling.

Step13. Set I2C_CR.AA to 1 to enable the acknowledge flag.

Step14. Set I2C_CR.SI to 0, the slave sends data, and the master sends ACK or NACK according to I2C_CR.AA.

Step15. Wait for I2C_CR.SI to become 1, read the received data from I2C_DATA.

Step16. Query I2C_STAT, if the register value is 0x50 or 0x58, continue to the next step, otherwise, perform error handling.

Step17. If the data to be received is only the last byte, set I2C_CR.AA to 0 and enable the non-acknowlege flag.

Step18. If the data to be received is not completed, jump to step14 to continue execution.

Step19. Set I2C_CR.STO to 1, set I2C_CR.SI to 0, and the bus tries to send a Stop signal.

7.5.3 Slave Sending Example

Procedure

Step1. Refer to the relevant description of the port digital multiplexing function in the "General-Purpose I/O (GPIO)" chapter. Map SCL and SDA to the required pins; and configure the SCL and SDA pins to the open-drain output mode.

Step2. Set SYSCTRL module register PERI_CLKEN0.I2Cx to 1 to enable the I2C working clock.

Step3. Write 0 and 1 to SYSCTRL module register PERI_RESET0.I2Cx in sequence to reset the I2C module.

Step4. Set I2C_CR.ENS to 1 to enable the I2C module.

Step5. Configure I2C_ADDRx as the slave address.

Step6. Set I2C_CR.AA to 1 to enable the acknowledge flag.

Step7. Wait for I2C_CR.SI to become 1 and be addressed by SLA+R;

Step8. Query I2C_STAT, if the value of this register is 0xA8, continue to the next step, otherwise, perform error handling.

Step9. Write the data to be sent to I2C_DATA, set I2C_CR.SI to 0, and send the data.

Step10. Wait for I2C_CR.SI to become 1, the data has been sent to the bus.

Step11. Query I2C_STAT, if the value of this register is 0xB8 or 0xC0, continue to the next step, otherwise, perform error handling.

Step12. If the data to be sent is not completed, then jump to step9 to continue execution.

Step13. Set I2C_CR.AA to 0 and set I2C_CR.SI to 0.

7.5.4 Slave Receiving Example

Procedure

Step1. Refer to the relevant description of the port digital multiplexing function in the "General-Purpose I/O (GPIO)" chapter. Map SCL and SDA to the required pins; and configure the SCL and SDA pins to the open-drain output mode.

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Step2. Set SYSCTRL module register PERI_CLKEN0.I2Cx to 1 to enable the I2C working clock.

Step3. Write 0 and 1 to SYSCTRL module register PERI_RESET0.I2Cx in sequence to reset the I2C module.

Step4. Set I2C_CR.ENS to 1 to enable the I2C module.

Step5. Configure I2C_ADDRx as the slave address.

Step6. Set I2C_CR.AA to 1 to enable the acknowledge flag.

Step7. Wait for I2C_CR.SI to become 1 and be addressed by SLA+W.

Step8. Query I2C_STAT, if the register value is 0x60, continue to the next step, otherwise, perform error handling.

Step9. Set I2C_CR.SI to 0, the master sends data, and the slave returns ACK or NACK according to I2C_CR.AA.

Step10. Wait for I2C_CR.SI to become 1, read the received data from I2C_DATA.

Step11. Query I2C_STAT, if the register value is 0x80, continue to the next step, otherwise, perform error handling.

Step12. If the data to be received is not completed, jump to step9 to continue execution.

Step13. Set I2C_CR.AA to 0 and set I2C_CR.SI to 0.

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7.6 Register Description

7.6.1 Register List

- I2C0 base address: 0x40000400
- I2C1 base address: 0x40004400

Table 7-3 I2C Bus (I2C) Register Offset

Offset	Register	Description	Width
0x00	I2C_TMRUN	I2C Baud Rate Generator Enable Register	32
0x04	I2C_TM	I2C Baud Rate Counter Configuration Register	32
0x08	I2C_CR	I2C Configuration Register	32
0x0C	I2C_DATA	I2C Data Register	32
0x14	I2C_STAT	I2C Status Register	32
0x10	I2C_ADDR0	I2C Slave Address Register 0	32
0x20	I2C_ADDR1	I2C Slave Address Register 1	32
0x24	I2C_ADDR2	I2C Slave Address Register 2	32
0x28	I2C_MATCH	I2C Slave Address Match Register	32

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7.6.2 Baud Rate Generator Enable Register (I2C_TMRUN)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																														TME	
Access																															RW	

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-
0	TME	Baud rate generator enable control ● 0b0: Disable ● 0b1: Enable	RW

7.6.3 Baud Rate Counter Configuration Register (I2C_TM)

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								TM							
Access																									RW							

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7:0	TM	I2C bus SCL baud rate configuration $f_{SCL}= f_{PCLK}/8/(TM+1)$, and TM>0	RW

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7.6.4 Configuration Register (I2C_CR)

Offset	Bit Position																													
0x08	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																									ENS	STA	STO	SI	AA	Reserved	H1M
Access																										RW	RW	RW	RW	RW		RW

Bit	Name	Description	Access
31:7	*Reserved*	-	-
6	ENS	Module enable control ● 0b0: Disable ● 0b1: Enable	RW
5	STA	Bus state control ● 0b0: No function ● 0b1: Send START to the bus **Note** User program should set this bit to 0 after START transmission is completed.	RW
4	STO	Bus state control ● 0b0: No function ● 0b1: Send STOP to the bus **Note** The hardware automatically sets this bit to 0 after the STOP transmission is completed.	RW
3	SI	I2C interrupt flag Writing 0 clears the I2C interrupt flag and makes the state machine to perform the next action; writing 1 has no effect on the value of this bit. Read: ● 0b0: No I2C interrupt occurred ● 0b1: I2C interrupt has occurred	RW
2	AA	Acknowledge control ● 0b0: Send NAK during the acknowledge phase ● 0b1: Send ACK during the acknowledge phase	RW
1	*Reserved*	-	-

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Bit	Name	Description	Access
0	H1M	I2C filter parameter configuration ● 0b0: advanced filtering, higher anti-interference performance ● 0b1: simple filtering, faster communication rate **Note** For related functions, please refer to the input filter.	RW

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7.6.5 Data Register (I2C_DATA)

Offset	Bit Position																													
0x0C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								DAT							
Access																									RW							

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7:0	DAT	Data register ● In send mode, write the data to be sent ● In receive mode, read out received data	RW

7.6.6 Status Register (I2C_STAT)

Offset	Bit Position																													
0x14	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000000F8																															
Name	Reserved																								STAT							
Access																									RO							

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7:0	STAT	I2C state register For the specific definitions of status codes, please refer to the Status Code Expression.	RO

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7.6.7 Slave Address Register 0 (I2C_ADDR0)

Offset	Bit Position																													
0x10	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								ADDR0							GC
Access																									RW							RW

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7:1	ADDR0	I2C slave mode address 0	RW
0	GC	Broadcast address acknowledgment enable ● 0b0: Disable ● 0b1: Enable	RW

7.6.8 Slave Address Register 1 (I2C_ADDR1)

Offset	Bit Position																													
0x20	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								ADDR1							Reserved
Access																									RW							

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7:1	ADDR1	I2C slave mode address 1	RW
0	*Reserved*	-	-

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7.6.9 Slave Address Register 2 (I2C_ADDR2)

Offset	Bit Position																													
0x24	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								ADDR2							Reserved
Access																									RW							

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7:1	ADDR2	I2C slave mode address 2	RW
0	*Reserved*	-	-

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7.6.10 Slave Address Match Register (I2C_MATCH)

Offset	Bit Position																													
0x28	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																													AD2F	AD1F	AD0F
Access																														RO	RO	RO

Bit	Name	Functional Description	Access
31:3	*Reserved*	-	-
2	AD2F	I2C slave mode address 2 match flag bit ● 0b0: The device address received from the bus is not the same as ADDR2 ● 0b1: The device address received from the bus is the same as ADDR2	RO
1	AD1F	I2C slave mode address 1 match flag bit ● 0b0: The device address received from the bus is not the same as ADDR1 ● 0b1: The device address received from the bus is the same as ADDR1	RO
0	AD0F	I2C slave mode address 0 match flag bit ● 0b0: The device address received from the bus is not the same as ADDR0 ● 0b1: The device address received from the bus is the same as ADDR0	RO

Note

The address match flag bit will be cleared under the following conditions:

- When the module is reset
- When the START/STOP is sent
- When the STOP is generated internally by the slave.

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8 SPI

8.1 Introduction

The SPI interface is a synchronous serial data communication interface operating in full-duplex mode, using the following pins for communication: MISO, MOSI, SCK, and CS/NSS. In a single-master system, when SPI operates as the master, it controls the communication process by outputting CS and SCK signals. In a multi-master, multi-slave system, when SPI functions as a master, it needs to use NSS to detect the bus status, while the master that has acquired the bus controls the communication process by outputting CS and SCK signals. Whether in a single-master or multi-master system, when SPI operates as a slave, communication is carried out under the control of NSS and SCK signals.

8.2 Features

The serial peripheral interface mainly supports the following features:

- Support SPI master mode, SPI slave mode
- Support standard four-wire full-duplex communication
- Support configuration of serial clock polarity and phase
- The maximum division factor in master mode is PCLK/2
- The maximum division factor in slave mode is PCLK/4
- Set the frame length to 8 bits
- Support DMA hardware transmission handshake

8.3 Functional Description

8.3.1 Master Mode

The length of each data frame is fixed at 8 bits, and the first bit of sent data is fixed at MSB. Set SPI_CR.MSTR to 1, then the SPI interface works in master mode. Write data into the SPI_DATA register to start SPI transmission, and the SCK pin will automatically generate a serial clock; on the edge of the serial clock, the data in the shift register is sent to the MOSI pin, and the data on the MISO pin is received into the shift register.

The output frequency of the SCK pin is controlled by SPI_CR[SPR2:SPR0], with a range from PCLK/2 to PCLK/128.

The CS signal output can be controlled by either hardware or software:

- When using hardware control, the SPI_SSN.SSN to control the CS pin to output the corresponding logic level.
- When using software control, GPIOs can be flexibly selected, and the GPIO controller is used to control the output level of the selected pin to achieve chip selection for the slave device.

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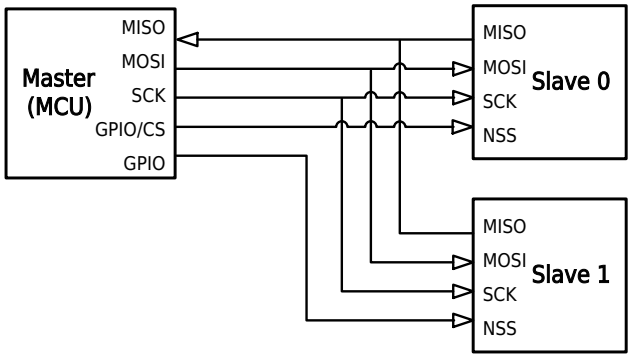

Figure 8-1 Typical Application Block Diagram of SPI Master Mode

The communication diagram for master mode is as follows, with CPOL=0 and CPHA=0.

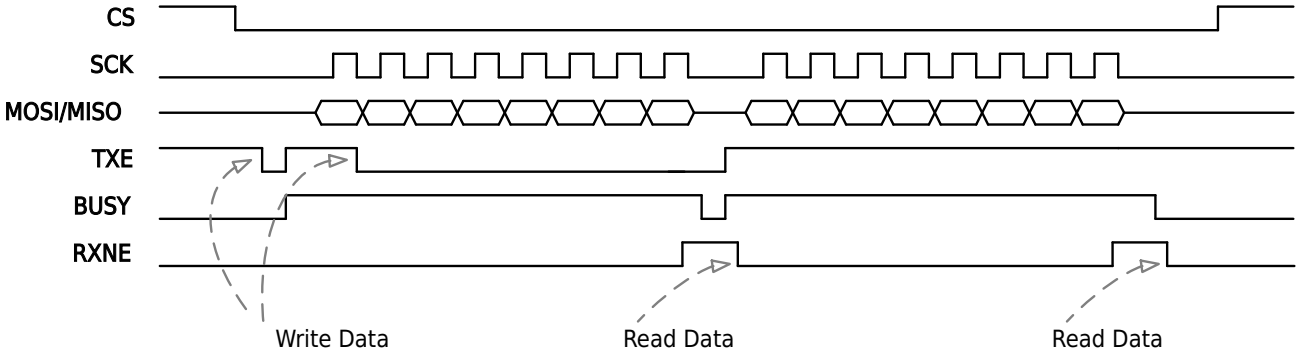

Figure 8-2 SPI Master Mode Communication Diagram

8.3.2 Slave Mode

The length of each data frame is fixed at 8 bits, and the first bit of received data is fixed at MSB. Set SPI_CR.MSTR to 0, and the SPI interface works in slave mode. In this mode, the SCK pin is used as an input pin and the serial clock comes from an external master; NSS pin is used as an input pin and the chip select signal comes from an external master or is fixed at low level. For more NSS pin information, see the "auxiliary registers" section in the chapter "General-Purpose I/O (GPIO)".

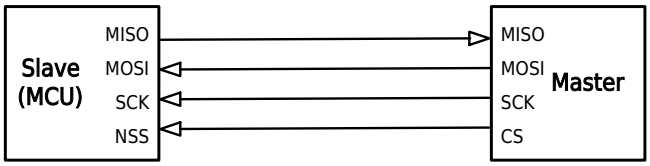

Figure 8-3 Typical Application Block Diagram of SPI Slave Mode

When the SPI slave receives a byte of data from the SPI master, the RXNE bit will be set high; the user program should read the received data as soon as possible. The communication timing of receiving data in slave mode is as follows, where CPOL=0, CPHA=0.

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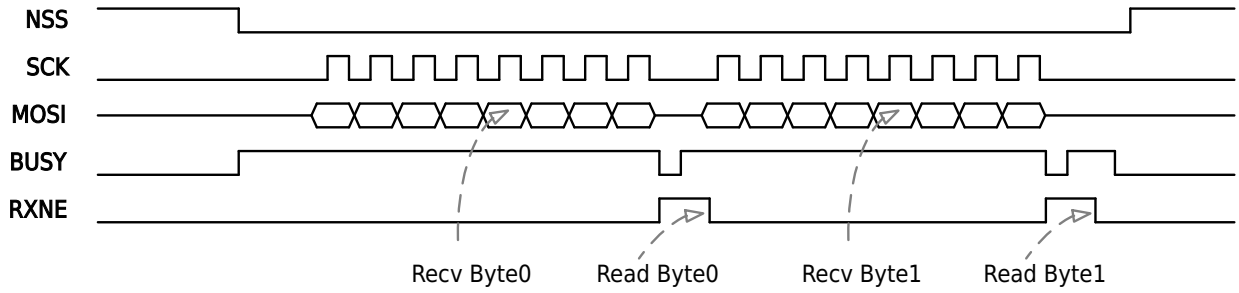

Figure 8-4 SPI Slave Mode Communication Diagram (Reception)

When the SPI slave needs to send data to the master, the following steps should be performed sequentially before the master pulls the slave NSS low:

1. Set SYSCTRL module register PERI_RESET0.SPIx bit to 0;
2. Set SYSCTRL module register PERI_RESET0.SPIx bit to 1;
3. Configure the SPI communication parameters and write the first byte of data to be transmitted into the SPI_DATA register;
4. After NSS is pulled low, before the arrival of SCK, write the second byte of data to be transmitted into the SPI_DATA register (the master must ensure that after pulling the slave NSS low, it waits at least 16 slave system clock cycles before sending SCK to the slave);
5. Whenever the TXE flag is set to 1, subsequent data to be transmitted should be promptly written into the SPI_DATA register.

The communication timing of sending data in slave mode is as follows, where CPOL=0, CPHA=0.

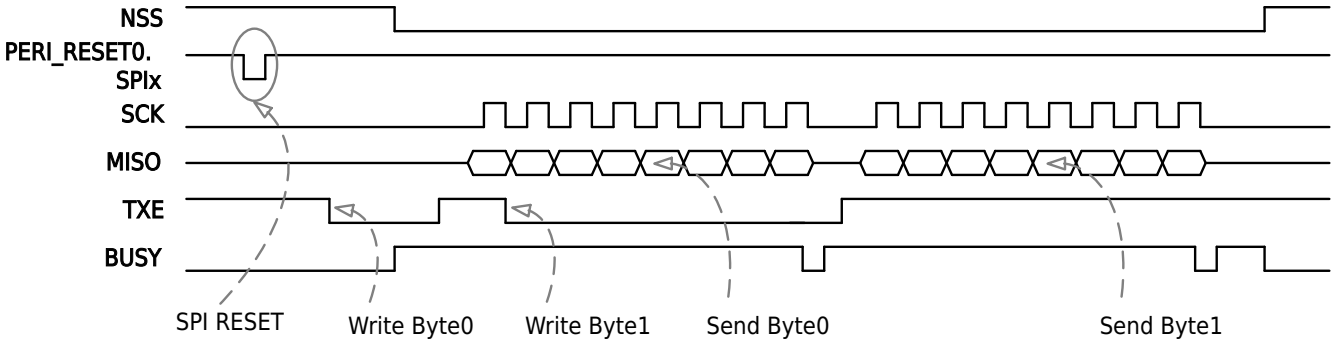

Figure 8-5 SPI Slave Mode Communication Diagram (Transmission)

8.3.3 Data Frame Format

The SPI interface frame format depends on the configuration of clock polarity bit CPOL and clock phase bit CPHA.

When CPOL is 0, the idle state of SCK line is low. When CPOL is 1, the idle state of SCK line is high level. When CPHA is 0, the data will be sampled when the first SCK clock transition signal jumps. When CPHA is 1, the data will be sampled when the second SCK clock signal jumps.

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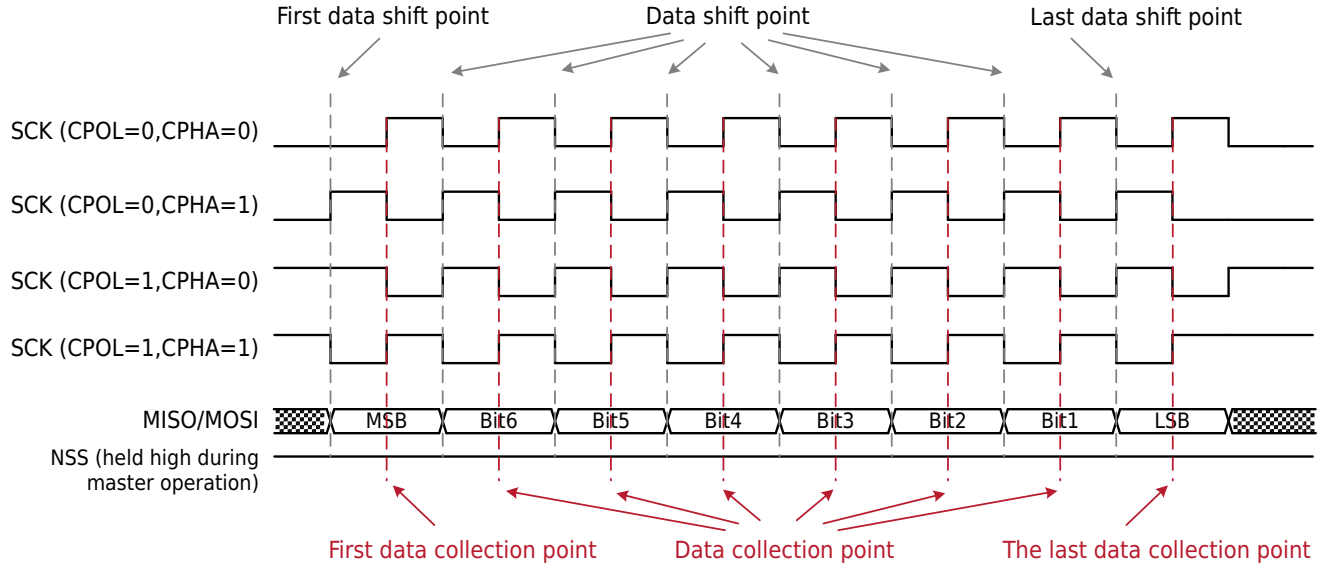

Figure 8-6 SPI Interface Master Mode Frame Format

SPI interface slave mode frame format:

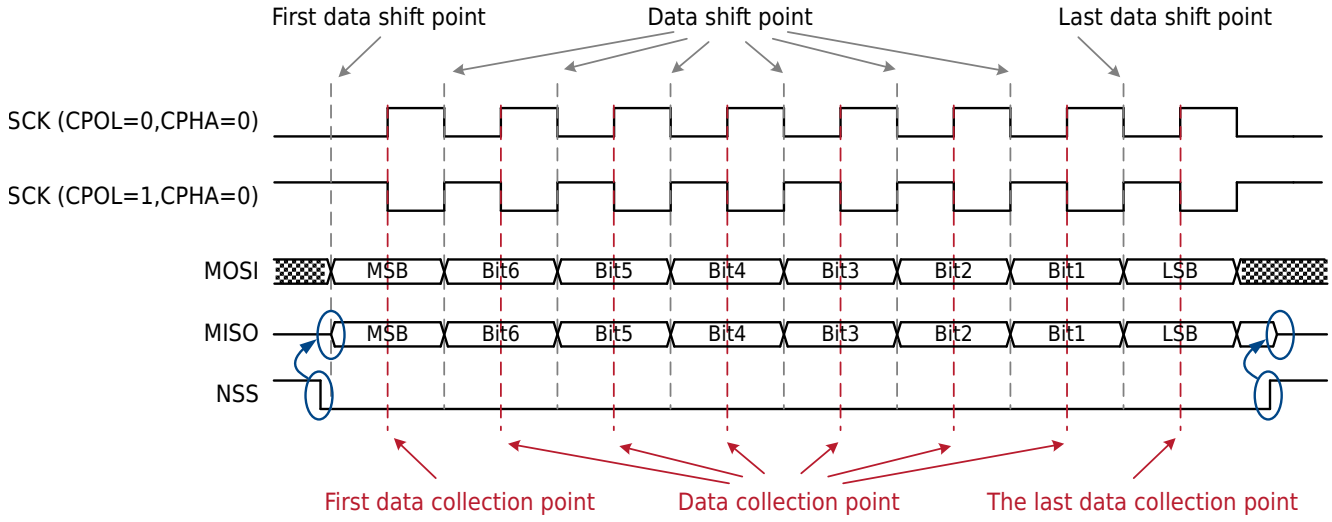

Figure 8-7 SPI Interface Slave Mode Data Frame Format when CPHA is 0

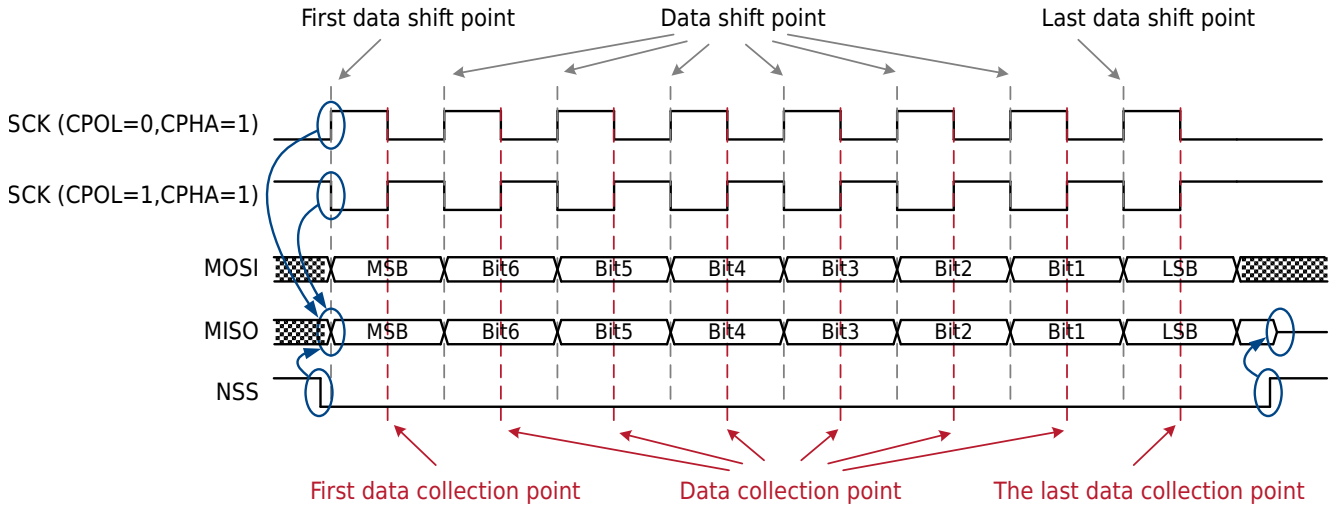

Figure 8-8 SPI Interface Slave Mode Data Frame Format when CHPA is 1

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8.3.4 Status Flags and Interrupt

SPI will generate the following four status flags during work, and the generation conditions and clearing methods are as follows.

- When the data in the send buffer (SPI_DATA) is transferred to the send shift register, SPI_STAT.TXE will be set by hardware, indicating that the send buffer is empty and the next data can be written. Writing data to SPI_DATA clears this flag bit.
- When the data in the receiving shift register is transferred to the receiving buffer (SPI_DATA), SPI_STAT.RXNE will be set by hardware, indicating that the receiving buffer is not empty, and the user needs to read the data as soon as possible. Reading data from SPI_DATA clears this flag bit.
- When the SPI operates as a master in a multi-master, multi-slave system and the external NSS input is low level, SPI_STAT.MDF is set by hardware, indicating that another SPI master is occupying the bus. When the NSS input is high level, SPI_STAT.MDF will be automatically cleared by hardware.
- When the SPI works in slave mode, if the NSS pin is pulled high during data transmission, SPI_STAT.SSERR will be set. Set SPI_CR.SPEN to 0 to clear this flag.

If the SPI interrupt control bit is enabled (SPI_CR2.INT_EN=1), any of the following three conditions can trigger an interrupt:

- SPI_CR2.TXEIE=1 and SPI_STAT.TXE=1 (i.e., the SPI transmit buffer is empty)
- SPI_CR2.RXNEIE=1 and SPI_STAT.RXNE=1 (i.e., the SPI receive buffer is not empty)
- SPI master mode is wrong, that is, SPI_STAT.MDF is 1

In the interrupt service routine, it is necessary to write 0x00 to SPI_ICLR to clear the internal interrupt flag.

8.3.5 Multi-machine System Configuration Description

- When the SPI module operates as a master in a single-master system, the slave can be controlled via either the SPI_CS pin or a GPIO pin. When the SPI_CS pin is selected as the slave select signal, setting SPI_SSN.SSN to 0 selects the slave, and setting SPI_SSN.SSN to 1 deselects the slave. When a GPIO pin is used as the chip select signal for the slave, driving the pin low selects the slave, while driving it high releases the slave.
- When the SPI module operates as a slave, configure the source of SPIx NSS as needed (refer to the auxiliary register descriptions in the chapter "General-Purpose I/O (GPIO)"). When the NSS input is low, the device enters the selected state and can communicate; when the NSS input is high, the device is in the unselected state.
- When the SPI operates in a multi-master, multi-slave system, all slave chip select signals are connected through the master's GPIO pins. The NSS signals of all masters must be connected to the GPIO pins of other masters to monitor whether the bus is occupied. After the slave finishes transmitting the last byte, software needs to switch the slave's MISO pin to digital input with pull-up. When the NSS of the slave is pulled low, the pin should be reconfigured as a MISO pin.

  The communication procedure for Master0 shown in the figure below is as follows:

  1. Wait for Master0 NSS input to go high;
  2. Drive GPIO0 low to notify Master1 that it intends to occupy the SPI bus;
  3. Drive GPIO2 low to select Slave1;
  4. Communicate with Slave1;
  5. Drive GPIO2 high to release Slave1;
  6. Drive GPIO0 high to notify Master1 that the SPI bus has been released.

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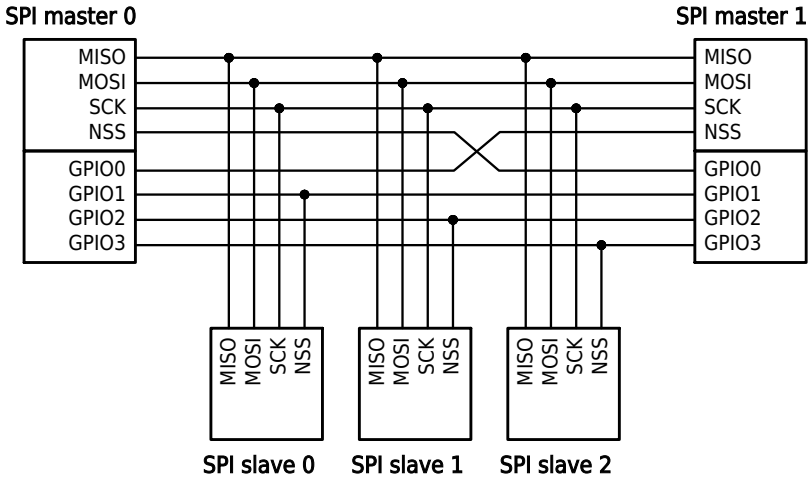

Figure 8-9 SPI Multi-master/Multi-slave System Diagram

8.3.6 Pin Configuration Description

SPI can maintain some or all functions under some special pin configurations. The specific situation is as follows ("✔" means that the pin is configured and used, and "✖" means that the pin is not configured):

Table 8-1 SPI Pin Configuration Description List

	SPI_CS (Master)/SPIxNSS (Slave)	SCK	MOSI	MISO	Function Description
Master Mode	✔	✔	✔	✔	All masters are generally configured to function properly.
	✖	✔	✔	✔	All Masters function normally
	✔	✔	✔	✖	Master sending function is normal
	✔	✔	✖	✔	Master receiving function is normal
	✖	✔	✔	✖	Master sending function is normal
	✖	✔	✖	✔	Master receiving function is normal
Slave Mode	✔	✔	✔	✔	All slaves are generally configured to function properly.
	✔	✔	✔	✖	Slave receiving function is normal
	✔	✔	✖	✔	Slave sending function is normal
	✔ fixed low level	✔	✔	✔	All slaves function normally
	✔ fixed low level	✔	✔	✖	Slave receiving function is normal
	✔ fixed low level	✔	✖	✔	Slave sending function is normal

Note

- Conditions not listed in the table are currently not supported.
- In master mode, even if the SPI_CS chip select output is not used, the SPI_SSN.SSN must still be configured. When the bus is idle, SPI_SSN.SSN must remain at 1; when data transmission is to occur, it must be set to 0, and it should remain 0 during the data transfer.
- In slave mode and chip select input is fixed at low level, in order to maintain normal function, SPI_CR.CPHA=1 must be satisfied.

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8.4 Operation Example

8.4.1 Master Sending Example

Procedure

Step1. Refer to the relevant descriptions of the pin digital multiplexing function in "General-Purpose I/O (GPIO)" to map CS/SCK/MISO/MOSI to the required pins; configure the CS, SCK, and MOSI pins as outputs, and configure the MISO pin as an input.

Step2. Set SPI_CR.MSTR to 1 to make SPI work in master mode.

Step3. Configure SPI_CR[SPR2:SPR0] to make the clock rate of SCK output meet the application requirements.

Step4. Configure SPI_CR.CPOL and SPI_CR.CPHA to make the data frame format meet the application requirements.

Step5. Set SPI_CR.SPEN to 1 to enable the SPI interface.

Step6. Set SPI_SSN.SSN to 0, thus make the CS pin output low level to select the slave.

Step7. When SPI_STAT.TXE is 1, write the data to be sent to SPI_DATA as soon as possible.

Step8. If the data to be sent is not completed, then jump to step7 to continue execution.

Step9. The query waits for SPI_STAT.TXE to become 1, and the last byte data has been sent.

Step10. Query and wait for SPI_STAT.BUSY to become 0, the SPI bus is idle.

Step11. Set SPI_SSN.SSN to 1, make the CS pin output high level to release the slave.

Note

- GPIO can be used instead of CS to realize chip select output, which is mostly used in multi-machine communication system.
- During the transmission process, SPI_SSN.SSN must be set to 0; after the transmission is complete, SPI_SSN.SSN must be set to 1.

8.4.2 Master Receiving Example

Procedure

Step1. Refer to the relevant descriptions of the pin digital multiplexing function in "General-Purpose I/O (GPIO)" to map CS/SCK/MISO/MOSI to the required pins; configure the CS, SCK, and MOSI pins as outputs, and configure the MISO pin as an input.

Step2. Set SPI_CR.MSTR to 1 to make SPI work in master mode.

Step3. Configure SPI_CR[SPR2:SPR0] to make the clock rate of SCK output meet the application requirements.

Step4. Configure SPI_CR.CPOL and SPI_CR.CPHA to make the data frame format meet the application requirements.

Step5. Set SPI_CR.SPEN to 1 to enable the SPI interface.

Step6. Set SPI_SSN.SSN to 0, thus make the CS pin output low level to select the slave.

Step7. Write arbitrary data to SPI_DATA to trigger the master to send SCK.

Step8. Query and wait for SPI_STAT.RXNE to become 1, and the data sent by the slave has been received.

Step9. Read the received data from SPI_DATA.

Step10. If the data to be received is not completed, jump to step7 to continue execution.

Step11. Set SPI_SSN.SSN to 1, make the CS pin output high level to release the slave.

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Note

- GPIO can be used instead of CS to realize chip select output, which is mostly used in multi-machine communication system.
- During the transmission process, SPI_SSN.SSN must be set to 0; after the transmission is complete, SPI_SSN.SSN must be set to 1.

8.4.3 Slave Sending Example

Context

Whenever the SPI slave needs to send data, it needs to start the initialization operation and sending operation from Step 2.

Procedure

Step1. Refer to the relevant descriptions of the pin digital multiplexing function in "General-Purpose I/O (GPIO)" to map NSS/SCK/MISO/MOSI to the required pins; configure the NSS/SCK/MOSI pins as inputs, and configure the MISO pin as an output. For NSS pin source configuration, please refer to the auxiliary register descriptions in the chapter "General-Purpose I/O (GPIO)".

Step2. Set SYSCTRL module register PERI_RESET0.SPIx to 0, so that the SPI module is in reset state.

Step3. Set SYSCTRL module register PERI_RESET0.SPIx to 1 to make the SPI module operational.

Step4. Set SPI_CR.MSTR to 0 to make SPI work in slave mode.

Step5. Configure SPI_CR.CPOL and SPI_CR.CPHA to make the data frame format meet the application requirements.

Step6. Set SPI_CR.SPEN to 1 to enable the SPI interface.

Step7. Write the first byte data to be sent into SPI_DATA.

Step8. After detecting that the NSS pin has been pulled low, the slave must immediately write the second byte of data to be transmitted into the SPI_DATA register before the arrival of SCK (the master must ensure that after NSS pulling the low, it waits at least 16 slave system clock cycles before sending SCK to the slave).

Step9. Whenever the SPI_STAT.TXE flag is set to 1, subsequent data to be transmitted should be promptly written into the SPI_DATA register.

Step10. When it is found that the NSS pin is low and the data to be sent has not been completed, jump to step9.

Step11. The query waits for the NSS pin to be pulled high, and the master releases the SPI slave.

8.4.4 Slave Receiving Example

Procedure

Step1. Refer to the relevant descriptions of the pin digital multiplexing function in "General-Purpose I/O (GPIO)" to map NSS/SCK/MISO/MOSI to the required pins; configure the NSS/SCK/MOSI pins as inputs, and configure the MISO pin as an output. NSS pin source configuration, please refer to the auxiliary register descriptions in chapter "General-Purpose I/O (GPIO)".

Step2. Set SPI_CR.MSTR to 0 to make SPI work in slave mode.

Step3. Configure SPI_CR.CPOL and SPI_CR.CPHA to make the data frame format meet the application requirements.

Step4. Set SPI_CR.SPEN to 1 to enable the SPI interface.

Step5. The query waits for the NSS pin to be pulled low, and the master selects the SPI slave.

Step6. Query and wait for SPI_STAT.RXNE to become 1, and the data sent by the master been received.

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Step7. Read the received data from SPI_DATA.

Step8. If the data to be received is not completed, jump to step6 to continue execution.

Step9. The query waits for the NSS pin to be pulled high, and the master releases the SPI slave.

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8.5 Register Description

8.5.1 Register List

- SPI0 base address: 0x40000800
- SPI1 base address: 0x40004800

Table 8-2 Serial Peripheral Interface (SPI) Register Offset

Offset	Register	Description
0x00	SPI_CR	SPI Configuration Register
0x04	SPI_SSN	SPI Chip Select Configuration Register
0x08	SPI_STAT	SPI Status Register
0x0C	SPI_DATA	SPI Data Register
0x10	SPI_CR2	SPI Configuration Register 2
0x14	SPI_ICLR	SPI Interrupt Clear Register

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8.5.2 SPI Configuration Register (SPI_CR)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000014																															
Name	Reserved																								SPR2	SPEN	Reserved	MSTR	CPOL	CPHA	SPR1	SPR0
Access																									RW	RW		RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7	SPR2	Master mode baud rate selection Parameter selection details (See table below)	RW
6	SPEN	SPI module enable control ● 0b0: Disable ● 0b1: Enable	RW
5	*Reserved*	-	-
4	MSTR	SPI working mode configuration ● 0b0: Slave mode ● 0b1: Master mode	RW
3	CPOL	SCK line idle state configuration ● 0b0: Low level ● 0b1: High level	RW
2	CPHA	Clock phase configuration ● 0b0: Sample on the first edge ● 0b1: Sample on the second edge	RW
1	SPR1	Master mode baud rate selection Parameter selection details (See table below)	RW
0	SPR0	Master mode baud rate selection Parameter selection details (See table below)	RW

Table 8-5 SPI Master Mode Baud Rate Selection

SPR2	SPR1	SPR0	SCK Rate
0b0	0b0	0b0	PCLK/2
0b0	0b0	0b1	PCLK/4
0b0	0b1	0b0	PCLK/8
0b0	0b1	0b1	PCLK/16
0b1	0b0	0b0	PCLK/32
0b1	0b0	0b1	PCLK/64

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SPR2	SPR1	SPR0	SCK Rate
0b1	0b1	0b0	PCLK/128
0b1	0b1	0b1	Reserved

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8.5.3 SPI Chip Select Configuration Register (SPI_SSN)

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000000FF																															
Name	Reserved																															SSN
Access																																RW

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-
0	SSN	SPI_CS output level configuration in master mode ● 0b0: SPI_CS pin outputs a low level ● 0b1: SPI_CS pin outputs a high level	RW

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8.5.4 SPI Status Register (SPI_STAT)

Offset	Bit Position																													
0x08	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000004																															
Name	Reserved																								SPIF	Reserved	SSERR	MDF	BUSY	TXE	RXNE	Reserved
Access																									RO		RO	RO	RO	RO	RO	

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7	SPIF	Receive completion flag ● 0b0: Receiving in progress ● 0b1: A byte has been received from the SPI bus.	RO
6	*Reserved*	-	-
5	SSERR	Slave mode NSS error flag	RO
4	MDF	In master mode, the conflict flag ● 0b0: NSS pin level is high ● 0b1: NSS pin level is low	RO
3	BUSY	SPI bus transfer status flag ● 0b0: SPI bus is idle. ● 0b1: SPI bus is transferring data.	RO
2	TXE	Transmit buffer status flag ● 0b0: Transmit buffer is not empty. ● 0b1: Transmit buffer is empty.	RO
1	RXNE	Receive buffer status flags ● 0b0: Receive buffer is empty. ● 0b1: Receive buffer is not empty.	RO
0	*Reserved*	-	-

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8.5.5 SPI Data Register (SPI_DATA)

Offset	Bit Position																													
0x0C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								DAT							
Access																									RW							

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7:0	DAT	Data register ● In send mode, write the byte to be sent to this register; ● In receive mode, the received byte is read from this register;	RW

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8.5.6 SPI Configuration Register 2 (SPI_CR2)

Offset	Bit Position																													
0x10	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000003																															
Name	Reserved																									RXNEIE	TXEIE	HDMA_TX	HDMA_RX	INT_EN	Reserved	
Access																										RW	RW	RW	RW	RW		

Bit	Name	Functional Description	Access
31:7	*Reserved*	-	-
6	RXNEIE	Receive buffer not empty interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
5	TXEIE	Transmit buffer empty interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
4	HDMA_TX	DMA hardware access transmit enable ● 0b0: Disable ● 0b1: Enable	RW
3	HDMA_RX	DMA hardware access receive enable ● 0b0: Disable ● 0b1: Enable	RW
2	INT_EN	SPI interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
1:0	*Reserved*	-	-

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8.5.7 SPI Interrupt Clear Register (SPI_ICLR)

Offset	Bit Position																													
0x14	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000000FF																															
Name	Reserved																															INT_CLR
Access																																WO

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-
0	INT_CLR	SPI interrupt clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO

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9 CLKTRIM

9.1 Introduction

The CLKTRIM (Clock Trimming) module is a circuit specially used to calibrate/monitor the clock. In the calibration mode, select an accurate clock source to calibrate the inaccurate clock source, repeat the calibration, and adjust the parameters of the inaccurate clock source until the frequency of the calibrated clock source meets the accuracy requirements. In the calibration mode, the count value will have a certain error, but it is within the allowable precision error range. In the monitoring mode, select a stable clock source to monitor the system's working clock. Under the set monitoring period, monitor whether the system's working clock is invalid and generate an interrupt. In the calibration mode and monitoring mode, the required clock sources must be initialized and enabled. For the specific configuration process, refer to the chapter "System Controller (SYSCTRL)" relevant description.

9.2 Features

CLKTRIM supports the following features:

- Calibration Mode
- Monitoring Mode
- 32-bit reference clock counter can be loaded with initial value
- 32-bit to-be-calibrated clock counter with configurable overflow value
- 6 reference clock sources
- 5 clock sources to be calibrated
- Support interrupt mode

9.3 Functional Description

9.3.1 Calibration Mode

Clock Calibration Principle

When calibrating a clock whose frequency is inaccurate but has parameter settings to adjust the frequency (the to-be-calibrated clock CAL_CLK), an accurate clock is required as the reference clock (REF_CLK). Set the calibration time T_{trim}, the to-be-calibrated clock frequency F_{cal}, and the reference clock frequency F_{ref}. Use both the to-be-calibrated clock and the reference clock for counting simultaneously, and stop counting when the calibration time ends.

Read the to-be-calibrated clock counter value M and the reference clock counter value N, yielding the equation: $T_{trim}=M/F_{cal}=N/F_{ref}$

Deriving $F_{cal}=F_{ref}*M/N$

Judging from the formula, the smaller the frequency error rate of the reference clock is, the smaller the error rate of the to-be-calibrated clock is.

After calculating the frequency of the to-be-calibrated clock, if the error rate exceeds the range required by the system, you can adjust the parameters of the to-be-calibrated clock, and then repeat the above steps to calibrate until the error rate of the to-be-calibrated clock frequency meets the system requirements.

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Clock Calibration Module Hardware Structure

The time calibration module offers 5 clock sources for the to-be-calibrated clock and 6 clock sources for the reference clock, as shown in the following diagram:

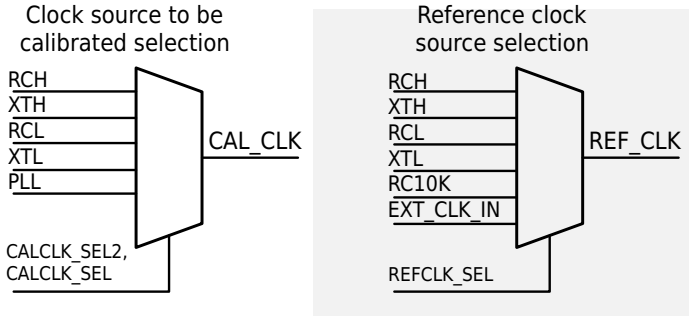

Figure 9-1 Clock Source Selection Diagram for Calibration Mode

The selection of the to-be-calibrated clock is configured by registers CLKTRIM_CR.CALCLK_SEL2 and CLKTRIM_CR.CALCLK_SEL. The reference clock selection is configured by register CLKTRIM_CR.REFCLK_SEL.

The clock calibration module contains two 32-bit counters:

- A down-counter with configurable initial value, clocked by the reference clock.

  The initial value is configured by register CLKTRIM_REFCON.RCNTVAL, and the counter value can be read from register CLKTRIM_REFCNT. When the counter decrements to 0, counting stops and an interrupt is generated.

- An up-counter with configurable overflow value, clocked by the to-be-calibrated clock.

  The overflow value is configured by register CLKTRIM_CALCON.CCNTVAL, and the counter value can be read from register CLKTRIM_CALCNT. When the counter increments to the overflow value, counting stops and an interrupt is generated.

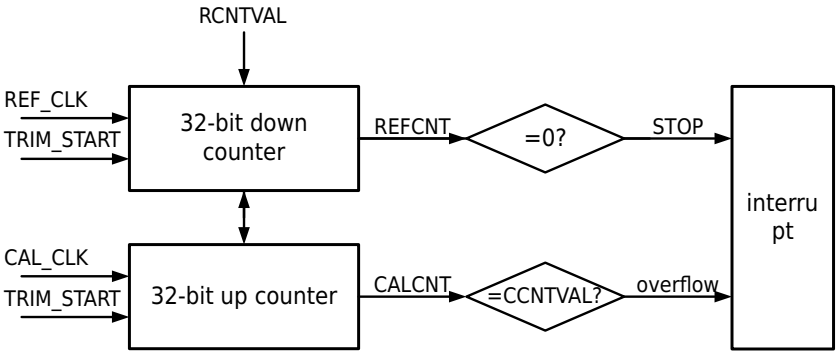

Figure 9-2 Clock Calibration Module Hardware Diagram

Clock Calibration Software Flow

The clock calibration steps are as follows:

Step1. Set register CLKTRIM_CR.REFCLK_SEL to select the reference clock.

Step2. Set register CLKTRIM_CR.CALCLK_SEL to select the to-be-calibrated clock.

Step3. Set register CLKTRIM_REFCON.RCNTVAL to define the calibration time.

Step4. Set register CLKTRIM_CR.IE to enable interrupts.

Step5. Set register CLKTRIM_CR.TRIM_START to initiate calibration.

Step6. The reference clock counter and the to-be-calibrated clock counter start counting.

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Step7. When the reference clock counter counts down from the initial value to 0, CLKTRIM_IFR.STOP is set to 1 and an interrupt is triggered.

Step8. The interrupt service subroutine judges that CLKTRIM_IFR.STOP is 1, reads the values of registers CLKTRIM_REFCNT and CLKTRIM_CALCNT,

Step9. Clear the CLKTRIM_CR.TRIM_START register to end the calibration.

Step10. Calculate the frequency of the clock to be calibrated using the formula described in the clock calibration principle, where M is the value of register CLKTRIM_CALCNT and N is the value of register CLKTRIM_REFCON.RCNTVAL.

If the frequency of the clock to be calibrated does not meet the error rate requirement, adjust its parameters and repeat steps 5-10 until the desired error tolerance is achieved.

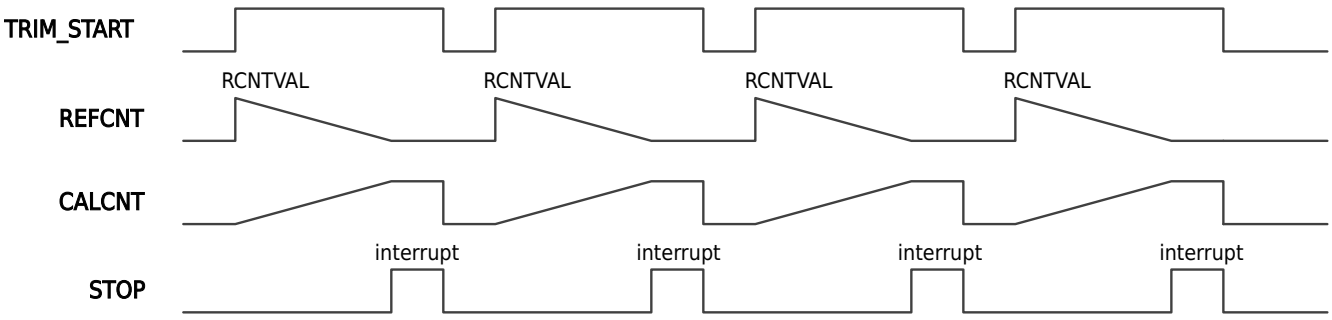

Figure 9-3 Clock Calibration Waveform Diagram

Note: During calibration, if the calibration time is set too long, the to-be-calibrated clock counter may overflow before CLKTRIM_IFR.STOP is set to 1. In this case, CLKTRIM_IFR.CALCNT_OF is set to 1, triggering an interrupt. When the interrupt service subroutine detects that CLKTRIM_IFR.CALCNT_OF is set to 1, it clears the CLKTRIM_CR.TRIM_START register to terminate calibration.

In this case, the calibration cannot be performed correctly, and the calibration time must be adjusted and re-calibrated. The operational steps are as follows:

Step1. Set register CLKTRIM_REFCON.RCNTVAL to adjust the calibration time.

Step2. Set register CLKTRIM_CR.TRIM_START to restart calibration.

9.3.2 Monitoring Mode

Clock Monitoring Principle

In order to monitor whether the system working clock (monitored clock CAL_CLK) is working normally, a stable clock is required as a reference clock (REF_CLK). Set the monitoring time T_{trim}, the monitored clock frequency F_{cal}, the reference clock frequency F_{ref}, the monitored clock counter overflow value CALVAL, use the monitored clock and the reference clock to count at the same time, stop counting when the monitoring time ends, and judge whether the monitored clock counter is in overflow state. If the monitored clock counter has overflowed, it means that the monitored clock works normally within the monitoring time, and the next monitoring is continued. If the counter of the monitored clock does not overflow, it means that the monitored clock is working abnormally within the monitoring time. The monitored clock may have stopped or the frequency has changed significantly, the monitored clock is abnormally interrupted, and the system working clock is switched by the hardware.

Clock Monitoring Hardware Structure

The time calibration module offers 3 clock sources for the monitored clock and 6 clock sources for the reference clock, as illustrated below:

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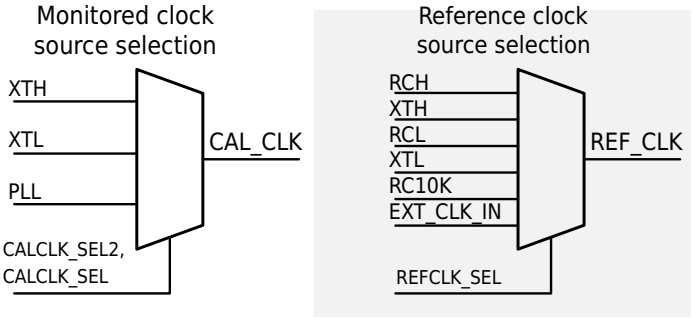

Figure 9-4 Clock Source Selection Diagram for Monitoring Mode

The monitored clock is configured via registers CLKTRIM_CR.CALCLK_SEL2 and CLKTRIM_CR.CALCLK_SEL, while the reference clock is configured by register CLKTRIM_CR.REFCLK_SEL.

Clock Monitoring Software Flow

The clock monitoring steps are as follows:

Step1. Set register CLKTRIM_CR.REFCLK_SEL to select the reference clock.

Step2. Set register CLKTRIM_CR.CALCLK_SEL to select the monitored clock.

Step3. Set register CLKTRIM_REFCON.RCNTVAL to define the monitoring interval time.

Step4. Set register CLKTRIM_CALCON.CCNTVAL to define the overflow time for the monitored clock counter.

Step5. Set register CLKTRIM_CR.MON_EN to enable the monitoring function.

Step6. Set register CLKTRIM_CR.IE to enable interrupts.

Step7. Set register CLKTRIM_CR.TRIM_START to initiate monitoring.

Step8. The reference clock counter and the monitored clock counter start counting.

Step9. When the reference clock counter reaches the monitoring interval time, CLKTRIM_IFR.STOP is set to 1, while simultaneously checking whether the monitored clock counter overflows (whether CLKTRIM_IFR.CALCNT_OF is set to 1). If overflow occurs (CLKTRIM_IFR.CALCNT_OF = 1), it indicates the monitored clock is functioning normally. If no overflow occurs (CLKTRIM_IFR.CALCNT_OF = 0), it indicates the monitored clock has failed, and CLK_FAULT (CLKTRIM_IFR.XTL_FAULT/XTH_FAULT) is set to 1, triggering an interrupt.

Step10. In the interrupt service subroutine, clear the interrupt flag CLK_FAULT (CLKTRIM_IFR.XTL_FAULT/XTH_FAULT) and reset the CLKTRIM_CR.TRIM_START register to terminate monitoring.

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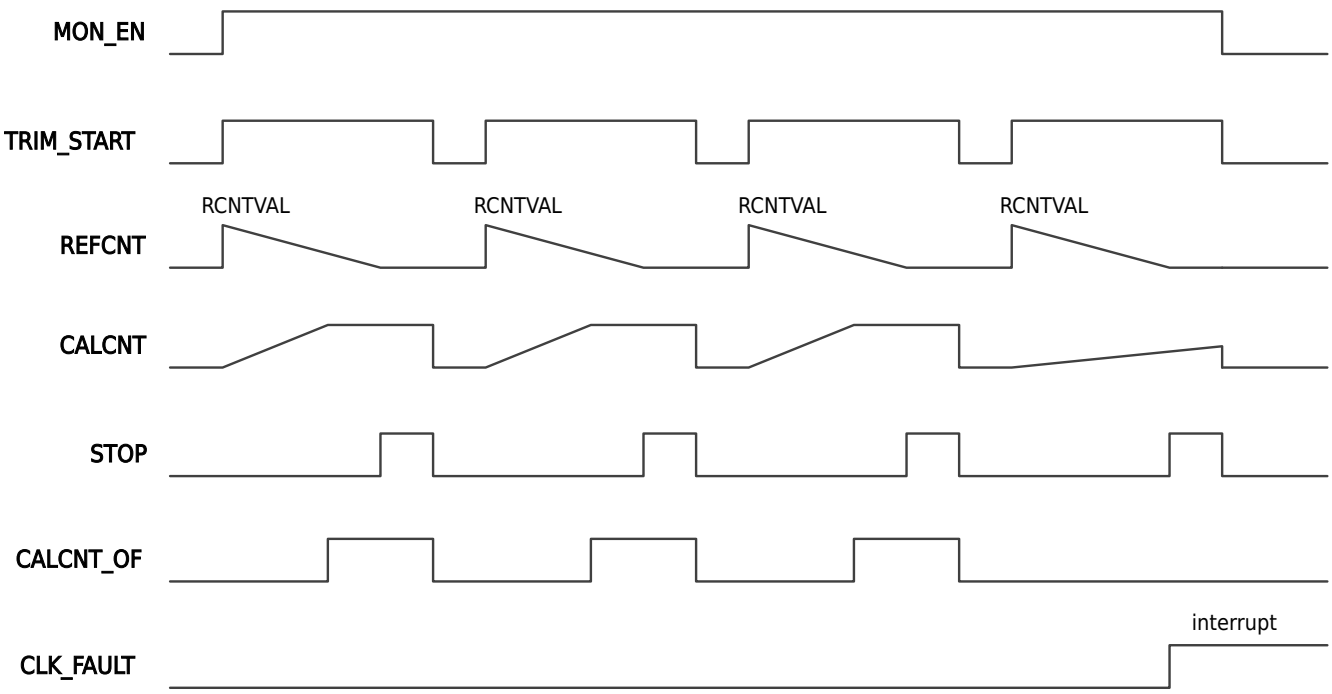

Figure 9-5 Clock Monitoring Waveform Diagram

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9.4 Register Description

9.4.1 Register List

Base address: 0x40001800

Table 9-1 Clock Trim Module (CLKTRIM) Register Offset

Offset	Register	Description	Width
0x00	CLKTRIM_CR	Configuration register	32
0x04	CLKTRIM_REFCON	Reference counter initial value configuration register	32
0x08	CLKTRIM_REFCNT	Reference counter value register	32
0x0C	CLKTRIM_CALCNT	Calibration counter value register	32
0x10	CLKTRIM_IFR	Interrupt flag register	32
0x14	CLKTRIM_ICLR	Interrupt flag clear register	32
0x18	CLKTRIM_CALCON	Calibration counter overflow value configuration register	32

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9.4.2 Configuration Register (CLKTRIM_CR)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																							CALCLK_SEL2	IE	MON_EN	CALCLK_SEL		REFCLK_SEL			TRIM_START
Access																								RW	RW	RW	RW		RW			RW

Bit	Name	Functional Description	Access
31:9	*Reserved*	-	-
8	CALCLK_SEL2	To-be-calibrated/monitored clock selection high register Parameter selection details (See Table Below)	RW
7	IE	Interrupt enable register ● 0b0: Disable ● 0b1: Enable	RW
6	MON_EN	Monitored mode enable register ● 0b0: Disable ● 0b1: Enable	RW
5:4	CALCLK_SEL	To-be-calibrated/monitored clock selection low register Parameter selection details (See Table Below)	RW
3:1	REFCLK_SEL	Reference clock select register ● 0b000: RCH ● 0b001: XTH ● 0b010: RCL ● 0b011: XTL ● 0b100: RC10K ● 0b101: EXT_CLK_IN	RW
0	TRIM_START	Calibration/monitoring start register ● 0b0: Stop ● 0b1: Start	RW

CALCLK_SEL2	CALCLK_SEL	To-Be-Calibrated/Monitored Clock
0b0	0b00	RCH
0b0	0b01	XTH
0b0	0b10	RCL
0b0	0b11	XTL
0b1	0b00	PLL
0b1	0b01-0b11	Reserved

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9.4.3 Reference Counter Initial Value Configuration Register (CLKTRIM_REFCON)

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	RCNTVAL																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	RCNTVAL	Reference counter initial value	RW

9.4.4 Reference Counter Value Register (CLKTRIM_REFCNT)

Offset	Bit Position																													
0x08	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFFFFFFFF																															
Name	REFCNT																															
Access	RO																															

Bit	Name	Functional Description	Access
31:0	REFCNT	Reference counter value	RO

9.4.5 Calibration Counter Value Register (CLKTRIM_CALCNT)

Offset	Bit Position																													
0x0C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	CALCNT																															
Access	RO																															

Bit	Name	Functional Description	Access
31:0	CALCNT	Calibration counter value	RO

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9.4.6 Interrupt Flag Register (CLKTRIM_IFR)

Offset	Bit Position																													
0x10	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																											PLL_FAULT	XTH_FAULT	XTL_FAULT	CALCNT_OF	STOP
Access																												RO	RO	RO	RO	RO

Bit	Name	Functional Description	Access
31:5	*Reserved*	-	-
4	PLL_FAULT	PLL failure flag	RO
3	XTH_FAULT	XTH failure flag	RO
2	XTL_FAULT	XTL failure flag	RO
1	CALCNT_OF	Calibration counter overflow flag CLKTRIM_CR. START write zero to clear this flag bit	RO
0	STOP	Reference counter stop flag CLKTRIM_CR. START write zero to clear this flag bit	RO

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9.4.7 Interrupt Flag Clear Register (CLKTRIM_ICLR)

Offset	Bit Position																													
0x14	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000000F																															
Name	Reserved																											PLL_FAULT_CLR	XTH_FAULT_CLR	XTL_FAULT_CLR	Reserved	
Access																												WO	WO	WO		

Bit	Name	Functional Description	Access
31:5	*Reserved*	-	-
4	PLL_FAULT_CLR	Clear PLL failure flag Write 0 to clear flag, write 1 has no effect; read always returns 0.	WO
3	XTH_FAULT_CLR	Clear XTH failure flag Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
2	XTL_FAULT_CLR	Clear XTL failure flag Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
1:0	*Reserved*	-	-

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9.4.8 Calibration Counter Overflow Value Configuration Register (CLKTRIM_CALCON)

Offset	Bit Position																													
0x18	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFFFFFFFF																															
Name	CCNTVAL																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	CCNTVAL	Calibration counter overflow value	RW

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10 CTRIM

10.1 Introduction

When the module works in calibration mode, it automatically performs real-time calibration of the RCH/RC48M/RCL output frequency, making the accuracy of the RCH/RC48M/RCL output frequency is no longer affected by environmental variations. When the module works in timer mode, it has general timing function and can still work normally under DeepSleep mode.

10.2 Features

The clock calibration supports the following features:

- Calibration mode: Supports RCH/RC48M/RCL automatic real-time calibration/single calibration
- Calibration mode: Multiple calibration steps, quickly approaching the target
- Timing mode: Can work in DeepSleep mode
- Timing mode: Supports automatic wake-up with a period range of 60μs to 65536s
- Timing mode: 8 clock signals available for selection
- Timing mode: Toggle output

10.3 Functional Description

10.3.1 RCH/RC48M Clock Calibration Mode

When CTRIM_CR1.MD is configured as 0b00, the module operates in RCH/RC48M calibration mode. This mode enables automatic real-time calibration of the output frequency of RCH/RC48M, ensuring the accuracy of RCH/RC48M remains unaffected by environmental variations. During calibrating RCH/RC48M, the module requires a precise low-frequency clock signal, which can be either the on-chip PCLK or an external input via the ETR pin.

Note

The RCLK frequency must be less than half of the frequency of RCH/RC48M.

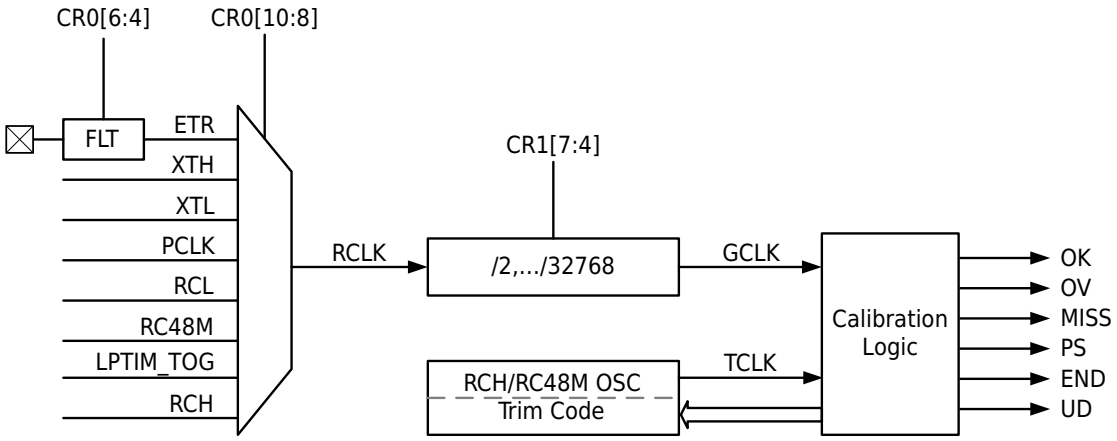

Figure 10-1 RCH/RC48M Clock Calibration Operational Block Diagram

When automatic calibration begins, the error counter performs down-counting on the TCLK signal (RCH/RC48M oscillation frequency) starting from CTRIM_ARR at each GCLK cycle, then switches to up-counting upon reaching zero. If the error counter value within a GCLK cycle is less than the CTRIM_FLIM register

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value, CTRIM_ISR.OK is set to flag that the output frequency of RCH/RC48M meets expectations. If the error counter value within a GCLK cycle is greater than the CTRIM_FLIM register value, the TrimCode of RCH/RC48M is automatically adjusted for the next counting cycle. The auto-adjustment rules are: If counting direction is down-counting, increase the TrimCode of RCH/RC48M by CTRIM_CR0.STEP; If counting direction is up-counting, decrease the TrimCode of RCH/RC48M by CTRIM_CR0.STEP. The calibration logic automatically reduces the value of CTRIM_CR0.STEP to achieve gradual convergence of the output frequency of RCH/RC48M toward the target value.

UD event is generated when the error counter count decrements to zero; MISS event is triggered when the error counter count increments to CTRIM_ARR, stopping further counting. Whenever the rising edge of GCLK arrives, the error counter starts counting again.

- **RCH/RC48M Single Calibration**

  Set CTRIM_CR1.MDRCH to 0b00 for single calibration of RC48M, then configure appropriate STEP, initial value, and FLIM using the same method as above.

  Set CTRIM_CR1.MDRCH to 0b01 for single calibration of RCH, then configure appropriate STEP, initial value, and FLIM using the same method as above.

- **Coarse and Fine Calibration of RC48M Separately**
  - Coarse calibration

    Set CTRIM_CR1.MDRCH to 0b10 to calibrate the RC48M 8bits coarse tuning, following the same method as above. After calibration is complete, write the TVAL value to RC48M_CR.TRIMC.
  - Fine calibration

    Set CTRIM_CR1.MDRCH to 0b11 to calibrate the RC48M 6bits fine tuning, following the same method as above. After calibration is complete, write the TVAL value to RC48M_CR.TRIMF.

10.3.2 RCL Clock Calibration Mode

When CTRIM_CR1.MD is set to 0b01, the module operates in RCL calibration mode. This mode can automatically calibrate the output frequency of RCL in real time, so that the accuracy of RCL output frequency will no longer be affected by environmental changes. When calibrating RCL, the module requires a precise high-frequency clock signal, which can be either the on-chip PCLK or an external input via the ETR pin.

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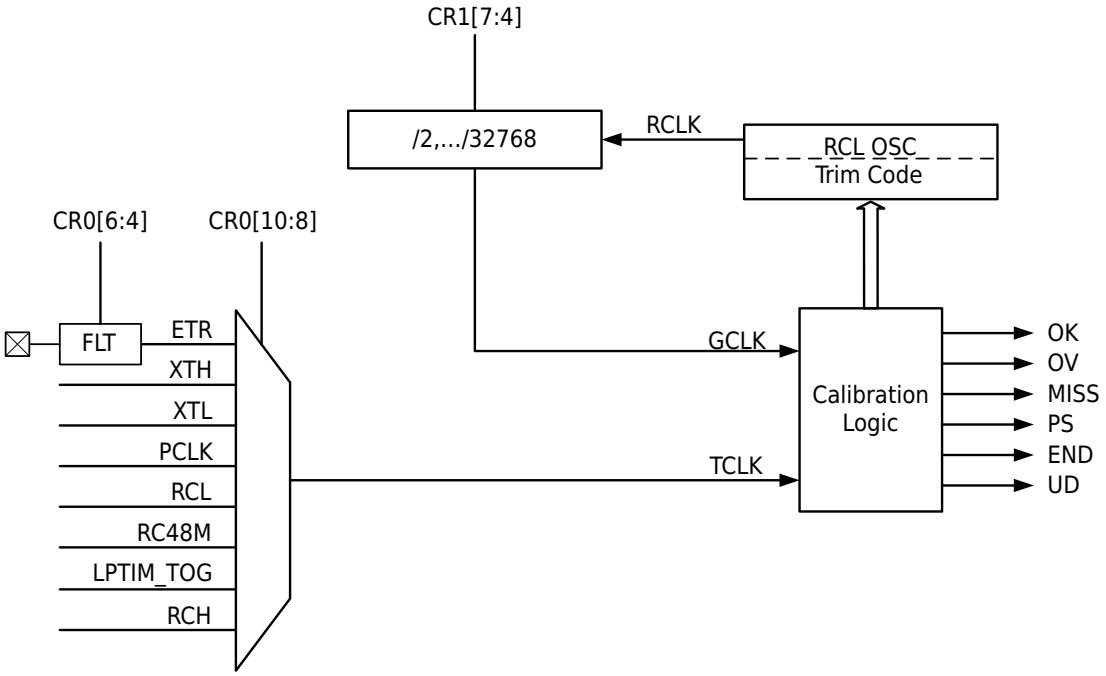

Figure 10-2 RCL Clock Calibration Operational Block Diagram

When automatic calibration begins, the error counter performs down-counting on the TCLK clock signal starting from CTRIM_ARR at each GCLK (the oscillation frequency of RCL after frequency division) cycle, then switches to up-counting upon reaching zero. If the error counter value within a GCLK cycle is less than the value of CTRIM_FLIM register, CTRIM_ISR.OK is set to flag that the RCL output frequency meets expectations. If the error counter value within a GCLK cycle is greater than the value of CTRIM_FLIM register, the TrimCode of RCL is automatically adjusted for the next counting cycle. The auto-adjustment rules are: If counting direction is down-counting, decrease TrimCode of RCL by CTRIM_CR0.STEP; If counting direction is up-counting, increase TrimCode of RCL by CTRIM_CR0.STEP. The calibration logic automatically reduces the value of CTRIM_CR0.STEP to achieve gradual convergence of the RCL output frequency toward the target value.

UD event is generated when the error counter decrements to zero; stopping further counting and MISS event is triggered when the counter increments to CTRIM_ARR. Whenever the rising edge of GCLK arrives, the error counter starts counting again.

10.3.3 Low Power Timer Mode

When CTRIM_CR1.MD is set to 0b10 or 0b11, the module operates in general low power timer mode. In this mode, CTRIM has timing and interrupt functions of a general timer. If the timer clock is RCL, it operates normally in DeepSleep mode, supporting automatic wake-up with a period range of 60μs-65536s.

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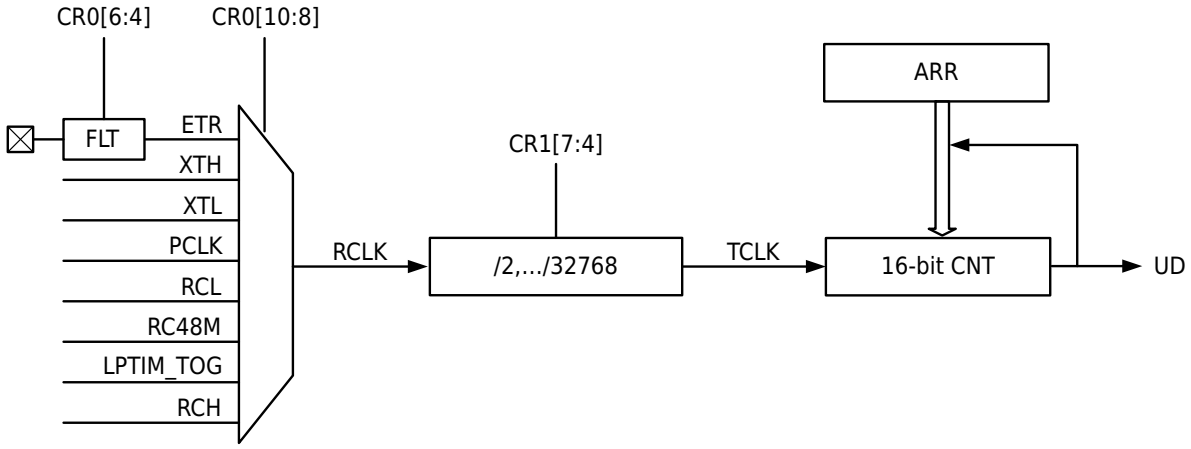

Figure 10-3 General Low Power Timer Scenario Operational Block Diagram

The timer counts down from ARR, and when it reaches 0, an underflow is generated. If the interrupt is enabled, underflow interrupt is generated, the counting period is ARR + 1.

TOG output level flips once every time the timer overflows; the user can output the TOG signal to the pin through the port multiplexing function of the GPIO to drive an external circuit.

10.4 Operation Example

10.4.1 RC48M Clock Automatic Calibration Example

Procedure

Step1. Refer to the "General-Purpose I/O (GPIO)" chapter for related description of pin multiplexing configuration, set the relevant pin function to CTRIM.ETR, and supply it with a 2kHz square wave.

Step2. Set CTRIM_CR1.MD to 0 to select RC48M clock calibration mode.

Step3. Set CTRIM_CR0.SRC to 0, and the external ETR pin input signal is used as RCLK.

Step4. Set CTRIM_CR1.PRS to 1, perform 2 frequency division on RCLK, and GCLK frequency is 1kHz.

Step5. Configure CTRIM_ARR to 47999, and the target count value in a GCLK count cycle is 48000.

> **Note**
> The ETR pin input signal is a 2kHz square wave, the period of GCLK is 1ms. The theoretical count value of the error counter for the RC48M output frequency within 1ms should be 48000.

Step6. Set CTRIM_FLIM to 240, select RC48M calibration accuracy of 0.5%.
48000*0.005=240.

Step7. Set CTRIM_CR0.STEP to 0, and select the initial calibration step to be 16.

Step8. Set CTRIM_CR1.AUTO to 1 to enable automatic calibration.

Step9. Set CTRIM_CR1.EN to 1 to start clock calibration.

Step10. Wait for CTRIM_ISR.END to be 1, and the automatic calibration is completed.

10.4.2 RCL Clock Automatic Calibration Example

Procedure

Step1. Refer to the "General-Purpose I/O (GPIO)" chapter for related description of pin multiplexing configuration, set the relevant pin function to CTRIM.ETR, and supply it with a 1MHz square wave.

Step2. Set CTRIM_CR1.MD to 1, select RCL clock calibration mode.

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Step3. Set CTRIM_CR0.SRC to 0, use the external ETR pin input signal as TCLK.

Step4. Set CTRIM_CR1.PRS to 0x0A, perform 1024 frequency division on RCLK (RCL output frequency is), and the target frequency of GCLK is 32Hz.

Step5. Configure CTRIM_ARR to 31249, and the target count value in a GCLK count cycle is 31250.

Note

The target period of GCLK is 31.25ms, during which the theoretical count value of the error counter for TCLK(1MHz) should be 31250.

Step6. Set CTRIM_FLIM to 156, select RCL correction accuracy to 0.5%.
31250*0.005=156.

Step7. Set CTRIM_CR0.STEP to 0, and select the initial calibration step to be 16.

Step8. Set CTRIM_CR1.AUTO to 1 to enable automatic calibration.

Step9. Set CTRIM_CR1.EN to 1 to start clock calibration.

Step10. Wait for CTRIM_ISR.END to be 1, and the automatic calibration is completed.

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10.5 Register Description

10.5.1 Register List

Base address: 0x40005000

Table 10-1 Clock Trim Module (CTRIM) Register Offset

Offset	Register	Description	Width
0x00	CTRIM_ARR	Autoload Register	32
0x04	CTRIM_CNT	Error Counter Register	32
0x0C	CTRIM_CR0	Control Register 0	32
0x10	CTRIM_CR1	Control Register 1	32
0x14	CTRIM_IER	Interrupt Enable Register	32
0x18	CTRIM_ISR	Interrupt and Status Register	32
0x1C	CTRIM_ICR	Interrupt Flag Clear Register	32
0x20	CTRIM_FCAP	Error Result Register, Counter Value at the End of the GCLK Cycle	32
0x24	CTRIM_TVAL	TRIM Result Register	32
0x28	CTRIM_FLIM	Error Upper Limit Register	32

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10.5.2 Autoload Register (CTRIM_ARR)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000FFFF																															
Name	Reserved																ARR															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	ARR	Error counter reload value	RW

10.5.3 Error Counter Register (CTRIM_CNT)

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																CNT															
Access																	RO															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	CNT	Error counter count value	RO

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10.5.4 Control Register 0 (CTRIM_CR0)

Note

This register can only be changed when CTRIM_CR1.EN is 0.

Offset	Bit Position																													
0x0C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																					SRC			Reserved		ETRFLT		Reserved		STEP	
Access																						RW					RW				RW	

Bit	Name	Functional Description	Access
31:11	*Reserved*	-	-
10:8	SRC	Clock source selection ● 0b000: ETR ● 0b001: XTH ● 0b010: XTL ● 0b011: PCLK ● 0b100: RCL ● 0b101: RC48M ● 0b110: LPTIM_TOG ● 0b111: RCH	RW
7	*Reserved*	-	-
6:4	ETRFLT	External input pin (ETR) filter configuration ● 0b000: No filter ● 0b001: F_{sample}=PCLK, N=2 ● 0b010: F_{sample}=PCLK, N=4 ● 0b011: F_{sample}=PCLK, N=6 ● 0b100: F_{sample}=PCLK/4, N=4 ● 0b101: F_{sample}=PCLK/4, N=6 ● 0b110: F_{sample}=PCLK/8, N=4 ● 0b111: F_{sample}=PCLK/8, N=6	RW
3	*Reserved*	-	-

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Bit	Name	Functional Description	Access
2:0	STEP	TRIM initial step configuration ● 0b000: 0x10 ● 0b001: 0x02 ● 0b010: 0x04 ● 0b011: 0x08 ● 0b100: 0x100 ● 0b101: 0x20 ● 0b110: 0x40 ● 0b111: 0x80	RW

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10.5.5 Control Register 1 (CTRIM_CR1)

Offset	Bit Position																													
0x10	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																					MDRCH		OST	PRS				AUTO	MD		EN
Access																						RW		RW	RW				RW	RW		RW

Bit	Name	Functional Description	Access
31:11	*Reserved*	-	-
10:9	MDRCH	RCH calibration configuration ● 0b00: RC48M single calibration 14bits ● 0b01: RCH single calibration 9bits ● 0b10: RC48M coarse calibration 8bits ● 0b11: RC48M fine tuning 6bits	RW
8	OST	Calibration mode configuration ● 0b0: Real-time calibration mode, the TRIM process continues ● 0b1: Single calibration mode, end when STEP becomes 1	RW
7:4	PRS	Reference clock prescaler configuration ● 0b0000: Setting prohibited ● 0b0001: Divide by 2 ● 0b0010: Divide by 4 ● 0b0011: Divide by 8 ● 0b0100: Divide by 16 ● 0b0101: Divide by 32 ● 0b0110: Divide by 64 ● 0b0111: Divide by 128 ● 0b1000: Divide by 256 ● 0b1001: Divide by 512 ● 0b1010: Divide by 1024 ● 0b1011: Divide by 2048 ● 0b1100: Divide by 4096 ● 0b1101: Divide by 8192 ● 0b1110: Divide by 16384 ● 0b1111: Divide by 32768	RW
3	AUTO	RCH/RC48M/RCL automatic TRIM enable configuration ● 0b0: Disable ● 0b1: Enable	RW

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Bit	Name	Functional Description	Access
2:1	MD	Operating mode configuration ● 0b00: RCH/RC48M calibration mode, CR0.SRC needs to select a low-speed precision clock ● 0b01: RCL calibration mode, CR0.SRC needs to select a high-speed precision clock ● 0b10: Timer mode ● 0b11: Timer mode	RW
0	EN	Timer enable control ● 0b0: Disable ● 0b1: Enable	RW

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10.5.6 Interrupt Enable Register (CTRIM_IER)

Offset	Bit Position																													
0x14	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																										OK	OV	MISS	PS	END	UD
Access																											RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:6	*Reserved*	-	-
5	OK	Auto Trim results in range interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
4	OV	TrimCode overflow interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
3	MISS	Count failure interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
2	PS	Error counter completion interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
1	END	Auto Trim end interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
0	UD	Error counter underflow interrupt enable ● 0b0: Disable ● 0b1: Enable	RW

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10.5.7 Interrupt and Status Register (CTRIM_ISR)

Offset	Bit Position																													
0x18	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																									DIR	OK	OV	MISS	PS	END	UD
Access																										RO	RO	RO	RO	RO	RO	RO

Bit	Name	Functional Description	Access
31:7	*Reserved*	-	-
6	DIR	Error counter counting direction ● 0b0: Counting up, RCH/RC48M output frequency is higher than the target frequency, RCL output frequency is lower than the target frequency ● 0b1: Counting down, RCH/RC48M output frequency is lower than the target frequency, RCL output frequency is higher than the target frequency	RO
5	OK	Trim accuracy flag ● 0b0: Accuracy does not meet FLIM requirements when Trim is completed ● 0b1: Accuracy meets FLIM requirements when Trim is completed	RO
4	OV	TrimCode overflow flag ● 0b0: The TrimCode of RCH/RC48M/RCL is not 0x000 or 0x1FF ● 0b1: The TrimCode of RCH/RC48M/RCL is adjusted to 0x000 or 0x1FF	RO
3	MISS	Counting failure flag ● 0b0: The error counter does not count up to ARR during one cycle of GCLK ● 0b0: The error counter counts up to ARR during one cycle of GCLK	RO
2	PS	Error counter completion flag ● 0b0: Error counter is counting ● 0b1: Error counter has completed one counting cycle and stopped	RO
1	END	Auto Trim end flag ● 0b0: Auto Trim is in progress ● 0b1: Auto Trim is completed	RO
0	UD	Error counter underflow flag ● 0b0: The error counter has not counted to 0 ● 0b1: The error counter has counted to 0	RO

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10.5.8 Interrupt Status Flag Register (CTRIM_ICR)

Offset	Bit Position																													
0x1C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000003F																															
Name	Reserved																										OK	OV	MISS	PS	END	UD
Access																											WO	WO	WO	WO	WO	WO

Bit	Name	Functional Description	Access
31:6	*Reserved*	-	-
5	OK	Clear the calibration success OK flag Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
4	OV	Clear TrimCode overflow flag Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
3	MISS	Clear count failure flag Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
2	PS	Clear error counter completion flag Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
1	END	Clear auto Trim end flag Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
0	UD	Clear error counter underflow flag Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO

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10.5.9 Error Result Register (CTRIM_FCAP)

Offset	Bit Position																													
0x20	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000FFFF																															
Name	Reserved																FCAP															
Access																	RO															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	FCAP	Frequency error capture value	RO

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10.5.10 TRIM Result Register (CTRIM_TVAL)

Offset	Bit Position																													
0x24	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000100																															
Name	Reserved																						TVAL									
Access																							RO									

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	TVAL	Auto TRIM result **Note** 1. After auto TRIM completes, write the TVAL value to the corresponding TRIM register. 2. If reading during TRIM operation, two identical reads are required for validity.	RO

10.5.11 Error Upper Limit Register (CTRIM_FLIM)

Offset	Bit Position																													
0x28	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000010																															
Name	Reserved																						FLIM									
Access																							RW									

Bit	Name	Functional Description	Access
31:12	*Reserved*	-	-
11:0	FLIM	Error tolerance	RW

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11 FLASH

11.1 Introduction

This system includes a Flash memory with a capacity of 256KB/128KB, which is divided into 512/256 sectors, and the capacity of each sector is 512 bytes.

This controller supports erasing, programming and reading operations on Flash memory, also supports erasing and writing protection of Flash memory, and writing protection of control registers.

This controller supports data read and write operations of three-bit widths of byte (8 bits), half-word (16 bits) and word (32 bits) of Flash. Note that the target address of the Byte operation must be byte-aligned, the target address of the half-word operation must be half-word-aligned (the lowest bit of the address is 0b0), and the address of the word operation must be word-aligned (the lowest two bits of the address are 0b00). If the target address is not aligned according to the bit width, the operation is invalid and the CPU will enter the Hard Fault interrupt.

11.2 Functional Description

11.2.1 Capacity Division

The correspondence between the capacity division addresses and sequence numbers is as follows:

Table 11-1 Flash Capacity Division Table

Address	Serial Number	...	Address	Serial Number
0x0E00-0x0FFF	Sector7	...	0x3FE00-0x3FFFF	Sector511
0x0C00-0x0DFF	Sector6	...	0x3FC00-0x3FDFF	Sector510
0x0A00-0x0BFF	Sector5	...	0x3FA00-0x3FBFF	Sector509
0x0800-0x09FF	Sector4	...	0x3F800-0x3F9FF	Sector508
0x0600-0x07FF	Sector3	...	0x3F600-0x3F7FF	Sector507
0x0400-0x05FF	Sector2	...	0x3F400-0x3F5FF	Sector506
0x0200-0x03FF	Sector1	...	0x3F200-0x3F3FF	Sector505
0x0000-0x01FF	Sector0	...	0x3F000-0x3F1FF	Sector504

Note

- 128KByte Flash consists of Sector0-255.
- 256KByte Flash consists of Sector0-511.

11.2.2 Erasing Time

Flash memory has strict time requirements for the control signals of the erasing and programming operations, and failure of the timing of the control signals will cause the erasing and programming operations to fail. When powering on, the erasing parameters when HCLK is 4MHz are loaded by default; if the HCLK frequency is not 4MHz when erasing Flash, the user program should load the erasing parameters corresponding to the HCLK frequency. When operating on Flash, the highest supported HCLK is 48MHz.

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The registers related to the erasing timing parameters are: FLASH_TPNVS, FLASH_TSNVS, FLASH_TMNVS, FLASH_TPGS, FLASH_TPROG, FLASH_TSERASE, FLASH_TMERASE, FLASH_TPRCV, FLASH_TSRCV, FLASH_TMRCV, FLASH_TADS, FLASH_TADH, FLASH_TPGH, FLASH_TRW1, FLASH_TRW2. If the HCLK is increased from the default 4MHz to 8MHz, the value of the above FLASH_Tx register should be set to twice the default value, that is, keep the current result of Tsysclk*FLASH_Tx equal to the default value.

Note

- FLASH_TPNVS: Refers to the TNVS of the program
- FLASH_TSNVS: Refers to the TNVS of sector erase
- FLASH_TMNVS: Refers to the TNVS of chip erase
- FLASH_TRW1: Refers to the latency to the next operation after PROG/sector erase is low
- FLASH_TRW2: Refers to the latency to the next operation after chip erase is low

The following table shows the corresponding Flash erasing time parameters at different frequencies:

Table 11-2 Flash Erasing Time Parameters at Different Frequencies

Parameter	4M	8M	16M	24M	32M	48M
TPNVS	0x67	0xCF	0x19F	0x26F	0x33F	0x4DF
TSNVS	0x67	0xCF	0x19F	0x26F	0x33F	0x4DF
TMNVS	0x19F	0x33F	0x67F	0x9BF	0xCFF	0x137F
TPGS	0xEF	0x1DF	0x3BF	0x59F	0x77F	0xB3F
TPROG	0x17	0x2F	0x5F	0x8F	0xBF	0x11F
TSERASE	0x270F	0x4E1F	0x9C3F	0xEA5F	0x1387F	0x1D4BF
TMERASE	0x222DF	0x445BF	0x88B7F	0xCD13F	0x1116FF	0x19A27F
TPRCV	0xEF	0x1DF	0x3BF	0x59F	0x77F	0xB3F
TSRCV	0xEF	0x1DF	0x3BF	0x59F	0x77F	0xB3F
TMRCV	0x3E7	0x7CF	0xF9F	0x176F	0x1F3F	0x2EDF
TADS	0x2	0x5	0xB	0x11	0x17	0x23
TADH	0x2	0x5	0xB	0x11	0x17	0x23
TPGH	0x2	0x5	0xB	0x11	0x17	0x23
TRW1	0x3	0x7	0xF	0x1F	0x1F	0x2F
TRW2	0x2F	0x5F	0xBF	0x11F	0x17F	0x23F

11.2.3 Read Wait Period

The fastest instruction fetch frequency supported by the built-in Flash of this device is 24MHz. When the HCLK frequency exceeds 24MHz and is less than or equal to 48MHz, waiting period must be inserted for the Flash read time, that is, set FLASH_CR.WAIT to 1. When the wait cycle is inserted, Flash will complete a read operation every two periods.

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11.2.4 Flash Security Protection

Sector Erase/Write Protection

The entire 256KB/128KB Flash memory is divided into 512/256 sectors, and every 4 sectors share an erase/write protection bit. When the page is protected, the erasing and writing operations on the sector are invalid and an alarm flag and interrupt signal are generated. When any sector in the Flash memory is protected, the whole-chip erasing of the Flash is invalid, and an alarm flag and an interrupt signal are generated.

PC Address Erase and Write Protection

The CPU runs the program in Flash, if the current PC pointer just falls within the address range of the page to be erased, then the erase operation is invalid and an alarm flag and an interrupt signal are generated.

Register Write Protection

The important controller of this module shields ordinary write operations, and must be modified by writing sequence.

- **Registers Can Be Changed After a Write Sequence Are As Follows:**

  FLASH_TPNVS, FLASH_TPGS, FLASH_TPROG, FLASH_TSERASE, FLASH_TMERASE, FLASH_TPRCV, FLASH_TSRCV, FLASH_TMRCV, FLASH_CR, FLASH_SLOCK0, FLASH_SLOCK1, FLASH_SLOCK2, FLASH_SLOCK3, FLASH_TSNVS, FLASH_TMNVS, FLASH_TADS, FLASH_TADH, FLASH_TPGH, FLASH_TRW1, FLASH_TRW2
- **Registers Can Be Changed Without a Write Sequence Are As Follows:**

  FLASH_ICLR, FLASH_BYPASS

The specific operation steps to modify the register value by writing sequence are as follows:

Step1. Write 0x5A5A to the FLASH_BYPASS register.

Step2. Write 0xA5A5 to the FLASH_BYPASS register.

Step3. Write the target value to the register to be modified.

Step4. Verify whether the current value of the register to be modified is the same as the target, if not, jump to Step1.

Step5. Perform other operations.

Notice

Write 0x5A5A, 0xA5A5, and write the target register. Do not insert any write operations (write Flash, RAM, REG, etc.) between these three steps of writing operations, otherwise the value of the target register cannot be rewritten. If rewriting fails, you need to perform these three steps again.

Data Readout Protection

The chip's Flash supports 4 -level read protection, and the current protection level can be read through the FLASH_LOCK_ST register. When programming the chip with a programmer, the read protection level of Flash can be configured.

The functions of the chip under each protection level are shown in the table below.

Protection Level	Chip Function
Level0	Flash can be read and written through ISP and SWD interfaces

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Protection Level	Chip Function
Level1	Data cannot be read Date can be downgraded to Level 0 via ISP and SWD interfaces. After downgrading, the Flash content is all FF
Level2	Data cannot be read Data can be downgraded to Level0 through ISP. After downgrading, the Flash content is all FF The SWD interfaces is disabled
Level3	Data cannot be read The functions of the ISP and SWD interfaces being unreadable, that is, the chip can only be programmed once

11.3 Operation Example

11.3.1 Sector Erase

Context

Sector erase allows the user to erase one user-specified sector at a time. After the erase operation is completed, the data in the sector are all 0xFF. If the erase operation is performed from Flash, the CPU will stop fetching instructions, and the hardware will automatically wait for the operation to complete(FLASH_CR.BUSY becomes 0); if the erase operation is performed from RAM, the CPU will not stop fetching instructions, user software should wait for the operation to complete(FLASH_CR.BUSY becomes 0).

Procedure

Step1. Configure the Flash erasing time parameters. For detailed instructions, please refer to Erasing Time, For operation steps, please refer to Configuring Flash Erasing Parameters.

Step2. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step3. Configure FLASH_CR.OP to 2, set the Flash operation mode to Sector Erase.

Step4. Check if FLASH_CR.OP is 2, if not, jump to Step2.

Step5. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step6. Set the corresponding bit of FLASH_SLOCKx to 1 to remove the sector 's erasure protection.

Step7. Check whether the corresponding bit of FLASH_SLOCKx is 1, if it is not 1, jump to Step5.

Step8. Write arbitrary data to any address in the Sector to be erased, triggering Sector erasure.

```
*((unsigned char *)0x00000200) = 0x00
```

Step9. Wait for FLASH_CR.BUSY to become 0, and the Sector erase operation is completed.

Step10. To erase other Sectors, repeat Step5-Step9.

11.3.2 Chip Erase

Context

Chip erase can erase all sector at one time. After the erase operation is completed, the data in all sector are 0xFF. If the erase operation is performed from the Flash, the operation will be prohibited. Because this operation will erase the program segment where the current PC is located. If

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this happens, the FLASH_IFR.RC will be set; if the erase operation is performed from RAM, the CPU will not stop fetching instructions, and the user software should wait for the operation to complete (FLASH_CR.BUSY becomes 0).

Procedure

Step1. Configure the Flash erasing time parameters. For detailed instructions, please refer to Erasing Time, For operation steps, please refer to Configuring Flash Erasing Parameters.

Step2. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step3. Configure FLASH_CR.OP to 3, set the Flash operation mode to Chip erase.

Step4. Check if FLASH_CR.OP is 3, if not, jump to Step2.

Step5. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step6. Set FLASH_SLOCK0 to 0xFFFFFFFF, remove the erase protection of Sector0-127.

Step7. Check whether FLASH_SLOCK0 is 0xFFFFFFFF, if not 0xFFFFFFFF, jump to Step5.

Step8. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step9. Set FLASH_SLOCK1 to 0xFFFFFFFF, remove the erase protection of Sector128-255.

Step10. Check whether FLASH_SLOCK1 is 0xFFFFFFFF, if not 0xFFFFFFFF, jump to Step8.

Step11. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step12. Set FLASH_SLOCK2 to 0xFFFFFFFF, remove the erase protection of Sector256-383.

Step13. Check whether FLASH_SLOCK2 is 0xFFFFFFFF, if not 0xFFFFFFFF, jump to Step11.

Step14. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step15. Set FLASH_SLOCK3 to 0xFFFFFFFF, remove the erase protection of Sector384-511.

Step16. Check whether FLASH_SLOCK3 is 0xFFFFFFFF, if not 0xFFFFFFFF, jump to Step14.

Step17. Write any address in the Chip to be erased to trigger Chip erasure.

```
*((unsigned char *)0x00000000) = 0x00
```

Step18. Wait for FLASH_CR.BUSY to become 0, and the Chip erase operation is completed.

11.3.3 Program

Context

The program can only change the bit data in Flash from 1 to 0, so before writing data, make sure that the data in the address to be written is 0xFF. Support 3 write lengths: Byte (8bits), Half-word (16bits), Word (32bits), the written data is stored in Flash in little-endian mode, that is, the low byte of the data is stored in the low address. If the program is executed from Flash, the CPU will stop fetching instructions, and the hardware will automatically wait for the operation to complete (for FLASH_CR.BUSY to becomes 0); if the program is executed from RAM, the CPU will not stop fetching instructions, and the user Software should wait for the operation to complete (for FLASH_CR.BUSY to goes to 0).

Procedure

- **Byte Program**

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Step1. Configure the Flash erasing time parameters. For detailed instructions, please refer to Erasing Time, and for operation steps, please refer to Configuring Flash Erasing Parameters.

Step2. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step3. Configure FLASH_CR.OP to 1, set the Flash operation mode to write.

Step4. Check if FLASH_CR.OP is 1, if not, jump to Step2.

Step5. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step6. Set the corresponding bit of FLASH_SLOCK to 1 to remove the erase protection.

Step7. Check whether the corresponding bit of FLASH_SLOCK is 1, if it is not 1, jump to Step5.

Step8. Perform Byte program on the target address to be written to trigger the program.

```
*((unsigned char *)0x00001231) = 0x5A
```

Step9. Wait for for FLASH_CR.BUSY to to become 0, and the program is completed.

Step10. To write Byte to other addresses, repeat Step8-Step9.

- **Half-word Program**

Step1. Configure the Flash erasing time parameters. For detailed instructions, please refer to Erasing Time, and for operation steps, please refer to Configuring Flash Erasing Parameters.

Step2. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step3. Configure FLASH_CR.OP to 1, set the Flash operation mode to write.

Step4. Check if FLASH_CR.OP is 1, if not, jump to Step2.

Step5. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step6. Set the corresponding bit of FLASH_SLOCK to 1 to remove the erase protection.

Step7. Check whether the corresponding bit of FLASH_SLOCK is 1, if it is not 1, jump to Step5.

Step8. Perform a Half-word program on the target address to be written to trigger the program.

```
*((unsigned short int *)0x00001232) = 0xABCD
```

Step9. Wait for for FLASH_CR.BUSY to to become 0, and the program is completed.

Step10. To write Half-word to other addresses, repeat Step8-Step9.

- **Word Program**

Step1. Configure the Flash erasing time parameters. For detailed instructions, please refer to Erasing Time, and for operation steps, please refer to Configuring Flash Erasing Parameters.

Step2. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step3. Configure FLASH_CR.OP to 1, set the Flash operation mode to write.

Step4. Check if FLASH_CR.OP is 1, if not, jump to Step2.

Step5. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step6. Set the corresponding bit of FLASH_SLOCK to 1 to remove the erase protection.

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Step7. Check whether the corresponding bit of FLASH_SLOCK is 1, if it is not 1, jump to Step5.

Step8. Perform a Word program on the target address to be written to trigger the program.

```
*((unsigned int *)0x00001234) = 0x55667788
```

Step9. Wait for for FLASH_CR.BUSY to to become 0, and the program is completed.

Step10. To write Word to other addressed, repeat Step8-Step9.

11.3.4 Cont-Program

Context

The program can only change the bit data in Flash from 1 to 0, so before writing data, make sure that the data in the address to be written is 0xFF. Support 3 write lengths: Byte (8bits), Half-word (16bits), Word (32bits), The written data is stored in Flash in little-endian mode, that is, the low byte of the data is stored in the low address. Cont-program can only be performed from RAM, and "read " on Flash are prohibited. User software should wait for the operation to complete (for FLASH_CR.BUSY to becomes 0).

It is recommended that HCLK not be lower than 2 MHz during continuous programming.

Procedure

- **Byte Program**

Step1. Configure the Flash erasing time parameters. For detailed instructions, please refer to Erasing Time, and for operation steps, please refer to Configuring Flash Erasing Parameters.

Step2. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step3. Configure FLASH_CR.OP value at 0.

Step4. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step5. Configure FLASH_CR.CONTP to 1, set the Flash operation mode to continuous write.

Step6. Check whether FLASH_CR.OP and FLASH_CR.CONTP are 0 and 1 respectively, if not, jump to Step2.

Step7. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step8. Set the corresponding bit of FLASH_SLOCK to 1 to remove the erase protection.

Step9. Check whether the corresponding bit of FLASH_SLOCK is 1, if it is not 1, jump to Step7.

Step10. Perform Byte program on the target address to be written to trigger the program.

```
*((unsigned char *)0x00001232) = 0xAB
```

Step11. Wait for for FLASH_CR.BUSY to to become 0, and the program is completed.

Step12. To write Byte to other addresses, repeat Step10-Step11.

Step13. If all the writing operation is completed, proceed to the next step.

Step14. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step15. Configure FLASH_CR.OP at 1.

Step16. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step17. Configure FLASH_CR.CONTP to 0.

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Step18. Check whether FLASH_CR.OP and FLASH_CR.CONTP are 1 and 0 respectively, if not, jump to Step14.

Step19. Wait FLASH_CR.BUSY to become 0.

Step20. Proceed with the following, FLASH_CR.OP can be changed to the value of other modes complete other functional operations.

- **Half-word Program**

Step1. Configure the Flash erasing time parameters. For detailed instructions, please refer to Erasing Time, and for operation steps, please refer to Configuring Flash Erasing Parameters.

Step2. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step3. Configure FLASH_CR.OP value at 0.

Step4. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step5. Configure FLASH_CR.CONTP to 1, set the Flash operation mode to continuous write.

Step6. Check whether FLASH_CR.OP and FLASH_CR.CONTP are 0 and 1 respectively, if not, jump to Step2.

Step7. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step8. Set the corresponding bit of FLASH_SLOCK to 1 to remove the erase protection.

Step9. Check whether the corresponding bit of FLASH_SLOCK is 1, if it is not 1, jump to Step7.

Step10. Perform a Half-word program on the target address to be written to trigger the program.

```
*((unsigned short int *)0x00001232) = 0xABCD
```

Step11. Wait for for FLASH_CR.BUSY to to become 0, and the program is completed.

Step12. To write Half-word to other addresses, repeat Step10-Step11.

Step13. If all the writing operation is completed, proceed to the next step.

Step14. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step15. Configure FLASH_CR.OP at 1.

Step16. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step17. Configure FLASH_CR.CONTP to 0.

Step18. Check whether FLASH_CR.OP and FLASH_CR.CONTP are 1 and 0 respectively, if not, jump to Step14.

Step19. Wait FLASH_CR.BUSY to become 0.

Step20. Proceed with the following, FLASH_CR.OP can be changed to the value of other modes complete other functional operations.

- **Word Program**

Step1. Configure the Flash erasing time parameters. For detailed instructions, please refer to Erasing Time, and for operation steps, please refer to Configuring Flash Erasing Parameters.

Step2. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

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Step3. Configure FLASH_CR.OP value at 0.

Step4. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step5. Configure FLASH_CR.CONTP to 1, set the Flash operation mode to continuous write.

Step6. Check whether FLASH_CR.OP and FLASH_CR.CONTP are 0 and 1 respectively, if not, jump to Step2.

Step7. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step8. Set the corresponding bit of FLASH_SLOCK to 1 to remove the erase protection.

Step9. Check whether the corresponding bit of FLASH_SLOCK is 1, if it is not 1, jump to Step7.

Step10. Perform a Word program on the target address to be written to trigger the program.

```
*((unsigned int *)0x00001234) = 0xABCDABCD
```

Step11. Wait for for FLASH_CR.BUSY to to become 0, and the write operation is completed.

Step12. To write Word to other addressed, repeat Step10-Step11.

Step13. If all the writing operation is completed, proceed to the next step.

Step14. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step15. Configure FLASH_CR.OP to 1, set the Flash operation mode to write.

Step16. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step17. Configure FLASH_CR.CONTP to 0.

Step18. Check whether FLASH_CR.OP and FLASH_CR.CONTP are 1 and 0 respectively, if not, jump to Step14.

Step19. Wait FLASH_CR.BUSY to become 0.

Step20. Proceed with the following, FLASH_CR.OP can be changed to the value of other modes complete other functional operations.

11.3.5 Read

Context

Support to 3 kinds read: Byte(8bits), Half-word(16bits), Word(32bits), the read data is little-endian mode, that is, the low byte of the data is stored in the low address. Read need no prior steps, the data in the FLASH can be read at any time.

Procedure

- **Byte Read**

```
temp = *((unsigned char *)0x00001231)
```

- **Half-word Read**

```
temp = *((unsigned short int *)0x00001232)
```

- **Word Read**

```
temp = *((unsigned int *)0x00001234)
```


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11.3.6 Configure FLASH Erase/Write Parameters

Context

Using the configuration of Erase/Write timing parameters when setting the system frequency to 8MHz as an example, introduce the configuration process.

Procedure

Step1. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step2. Write 0xCF to the FLASH_TNVS register, if the read value of this register is not 0xCF, then jump to the previous step.

Step3. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step4. Write 0xCF to the FLASH_TSNVS register, if the read value of this register is not 0xCF, then jump to the previous step.

Step5. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step6. Write 0x33F to the FLASH_TMNVS register, if the read value of this register is not 0x33F, then jump to the previous step.

Step7. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step8. Write 0x1DF to the FLASH_TPGS register, if the read value of this register is not 0x1DF, then jump to the previous step.

Step9. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step10. Write 0x2F to the FLASH_TPROG register, if the read value of this register is not 0x2F, then jump to the previous step.

Step11. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step12. Write 0x4E1F to the FLASH_TSERASE register, if the read value of this register is not 0x4E1F, then jump to the previous step.

Step13. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step14. Write 0x445BF to the FLASH_TMERASE register, if the read value of this register is not 0x445BF, then jump to the previous step.

Step15. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step16. Write 0x1DF to the FLASH_TPRCV register, if the read value of this register is not 0x1DF, then jump to the previous step.

Step17. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step18. Write 0x1DF to the FLASH_TSRCV register, if the read value of this register is not 0x1DF, then jump to the previous step.

Step19. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

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Step20. Write 0x7CF to the FLASH_TMRCV register, if the read value of this register is not 0x7CF, then jump to the previous step.

Step21. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step22. Write 0x5 to the FLASH_TADS register, if the read value of this register is not 0x5, then jump to the previous step.

Step23. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step24. Write 0x5 to the FLASH_TADH register, if the read value of this register is not 0x5, then jump to the previous step.

Step25. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step26. Write 0x5 to the FLASH_TPGH register, if the read value of this register is not 0x5, then jump to the previous step.

Step27. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step28. Write 0x7 to the FLASH_TRW1 register, if the read value of this register is not 0x7, then jump to the previous step.

Step29. Write 0x5A5A and 0xA5A5 to the FLASH_BYPASS register in sequence to enable register rewriting.

Step30. Write 0x5F to the FLASH_TRW2 register, if the read value of this register is not 0x5F, then jump to the previous step.

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11.4 Register Description

11.4.1 Register List

Base address: 0x40020000

Table 11-4 Flash Controller (FLASH) Register Offset

Offset	Register	Description
0x00	FLASH_TPNVS	Tpnvs Programming arameter
0x04	FLASH_TPGS	Tpgs Time Parameter
0x08	FLASH_TPROG	Tprog Time Parameter
0x0C	FLASH_TSERASE	Tserase Time Parameter
0x10	FLASH_TMERASE	Tmerase Time Parameter
0x14	FLASH_TPRCV	Tprcv Time Parameter
0x18	FLASH_TSRCV	Tsrcv Time Parameter
0x1C	FLASH_TMRCV	Tmrcv Time Parameter
0x20	FLASH_CR	Control Register
0x24	FLASH_IFR	Interrupt Flag Register
0x28	FLASH_ICLR	Interrupt Flag Clear Register
0x2C	FLASH_BYPASS	0x5A5A-0xA5A5 Bypass Sequence Register
0x30	FLASH_SLOCK0	Sector0-127 Erase and Write Protection Register
0x34	FLASH_SLOCK1	Sector128-255 Erase and Write Protection Register
0x40	FLASH_SLOCK2	Sector256-383 Erase and Write Protection Register
0x44	FLASH_SLOCK3	Sector384-511 Erase and Write Protection Register
0x50	FLASH_TSNVS	Tnvs Page Erase Parameter
0x54	FLASH_TMNVS	Tnvs Chip Erase Parameter
0x58	FLASH_TADS	Tads Time Parameter
0x5C	FLASH_TADH	Tadh Time Parameter
0x60	FLASH_TPGH	Tpgh Time Parameter
0x64	FLASH_TRW1	Trw1 Time Parameter
0x68	FLASH_TRW2	Trw2 Time Parameter
0x6C	FLASH_LOCK_ST	Protection Status Register

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11.4.2 TPNVS Programming Parameter Register (FLASH_TPNVS)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000067																															
Name	Reserved																						TPNVS									
Access																							RW									

Bit	Name	Functional Description	Access
31:11	*Reserved*	-	-
10:0	TPNVS	TPNVS programming parameter For FLASH erase/write timing parameters under different frequencies, refer to The FLASH erase time Parameters.	RW

11.4.3 TPGS Parameter Register (FLASH_TPGS)

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000000EF																															
Name	Reserved																						TPGS									
Access																							RW									

Bit	Name	Functional Description	Access
31:12	*Reserved*	-	-
11:0	TPGS	TPGS Parameters For FLASH erase/write timing parameters under different frequencies, refer to The FLASH erase time Parameters.	RW

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11.4.4 TPROG Parameter Register (FLASH_TPROG)

Offset	Bit Position																													
0x08	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000017																															
Name	Reserved																							TPROG								
Access																								RW								

Bit	Name	Functional Description	Access
31:9	*Reserved*	-	-
8:0	TPROG	TPROG Parameters For FLASH erase/write timing parameters under different frequencies, refer to The FLASH erase time Parameters.	RW

11.4.5 TSERASE Parameter Register (FLASH_TSERASE)

Offset	Bit Position																													
0x0C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000270F																															
Name	Reserved																							TSERASE								
Access																								RW								

Bit	Name	Functional Description	Access
31:17	*Reserved*	-	-
16:0	TSERASE	TSERASE Parameters For FLASH erase/write timing parameters under different frequencies, refer to The FLASH erase time Parameters.	RW

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11.4.6 TMERASE Parameter Register (FLASH_TMERASE)

Offset	Bit Position																													
0x10	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000222DF																															
Name	Reserved																						TMERASE									
Access																							RW									

Bit	Name	Functional Description	Access
31:21	*Reserved*	-	-
20:0	TMERASE	TMERASE Parameters For FLASH erase/write timing parameters under different frequencies, refer to The FLASH erase time Parameters.	RW

11.4.7 TPRCV Parameter Register (FLASH_TPRCV)

Offset	Bit Position																													
0x14	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000000EF																															
Name	Reserved																										TPRCV					
Access																											RW					

Bit	Name	Functional Description	Access
31:12	*Reserved*	-	-
11:0	TPRCV	TPRCV Parameters For FLASH erase/write timing parameters under different frequencies, refer to The FLASH erase time Parameters.	RW

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11.4.8 TSRCV Parameter Register (FLASH_TSRCV)

Offset	Bit Position																													
0x18	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000000EF																															
Name	Reserved																				TSRCV											
Access																					RW											

Bit	Name	Functional Description	Access
31:12	*Reserved*	-	-
11:0	TSRCV	TSRCV Parameters For FLASH erase/write timing parameters under different frequencies, refer to The FLASH erase time Parameters.	RW

11.4.9 TMRCV Parameter Register (FLASH_TMRCV)

Offset	Bit Position																													
0x1C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000003E7																															
Name	Reserved																				TMRCV											
Access																					RW											

Bit	Name	Functional Description	Access
31:14	*Reserved*	-	-
13:0	TMRCV	TMRCV Parameters For FLASH erase/write timing parameters under different frequencies, refer to The FLASH erase time Parameters.	RW

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11.4.10 CR Register (FLASH_CR)

Offset	Bit Position																													
0x20	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000200																															
Name	Reserved																				RO	CONTP	DPSTB_EN	Reserved			IE		BUSY	WAIT		OP	
Access																					RW	RW	RW				RW		RO	RW		RW	

Bit	Name	Functional Description	Access
31:12	*Reserved*	-	-
11	RO	Read-only enable bit ● 0b0: Readable, programmable, erasable ● 0b1: Read only, not programmable or erasable	RW
10	CONTP	Continuous programming ● 0b0: Single programming ● 0b1: Continuous programming	RW
9	DPSTB_EN	FLASH dpstb enable mask bit ● 0b0: When the system enters DeepSleep mode, FLASH does not enter low power consumption mode ● 0b1: When the system enters DeepSleep mode, FLASH enters low power consumption mode	RW
8:7	*Reserved*	-	-
6:5	IE	FLASH interrupt enable IE[6]: FLASH erase/write protected address interrupt enable IE[5]: FLASH erase PC Value interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
4	BUSY	Idle/Busy flag bit ● 0b0: Idle State ● 0b1: Busy State	RO
3:2	WAIT	Read FLASH period ● 0b00: 1 period, 0-24MHz ● 0b01: 2 periods, 24-48MHz ● 0b10: Setting prohibited ● 0b11: Setting prohibited	RW
1:0	OP	FLASH operation ● 0b00: Read ● 0b01: Program ● 0b10: Sector erase ● 0b11: Chip erase	RW

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11.4.11 IFR Register (FLASH_IFR)

Offset	Bit Position																													
0x24	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000010																															
Name	Reserved																														PROT	PC
Access																															RO	RO

Bit	Name	Functional Description	Access
31:2	*Reserved*	-	-
1	PROT	FLASH erase/write protection alarm interrupt flag bit	RO
0	PC	FLASH erase/write PC address alarm interrupt flag bit	RO

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11.4.12 ICLR Register (FLASH_ICLR)

Offset	Bit Position																													
0x28	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000000F																															
Name	Reserved																														PROT	PC
Access																															WO	WO

Bit	Name	Functional Description	Access
31:2	*Reserved*	-	-
1	PROT	Clear protection alarm interrupt flag bit Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
0	PC	Clear the PC address alarm interrupt flag bit Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO

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11.4.13 BYPASS Register (FLASH_BYPASS)

Offset	Bit Position																													
0x2C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																BYSEQ															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	BYSEQ	FLASH module protection control register Write 0x5A5A first to FLASH_BYPASS, and then write 0xA5A5 to start the program to FLASH module registers. As long as the program is done to module register, this protection bit automatically recovers to the protection state. Subsequent program to the FLASH module registers require repeating the previous procedures.	RW

11.4.14 SLOCK0 Register (FLASH_SLOCK0)

Offset	Bit Position																													
0x30	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0X00000000 (Peripheral reset is invalid)																													
Name	SLOCK																													
Access	RW																													

Bit	Name	Functional Description	Access
31:0	SLOCK	Sector Erase/Write Protection Bit ● 0b0: Disable erase/write ● 0b1: Enable erase/write	RW

Bit	Serial Number
0	Sector0-3
1	Sector4-7
2	Sector8-11
3	Sector12-15
...	...
31	Sector124-127

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11.4.15 SLOCK1 Register (FLASH_SLOCK1)

Offset	Bit Position																													
0x34	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0X00000000 (Peripheral reset is invalid)																															
Name	SLOCK																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	SLOCK	Sector Erase/Write Protection Bit ● 0b0: Disable erase/write ● 0b1: Enable erase/write	RW

Bit	Serial Number
0	Sector128-131
1	Sector132-135
2	Sector136-139
3	Sector140-143
...	...
31	Sector252-255

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11.4.16 SLOCK2 Register (FLASH_SLOCK2)

Offset	Bit Position																													
0x40	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0X00000000 (Peripheral reset is invalid)																															
Name	SLOCK																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	SLOCK	Sector Erase/Write Protection Bit ● 0b0: Disable erase/write ● 0b1: Enable erase/write	RW

Bit	Serial Number
0	Sector256-259
1	Sector260-263
2	Sector264-267
3	Sector268-271
...	...
31	Sector380-383

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11.4.17 SLOCK3 Register (FLASH_SLOCK3)

Offset	Bit Position																													
0x44	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0X00000000 (Peripheral reset is invalid)																															
Name	SLOCK																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	SLOCK	Sector Erase/Write Protection Bit ● 0b0: Disable erase/write ● 0b1: Enable erase/write	RW

Bit	Serial Number
0	Sector384-387
1	Sector388-391
2	Sector392-395
3	Sector396-399
...	...
31	Sector508-511

11.4.18 TNVS Page Erase Parameter Register (FLASH_TSNVS)

Offset	Bit Position																													
0x50	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000067																															
Name	Reserved																						TSNVS									
Access																							RW									

Bit	Name	Functional Description	Access
31:11	*Reserved*	-	-
10:0	TSNVS	TNVS page erase parameter For FLASH erase/write timing parameters under different frequencies, refer to The FLASH erase time Parameters.	RW

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11.4.19 TNVS Chip Erase Parameter Register (FLASH_TMNVS)

Offset	Bit Position																													
0x54	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000019F																															
Name	Reserved																			TMNVS												
Access																				RW												

Bit	Name	Functional Description	Access
31:13	*Reserved*	-	-
12:0	TMNVS	TNVS chip erase parameter For FLASH erase/write timing parameters under different frequencies, refer to The FLASH erase time Parameters.	RW

11.4.20 TADS Parameter Register (FLASH_TADS)

Offset	Bit Position																													
0x58	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000002																															
Name	Reserved																											TADS				
Access																												RW				

Bit	Name	Functional Description	Access
31:6	*Reserved*	-	-
5:0	TADS	TADS Parameters For FLASH erase/write timing parameters under different frequencies, refer to The FLASH erase time Parameters.	RW

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11.4.21 TADH Parameter Register (FLASH_TADH)

Offset	Bit Position																													
0x5C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000002																															
Name	Reserved																										TADH					
Access																											RW					

Bit	Name	Functional Description	Access
31:6	*Reserved*	-	-
5:0	TADH	TADH Parameters For FLASH erase/write timing parameters under different frequencies, refer to The FLASH erase time Parameters.	RW

11.4.22 TPGH Parameter Register (FLASH_TPGH)

Offset	Bit Position																													
0x60	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000002																															
Name	Reserved																										TPGH					
Access																											RW					

Bit	Name	Functional Description	Access
31:6	*Reserved*	-	-
5:0	TPGH	TPGH Parameters For FLASH erase/write timing parameters under different frequencies, refer to The FLASH erase time Parameters.	RW

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11.4.23 TRW1 Parameter Register (FLASH_TRW1)

Offset	Bit Position																													
0x64	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000003																															
Name	Reserved																													TRW1		
Access																														RW		

Bit	Name	Functional Description	Access
31:6	*Reserved*	-	-
5:0	TRW1	TRW1 parameter For FLASH erase/write timing parameters under different frequencies, refer to The FLASH erase time Parameters.	RW

11.4.24 TRW2 Parameter Register (FLASH_TRW2)

Offset	Bit Position																													
0x68	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000002F																															
Name	Reserved																													TRW2		
Access																														RW		

Bit	Name	Functional Description	Access
31:10	*Reserved*	-	-
9:0	TRW2	TRW2 parameter For FLASH erase/write timing parameters under different frequencies, refer to The FLASH erase time Parameters.	RW

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11.4.25 Protection Status Register (FLASH_LOCK_ST)

Offset	Bit Position																													
0x6C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																														LOCK_ST	
Access																															RO	

Bit	Name	Functional Description	Access
31:2	*Reserved*	-	-
1:0	LOCK_ST	FLASH Protection Status ● 0b00: Level0, ISP can read and write, SWD can read and write ● 0b01: Level1, ISP can be downgraded, SWD can be downgraded; data cannot be read out ● 0b10: Level2, ISP can be downgraded, SWD has no function; data cannot be read out ● 0b11: Level3, ISP has no function, SWD has no function; data cannot be read out	RO

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12 RAM

12.1 Introduction

This system includes an SRAM block with a capacity of 32KB/16KB, supporting read and write operations in byte (8 bits), halfword (16 bits), and word (32 bits) formats. Read and write operations can be performed at the system clock frequency without waiting for cycles. In addition, this controller also supports parity check, which can perform parity check on each byte of SRAM data, and generate a parity check error interrupt.

12.2 Functional Description

12.2.1 RAM Address Range

RAM in the system map is shown in the table below:

Table 12-1 RAM Address Mapping

Address Range	Size	Memory Type
0x20000000-0x20007FFF	32KByte	SRAM
0x20000000-0x20003FFF	16KByte	SRAM

12.2.2 Read and Write Bit Width

This controller supports byte (8 bits), halfword (16 bits), word (32 bits) read and write operations with three-bit widths.

- Addresses for byte operations must be byte aligned
- The target address for halfword operations must be halfword-aligned (the least significant bit of the address must be 0b0).
- The address for word operations must be word-aligned (the least significant two bits of the address must be 0b00).

If the target address of the read and write operation is not aligned according to the bit width, the operation is invalid, and the system will generate a Hard Fault error interrupt.

12.2.3 Parity Check

This controller supports parity check of SRAM data:

- When writing data to SRAM, do a parity check on each byte of data, and store the 1-bit check value and 8-bit data into the SRAM together.
- When reading data from SRAM, the controller reads 8 bits of data along with a 1-bit parity value and performs a parity check.

If there is an error in the check, the parity check error flag is set, and if the interrupt is enabled, an error interrupt will be generated.

Notice

When the parity check is enabled, the SRAM must be initialized before reading the SRAM data, otherwise the parity check alarm flag or interrupt may be triggered by mistake.

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12.3 Register Description

12.3.1 Register List

Base address: 0x40020400

Table 12-2 RAM Controller (RAM) Register Offset

Offset	Register	Description	Width
0x00	RAM_CR	Control register	32
0x04	RAM_ERRADDR	Parity Check Error Address Register	32
0x08	RAM_IFR	Error Interrupt Flag Register	32
0x0C	RAM_ICLR	Error Interrupt Flag Clear Register	32

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12.3.2 Control Register (RAM_CR)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																													IE	Reserved	
Access																														RW		

Bit	Name	Functional Description	Access
31:2	*Reserved*	-	-
1	IE	Parity check error alarm interrupt enable control ● 0b0: Disable ● 0b1: Enable	RW
0	*Reserved*	-	-

12.3.3 Parity Check Error Address Register (RAM_ERRADDR)

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								ERRADDR							
Access																									RO							

Bit	Name	Functional Description	Access
31:15	*Reserved*	-	-
14:0	ERRADDR	Parity check error Byte address After the interrupt flag is cleared, the corresponding address is also cleared.	RO

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12.3.4 Error Interrupt Flag Register (RAM_IFR)

Offset	Bit Position																													
0x08	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																															ERR
Access																																RO

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-
0	ERR	Parity check error flag ● 0b0: when reading RAM, the parity check is correct ● 0b1: parity check error when reading RAM	RO

12.3.5 Error Interrupt Flag Clear Register (RAM_ICLR)

Offset	Bit Position																													
0x0C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000001																															
Name	Reserved																															ERRCLR
Access																																WO

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-
0	ERRCLR	Error interrupt flag clear bit Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO

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13 DMAC

13.1 Introduction

Direct memory access (DMA) is used to provide high-speed data transmission between peripherals and memory or between memory and memory. The CPU does not need to participate in the transmission process, so the CPU can perform other operations synchronously. The DMAC has 2 independent DMA channels, each channel is dedicated to managing requests from peripherals or memory access. There is also an arbiter to coordinate the priority of each DMA request.

13.2 Features

DMA controller supports the following features:

- 2 independent DMA channels, support priority configuration
- 3 data transfer widths: 8-bit, 16-bit, 32-bit
- 4 transmission modes: Software Block, Software Burst, Hardware Block, Hardware Burst
- 2 source address types: peripheral, memory
- 2 target address types: peripheral, memory
- 2 address change modes: fixed, auto-increment
- Transmission address addressing range: 0x00000000-0xFFFFFFFF
- The number of data blocks to be transmitted is configurable: 1-65536
- The size of the data block to be transmitted is configurable: 1-16
- Support address and transfer number reload function

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13.3 Functional Description

13.3.1 Function Block Diagram

- DMAC

  DMAC has 2 DMA channels, and when conflicts occur between channels, arbitration is performed by the priority controller.

- Bus Matrix

  CPU and DMAC are connected to the bus matrix. When the CPU and DMAC access different AHB bus devices or AHB bridges, data transfers can be performed simultaneously. When the CPU and DMAC access the same bus device or AHB bridge, the priority of the CPU is higher than that of the DMAC. That is, only when the CPU releases the AHB bus device or the AHB bridge, the DMAC can access the AHB bus device or the AHB bridge.

- DMA Requests

  If the peripheral supports hardware DMA request, the DMA channel can be configured as a hardware trigger, otherwise, it can only be configured as a software trigger.

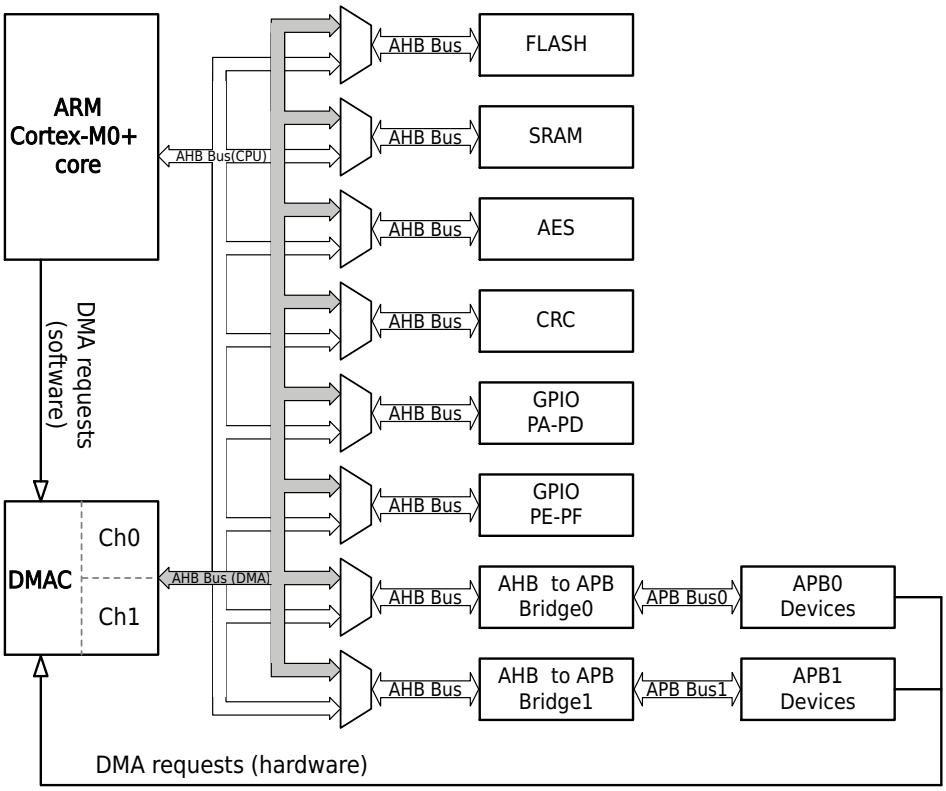

Figure 13-1 DMA Controller Functional Block Diagram

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13.3.2 DMAC Transfer Mode

13.3.2.1 DMAC Transfer Mode Overview

DMA controller supports 4 transfer modes: software Block transfer mode, software Burst transfer mode, hardware Block transfer mode, and hardware Burst transfer mode.

Table 13-1 DMAC Transfer Mode Comparison Table

Compare Items	Software Block Transfer	Software Burst Transfer	Hardware Block Transfer	Hardware Burst Transfer
Whether interrupted by higher priority DMA channel or CPU	Can	Can't	Can	Can't
Conditions that trigger the start of the transfer	Write DMAC register		Peripheral interrupt flag	
The amount of data that a transfer is triggered	(BC+1)*(TC+1)		BC+1	(BC+1)*(TC+1)
The total amount of data transferred after configuration	(BC+1)*(TC+1)			
Main application scenarios	● Memory to memory ● Memory to peripherals without DMA requests		● Memory to peripherals with DMA requests ● Peripherals with DMA requests to memory	● Memory to memory ● Memory to peripherals without DMA requests

13.3.2.2 Software Block Transfer Mode

When configuring DMAC_CONFAx.TRI_SEL=0 and DMAC_CONFBx.MODE=0, DMAC works in software Block transfer mode.

In this mode, the user writes 1 to DMAC_CONFAx.ST, which triggers the DAMC to start the software Block transfer mode, and stops after transferring (BC+1) * (TC+1) data. Each transmission of BC+1 data is completed, the DMAC inserts a transmission gap, and the priority arbiter performs priority arbitration in the gap. If a CPU or higher-priority DMA channel requests the bus during this gap, bus ownership is transferred to the CPU or higher-priority DMA channel. Once released, the remaining data transfer will resume and complete.

The software Block transfer diagram is shown below, where SA represents the source address and DA represents the destination address; The size of the data block is 3 (BC=2), the number of data blocks is 3 (TC=2), the data width is 16-bit, and the address increases automatically.

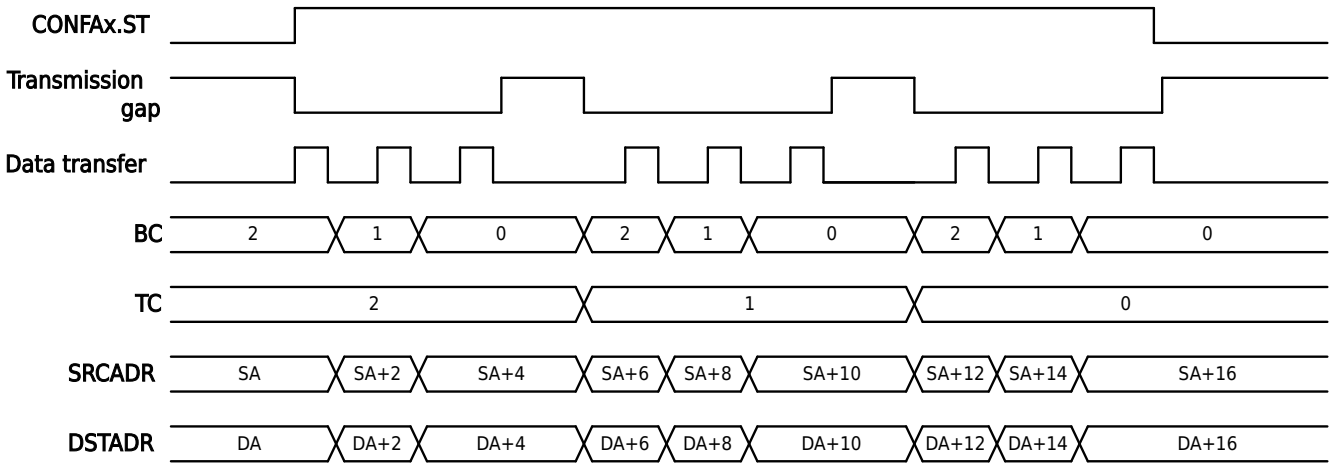

Figure 13-2 DMA Software Block Transfer Mode

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13.3.2.3 Software Burst Transfer Mode

When configuring DMAC_CONFAx.TRI_SEL=0 and DMAC_CONFBx.MODE=1, DMAC works in software Burst transfer mode.

In this mode, the user writes 1 to DMAC_CONFAx.ST, which triggers the DMAC to start the software Burst transfer mode, and stops after transmitting (BC+1) * (TC+1) data. There is no transmission gap in this transfer. Before all data transfers are completed, the DMA channel which is working currently will always occupy the bus. The CPU or a higher priority DMA channel can only access the bus after the operation is completed. It is recommended to avoid transferring excessive data at once, as this may render the CPU completely unable to operate for a period of time.

The software Burst transfer diagram is shown below, where SA represents the source address, DA represents the destination address; the data block size is 3 (BC=2), the number of data blocks is 3 (TC=2), the data width is 16-bit, and the address increases automatically.

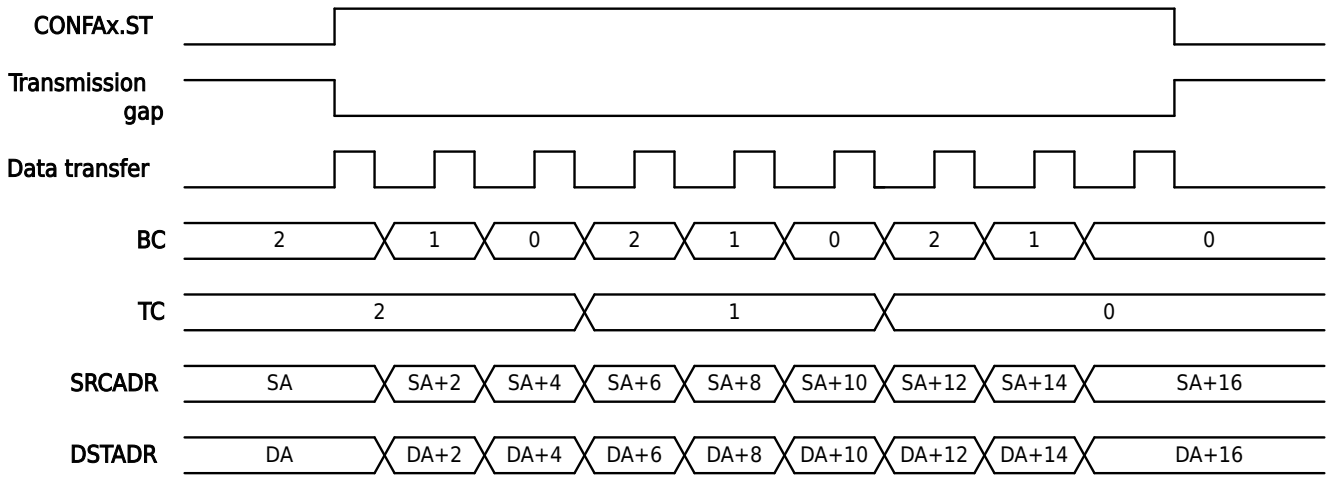

Figure 13-3 DMA Software Burst Transfer Mode

13.3.2.4 Hardware Block Transmission Mode

When configuring DMAC_CONFAx.TRI_SEL is not 0 and DMAC_CONFBx.MODE is 0, DMAC works in hardware Block transfer mode.

In this mode, whenever the peripheral DMA request signal appears once, the DMAC is triggered to start a hardware block transfer, and transfer (BC+1) data. It needs to appear (TC+1) peripheral DMA request signal to complete the transmission of all DMA data. Every (BC+1) data is completed, the DMAC inserts a transmission gap, and the priority arbiter performs priority arbitration in the gap. If the CPU or a higher-priority DMA channel requests the bus during this gap, bus ownership is transferred to the CPU or higher-priority DMA channel. Once released, the remaining data transfer will resume and complete.

Note

In this mode, generally set BC to 0 to obtain a data from the peripheral or provide a data to the peripheral.

For DMA-supported hardware request signal types, refer to the DMAC_CONFAx.TRI_SEL bit function description.

The hardware block transmission diagram is shown below, where SA represents the source address, DA represents the destination address; the data block size is 2 (BC=1), the number of data blocks is 3 (TC=2), the data width is 8-bit, and the target address increases automatically, the source address is fixed, and the transmission is automatically disabled after completion.

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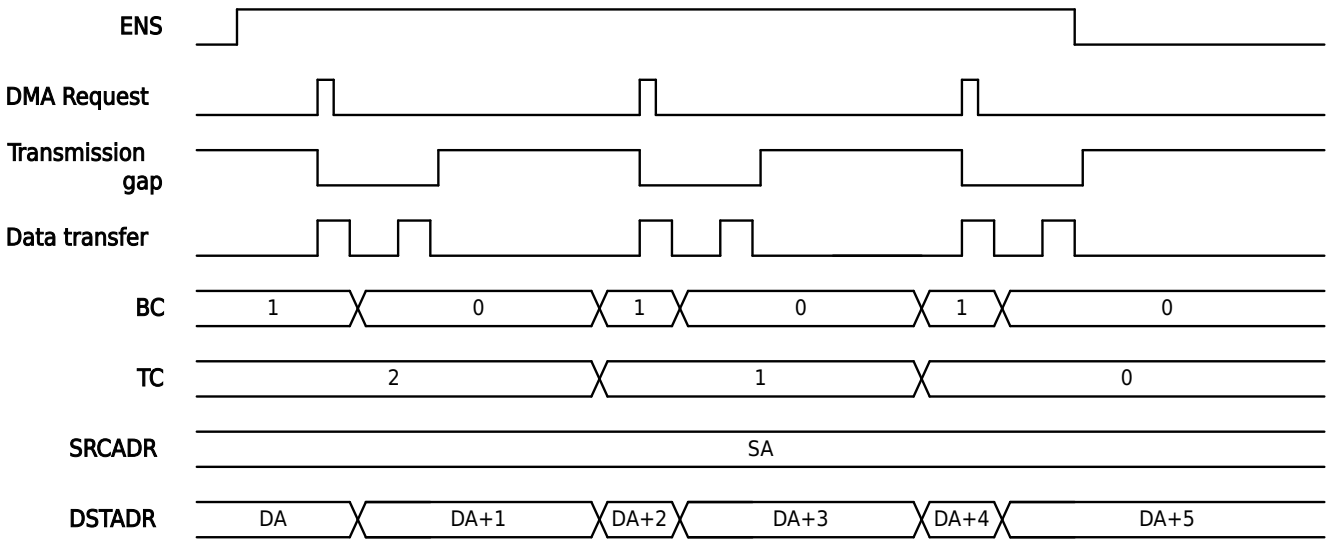

Figure 13-4 DMA Hardware Block Transfer Mode

13.3.2.5 Hardware Burst Transfer Mode

When configuring DMAC_CONFAx.TRI_SEL is not 0 and DMAC_CONFBx.MODE is 1, DMAC works in hardware Burst transfer mode.

In this mode, when a peripheral DMA request signal occurs, the DMAC initiates hardware Burst transfer mode, stopping after transmitting (BC+1)*(TC+1) data. There is no transmission gap in this transfer. Before all data transfers are completed, the DMA channel which is working currently will always occupy the bus. The CPU or a higher priority DMA channel can only access the bus after the operation is completed. It is recommended to avoid transferring excessive data at once, as this may render the CPU completely unable to operate for a period of time.

For DMA-supported hardware request signal types, refer to the DMAC_CONFAx.TRI_SEL bit function description.

The hardware Burst transmission diagram is shown below, where SA represents the source address, DA represents the destination address; the data block size is 3 (BC=2), the number of data blocks is 3 (TC=2), the data width is 8-bit, and the source address increases automatically, the target address is fixed, and the transfer is automatically disabled after completion.

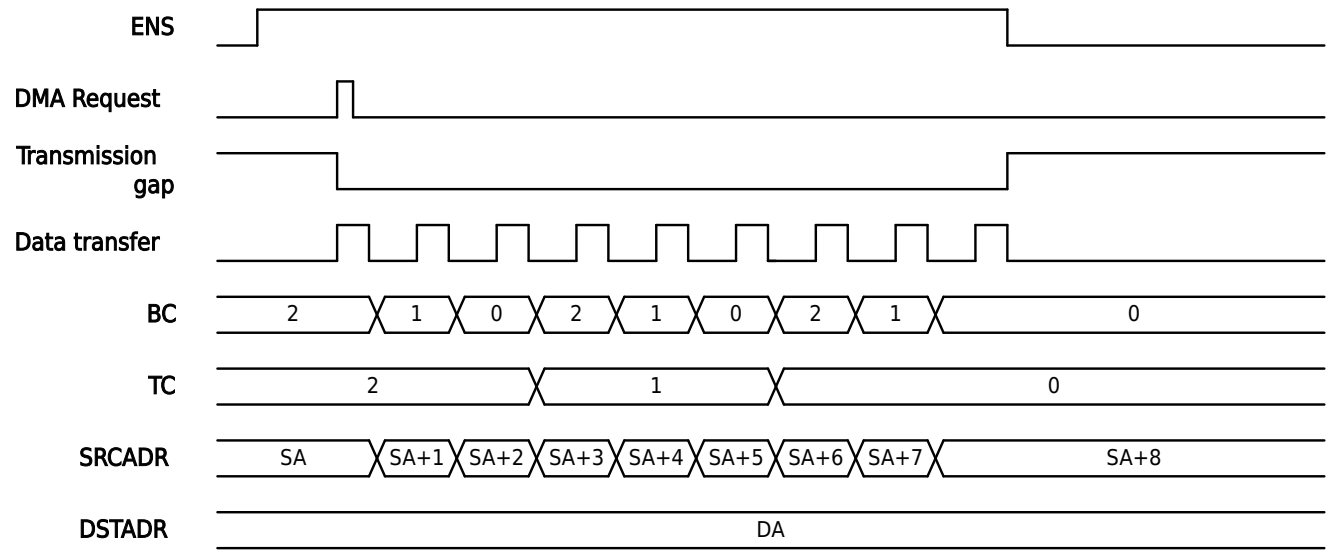

Figure 13-5 DMA Hardware Burst Transfer Mode

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13.3.3 DMA Transfer Pause

Transfer Pause in Software Block Transfer Mode

When DMAC works in software Block transfer mode:

When DMAC_CONF.HALT is set to a non-zero value, all active transfer channels will enter a paused state during transfer intervals and cease data transmission. After setting DMAC_CONF.HALT to 0: Previously active DMAC channels (DMAC_CONFAx.ST=1) will resume unfinished transfers; Inactive DMAC channels (DMAC_CONFAx.ST=0) will wait until DMAC_CONFAx.ST becomes 1 to initiate transfers.

When DMAC_CONFAx.PAS is set to 1, the corresponding active channel to x will pause during transfer intervals and halt data transmission; After setting DMAC_CONFAx.PAS is set to 0, the channel will resume the unfinished transfer.

Transfer Pause in Software Burst Transfer Mode

When the DMAC operates in software Burst transfer mode with no active data transmission:

When DMAC_CONF.HALT is set to a non-zero value, DMA channels will enter a paused state and cease data transmission. If a DMAC channel has software trigger enabled (DMAC_CONFAx.ST=1) during the pause, then after setting DMAC_CONF.HALT to 0, the channel will initiate a new complete transfer; if a DMAC channel has software trigger disabled (DMAC_CONFAx.ST=0) during the pause, then after setting DMAC_CONF.HALT to 0, wait until the channel's software trigger is enabled (DMAC_CONFAx.ST=1), and a new complete transfer will be initiated.

When DMAC_CONFAx.PAS is set to 1, DMA channels will enter a paused state and cease data transmission. If the channel's software trigger is enabled (DMAC_CONFAx.ST=1) during the pause, then after setting DMAC_CONFAx.PAS to 0, the channel will initiate a new complete transfer; if the channel's software trigger is disabled (DMAC_CONFAx.ST=0) during the pause, then after setting DMAC_CONFAx.PAS to 0, wait until the channel's software trigger is enabled (DMAC_CONFAx.ST=1), and a new complete transfer will be initiated.

When the DMAC is working in the software Burst transfer mode and data transfer is in progress, writing a non-zero value to DMAC_CONF.HALT or writing 1 to DMAC_CONFAx.PAS cannot pause the ongoing transfer; the DMA channel will not enter the pause state after the current transfer is completed.

Transfer Pause in Hardware Block Transfer Mode

When DMAC works in hardware Block transfer mode:

When DMAC_CONF.HALT is set to a non-zero value, all active transfer channels will enter a paused state during transfer intervals and cease data transmission. After setting DMAC_CONF.HALT to 0, each DMAC channel will require the next trigger signal to resume the previously unfinished transfer.

When DMAC_CONFAx.PAS is set to 1, the corresponding active channel to x will pause during transfer intervals and halt data transmission. After setting DMAC_CONFAx.PAS to 0, the channel will require the next trigger signal to resume the previously unfinished transfer.

Transfer Pause in Hardware Burst Transfer Mode

When the DMAC operates in hardware Burst transfer mode with no active data transmission:

When DMAC_CONF.HALT is set to a non-zero value, DMA channels will enter a paused state and cease data transmission. After configuring DMAC_CONF.HALT to 0, DMAC will start a new complete transmission when it receives the next trigger signal.

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When DMAC_CONFAx.PAS is set to 1, DMA channels will enter a paused state and cease data transmission. After configuring DMAC_CONFAx.PAS to 0, DMAC will start a new complete transmission when it receives the next trigger signal.

When the DMAC is working in the hardware Burst transfer mode and data transfer is in progress, writing a non-zero value to DMAC_CONF.HALT or writing 1 to DMAC_CONFAx.PAS cannot pause the ongoing transfer; the DMA channel will not enter the pause state after the current transfer is completed.

13.3.4 Other Configurations of DMA

Data Width

Configure DMAC_CONFBx.WIDTH, you can configure the width of each data to be transferred as 8-bit, 16-bit, or 32-bit, noting that this bit width must exactly match the bit width of the DMA source and destination addresses.

Block Size

Configure DMAC_CONFAx.BC, you can configure the number of data to be transmitted in each data block as 1-16. Note: The value of BC should match the number of consecutive operations provided by the source and destination addresses.

- If the source address or destination address can only provide or receive one data at a time, then BC can only be configured as 0. For example, UART/LPUART/SPI can only provide one data to DMA each time, while UART/LPUART/SPI/DAC can only receive one data from DMA each time, so BC can only be configured as 0.
- If both the source address and the destination address can provide or receive multiple data, then BC can be configured to a larger value to speed up the transmission speed. For example, when transferring from FLASH to RAM or from FLASH to CRC, the source address and destination address can be operated continuously, so BC can be configured as 15 to achieve fast transfer.

Number of Data Blocks

Configure DMAC_CONFAx.TC, you can configure the number of data blocks to be transferred from 1 to 65536 after each DMA is started.

Channel Priority

- When DMAC_CONF.PRIO=0b0, DMAC works in fixed priority mode. At this time, CH0 has a higher priority than CH1, Only when the high priority channel does not transmit data, the low priority channel can transmit data.
- When DMAC_CONF.PRIO=0b1, DMAC works in cycle priority mode. At this time, CH0 and CH1 have higher priority in turn, and the two channels will occupy the bus in turn for data transmission.

Auto-Reload

If the automatic reload function is enabled, the data block size, number of data blocks, source address, and destination address will be automatically loaded to the last configuration value after the transmission is completed, and there is no need to configure it every time.

13.3.5 DMA Interrupt

DMA supports two types of interrupts: transfer error and transfer complete. When an interrupt is triggered, the status register DMAC_CONFBx.STAT can be checked to determine what condition triggered the interrupt, and the built-in interrupt status flag can be cleared by clearing the register DMAC_CONFBx.STAT.

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Support conditions that trigger the DMA interrupt are as follows:

- Transport address out of addressing range
- Peripheral request to stop DMA
- Access transfer source address error
- Access transfer destination address error
- Transmission completed

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13.4 Register Description

13.4.1 Register List

Base address: 0x40021000

Table 13-2 DMA Controller (DMA) Register Offset

Offset	Register	Description	Width
0x00	DMAC_CONF	All channel configuration registers	32
0x10+0x10*x	DMAC_CONFAx	Channel x configuration A register (x=0-1)	32
0x14+0x10*x	DMAC_CONFBx	Channel x configuration B register(x=0-1)	32
0x18+0x10*x	DMAC_SRCADRx	Channel x transfer source address register (x=0-1)	32
0x1C+0x10*x	DMAC_DSTADRx	Channel x transfer destination address register (x=0-1)	32

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13.4.2 All Channel Configuration Register (DMAC_CONF)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	EN	Reserved		PRIO	HALT				Reserved																							
Access	RW			RW	RW																											

Bit	Name	Functional Description	Access
31	EN	DMA controller enable ● 0b0: Disable ● 0b1: Enable **Notice** When the DMA controller is disabled, ongoing transfers will be forcibly terminated, resulting in unpredictable consequences.	RW
30:29	*Reserved*	-	-
28	PRIO	DMA channel priority configuration ● 0b0: Fixed priority mode, CH0>CH1 priority ● 0b1: Cycle priority mode, CH0/CH1 take turns to obtain bus access	RW
27:24	HALT	DMA all channel transfer pause control ● 0b0000: Resume all channel data transmission ● 0b0001-0b1111: Suspend all channel data transmission	RW
23:0	*Reserved*	-	-

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13.4.3 Channel x Configuration A Register (DMAC_CONFAx) (x=0-1)

Offset: 0x10+0x10*x

Offset	Bit Position																															
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	ENS	PAS	ST	TRI_SEL							Reserved		BC				TC															
Access	RW	RW	RW	RW									RW				RW															

Bit	Name	Functional Description	Access
31	ENS	DMA channel enable control ● 0b0: Disable the current DMA channel ● 0b1: Enable the current DMA channel; if CONFBx.MSK is 0, this bit is automatically cleared when the transfer is completed **Notice** ● When the DMA controller is disabled, ongoing transfers will be forcibly terminated, resulting in unpredictable consequences. ● DMA channel enable, the operation is recommended to be performed after all DMA configurations are completed.	RW
30	PAS	DMA channel data transfer pause control ● 0b0: Resume DMA channel data transfer ● 0b1: Suspend DMA channel data transfer	RW
29	ST	DMA channel software trigger control ● 0b0: Stop DMA channel software Block/Burst transfer ● 0b1: Trigger DMA channel to start software Block/Burst transfer, this bit is automatically cleared when the transfer is completed	RW
28:22	TRI_SEL	DMA channel trigger source configuration ● 0x00: Software trigger ● 0x40: SPI0 receiving Buf is not empty ● 0x41: SPI0 sending Buf is empty ● 0x42: SPI1 receiving Buf is not empty ● 0x43: SPI1 sending Buf is empty ● 0x44: ADC JQR conversion completed ● 0x45: ADC SQR conversion completed ● 0x46: LCD timing interrupt ● 0x47: Setting prohibited ● 0x48: UART0 receiving Buf is not empty ● 0x49: UART0 sending Buf is empty ● 0x4A: UART1 receiving Buf is not empty ● 0x4B: UART1 sending Buf is empty ● 0x4C: LPUART0 receiving Buf is not empty ● 0x4D: LPUART0 sending Buf is empty ● 0x4E: LPUART1 receiving Buf is not empty	RW

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Bit	Name	Functional Description	Access
28:22	TRI_SEL	● 0x4F: LPUART1 sending Buf is empty ● 0x50: DAC conversion completed ● 0x51: Setting prohibited ● 0x52: TIM0 channel A, occurrs capture event or compare event ● 0x53: TIM0 channel B, occurrs capture event or compare event ● 0x54: TIM1 channel A, occurrs capture event or compare event ● 0x55: TIM1 channel B, occurrs capture event or compare event ● 0x56: TIM2 channel A, occurrs capture event or compare event ● 0x57: TIM2 channel B, occurrs capture event or compare event ● 0x58: TIM3 channel A, occurrs capture event or compare event ● 0x59: TIM3 channel B, occurrs capture event or compare event ● 0x5A: TIM4 channel A, occurrs capture event or compare event ● 0x5B: TIM4 channel B, occurrs capture event or compare event ● 0x5C: TIM5 channel A, occurrs capture event or compare event ● 0x5D: TIM5 channel B, occurrs capture event or compare event ● 0x5E: TIM6 channel A, occurrs capture event or compare event ● 0x5F: TIM6 channel B, occurrs capture event or compare event ● 0x60: UART2 receive Buf is not empty ● 0x61: UART2 sending Buf is empty ● 0x62: UART3 receive Buf is not empty ● 0x63: UART3 sending Buf is empty ● Others: Setting prohibited	RW
21:20	*Reserved*	-	-
19:16	BC	DMA channel transfer data block size Configure the size of the data block to be transmitted by the DMA channel as BC+1 **Note** When the source address or destination address can only provide or receive a data every once in a while, the BC value can only be set to 0.	RW
15:0	TC	Number of data blocks transferred by DMA channel Configure the number of data blocks to be transmitted by the DMA channel as TC+1 During transmission, every time a data block is transmitted, the value of this register will be decremented by 1 **Note** The total amount of data transferred by DMA is (TC +1)*(BC +1).	RW

Note

- The trigger source of TIM0/1/2/3:
  - TIM0/1/2/3 channel A: Compare capture A, external trigger
  - TIM0/1/2/3 channel B: Compare capture B, event update
- The trigger source of TIM4/5/6:
  - TIM4/5/6 channel B: Compare capture A/C, counter overflow, dedicated compare A
  - TIM4/5/6 channel B: Compare capture B/D, counter underflow, dedicated compare B

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13.4.4 Channel x Configuration B Register (DMAC_CONFBx) (x=0-1)

Offset: 0x14+0x10*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved		MODE		WIDTH		FS	FD	RC	RS	RD	ERR_IE	FIS_IE	STAT	Reserved																	MSK
Access			RW		RW		RW	RW	RW	RW	RW	RW	RW	RW																		RW

Bit	Name	Functional Description	Access
31:30	*Reserved*	-	-
29:28	MODE	DMA channel transfer mode configuration ● 0b00: Block transfer ● 0b01: Burst transfer ● 0b10: Setting prohibited ● 0b11: Setting prohibited	RW
27:26	WIDTH	DMA channel transfer data width configuration ● 0b00: 8-bit ● 0b01: 16-bit ● 0b10: 32-bit ● 0b11: Setting prohibited	RW
25	FS	DMA channel source address auto-increment enable ● 0b0: The source address will be incremented automatically after each data transmission is completed ● 0b1: The source address remains unchanged during transmission **Note** The auto-increment corresponding to the data width of 8-bit/16-bit/32-bit is 1/2/4 respectively.	RW
24	FD	DMA channel destination address auto-increment enable ● 0b0: The target address will be incremented automatically after each data transmission is completed ● 0b1: The destination address remains unchanged during transmission **Note** The auto-increment corresponding to the data width of 8-bit/16-bit/32-bit is 1/2/4 respectively.	RW

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Bit	Name	Functional Description	Access
23	RC	DMA channel BC and TC reload enable ● 0b0: Disable BC/TC reloading, and the values of BC/TC are all 0 after the transmission is completed ● 0b1: Enable BC/TC reloading, and the values of BC/TC will automatically restore to the written initial value after the transmission is completed	RW
22	RS	DMA channel source address reload enable ● 0b0: Disable source address overloading, the value of the source address is uncertain after the transmission is completed ● 0b1: Enable the source address reloading, and the value of the source address is the written initial value after the transmission is completed	RW
21	RD	DMA channel destination address reload enable ● 0b0: Disable destination address overloading, the value of the destination address is uncertain after the transmission is completed ● 0b1: Enable target address reloading, the value of the destination address will automatically restore to the written initial value after the transmission is completed	RW
20	ERR_IE	DMA channel transfer error interrupt enable ● 0b0: Disable ● 0b1: Enable **Note** In the interrupt service routine, you need to write 0x00 to STAT to clear the interrupt status.	RW
19	FIS_IE	DMA channel transfer complete interrupt enable ● 0b0: Disable ● 0b1: Enable **Note** In the interrupt service routine, you need to write 0x00 to STAT to clear the interrupt status.	RW
18:16	STAT	DMA channel current transfer status ● 0b000: Initial value ● 0b001: Transmission error, the transmission address exceeds the addressing range ● 0b010: Transmission error, peripheral request to stop DMA ● 0b011: Transmission error, access transmission source address error ● 0b100: Transmission error, access transmission destination address error ● 0b101: Transmission completed ● 0b110: Setting prohibited ● 0b111: Transmission pause	RW
15:1	*Reserved*	-	-

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Bit	Name	Functional Description	Access
0	MSK	Auto-disable/enable configuration when DMA channel transfer completes ● 0b0: CONFAx.ENS is automatically cleared when the DMA channel transfer completes ● 0b1: CONFAx.ENS remains unchanged when DMA channel transfer completes	RW

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13.4.5 Channel x Transfer Source Address Register (DMAC_SRCADRx) (x=0-1)

Offset: 0x18+0x10*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	SRCADR																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	SRCADR	DMA channel source address configuration Auto-reload can be configured via CONFBx.RS **Notice** The address alignment should match the data width, otherwise, it will cause address access errors.	RW

13.4.6 Channel x Transfer Destination Address Register (DMAC_DSTADRx) (x=0-1)

Offset: 0x1C+0x10*x

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	DSTADR																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	DSTADR	DMA channel destination address configuration Auto-reload can be configured via CONFBx.RD **Notice** The address alignment should match the data width, otherwise, it will cause address access errors.	RW

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14 TIM0/1/2/3

14.1 Introduction

TIM0/1/2 is a timer composed of 1 counting unit and 2 comparing units respectively. Each timer supports 2 independent PWM outputs or 1 pair of complementary PWM outputs plus 1 independent PWM output, with support for 2 capture inputs. TIM0/1/2 can form 3 pairs of complementary PWM outputs.

TIM3 is a timer composed of 1 counting unit and 8 comparison units, supporting 6 independent PWM outputs or 3 pairs of complementary PWM outputs, with support for 6 capture inputs. Additionally, there are 2 dedicated comparison units that can generate compare interrupts and be used to trigger ADC and DMA operations.

Using timer prescaler, system prescaler and system clock selection, the pulse width and waveform period can be flexibly adjusted; the pulse width can be measured conveniently.

14.2 Features

14.2.1 TIM0/1/2 Features

- Two independent PWM outputs CHA, CHB
- One complementary PWM output (CHA, CHB)+one independent PWM output (gate)
- One complementary PWM output (CHA, CHB)+one capture function (gate)
- Up to two capture inputs
- Pulse width measurement
- Quadrature encoder counting function
- Single pulse mode
- External counting function
- DMA Trigger
- Dead-time control
- Braking control
- Cycle-by-cycle current limiting
- Edge alignment, symmetric center alignment and asymmetric center alignment PWM output

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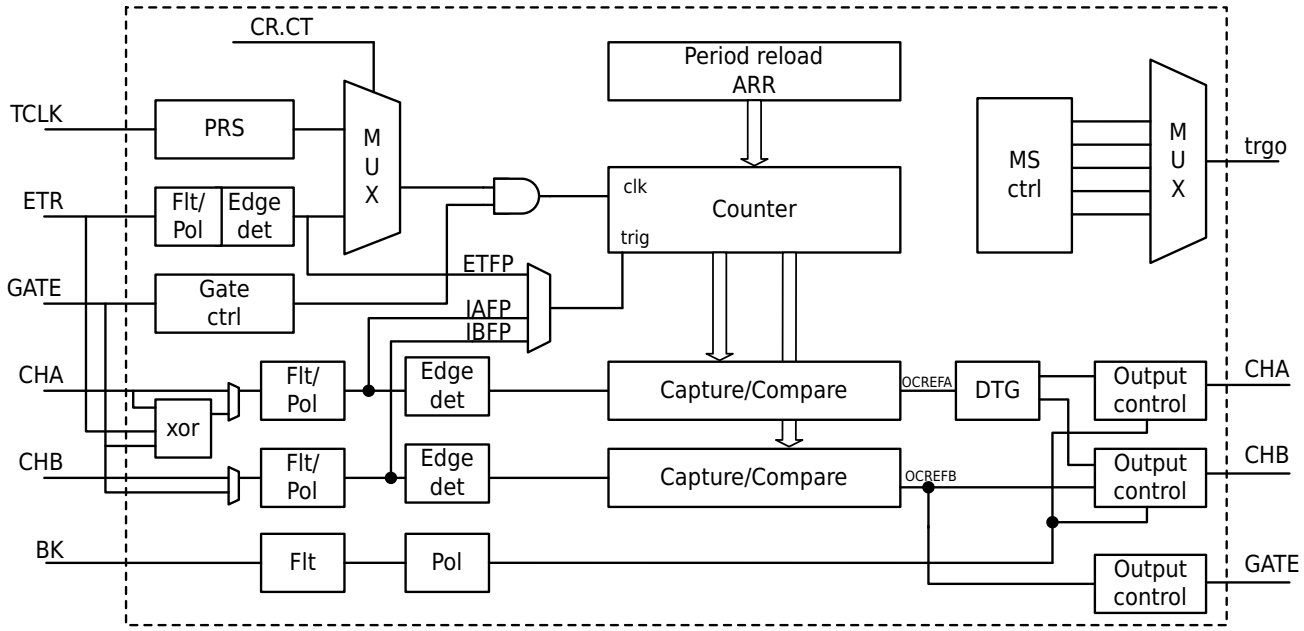

Figure 14-1 TIM0/1/2 Block Diagram

14.2.2 TIM3 Features

- 6 independent PWM outputs CH0A, CH0B, CH1A, CH1B, CH2A, CH2B
- 3 complementary PWM outputs(CHxA, CHxB)+1 independent PWM output (gate)
- 3 complementary PWM outputs(CHxA, CHxB)+1 capture function (gate)
- Two dedicated comparison unit, triggers ADC and DMA
- Up to 6 capture inputs
- Pulse width measurement
- Quadrature encoder counting function
- Single pulse mode
- External counting function
- DMA trigger
- Dead-time control
- Braking control
- Cycle-by-cycle current limiting
- Edge alignment, symmetric center alignment and asymmetric center alignment PWM output

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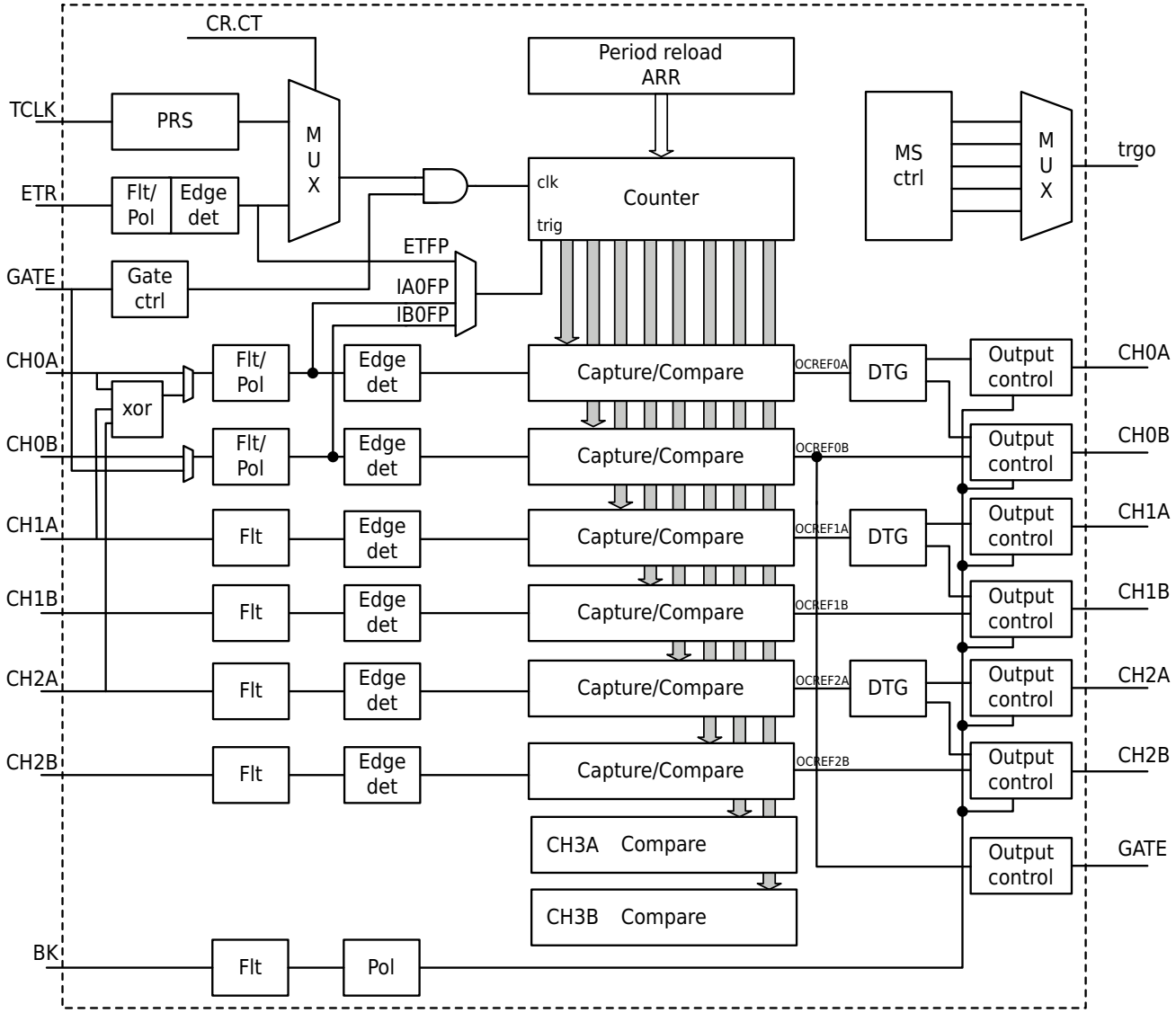

Figure 14-2 TIM3 Block Diagram

14.3 Functional Description

14.3.1 Timer Clock

The timer uses PCLK as the timer clock, and the timer clock is marked with TCLK below.

14.3.2 Timer Counter

The main module of programmable general timer consists of a 16-bit counter and its associated auto-reload register. The counter can count up, count down, or alternately count up and down. The counter clock can be divided by a prescaler.

The counter, auto-reload register and prescaler register can be read and written by software. Read and write operations can be performed even when the counter is running.

14.3.3 Timer Prescaler

When using TCLK as the timer clock, the prescaler can be used. The prescaler settings are as follows:

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PRS	0b000	0b001	0b010	0b011	0b100	0b101	0b110	0b111
Frequency division ratio	1	2	4	8	16	32	64	256

The prescaler does not have a preloaded buffer, so any changes to the prescaler will take effect immediately.

14.3.4 Mode 0 Count Timer Function

The counter counts up in this mode. The counter supports two counting modes, reload mode and free counting mode, and you can choose external clock ETR counting or system clock counting. The gate can control the count mask. Counting to the maximum overflow generates an interrupt. The inverted output signals TOG/TOGN are output through ports CHA/CHB.

The counting range of the reload mode counts up from ARR to 0xFFFF overflow, and then starts counting from ARR, and the counting period is 0xFFFF-ARR+1; the free counting mode overflows after counting from the set count value to 0xFFFFFFFF, and the count value restarts count from 0x0 after overflow.

The counter can be used to control whether the counter counts through the external gate control function. The control relationship is as follows:

M0CR.GATE	M0CR.GATEP	Port GATE Input	M0CR.CTEN	Counter
×	×	×	0	Not count
0	×	×	1	Count
1	0	High level	1	Count
1	0	Low level	1	Not count
1	1	High level	1	Not count
1	1	Low level	1	Count

Function Block Diagram

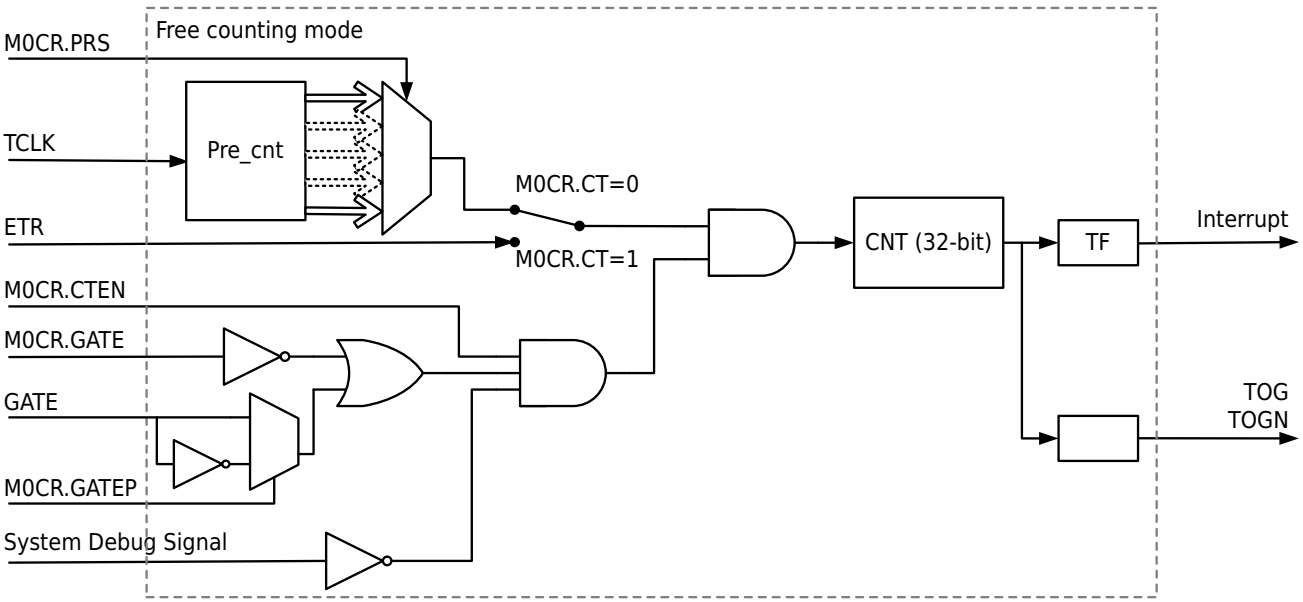

Figure 14-3 Mode0 Count Timer Free Counting Block Diagram

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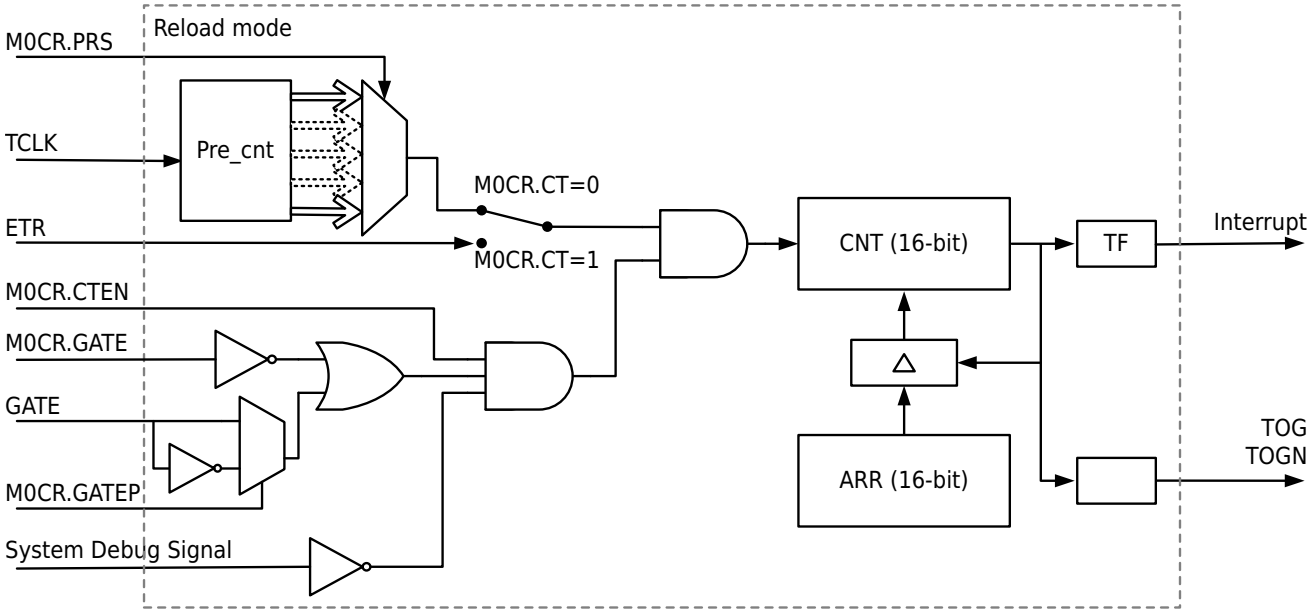

Figure 14-4 Mode0 Count Timer Reload Counting Block Diagram

Note

The "System Debug Signal" in the block diagram originates from DEBUG_ACTIVE.

Count Waveform

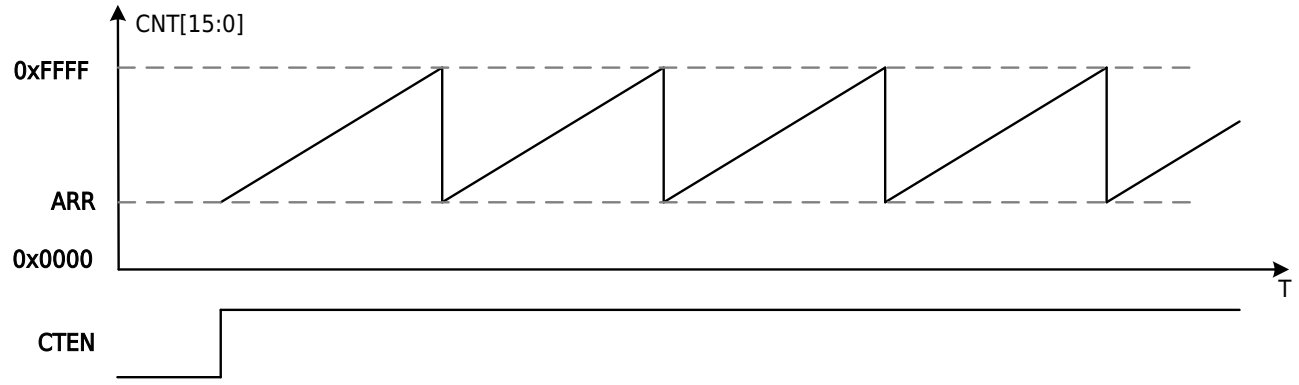

Figure 14-5 Mode0 Count Timer 16-Bit Reload Counting Waveform

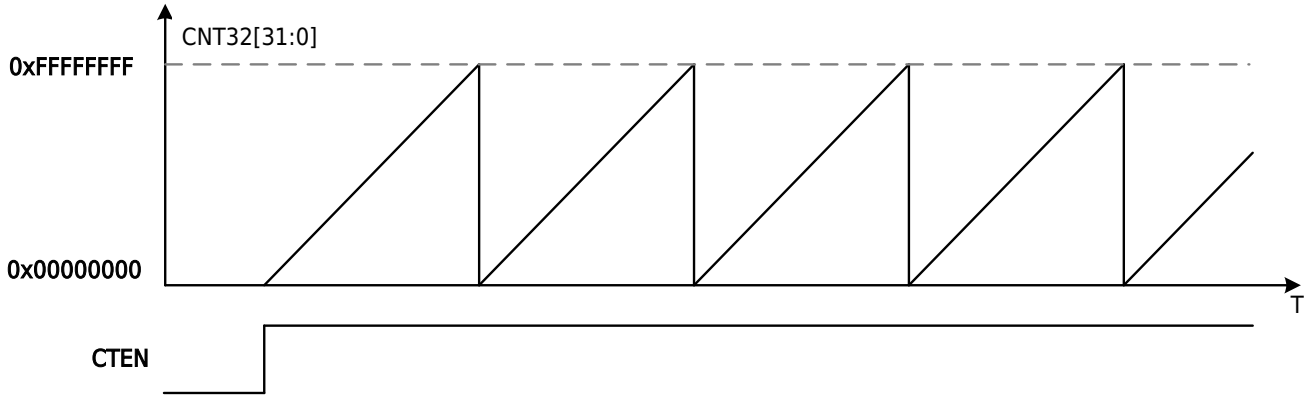

Figure 14-6 Mode0 Count Timer 32-Bit Free Counting Waveform

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Counting Function

Counting function are used to determine the number of times an event occurs. In the counting function, the counter increments every falling edge of the corresponding input clock. The input signal is sampled by the internal TCLK. Therefore, the external input signal must remain stable for a duration longer than one TCLK clock cycle. Counting to the maximum value will overflow and generate an interrupt. The interrupt flag needs to be cleared by software.

Notice

When the ETR input serves as the count clock of the counter, the ETR clock frequency must not exceed 1/2 of the TCLK clock.

Timing Function

The timing function is used to generate interval timing. In the timing function, the timer has a pre-divided frequency, and the timer accumulates once per clock of each pre-divided frequency. When counting to the maximum value, it will overflow and generate an interrupt. The interrupt flag needs to be cleared by software.

Timing Diagram

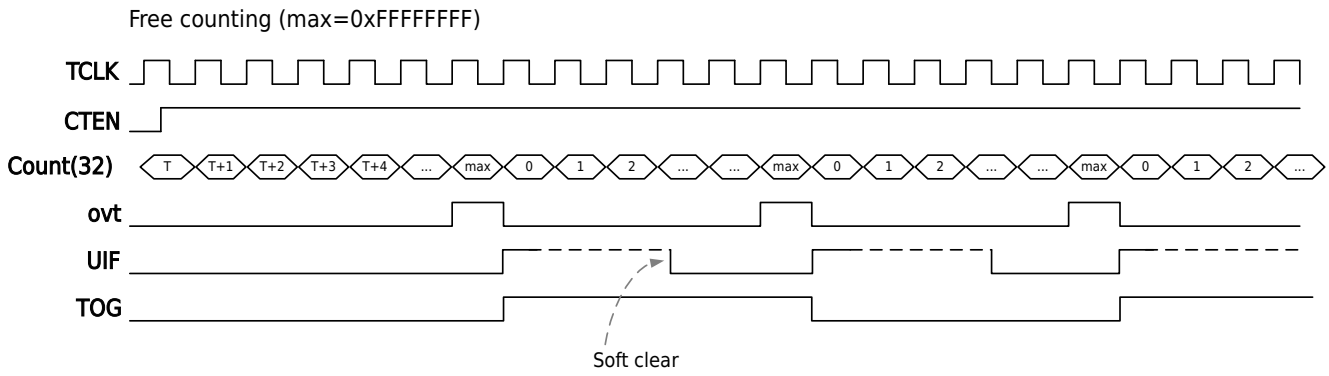

Figure 14-7 Mode0 Count Timer Free Counting Timing Diagram

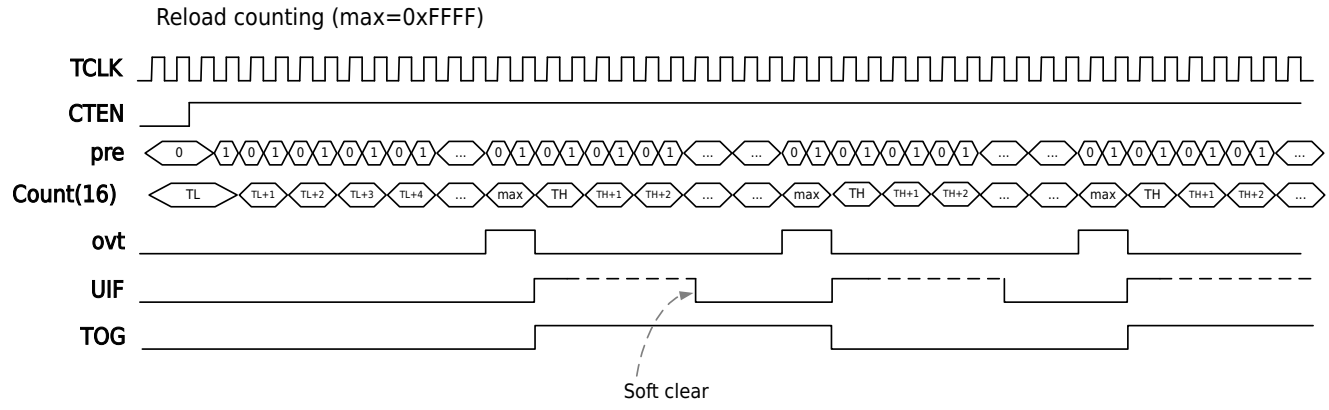

Figure 14-8 Mode0 Count Timer Reload Counting Timing Diagram (Prescaler=2)

Buzzer Function

The Buzzer function can be realized through the toggling output function of the timer. To use toggle output, the DTR.MOE control bit must be enabled. Setting M0CR.TOGEN to 0 simultaneously sets both CHA and CHB outputs to 0. The timer reload mode configurations for Buzzer output at different frequencies under a 4MHz counting clock are as follows:

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Buzzer Frequency	Counter Period	Counter Count Value	Counter Reload Value	CNT Initial Value	ARR Reload Value
1000Hz	0.5ms	2000	63536	0xF830	0xF830
2000Hz	0.25ms	1000	64536	0xFC18	0xFC18
4000Hz	0.125ms	500	65036	0xFE0C	0xFE0C

14.3.5 Mode 1 Pulse Width Measurement PWC

In this mode, the high level and low level or period width of the input pulse can be automatically measured.

The first valid edge counter initializes to 0x0001, the second valid edge will stop counting, store the current count value in CCR0A, generate a capture interrupt CA0F, and if the counter overflows, an overflow flag will be raised. Setting overflow interrupt enable will generate overflow interrupt.

M1CR.EDG1ST	0	0	1	1
M1CR.EDG2ND	0	1	0	1
Pulse width measurement	Upper edge-upper edge Cycle width	Upper edge-lower edge High level width	Lower edge-upper edge Low level width	Lower edge-lower edge Cycle width

During period measurement, a period is measured at intervals of one period.

PWC Function Block Diagram

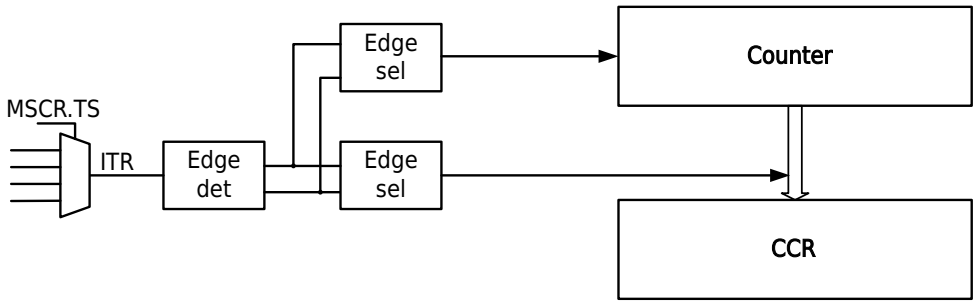

Figure 14-9 Mode1 Pulse Width Measurement PWC Function Block Diagram

Select the measurement signal source by registering MSCR.TS.

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Trigger Selection	Value	Signal Source
MSCR.TS	0b000	ETFP: ETR filtered external input phase selection signal, selectable between external filtered and input inverted phase
	0b001	ITR0: Timer internal interconnection signal 0, TRGO output from other timers
	0b010	ITR1: Timer internal interconnection signal 1, TRGO output from other timers
	0b011	ITR2: Timer internal interconnection signal 2, TRGO output from other timers
	0b100	ITR3: Timer internal interconnection signal 3, TRGO output from other timers
	0b101	IA0ED: Invalid
	0b110	IAFP: CH0A filtered external input phase selection signal, selectable between external filtered and input inverted phase (polarity selection invalid in pulse width measurement mode)
	0b111	IBFP: CH0B filtered external input phase selection signal, selectable between external filtered and input inverted phase (polarity selection invalid in pulse width measurement mode)

For TRGO output, refer to the corresponding register description.

Timer	ITR0	ITR1	ITR2	ITR3
Timer0	-	TIM1_TRGO	TIM2_TRGO	TIM3_TRGO
Timer1	TIM0_TRGO	-	TIM2_TRGO	TIM3_TRGO
Timer2	TIM0_TRGO	TIM1_TRGO	-	TIM3_TRGO
Timer3	TIM0_TRGO	TIM1_TRGO	TIM2_TRGO	-

PWC Waveform Measurement Timing Diagram

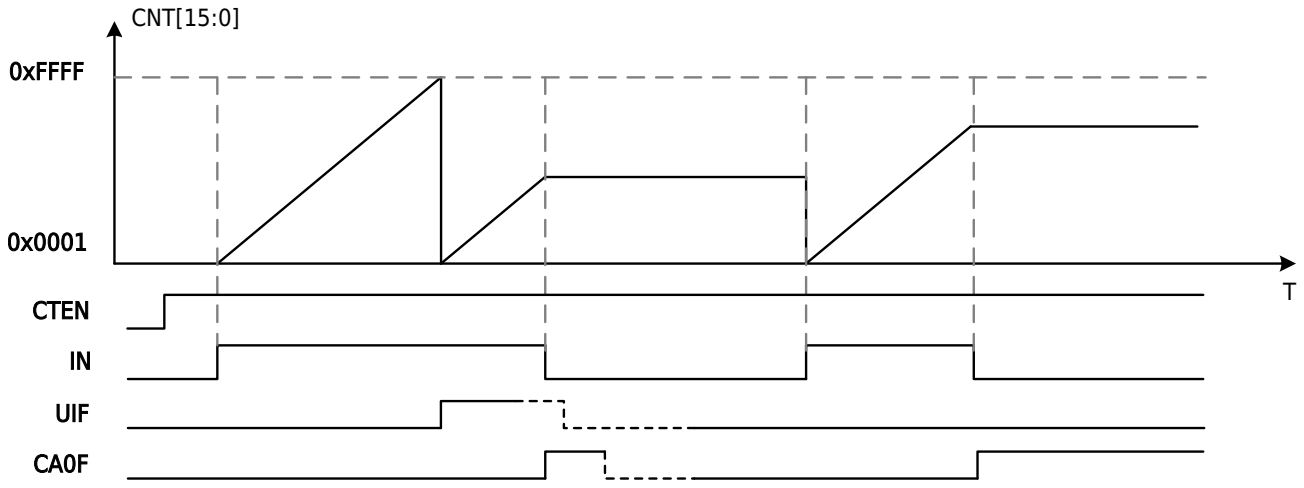

Figure 14-10 Mode1: Pulse Width Measurement PWC High-Level Pulse Width Measurement

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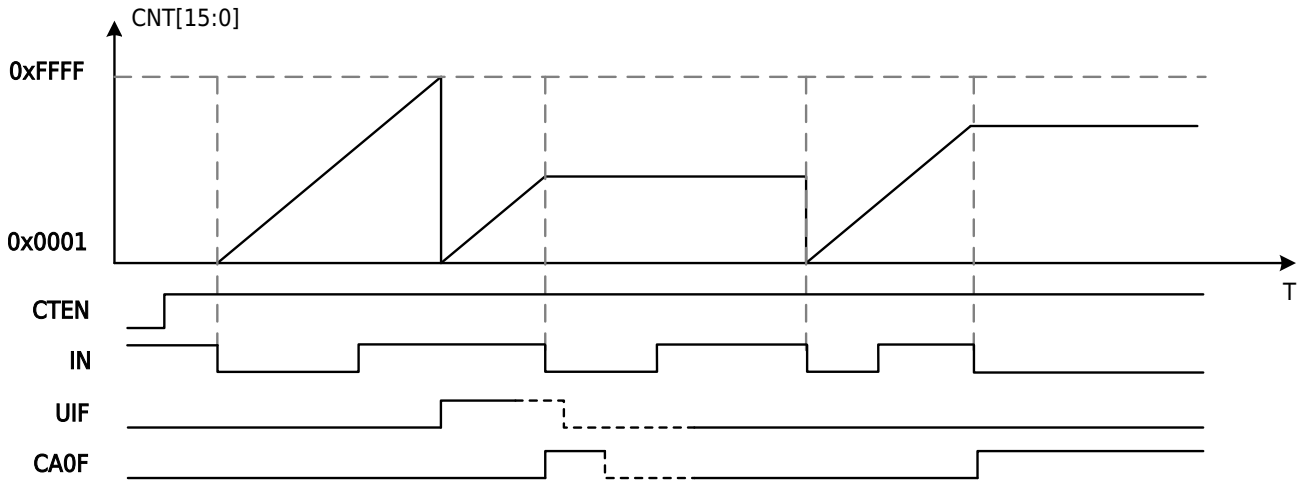

Figure 14-11 Mode1: Pulse Width Measurement PWC Falling Edge to Falling Edge Period Measurement

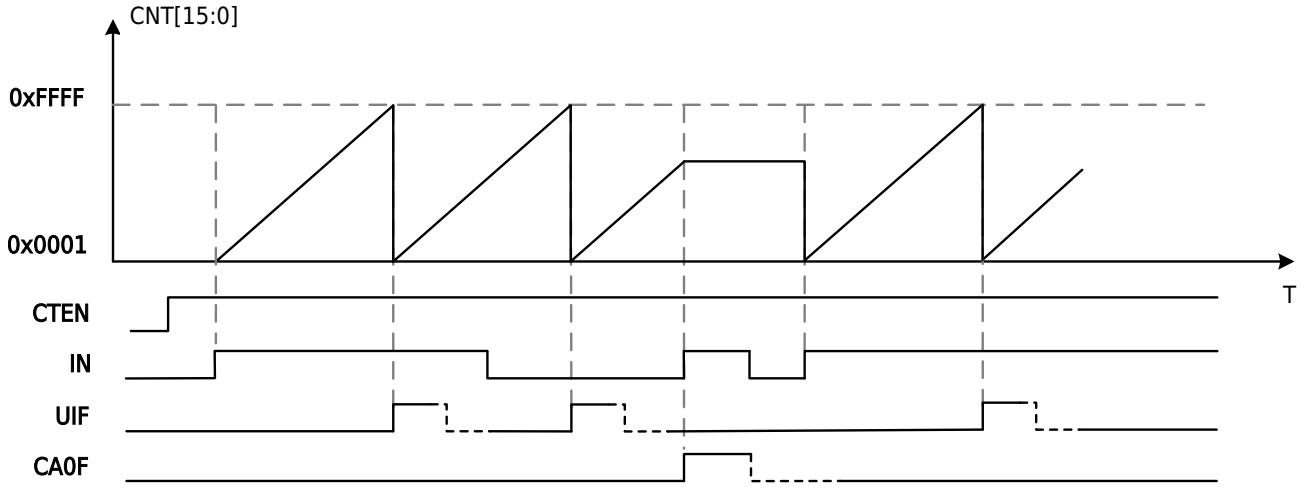

Figure 14-12 Mode1: Pulse Width Measurement PWC Rising Edge to Rising Edge Period Measurement

PWC Single trigger Mode

Set M1CR.ONESHOT=1 to set PWC single measurement, and CTEN will be cleared after the measurement is completed.

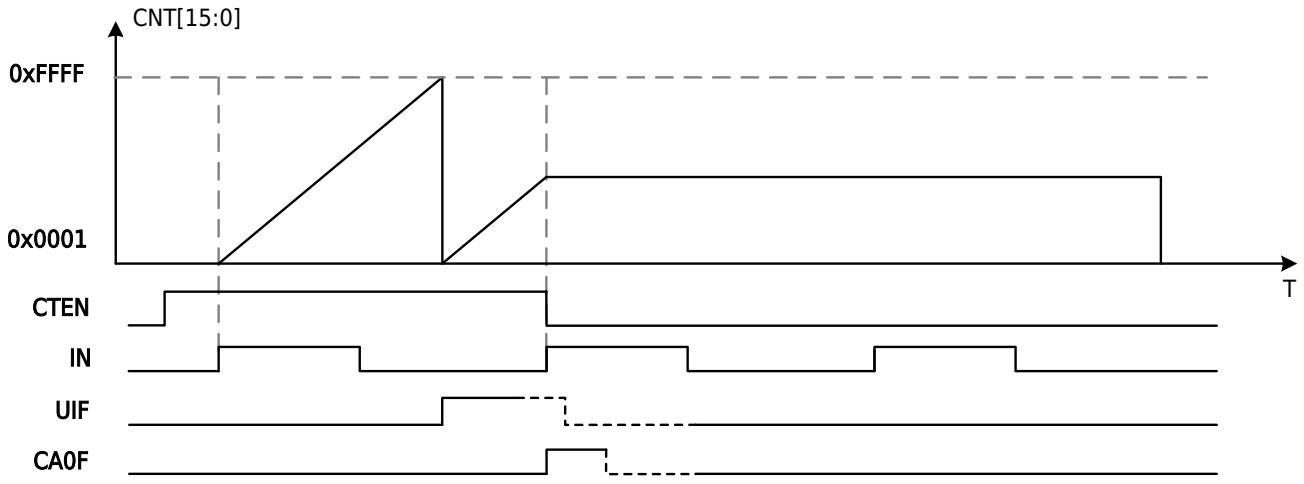

Figure 14-13 Mode1: Pulse Width Measurement PWC Rising Edge to Rising Edge Period Measurement Single Mode

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14.3.6 Mode2/3 Compare Capture Mode

14.3.6.1 Counter

The main part of the counter is a 16-bit counter with associated auto-loaded register. This counter can count up (mode 2), count down (mode 2) or count up and down in both directions (mode 3). The clock of the counter can be divided by the prescaler PRS, or ETR can be selected to input an external clock or the external input signal and internal interconnection signal selected by MSCR.TS.

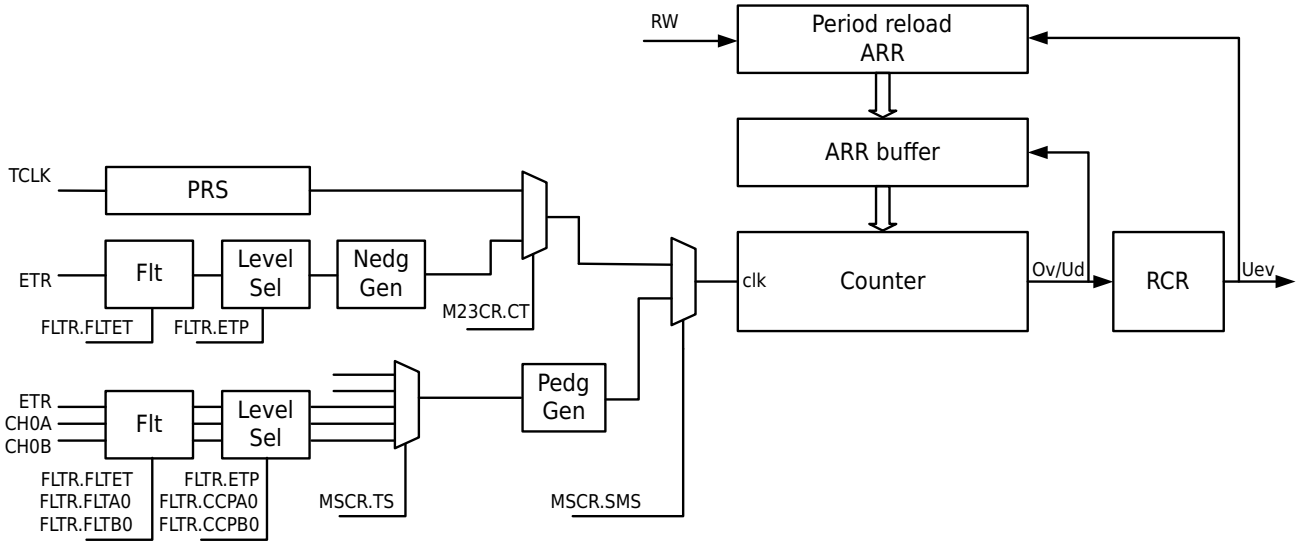

Figure 14-14 Mode 2/3 Compare Capture Mode Counter Block Diagram

The basic counter unit includes:

- Counter register CNT
- Prescaler register M23CR.PRS
- Auto-reload register ARR
- Repeat count register RCR
- Clock selection control registers FLTR, M23CR, MSCR

The auto-loaded register has a cache function, and the reload value is updated from the buffer register to the counter after the counter generates an event update. When the counter is in the stopped state or the cache function is disabled, the auto-reload register is immediately updated to the buffer register. When the timer is in the running state and the cache function is enabled, the value written to the auto-reload register is not immediately updated to the buffer register. The auto-reload register updates to the buffer register only after an event update occurs.

For clock selection and gating functions, trigger functions, and reset functions, refer to the relevant descriptions in the Mode2/3 Slave Mode chapter.

14.3.6.2 Counter Waveform

Mode 2 Sawtooth Counting Waveform

Mode 2 operates as a sawtooth counting waveform, and the counting direction can be changed by configuring M23CR.DIR.

When M23CR.DIR is set to 0, the counter operates in up-counting mode. In this mode, the counter increments from 0 to the auto-reload value (TIMx_ARR), then start counting from 0 again and generates a counter overflow event. If the repeat counter is used, an update event (UEV) is generated when the

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number of up-counting repetitions reaches the programmed value in the repeat counter register plus one (TIMx_RCR+1). Otherwise, an update event is generated on every counter overflow.

An update event is also generated when M23CR.UG is set to 1 (either by software or using the slave mode controller).

When the update event occurs, all registers will be updated and the update flag (TIMx_IFR.UIF bit) will be set to 1 (depending on the M23CR.URS bit):

- The auto-reload cache value will be updated with the ARR register value
- The compare buffer values will be updated with the compare register CCRxy.

The following diagrams illustrate the counter waveforms for different counting directions when ARR = 0x2C. The number of count overflow period clocks is ARR+1.

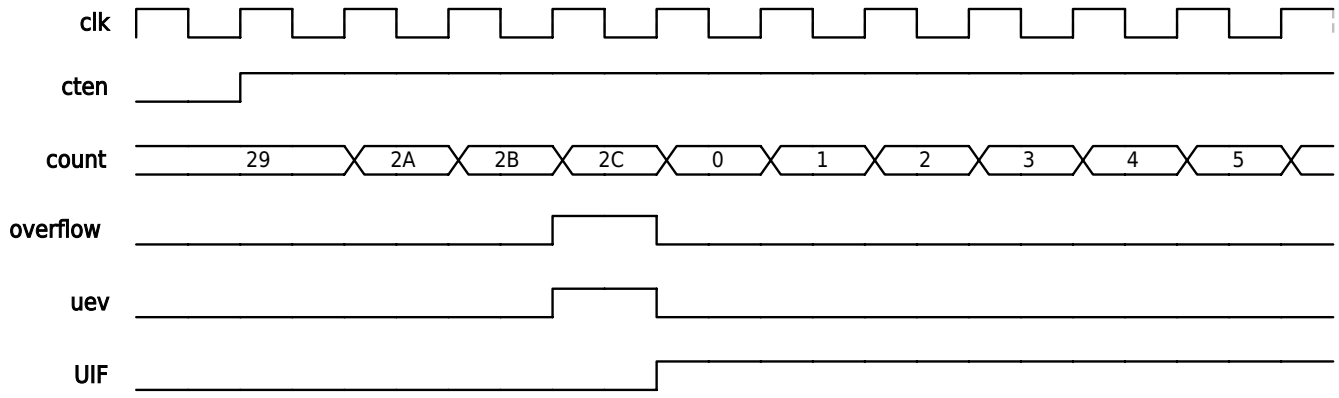

Figure 14-15 Mode 2 Compare Capture Mode Up-Counting Without Prescaler

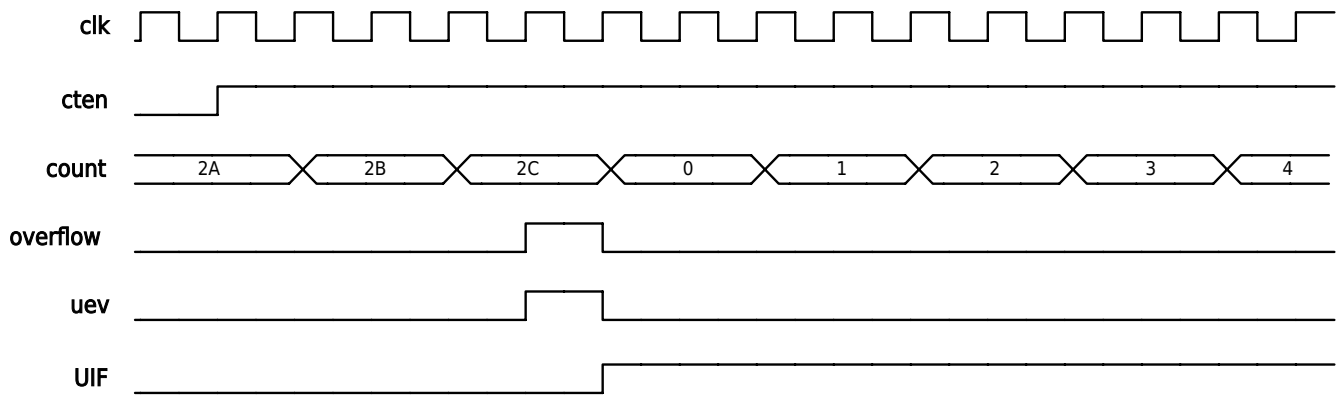

Figure 14-16 Mode 2 Compare Capture Mode Up-Counting With Prescaler

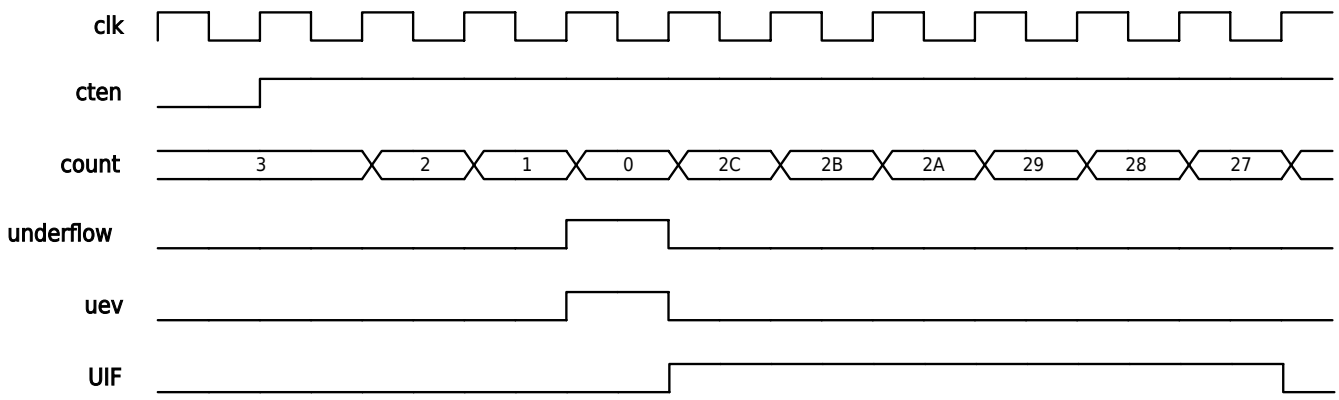

Figure 14-17 Mode 2 Compare Capture Mode Down-Counting Without Prescaler

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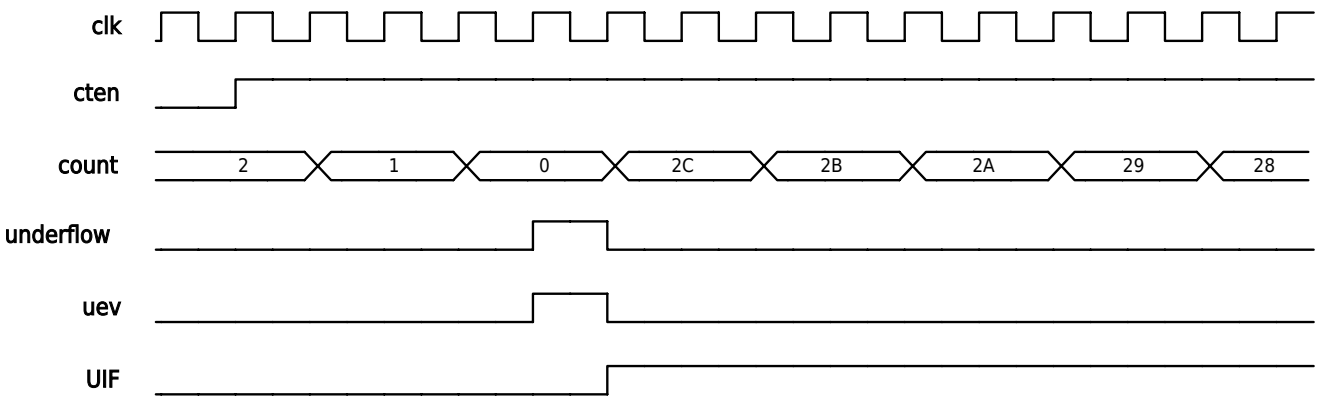

Figure 14-18 Mode 2 Compare Capture Mode Down-Counting With Prescaler

The counting waveforms for mode 2 are shown in the following diagrams:

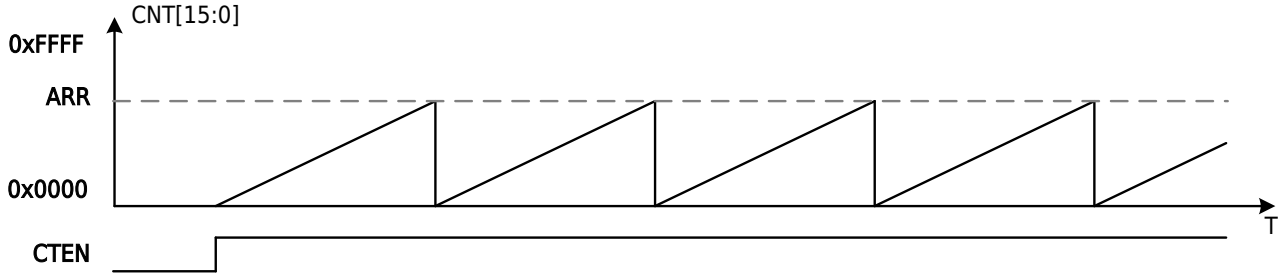

Figure 14-19 Mode2 Edge-Aligned Timer Waveform (M23CR.DIR=0)

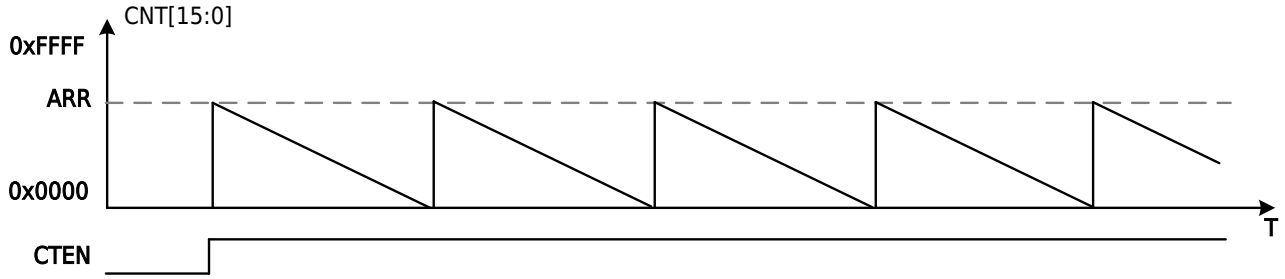

Figure 14-20 Mode2 Edge-Aligned Timer Waveform (M23CR.DIR=1)

Mode3 Triangular Counting Waveform

Mode 3 is a triangular counting waveform, the counting direction control bit is read-only, and the counting direction cannot be changed.

In center-aligned (triangular wave) mode, the M23CR.DIR direction bit is read-only, and writing to it has no effect. Switching from other modes to center-aligned mode DIR is automatically cleared to 0. DIR is automatically cleared in reset mode by software event update and external trigger in slave mode.

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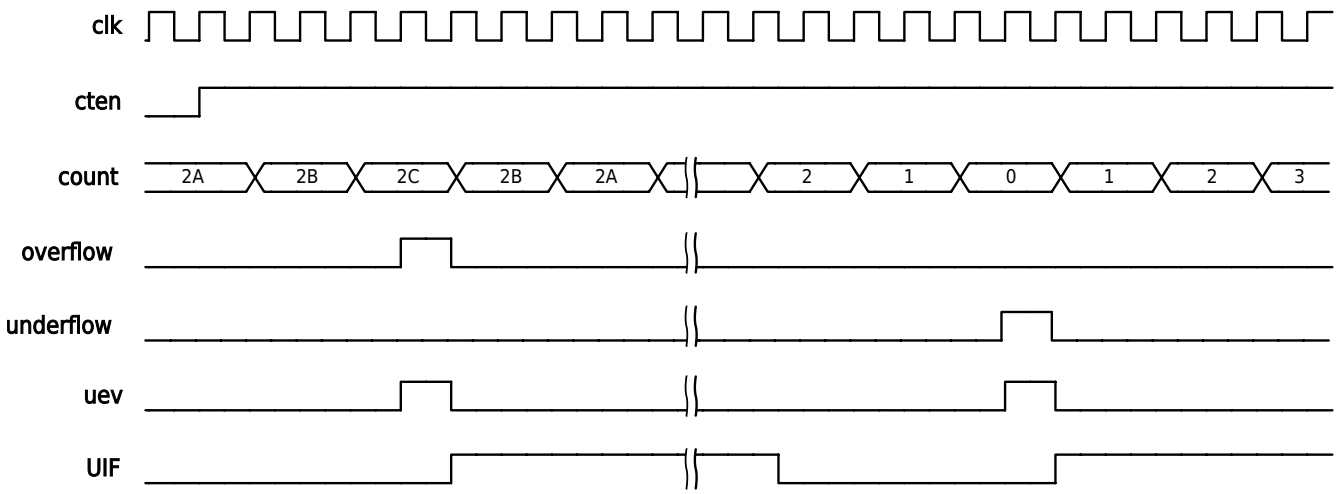

Figure 14-21 Mode3 Compare Capture Mode Up/Down-Counting with Prescaler

The counting waveforms for mode 3 are shown in the following diagrams:

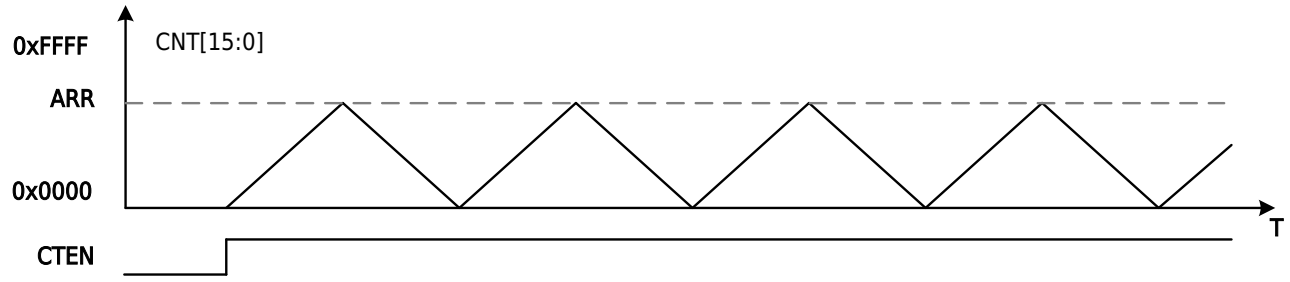

Figure 14-22 Mode3 Center-Aligned Counter Waveform

14.3.6.3 Repeat Counting

The repeat counter performs down-counting using counter overflows. When counting reaches 0, that is, when the counter overflows by the value set in the repeat register plus one. If buffer register is enabled, the period reload register updates to the period buffer register. In compare mode, the compare register value updates to the compare buffer register.

The repetition counter decrements when the following conditions are met (when RCR.UND=0 and RCR.OV=0):

- In up-counting mode: upon each counter overflow
- In down-counting mode: upon each counter underflow
- In triangular wave mode: upon each overflow and underflow

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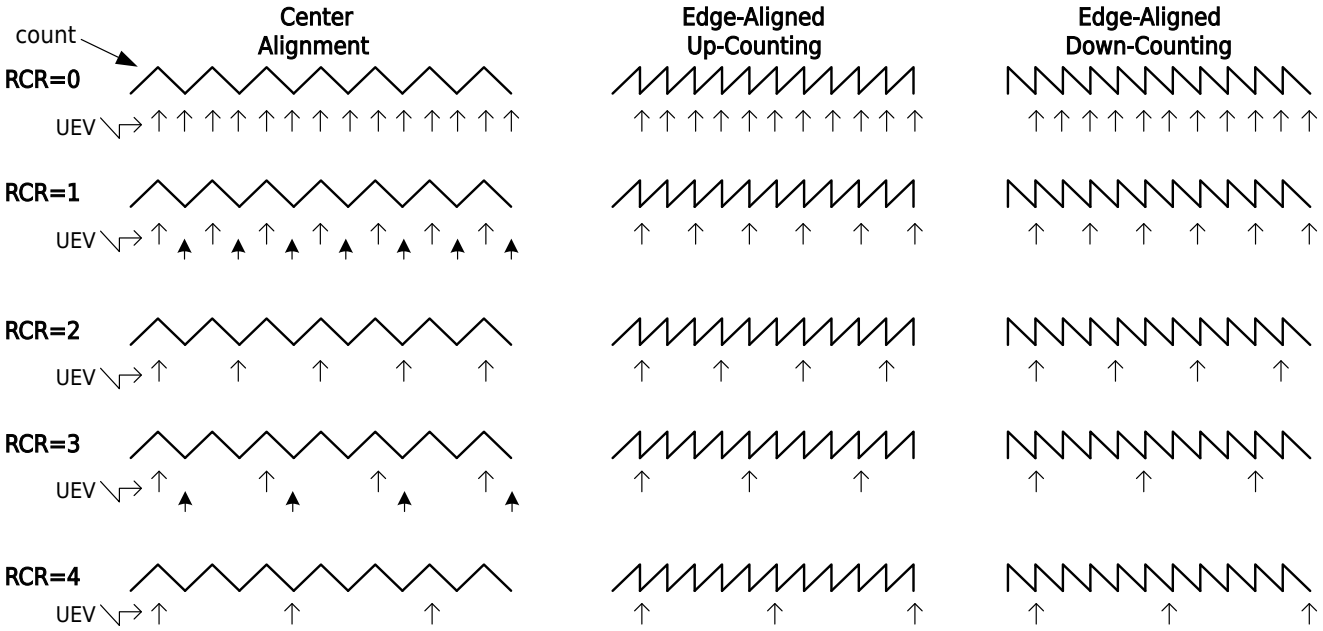

Figure 14-23 Repetition Counter Generates Update Timing (RCR.OV=0, RCR.UND=0)

RCR.OV is the overflow mask control bit for the repeat counter. When RCR.OV=1, overflow events are ignored during repeat counting.

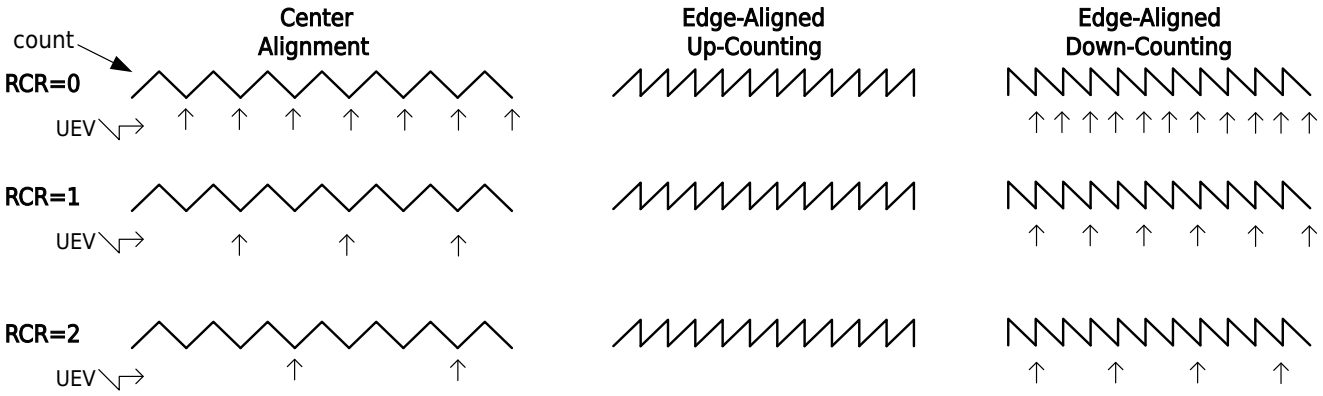

Figure 14-24 Update Timing Generated by Repetition Counter when Overflow Is Masked (RCR.OV=1, RCR.UND=0)

RCR.UND is the underflow mask control bit for the repetition counter. If RCR.UND is 1, underflow events will be ignored during repetition counting.

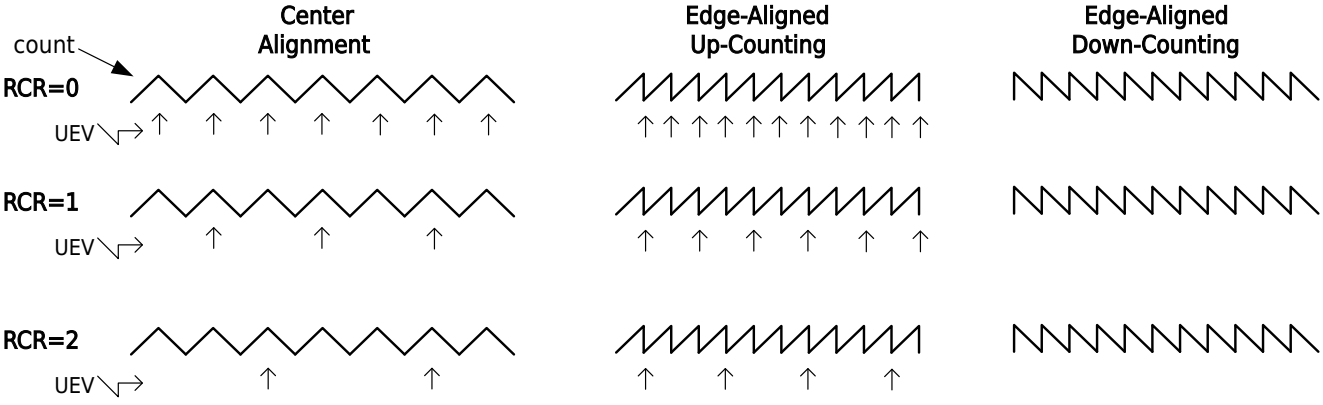

Figure 14-25 Update Timing Generated by Repetition Counter when Underflow Is Masked (RCR.OV=0, RCR.UND=1)

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In addition to events update (UEV) generated by overflow/underflow through the repeat counter, software-triggered and slave-mode reset events update (UEV) can also be generated by writing to register M23CR.UG. This operation requires configuration of M23CR.URS.

14.3.6.4 Data Buffer

Both the auto-reload data (ARR) and compare registers (CCRxy) can be configured with buffering function. When buffering function is enabled, the written period value (ARR) and compare value (CCRxy) only take effect upon a UEV event update.

The update timing diagrams for the auto-reload value under different counting modes are shown below:

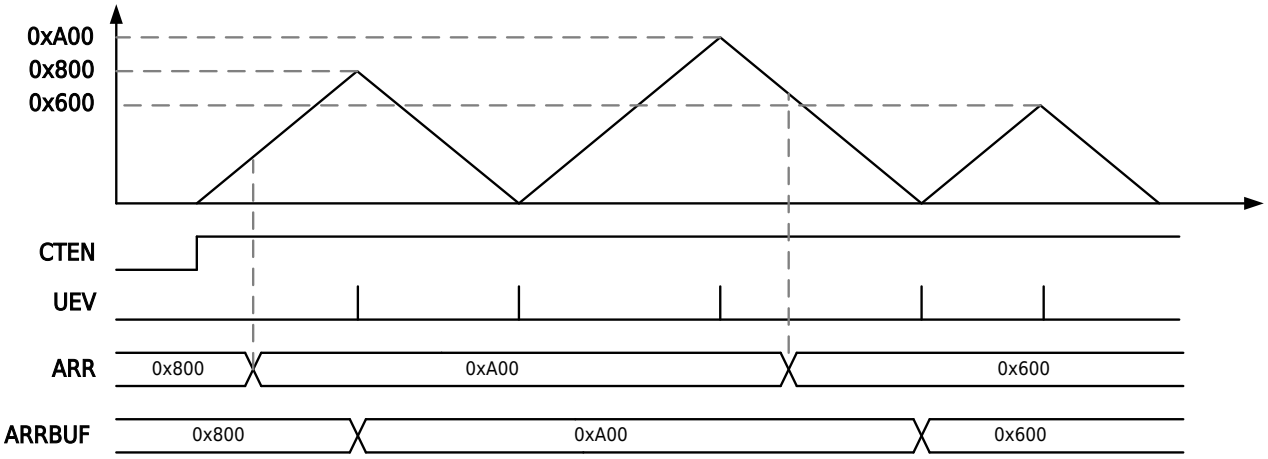

Figure 14-26 Mode 3 Triangular Wave Mode with Cache Enable

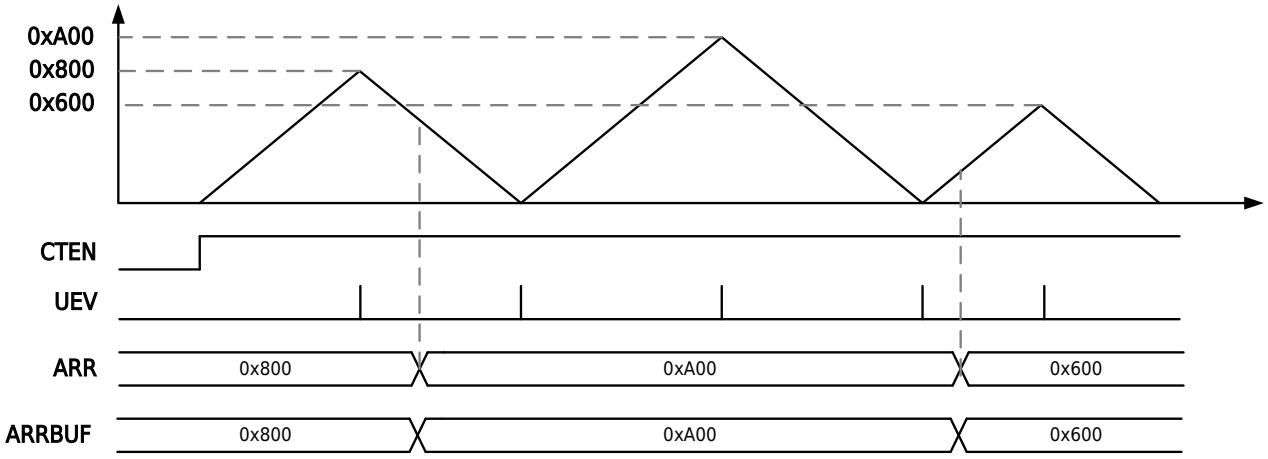

Figure 14-27 Mode 3 Triangular Wave Mode with Cache Invalid

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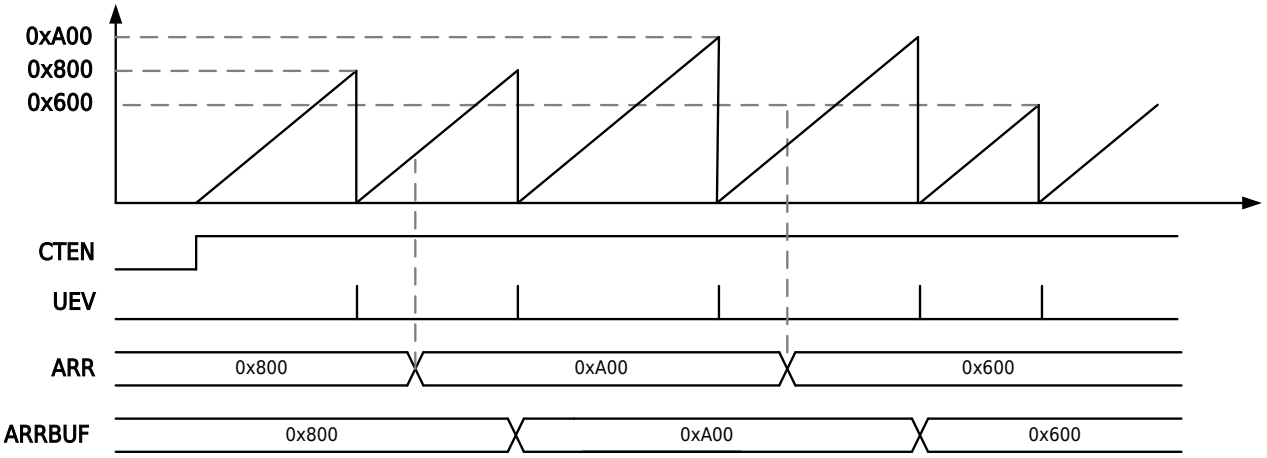

Figure 14-28 Mode 2 Sawtooth Wave Mode Up-Counting with Cache Enable

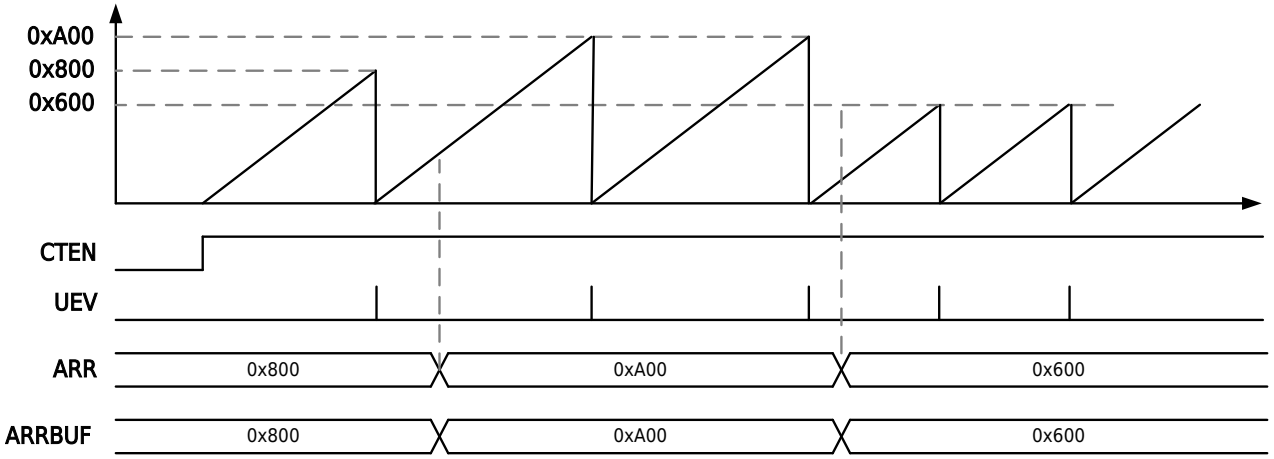

Figure 14-29 Mode 2 Sawtooth Wave Mode Up-Counting with Cache Invalid

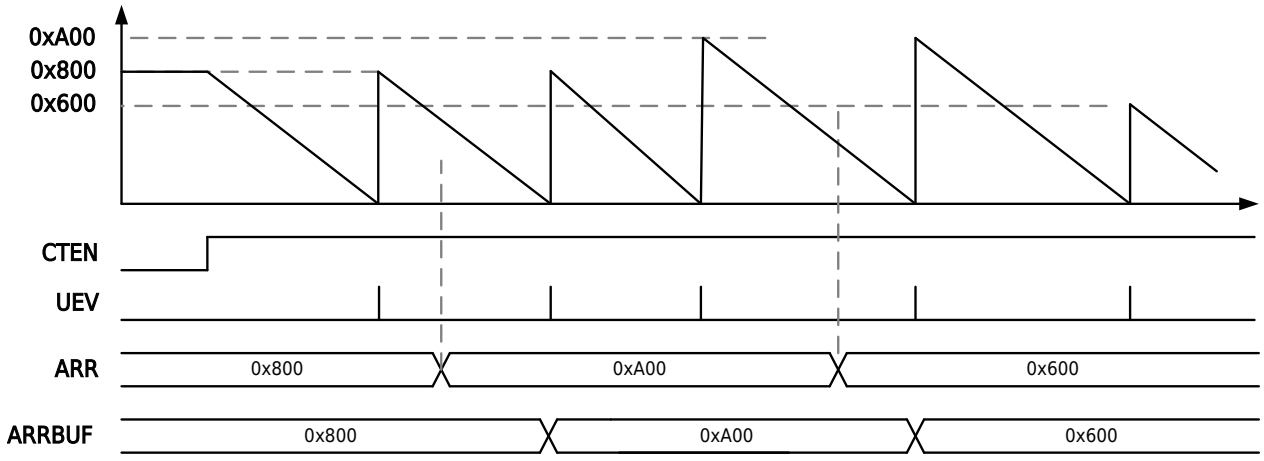

Figure 14-30 Mode 2 Sawtooth Wave Mode Down-Counting with Cache Enable

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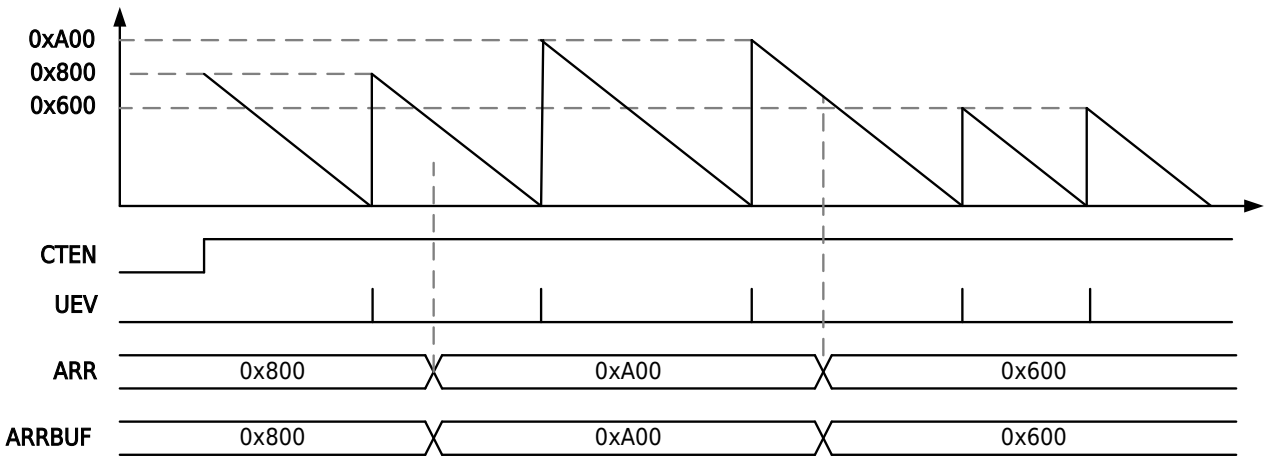

Figure 14-31 Mode 2 Sawtooth Wave Mode Down-Counting with Cache Invalid

Note

In triangular wave mode and sawtooth up-counting mode, when cache is disabled and the ARR value is modified, the current counter value must be less than the ARR period value to be changed; otherwise, the current cycle will count up to 0xFFFF.

The update behavior of the compare cache and period cache remains consistent, therefore their timing diagrams are not listed individually here.

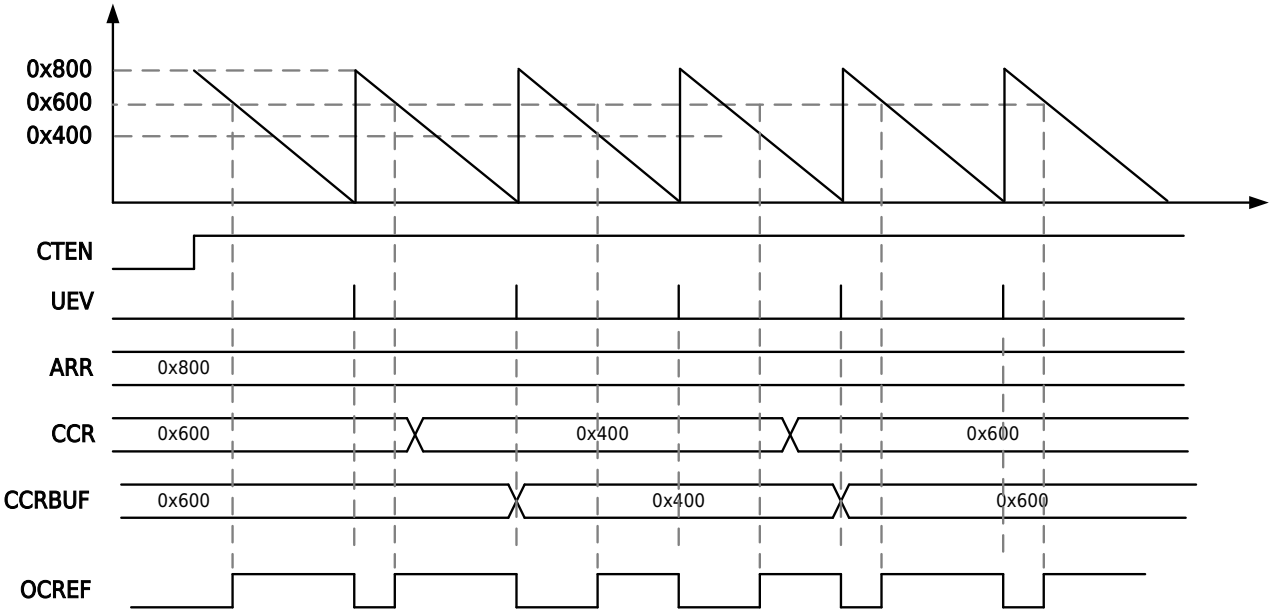

Figure 14-32 Mode2 Sawtooth Wave Down-Counting Mode with Compare Cache Enable

14.3.6.5 Compare Output OCREF

The compare output OCREFA can be configured for single point comparison, where the OCREFA output is controlled by compare register CCRA. Alternatively, OCREFA compare output can be configured for dual point comparison, where its output is jointly controlled by compare registers CCRA and CCRB.

OCREFB can only use single point comparison, and the comparison register CCRB is used to control the comparison output of OCREFB.

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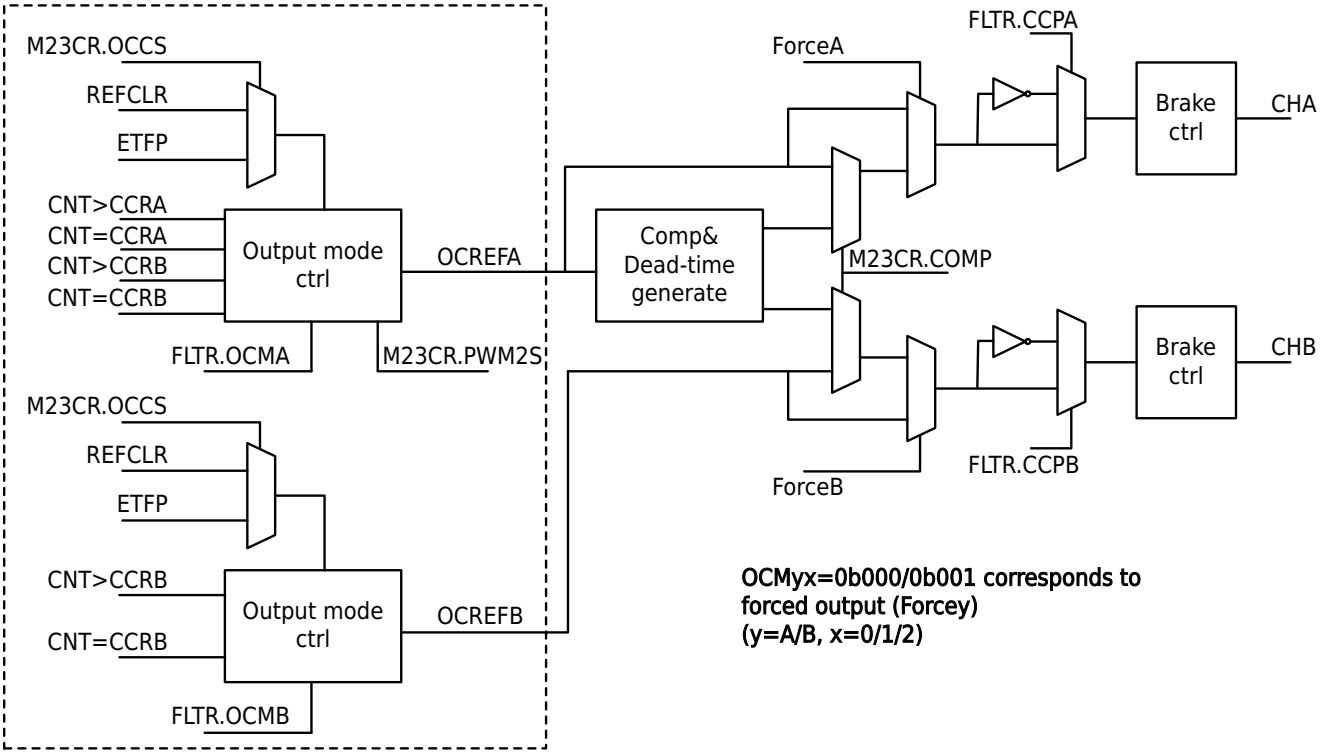

Figure 14-33 OCREF Output Block Diagram

OCREF output uses TIMx_FLTR.OCMyx selection:

- 0b000: Force to 0
- 0b001: Force to 1
- 0b010: Force to 0 on compare match
- 0b011: Force to 1 on compare match
- 0b100: Toggle on compare match
- 0b101: Output high level for one clock cycle on compare match
- 0b110: PWM mode 1
  - Single point comparison

    During up-counting, the output is high level when CNT<CCRxy; during down-counting, the output is low level when CNT>CCRxy.
  - Dual point comparison
    - For sawtooth wave up-counting, the output is low level when CCRxA<CNT≤CCRxB
    - For sawtooth wave down-counting, the output is high level when CCRxA<CNT≤CCRxB
    - For triangular wave up-counting, the output is high level when CNT<CCRxA; for down-counting, the output is low level when CNT>CCRxB
- 0b111: PWM mode 2
  - Single point comparison

    During up-counting, the output is low level when CNT<CCRxy; during down-counting, the output is high level when CNT>CCRxy
  - Dual point comparison
    - For sawtooth wave up-counting, the output is high level when CCRxA≤CNT<CCRxB
    - For sawtooth wave down-counting, the output is low level when CCRxA≤CNT<CCRxB
    - For triangular wave up-counting, the output is low level when CNT<CCRxA; for down-counting, the output is high level when CNT>CCRxB

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Note

Forced output has higher priority. When forced output is active, complementary output control becomes invalid.

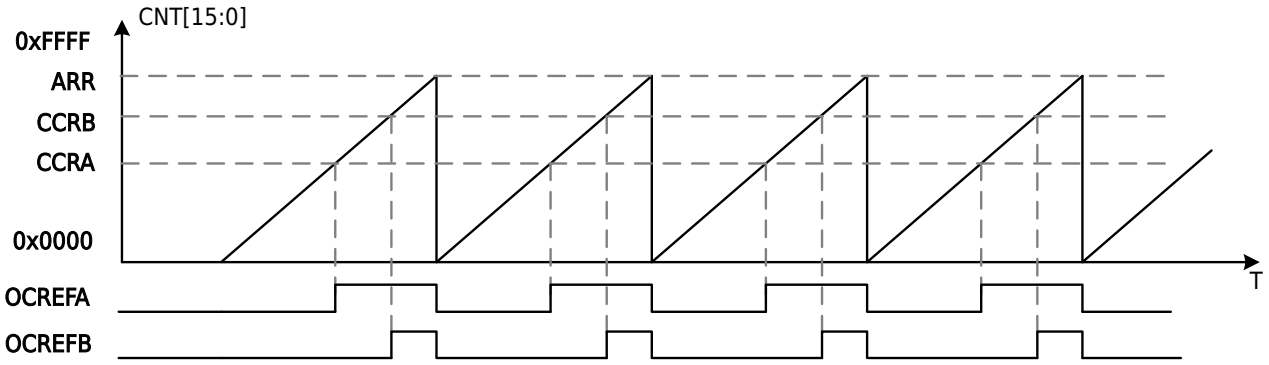

Figure 14-34 Sawtooth Counting Single Point Comparison OCREF Output Waveform (OCMyx=0b111)

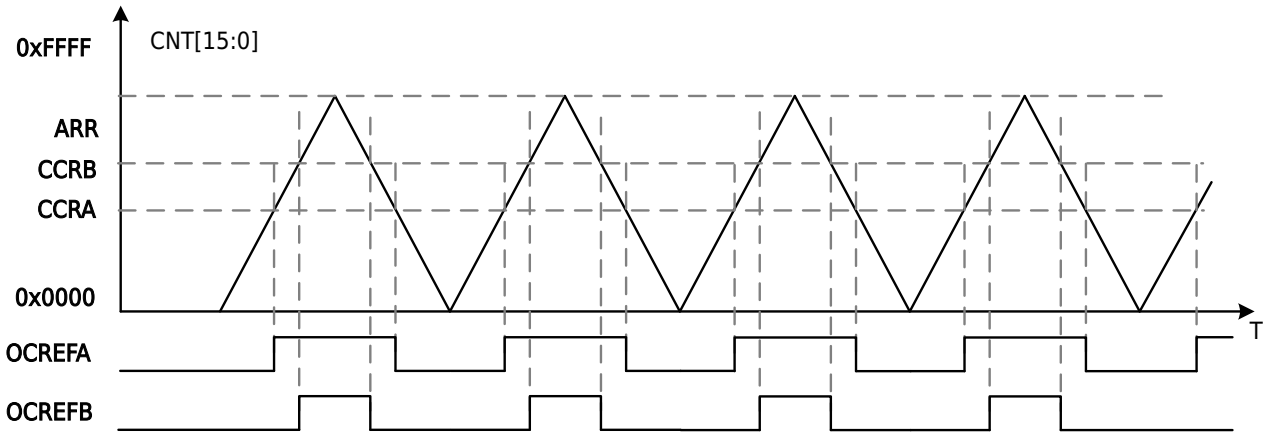

Figure 14-35 Triangular Counting Single Point Comparison OCREF Output Waveform (OCMyx=0b111)

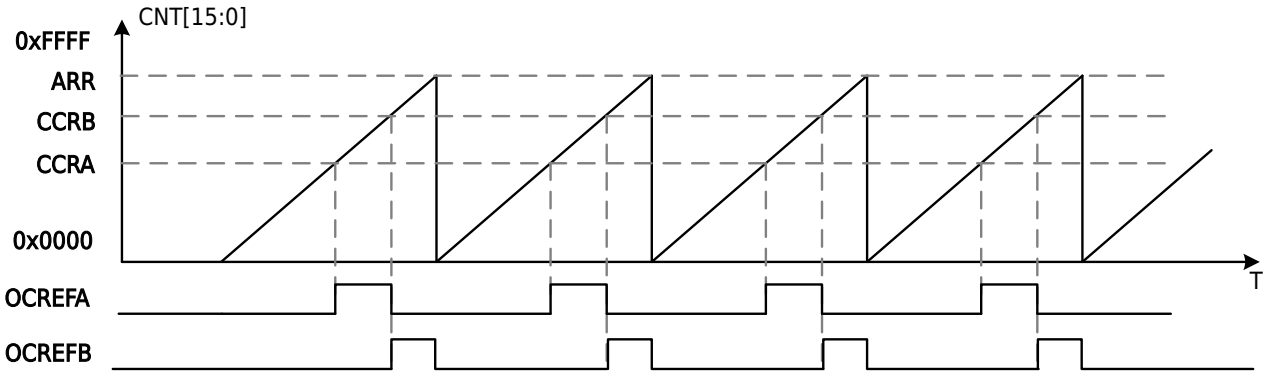

Figure 14-36 Sawtooth Counting Dual Point Comparison OCREF Output Waveform (OCMyx=0b111)

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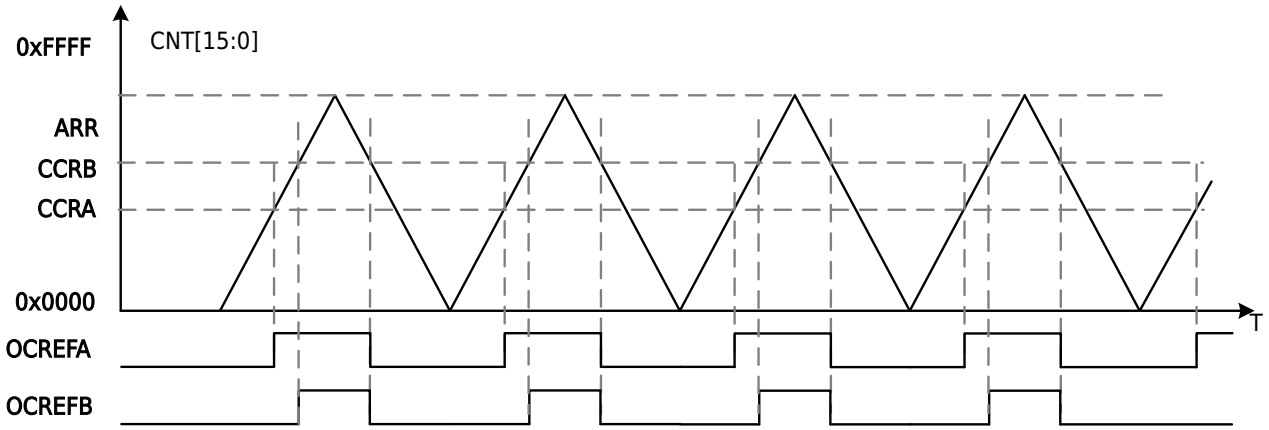

Figure 14-37 Triangular Counting Dual Point Comparison OCREF Output Waveform (OCMyx=0b111)

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14.3.6.6 Independent PWM Output

The output of CHA is controlled by OCREFA, and the output of CHB is controlled by OCREFB. The inversion of CHA and CHB outputs can be controlled through FLTR.CCPA and FLTR.CCPB respectively.

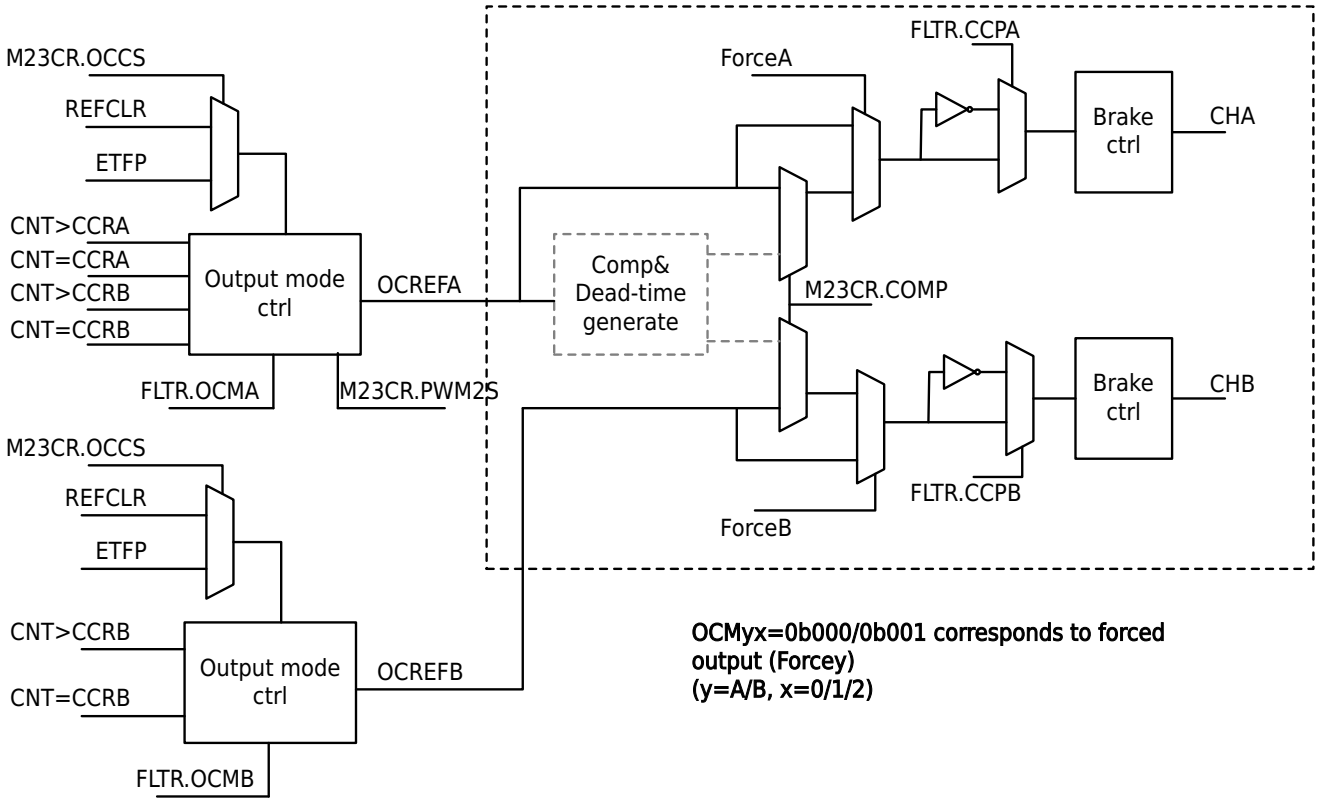

Figure 14-38 Independent PWM Output Block Diagram

PWM output and OCREF relationship, as shown in the following diagram:

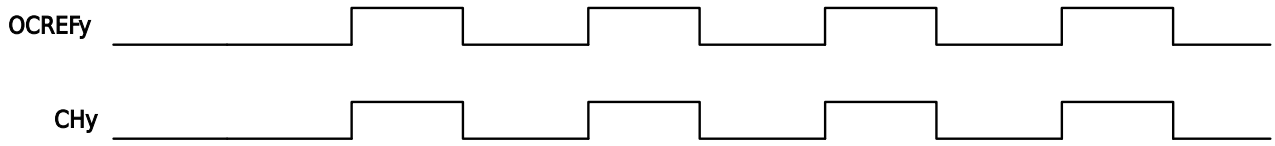

Figure 14-39 PWM Output Waveform When CCPy=0

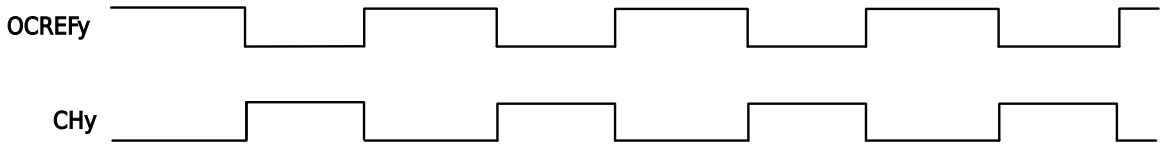

Figure 14-40 PWM Output Waveform When CCPy=1

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14.3.6.7 Complementary PWM Output

CHA is controlled by OCREFA, and OCREFA controls the output of CHB at the same time. The compare register CCRxB can be used as a dedicated compare control ADC trigger.

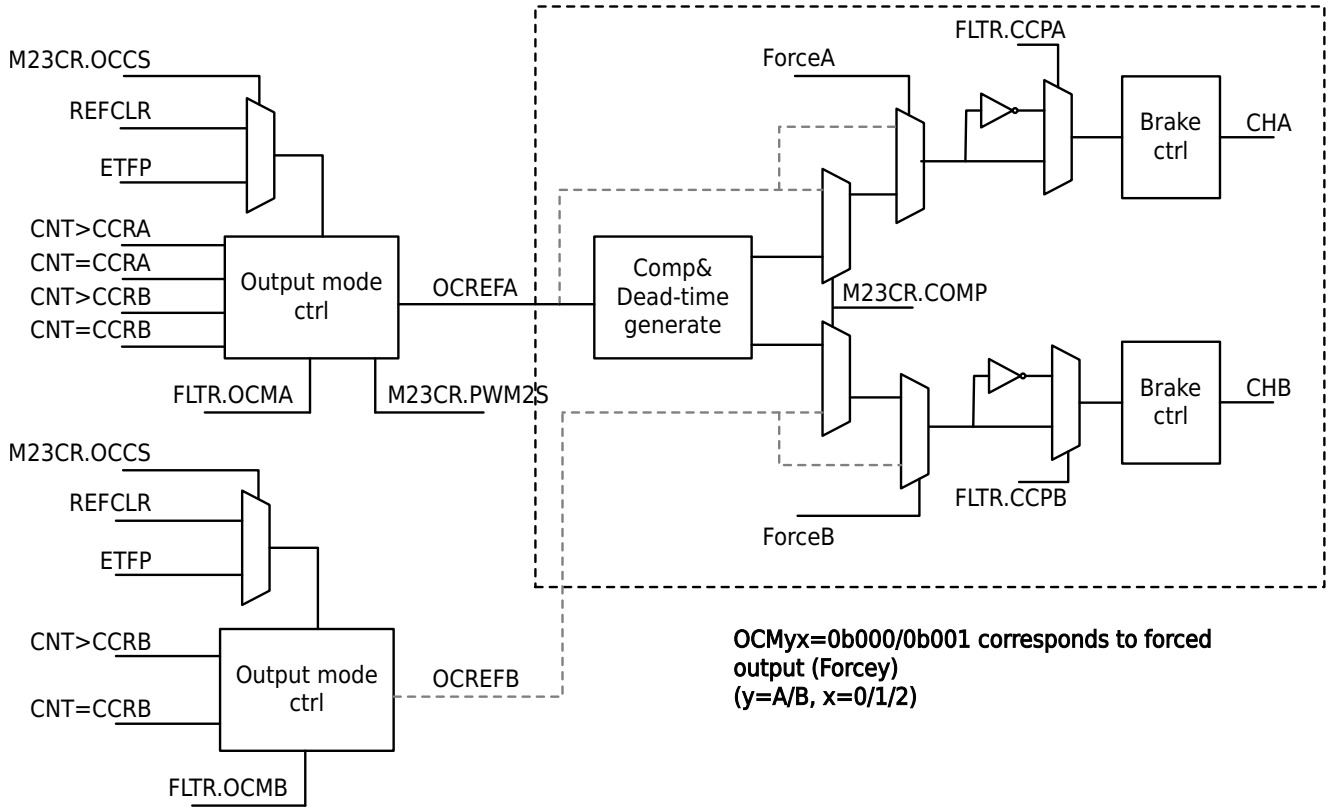

Figure 14-41 Complementary PWM Output Block Diagram

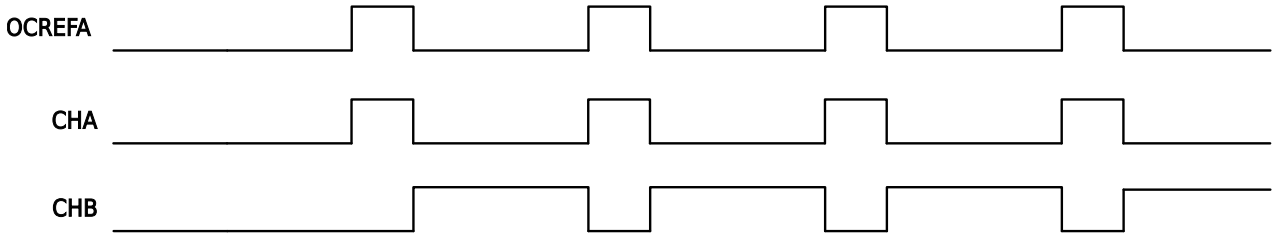

Figure 14-42 Complementary PWM Output Waveform

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14.3.6.8 PWM Output with Dead Time

The dead time function can be set in complementary PWM output mode.

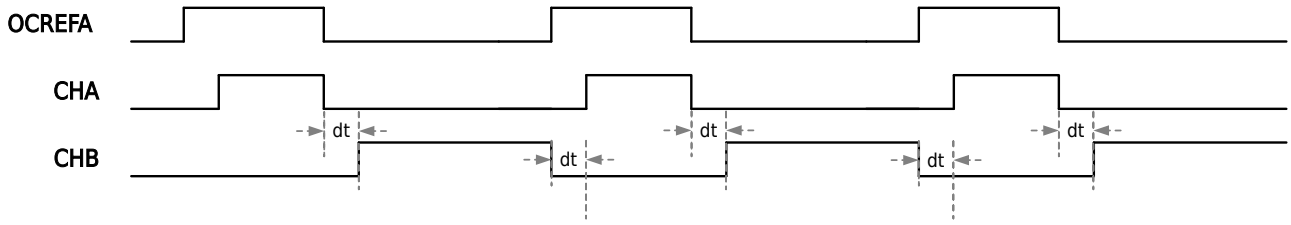

Figure 14-43 Complementary PWM Output Waveform (with Dead Time)

The dead time duration is controlled by 8-bit DTR. The relationship between dead time dt and DTR is as follows:

DTR	T	dt	step
DTR[7]=0b0	DTR[6:0] + 2	2-129	1
DTR[7:6]=0b10	{DTR[5:0] + 64}* 2 + 2	130-256	2
DTR[7:5]=0b110	{DTR[4:0] + 32}* 8 + 2	258-506	8
DTR[7:5]=0b111	{DTR[4:0] + 32}* 16 + 2	514-1010	16

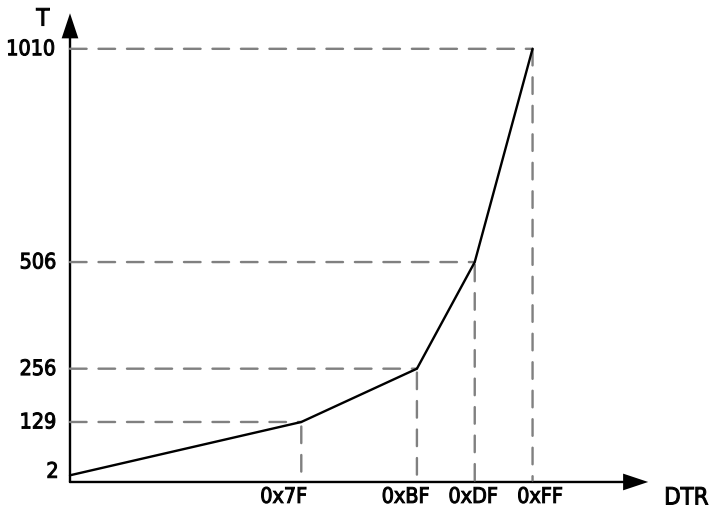

Figure 14-44 Dead Time

Note

When TCLK is 48MHz and M23CR.PRS is set to 0, the dead time is adjusted from 5.33μs to 21.04μs.

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14.3.6.9 Single Pulse Output

Single pulse mode (ONESHOT) is a special case of the aforementioned PWM modes. In this mode, the counter can be triggered to start by an excitation signal and generate a programmable width pulse, as shown in the following diagram.

The counter can be started by the slave mode controller. Waveforms can be generated in either output compare mode or PWM mode. Setting the TIMx_M23CR.ONESHOT register to 1 enables single pulse mode. Thus, when the next update event (UEV) occurs, the counter will automatically stop.

Single pulse mode in sawtooth wave down-counting mode, the counter initial value should not be set to 0, and the count value in up-counting mode should not be set to a value greater than or equal to ARR.

Output pulse can only be correctly generated when the compare value differs from the counter initial value. Before starting (when the timer is waiting for a trigger), the following configurations must be made:

- For increment counting: CNT<CCRxy≤ARR (special attention: CCRxy>0)
- For decrement counting: CNT>CCRxy

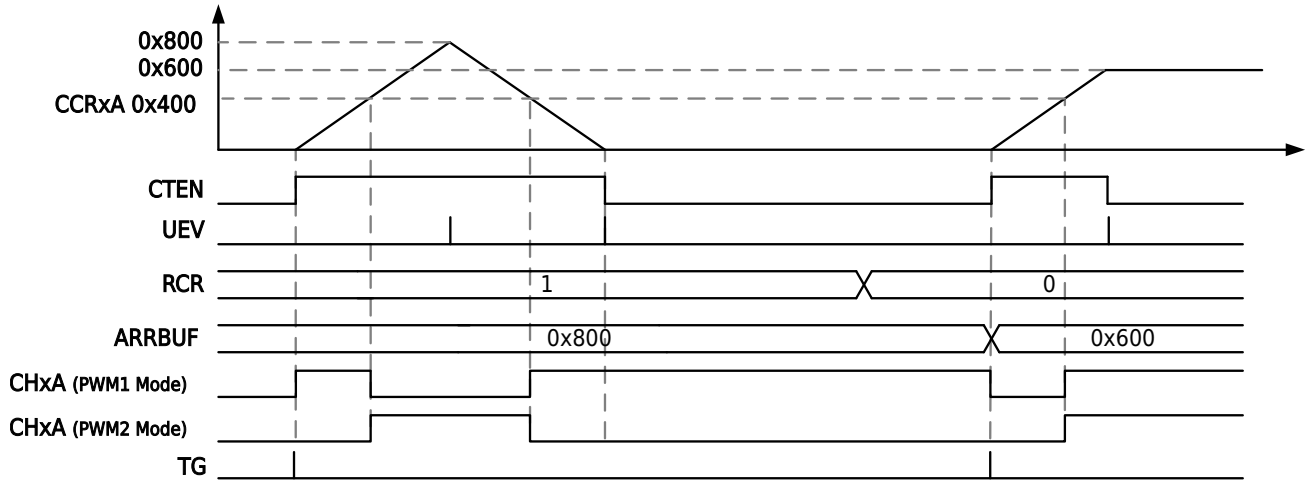

Figure 14-45 Triangular Wave Mode Single Pulse Counting

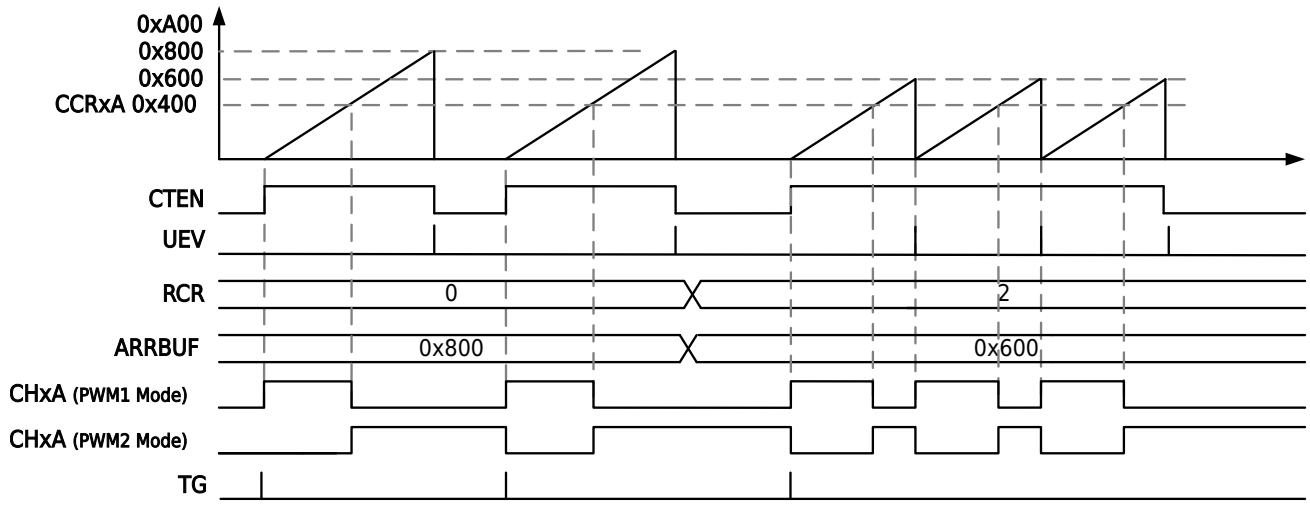

Figure 14-46 Sawtooth Up-Counting Single Pulse Mode

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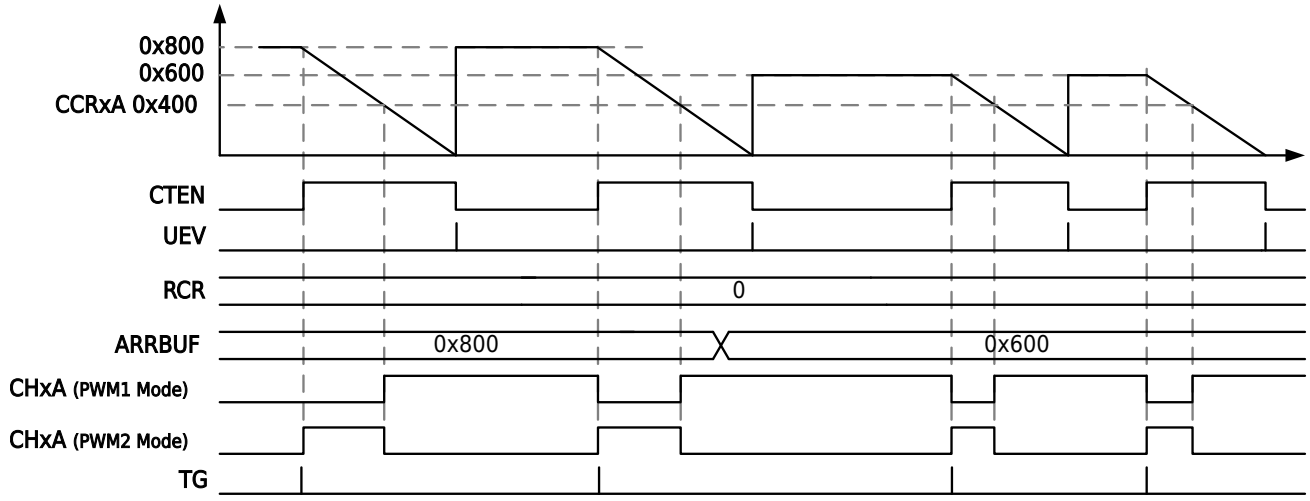

Figure 14-47 Sawtooth Down-Counting Single Pulse Mode

Notice

In up-counting, when configured as PWM2 mode, since the channel initial output is low level, the first trigger will generate a rising edge and maintain a high level. Upon the second trigger, a programmable width low level pulse can be output. In down-counting, when configured as PWM1 mode, since the channel initial output is low level, the first trigger will generate a rising edge and maintain a high level. Upon the second trigger, a programmable width low level pulse can be output.

14.3.6.10 Compare Interrupt

Sawtooth wave compare match will set the corresponding flag in the IFR register to 1. If the interrupt enables CRCHx.CIEy (x=0/1/2; y=A/B), an interrupt will be triggered.

For triangular wave compare match, it can independently select rising count compare match, falling count compare match, or both.

For compare A match, when the count value equals CCRxA, it is uniformly controlled by M23CR.CIS:

- M23CR.CIS=0b00: no output on compare match
- M23CR.CIS=0b01: compare match during up-counting
- M23CR.CIS=0b10: compare match during down-counting
- M23CR.CIS=0b11: compare match during both up-counting and down-counting

For compare B match, when the count value equals CCRxB, each channel can be individually controlled by CRCHx.CISB:

- When CRCHx.CISB=0b00, channel x has no output on compare match.
- When CRCHx.CISB=0b01, channel x compare match during up-counting.
- When CRCHx.CISB=0b10, channel x compare match during down-counting.
- When CRCHx.CISB=0b11, channel x compare match during both up-counting and down-counting.

The independent control of channel B compare match enables more flexible ADC triggering. For more details, refer to the Timer Trigger ADC section in the documentation.

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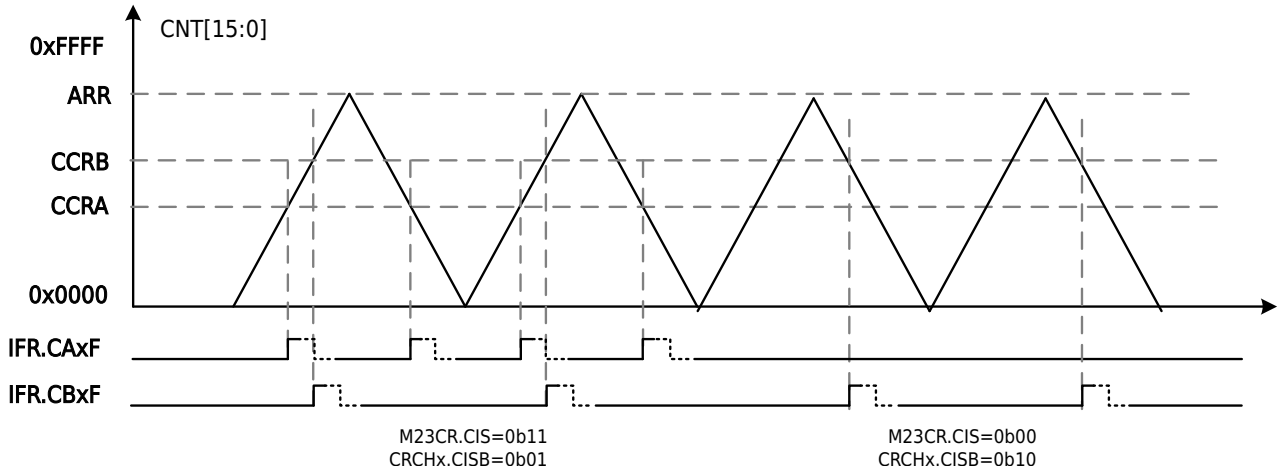

Figure 14-48 Compare Interrupt Diagram

14.3.6.11 Capture Input

The capture function (M23CR.MODE=2/3) can be configured in both triangular wave counting mode and sawtooth wave counting mode. The capture level edge can be set, and when a capture occurs, the captured value is stored in the compare capture register and generates a capture interrupt.

The compare capture function for each channel can be individually configured and selected through the CRCHx.CSA/CSB register. The capture edge for each channel can be independently set and via the CRCHx.CFy/CRy (x=0/1/2; y=A/B) register to select the triggering edge.

When the capture action occurs again before the capture flag is cleared after the capture occurs, the capture data overwrite flag will be generated. When the timer is not started, if there is a valid capture edge, the capture flag and capture action will also be generated.

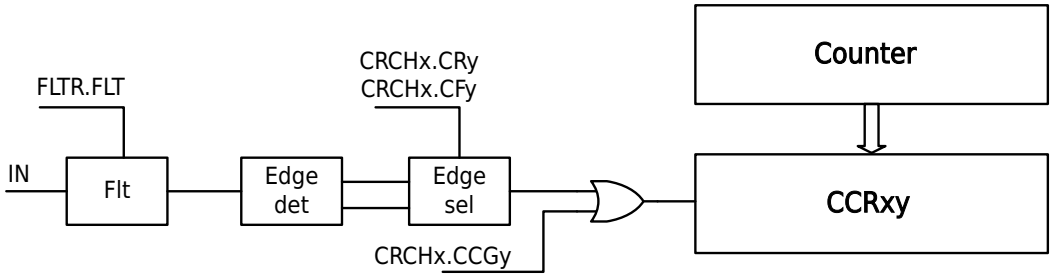

Figure 14-49 Capture Function Block Diagram

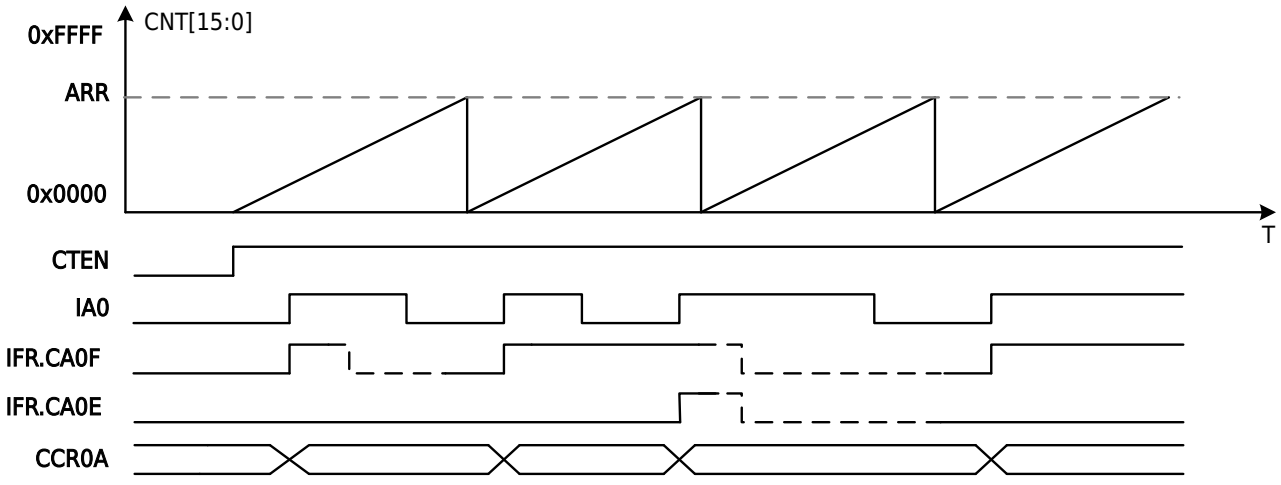

Figure 14-50 Capture Timing Diagram

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CH0A Capture Input

The capture input signal for CH0A is as shown in the table below.

Table 14-8 CH0A Capture Input Signal

MSCR.IA0S	TIM0/1/2	TIM3
0b0	CH0A	CH0A
0b1	CH0A ETR GATE XOR Input	CH0A CH1A CH2A XOR Input

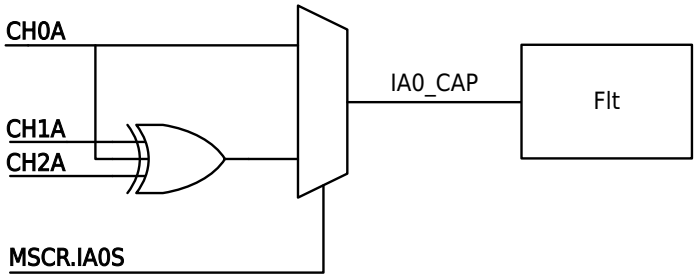

Figure 14-51 TIM3 CH0A Capture Input Port Selection

CH0B Capture Input

The capture input signal for CH0B is as shown in the table below.

MSCR.IB0S	TIM0/1/2/3
0b0	CH0B
0b1	Internal trigger MSCR.TS select signal

MSCR.TS Value	Channel B Capture Input
0b000	ETR filtered phase selection output signal, filter phase selection configurable
0b001	Internal interconnection ITR0
0b010	Internal interconnection ITR1
0b011	Internal interconnection ITR2
0b100	Internal interconnection ITR3
0b101	CH0A edge
0b110	CH0A filtered output signal, filter function configurable
0b111	Reserved

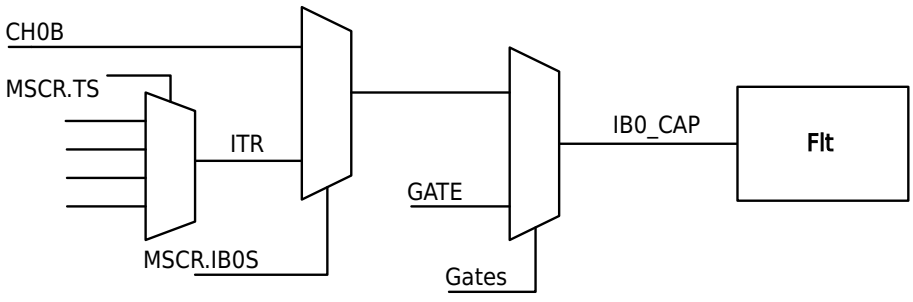

Figure 14-52 CH0B Capture Input Port Selection

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The Gates signal is generated for selecting the PWM complementary output function. When PWM is the single point comparison complementary output, the compare capture register CCR0B is unused, and automatically switches to using GATE as the capture compare output.

Notice

When GATE is configured for compare output, its output mode only supports being set to force the output to 0 or 1 and being set to PWM mode valid (that is, OCMB0 is configured as 0/1/6/7).

14.3.7 Mode2/3 Slave Mode

The timer can be synchronized to an external trigger in several modes: reset mode, gated mode and triggered mode.

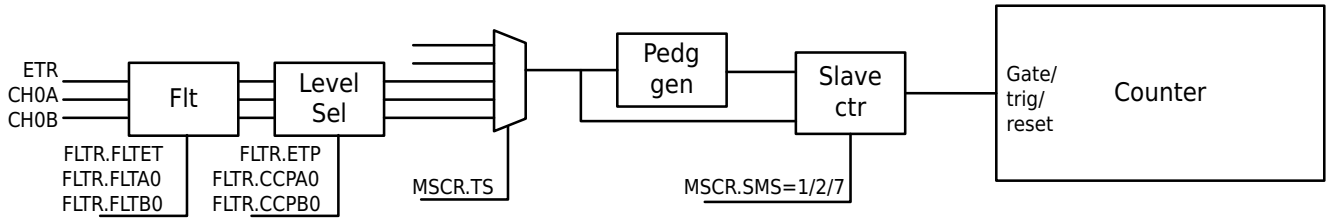

Figure 14-53 Mode2/3 Slave Mode Diagram

The slave mode function is selected via MSCR.SMS:

	Value	Description
MSCR.SMS	0b001	Slave mode function selection: reset mode
	0b010	Slave mode function selection: trigger mode
	0b111	Slave mode function selection: gating mode
MSCR.TS	0b000	The filtered phase selected signal ETFP from port ETR features configurable filtering function
	0b001	Internal interconnect signal ITR0
	0b010	Internal interconnect signal ITR1
	0b011	Internal interconnect signal ITR2
	0b100	Internal interconnect signal ITR3
	0b101	Port CH0A edge signal
	0b110	The filtered phase selected signal IAFP from port CH0A features configurable filtering function
	0b111	The filtered phase selected signal IBFP from port CH0B features configurable filtering function

Gated Counting

Enable the counter according to the selected input level. In the following example, the counter only counts up when CH0A is low:

- Configure channel CH0A to detect a low level on CH0A. Configure the input filter bandwidth (filtering is not required in this case, therefore maintain FLTR.FLTA0=0b000). Set FLTR.CCPA0=1 to determine the polarity (only detect low level).

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- Set MSCR.SMS=0b111 to configure the timer in gating mode; set MSCR.TS=0b110 to select CH0A as the input source.
- Set the M23CR.CTEN=1 to start the counter. In gating mode, if CTEN=0, the counter cannot be started regardless of the trigger input level. As long as CH0A is low, the counter starts counting according to the internal clock, and stops counting once CH0A becomes high.

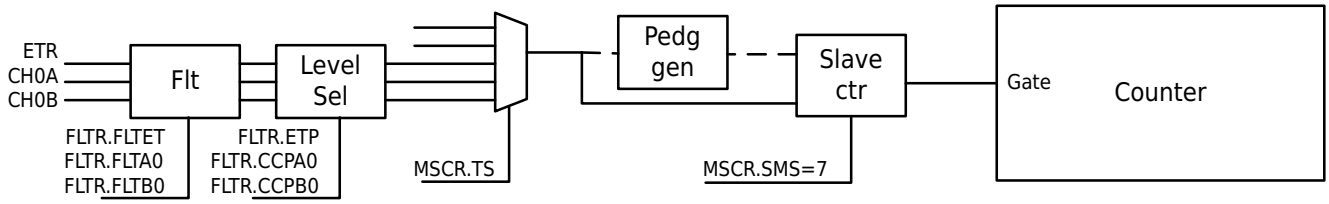

Figure 14-54 Mode2/3 Slave Mode Gating Function

Trigger Function

Using external triggers (CH0A, CH0B, ETR) enables synchronous timer startup. Alternatively, timer synchronization can be configured using the timer internal interconnect signals combined with MSCR.MSM. For related operations, refer to the examples of simultaneous PWM output setup for timers TIM0/1/2 (using TIM0's CTEN to trigger TIM1/2) and simultaneous PWM output setup for timers TIM0/1/2 (using TIM1's UG to trigger TIM0/2). The trigger signal is the rising edge of the input signal. Alternatively, software trigger function can be initiated by writing to M23CR.TG.

A selected event on the input enables the counter. In the example below, the counter starts up counting on the rising edge of the CH0B input:

- Configure channel CH0B to detect the rising edge of CH0B. Configure the input filter bandwidth (in this example, no filter is required, keep FLTR.FLTB0=0b000). Set FLTR.CCPB0=0 to determine polarity (no inversion).
- Set MSCR.SMS=0b010 to configure the timer in trigger mode; set MSCR.TS=0b111 to select CH0B as the input source. When a rising edge appears on CH0B, the counter starts counting driven by the internal clock and sets the TIF flag at the same time. The delay between the rising edge of CH0B and the start of the counter depends on the synchronization circuit at the CH0B input.

Note

When using falling edge trigger, first select the trigger polarity and then choose the mode; otherwise, false triggering may occur.

Reset Counting

When a trigger input event occurs, both the counter and its prescaler can be reinitialized; Simultaneously, if the M23CR.URS is low, an update event UEV is generated; Subsequently, all preload registers (ARR, CCRxy) are updated.

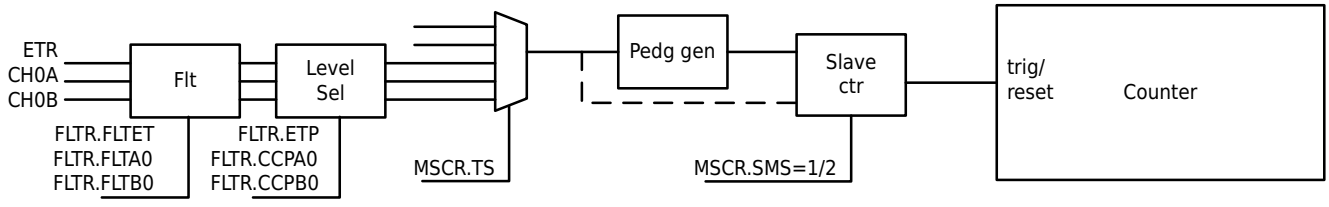

Figure 14-55 Mode2/3 Slave Mode Trigger and Reset Function

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14.3.8 Quadrature Encoder Counting Function

MSCR.SMS=4/5/6, corresponding to the mode 1/2/3 of quadrature encoder mode. At this point, the counter performs encoder counting based on the phase relationship between IAFP and IBFP. IAFP and IBFP are the filtered phase selection signals for port inputs CH0A and CH0B.

Mode 1 uses the edge count of CH0A. Mode 2 uses the edge count of CH0B. Mode 3 uses both the edges count of CH0A and CH0B.

In order to ensure the correctness of the counting phase, it is necessary to ensure that the phase of the A/B input is greater than the phase difference of one pulse width, and the A/B input pulse width needs to be greater than two pulse widths.

As shown in the table below, the edge condition of IAFP corresponds to the level signal of IBFP, while the edge condition of IBFP corresponds to the level signal of IAFP. For example, in MOD1, when IBFP is at a high level and a rising edge is detected on IAFP, the counter counts down; when IBFP is at a high level and a falling edge is detected on IAFP, the counter counts up.

Mode	Quadrature Signal Level Condition		Quadrature Signal IAFP Edge Condition		Quadrature Cignal IBFP Edge Condition	
	IBFP	IAFP	Rising Edge	Falling Edge	Rising Edge	Falling Edge
MOD1	High level	-	Down-counting	Up-counting	-	-
	Low level	-	Up-counting	Down-counting	-	-
MOD2	-	High level	-	-	Up-counting	Down-counting
	-	Low level	-	-	Down-counting	Up-counting
MOD3	High level	-	Down-counting	Up-counting	-	-
	Low level	-	Up-counting	Down-counting	-	-
	-	High level	-	-	Up-counting	Down-counting
	-	Low level	-	-	Down-counting	Up-counting

CHAF/CHBF is the signal filtered by port CH0A/CH0B, and IAFP/IBFP is the signal after port filter phase selection.

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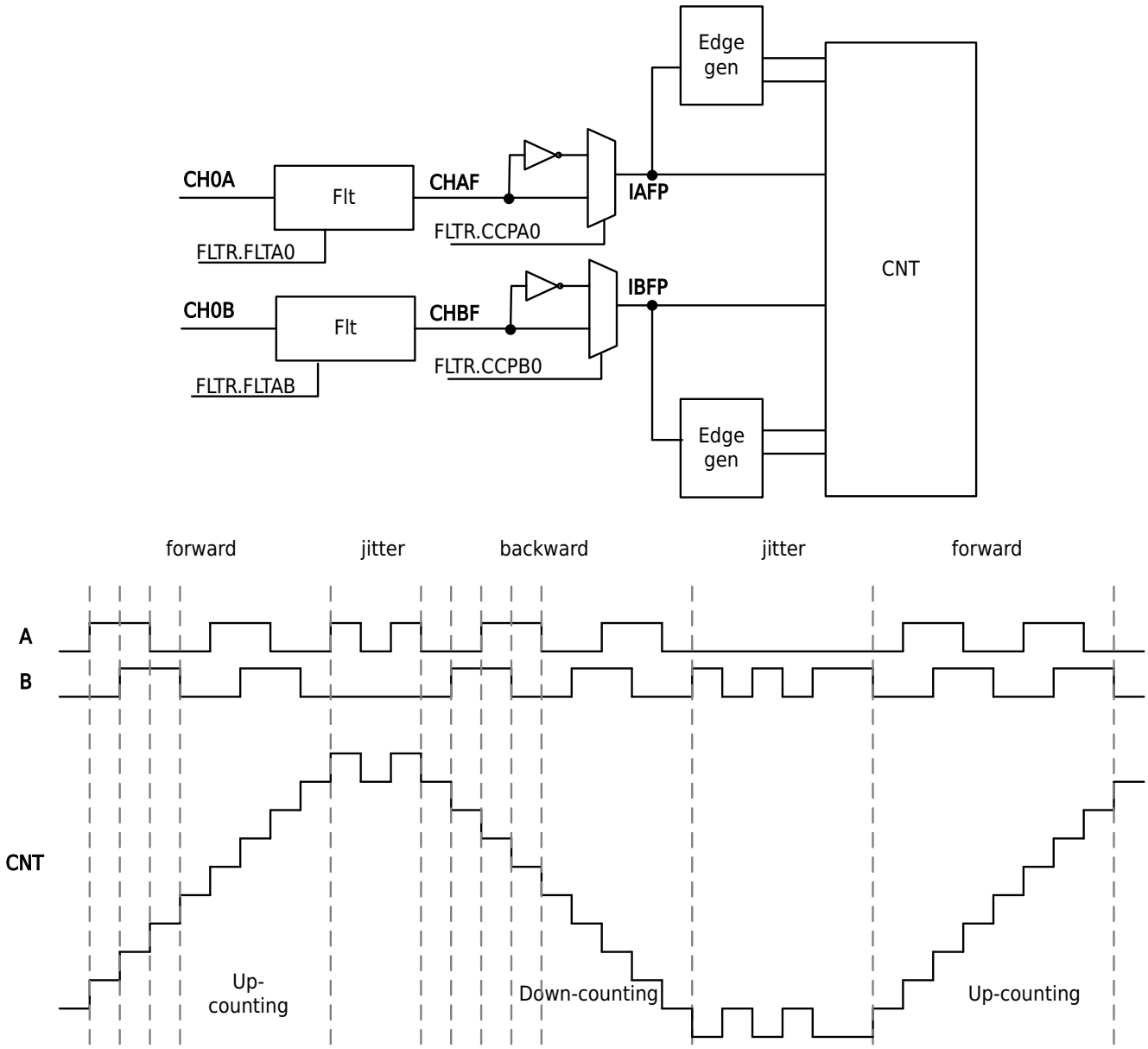

Figure 14-57 Quadrature Encoder Counting Mode3 Counting Diagram

14.3.9 Timer Triggers ADC

UEV Triggers ADC

When a update event (UEV) is generated and both ADTR.UEVE and ADTR.ADTE are enabled, a trigger request can be output to the ADC.

Compare Match Triggers ADC

CCR0A, CCR1A, and CCR2A compare matches can be configured to trigger the ADC.

- Mode3: The comparison match conditions for CHxA channels are uniformly controlled through the M23CR.CIS control register. You can select to trigger up-counting comparison match, down-counting comparison match, or both up-counting and down-counting comparison matches.
- Mode2: No need to configure M23CR.CIS.

CCR0B, CCR1B, and CCR2B compare matches can be configured to trigger the ADC.

- Mode 3: The comparison match conditions for CHxB channels are individually controlled via the CRCHx.CISB register. Options include triggering up-counting comparison match, down-counting comparison match, or both up-counting and down-counting comparison matches.

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- Mode2: No configuration of CRCHx.CISB is required.

The comparison matches of CCR3A and CCR3B can also be configured to trigger the ADC (If using channel 3A or channel 3B to trigger the ADC, no separate channel trigger enable needs to be set in the ADTR register; only enabling ADTR.ADTE is required).

- Mode3: The comparison match conditions for channel 3A and channel 3B are individually controlled by CRCH3A.CIS and CRCH3B.CIS registers respectively. Options include triggering on up-counting comparison match, down-counting comparison match, or both up-counting and down-counting comparison matches.
- Mode2: No configuration of CRCH3A.CIS and CRCH3B.CIS is required.

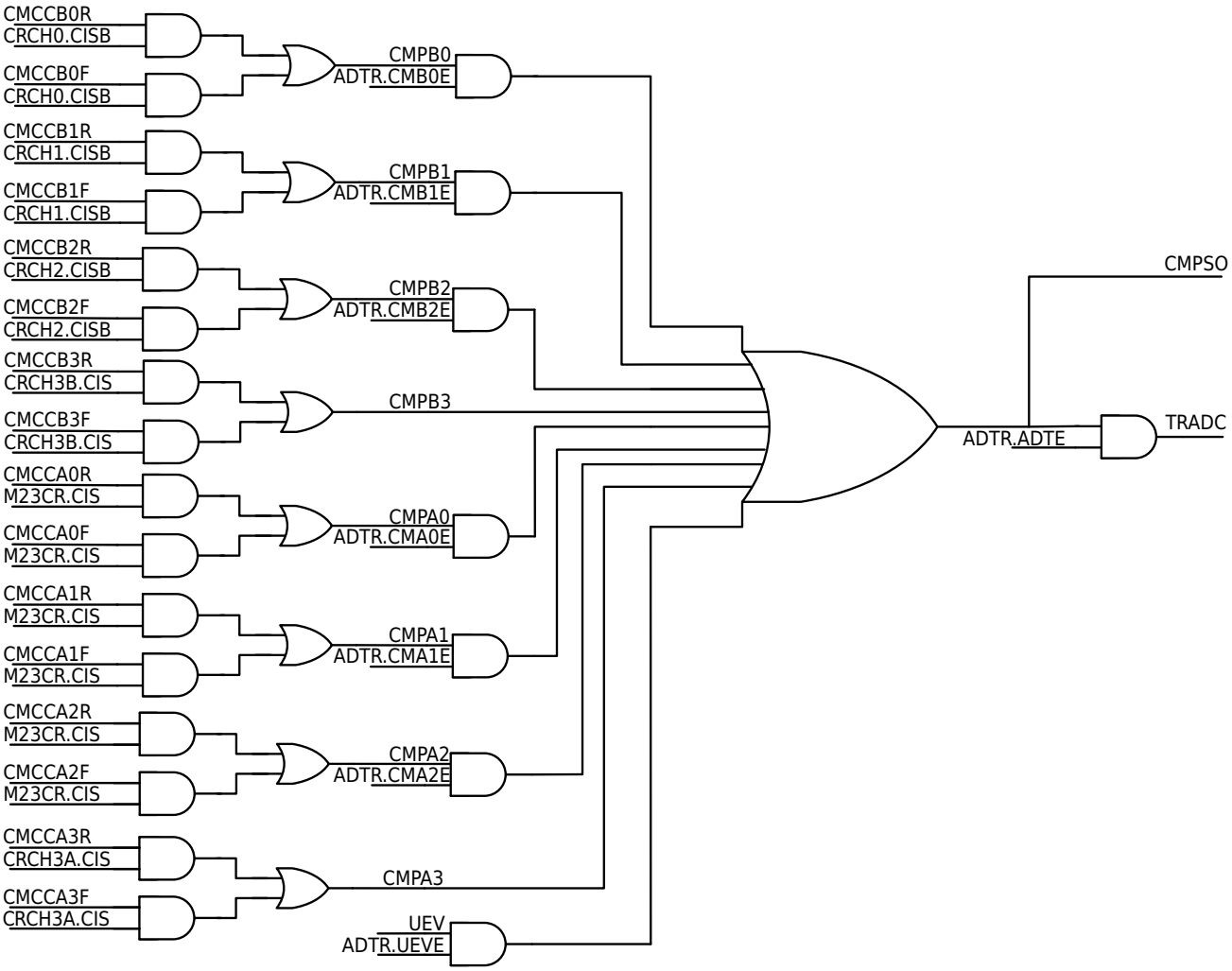

Figure 14-58 Timer Triggers ADC

14.3.10 Cycle-By-Cycle Current Limiting and Brake Control

Cycle-By-Cycle Current Limiting

M23CR.OCCE can select to enable or disable the cycle-by-cycle current limiting function. M23CR.OCCS can select the OCREF_CLR signal from either the VC output signal REFCLR or the filtered phase-selected signal ETFP from the ETR port.

The OUT_CFG.TIMxRCLR (x=0/1/2/3) of VC0/1/2 configure whether to enable the REFCLR signal to TIM0/1/2/3. OUT_CFG.INV_TIMER determines whether the REFCLR signal is active-high level (OUT_CFG.INV_TIMER=0) or active-low level (OUT_CFG.INV_TIMER=1). FLTR.ETP configures whether the

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ETR port input level is active-high level (FLTR.ETP=0) or active-low level(FLTR.ETP=1), while FLTR.FLTET sets the filtering time for ETR.

When DTR.AOE=0 and DTR.MOE=1, after enabling M23CR.OCCE, a valid OCREF_CLR signal can clear the current OCREFxy (x=0/1/2, y=A/B) signal (this clearing action is effective when FLTR.OCMyx>1 (x=0/1/2, y=A/B), while DTR.MOE will not be cleared. When the OCREF_CLR signal becomes invalid, the PWM output resumes after the next event update UEV.

Brake Control

Brake control can be implemented through the following methods:

1. VC comparator control: The OUT_CFG.INV_TIMER register of VC0/1/2 determines whether the VC output brake level signal is active-high level (OUT_CFG.INV_TIMER=0) or active-low level (OUT_CFG.INV_TIMER=1). EnableOUT_CFG.TIMBK, and enable DTR.VCE, when the VC output reaches the valid level, a valid brake condition is generated to control the braking function.
2. For external port control: Configure the designated port as the TIMx_BK (x=0/1/2/3) alternate function, set the brake active level (FLTR.BKP=0 for high level braking, FLTR.BKP=1 for low braking) in FLTR.BKP, configure the input filter time in FLTR.FLTBK, and enable DTR.BKE port braking. When a valid level is input from this port, the braking condition becomes active, enabling control of the braking function.
3. System Safety braking (DeepSleep/Reset) control.
4. M23CR.BG software brake control.

When DTR.AOE=0 and DTR.MOE=1, after the braking condition takes effect, the DTR.MOE bit will be cleared to 0, and the PWM pins will perform the specified actions according to the preset configuration of CRCHx.BKSA/CRCHx.BKSB (x=0/1/2). To restore PWM output, the DTR.MOE bit must be set again after the braking condition is deactivated.

When DTR.AOE=1 and DTR.MOE=1, after the braking condition takes effect, the DTR.MOE bit will be cleared to 0, and the PWM pins will perform the specified actions according to the preset configuration of CRCHx.BKSA/CRCHx.BKSB. Once the braking condition is deactivated, DTR.MOE will be automatically set, and PWM output will resume.

The TIM0/1/2 outputs of the two channels can either use TIM0 brake port to control the braking function of TIM1/2 or use their respective brake inputs to control their own braking functions. When DTR.BKSEL is set to 1, TIM1/2 share the brake input of TIM0.

14.3.11 Interrupt

Table 14-13 TIM0/1/2/3 Interrupt List

Interrupt Control Register	Interrupt Name
MxCR.UIE (x=0/1/23)	Overflow interrupt/event update interrupt
CRCHx.CIEA (x=0/1/2)	Channel (0/1/2) A compare capture interrupt
CRCHx.CIEB (x=0/1/2)	Channel (0/1/2) B compare capture interrupt
CRCH3y.CIE (y=A/B)	Channel 3A/B compare interrupt
M23CR.BIE	Brake interrupt
M23CR.TIE	Trigger interrupt
M23CR.OVE	Overflow interrupt

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Interrupt Control Register	Interrupt Name
M23CR.UNDE	Underflow interrupt

14.3.12 Timer Interconnection

The TRGO output signal can be connected to the ITR signal of other timers. The connection relationship is as follows:

Table 14-14 Timer Interconnection Signal List

	ITR0	ITR1	ITR2	ITR3
Timer0	-	TIM1_TRGO	TIM2_TRGO	TIM3_TRGO
Timer1	TIM0_TRGO	-	TIM2_TRGO	TIM3_TRGO
Timer2	TIM0_TRGO	TIM1_TRGO	-	TIM3_TRGO
Timer3	TIM0_TRGO	TIM1_TRGO	TIM2_TRGO	-

14.3.13 Input Interconnection

14.3.13.1 GATE Input Interconnection

When GPIO_TIMGS.TIMx_G=0b000, the gating GATE input is the port input selected by Pxy_SEL; when GPIO_TIMGS.TIMx_G=0b001-0b111, it connects to the input or output of other modules. Details see the "Port Auxiliary Function Timer Gate Selection (GPIO_TIMGS)" description in the "General-Purpose I/O (GPIO)" chapter.

14.3.13.2 ETR Input Interconnection

When GPIO_TIMES.TIMx_E=0b000, the ETR input is the port input selected by Pxy_SEL; when GPIO_TIMES.TIMx_E=0b001-0b111, it connects to the input or output of other modules. For detailed information, refer to the description of the register "Port Auxiliary Function Timer ETR Selection (GPIO_TIMES)" in the "General-Purpose I/O (GPIO)" chapter.

14.3.13.3 CHx Capture Input Interconnection

When GPIO_TIMCPS.TIMx_Cy=0b000, the capture input (Timer0/1/2 CHA, Timer3 CH0A/CH0B) is the port input selected by Pxy_SEL. When GPIO_TIMCPS.TIMx_Cy=0b001-0b111, it connects to the input or output of other modules. For detailed information, refer to the description of the register "Port Auxiliary Function Timer Capture Input Selection (GPIO_TIMCPS)" in the "General-Purpose I/O (GPIO)" chapter.

14.3.14 DMA

Timer supports software and hardware to trigger DMA for data transfer. Data is supported to be written to the timer from other locations, or read and written from the timer to other locations. It can be applied to the automatic handling of data after data capture and the automatic adjustment of the pulse width changing the period value or duty cycle. Each timer has two DMA requests: request A trigger source can select between compare capture A or external trigger ETR; request B trigger source can select between compare capture B or update event UEV.

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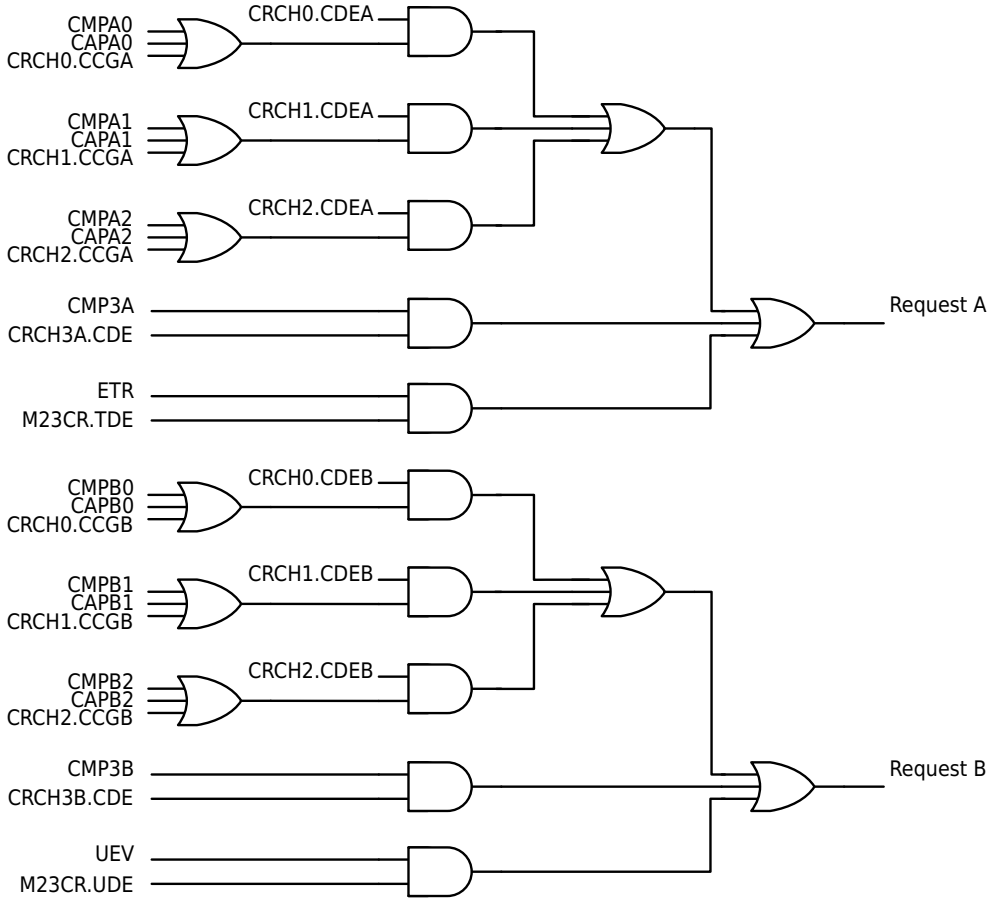

Figure 14-59 DMA Request Trigger Sources

14.4 Operation Example

14.4.1 Mode0 Counting Timer Function Configuration Example

Procedure

- **Reload Timer Setting**
  - **Step1.** Configure timer mode M0CR.MODE=0;
  - **Step2.** Set load value ARR;
  - **Step3.** Set counter initial value CNT;
  - **Step4.** Clear interrupt flag;
  - **Step5.** Enable interrupt M0CR.UIE;
  - **Step6.** Enable reload mode M0CR.MD;
  - **Step7.** Start timer M0CR.CTEN.
- **Gating External Clock Free Counting Setting**
  - **Step1.** Configure timer mode M0CR.MODE=0;
  - **Step2.** Set counter initial value CNT;
  - **Step3.** Enable gating function M0CR.GATE;
  - **Step4.** Select gating active level M0CR.GATEP;
  - **Step5.** Clear interrupt flag;
  - **Step6.** Enable interrupt M0CR.UIE;
  - **Step7.** Enable external clock mode M0CR.CT;
  - **Step8.** Start timer M0CR.CTEN.

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- **BUZZER Output Control**
  - **Step1.** Set appropriate ARR value based on output frequency;
  - **Step2.** Configure timer as reload mode, refer to Reload Timer Settings;
  - **Step3.** Enable output enable DTR.MOE;
  - **Step4.** Start another timer to control M0CR.TOGEN for implementing interval frequency output.

14.4.2 Mode1 Pulse Width Measurement PWC Configuration Example

Procedure

- **Pulse Low Level Measurement Setting**
  - **Step1.** Configure pulse measurement mode M1CR.MODE=1;
  - **Step2.** Set MSCR.TS to select measurement signal, then configure MSCR.IA0S/IB0S (IB0S cannot be set to 1) based on MSCR.TS setting to select measurement channel;
  - **Step3.** Set M1CR.EDG2ND=0 and M1CR.EDG1ST=1 to measure low level;
  - **Step4.** Clear interrupt flag;
  - **Step5.** Enable overflow interrupt M1CR.UIE;
  - **Step6.** Enable measurement completion interrupt CR0.CIEA;
  - **Step7.** Enable timer M1CR.CTEN;
  - **Step8.** In interrupt service routine, read CCR0A and overflow count then clear interrupt flag;
  - **Step9.** Wait for next measurement.
- **Pulse High Level Single Measurement Setting**
  - **Step1.** Configure pulse measurement mode M1CR.MODE=1;
  - **Step2.** Set MSCR.TS to select measurement signal, then configure MSCR.IA0S/IB0S (IB0S cannot be set to 1) based on MSCR.TS setting to select measurement channel;
  - **Step3.** Set pulse single-shot measurement mode M1CR.ONESHOT=1;
  - **Step4.** Configure M1CR.EDG2ND=1 and M1CR.EDG1ST=0 to measure high level;
  - **Step5.** Clear interrupt flag;
  - **Step6.** Enable overflow interrupt M1CR.UIE;
  - **Step7.** Enable measurement completion interrupt CR0.CIEA;
  - **Step8.** Enable timer M1CR.CTEN;
  - **Step9.** In interrupt service routine, read CCR0A and overflow count then clear interrupt flag;
  - **Step10.** Measurement is completed.

14.4.3 Mode2/3 Compare Capture Mode Configuration Example

Procedure

- **Edge-aligned Independent PWM Output Setting**
  - **Step1.** Set mode M23CR.MODE=2;
  - **Step2.** Configure sawtooth wave counting direction M23CR.DIR;
  - **Step3.** Set PWM period value ARR;
  - **Step4.** Set counter initial value (must be smaller than period value);
  - **Step5.** Configure PWM compare value CCRxA/CCRxB;
  - **Step6.** Set PWM output compare modes FLTR.OCMAx and FLTR.OCMBx to 6 or 7;
  - **Step7.** Clear relevant interrupt flags;
  - **Step8.** Enable corresponding interrupts;
  - **Step9.** Configure output polarities FLTR.CCPAx and FLTR.CCPBx;

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Step10. Enable output DTR.MOE;

Step11. Enable timer M23CR.CTEN.

- **Center-Aligned Complementary PWM Output Setting**

  Step1. Set mode M23CR.MODE=3;

  Step2. Configure complementary output M23CR.COMP;

  Step3. Set PWM period value ARR;

  Step4. Set counter initial value (must be smaller than period value);

  Step5. Set PWM compare value CCRxA (CCRxB does not need to be set as PWM output is independent of this register);

  Step6. Set PWM output compare modes FLTR.OCMAx and FLTR.OCMBx to 6 or 7;

  Step7. Clear relevant interrupt flags;

  Step8. Enable corresponding interrupts;

  Step9. Configure output polarities FLTR.CCPAx and FLTR.CCPBx;

  Step10. Enable output DTR.MOE;

  Step11. Enable timer M23CR.CTEN.

- **Asymmetric Center-Aligned Complementary PWM Output with Dead-Time Setting**

  Step1. Set mode M23CR.MODE=3;

  Step2. Configure complementary output M23CR.COMP;

  Step3. Enable dual-point comparison enable M23CR.PWM2S;

  Step4. Set PWM period value ARR;

  Step5. Set counter initial value (must be smaller than period value);

  Step6. Set PWM compare values CCRxA and CCRxB (up-counting comparison point is CCRxA, down-counting comparison point is CCRxB);

  Step7. Set PWM output compare modes FLTR.OCMAx and FLTR.OCMBx to 6 or 7;

  Step8. Clear relevant interrupt flags;

  Step9. Enable corresponding interrupts;

  Step10. Configure output polarities FLTR.CCPAx and FLTR.CCPBx;

  Step11. Set dead time enbale DTR.DTEN;

  Step12. Set dead time duration DTR.DTR;

  Step13. Enable output DTR.MOE;

  Step14. Enable timer M23CR.CTEN.

- **Capture Function Configuration**, setting CH0B for rising edge capture function

  Step1. Select counter counting mode, set M23CR.MODE=2;

  Step2. Configure CH0B as capture mode CRCH0.CSB=1;

  Step3. Select input filter FLTR.FLTB0 as needed;

  Step4. Select capture edge CRCH0.CRB=1;

  Step5. Set ARR to change the period value;

  Step6. Clear relevant interrupt flags;

  Step7. Clear the capture flag and enable the corresponding interrupt;

  Step8. Start timer M23CR.CTEN;

  Step9. After detecting the capture flag, read CCR0B to obtain the captured value.

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> **Note**
> When the timer is not started, if there is a valid capture edge, the capture flag and capture action will also be generated.

- **Complementary PWM Output Uses GATE as PWM Output Function**
  - **Step1.** Configure as PWM complementary output mode, with steps referenced to Center-aligned Complementary PWM Output Setup;
  - **Step2.** Set CCR0B to configure the GATE PWM comparison value;
  - **Step3.** Set FLTR.OCMB0=6/7 to configure the PWM output mode;
  - **Step4.** Enable PWM output DTR.MOE;
  - **Step5.** Start the timer M23CR.CTEN.
- **Complementary PWM Output Uses GATE Falling Edge as Capture Input Function**
  - **Step1.** Configure as PWM complementary output mode, with steps referenced to Center-aligned Complementary PWM Output Setup;
  - **Step2.** Set GATE as capture input M23CR.CSG;
  - **Step3.** Select GATE capture input edge configuration M23CR.CFG (GATE as capture input B channel filter setting is invalid);
  - **Step4.** Clear relevant interrupt flags;
  - **Step5.** Clear the capture flag and enable the corresponding interrupt;
  - **Step6.** Start timer M23CR.CTEN;
  - **Step7.** After detecting the capture flag, read CCR0B to obtain the captured value.

14.4.4 Complementary PWM Output B Compare as ADC Trigger Function

Procedure

- **Step1.** Configure as PWM complementary output mode, with setup steps referring to Center-Aligned Complementary PWM Output Setting
- **Step2.** Set CCRxB to set ADC trigger comparison point
- **Step3.** Set CRCHx.CISB to select up-counting and down-counting comparison matching (sawtooth wave does not need to be selected)
- **Step4.** Select the source ADTR for ADC trigger comparison
- **Step5.** Enable ADC triggers ADTR.ADTE

14.4.5 Simultaneous PWM Output Startup for Timer TIM0/1/2 Configuration (Using TIM0 CTEN to Trigger TIM1/2) Example

Procedure

- **Step1.** Refer to the PWM output setting to set the pulse adjustment output of timer 0/1/2
- **Step2.** Configure TIM0 as master mode MSCR.MSM=1
- **Step3.** Set TIM0 CTEN to trigger the other two timers MSCR.MMS=1
- **Step4.** Keep MSCR.MSM=0 of TIM1/2
- **Step5.** Set TIM1/2 as trigger mode MSCR.SMS=2
- **Step6.** Select TIM0 TRGO as trigger source for TIM1/2, MSCR.TS=1
- **Step7.** Enable timer TIM0, startup the timer M23CR.CTEN=1

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14.4.6 Simultaneous PWM Output Startup for Timer TIM0/1/2 Configuration (Using TIM1 UG to Trigger TIM0/2) Example

Procedure

Step1. Refer to the PWM output setting to set the pulse adjustment output of timer 0/1/2

Step2. Set TIM1 as trigger master mode (MSCR.MSM=1)

Step3. Set TIM1 UG to trigger the other two timers MSCR.MMS=0

Step4. Keep MSCR.MSM=0 of TIM0/2

Step5. Set TIM0/2 as trigger mode MSCR.SMS=2

Step6. Select TIM0 TRGO as trigger source for TIM0/2, MSCR.TS=2

Step7. Enable timer TIM1, startup the timer M23CR.UG=1

14.4.7 DMA Configuration Example

Procedure

- **Capture Data DMA Data Transmission**

  Step1. Enable DMA

  Step2. Enable DMA channel enable

  Step3. Select the channel for timer DMA

  Step4. Set the transmission type, transmission length, transmission method

  Step5. Set source start address, destination start address

  Step6. Set the increment method of source address and destination address

  Step7. Enable DMA interrupts as needed

  Step8. Set up data capture with reference to the data capture process

  Step9. Enable CRCHx.CDEy to enable capture data triggering DMA transfer.

  Note

  Set the source address to the channel compare capture register, with the source address fixed and the destination address variable.

- **Pulse Adjusted DMA Data Transmission**

  Step1. Enable DMA

  Step2. Enable DMA channel enable

  Step3. Select the channel for timer DMA

  Step4. Set the transmission type, transmission length, transmission method

  Step5. Set source start address, destination start address

  Step6. Set the increment method of source address and destination address

  Step7. Enable DMA interrupts as needed

  Step8. Reference pulse adjustment output setting pulse modulation output

  Step9. Select the condition of hardware triggering DMA according to needs (UEV trigger or comparison match trigger)

  Note

  Set the destination address to the channel compare capture register, with the source address variable and the destination address fixed.

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14.5 Register Description

14.5.1 Register List

- Timer0 base address: 0x40000C00
- Timer1 base address: 0x40000D00
- Timer2 base address: 0x40000E00
- Timer3 base address: 0x40005800

Table 14-15 Mode0 Timer Register Offset

Offset	Register	Description	Width
0x000	TIM_ARR	16-Bit Mode Reload Register/Period	32
0x004	TIM_CNT	16-Bit Mode Count Register	32
0x008	TIM_CNT32	32-Bit Mode Count Register **Note** TIM_CNT32 is the remapping register for TIM_ARR and TIM_CNT. In order to facilitate the 32-bit timer write operation.	32
0x00C	TIM_M0CR	Mode0 Control Register	32
0x010	TIM_IFR	Interrupt Flag Register	32
0x014	TIM_ICLR	Interrupt Flag Clear Register	32
0x030	TIM_DTR	Dead Time Register	32

Table 14-16 Mode1 Pulse Width Measurement (PWM) Register Offset

Offset	Register	Description	Width
0x004	TIM_CNT	16-Bit Mode Count Register	32
0x00C	TIM_M1CR	Mode1 Control Register	32
0x010	TIM_IFR	Interrupt Flag Register	32
0x014	TIM_ICLR	Interrupt Flag Clear Register	32
0x018	TIM_MSCR	Master-Slave Mode Control Register	32
0x01C	TIM_FLTR	Input Filter Register	32
0x024	TIM_CR0	Control Register	32
0x03C	TIM_CCR0A	Compare Capture Register	32

Table 14-17 Mode2/3 Compare-Capture Mode Register Offset

Offset	Register	Description	Width
0x000	TIM_ARR	16-Bit Mode Reload Register/Period	32

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Offset	Register	Description	Width
0x004	TIM_CNT	16-Bit Mode Count Register	32
0x00C	TIM_M23CR	Mode2/3 Control Register	32
0x010	TIM_IFR	Interrupt Flag Register	32
0x014	TIM_ICLR	Interrupt Flag Clear Register	32
0x018	TIM_MSCR	Master-Slave Mode Control Register	32
0x01C	TIM_FLTR	Output Control/Input Filter Register	32
0x020	TIM_ADTR	ADC Trigger Control Register	32
0x024	TIM_CRCH0	Channel 0 Control Register	32
0x028	TIM_CRCH1	Channel 1 Control Register (only TIM3 exists)	32
0x02C	TIM_CRCH2	Channel 2 Control Register (only TIM3 exists)	32
0x030	TIM_DTR	Dead Time Register	32
0x034	TIM_RCR	Repeat Cycle Setting Value Register	32
0x038	TIM_ARRDM	Reload Register/Period Mapped Address	32
0x03C	TIM_CCR0A	Channel 0A Compare/Capture Register	32
0x040	TIM_CCR0B	Channel 0B Compare/Capture Register	32
0x044	TIM_CCR1A	Channel 1A Compare/Capture Register (only TIM3 exists)	32
0x048	TIM_CCR1B	Channel 1B Compare/Capture Register (only TIM3 exists)	32
0x04C	TIM_CCR2A	Channel 2A Compare/Capture Register (only TIM3 exists)	32
0x050	TIM_CCR2B	Channel 2B Compare/Capture Register (only TIM3 exists)	32
0x054	TIM_CCR3A	Channel 3A Compare Register (only TIM3 exists)	32
0x058	TIM_CRCH3A	Channel 3A Control Register (only TIM3 exists)	32
0x05C	TIM_CCR3B	Channel 3B Compare Register (only TIM3 exists)	32
0x060	TIM_CRCH3B	Channel 3B Control Register (only TIM3 exists)	32

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14.5.2 Mode0 Count Timer Register

14.5.2.1 16-Bit Mode Reload Register (TIM_ARR)

Offset	Bit Position																													
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																						ARR									
Access																							RW									

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	ARR	16-bit reload timer reload value register	RW

14.5.2.2 16-Bit Mode Count Register (TIM_CNT)

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																						CNT									
Access																							RW									

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	CNT	16-bit reload timer count value register	RW

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14.5.2.3 32-Bit Mode Count Register (TIM_CNT32)

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	CNT32																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	CNT32	32-bit timer count value register Valid only in Mode 0 32-bit timer free-counting mode, and writing to this register disables in other modes.	RW

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14.5.2.4 Mode0 Control Register (TIM_M0CR)

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00600008																															
Name	Reserved																		MODE		Reserved	UIE	GATEP	GATE	Reserved	PRS			TOGEN	CT	MD	CTEN
Access																			RW			RW	RW	RW		RW			RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:14	*Reserved*	-	-
13:12	MODE	Working mode ● 0b00: Timer mode 0 ● 0b01: PWC mode ● 0b10: Sawtooth wave mode ● 0b11: Triangle wave mode	RW
11	*Reserved*	-	-
10	UIE	Interrupt enable control ● 0b0: Disable ● 0b1: Enable	RW
9	GATEP	Port GATE polarity control ● 0b0: Port GATE high level is valid ● 0b1: Port GATE low level is valid	RW
8	GATE	Timer gating enable ● 0b0: No gating, timer works when CTEN=1 ● 0b1: Gating enabled, timer only operates when GATE port is valid and CTEN=1	RW
7	*Reserved*	-	-
6:4	PRS	Internal clock frequency division selection ● 0b000: 1 ● 0b001: 2 ● 0b010: 4 ● 0b011: 8 ● 0b100: 16 ● 0b101: 32 ● 0b110: 64 ● 0b111: 256	RW
3	TOGEN	Toggle output enable in mode 0 ● 0b0: Toggle output disabled, CHA and CHB outputs remain low level ● 0b1: Toggle output enabled	RW

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Bit	Name	Functional Description	Access
2	CT	Count clock selection ● 0b0: Internal count clock TCLK ● 0b1: External count clock ETR	RW
1	MD	Mode selection 32 timing/16 timing mode selection ● 0b0: 32-bit free counting ● 0b1: 16-bit reload counting	RW
0	CTEN	Timer enable ● 0b0: Disable ● 0b1: Enable	RW

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14.5.2.5 Interrupt Flag Register (TIM_IFR)

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																															UIF
Access																																RO

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-
0	UIF	Overflow interrupt ● 0b0: Counter is not overflowed ● 0b1: Counter overflowed	RO

14.5.2.6 Interrupt Flag Clear Register (TIM_ICLR)

Offset	Bit Position																													
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000FFFF																															
Name	Reserved																															UIF
Access																																WO

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-
0	UIF	Overflow interrupt clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO

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14.5.2.7 Dead Time Register (TIM_DTR)

Offset	Bit Position																													
0x030	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																			MOE	Reserved											
Access																				RW												

Bit	Name	Functional Description	Access
31:13	*Reserved*	-	-
12	MOE	Toggle output enable ● 0b0: Toggle output in input status ● 0b1: Toggle port in output status	RW
11:0	*Reserved*	-	-

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14.5.3 Mode1 Pulse Width Measurement PWC Register

14.5.3.1 16-Bit Mode Count Register (TIM_CNT)

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																CNT															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	CNT	Count value register	RW

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14.5.3.2 Mode1 Control Register (TIM_M1CR)

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00600008																															
Name	Reserved																	ONESHOT	MODE		Reserved	UIE	EDG2ND	EDG1ST	Reserved	PRS			Reserved	CT	Reserved	CTEN
Access																		RW	RW		RW	RW	RW	RW		RW			RW		RW	RW

Bit	Name	Functional Description	Access
31:15	*Reserved*	-	-
14	ONESHOT	Single trigger mode selection ● 0b0: Cycle measurement ● 0b1: Automatically terminates after completing one pulse measurement, re-enable CTEN is required for subsequent measurements	RW
13:12	MODE	Working mode ● 0b00: Timer mode 0 ● 0b01: PWC mode ● 0b10: Sawtooth wave mode ● 0b11: Triangle wave mode	RW
11	*Reserved*	-	-
10	UIE	Interrupt enable control Counting to 0xFFFF will overflow and generate an overflow flag ● 0b0: Disable ● 0b1: Enable	RW
9	EDG2ND	Pulse width measurement end edge selection Refer to the EDG1ST function description for details	RW
8	EDG1ST	Pulse width measurement start edge selection **EDG2ND / EDG1ST / Measurement** 0b0 / 0b0 / Up edge-up edge period 0b0 / 0b1 / Low level width 0b1 / 0b0 / High level width 0b1 / 0b1 / Falling edge-falling edge period	RW
7	*Reserved*	-	-

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Bit	Name	Functional Description	Access
6:4	PRS	Internal clock frequency division selection ● 0b000: 1 ● 0b001: 2 ● 0b010: 4 ● 0b011: 8 ● 0b100: 16 ● 0b101: 32 ● 0b110: 64 ● 0b111: 256	RW
3	*Reserved*	-	-
2	CT	Count clock selection ● 0b0: Internal count clock TCLK ● 0b1: External count clock ETR	RW
1	*Reserved*	-	-
0	CTEN	Pulse width measurement enable ● 0b0: Disable ● 0b1: Enable	RW

14.5.3.3 Interrupt Flag Register (TIM_IFR)

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																													CA0F	Reserved	UIF
Access																														RO		RO

Bit	Name	Functional Description	Access
31:3	*Reserved*	-	-
2	CA0F	Pulse width measurement interrupt flag ● 0b0: Pulse width measurement is not completed ● 0b1: Pulse width measurement completed	RO
1	*Reserved*	-	-
0	UIF	Overflow interrupt flag ● 0b0: Counter is not overflowed ● 0b1: Counter overflowed	RO

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14.5.3.4 Interrupt Flag Clear Register (TIM_ICLR)

Offset	Bit Position																													
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000FFFF																															
Name	Reserved																													CA0F	Reserved	UIF
Access																														WO		WO

Bit	Name	Functional Description	Access
31:3	*Reserved*	-	-
2	CA0F	Pulse width measurement interrupt flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
1	*Reserved*	-	-
0	UIF	Overflow interrupt clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO

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14.5.3.5 Master-Slave Mode Control Register (TIM_MSCR)

Offset	Bit Position																													
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																			IB0S	IA0S	Reserved			TS			Reserved				
Access																				RW	RW				RW							

Bit	Name	Functional Description	Access
31:13	*Reserved*	-	-
12	IB0S	CH0B input selection ● 0b0: CH0B ● 0b1: Internal trigger TS selection signal	RW
11	IA0S	IA0 input selection ● 0b0: CH0A ● 0b1: ▶ CH0A CH1A CH2A XOR (TIM3) ▶ CH0A ETR GATE XOR (TIM0/1/2) **Note** Setting to 1 will cause input changes upon any port transition.	RW
10:8	*Reserved*	-	-
7:5	TS	Trigger selection ● 0b000: Signal ETFP after port ETR filtered phase selection ● 0b001: Internal interconnect signal ITR0 ● 0b010: Internal interconnect signal ITR1 ● 0b011: Internal interconnect signal ITR2 ● 0b100: Internal interconnect signal ITR3 ● 0b101: Setting prohibited ● 0b110: Signal IAFP after port CH0A filtered phase selection ● 0b111: Signal IBFP after port CH0B filtered phase selection	RW
4:0	*Reserved*	-	-

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14.5.3.6 Input Filter Register (TIM_FLTR)

Offset	Bit Position																													
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	ETP	FLTET			Reserved																					FLTB0			Reserved	FLTA0		
Access	RW	RW																								RW				RW		

Bit	Name	Functional Description	Access
31	ETP	ETR input phase selection ● 0b0: Same phase ● 0b1: Reverse input	RW
30:28	FLTET	ETR filter control ● 0b000-0b011: Filter is invalid ● 0b100: PCLK, three consecutive valid samples ● 0b101: PCLK/4, three consecutive valid samples ● 0b110: PCLK/16, three consecutive valid samples ● 0b111: PCLK/64, three consecutive valid samples	RW
27:7	*Reserved*	-	-
6:4	FLTB0	CHB input filter control ● 0b000-0b011: Filter is invalid ● 0b100: PCLK, three consecutive valid samples ● 0b101: PCLK/4, three consecutive valid samples ● 0b110: PCLK/16, three consecutive valid samples ● 0b111: PCLK/64, three consecutive valid samples	RW
3	*Reserved*	-	-
2:0	FLTA0	CHA input filter control ● 0b000-0b011: Filter is invalid ● 0b100: PCLK, three consecutive valid samples ● 0b101: PCLK/4, three consecutive valid samples ● 0b110: PCLK/16, three consecutive valid samples ● 0b111: PCLK/64, three consecutive valid samples	RW

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14.5.3.7 Control Register (TIM_CR0)

Offset	Bit Position																															
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00003000																															
Name	Reserved																							CIEA	Reserved		CSB	CSA	Reserved			
Access																								RW			RW	RW				

Bit	Name	Functional Description	Access
31:9	*Reserved*	-	-
8	CIEA	Pulse width measurement complete interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
7:6	*Reserved*	-	-
5	CSB	B channel capture/compare function selection When pulse width measurement uses channel B filtering, CSB must be set to 1 ● 0b0: Compare mode ● 0b1: Capture mode	RW
4	CSA	A channel capture/compare function selection When pulse width measurement uses channel A filtering, CSA must be set to 1 ● 0b0: Compare mode ● 0b1: Capture mode	RW
3:0	*Reserved*	-	-

14.5.3.8 Compare Capture Register (TIM_CCR0A)

Offset	Bit Position																															
0x03C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																CCR0A															
Access																	RO															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	CCR0A	Pulse width measurement result	RO

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14.5.4 Mode2/3 Compare Capture Mode Register

14.5.4.1 16-Bit Mode Reload Register (TIM_ARR)

Offset	Bit Position																													
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																ARR															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	ARR	Reload register/period register With cache function, when the counter is not enabled or the cache is not enabled, the cache register can be updated immediately	RW

14.5.4.2 16-Bit Mode Count Register (TIM_CNT)

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																CNT															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	CNT	Reload timer count value register When using PWM compare output, triangular wave mode or saw-tooth wave mode up-counting, the initialized CNT value must be less than the ARR value.	RW

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14.5.4.3 Mode2/3 Control Register (TIM_M23CR)

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00600008																															
Name	Reserved		UNDE	OVE	DIR	BG	UG	TG	OCCE	CIS		BIE	TIE	TDE	URS	OCCS	CSG	ONESHOT	MODE		UDE	UIE	CFG	CRG	BUFPEN	PRS		PWM2S	CT	COMP	CTEN
Access			RW	RW	RW/RO	WO	WO	WO	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW		RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:30	*Reserved*	-	-
29	UNDE	Underflow interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
28	OVE	Overflow interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
27	DIR	Count direction Write only in sawtooth wave mode. Read only in other modes, write invalid ● 0b0: Up-counting ● 0b1: Down-counting **Note** DIR is automatically cleared when switching from other modes to center-aligned mode. In the center-aligned mode, DIR is automatically cleared in reset mode by software event update and external trigger in slave mode.	RW/RO
26	BG	Software brake Auto-clear. Write 1 to generate a software brake, write 0 has no effect.	WO
25	UG	Software update Auto-clear. Write 1 to generate a software update, write 0 has no effect. Initializes the counter and updates the buffer register to the corresponding registers (buffer enable), the PRS bit will also be cleared.	WO
24	TG	Software trigger Auto-clear. Write 1 to generate a software trigger, write 0 has no effect. Triggering is available in trigger mode SMS=2 and mode=2/3.	WO

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Bit	Name	Functional Description	Access
23	OCCE	OCREF clear enable ● 0b0: OCREF output unaffected by OCREF_CLR ● 0b1: OCREF_CLR signal can clear OCREF output	RW
22:21	CIS	Channel A compare match mode ● 0b00: No match ● 0b01: Compare match during up-counting ● 0b10: Compare match during down-counting ● 0b11: Compare match during both up/down counting **Note** Channel B compare match mode is controlled by the CISB bit in the CRCHx register.	RW
20	BIE	Brake interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
19	TIE	Trigger interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
18	TDE	Trigger start DMA enbale ● 0b0: Disable ● 0b1: Enable	RW
17	URS	Update source ● 0b0: Overflow/underflow/software update UG/slave mode reset ● 0b1: Overflow/underflow	RW
16	OCCS	OCREF_CLR signal source selection ● 0b0: Voltage comparator VC output, VC selection is configured in the VC_OUT_CFG register. ● 0b1: Signal after ETR port filtered phase selection When OCCE is enabled, OCREF_CLR can clear the OCREF compare output signal (valid when OCMyx>1), and the compare output resumes after the next UEV event.	RW
15	CSG	GATE capture/compare selection in PWM complementary mode Valid only during PWM complementary output, using CCR0B as the GATE compare or capture channel ● 0b0: Compare ● 0b1: Capture	RW
14	ONESHOT	Single trigger mode selection ● 0b0: Cycle count ● 0b1: Timer stops after an event update occurs	RW
13:12	MODE	Working mode ● 0b00: Timer mode 0 ● 0b01: PWC mode ● 0b10: Sawtooth wave mode ● 0b11: Triangle wave mode	RW

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Bit	Name	Functional Description	Access
11	UDE	Update trigger DMA enable ● 0b0: Disable ● 0b1: Enable	RW
10	UIE	Update interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
9	CFG	Falling edge capture valid control when GATE is used as capture input Only valid when PWM complementary output ● 0b0: Lower edge capture is invalid ● 0b1: Lower edge capture is valid	RW
8	CRG	Rising edge capture valid control when GATE is used as capture input Only valid when PWM complementary output ● 0b0: Upper edge capture is invalid ● 0b1: Upper edge capture is valid	RW
7	BUFPEN	Auto-reload ARR cache enable ● 0b0: Period cache disabled, written value immediately affects the period value ● 0b1: Period cache enabled, written value affects the period value after the next event update	RW
6:4	PRS	Internal clock frequency division selection ● 0b000: 1 ● 0b001: 2 ● 0b010: 4 ● 0b011: 8 ● 0b100: 16 ● 0b101: 32 ● 0b110: 64 ● 0b111: 256	RW
3	PWM2S	OCREFA dual-point compare selection ● 0b0: Dual-point compare enabled, uses CCRA and CCRB compares to control OCREFA output ● 0b1: Single-point compare enabled, only uses CCRA compare to control OCREFA output **Note** OCREFB remains unaffected and still uses CCRB to control OCREFB output.	RW
2	CT	Count clock selection ● 0b0: Internal count clock TCLK ● 0b1: External count clock ETR	RW
1	COMP	PWM complementary output mode selection ● 0b0: Independent PWM output ● 0b1: Complementary PWM output	RW

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Bit	Name	Functional Description	Access
0	CTEN	Timer enable ● 0b0: Disable ● 0b1: Enable It can be enabled by external trigger, and this bit is automatically cleared at the end of ONESHOT mode	RW

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14.5.4.4 Interrupt Flag Register (TIM_IFR)

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved												CB3F	CA3F	UNDF	OVF	TIF	BIF	CB2E	CB1E	CB0E	CA2E	CA1E	CA0E	CB2F	CB1F	CB0F	CA2F	CA1F	CA0F	Reserved	UIF
Access													RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO		RO

Bit	Name	Functional Description	Access
31:20	*Reserved*	-	-
19	CB3F	Channel CH3B compare match flag Only TIM3 exists ● 0b0: Not occurred ● 0b1: Occurred	RO
18	CA3F	Channel CH3A compare match flag Only TIM3 exists ● 0b0: Not occurred ● 0b1: Occurred	RO
17	UNDF	Underflow interrupt flag ● 0b0: Not occurred ● 0b1: Occurred	RO
16	OVF	Overflow interrupt flag ● 0b0: Not occurred ● 0b1: Occurred	RO
15	TIF	Trigger interrupt flag ● 0b0: Not occurred ● 0b1: Occurred	RO
14	BIF	Brake interrupt flag ● 0b0: Not occurred ● 0b1: Occurred	RO
13	CB2E	Channel CH2B capture data loss flag Only TIM3 exists ● 0b0: No data loss ● 0b1: Data loss	RO
12	CB1E	Channel CH1B capture data loss flag Only TIM3 exists ● 0b0: No data loss ● 0b1: Data loss	RO
11	CB0E	Channel CH0B capture data loss flag ● 0b0: No data loss ● 0b1: Data loss	RO

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Bit	Name	Functional Description	Access
10	CA2E	Channel CH2A capture data loss flag Only TIM3 exists ● 0b0: No data loss ● 0b1: Data loss	RO
9	CA1E	Channel CH1A capture data loss flag Only TIM3 exists ● 0b0: No data loss ● 0b1: Data loss	RO
8	CA0E	Channel CH0A capture data loss flag ● 0b0: No data loss ● 0b1: Data loss	RO
7	CB2F	Channel CH2B capture/compare match flag Only TIM3 exists ● 0b0: Not occurred ● 0b1: Occurred	RO
6	CB1F	Channel CH1B capture/compare match flag Only TIM3 exists ● 0b0: Not occurred ● 0b1: Occurred	RO
5	CB0F	Channel CH0B capture/compare match flag ● 0b0: Not occurred ● 0b1: Occurred	RO
4	CA2F	Channel CH2A capture/compare match flag Only TIM3 exists ● 0b0: Not occurred ● 0b1: Occurred	RO
3	CA1F	Channel CH1A capture/compare match flag Only TIM3 exists ● 0b0: Not occurred ● 0b1: Occurred	RO
2	CA0F	Channel CH0A capture/compare match flag ● 0b0: Not occurred ● 0b1: Occurred	RO
1	*Reserved*	-	-
0	UIF	Event update interrupt flag ● 0b0: Not occurred ● 0b1: Occurred	RO

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14.5.4.5 Interrupt Flag Clear Register (TIM_ICLR)

Offset	Bit Position																													
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000FFFF																															
Name	Reserved												CB3F	CA3F	UNDF	OVF	TIF	BIF	CB2E	CB1E	CB0E	CA2E	CA1E	CA0E	CB2F	CB1F	CB0F	CA2F	CA1F	CA0F	Reserved	UIF
Access													WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO		WO

Bit	Name	Functional Description	Access
31:20	*Reserved*	-	-
19	CB3F	Channel CH3B compare match flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1. Only TIM3 exists	WO
18	CA3F	Channel CH3A compare match flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1. Only TIM3 exists	WO
17	UNDF	Underflow interrupt flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
16	OVF	Overflow interrupt flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
15	TIF	Trigger interrupt flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
14	BIF	Brake interrupt flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
13	CB2E	Channel CH2B capture data loss flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1. Only TIM3 exists	WO
12	CB1E	Channel CH1B capture data loss flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1. Only TIM3 exists	WO
11	CB0E	Channel CH0B capture data loss flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
10	CA2E	Channel CH2A capture data loss flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1. Only TIM3 exists	WO
9	CA1E	Channel CH1A capture data loss flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1. Only TIM3 exists	WO
8	CA0E	Channel CH0A capture data loss flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO

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Bit	Name	Functional Description	Access
7	CB2F	Channel CH2B capture/compare match flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1. Only TIM3 exists	WO
6	CB1F	Channel CH1B capture/compare match flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1. Only TIM3 exists	WO
5	CB0F	Channel CH0B capture/compare match flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
4	CA2F	Channel CH2A capture/compare match flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1. Only TIM3 exists	WO
3	CA1F	Channel CH1A capture/compare match flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1. Only TIM3 exists	WO
2	CA0F	Channel CH0A capture/compare match flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
1	*Reserved*	-	-
0	UIF	Event update interrupt flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO

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14.5.4.6 Master-Slave Mode Control Register (TIM_MSCR)

Offset	Bit Position																													
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																			IB0S	IA0S	SMS			TS			MSM	CCDS	MMS		
Access																				RW	RW	RW			RW			RW	RW	RW		

Bit	Name	Functional Description	Access
31:13	*Reserved*	-	-
12	IB0S	CH0B input selection ● 0b0: CH0B ● 0b1: Internal trigger TS selection signal	RW
11	IA0S	IA0 input selection ● 0b0: CH0A ● 0b1: ▶ CH0A CH1A CH2A XOR (TIM3) ▶ CH0A ETR GATE XOR (TIM0/1/2) **Note** Setting to 1 will cause input changes upon any port transition.	RW
10:8	SMS	Slave mode function selection ● 0b000: Use internal clock ● 0b001: Reset function ● 0b010: Trigger mode ● 0b011: External clock mode ● 0b100: Quadrature encoder counting mode1 ● 0b101: Quadrature encoder counting mode2 ● 0b110: Quadrature encoder counting mode3 ● 0b111: Gating function	RW
7:5	TS	Trigger selection ● 0b000: Signal ETFP after port ETR filtered phase selection ● 0b001: Internal interconnect signal ITR0 ● 0b010: Internal interconnect signal ITR1 ● 0b011: Internal interconnect signal ITR2 ● 0b100: Internal interconnect signal ITR3 ● 0b101: Edge signal of port CH0A ● 0b110: Signal IAFP after port CH0A filtered phase selection ● 0b111: Signal IBFP after port CH0B filtered phase selection	RW

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<table>
<tr><th>Bit</th><th>Name</th><th>Functional Description</th><th>Access</th></tr>
<tr><td>4</td><td>MSM</td><td>Master-slave selection
● 0b0: No delay
● 0b1: Delay enabled, synchronously starts both master and slave counters
Note
When using the trigger mode, the slave mode is set to 0, and the master mode is set to 1, so that the master and slave counts can be started at the same time.</td><td>RW</td></tr>
<tr><td>3</td><td>CCDS</td><td>DMA compare trigger selection in compare mode
● 0b0: Compare match trigger DMA
● 0b1: Compare match does not trigger DMA, event update replaces compare match to trigger DMA</td><td>RW</td></tr>
<tr><td>2:0</td><td>MMS</td><td>Master mode input selection
For internal interconnection, connected to ITRx of other timers
<table>
<tr><th></th><th>TIM0/1/2</th><th>TIM3</th></tr>
<tr><td>0b000</td><td>Software update UG, write M23CR.UG</td><td>Software update UG, write M23CR.UG
Software update TG, write M23CR.TG</td></tr>
<tr><td>0b001</td><td>Timer enable CTEN</td><td>Timer enable CTEN</td></tr>
<tr><td>0b010</td><td>Timer event update UEV</td><td>Timer event update UEV</td></tr>
<tr><td>0b011</td><td>Compare match select output CMPSO</td><td>Compare match select output CMPSO</td></tr>
<tr><td>0b100</td><td>Timer compare parameter output OCREF0A</td><td>Timer compare parameter output OCREF0A</td></tr>
<tr><td>0b101</td><td>Timer compare parameter output OCREF0B</td><td>Timer compare parameter output OCREF1A</td></tr>
<tr><td>0b110</td><td>Timer compare parameter output OCREF0B</td><td>Timer compare parameter output OCREF2A</td></tr>
<tr><td>0b111</td><td>Timer compare parameter output OCREF0B</td><td>Timer compare parameter output OCREF0B</td></tr>
</table></td><td>RW</td></tr>
</table>

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14.5.4.7 Output Control/Input Filter Register (TIM_FLTR)

Offset	Bit Position																													
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	ETP	FLTET			BKP	FLTBK			CCPB2	OCMB2/FLTB2			CCPA2	OCMA2/FLTA2			CCPB1	OCMB1/FLTB1			CCPA1	OCMA1/FLTA1			CCPB0/CCPB0	OCMB0/FLTB0			CCPA0/CCPA0	OCMA0/FLTA0		
Access	RW	RW			RW	RW			RW	RW			RW	RW			RW	RW			RW	RW			RW	RW			RW	RW		

Bit	Name	Functional Description	Access
31	ETP	ETR input phase selection ● 0b0: Same phase ● 0b1: Inverted input	RW
30:28	FLTET	ETR filter control ● 0b000-0b011: Filter is invalid ● 0b100: PCLK, three consecutive valid samples ● 0b101: PCLK/4, three consecutive valid samples ● 0b110: PCLK/16, three consecutive valid samples ● 0b111: PCLK/64, three consecutive valid samples	RW
27	BKP	Brake BK input phase selection ● 0b0: Same phase ● 0b1: Inverted input	RW
26:24	FLTBK	Brake input filter control ● 0b000-0b011: Filter is invalid ● 0b100: PCLK, three consecutive valid samples ● 0b101: PCLK/4, three consecutive valid samples ● 0b110: PCLK/16, three consecutive valid samples ● 0b111: PCLK/64, three consecutive valid samples	RW
23	CCPB2	Compare function: CH2B channel compare output phase control ● 0b0: Normal output ● 0b1: Inverted output	RW
22:20	OCMB2	Compare function: CH2B channel compare control Refer to OCMB0 setting	RW
	FLTB2	Capture function: CH2B input channel filter setup Refer to FLTBK setting	RW
19	CCPA2	Compare function: CH2A channel compare output phase control ● 0b0: Normal output ● 0b1: Inverted output	RW

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Bit	Name	Functional Description	Access
18:16	OCMA2	Compare function: CH2A channel compare control Refer to OCMB0 setting	RW
	FLTA2	Capture function: CH2A input channel filter setup Refer to FLTBK setting	RW
15	CCPB1	Compare function: CH1B channel compare output phase control ● 0b0: Normal output ● 0b1: Inverted output	RW
14:12	OCMB1	Compare function: CH1B channel compare control Refer to OCMB0 setting	RW
	FLTB1	Capture function: CH1B input channel filter setup Refer to FLTBK setting	RW
11	CCPA1	Compare function: CH1A channel compare output phase control ● 0b0: Normal output ● 0b1: Inverted output	RW
10:8	OCMA1	Compare function: CH1A channel compare control Refer to OCMB0 setting	RW
	FLTA1	Capture function: CH1A input channel filter setup Refer to FLTBK setting	RW
7	CCPB0	Compare function: output compare mode CCPBx compare output CHBx port polarity control ● 0b0: Normal output ● 0b1: Inverted output	RW
	CCPB0	Encode count and slave mode gating function: input phase control CCPB0 slave mode gating, reset, external trigger, external clock using CH0B port input polarity control ● 0b0: Normal input ● 0b1: Inverted input	RW
6:4	OCMB0	Compare function: CH0B channel compare control ● 0b000: Force to 0 ● 0b001: Force to 1 ● 0b010: Force to 0 on compare match ● 0b011: Force to 1 on compare match ● 0b100: Toggle on compare match ● 0b101: Output high level for one clock cycle on compare match ● 0b110: PWM mode 1 ▶ Single point comparison During up-counting, the output is high level when CNT<CCRxy; during down-counting, the output is low level when CNT>CCRxy. ▶ Dual point comparison ◆ For sawtooth wave up-counting, the output is low level when CCRxA<CNT≤CCRxB ◆ For sawtooth wave down-counting, the output is high level when CCRxA<CNT≤CCRxB	RW

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Bit	Name	Functional Description	Access
6:4	OCMB0	◆ For triangular wave up-counting, the output is high level when CNT<CCRxA; for down-counting, the output is low level when CNT>CCRxB ● 0b111: PWM mode 2 ▶ Single point comparison During up-counting, the output is low level when CNT<CCRxy; during down-counting, the output is high level when CNT>CCRxy ▶ Dual point comparison ◆ For sawtooth wave up-counting, the output is high level when CCRxA≤CNT<CCRxB ◆ For sawtooth wave down-counting, the output is low level when CCRxA≤CNT<CCRxB ◆ For triangular wave up-counting, the output is low level when CNT<CCRxA; for down-counting, the output is high level when CNT>CCRxB	
	FLTB0	Capture function: CH0B input channel filter setup Refer to FLTBK setting **Note** In order to ensure the PWM output setting of OCMB0, GATE is used as the capture input in PWM complementary mode, and the filter setting is invalid.	RW
3	CCPA0	Compare function: output compare mode CCPAx compare output CHAx port polarity control ● 0b0: Normal output ● 0b1: Inverted output	RW
	CCPA0	Encode count and slave mode gating function: input phase control CCPA0 slave mode gating, reset, external trigger, external clock using CH0A port input polarity control ● 0b0: Normal input ● 0b1: Inverted input	RW
2:0	OCMA0	Compare function: channel A compare control Refer to OCMB0 setting	RW
	FLTA0	Capture function: CH0A input channel filter setup Refer to FLTBK setting	RW

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14.5.4.8 ADC Trigger Control Register (TIM_ADTR)

Offset	Bit Position																													
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								ADTE	CMB2E	CMB1E	CMB0E	CMA2E	CMA1E	CMA0E	UEVE
Access																									RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7	ADTE	Enable ADC trigger global control ● 0b0: Disable ● 0b1: Enable	RW
6	CMB2E	Channel 2B compare match trigger ADC enable Only TIM3 exists ● 0b0: Disable ● 0b1: Enable	RW
5	CMB1E	Channel 1B compare match trigger ADC enable Only TIM3 exists ● 0b0: Disable ● 0b1: Enable	RW
4	CMB0E	Channel 0B compare match trigger ADC enable ● 0b0: Disable ● 0b1: Enable	RW
3	CMA2E	Channel 2A compare match trigger ADC enable Only TIM3 exists ● 0b0: Disable ● 0b1: Enable	RW
2	CMA1E	Channel 1A compare match trigger ADC enable Only TIM3 exists ● 0b0: Disable ● 0b1: Enable	RW
1	CMA0E	Channel 0A compare match trigger ADC enable ● 0b0: Disable ● 0b1: Enable	RW
0	UEVE	Event update trigger ADC enable ● 0b0: Disable ● 0b1: Enable	RW

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14.5.4.9 Channel x Control Register (TIM_CRCHx) (x=0/1/2)

Offset: 0x024 (CRCH0), 0x028 (CRCH1), 0x02C (CRCH2)

Note

CRCH1/CRCH2 only TIM3 exists.

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00003000																															
Name	Reserved																CCGB	CCGA	CISB		CDEB	CDEA	CIEB	CIEA	BUFEB	BUFEA	CSB	CSA	CFB_CRB/BKSB		CFA_CRA/BKSA	
Access																	WO	WO	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15	CCGB	Capture compare B software trigger Hardware auto-clear, writing 1 triggers the following actions, writing 0 has no effect: ● In compare mode, generates interrupt only ● In capture mode, generates interrupt and captures counter value to capture register	WO
14	CCGA	Capture compare A software trigger Hardware auto-clear, writing 1 triggers the following actions, writing 0 has no effect: ● In compare mode, generates interrupt only ● In capture mode, generates interrupt and captures counter value to capture register	WO
13:12	CISB	B channel compare match setting ● 0b00: No match ● 0b01: Compare match during up-counting ● 0b10: Compare match during down-counting ● 0b11: Compare match during both up/down counting	RW
11	CDEB	B capture compare trigger DMA enable ● 0b0: Disable ● 0b1: Enable	RW
10	CDEA	A capture compare trigger DMA enable ● 0b0: Disable ● 0b1: Enable	RW
9	CIEB	B capture compare trigger interrupt enable ● 0b0: Disable ● 0b1: Enable	RW

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Bit	Name	Functional Description	Access
8	CIEA	A capture compare trigger interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
7	BUFEB	Compare function: B compare cache enable control ● 0b0: Disable ● 0b1: Enable	RW
6	BUFEA	Compare function: A compare cache enable control ● 0b0: Disable ● 0b1: Enable	RW
5	CSB	B channel capture/compare function selection ● 0b0: Compare mode ● 0b1: Capture mode	RW
4	CSA	A channel capture/compare function selection ● 0b0: Compare mode ● 0b1: Capture mode	RW
3:2	CFB_CRB	Capture function: channel B rising falling edge capture enable ● 0b00: Disable ● 0b01: Rising edge capture ● 0b10: Falling edge capture ● 0b11: Both rising and falling edge capture	RW
	BKSB	Compare function: channel B output brake level control ● 0b00: High-impedance output ● 0b01: No effect on output ● 0b10: Force output low level ● 0b11: Force output high level	RW
1:0	CFA_CRA	Capture function: channel A rising falling edge capture enable ● 0b00: Disable ● 0b01: Rising edge capture ● 0b10: Falling edge capture ● 0b11: Both rising and falling edge capture	RW
	BKSA	Compare function: channel A output brake level control ● 0b00: High-impedance output ● 0b01: No effect on output ● 0b10: Force output low level ● 0b11: Force output high level	RW

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14.5.4.10 Dead Time Register (TIM_DTR)

Offset	Bit Position																													
0x030	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																	VCE	SAFEEN	MOE	AOE	BKE	DTEN	BKSEL	DTR							
Access																		RW	RW	RW	RW	RW	RW	RW	RW							

Bit	Name	Functional Description	Access
31:15	*Reserved*	-	-
14	VCE	VC brake enable ● 0b0: Disable ● 0b1: Enable	RW
13	SAFEEN	Safety brake enbale (DeepSleep/reset) ● 0b0: Disable ● 0b1: Enable	RW
12	MOE	PWM output enable ● 0b0: Disable ● 0b1: Enable	RW
11	AOE	PWM output automatically enable ● 0b0: Disable ● 0b1: Enable	RW
10	BKE	Port brake enable ● 0b0: Disable ● 0b1: Enable	RW
9	DTEN	Dead time control enable ● 0b0: Disable ● 0b1: Enable	RW
8	BKSEL	Brake selection ● 0b0: Use own brake control ● 0b1: TIM1/2 uses brake control of TIM0 **Note** TIM0 and TIM3 bit selection is invalid.	RW

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<table>
<tr><th>Bit</th><th>Name</th><th>Functional Description</th><th>Access</th></tr>
<tr><td>7:0</td><td>DTR</td><td>Dead time
<table>
<tr><th>DTR</th><th>T</th><th>dt</th><th>step</th></tr>
<tr><td>DTR[7]=0b0</td><td>DTR[6:0] + 2</td><td>2-129</td><td>1</td></tr>
<tr><td>DTR[7:6]=0b10</td><td>{DTR[5:0] + 64}* 2 + 2</td><td>130-256</td><td>2</td></tr>
<tr><td>DTR[7:5]=0b110</td><td>{DTR[4:0] + 32}* 8 + 2</td><td>258-506</td><td>8</td></tr>
<tr><td>DTR[7:5]=0b111</td><td>{DTR[4:0] + 32}* 16 + 2</td><td>514-1010</td><td>16</td></tr>
</table></td><td>RW</td></tr>
</table>

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14.5.4.11 Repeat Cycle Setting Value Register (TIM_RCR)

Offset	Bit Position																													
0x034	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																						UND	OV	RCR							
Access																							RW	RW	RW							

Bit	Name	Functional Description	Access
31:10	*Reserved*	-	-
9	UND	Underflow mask control for repeating counting ● 0b0: Down-counting overflow enable ● 0b1: Down-count overflow mask	RW
8	OV	Overflow mask control for repetiting counting ● 0b0: Up-counting overflow enable ● 0b1: Up-counting overflow mask	RW
7:0	RCR	Repetition period count value Sets RCR+1 periods. The overflow controlled by [9:8] generates an update event. When the counter overflows up or down, the internal RCR_CNT decrements by 1. When counting reaches zero, RCR_CNT reloads the RCR value and generates an update event UEV signal.	RW

14.5.4.12 Reload Register/Period Mapped Address (TIM_ARRDM)

Offset	Bit Position																													
0x038	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																ARRDM															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	ARRDM	Reload register/period register With cache function, when the counter is not enabled or the cache is not enabled, the cache register can be updated immediately	RW

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14.5.4.13 Channel x Compare Capture Register (TIM_CCRxy) (x=0/1/2, y=A/B)

Offset: 0x03C (CCR0A), 0x040 (CCR0B), 0x044 (CCR1A), 0x048 (CCR1B), 0x04C (CCR2A), 0x050 (CCR2B)

Note

CCR1A/CCR1B/CCR2A/CCR2B only TIM3 exists.

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																CCRxy															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	CCRxy	Compare capture register Comparison with cache function	RW

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14.5.4.14 Channel 3A Compare Register (TIM_CCR3A) (Only TIM3 Exists)

Offset	Bit Position																													
0x054	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																						CCR3A									
Access																							RW									

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	CCR3A	Compare register Comparison with cache function	RW

14.5.4.15 Channel 3A Control Register (TIM_CRCH3A) (Only TIM3 Exists)

Offset	Bit Position																													
0x058	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																										C3AEN	CIS		CDE	CIE	BUF
Access																											RW	RW		RW	RW	RW

Bit	Name	Functional Description	Access
31:6	*Reserved*	-	-
5	C3AEN	Channel compare enable ● 0b0: Disable ● 0b1: Enable	RW
4:3	CIS	Channel compare match setting ● 0b00: No match ● 0b01: Compare match during up-counting ● 0b10: Compare match during down-counting ● 0b11: Compare match during both up/down counting	RW
2	CDE	Compare trigger DMA enable ● 0b0: Disable ● 0b1: Enable	RW
1	CIE	Compare trigger interrupt enable ● 0b0: Disable ● 0b1: Enable	RW

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Bit	Name	Functional Description	Access
0	BUF	Compare cache enable ● 0b0: Disable ● 0b1: Enable	RW

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14.5.4.16 Channel 3B Compare Register (TIM_CCR3B) (Only TIM3 Exists)

Offset	Bit Position																													
0x05C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																CCR3B															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	CCR3B	Compare register Comparison with cache function	RW

14.5.4.17 Channel 3B Control Register (TIM_CRCH3B) (Only TIM3 Exists)

Offset	Bit Position																													
0x060	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																										C3BEN	CIS		CDE	CIE	BUF
Access																											RW	RW		RW	RW	RW

Bit	Name	Functional Description	Access
31:6	*Reserved*	-	-
5	C3BEN	Channel compare enable ● 0b0: Disable ● 0b1: Enable	RW
4:3	CIS	Channel compare match setting ● 0b00: No match ● 0b01: Compare match during up-counting ● 0b10: Compare match during down-counting ● 0b11: Compare match during both up/down counting	RW
2	CDE	Compare trigger DMA enable ● 0b0: Disable ● 0b1: Enable	RW
1	CIE	Compare trigger interrupt enable ● 0b0: Disable ● 0b1: Enable	RW

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Bit	Name	Functional Description	Access
0	BUF	Compare cache enable ● 0b0: Disable ● 0b1: Enable	RW

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15 LPTIM

15.1 Introduction

The LPTimer is an asynchronous 16-bit timer/counter that can continue timing/counting via the internal low-speed RC oscillator, external low-speed crystal oscillator, even after the system clock is turned off. Wake up the system in low power mode through interrupts.

This module includes 2 low power timers, which can be cascaded internally.

15.2 Features

- 16-bit asynchronous counter/timer
- Optional counting/timing clock sources: RCL/PCLK/XTL
- 3 bits prescaler configuration register, supporting a maximum prescaler value of 256
- ARR reload configurable
- Overflow interrupt wake-up

15.3 Functional Description

15.3.1 Function Block Diagram

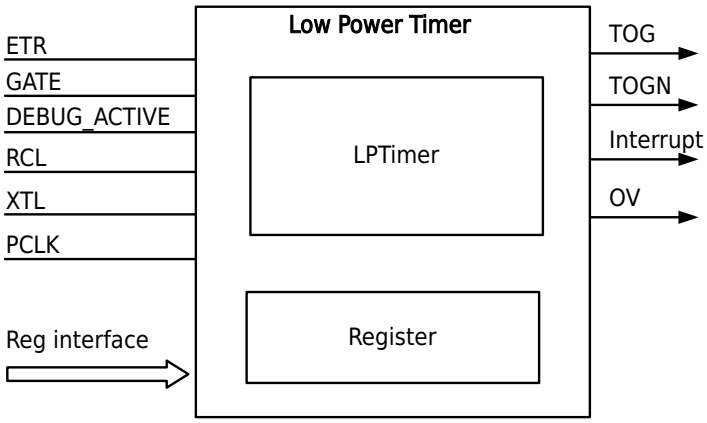

Figure 15-1 LPTimer Block Diagram

15.3.2 Working Mode

LPTimer supports 2 working modes, each timer/counter has an independent control start signal, as well as external input clock and gating signal.

LPTimer utilizes ETR (External Trigger) and GATE for counting operations:

- ETR serves as an external input clock signal for the counter.
- GATE acts as an active-level counting enable signal.

The timer of LPTimer supports two working modes. The working mode can be selected by setting CR.MD: Mode 1 is a 16-bit free-counting mode, and Mode 2 is a 16-bit overloading mode.

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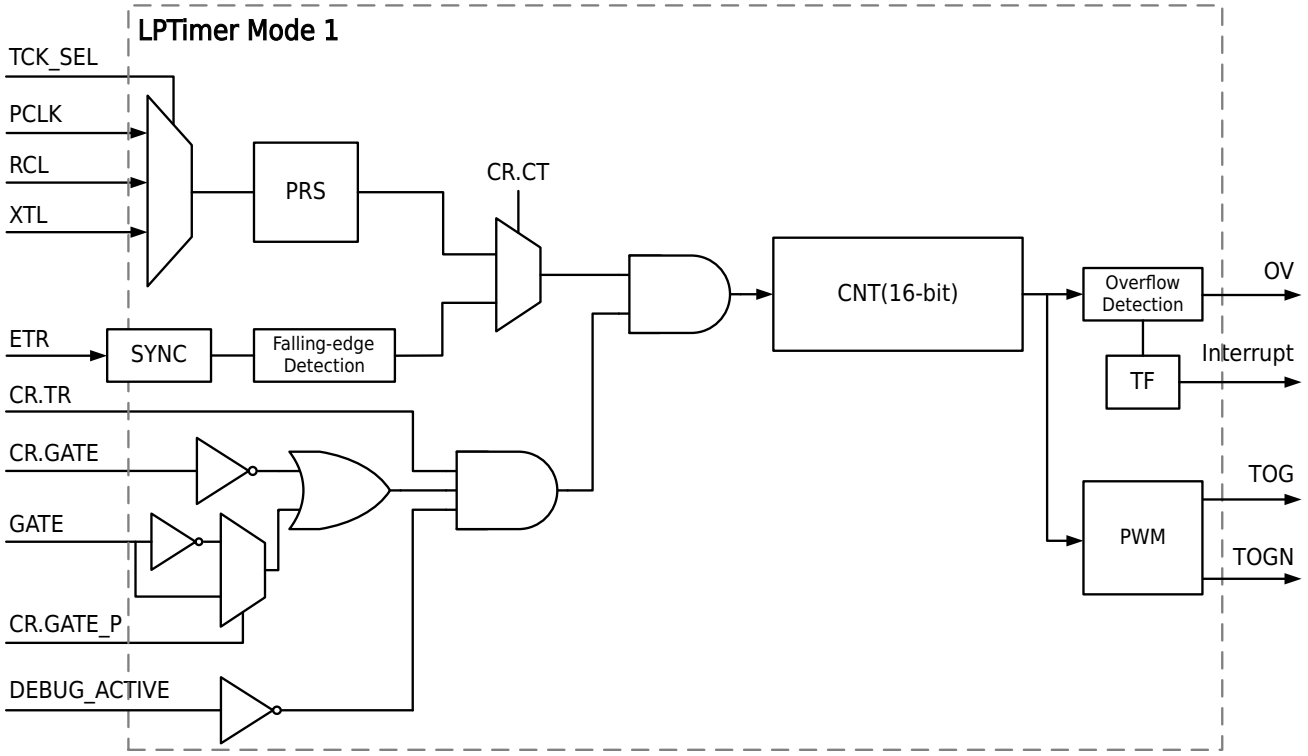

Figure 15-2 LPTimer Mode 1

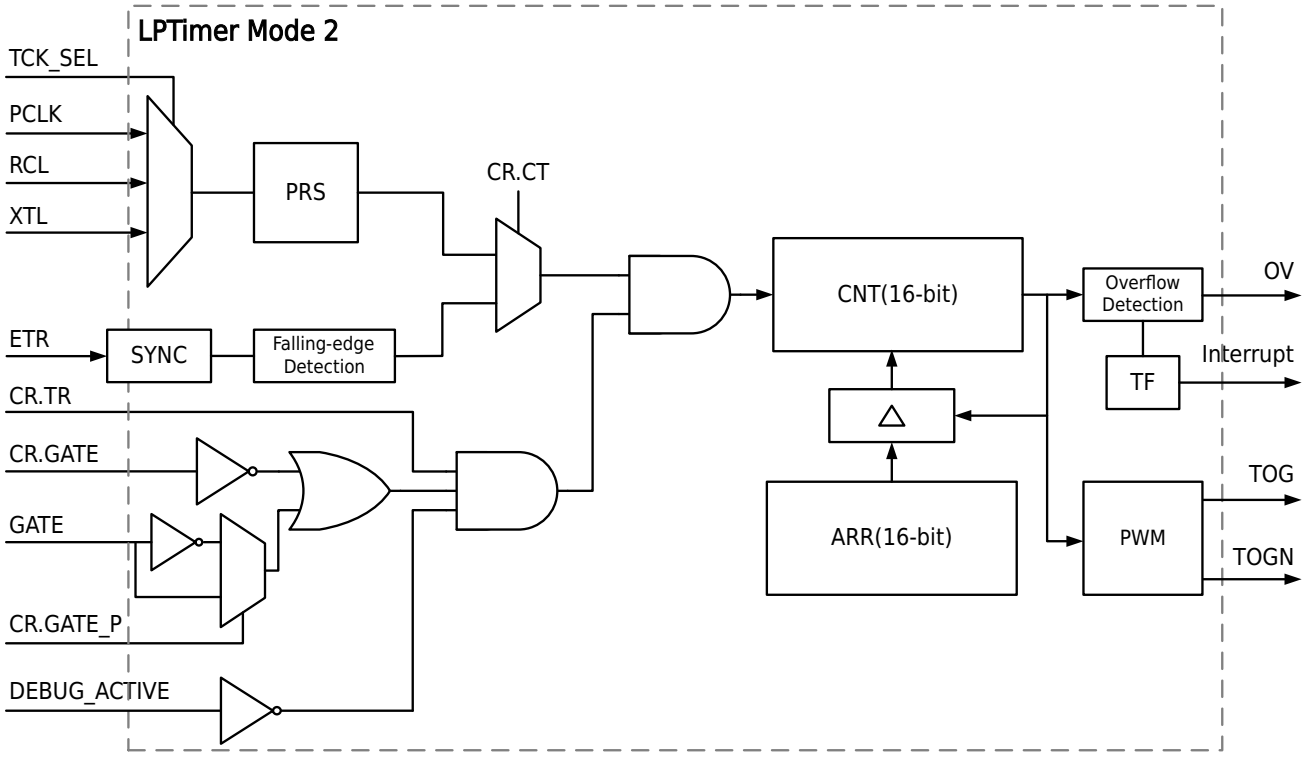

Figure 15-3 LPTimer Mode 2

When LPTimer starts, it will automatically load the value of the reload register ARR into the counter. LPTimer can select 3 clock sources as the timer clock via control register CR.TCK_SEL (default: PCLK). The clock selection is as shown in the table:

TCK_SEL	Timer Clock	Read Timer Count Value
0b00	PCLK	Read synchronized

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TCK_SEL	Timer Clock	Read Timer Count Value
0b01	PCLK	No synchronize
0b10	XTL	Read synchronized
0b11	RCL	Read synchronized

When the corresponding timer TR is set to 1, the timer starts to run. The counter starts counting from the set value, and generates an overflow interrupt after counting to a maximum of 0xFFFF. After Mode 1 generates an interrupt, the counter is cleared and continues to count up. After Mode 2 generates an interrupt, the value of the reload register ARR is transferred to the counter and counts up. The initial value of the counter CNT is automatically loaded by ARR when the timer is started.

15.3.3 Counting Function

Counting functions are used to determine the number of times an event occurs. In the counting function, the counter increments every falling edge of the corresponding input clock. The input signal is sampled by the internal count clock, so the external input clock frequency cannot exceed the system count clock. Counting to the maximum value will overflow and generate an interrupt.

15.3.4 Timing Function

The timing function is used to generate interval timing. In the timing function, the timer accumulates once per clock, and when the count reaches the maximum value, it will overflow and generate an interrupt.

The timing clock cycle count is (0xFFFF-ARR+0x0001) (when reload mode is enabled).

15.3.5 GATE Interconnection

When LPTIMx_G=0b000, the gate control GATE input is the port input selected by Pxy_SEL. When LPTIMx_G=0b001-0b111, it is connected to the input or output of other modules. For details, refer to the descriptions of the registers in the "General-Purpose I/O (GPIO)" chapter: "Port Auxiliary Function Timer Gate Selection (GPIO_TIMGS)", "Port Auxiliary Function PCA Capture Selection (GPIO_PCAS)".

15.3.6 ETR Interconnection

When LPTIMx_E=0b000, the ETR input is the port input selected by Pxy_SEL. When LPTIMx_E=0b001-0b111, it is connected to the input or output of other modules. For details, refer to the descriptions of the registers in the "General-Purpose I/O (GPIO)" chapter: "Port Auxiliary Function Timer ETR Selection (GPIO_TIMES)", and "Port Auxiliary Function PCA Capture Selection (GPIO_PCAS)".

Set the external input LPTIM1_E of the LPTIM1 timer to 0b101, the toggle output LPTIM0_TOG signal of LPTIM0 is selected to be output from inside the chip to LPTIM1, as the external clock input of LPTIM1, which is set to external counting mode. In this way, two timers can be used in cascade.

15.3.7 Toggle Output Interconnection

The LPTimer flip is output to the port, which can drive the Buzzer to realize the control of the buzzer.

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15.4 Register Description

15.4.1 Register List

- LPTimer0 base address: 0x40000F00
- LPTimer1 base address: 0x40000F40

Table 15-2 Low Power Timer (LPTIM) Register Offset

Offset	Register	Description	Width
0x000	LPTIM_CNT	Counter Count Value Register	32
0x004	LPTIM_ARR	Reload Register	32
0x00C	LPTIM_CR	Control Register	32
0x010	LPTIM_IFR	Interrupt Flag Register	32
0x014	LPTIM_ICLR	Interrupt Flag Clear Register	32

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15.4.2 Counter Count Value Register (LPTIM_CNT)

Offset	Bit Position																													
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																CNT															
Access																	RO															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	CNT	Timer count value	RO

15.4.3 Reload Register (LPTIM_ARR)

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																ARR															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	ARR	Timer reload register Before writing the ARR register, the CR.WT_FLAG must be read. Data can be written only when WT_FLAG is 1. After writing to the ARR register, CR.WT_FLAG is set to 0. **Note** This value will be loaded into the timer counter when the timer is started or reloaded. The timer counter value cannot be changed by software.	RW

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15.4.4 Control Register (LPTIM_CR)

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000088																															
Name	Reserved																		PRS			IE	GATE_P	GATE	WT_FLAG	Reserved	TCK_SEL		TOG_EN	CT	MD	TR
Access																			RW			RW	RW	RW	RO		RW		RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:14	*Reserved*	-	-
13:11	PRS	Prescaler Cannot be changed while the timer is running ● 0b000: 1 ● 0b001: 2 ● 0b010: 4 ● 0b011: 8 ● 0b100: 16 ● 0b101: 32 ● 0b110: 64 ● 0b111: 256	RW
10	IE	Interrupt enable control ● 0b0: Disable ● 0b1: Enable	RW
9	GATE_P	GATE polarity control ● 0b0: High level is valid ● 0b1: Low level is valid	RW
8	GATE	Timer gating ● 0b0: No gate control, the timer works when TR=1 ● 0b1: The timer operates only when the gate is set to 1 and TR=1	RW
7	WT_FLAG	WT write synchronization flag ● 0b0: Synchronizing, writing ARR is invalid ● 0b1: Synchronization is complete, ARR can be changed at this time	RO
6	*Reserved*	-	-
5:4	TCK_SEL	LPTimer clock selection ● 0b00: PCLK ● 0b01: PCLK ● 0b10: XTL ● 0b11: RCL	RW

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Bit	Name	Functional Description	Access
3	TOG_EN	TOG output enable ● 0b0: TOG, TOGN output 0 at the same time ● 0b1: TOG, TOGN output signals with opposite phases for buzzers	RW
2	CT	Counter/timer function selection ● 0b0: Timer function, the timer uses the clock selected by TCK_SEL to count ● 0b1: Counter function, the counter uses the falling edge of the external input to count **Note** The sampling clock uses the clock selected by TCK_SEL, and the external input clock is lower than 1/2 sampling clock.	RW
1	MD	Timer working mode ● 0b0: Mode 1 no reload mode 16-bit counter/timer ● 0b1: Mode 2 auto-reload 16-bit counter/timer	RW
0	TR	Timer run control bit ● 0b0: Timer stop ● 0b1: Timer run	RW

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15.4.5 Interrupt Flag Register (LPTIM_IFR)

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																														OV	
Access																															RO	

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-
0	OV	Counter overflow flag ● 0b0: No overflow ● 0b1: Overflow	RO

15.4.6 Interrupt Flag Clear Register (LPTIM_ICLR)

Offset	Bit Position																													
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																														OV	
Access																															WO	

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-
0	OV	Counter overflow flag cleared Write 0 to clear flag, write 1 has no effect; read always returns 0.	WO

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16 PCA

16.1 Introduction

The PCA (Programmable Counter Array) supports up to five 16-bit capture/compare modules. The timer/counter can be used as a common clock count/event counter capture/compare function. Each module of the PCA can be independently programmed to provide input capture, output compare, or pulse width modulation. In addition, module 4 has an additional watchdog timer mode.

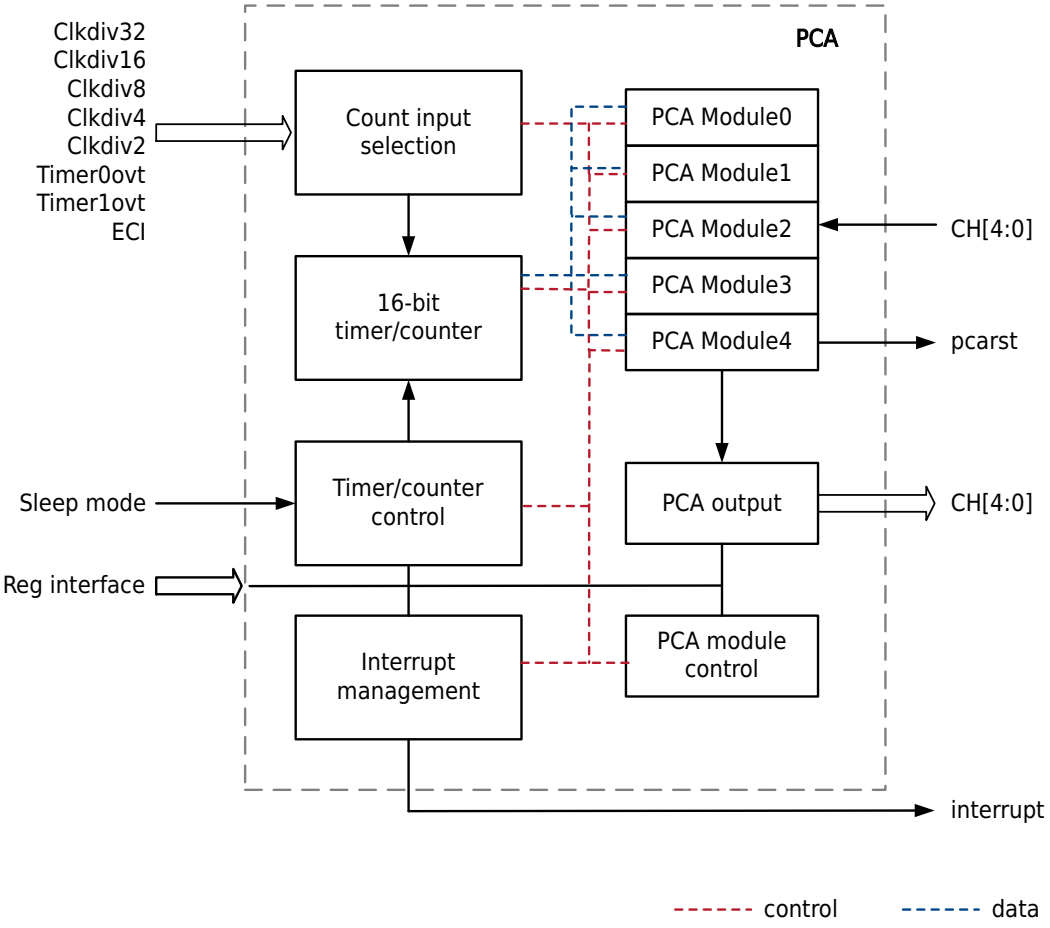

Figure 16-1 PCA Overall Block Diagram

16.2 Functional Description

PCA all five modules can be configured to work independently, and there are three working modes: edge-triggered capture, output comparison, and 8/16-bit pulse width modulation. Each module has its own function registers in the system controller, and these registers are used to configure the working mode of the module and exchange data with the module.

Each comparison/capture module is composed of a comparison/capture register group (CCAPx), a 16-bit comparator, and various logic gate controls. The register group is used to store time or times, for external trigger capture conditions, or internal trigger comparison conditions. In 8-bit PWM mode, the register (CCAPxL) is used to control the duty cycle of the output waveform, and CCAPxH is an 8-bit compare buffer. In 16-bit PWM mode, CARR is used to control the period of PWM output, and the CCAPx register controls the duty cycle.

Each module can be independently programmed to operate in any of the following modes:

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- 16-bit capture mode triggered by rising edge, falling edge, or any edge.
- Compare mode: 16-bit high-speed output, 16-bit watchdog timer (module 4) or 16/8-bit PWM.
- Disabled.

The Compare/Capture Module Mode Registers (CCAPMx) determine the corresponding operating mode. When programming the compare/capture modules, they are based on a common time count. The timer/counter is turned on and off through the CCON.CR bit to control the operation of the PCA timer/counter. On a compare/capture module capture, the software timer, high-speed output, sets the module's compare/capture flag (CCON.CCFx), and generates a PCA interrupt request if the corresponding enable bit is set in the CCAPMx register. The CPU can read and write the CCAPx registers at any time.

16.2.1 PCA Timer/Counter

This group of special function registers of CNT can be used as a 16-bit timer/counter. This is a 16-bit up counter. If the CMOD.CFIE bit is set to 1 when the CNT overflows, the hardware automatically sets the PCA overflow flag (CCON.CF) and generates a PCA interrupt request. CMOD.CPS[2: 0] three bits select eight signals to input to timer/counter.

- The system clock PCLK is divided by 32
- The system clock PCLK is divided by 16
- The system clock PCLK is divided by 8
- The system clock PCLK is divided by 4
- The system clock PCLK is divided by 2
- Timer 0 overflow

  CNT is incremented each time Timer 0 overflows, thus providing a variable programming frequency input to the PCA.
- Timer 1 overflow

  CNT is incremented each time Timer 1 overflows, thus providing a variable programming frequency input to the PCA.
- ECI

  The CPU samples the PCAECI every 4 PCLK clock cycles. When the sampling result changes from high to low each time, CL is automatically increased by 1. Therefore, the highest ECI input frequency cannot be higher than 1/8 of the system clock PCLK to meet sampling requirements.

Set the run controller (CCON.CR) to start the PCA timer/counter. When CMOD.CIDL is set to 1 the PCA timer/counter can continue to run in idle mode. The CPU can read the value of CNT at any time, but when the count is started (CCON.CR=1), in order to prevent counting errors, CNT is prohibited from being written.

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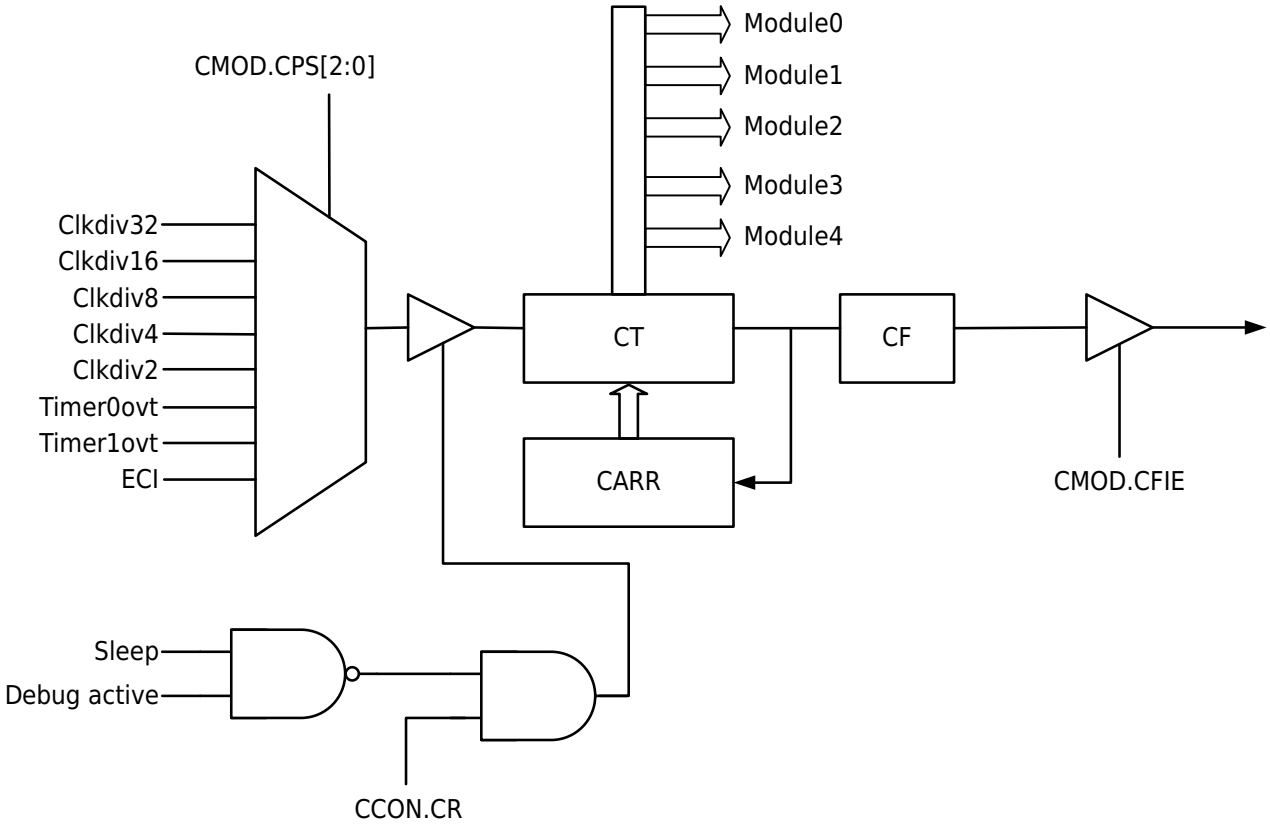

Figure 16-2 PCA Counter Block Diagram

16-bit Free Count Mode

After the counter counts to the maximum value of 0xFFFF and overflows, the value of the counter becomes 0 and starts counting up again. If you need to change the counting period value, you can stop PCA to change the initial value of the counter and continue counting. Can be used in PCA capture mode, 8-bit PWM mode.

16-bit Reload Count Mode

When the counter counts to the same value as the register CARR, the value of the counter overflows and becomes 0, and continues to count up. It can be used in PCA capture mode and 16-bit PWM mode.

16.2.2 PCA Capture Function

PCA capture mode provides 5- way PCA to measure pulse period, pulse width, duty cycle and phase difference.

A level transition on the pin causes the PCA to capture the value of the PCA counter/timer and load it into the corresponding module's 16 -bit capture/compare register (CCAPx). The CCAPMx.CAPP and CCAPMx.CAPN bits are used to select the type of level change that triggers the capture: low to high (positive edge), high to low (negative edge), or any change (positive or negative edge) . When a capture occurs, the capture/compare flag (CCFn) in CCON is set to logic 1 and an interrupt request is generated (if CCF interrupts are enabled). When the CPU turns to the interrupt service routine, the CCFn bit cannot be automatically cleared by hardware, and the user software can write the INTCL register to clear this flag bit. If the CCAPMx.CAPP and CCAPMx.CAPN bits are both set to logic 1, you can directly read the state of the corresponding port pin to determine whether the capture is triggered by a rising edge or a falling edge.

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The resolution is equal to the clock of the timer/counter. 2 clock cycles during the high level or low level to ensure that the input signal can be recognized by the hardware.

The CPU can read or write the CCAPx registers at any time.

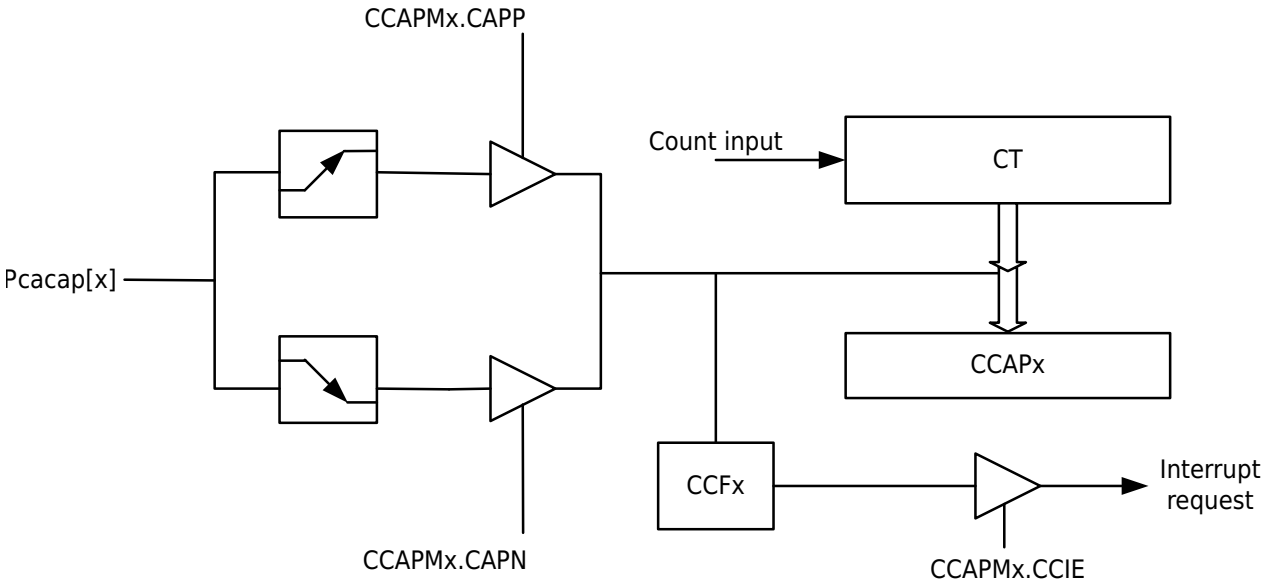

Figure 16-3 PCA Capture Functional Block Diagram

16.2.3 PCA Comparison Function

The comparison function provides the following functions, high-speed output mode, WDT mode, 16-bit PWM mode and 8-bit PWM mode. In the first three functions, the compare/capture module compares the value of the 16-bit PCA timer/counter with the 16-bit value preloaded into the module's CCAPx register. In 8-bit PWM mode, the PCA module continuously compares the PCA Timer/Counter Low Register (CNT) with an 8-bit value in the CCAPxL module register. The comparison is done every 4 clock cycles, which matches the clock rate of the fastest PCA timer/counter.

Setting the CCAPMx.ECOM bit selects the compare function for this module.

To use modules in compare mode correctly, follow the general procedure below:

- Select the operating mode of the PCA module.
- Select the input signal for the PCA timer/counter.
- The compare value is loaded into the module's compare/capture register pair.
- Set the PCA timer/counter run control bit.
- An interrupt is generated after a match, and the compare/capture flag of the module is cleared.

16.2.3.1 Compare Toggle Output Mode

In the compare toggle output mode, whenever the value in the PCA counter matches the 16-bit capture/compare register (CCAPx) of the module, the logic level on the CH[x] pin of the module PCA will change. higher precision than switching IO output, because this output will not be interrupted to respond and affect the output frequency. If the CPU is used to switch the IO output, power consumption and precision are lacking.

To set the compare toggle output mode of a compare/capture module, set the CCAPMx.ECOM, CCAPMx.MAT and CCAPMx.TOG bits. PCA timer/counter and the compare/capture register (CCAPx) toggles the PCA 's CH[x] signal and sets the module's compare/capture flag (CCON.CCFx). By software

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setting or clearing the CH[x] signal of the PCA, the user can choose to match the switching signal from low to high or high to low.

The user can also choose to generate an interrupt request, by setting the corresponding interrupt enable bit (CCAPMx.CCIE), when a match occurs, an interrupt request can be generated. Since the compare/capture flag interrupt cannot be cleared by hardware, the user must clear this flag in software. If the user does not change the comparison/capture register in the interrupt program, PCA will re-count the comparison value, and if it matches, the next rollover will occur. In the interrupt service routine, a new 16-bit compare value can be written to the compare/capture register (CCAPx).

Notice

To prevent invalid matches, user software is required write CCAPxL first, then by CCAPxH register. Writing to the CCAPxL register will clear the ECOM bit in the CCAPMx register (set it to 0).

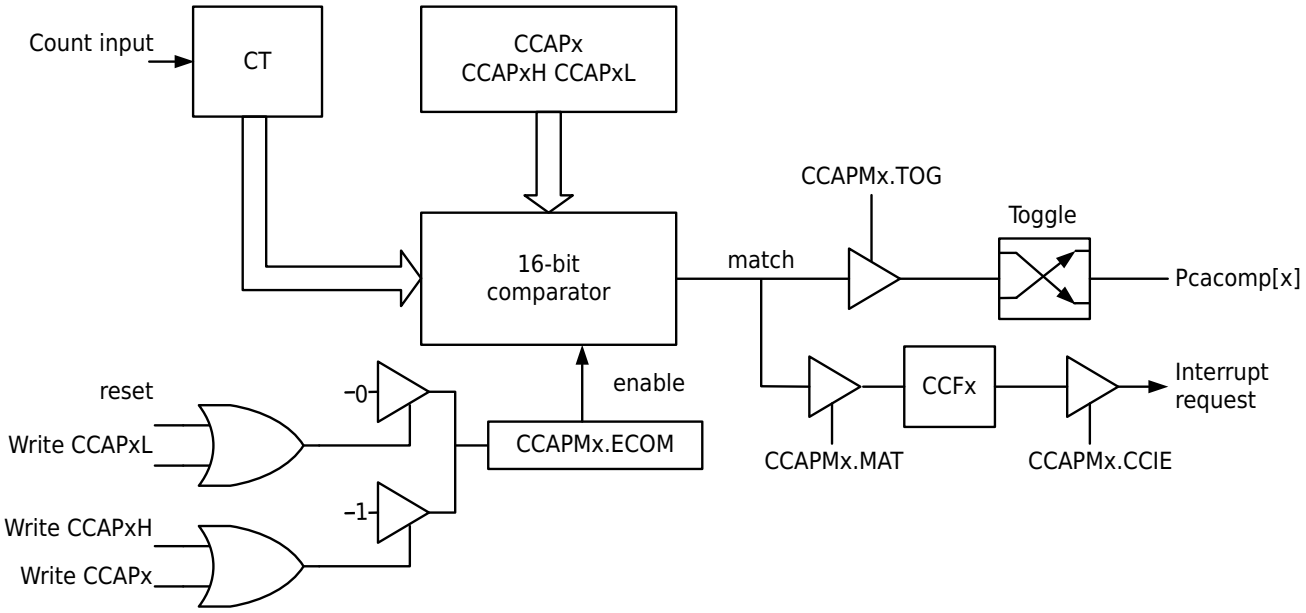

Figure 16-4 PCA Compare Functional Block Diagram

16.2.3.2 PCA 16-Bit PWM Function

In compare output PWM mode, whenever the value in the PCA counter matches the 16-bit capture/compare register (CCAPx) of the module, the logic level on the CH[x] pin of the module PCA will change. When the counter overflows, the logic level on the CH[x] pin will be cleared. This can provide a set of 16-bit PWM outputs.

To set the PWM mode of a compare/capture module, set the CCAPMx.ECOM, CCAPMx.MAT and CCAPMx.TOG bits and the EPWM register. PCA timer/counter and the compare/capture register (CCAPx) toggles the PCA 's CH[x] signal and sets the module's compare/capture flag (CCON.CCFx).

The user can also choose to generate an interrupt request, by setting the corresponding interrupt enable bit (CCAPMx.CCIE), when a match occurs, an interrupt request can be generated. Since the compare/capture flag interrupt cannot be cleared by hardware, the user must clear this flag in software.

Notice

When using 16-bit PWM mode, it is recommended not to use PCA clock division; otherwise, the maximum output duty cycle may differ by one cycle.

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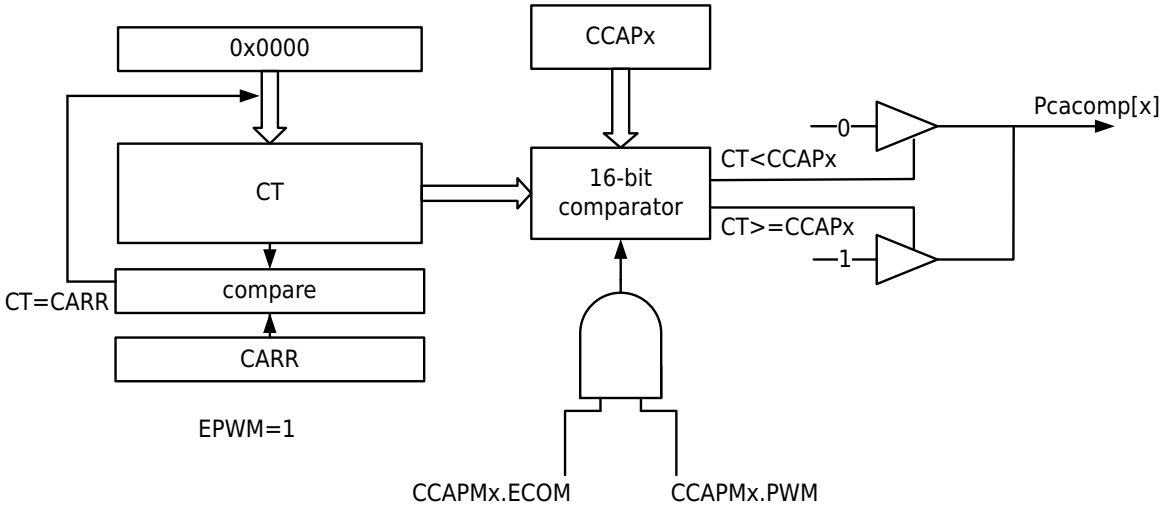

Figure 16-5 PCA 16-bit PWM Functional Block Diagram

16.2.3.3 WDT Function of PCA Module 4

In addition to WDT hardware module and PCA module 4, this series also provides a 16-bit WDT with programmable frequency. This mode generates a reset signal when the count value of the PCA timer/counter matches the value compare/capture register (CCAP4) stored in module 4. WDT reset signal of PCA is used as an independent reset signal. Combined with external reset (RST), hardware watchdog reset (WDTRST) and LVD low voltage reset, POR power-on and power-off reset. Users are free to combine them or use them individually. Module 4 is the one with the unique PCA of the WDT pattern. When not set as WDT, it can be used independently in other modes.

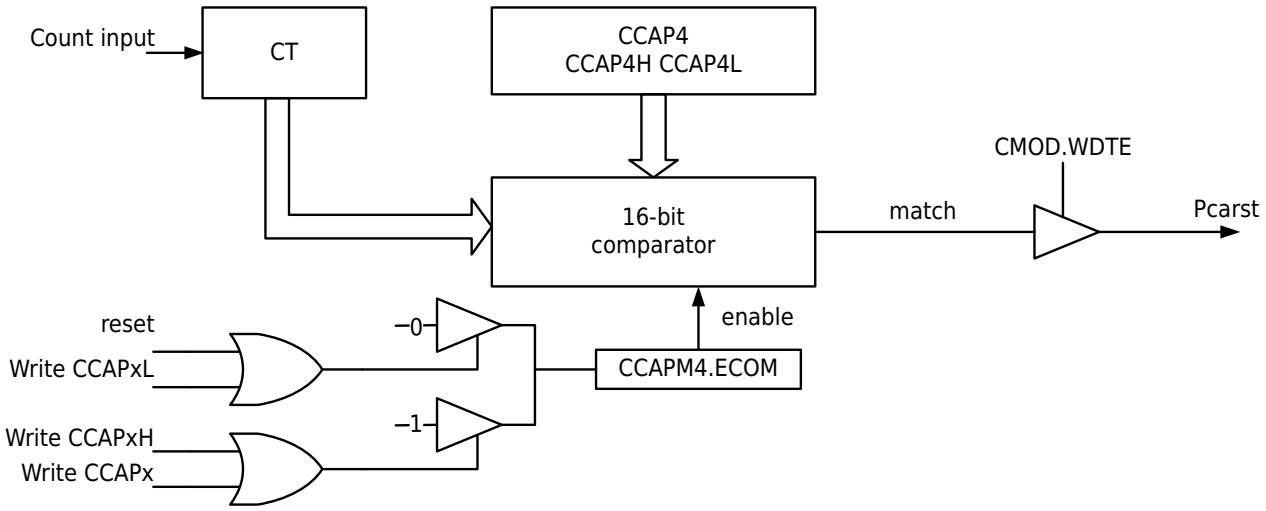

Figure 16-6 PCA WDT Functional Block Diagram

When PCA module 4 is used as WDT, CCAPM4.ECOM4, CCAPM4.MAT4 and CMOD.WDTE must be set. In addition, the PCA timer/counter can set CMOD.CPS to select different input counting frequencies.

Input a 16-bit compare value in the compare/capture register (CCAP4). In the PCA timer/counter (CNT), enter a 16-bit initial value or use a reset value (0x0000). These values multiplied by the PCA input pulse rate determines the WDT match run time. Setting the timer/counter run control bit (CCON.CR) starts the PCAWDT. The WDT of the PCA generates a reset signal every time there is a match. To prevent a PCAWDT from resetting, the user has three options.

- Periodically the comparison value CCAP4 changes, so a match never occurs.
- Periodically change the PCA timer/counter value (CNT) so a match never happens.

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- Disable the module reset output signal by clearing the CMOD.WDTE bit before a match, and then re-enable it later.

Note

The first two options are more reliable because the WDT is not disabled in the third option.

In most cases, the first option is recommended. The second option is not recommended when other PCA modules are in use, as all five modules share a common time base.

16.2.3.4 PCA 8-bit PWM Function

Pulse Width Modulation is a technique that uses a program to control the duty cycle, period, and phase of a waveform. Each of the five PCA modules can be used independently to generate a pulse width modulation (PWM) output on the corresponding PCA's CH[x] pin, with a pulse width of 8-bit resolution. The frequency of the PWM output depends on the time base of the PCA counter/timer. Use the capture/compare register CCAPxL of the module to change the duty cycle of the PWM output signal. When the low byte (CL) of the PCA counter/timer is equal to the value in CCAPxL, the output on the CH[x] pin of the PCA is set to 1; when the count value in CL overflows, the CH [x] pin of the PCA output is reset to 0. When the low byte CL of the counter/timer overflows (from 0xFF to 0x00), the value stored in CCAPxH is automatically loaded into CCAPxL without software intervention.

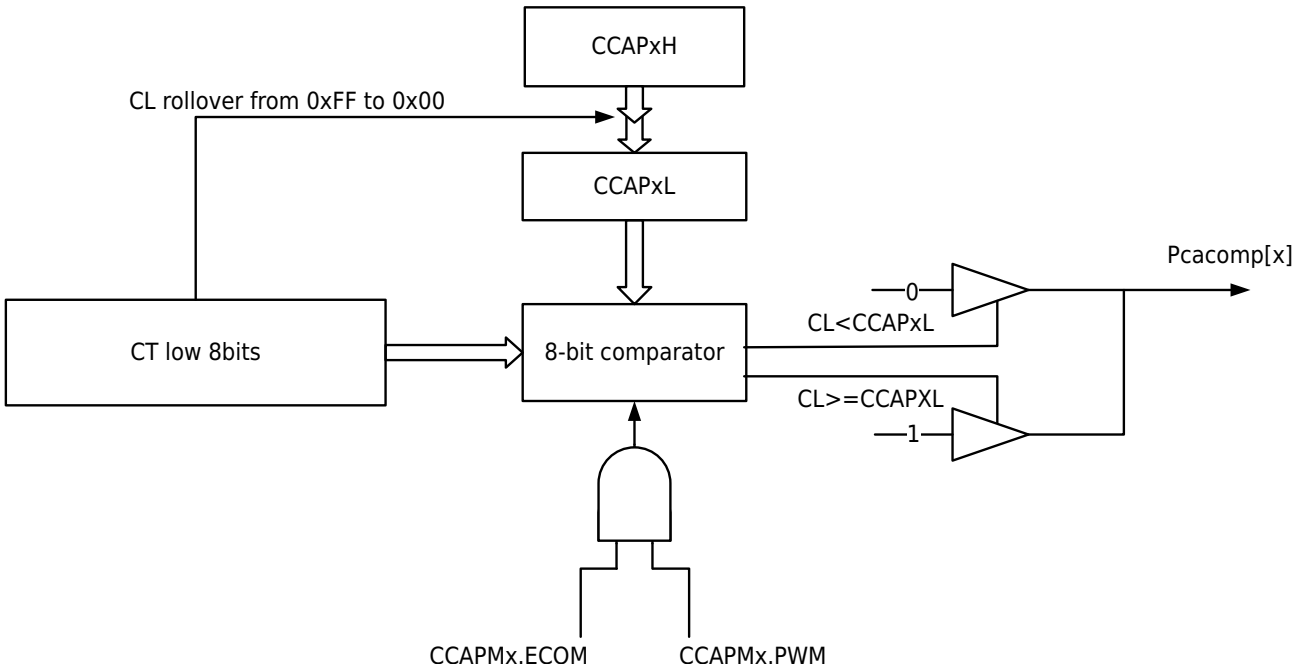

Figure 16-7 PCA PWM Functional Block Diagram

In this mode, the value in the low byte of the PCA timer/counter (CL) is constantly compared with the value in the low byte compare/capture register (CCAPxL). When CL < CCAPxL, the output waveform is low. When both match (CL=CCAPxL), the output waveform goes high until CL overflows from 0xFF to 0x00, and remains high during the end period. On overflow, the value in CCAPxH is automatically loaded into CCAPxL, and a new cycle begins.

The value in CCAPxL determines the duty cycle of the current waveform. The value in CCAPxH determines the duty cycle of the next waveform. Pulse width modulation can be changed by changing the value in CCAPxL. As shown, the 8-bit value in CCAPxL can range from 0 (100 % duty cycle), to 255 (0.4 % duty cycle). To change the CCAPxL value without glitching, write a new value in the high byte register (CCAPxH). When CL rolls over 0xFF to 0x00, this value is automatically loaded into CCAPxL by hardware.

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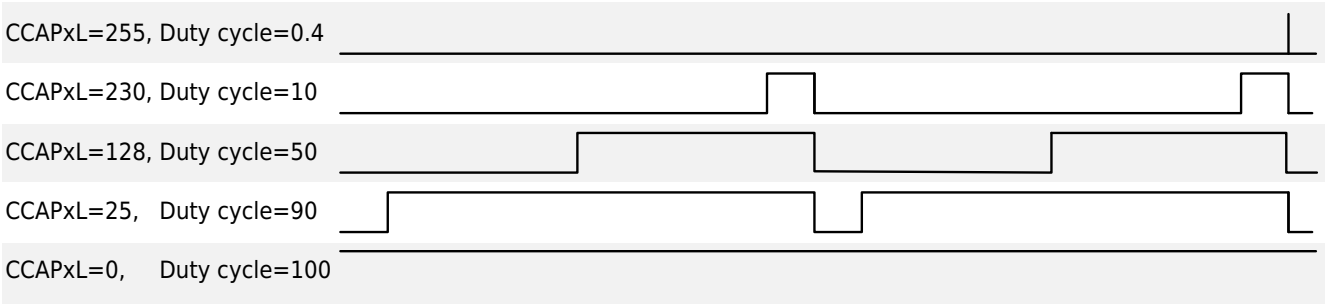

Figure 16-8 PCA PWM Output Waveform

To set a compare/capture module in PWM mode, the CCAPMx.ECOM and CCAPMx.PWM bits need to be set. In addition, the PCA timer/counter can select the input count signal frequency by programming CMOD.CSP[2:0]. Enter an 8-bit value in CCAPxL to specify the duty cycle of the first PWM waveform. Entering an 8-bit value in CCAPxH specifies the duty cycle of the second PWM waveform. Set the timer/counter run control bit (CCON.CR) to start the PCA timer/counter.

Table 16-1 PCA Comparison Capture Function Module Setup

ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	EPWM	Way of Working
×	1	0	0	0	0	×	0	Capture with positive edge trigger
×	0	1	0	0	0	×	0	Trigger capture with negative edge
×	1	1	0	0	0	×	0	Capture with edge trigger
1	0	0	1	0	0	×	0	Software timer
1	0	0	1	1	0	×	0	High speed output
1	0	0	0	0	1	×	0	8-bit pulse width modulator
1	0	0	1	1	0	×	1	16-bit pulse width modulator

16.2.4 Interconnection and Control of PCA Module and Other Modules

When GPIO_PCAS.PCA_ECI=0b000, the PCA_ECI input is taken from the port input selected by Pxy_SEL. When GPIO_PCAS.PCA_ECI=0b001 to 0b111, it is connected to the input or output of other modules.

When GPIO_PCAS.PCA_CH0=0b000, the PCA_CH0 input is taken from the port input selected by Pxy_SEL. When GPIO_PCAS.PCA_CH0=0b001 to 0b111, it is connected to the input or output of other modules.

For more information, see the description of the "Port Auxiliary Function PCA Capture Selection (GPIO_PCAS)" register in the chapter "General-Purpose I/O (GPIO)".

16.3 Operation Example

16.3.1 PCA Timer/Counter Setup Example

Procedure

- **16-bit Free Count Mode**

  Step1. Set the EPMW of PCA_EPWM to 0

  Step2. Set PCA_CMOD.CPS to select the count clock

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Step3. Set PCA_CMOD.CFIE to enable count overflow interrupt as required

Step4. Setup clock PCA_CCON.CR , starts the PCA counter

Step5. Overflow to change the initial value of the counter needs to stop the PCA counter

- **16-bit Reload Count Mode**

Step1. Set the EPMW of PCA_EPWM to 1

Step2. Set PCA_CARR to set the count period value

Step3. Set PCA_CMOD.CPS to select the count clock

Step4. Set PCA_CMOD.CFIE to enable count overflow interrupt as required

Step5. Setup clock PCA_CCON.CR , starts the PCA counter

16.3.2 PCA Capture Function Setup Example

Procedure

Step1. Select the capture trigger form:

- When capturing on an external rising edge is required, the CCAPMx.CAPP=1 and CCAPMx.CAPN=0
- When capturing on an external falling edge is required, the CCAPMx.CAPP=0 and CCAPMx.CAPN=1
- When capture is required on external rising and falling edges, the CCAPMx.CAPP=1 and CCAPMx.CAPN=1

Step2. Configure capture interrupts and interrupt handlers as required.

Note

Captures by the same module override existing captured values. In order to keep the captured value, save it in RAM in the interrupt service routine, this operation must be completed before the next event occurs, otherwise the previous captured sampling value will be lost.

Step3. PCA counter to start according to the timer/counter.

16.3.3 PCA WDT Setup Example

Procedure

Step1. Configure WDT compare/capture register PCA_CCAP4

Step2. Configure the PCA count register PCA_CNT

Step3. Configure PCA_CCAPM4 to select the compare and match function

Step4. Configure PCA_CMOD to select the input clock and enable the WDT function

Step5. Start PCA

Step6. Select to clear PCAWDT before PCAWDT reset occurs.

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16.4 Register Description

16.4.1 Register List

Base address: 0x40001000

Table 16-2 Programmable Counter Array (PCA) Register Offset

Offset	Register	Description	Width
0x000	PCA_CCON	PCA Control Register	32
0x004	PCA_CMOD	PCA Mode Register	32
0x008	PCA_CNT	PCA Count Register	32
0x00C	PCA_ICLR	PCA Interrupt Clear Register	32
0x010	PCA_CCAPM0	PCA Compare/Capture Module 0 Mode Register	32
0x014	PCA_CCAPM1	PCA Compare/Capture Module 1 Mode Register	32
0x018	PCA_CCAPM2	PCA Compare/Capture Module 2 Mode Register	32
0x01C	PCA_CCAPM3	PCA Compare/Capture Module 3 Mode Register	32
0x020	PCA_CCAPM4	PCA Compare/Capture Module 4 Mode Register	32
0x024	PCA_CCAP0H	PCA Compare/Capture Module 0 Data Register High 8 -bit	32
0x028	PCA_CCAP0L	PCA Compare/Capture Module 0 Data Register Low 8 -bit	32
0x02C	PCA_CCAP1H	PCA Compare/Capture Module 1 Data Register High 8 -bit	32
0x030	PCA_CCAP1L	PCA Compare/Capture Module 1 Data Register Low 8 -bit	32
0x034	PCA_CCAP2H	PCA Compare/Capture Module 2 Data Register High 8 -bit	32
0x038	PCA_CCAP2L	PCA Compare/Capture Module 2 Data Register Low 8 -bit	32
0x03C	PCA_CCAP3H	PCA Compare/Capture Module 3 Data Register High 8 -bit	32
0x040	PCA_CCAP3L	PCA Compare/Capture Module 3 Data Register Low 8 -bit	32
0x044	PCA_CCAP4H	PCA Compare/Capture Module 4 Data Register High 8 -bit	32
0x048	PCA_CCAP4L	PCA Compare/Capture Module 4 Data Register Low 8 -bit	32
0x04C	PCA_CCAPO	Compare High Speed Output Flag Register	32

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Offset	Register	Description	Width
0x050	PCA_CCAP0	PCA Compare/Capture Module 0 16 -bit Data Register	32
0x054	PCA_CCAP1	PCA Compare/Capture Module 1 16 -bit Data Register	32
0x058	PCA_CCAP2	PCA Compare/Capture Module 2 16 -bit Data Register	32
0x05C	PCA_CCAP3	PCA Compare/Capture Module 3 16 -bit Data Register	32
0x060	PCA_CCAP4	PCA Compare/Capture Module 4 16 -bit Data Register	32
0x064	PCA_CARR	PCA Period Register	32
0x068	PCA_EPWM	PCA Enhanced PWM Control Register	32

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16.4.2 Control Register (PCA_CCON)

Offset	Bit Position																													
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								CF	CR	Reserved	CCF4	CCF3	CCF2	CCF1	CCF0
Access																									RO	RW		RO	RO	RO	RO	RO

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7	CF	PCA counter overflow flag When the PCA count overflows, CF is set by hardware, if the CFIE bit of the CMOD register is 1, the CF flag can generate an interrupt ● 0b0: No overflow occurred ● 0b1: Generation counter has overflowed	RO
6	CR	PCA counter run control bit ● 0b0: Disable PCA counter counting ● 0b1: Start PCA counter counting	RW
5	*Reserved*	-	-
4	CCF4	PCA counter module 4 compare/capture flag bit This bit is set by hardware when a match or capture occurs. When CCAPM4.CCIE is set, this flag will generate a PCA interrupt	RO
3	CCF3	PCA counter module 3 compare/capture flag bit This bit is set by hardware when a match or capture occurs. When CCAPM3.CCIE is set, this flag will generate a PCA interrupt	RO
2	CCF2	PCA counter module 2 compare/capture flag bit This bit is set by hardware when a match or capture occurs. When CCAPM2.CCIE is set, this flag will generate a PCA interrupt	RO
1	CCF1	PCA counter module 1 compare/capture flag bit This bit is set by hardware when a match or capture occurs. When CCAPM1.CCIE is set, this flag will generate a PCA interrupt	RO
0	CCF0	PCA counter module 0 compare/capture flag bit This bit is set by hardware when a match or capture occurs. When CCAPM1.CCIE is set, this flag will generate a PCA interrupt	RO

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16.4.3 Mode Register (PCA_CMOD)

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								CIDL	WDTE	Reserved		CPS		CFIE	
Access																									RW	RW			RW		RW	

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7	CIDL	Whether PCA stops working in Sleep mode ● 0b0: In Sleep mode, PCA continues to work. ● 0b1: In Sleep mode, PCA stops working.	RW
6	WDTE	PCA WDT function enable control bit ● 0b0: Disable PCA module 4 WDT function ● 0b1: Start PCA module 4 WDT function	RW
5:4	*Reserved*	-	-
3:1	CPS	Clock frequency division selection and clock source selection ● 0b000: PCLK/32 ● 0b001: PCLK/16 ● 0b010: PCLK/8 ● 0b011: PCLK/4 ● 0b100: PCLK/2 ● 0b101: Timer0 overflow ● 0b110: Timer1 overflow ● 0b111: ECI external clock, clock PCLK four-frequency sampling	RW
0	CFIE	PCA counter interrupt enable control signal ● 0b0: Disable ● 0b1: Enable	RW

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16.4.4 Count Register (PCA_CNT)

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																CNT															
Access																	RW															

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
15:0	CNT	The value of the timer counter CNT can only be written in the PCA stop state, otherwise the write is invalid	RW

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16.4.5 Interrupt Clear Register (PCA_ICLR)

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000000FF																															
Name	Reserved																								CF	Reserved		CCF4	CCF3	CCF2	CCF1	CCF0
Access																									WO			WO	WO	WO	WO	WO

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7	CF	PCA counter overflow flag clears Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
6:5	*Reserved*	-	-
4	CCF4	PCA counter module 4 compare/capture flag bit clears Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
3	CCF3	PCA counter module 3 compare/capture flag bit clears Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
2	CCF2	PCA counter module 2 compare/capture flag bit clears Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
1	CCF1	PCA counter module 1 compare/capture flag bit clears Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
0	CCF0	PCA counter module 0 compare/capture flag bit clears Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO

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16.4.6 Compare/Capture Module x Mode Register (PCA_CCAPMx)(x=0-4)

Offset: 0x010 (CCAPM0), 0x014 (CCAPM1), 0x018 (CCAPM2), 0x01C (CCAPM3), 0x020 (CCAPM4)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																									ECOM	CAPP	CAPN	MAT	TOG	PWM	CCIE
Access																										RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:7	*Reserved*	-	-
6	ECOM	Enable comparator function control bit ● 0b0: Disable ● 0b1: Enable **Note** When the PCA is used in software counter, high-speed output, PWM mode, or WDT mode, the ECOM bit must be set to 1. Writing CCAPxH or CCAPx register will set the ECOM bit to 1; writing CCAPxL register will set the ECOM bit to 0	RW
5	CAPP	Positive edge capture control bit ● 0b0: Disable rising edge capture ● 0b1: Enable rising edge capture	RW
4	CAPN	Negative edge capture control bit ● 0b0: Disable falling edge capture ● 0b1: Enable falling edge capture	RW
3	MAT	Allow match control bits ● 0b0: Disable match function ● 0b1: Once the PCA count value matches the value in the module's compare/capture register, the interrupt flag CCFx in the CCON register will be set	RW
2	TOG	Toggle control bit ● 0b0: Disable flip function ● 0b1: Operates in PCA high-speed output mode. Once the PCA counter value matches the value in the module's compare/capture register, the CHx pin will toggle	RW
1	PWM	PWM control bits ● 0b0: Disable PWM pulse width modulation function ● 0b1: Enable the CHx pin as a PWM output **Note** Only when CCAPMx[6:0]=0b1000010 is the PWM function enabled.	RW

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Bit	Name	Functional Description	Access
0	CCIE	PCA enable interrupt ● 0b0: Disable ● 0b1: Enable	RW

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16.4.7 Capture/Compare Module x Data Register High 8-Bit (PCA_CCAPxH)(x = 0-4)

Offset: 0x024 (CCAP0H), 0x02C (CCAP1H), 0x034 (CCAP2H), 0x03C (CCAP3H), 0x044 (CCAP4H)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								CCAPx[15:8]							
Access																									RW							

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7:0	CCAPx[15:8]	Compare/capture mode high 8 -bit register ● When the PCA operates in compare/capture mode, this register stores the high 8 bits of the 16-bit captured counter value. Write CCAPxH register will set CCAPMxregister's ECOM to 1. ● When PCA mode is used in PWM mode, it is used to control the output duty ratio load register. When the low 8 bits of the counter overflow, the load register will be automatically updated to the PWM comparison register.	RW

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16.4.8 Compare/Capture Module x Data Register Low 8-Bit (PCA_CCAPxL)(x=0-4)

Offset: 0x028 (CCAP0L), 0x030 (CCAP1L), 0x038 (CCAP2L), 0x040 (CCAP3L), 0x048 (CCAP4L)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								CCAPx[7:0]							
Access																									RW							

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7:0	CCAPx[7:0]	Compare/capture mode lower 8 -bit register ● Used to store the lower 8 bits of the 16-bit captured counter value when the PCA operates in compare/capture mode. Write CCAPxL register will set CCAPMx register's EOM to 0. ● When the PCA operates in PWM mode, this register is used as the compare register to control the output duty cycle. The PWM output is low when the lower 8 bits of the counter are less than the value of CCAPx[7:0]; otherwise, the PWM output is high.	RW

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16.4.9 Compare/Capture Module x 16-Bit Data Register (PCA_CCAPx)(x=0-4)

Offset: 0x050 (CCAP0), 0x054 (CCAP1), 0x058 (CCAP2), 0x05C (CCAP3), 0x060 (CCAP4)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																CCAPx															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	CCAPx	Compare/capture mode 16-bit register ● When the PCA mode is used for compare/capture, this register holds the 16-bit captured count value. Writing to the CCAPx register will set the ECOM bit to 1 in the CCAPMx register. **Note** In compare/capture mode, this register can be directly read and written, equivalent to writing to the CCAPxH and CCAPxL registers. ● When the PCA is configured in PWM mode, this register is not used; instead, the CCAPxH and CCAPxL registers are used.	RW

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16.4.10 Compare High Speed Output Flag Register (PCA_CCAPO)

Offset	Bit Position																															
0x04C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																											CCAPO4	CCAPO3	CCAPO2	CCAPO1	CCAPO0
Access																												RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:5	*Reserved*	-	-
4	CCAPO4	Compare the output value of module 4	RW
3	CCAPO3	Compare the output value of module 3	RW
2	CCAPO2	Compare the output value of module 2	RW
1	CCAPO1	Compare the output value of module 1	RW
0	CCAPO0	Compare the output value of module 0	RW

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16.4.11 Period Register (PCA_CARR)

Offset	Bit Position																													
0x064	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000FFFF																															
Name	Reserved																CARR															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	CARR	Count cycle reload register	RW

16.4.12 Enhanced PWM Control Register (PCA_EPWM)

Offset	Bit Position																													
0x068	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																															EPWM
Access																																RW

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-
0	EPWM	16-bit PWM enable	RW

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17 TIM4/5/6

17.1 Introduction

The Advanced Timer includes three timers: Tmer4/5/6. Timer4/5/6 are high-performance timers with identical functions, capable of counting to generate various clock waveforms. A single timer can produce either a complementary pair of PWM outputs or two independent PWM outputs, and can capture external inputs for pulse width or period measurement.

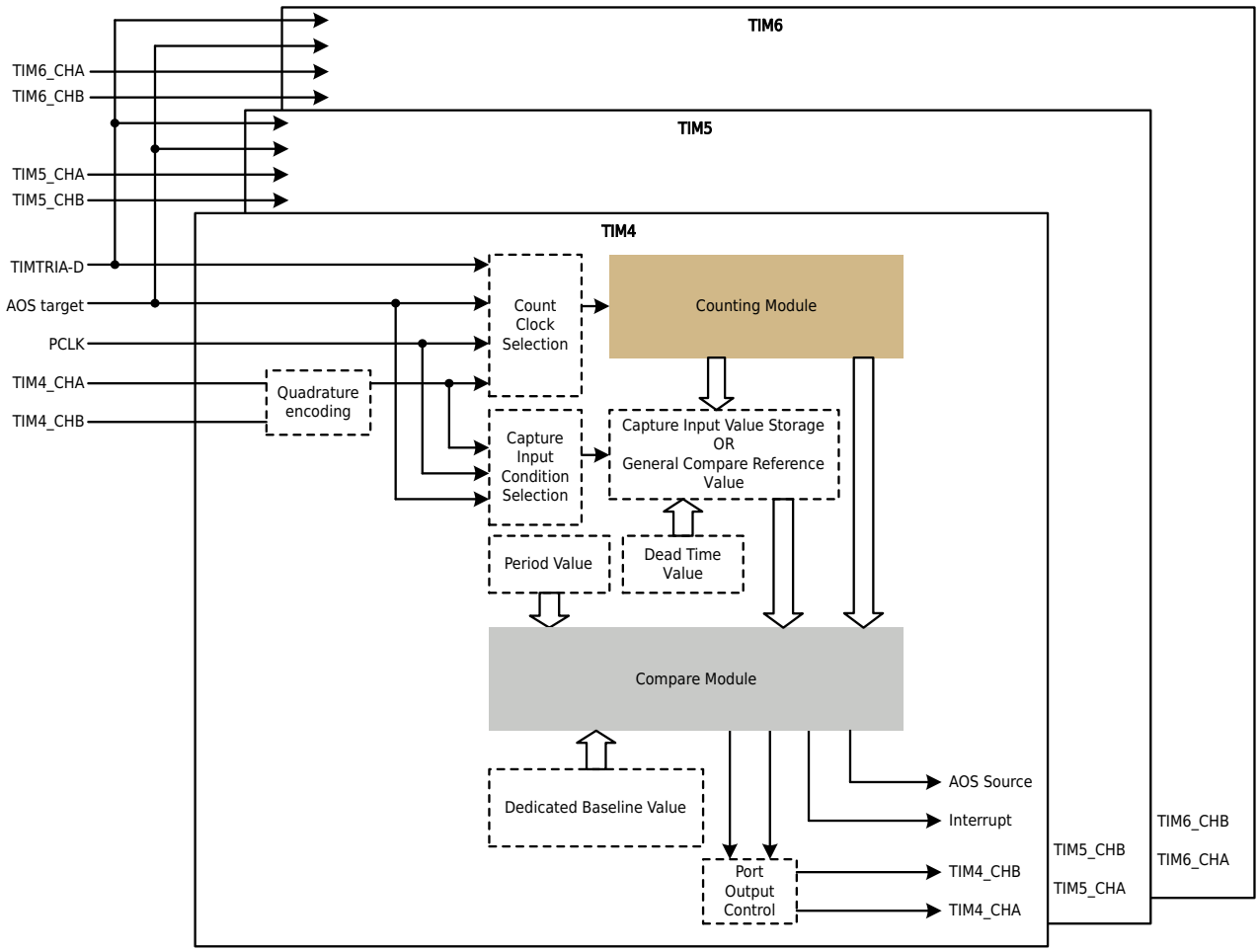

Figure 17-1 Advanced Timer Block Diagram

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17.2 Features

Table 17-1 Advanced Timer Basic Features

Basic Features	Description
Waveform mode	Sawtooth wave, triangle wave
Basic function	Up/down counting direction
	Software synchronization
	Hardware Synchronization
	Cache function
	Capture input
	Pulse width/period measurement
	External input counting
	Quadrature encoding count
	General PWM output
	Dead-time control
	Protection mechanism
	AOS associated action
Interrupt type	Count comparison match interrupt
	Count period match interrupt
	Dead-time error interrupt
	Same high same low interrupt

Table 17-2 Advanced Timer Port List

Port Name	Direction	Function
TIMx_CHA	Input/output	Quadrature encoding count clock input port or capture input port or compare output port (x=4-6) Hardware start, stop, clear condition input port
TIMx_CHB		
TIMTRIA	Input	Hardware count clock input port or capture input port Hardware start, stop, clear condition input port
TIMTRIB		
TIMTRIC		
TIMTRID		

17.3 Functional Description

17.3.1 Basic Actions

Basic Waveform Mode

Timer4/5/6 have two basic counting waveform modes: sawtooth mode and triangular wave mode. The triangular wave mode is further subdivided based on different internal counting behaviors, categorized into triangular wave A mode and triangular wave B mode. The basic waveforms for sawtooth and

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triangular waves are shown in the figure below. The difference between triangular wave A mode and triangular wave B mode lies in the buffer transfer timing. Triangular wave A mode performs buffer transfer only once per cycle (at the valley point), whereas triangular wave B mode performs buffer transfer twice per cycle (at both the peak and valley points).

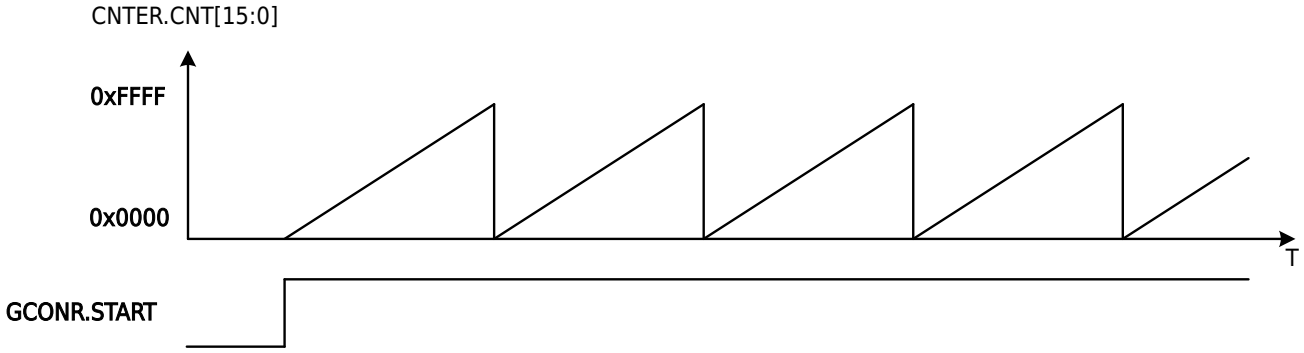

Figure 17-2 Advanced Timer Sawtooth Waveform (Up-Counting)

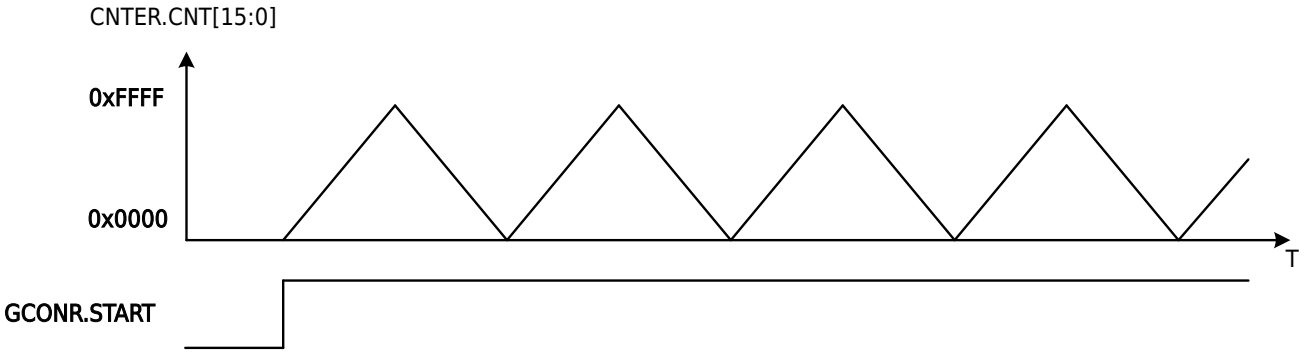

Figure 17-3 Advanced Timer Triangular Waveform

Comparison Output

Timer4/5/6 has two compare output channels (CHA, CHB) per timer, which can output specified levels when the counter matches the compare reference values. The GCMAR and GCMBR registers define the compare reference values for CHA and CHB, respectively. When the counter value matches GCMAR, the CHA output is set to the specified level. When the counter value matches GCMBR, the CHB output is set to the specified level.

The initial level, stop level, and compare-match output level for CHA and CHB are configured via the Port Control Register (PCONR) bits: PCONR.STACA, PCONR.STPCA, PCONR.STASTPSA, PCONR.CMPCA[1:0], PCONR.PERCA[1:0] and PCONR.STACB, PCONR.STPCB, PCONR.STASTPSB, PCONR.CMPCB[1:0], PCONR.PERCB[1:0].

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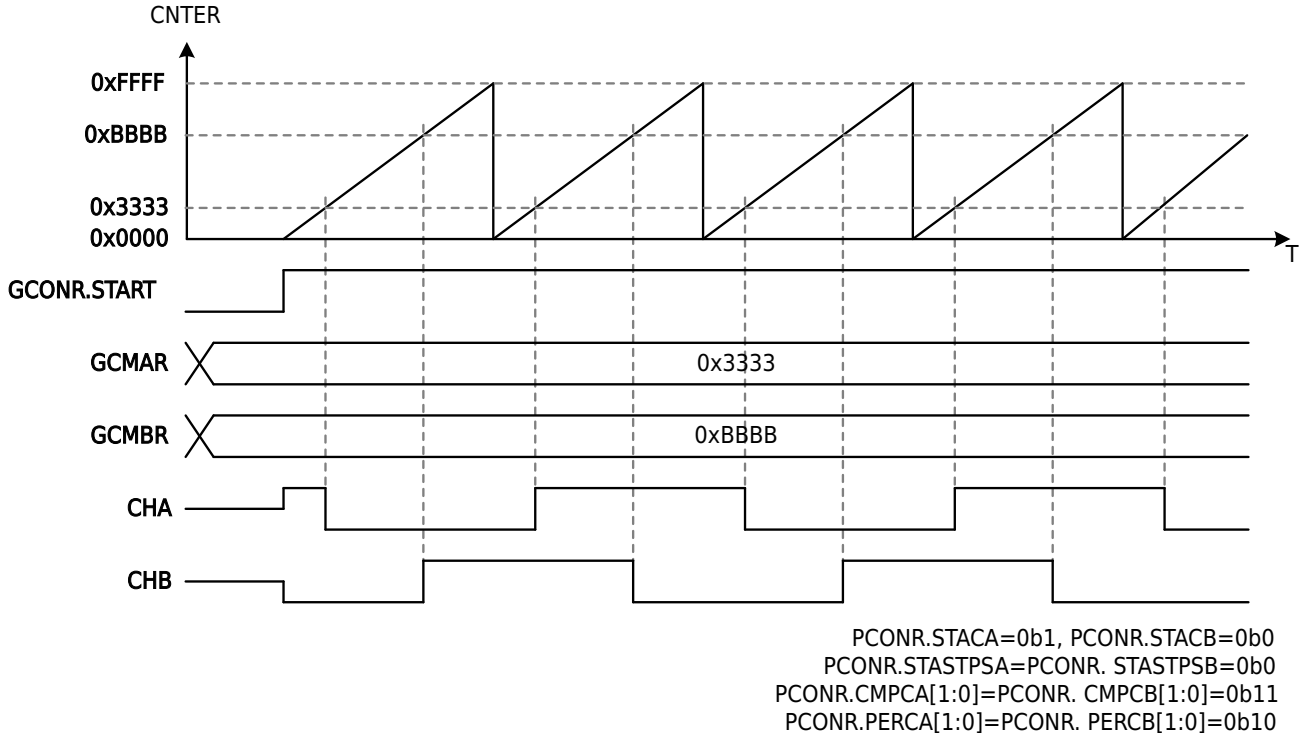

Figure 17-4 Advanced Timer Compare Output Action

Capture Input

Timer4/5/6 feature capture input function, with each timer equipped with two capture input registers (GCMAR, GCMBR) to store captured counter values. Setting the PCONR.CAPCA and PCONR.CAPCB bits of the Port Control Register (PCONR) to 1 enables the capture input function. When the corresponding capture input condition is configured and triggered, the current counter value is saved to the respective register (GCMAR or GCMBR).

The capture input conditions for each group can be triggered by: AOS events, TIMTRIA-TIMTRID inputs, CHA or CHB inputs. The specific trigger conditions can be selected through the Hardware Capture Event Selection Registers (HCPAR, HCPBR).

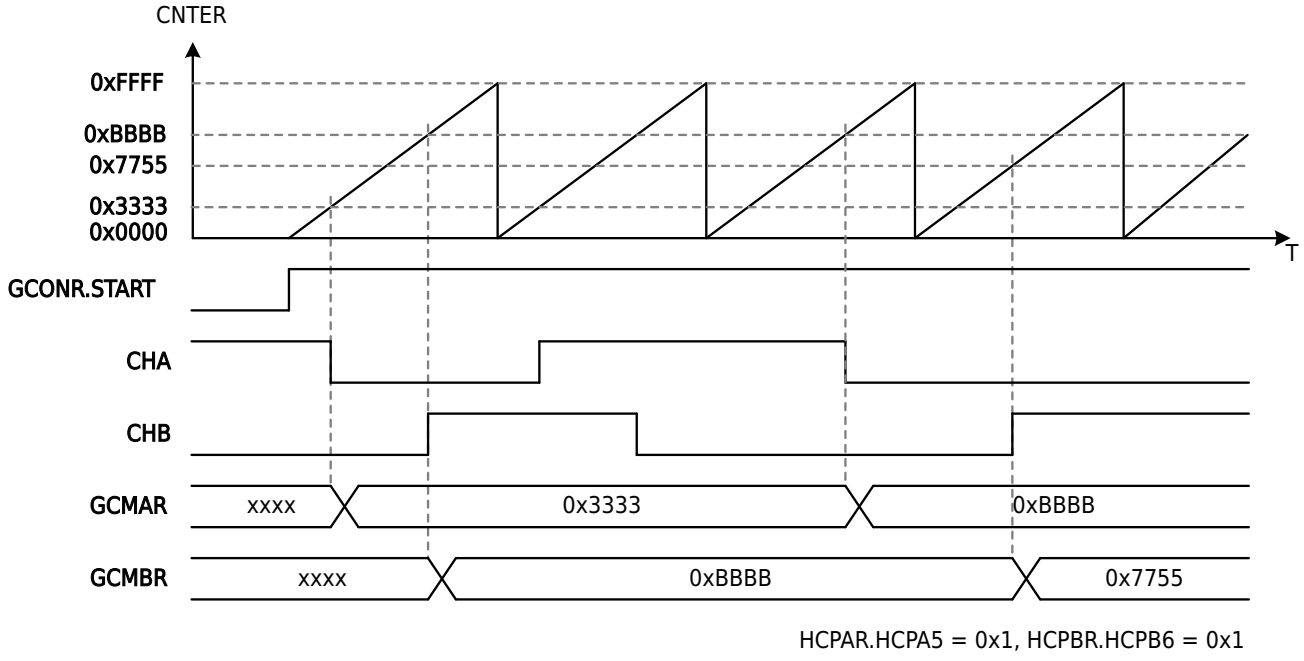

Figure 17-5 Advanced Timer Capture Input Action

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17.3.2 Clock Source Selection

Timer4/5/6 can select their counting clock from the following sources:

1. PCLK and its 2/4/8/16/64/256/1024 divisions (configured by GCONR.CKDIV[2:0])
2. AOS event trigger input (configured by HCUPR.HCUP[19:16] or HCDOR.HCDO[19:16])
3. Quadrature encoder input from CHA/CHB (configured by HCUPR.HCUP[7:0] or HCDOR.HCDO[7:0])
4. Port input from TIMTRIA-TIMTRID (configured by HCUPR.HCUP[15:8] or HCDOR.HCDO[15:8])

As described above, clock sources 2/3/4 operate independently, each can be individually enabled or disabled. When any of sources 2/3/4 is selected, source 1 is automatically disabled.

17.3.3 Count Direction

The counting direction of Timer4/5/6 can be changed via software. The method of changing the counting direction may vary slightly depending on the selected waveform mode.

Sawtooth Count Direction

The method for changing the counting direction varies slightly depending on the sawtooth wave mode.

During incremental counting, if GCONR.DIR=0 (decremental counting) is set, the counter will switch to decremental counting mode after counting up to overflow. During decremental counting, if GCONR.DIR=1 (incremental counting) is set, the counter will switch to incremental counting mode after counting down to underflow.

When counting is stopped, the GCONR.DIR bit is set. GCONR.DIR will not be reflected in the counting until the counting starts until overflow or underflow.

Triangular Wave Count Direction

In triangle wave mode, the counting direction can only be set when the counter is stopped. It is invalid to set the counting direction in counting.

When counting is stopped, the GCONR.DIR bit is set. GCONR.DIR will not be reflected in the counting until the counting starts until overflow or underflow.

17.3.4 Digital Filtering

Timer4/5/6's CHA, CHB, and TIMTRIA-D port inputs all feature digital filtering function. The filtering function for corresponding ports can be enabled by setting the relevant enable bits in the Filter Control Register (FCONR). The reference clock for filtering is also configured via the Filter Control Register (FCONR).

When the port level sampled by the Filter Sampling Reference Clock remains consistent for 3 consecutive times, that level is transmitted as a valid signal to the internal block. Levels with fewer than 3 consistent samples are filtered as external noise and not transmitted to the internal block. An example of this filtering behavior is shown in the figure below.

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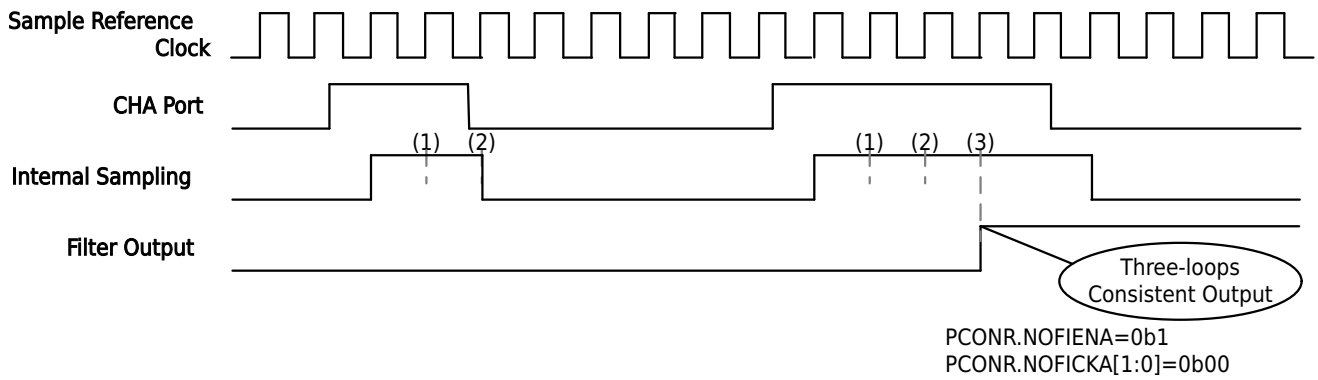

Figure 17-6 Digital Filtering Function of Capture Input Ports

The TIMTRIA-D ports are a shared port group among Timer4/5/6. The digital filtering function for this port group is implemented only in Timer4. The digital filtering configuration for these ports is ineffective in other timers (Timer5/6).

17.3.5 Software Synchronization

Software Synchronous Start

Timer4/5/6 can achieve synchronous startup of target timers by setting the relevant bits in the Software Synchronization Start Register (SSTAR).

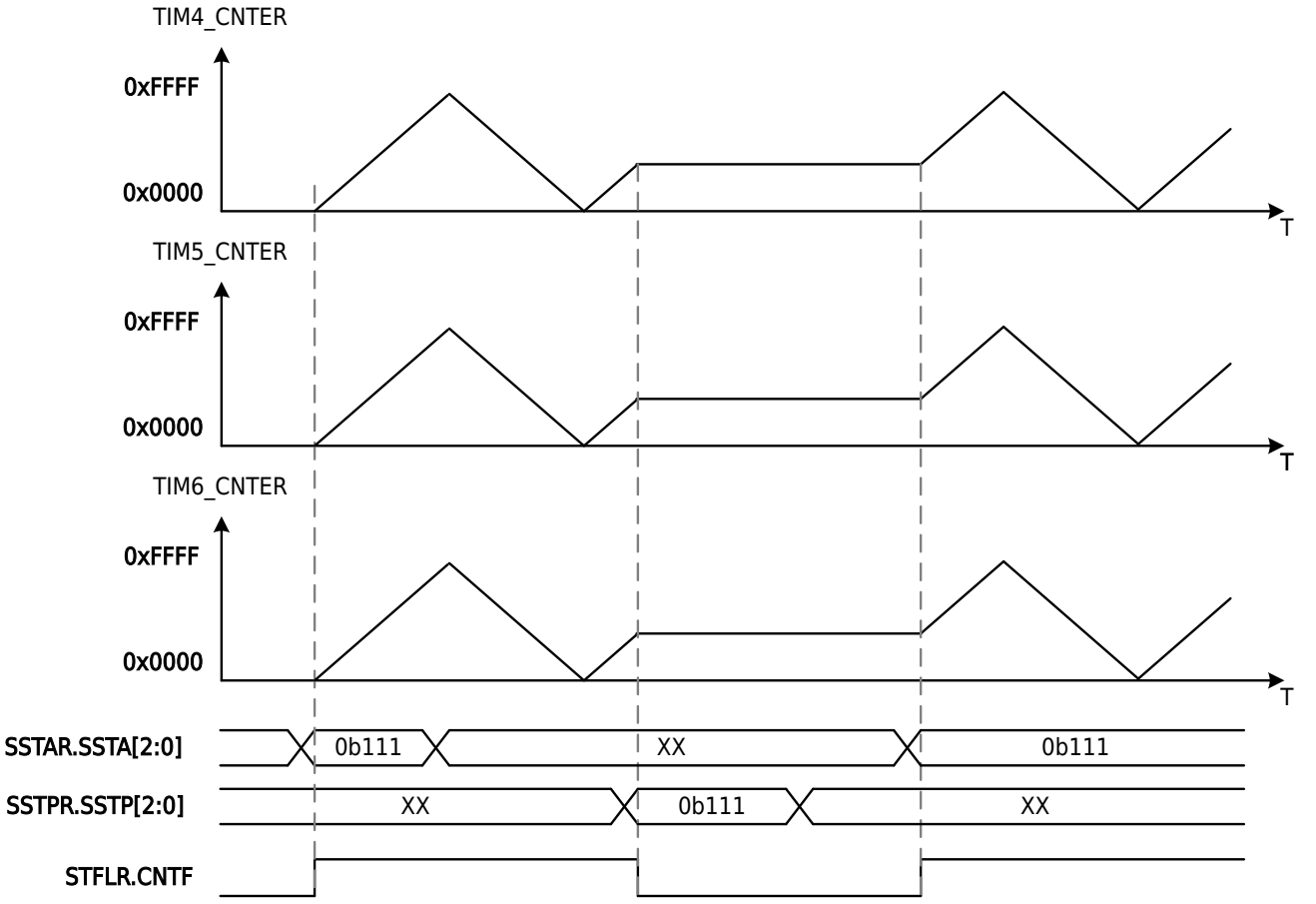

Figure 17-7 Software Synchronization Action

Software Synchronous Stop

Timer4/5/6 can achieve synchronous stopping of target timers by setting the relevant bits in the Software Synchronization Stop Register (SSTPR).

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Software Synchronous Clear

Timer4/5/6 can achieve synchronous clearing of target timers by setting the relevant bits in the Software Synchronization Clear Register (SCLRR).

As shown in the Figure 17-7 : Software Synchronization Action, setting Timer4's SSTAR[2:0]=0b111 enables software synchronous startup of Timer4/5/6.

The software synchronization operation registers (SSTAR, SSTPR, SCLRR) are a set of shared registers independent of Timer4/5/6 and common across all TIM modules. Each bit in these registers is valid only when written as 1, while writing 0 has no effect. When reading the SSTAR register, the counter status of each timer is retrieved. Reading SSTPR or SCLRR returns 0.

17.3.6 Hardware Synchronization

Each timer not only has two dedicated general-purpose input ports (CHA, CHB), but also shares four external general-purpose input ports (TIMTRIA, TIMTRIB, TIMTRIC, TIMTRID) and four AOS targets, enabling hardware synchronization between timers.

Hardware Synchronous Start

Timer4/5/6 can all be configured to start their counters via hardware. Timers sharing the same hardware start condition will synchronously start when the trigger condition is met. The specific hardware start condition is determined by the settings in the Hardware Start Event Selection Register (HSTAR).

Hardware Synchronous Stop

Timer4/5/6 can all be configured to stop their counters via hardware. Timers sharing the same hardware stop condition will synchronously stop when the trigger condition is met. The specific hardware stop condition is determined by the settings in the Hardware Stop Event Selection Register (HSTPR).

Hardware Synchronous Clear

Timer4/5/6 can all be configured to clear their counters via hardware. Timers sharing the same hardware clear condition will synchronously clear when the trigger condition is met. The specific hardware clear condition is determined by the settings in the Hardware Clear Event Selection Register (HCLRR).

Hardware Synchronous Capture Input

Timer4/5/6 can all be configured to perform capture input operations via hardware. Timers sharing the same capture input condition will synchronously trigger capture input when the condition is met. The specific hardware capture input condition is determined by the settings in the Hardware Capture Event Selection Registers (HCPAR, HCPBR).

Hardware Synchronous Count

Timer4/5/6 can all be configured to use hardware inputs as CLOCK for counting. Timers sharing the same hardware counting condition will synchronously count when the hardware counting CLOCK is active. The specific hardware counting conditions are determined by the settings of the Hardware Increment Event Selection Register (HCUPR) and Hardware Decrement Event Selection Register (HCDOR).

When the hardware synchronous counting function is selected, only the external input clock source is chosen, without affecting the counter's start, stop, or clear operations. The start, stop, and clear operations of the counter still require separate configuration.

The hardware synchronization behavior of Timer4/5/6 is illustrated in the figure below.

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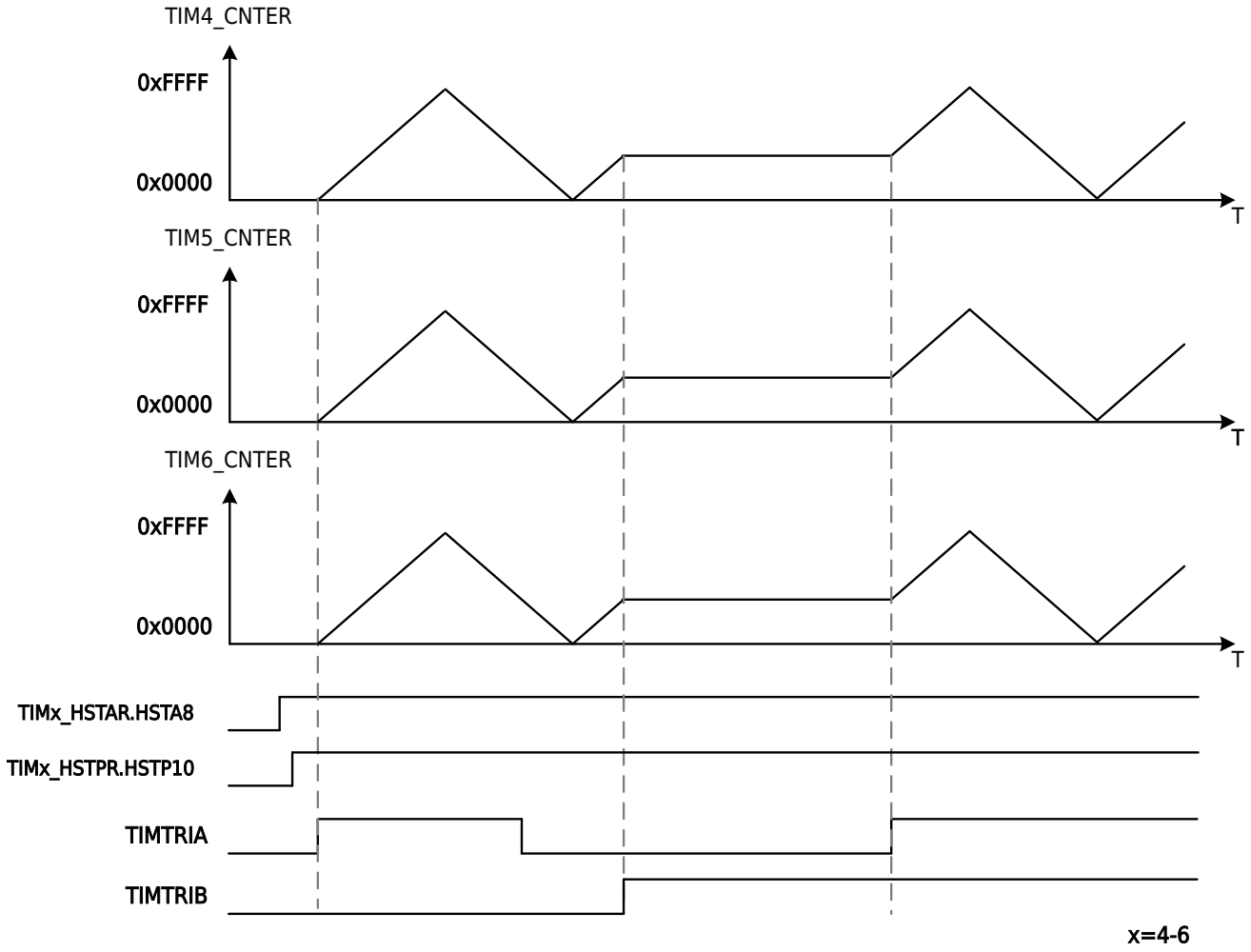

Figure 17-8 Hardware Synchronized Action

17.3.7 Buffer Function

The buffer operation refers to configuring the Buffer Control Register (BCONR) to select the following events at the buffer transfer timing:

1. The value of the General Period Buffer Register (PERBR) is automatically transferred to the General Period Reference Value Register (PERAR);
2. The values of the General Comparison Reference Value Registers (GCMCR, GCMDR) are automatically transferred to the General Comparison Reference Value Registers (GCMAR, GCMBR) (during compare output);
3. The values of the General Comparison Reference Value Registers (GCMAR, GCMBR) are automatically transferred to the General Comparison Reference Value Registers (GCMCR, GCMDR) (during capture input).

The figure below shows the timing diagram of the single-buffer mode for the General Comparison Reference Value Registers and the General Period Reference Value Register during compare output operation. As seen in the figure, modifying the value of the General Comparison Reference Value Register (GCMAR) during counting can adjust the output duty cycle, while changing the value of the General Period Reference Value Register (PERAR) can adjust the output period.

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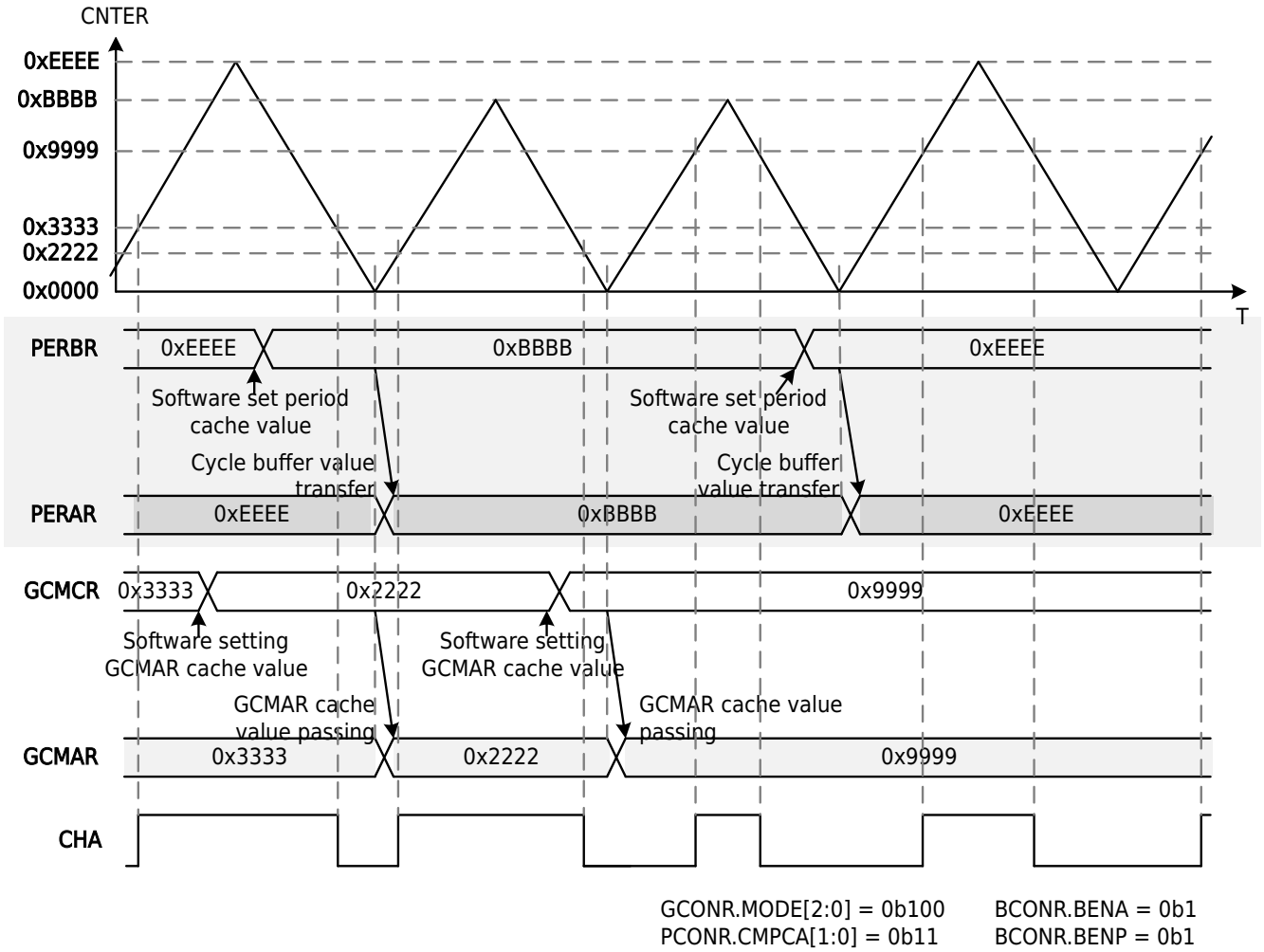

Figure 17-9 Timing Diagram of Compare Output in Single Buffer Mode

Cache Transfer Time Point

- **General Period Base Cache Transfer Time Point**

  The periodic reference value buffer transfer time points are at the up-count overflow point or down-count underflow point for sawtooth waves, and at the count valley point for triangular waves.

- **General Comparison Reference Value Cache Transfer Time Point**

  In sawtooth wave mode, set BCONR.BENA = 0b1 or BCONR.BNEB=0b1 to enable buffer operation. Buffer transfer occurs at the overflow point and underflow point.

  In triangular wave A mode, set BCONR.BENA = 0b1 or BCONR.BNEB=0b1 to enable buffer operation. Buffer transfers occur at the count valley points.

  In triangular wave B mode, set BCONR.BENA = 0b1 or BCONR.BNEB=0b1 to enable buffer operation. Buffer transfer occurs at the count valley point and count peak point.

- **Capture Input Value Buffer Transfer Time Point**

  The buffer transfer time point for capture input action occurs when the capture input is triggered.

Buffer Transfer Upon Clear Operation

In sawtooth wave counting mode or hardware counting mode, if a clear operation occurs during normal comparison output operation, both the general period reference value and general comparison reference value will perform one buffer transfer according to their respective buffer operation configuration settings.

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17.3.8 General PWM Output

PWM Spread Spectrum Output

To reduce external interference from PWM output, spread spectrum configuration is implemented at the PWM output stage. The phase of PWM output is slightly adjusted every PWM cycle.

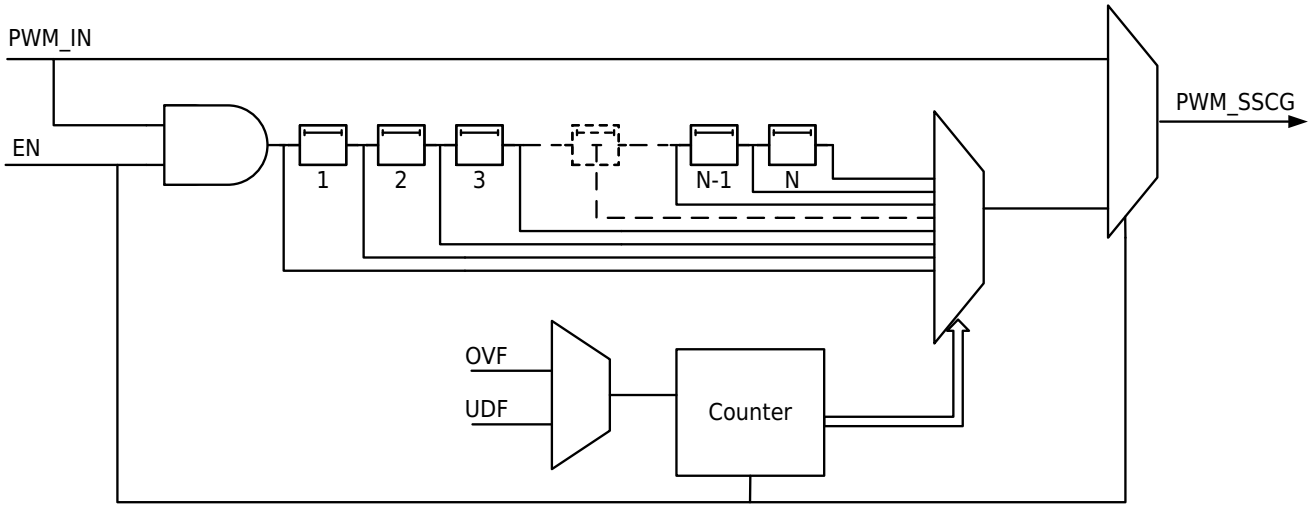

Figure 17-10 PWM Spread Spectrum Output Diagram

Independent PWM Output

Each timer's two channels (CHA and CHB) can independently output PWM waveforms. As shown below, Timer6 CHA channel outputs the PWM waveform.

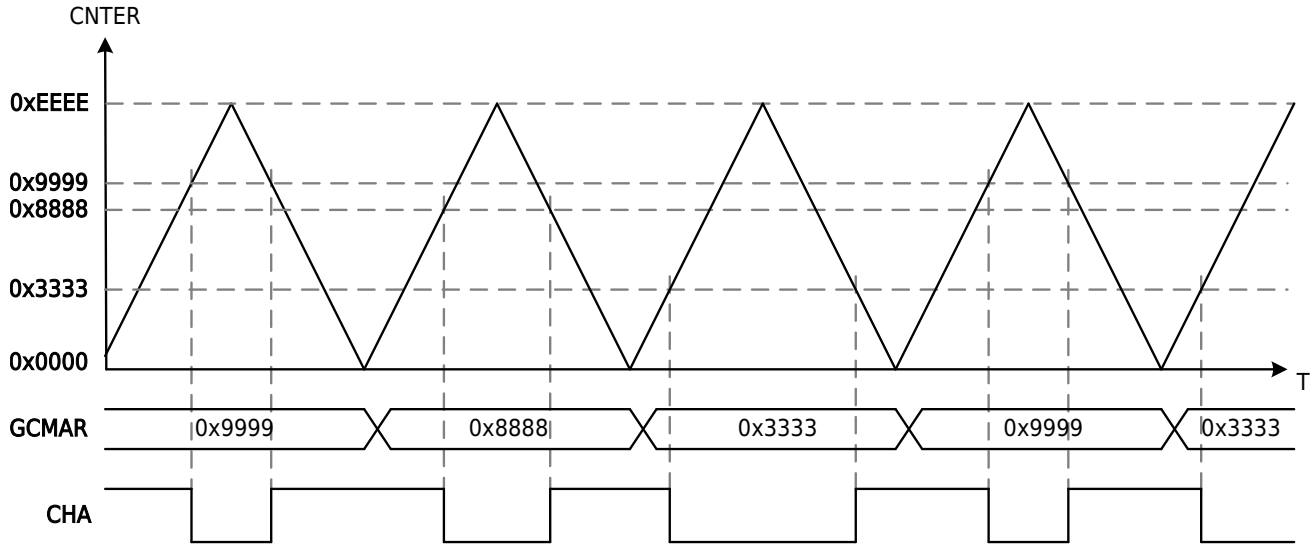

Figure 17-11 CHA Outputs PWM Wave

Complementary PWM Output

The CHA and CHB channels can be configured to output complementary PWM waveforms in different operating modes.

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- **Software-Configured GCMBR Complementary PWM Output**

  In sawtooth wave mode, triangular wave A mode, and triangular wave B mode, the General Comparison Reference Value Registers (GCMBR) for CHB channel waveform output is directly set by software. Its value is independent of the General Comparison Reference Value Registers (GCMAR) value.

  The figure below shows an example of software-configured GCMBR complementary PWM waves output.

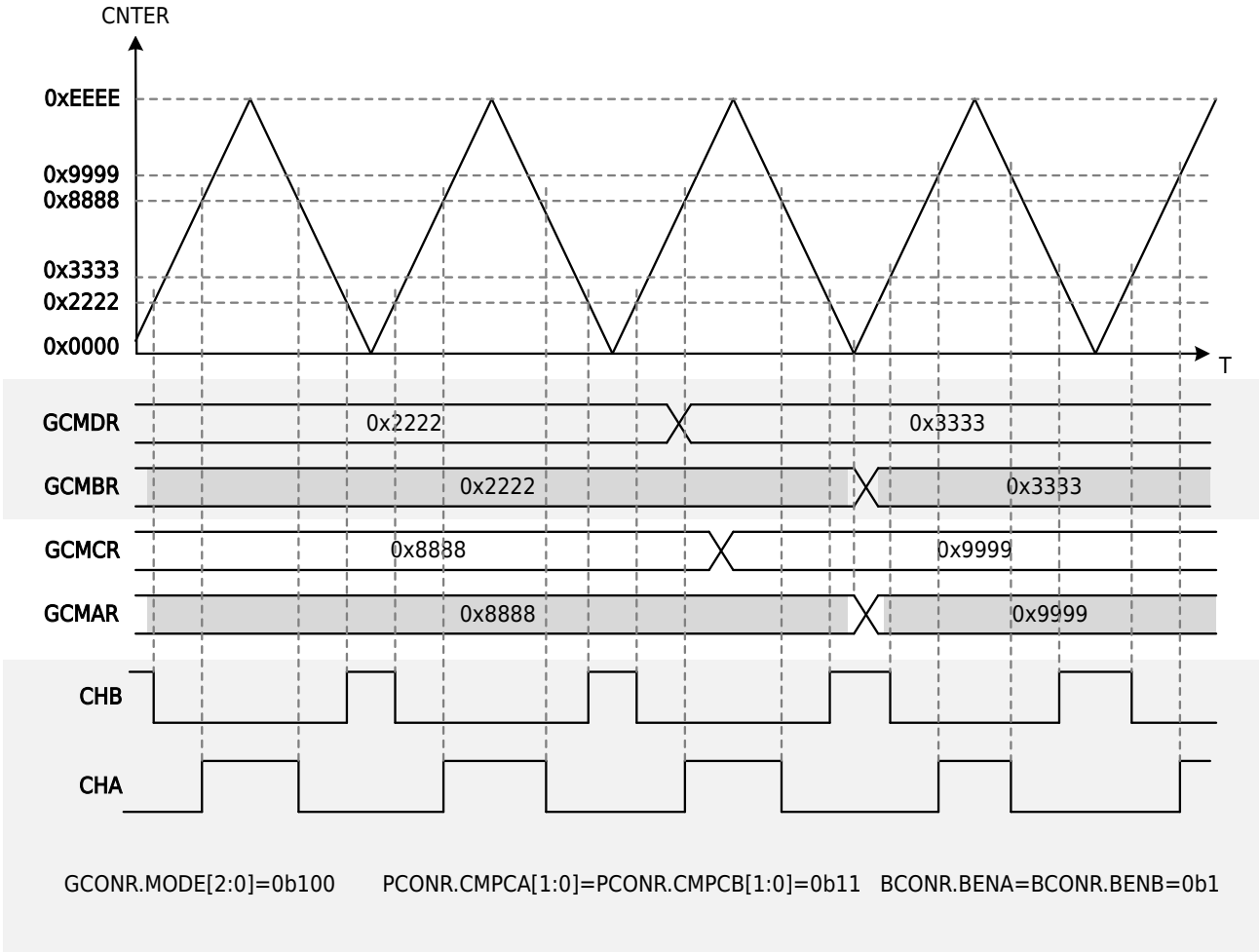

Figure 17-12 In Triangle Wave Mode A, the Software Configures GCMBR Complementary PWM Waves Output

- **Hardware-Set GCMBR Complementary PWM Output**

  Hardware-configured GCMBR complementary PWM output refers to the value of the General Comparison Reference Value Registers (GCMBR) for CHB port waveform output in triangle wave mode A and triangle wave mode B, which is determined by the values of the General Comparison Reference Value Registers (GCMAR) and Dead Time Reference Value Registers (DTUAR, DTDAR) through calculation.

  The following figure shows an example of hardware-configured GCMBR complementary PWM waves output.

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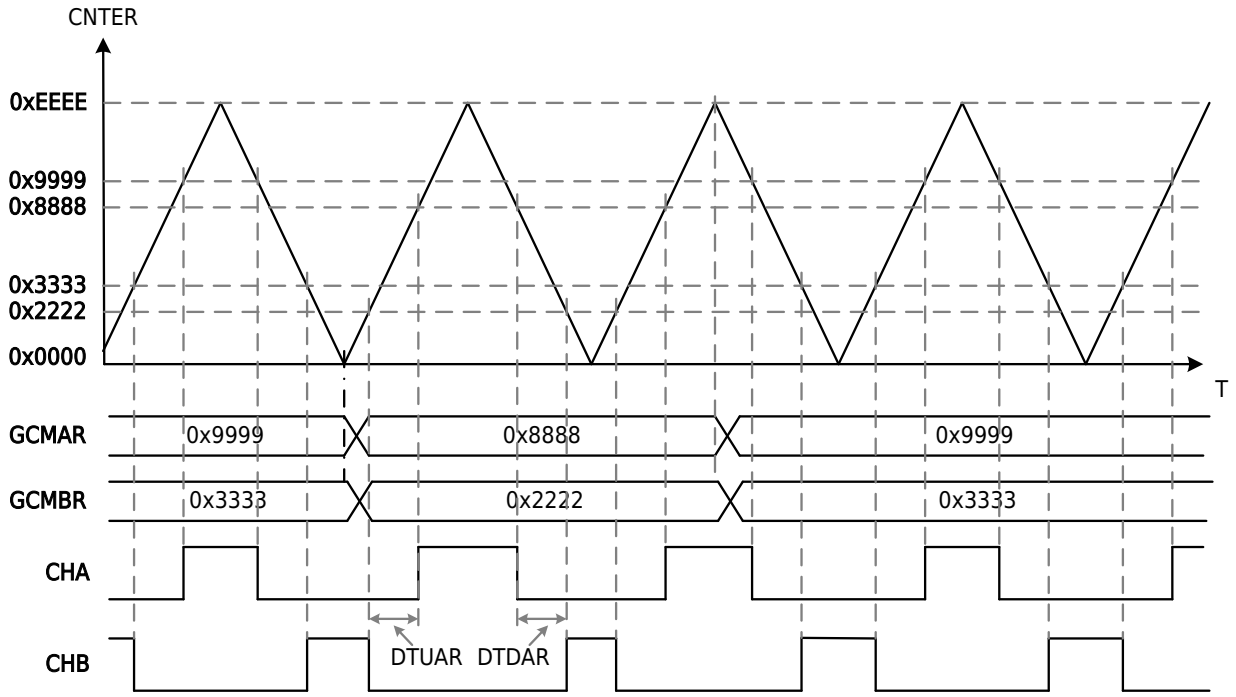

In up counting mode: GCMBR = GCMAR – DTUAR
In down counting mode: GCMBR = GCMAR – DTDAR
GCONR.MODE[2:0]=0b101 PCONR.CMPCA[1:0]=PCONR. CMPCB[1:0]=0b11 DCONR.DTCEN = 0b1
DCONR.SPEA = 0b1
DTUAR=DTDAR = 0x6666

Figure 17-13 Hardware-Configured GCMBR Complementary PWM Waves Output (Symmetric Dead Time) in Triangle Wave Mode B

Multiphase PWM Output

Each timer's CHA and CHB ports can output two independent PWM waves or a set of complementary PWM waves. By combining multiple timers and coordinating software and hardware synchronization, multiphase PWM waves output can be achieved.

As shown in the figure below, Timer4, Timer5, and Timer6 are combined to output 6-phase PWM waves.

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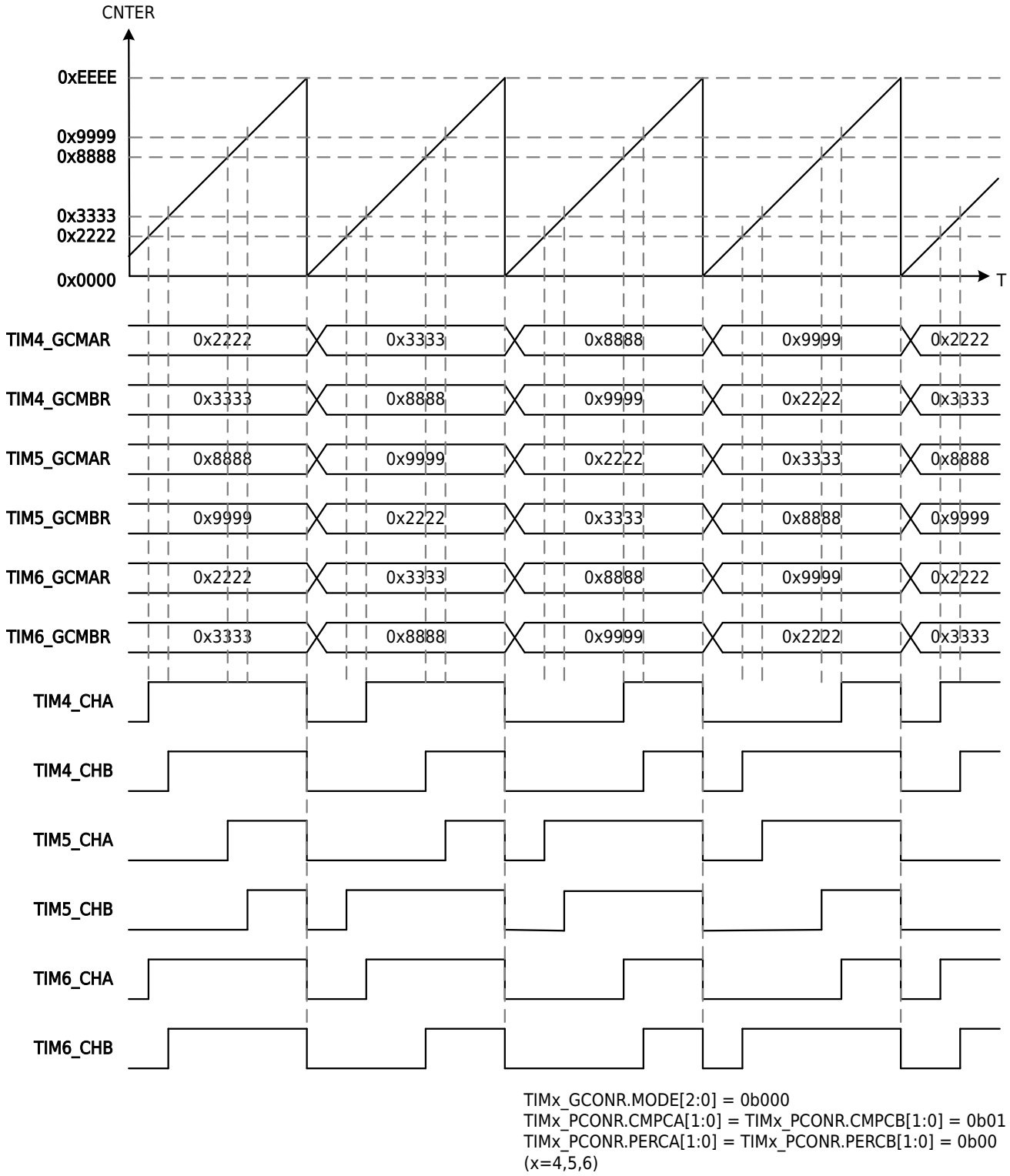

Figure 17-14 6-Phase PWM Waves

As shown in the figure below, Timer4, Timer5, and Timer6 are combined to output 3-phase complementary PWM waves.

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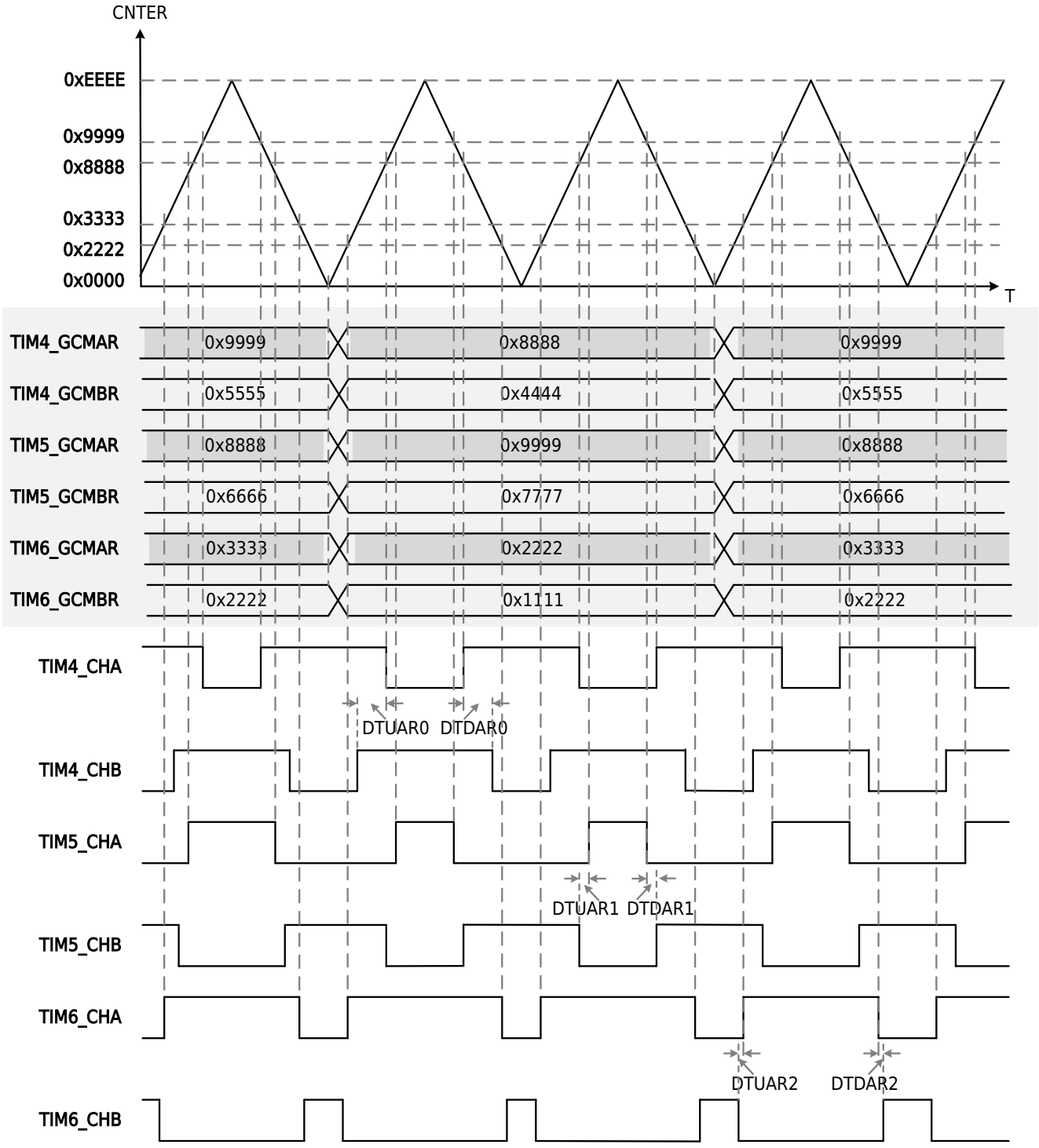

In up counting mode: GCMBR = GCMAR – DTUAR
In down counting mode: GCMBR = GCMAR – DTDAR

TIMx_GCONR.MODE[2:0]=0b100 (x=4,5,6)	TIMx_PCONR.CMPCA[1:0]=0b11 TIMx_PCONR.CMPCB[1:0]=0b11 (x=4,5,6)	TIMx_DCONR.DTCEN=0b1 TIMx_DCONR.SPEA=0b1 TIM4_DTUAR=TIM4_DTDAR=0x4444 TIM5_DTUAR=TIM5_DTDAR=0x2222 TIM6_DTUAR=TIM6_DTDAR=0x1111 (x=4,5,6)

Figure 17-15 In Triangle Wave Mode A, 3-Phase Complementary PWM Waves Output with Dead Time is Generated

17.3.9 Quadrature Encoding Count

By treating CHA input as AIN input, CHB input as BIN input, and any input in TIMTRIA-D as ZIN input, the Advanced Timer can achieve quadrature encoding counting with three input channels.

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A single timer's AIN and BIN can operate independently to implement position counting mode. By combining AIN, BIN, and ZIN from two timers, revolution counting mode can be achieved—one timer for position counting and another for revolution counting.

In revolution counting mode, every combination of two timers (combination of timers 4 and 5, timer 4 as a position counting unit, timer 5 as a revolution counting unit) realizes position counting and revolution counting respectively.

The counting conditions for AIN and BIN are configured by setting the quadrature relationship of CHA and CHB in the hardware increment event selection register (HCUPR) and hardware decrement event selection register (HCDOR). The ZIN input action clears the position counter of the position counting unit by setting the hardware clear event selection register (HCELR), while incrementing the revolution counter of the revolution counting unit is achieved by configuring the hardware increment event selection register (HCUPR).

17.3.9.1 Position Counting Mode

Quadrature encoder position mode refers to implementing basic counting functions, phase difference counting functions, and direction counting functions based on the inputs of AIN and BIN.

Basic Counting

By configuring the HCUPR and HCDOR registers, various phase-difference counting methods can be flexibly implemented.

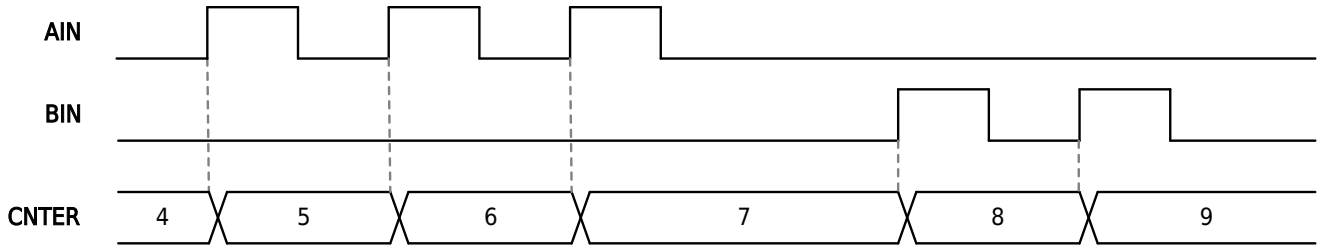
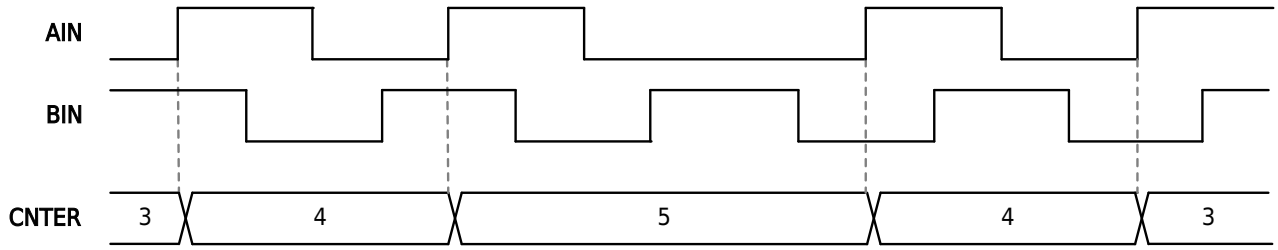


Figure 17-16 Basic Counting Operation in Position Mode

Phase Difference Counting

Phase difference counting operates based on the phase relationship between AIN and BIN. Depending on the configuration, the system can perform 1x counting, 2x counting, or 4x counting.



HCUPR.HCUP6=0b1 && HCDOR.HCDO4=0b1

Figure 17-17 Phase Difference Counting Operation Setting in Position Mode (One Time)

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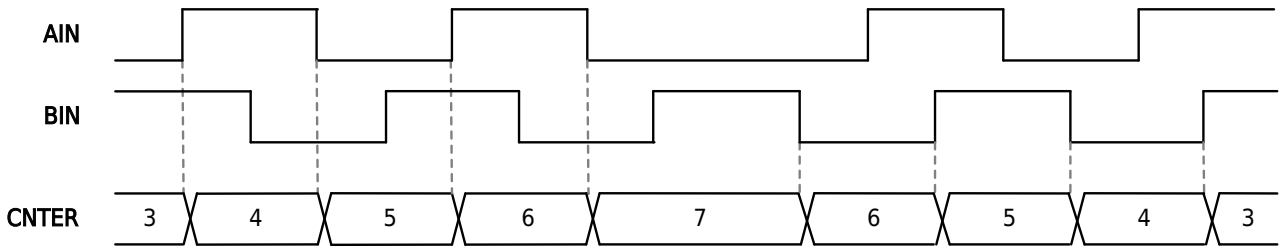
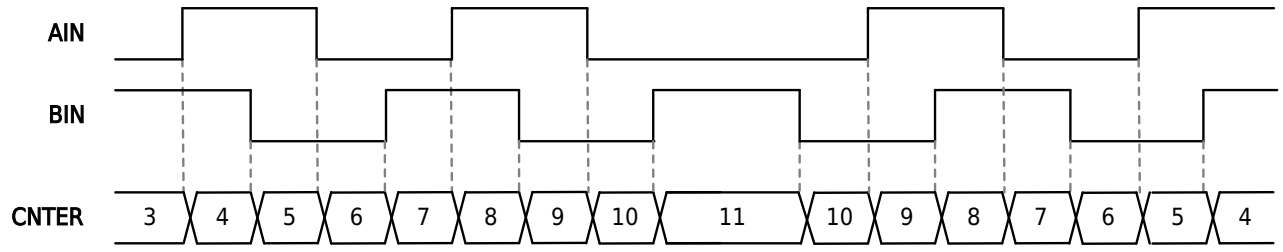


HCUPR.HCUP6=HCUPR.HCUP5=0b1 && HCDOR.HCDO2=HCDOR.HCDO1=0b1

Figure 17-18 Phase Difference Counting Operation Setting in Position Mode (Two Times)

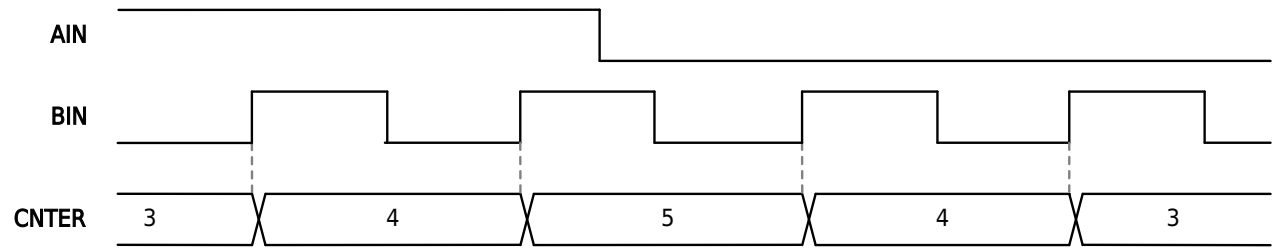


HCUPR.HCUP6=HCUPR.HCUP5=HCUPR.HCUP3=HCUPR.HCUP0=0b1
HCDOR.HCDO7=HCDOR.HCDO4=HCDOR.HCDO2=HCDOR.HCDO1=0b1

Figure 17-19 Phase Difference Counting Operation Setting in Position Mode (Four Times)

Direction Countting

Direction counting refers to configuring the AIN input state as direction control while using the BIN input as clock counting, as shown in the following diagram.



HCUPR.HCUP2=0b1 && HCDOR.HCDO0=0b1

Figure 17-20 Direction Counting Operation In Position Mode

17.3.9.2 Rotation Mode

The quadrature encoding revolution mode refers to adding ZIN input events on the basis of AIN and BIN counting to enable judgment of rotating counts and other parameters. In revolution mode, depending on the counting method of the rotation counter, it can achieve Z-phase counting functionality, position counter output counting function, or a mixed counting function combining Z-phase counting and position counter output. This function is implemented using two Advanced Timers.

Z-Phase Counting

Z-phase counting refers to a counting operation in which the rotation counting unit increments based on the ZIN input signal, while the position counting unit is reset to zero.

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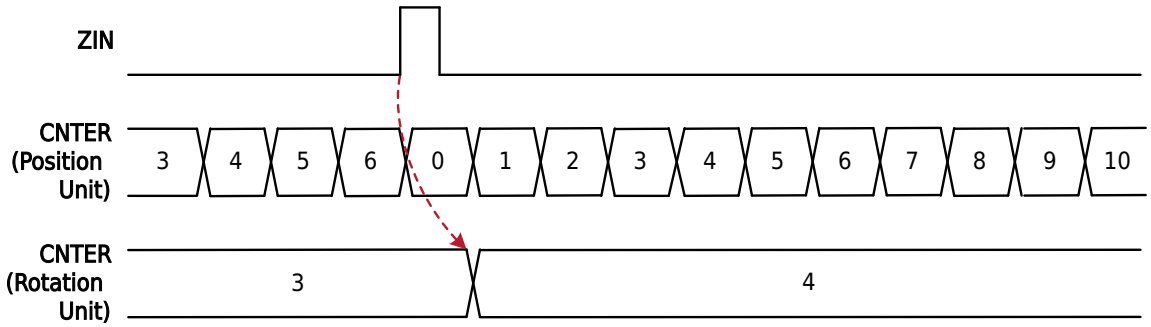

Figure 17-21 Z-Phase Counting Operation in Rotation Mode

Position Overflow Counting

Position overflow counting refers to the condition where the position counting unit generates an overflow or underflow event, which then triggers the rotation counting unit to increment or decrement once. (In this counting mode, the ZIN input does not trigger counting in the rotation counting unit or clear the position counting unit.)

The overflow event of the position counting unit enables position overflow counting by linking through the AOS module to gate the revolution counting unit's count. For the rotation counting unit's hardware increment (decrement) event, select one bit in the event selection register (HCUPR or HCDOR) bits [19:16], while configuring the AOS module to set the corresponding increment (decrement) event source as the position counting unit's overflow event. For details, refer to the AOS Trigger.

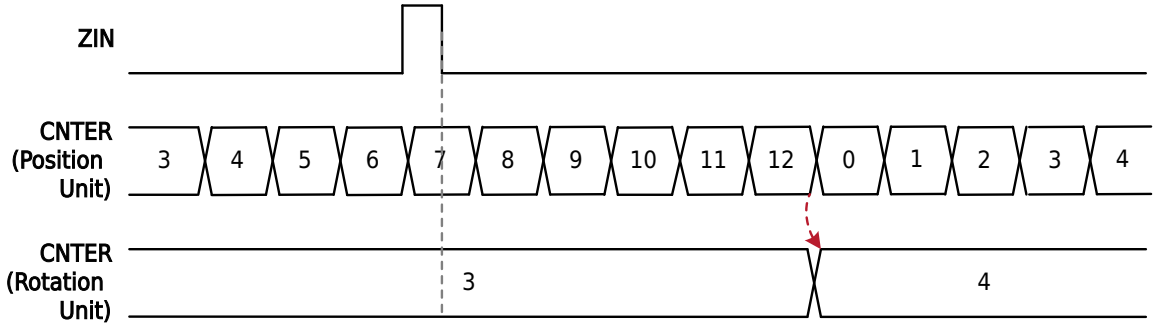

Figure 17-22 Position Counter Output Counting Operation in Rotation Mode

Mixed Counting

Mixed counting refers to a combined counting method that integrates both Z-phase counting and position overflow counting. Its implementation method is also a combination of the above two counting methods.

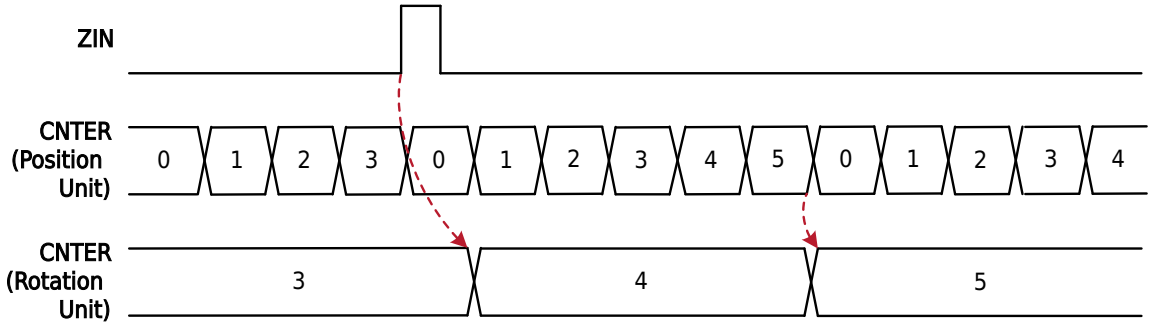

Figure 17-23 Z-Phase and Position Counter Output Mixed Counting Operation in Rotation Mode

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Z-Phase Motion Shielding

In the Z-phase counting function or mixed counting function of rotation counting mode, it can be configured to mask valid ZIN inputs (without triggering counting in the rotation counting unit or clearing the position counting unit) for a specified number of cycles (set by GCONR.ZMSK[0:1]) after the overflow or underflow point of the position counter.

When GCONR.ZMSKPOS of the position counting unit's general control register (GCONR) is set to 1, the Z-phase masking function of the position counting unit is enabled, with the number of masking cycles determined by GCONR.ZMSK. When GCONR.ZMSKREV of the revolution counting unit's general control register (GCONR) is set to 1, the Z-phase masking function of the revolution counting unit is enabled.

The figure below illustrates the operation during mixed counting in revolution counting mode: when a ZIN input occurs within four counting cycles after an overflow of the position counting unit, the ZIN input action is invalid (i.e., the rotation counting unit does not count, and the position counting unit is not cleared). Subsequent ZIN inputs thereafter operate normally.

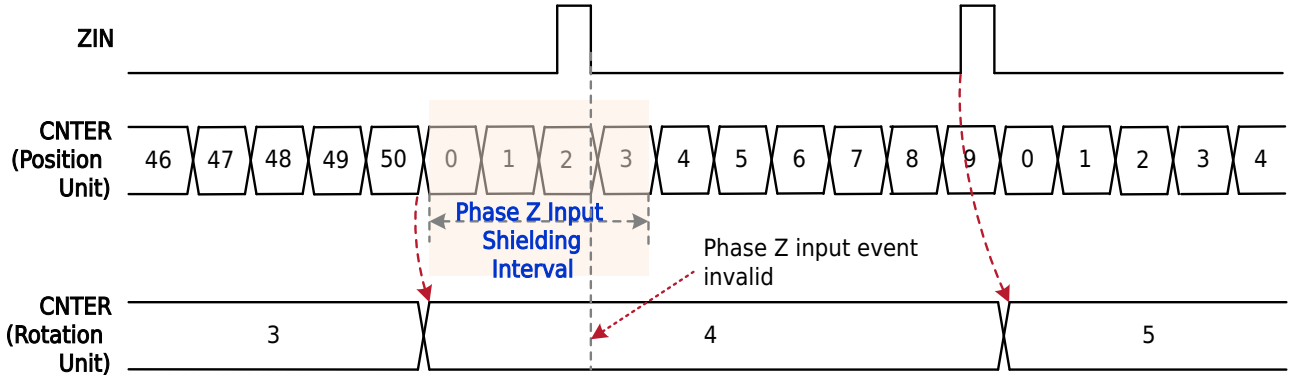

Figure 17-24 Rotation Counting Mode-Mixed Count Z-Phase Masking Action Instance 1

The figure below illustrates the operation during mixed counting in rotation counting mode: On the 3rd cycle after an overflow of the position counting unit, the counting direction changes. At this point, the originally configured four cycles masking period becomes invalid (the actual ZIN masking function was maintained for three cycles), and downward counting begins. After the counting underflow occurs in the position counting unit, the ZIN phase shielding function is re-opened and becomes invalid after four cycles. During the masking period of the ZIN phase, the input function of the ZIN phase is invalid, that is, the revolution counting unit does not count, and the position counting unit does not clear; the subsequent ZIN phase input operates normally.

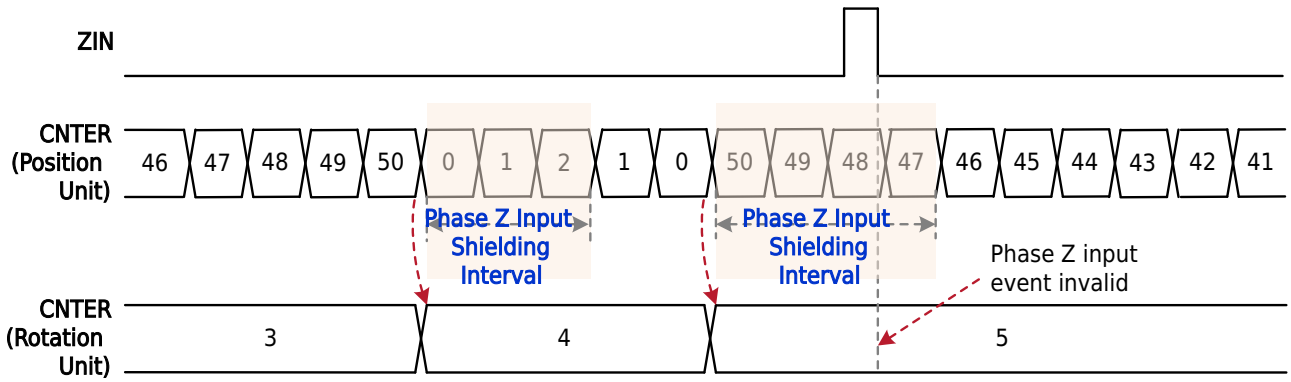

Figure 17-25 Rotation Counting Mode-Mixed Count Z-Phase Masking Action Instance 2

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17.3.10 Periodic Interval Response

The general comparison reference value register (GCMAR-GCMDR) of Timer4/5/6 can generate dedicated valid request signals upon counter compare match, which are sent to the AOS module for coordinated actions with other modules.

These request signals can generate a valid request signal once every few cycles. By setting the VPERR.PCNTS bit in the valid period register (VPERR), the number of cycles between valid request signals can be specified. During other cycles, even if the counter value matches the reference value in GCMAR or GCMBR, no valid request signal will be output. The figure below shows an example of periodic valid request signal operation.

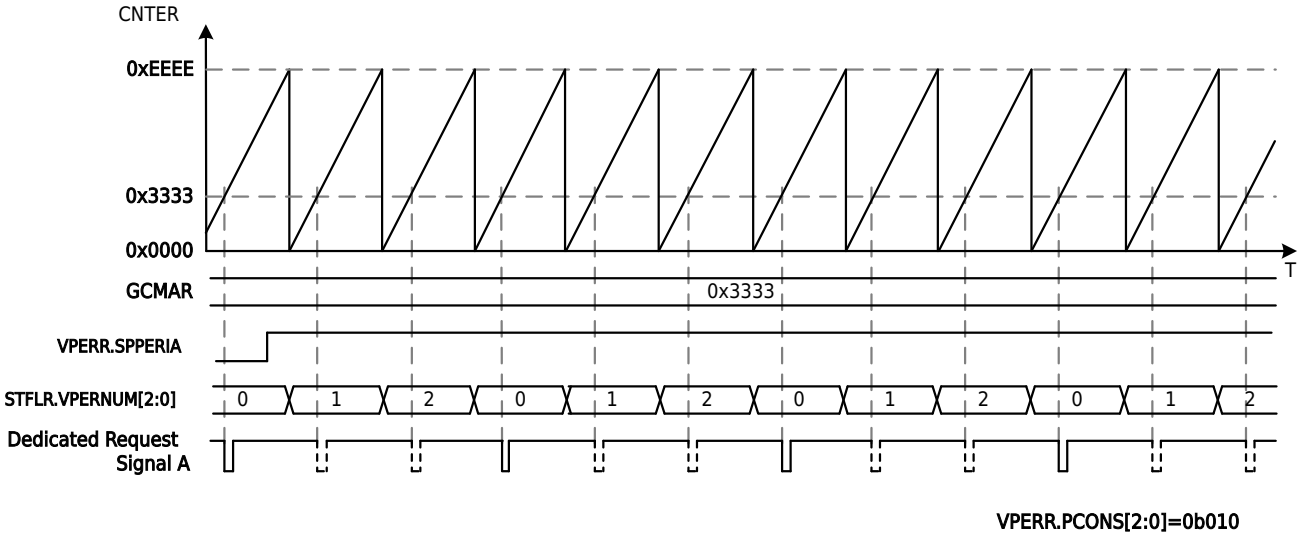

Figure 17-26 Periodic Interval Valid Request Signal Operation

17.3.11 Protection Mechanism

The Advanced Timer can implement protection control over the output state of its ports.

The Advanced Timer has four shared port output disable event interfaces, which are connected to the four sets of brake events output by the brake control module. The selected abnormal condition events for each interface can be configured via the brake control settings. When an abnormal condition is detected on these interfaces, the general PWM outputs can be controlled accordingly.

During normal port output, if a brake event from the brake control is monitored, the port's output state can transit to a predefined condition. When a brake control abnormal event occurs, the general PWM output port state can switch to high-impedance, output low level, or output high level (determined by the settings of PCONR.DISVALA and PCONR.DISVALB).

For example, if PCONR.DISSELA[1:0] = 0b01 and PCONR.DISVALA = 0b01 are configured, then during normal output on the CHA port, if a brake event occurs on output disable condition 1, the CHA port will switch to a high impedance state.

17.3.12 Interrupt Description

Timer4/5/6 each contain three categories totaling nine interrupts. These include four general counter compare match interrupts (including two capture input interrupts), two counter period match interrupts, one dead-time error interrupt, and output level same-high/same-low interrupts.

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Counting Comparison Match Interrupt

Four general comparison reference value registers (GCMAR-GCMDR), which can be compared with the count value to generate a comparison match valid signal. When a counter compare match occurs, the corresponding status flag bits (STFLR.CMAF-STFLR.CMDF) in the Status Flag Register (STFLR) are set to 1. If the corresponding interrupt enable bits (ICONR.INTENA-ICONR.INTEND) in the Interrupt Control Register (ICONR) are set to 1, the associated interrupt request will be triggered.

When the capture input valid condition selected by the hardware capture event selection registers (HCPAR, HCPBR) occurs, a capture input action is executed. If the ICONR.INTENA or ICONR.INTENB bit in the interrupt control register (ICONR) is set to 1 to enable the interrupt, the corresponding interrupt request will be triggered.

Counting Period Match Interrupt

When the sawtooth wave counts up to the overflow point, the sawtooth wave counts down to the underflow point, the triangle wave counts to the valley point, or the triangle wave counts to the peak point, the STFLR.OVFF or STFLR.UDFF bit in the status flag register (STFLR) will be set to 1. If the ICONR.INTENOVF and ICONR.INTENUDF bits in the interrupt control register (ICONR) are enabled, a counter period match interrupt will be triggered at the corresponding timing point.

Dead Time Error Interrupt

When loading the values from the dead time reference value registers (DTUAR, DTDAR) into the general comparison reference value register (GCMBR), if the values exceed the period limit, a dead-time error will occur. This sets the STFLR.DTEF bit in the status flag register (STFLR) to 1. If the ICONR.INTENDE bit in the interrupt control register (ICONR) is set to enable the interrupt at this time, a dead-time error interrupt will be triggered.

17.3.13 DMA

Timer supports software and hardware to trigger DMA for data transfer. Data is supported to be written to the timer from other locations, or read and written from the timer to other locations. It can be applied to the automatic handling of data after data capture and the automatic adjustment of the pulse width changing the period value or duty cycle. Each timer has two DMA requests:

- The TIMxA request trigger source can be selected from general compare/capture A/C, counter overflow, and dedicated compare A.
- The TIMxB request trigger source can be selected from general compare/capture B/D, counter underflow, and dedicated compare B.

IDREQ	Interrupt Signal of Peripheral
0x5A	TIM4A
0x5B	TIM4B
0x5C	TIM5A
0x5D	TIM5B
0x5E	TIM6A
0x5F	TIM6B

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17.3.14 Braking Protection

During initialization, disable conditions 0-3 are configured via PCONR.DISSELA and PCONR.DISSELB, while the preset port state is selected by setting PCONR.DISVALA and PCONR.DISVALB. When a disable condition becomes active, the hardware automatically changes the port state to the preset state (options: maintain normal output, high impedance, low level, or high level).

Port Brake and Software Brake

After polarity selection control and effective enablement, the port signal undergoes digital filtering and synchronization to generate a port braking flag. This port braking flag serves as disable condition 3 for the Advanced Timer. The port brake flag needs to be cleared by software.

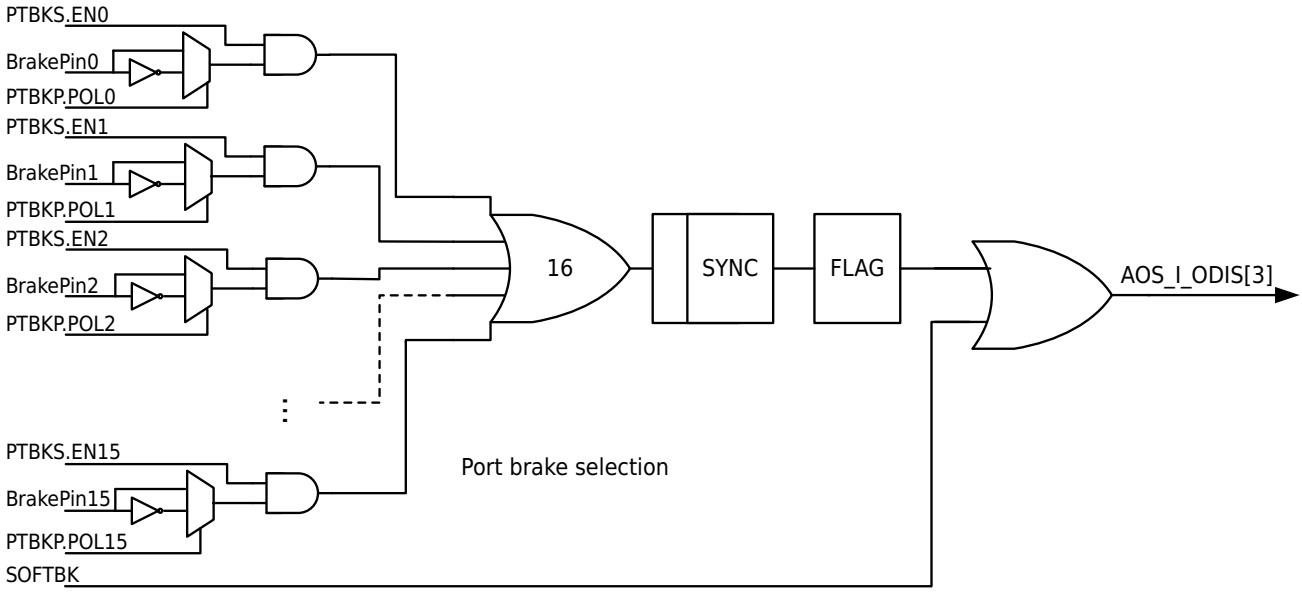

Figure 17-27 Port Braking And Software Braking Diagram

Automatic Braking in Low Power Mode

When the system enters low-power mode and the clock stops, PWM operation is halted. Low-power mode acts as disable condition 2 for the Advanced Timer, triggering PWM braking.

Output Level Same-High/Same-Low Brake

The output levels are monitored, and after effective enablement and synchronization, a same-high/same-low braking flag is generated. This flag serves as disable condition 1 for the Advanced Timer. The same high and same low brake flag needs to be cleared by software.

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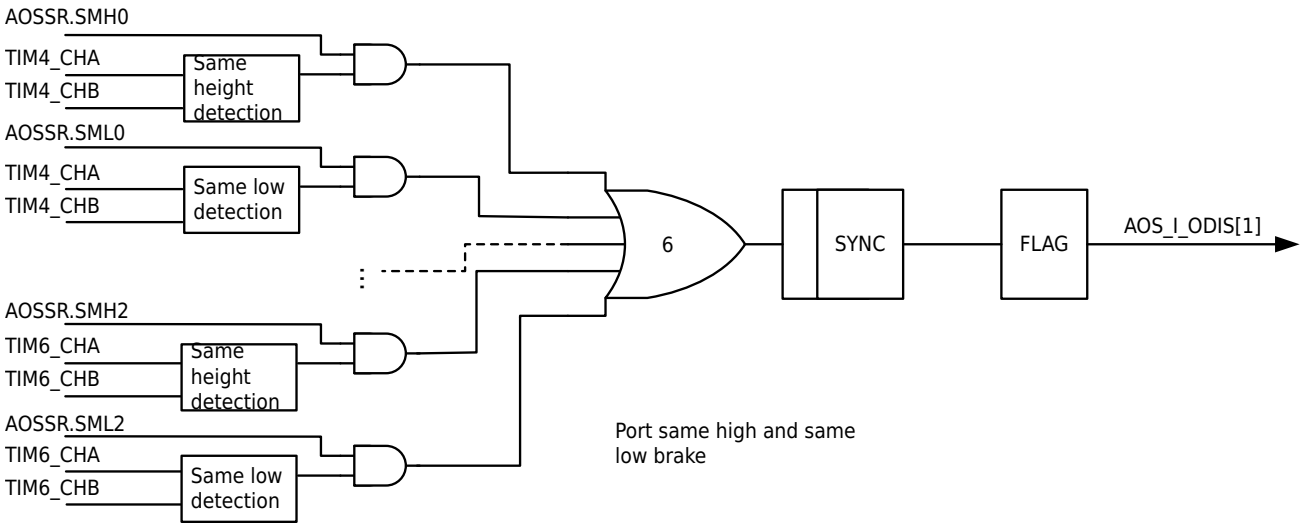

Figure 17-28 Output Same-High/Same-Low Brake Diagram

VC Brake

VC0, VC1, and VC2 interrupt flags, when enabled, serve as invalid condition 0 for the advanced timer.

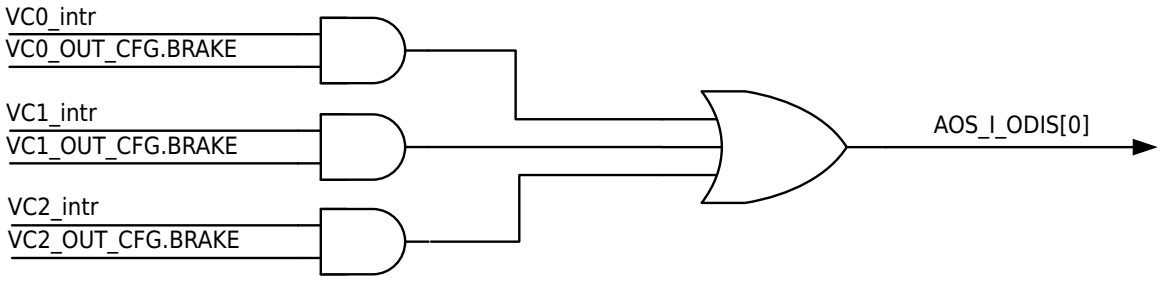

Figure 17-29 VC Brake Control Diagram

17.3.15 Interconnection

Period and Compare Match Trigger Output

Since one INTS of Timer4/5/6 contains multiple match trigger sources. The match signals controlling DMA, ADC, and AOS triggers have independent controls allowing selection of different sources, including overflow, underflow, general compare matches (four types), and dedicated compare matches (two types), totaling any one of the ten TIMx match trigger sources as the trigger condition.

If only output requests are needed to trigger DMA, ADC, and AOS, the corresponding interrupts do not need to be enabled.

The figure below shows the TIM4/5/6 match trigger selection diagram for ADC and AOS. The match trigger DMA selection differs in the CR register control bits.

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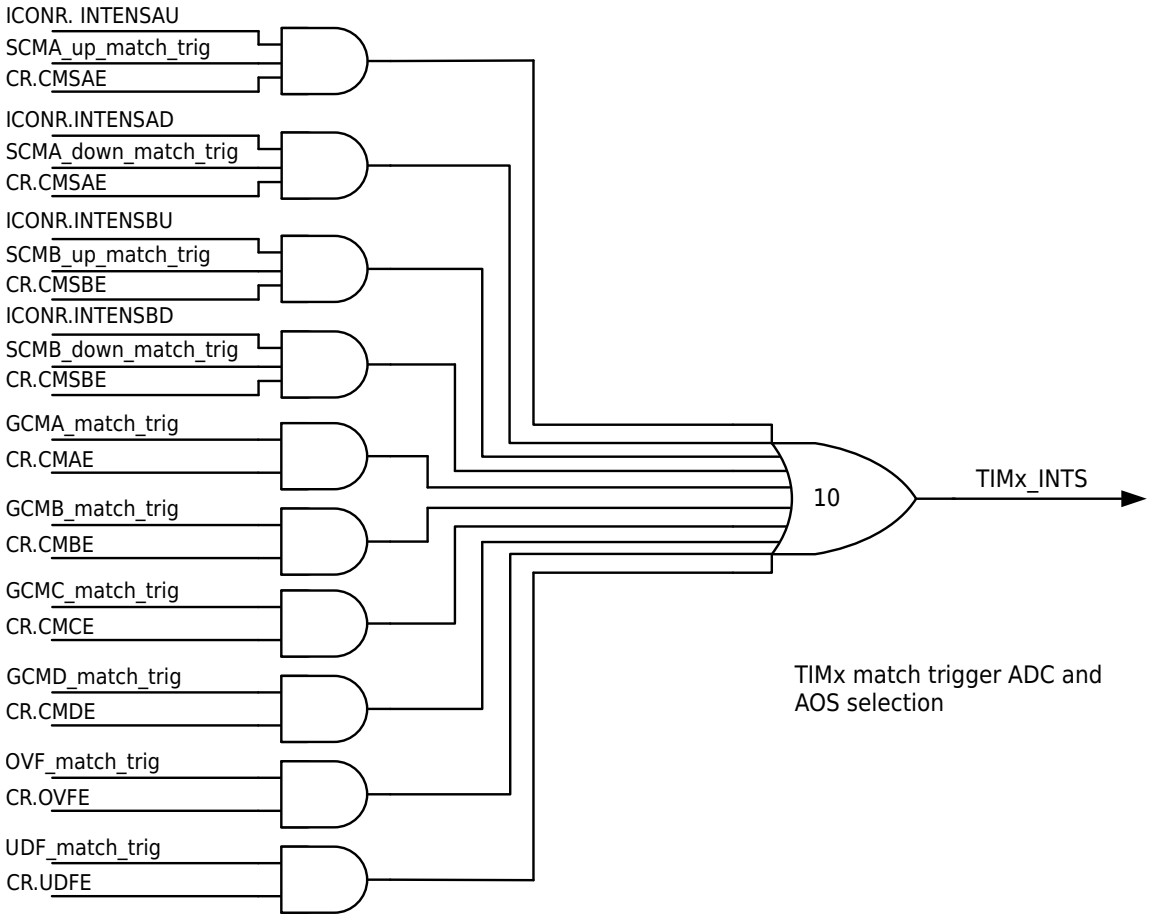

Figure 17-30 Timer4/5/6 Match Trigger ADC and AOS Selection

AOS Trigger

AOS is an internal system signal that, after selection and control, can trigger functions such as start, stop, clear, increment by 1, and decrement by 1 of the Advanced Timer's counter. The Advanced Timer has four AOS trigger channels, each of which can select interrupt sources from different modules. The selected signal generates a single-pulse trigger input to the Advanced Timer, controlling actions such as start, stop, clear, increment by 1, and decrement by 1 of the counter.

Timer4/5/6 internally uses registers to select different AOS_I_TRIG signals as their trigger sources. If you can use the HSTAR register, you can use an interrupt to trigger the hardware start of the corresponding timer.

Table 17-4 AOS Source Selection

	AOS_i_trig3	AOS_i_trig2	AOS_i_trig1	AOS_i_trig0
Select Control Signal	ITRIG.IAOS3S	ITRIG.IAOS2S	ITRIG.IAOS1S	ITRIG.IAOS0S
0b0000	TIM0_INT	TIM0_INT	TIM0_INT	TIM0_INT
0b0001	TIM1_INT	TIM1_INT	TIM1_INT	TIM1_INT
0b0010	TIM2_INT	TIM2_INT	TIM2_INT	TIM2_INT
0b0011	LPTIMER_INT	LPTIMER_INT	LPTIMER_INT	LPTIMER_INT
0b0100	TIM4_INTS	TIM4_INTS	TIM4_INTS	TIM4_INTS
0b0101	TIM5_INTS	TIM5_INTS	TIM5_INTS	TIM5_INTS

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	AOS_i_trig3	AOS_i_trig2	AOS_i_trig1	AOS_i_trig0
Select Control Signal	ITRIG.IAOS3S	ITRIG.IAOS2S	ITRIG.IAOS1S	ITRIG.IAOS0S
0b0110	TIM6_INTS	TIM6_INTS	TIM6_INTS	TIM6_INTS
0b0111	UART0_INT	UART0_INT	UART0_INT	UART0_INT
0b1000	UART1_INT	UART1_INT	UART1_INT	UART1_INT
0b1001	LPUART0_INT	LPUART0_INT	LPUART0_INT	LPUART0_INT
0b1010	VC0_INT	VC0_INT	VC0_INT	VC0_INT
0b1011	VC1_INT	VC1_INT	VC1_INT	VC1_INT
0b1100	RTC_INT	RTC_INT	RTC_INT	RTC_INT
0b1101	PCA_INT	PCA_INT	PCA_INT	PCA_INT
0b1110	SPI_INT	SPI_INT	SPI_INT	SPI_INT
0b1111	ADC_INT	ADC_INT	ADC_INT	ADC_INT

Port Triggers (TRIGA-TRIGD)

Port triggers can control hardware start, stop, clear, capture, and counter increment/decrement functions of the Advanced Timer. Digital filtering is optional, and the ports can be configured to following specific designated ports on the chip.

Table 17-5 Port Trigger Selection

	TRIGD	TRIGC	TRIGB	TRIGA
Select Control Signal	TTRIG.TRIGDS	TTRIG.TRIGCS	TTRIG.TRIGBS	TTRIG.TRIGAS
0b0000	PA3	PA3	PA3	PA3
0b0001	PB3	PB3	PB3	PB3
0b0010	PC3	PC3	PC3	PC3
0b0011	PD3	PD3	PD3	PD3
0b0100	PA7	PA7	PA7	PA7
0b0101	PB7	PB7	PB7	PB7
0b0110	PC7	PC7	PC7	PC7
0b0111	Reserved	Reserved	Reserved	Reserved
0b1000	PA11	PA11	PA11	PA11
0b1001	PB11	PB11	PB11	PB11
0b1010	PC11	PC11	PC11	PC11
0b1011	PD1	PD1	PD1	PD1
0b1100	PA15	PA15	PA15	PA15
0b1101	PB15	PB15	PB15	PB15
0b1110	PC15	PC15	PC15	PC15

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	TRIGD	TRIGC	TRIGB	TRIGA
Select Control Signal	TTRIG.TRIGDS	TTRIG.TRIGCS	TTRIG.TRIGBS	TTRIG.TRIGAS
0b1111	Reserved	Reserved	Reserved	Reserved

VC Compare Output Interconnection with Advanced Timer

VC signals can be internally interconnected to the capture inputs of the Advanced Timer, allowing edge detection of VC outputs. VC0 is connected to CHA, and VC1 is connected to CHB. The control is realized in the VC control register.

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17.4 Register Description

17.4.1 Register List

- Timer4 base address: 0x40003000
- Timer5 base address: 0x40003400
- Timer6 base address: 0x40003800

Table 17-6 Advanced Timer Register Offset

Offset	Register	Description	Width
0x000	TIM_CNTER	General counting reference value register	32
0x004	TIM_PERAR	General period reference value register	32
0x008	TIM_PERBR	General period buffer register	32
0x010	TIM_GCMAR	General comparison A reference value register	32
0x014	TIM_GCMBR	General comparison B reference value register	32
0x018	TIM_GCMCR	General comparison C reference value register	32
0x01C	TIM_GCMDR	General comparison D reference value register	32
0x028	TIM_SCMAR	Special comparison A reference value register	32
0x02C	TIM_SCMBR	Special comparison B reference value register	32
0x040	TIM_DTUAR	Dead time up-counting reference value register	32
0x044	TIM_DTDAR	Dead time down-counting reference value register	32
0x050	TIM_GCONR	General control register	32
0x054	TIM_ICONR	Interrupt control register	32
0x058	TIM_PCONR	Port control register	32
0x05C	TIM_BCONR	Buffer control register	32
0x060	TIM_DCONR	Dead time control register	32
0x068	TIM_FCONR	Filter control register	32
0x06C	TIM_VPERR	Valid period register	32
0x070	TIM_STFLR	Status flag register	32
0x074	TIM_HSTAR	Hardware start event selection register	32
0x078	TIM_HSTPR	Hardware stop event selection register	32

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Offset	Register	Description	Width
0x07C	TIM_HCELR	Hardware clear event selection register	32
0x080	TIM_HCPAR	Hardware capture A event selection register	32
0x084	TIM_HCPBR	Hardware capture B event selection register	32
0x088	TIM_HCUPR	Hardware increment event selection register	32
0x08C	TIM_HCDOR	Hardware decrement event selection register	32
0x100	TIM_IFR	Interrupt flag register	32
0x104	TIM_ICLR	Interrupt flag clear register	32
0x108	TIM_CR	Spread spectrum and trigger selection register	32
0x110	TIM_AOSSR	AOS selection control register (shared by three channels)(1)	32
0x114	TIM_AOSCL	AOS selection control flag clear register (shared by three channels)(1)	32
0x118	TIM_PTBKS	Port brake control register (shared by three channels)(1)	32
0x11C	TIM_TTRIG	Port trigger control register (shared by three channels)(1)	32
0x120	TIM_ITRIG	AOS trigger control register (shared by three channels)(1)	32
0x124	TIM_PTBKP	Port brake polarity control register (shared by three channels)(1)	32
0x3F4	TIM_SSTAR	Software synchronization start register	32
0x3F8	TIM_SSTPR	Software synchronization stop register	32
0x3FC	TIM_SCLRR	Software synchroniaztion clear register	32

Note

1. For the TIM_AOSSR, TIM_AOSCL, TIM_PTBKS, TIM_TTRIG, TIM_ITRIG, and TIM_PTBKP registers, Timer4/5/6 share the same physical register. Any modification made by one timer will simultaneously update the values in the other two timers.

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17.4.2 General Counting Reference Value Register (TIM_CNTER)

Offset	Bit Position																													
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																CNT															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	CNT	The count value of the current counter	RW

17.4.3 General Period Reference Value Register (TIM_PERAR)

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000FFFF																															
Name	Reserved																PERA															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	PERA	Counting period value Set the counting period value for each counting cycle	RW

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17.4.4 General Period Buffer Register (TIM_PERBR)

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000FFFF																															
Name	Reserved																PERB															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	PERB	Buffer value of the count period	RW

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17.4.5 General Comparison x Reference Value Register (TIM_GCMxR) (x=A/B/C/D)

Offset: 0x010 (GCMAR), 0x014 (GCMBR), 0x018 (GCMCR), 0x01C (GCMDR)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000FFFF																															
Name	Reserved																															
																	GCMx															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	GCMx	Count comparison reference value General comparison reference value setting, the matching signal is valid when it is equal to the count value	RW

17.4.6 Special Comparison x Reference Value Register (TIM_SCMxR) (x=A/B)

Offset: 0x028 (SCMAR), 0x02C (SCMBR)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000FFFF																															
Name	Reserved																															
																	SCMx															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	SCMx	Count comparison reference value Special comparison reference value setting, match signal becomes valid when equal to the count value	RW

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17.4.7 Dead Time Up-counting Reference Value Register (TIM_DTUAR)

Offset	Bit Position																													
0x040	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000FFFF																															
Name	Reserved																DTUA															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	DTUA	Dead time value Dead time up-counting reference preset value	RW

17.4.8 Dead Time Down-counting Reference Value Register (TIM_DTDAR)

Offset	Bit Position																													
0x044	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000FFFF																															
Name	Reserved																DTDA															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	DTDA	Dead time value Dead time down-counting reference preset value	RW

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17.4.9 General Control Register (TIM_GCONR)

Offset	Bit Position																													
0x050	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000100																															
Name	Reserved												ZMSK		ZMSKPOS	ZMSKREV	Reserved							DIR	Reserved	CKDIV			MODE		START	
Access													RW		RW	RW								RW		RW			RW		RW	

Bit	Name	Functional Description	Access
31:20	*Reserved*	-	-
19:18	ZMSK	Z-phase input mask cycle count Quadrature encoding phase Z input masked count period value ● 0b00: Z phase input mask function is disabled. ● 0b01: Z phase input is masked during the 4 counting cycles after position count overflow or underflow. ● 0b10: Z phase input is masked during the 8 counting cycles after position count overflow or underflow. ● 0b11: Z phase input is masked during the 16 counting cycles after position count overflow or underflow.	RW
17	ZMSKPOS	Z phase input position counter selection ● 0b0: When the Z-phase input is enabled, this timer functions as a position counter, and the position counter clear operation works normally during the mask period ● 0b1: When the Z-phase input is enabled, this timer functions as a position counter, and the position counter clear operation is masked during the mask period	RW
16	ZMSKREV	Z phase input rotation counter selection ● 0b0: When the Z-phase input is enabled, this timer functions as a rotation counter, and the revolution counter counting operation works normally during the mask period ● 0b1: When the Z-phase input is enabled, this timer functions as a rotation counter, and the revolution counter counting operation is masked during the mask period	RW
15:9	*Reserved*	-	-
8	DIR	Count direction ● 0b0: Decremental counting ● 0b1: Incremental counting	RW
7	*Reserved*	-	-

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Bit	Name	Functional Description	Access
6:4	CKDIV	Count clock selection ● 0b000: PCLK0 ● 0b001: PCLK0/2 ● 0b010: PCLK0/4 ● 0b011: PCLK0/8 ● 0b100: PCLK0/16 ● 0b101: PCLK0/64 ● 0b110: PCLK0/256 ● 0b111: PCLK0/1024	RW
3:1	MODE	Counting mode ● 0b000: Sawtooth wave mode ● 0b100: Triangle wave mode A ● 0b010: Triangle wave mode B **Notice** Do not set any values other than those specified above.	RW
0	START	Counter start ● 0b0: Counter stopped ● 0b1: Counter started **Note** This bit automatically clears to 0 when either a software stop condition or hardware stop condition becomes active.	RW

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17.4.10 Interrupt Control Register (TIM_ICONR)

Offset	Bit Position																													
0x054	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved												INTENSBD	INTENSBU	INTENSAD	INTENSAU	INTENSAMH	INTENSAML	Reserved					INTENDE	INTENUDF	INTENOVF	Reserved		INTEND	INTENC	INTENB	INTENA
Access													RW	RW	RW	RW	RW	RW						RW	RW	RW			RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:20	*Reserved*	-	-
19	INTENSBD	Dedicated down-counting compare match B trigger output enable ● 0b0: Trigger output disabled on match ● 0b1: Trigger output enabled on match	RW
18	INTENSBU	Dedicated up-counting compare match B trigger output enable ● 0b0: Trigger output disabled on match ● 0b1: Trigger output enabled on match	RW
17	INTENSAD	Dedicated down-counting compare match A trigger output enable ● 0b0: Trigger output disabled on match ● 0b1: Trigger output enabled on match	RW
16	INTENSAU	Dedicated up-counting compare match A trigger output enable ● 0b0: Trigger output disabled on match ● 0b1: Trigger output enabled on match	RW
15	INTENSAMH	Simultaneously high interrupt enable ● 0b0: Interrupt disabled when outputs are simultaneously high ● 0b1: Interrupt enabled when outputs are simultaneously high	RW
14	INTENSAML	Simultaneously low interrupt enable ● 0b0: Interrupt disabled when outputs are simultaneously low ● 0b1: Interrupt enabled when outputs are simultaneously low	RW
13:9	*Reserved*	-	-
8	INTENDE	Dead time error interrupt enable ● 0b0: When the dead time is wrong, the interrupt is invalid ● 0b1: When the dead time is wrong, the interrupt is enabled	RW
7	INTENUDF	Underflow interrupt enable ● 0b0: When an overflow occurs during a sawtooth wave or counts to the valley point during a triangular wave, the interrupt is invalid ● 0b1: When an underflow occurs during a sawtooth waveform or counts to a valley point during a triangular waveform, the interrupt is enabled	RW

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Bit	Name	Functional Description	Access
6	INTENOVF	Overflow interrupt enable ● 0b0: When an overflow occurs during a sawtooth wave or counts to the peak point during a triangular wave, the interrupt is invalid ● 0b1: When an overflow occurs in a sawtooth wave or counts to the peak point in a triangular wave, the interrupt is enabled	RW
5:4	*Reserved*	-	-
3	INTEND	General count compare match D interrupt enable ● 0b0: When the GCMDR register is equal to the count value, the interrupt is invalid ● 0b1: When the GCMDR register is equal to the count value, the interrupt is enabled	RW
2	INTENC	General count compare match C interrupt enable ● 0b0: When the GCMCR register is equal to the count value, the interrupt is invalid ● 0b1: When the GCMCR register is equal to the count value, the interrupt is enabled	RW
1	INTENB	General count compare match B interrupt enable ● 0b0: The interrupt is invalid when the GCMBR register is equal to the count value or when a capture input event occurs ● 0b1: This interrupt is enabled when the GCMBR register is equal to the count value, or when a capture input event occurs	RW
0	INTENA	General count compare match A interrupt enable ● 0b0: The interrupt is invalid when the GCMAR register is equal to the count value or when a capture input event occurs ● 0b1: This interrupt is enabled when the GCMAR register is equal to the count value, or when a capture input event occurs	RW

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17.4.11 Port Control Register (TIM_PCONR)

Offset	Bit Position																													
0x058	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved		DISVALB		DISSELB		OUTENB	PERCB		CMPCB		STASTPSB		STPCB	STACB		CAPCB	Reserved		DISVALA		DISSELA		OUTENA	PERCA		CMPCA		STASTPSA		STPCA	STACA		CAPCA
Access		RW		RW		RW		RW		RW		RW		RW	RW		RW		RW		RW		RW	RW		RW		RW		RW	RW		RW

Bit	Name	Functional Description	Access
31:29	*Reserved*	-	-
28:27	DISVALB	CHB output status control ● 0b00: When the condition selected among the forced output invalid conditions 0-3 is met, the CHB port outputs normally ● 0b01: When the selected condition among the forced output invalid conditions 0-3 is met, the CHB port outputs a high-impedance state ● 0b10: When the condition selected in the forced output invalid condition 0-3 is met, the CHB port outputs a low level ● 0b11: When the selected condition among the forced output invalid conditions 0-3 is met, the CHB port outputs a high level	RW
26:25	DISSELB	Force output invalid condition selection B ● 0b00: Select forced output invalid condition 0 ● 0b01: Select forced output invalid condition 1 ● 0b10: Select forced output invalid condition 2 ● 0b11: Select forced output invalid condition 3	RW
24	OUTENB	Output enable B ● 0b0: CHB port output is invalid when the Advanced Timer function is active ● 0b1: CHB port output is valid when the Advanced Timer function is active	RW
23:22	PERCB	Port status setting B upon period value match ● 0b00: When the counter count value is equal to the period value, the CHB port output remains low level ● 0b01: When the counter count value is equal to the period value, the CHB port output is set to high level ● 0b10: When the counter count value is equal to the period value, the CHB port output is set to the previous state ● 0b11: When the count value of the counter is equal to the period value, the output of the CHB port is set as the inversion level	RW

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Bit	Name	Functional Description	Access
21:20	CMPCB	Port status setting B upon compare value match ● 0b00: When the counter count value is equal to GCMBR, the CHB port output remains low level ● 0b01: When the counter count value is equal to GCMBR, the CHB port output is set to high level ● 0b10: When the counter count value is equal to GCMBR, the CHB port output is set to the previous state ● 0b11: When the count value of the counter is equal to GCMBR, the CHB port output is set as the inversion level	RW
19	STASTPSB	Counting start/stop port status selection B ● 0b0: When counting starts or stops, CHB port output is determined by STACB, STPCB ● 0b1: When counting starts or stops, the CHB port output is set to the previous state **Note** The counting start here refers to the initial counting start or stop and restart; the counting stop refers to the initial stop or counting start and then stop.	RW
18	STPCB	Counter stop port state setting B ● 0b0: When counting stops, CHB port output is set to low level ● 0b1: When counting stops, CHB port output is set to high level	RW
17	STACB	Port status setting B upon counting start ● 0b0: When counting starts, CHB port output is set to low level ● 0b1: When counting starts, CHB port output is set to high level	RW
16	CAPCB	Function mode selection B ● 0b0: Comparison output function ● 0b1: Capture input function	RW
15:13	*Reserved*	-	-
12:11	DISVALA	CHA output status control ● 0b00: When the condition selected among the forced output invalid conditions 0-3 is met, the CHA port outputs normally ● 0b01: When the selected condition among the forced output invalid conditions 0-3 is met, the CHA port outputs a high-impedance state ● 0b10: When the condition selected in the forced output invalid condition 0-3 is met, the CHA port outputs a low level ● 0b11: When the selected condition among the forced output invalid conditions 0-3 is met, the CHA port outputs a high level	RW
10:9	DISSELA	Force output invalid condition selection A ● 0b00: Select forced output invalid condition 0 ● 0b01: Select forced output invalid condition 1 ● 0b10: Select forced output invalid condition 2 ● 0b11: Select forced output invalid condition 3	RW

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Bit	Name	Functional Description	Access
8	OUTENA	Output enable A ● 0b0: CHA port output is invalid when the Advanced Timer function is active ● 0b1: CHA port output is valid when the Advanced Timer function is active	RW
7:6	PERCA	Port status setting A upon period value match ● 0b00: When the counter count value is equal to the period value, the CHA port output remains low level ● 0b01: When the counter count value is equal to the period value, the CHA port output is set to high level ● 0b10: When the counter count value is equal to the period value, the CHA port output is set to the previous state ● 0b11: When the count value of the counter is equal to the period value, the output of the CHA port is set as the inversion level	RW
5:4	CMPCA	Port status setting A upon compare value match ● 0b00: When the counter count value is equal to GCMAR, the CHA port output remains low level ● 0b01: When the counter count value is equal to GCMAR, the CHA port output is set to high level ● 0b10: When the counter count value is equal to GCMAR, the CHA port output is set to the previous state ● 0b11: When the count value of the counter is equal to GCMAR, the CHA port output is set as the inversion level	RW
3	STASTPSA	Counting start/stop port status selection A ● 0b0: When counting starts or stops, CHA port output is determined by STACA, STPCA ● 0b1: When counting starts or stops, the CHA port output is set to the previous state **Note** The counting start here refers to the initial counting start or stop and restart; the counting stop refers to the initial stop or counting start and then stop.	RW
2	STPCA	Count stop port state setting A ● 0b0: When counting stops, CHA port output is set to low level ● 0b1: When counting stops, CHA port output is set to high level	RW
1	STACA	Port status setting B upon counting start ● 0b0: When counting starts, CHA port output is set to low level ● 0b1: When counting starts, CHA port output is set to high level	RW
0	CAPCA	Function mode selection A ● 0b0: Comparison output function ● 0b1: Capture input function	RW

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17.4.12 Buffer Control Register (TIM_BCONR)

Offset	Bit Position																															
0x05C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																							BENP	Reserved					BENB	Reserved	BENA
Access																								RW						RW		RW

Bit	Name	Functional Description	Access
31:9	*Reserved*	-	-
8	BENP	Periodic value buffer transfer ● 0b0: Cache transfer disabled ● 0b1: Cache transfer enabled (PERBR-> PERAR)	RW
7:3	*Reserved*	-	-
2	BENB	General comparison value cache transfer B ● 0b0: Cache transfer is disabled ● 0b1: Cache transfer is enabled ▶ For comparison output function: GCMDR-> GCMBR ▶ For capture input function: GCMBR-> GCMDR	RW
1	*Reserved*	-	-
0	BENA	General comparison value cache transfer selection A ● 0b0: Cache transfer is disabled ● 0b1: Cache transfer is enabled ▶ For comparison output function: GCMCR-> GCMAR ▶ For capture input function: GCMAR-> GCMCR	RW

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17.4.13 Dead Time Control Register (TIM_DCONR)

Offset	Bit Position																													
0x060	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																							SEPA	Reserved							DTCEN
Access																								RW								RW

Bit	Name	Functional Description	Access
31:9	*Reserved*	-	-
8	SEPA	Separation Setting ● 0b0: DTUAR and DTDAR are set separately. ● 0b1: The value of DTDAR is automatically equal to the value of DTUAR	RW
7:1	*Reserved*	-	-
0	DTCEN	Dead zone function ● 0b0: Dead zone function is disabled ● 0b1: Dead zone function is enabled	RW

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17.4.14 Filter Control Register (TIM_FCONR)

Offset	Bit Position																													
0x068	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved	NOFICKTD		NOFIENTD	Reserved	NOFICKTC		NOFIENTC	Reserved	NOFICKTB		NOFIENTB	Reserved	NOFICKTA		NOFIENTA	Reserved									NOFICKGB		NOFIENGB	Reserved	NOFICKGA		NOFIENGA
Access		RW		RW		RW		RW		RW		RW		RW		RW										RW		RW		RW		RW

Bit	Name	Functional Description	Access
31	*Reserved*	-	-
30:29	NOFICKTD	TRIGD port input filter sampling reference clock selection ● 0b00: PCLK0 ● 0b01: PCLK0/4 ● 0b10: PCLK0/16 ● 0b11: PCLK0/64	RW
28	NOFIENTD	TRIGD port capture input filter enable ● 0b0: Disable ● 0b1: Enable	RW
27	*Reserved*	-	-
26:25	NOFICKTC	TRIGC port input filter sampling reference clock selection ● 0b00: PCLK0 ● 0b01: PCLK0/4 ● 0b10: PCLK0/16 ● 0b11: PCLK0/64	RW
24	NOFIENTC	TRIGC port capture input filter enable ● 0b0: Disable ● 0b1: Enable	RW
23	*Reserved*	-	-
22:21	NOFICKTB	TRIGB port input filter sampling reference clock selection ● 0b00: PCLK0 ● 0b01: PCLK0/4 ● 0b10: PCLK0/16 ● 0b11: PCLK0/64	RW
20	NOFIENTB	TRIGB port capture input filter enable ● 0b0: Disable ● 0b1: Enable	RW
19	*Reserved*	-	-

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Bit	Name	Functional Description	Access
18:17	NOFICKTA	TRIGA port input filter sampling reference clock selection ● 0b00: PCLK0 ● 0b01: PCLK0/4 ● 0b10: PCLK0/16 ● 0b11: PCLK0/64	RW
16	NOFIENTA	TRIGA port capture input filter enable ● 0b0: Disable ● 0b1: Enable	RW
15:7	*Reserved*	-	-
6:5	NOFICKGB	CHB port input filter sampling reference clock selection ● 0b00: PCLK0 ● 0b01: PCLK0/4 ● 0b10: PCLK0/16 ● 0b11: PCLK0/64	RW
4	NOFIENGB	CHB port capture input filter enable ● 0b0: Disable ● 0b1: Enable	RW
3	*Reserved*	-	-
2:1	NOFICKGA	CHA port input filter sampling reference clock selection ● 0b00: PCLK0 ● 0b01: PCLK0/4 ● 0b10: PCLK0/16 ● 0b11: PCLK0/64	RW
0	NOFIENGA	CHA port capture input filter enable ● 0b0: Disable ● 0b1: Enable	RW

Note

TRIGA-D filter setting is only valid in TIM4, and invalid in Timer5/6.

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17.4.15 Valid Period Register (TIM_VPERR)

Offset	Bit Position																													
0x06C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved											PCNTS			PCNTE		Reserved												GEPERID	GEPERIC	GEPERIB	GEPERIA
Access												RW			RW														RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:21	*Reserved*	-	-
20:18	PCNTS	Valid period selection ● 0b000: Effective cycle selection function is disabled ● 0b001: Effective once every one cycle ● 0b010: Effective once every two cycles ● 0b011: Effective once every three cycles ● 0b100: Effective once every four cycles ● 0b101: Effective once every five cycles ● 0b110: Effective once every six cycles ● 0b111: Effective once every seven cycles	RW
17:16	PCNTE	Valid cycle counting condition selection ● 0b00: Effective cycle selection function is disabled ● 0b01: Sawtooth wave count overflow/underflow or triangle wave trough as count condition ● 0b10: Sawtooth wave count overflow/underflow or triangle wave peak as count condition ● 0b11: Sawtooth wave count overflow/underflow or triangle wave trough/peak as count condition	RW
15:4	*Reserved*	-	-
3	GEPERID	General signal effective period selection D ● 0b0: Effective cycle selection function is disabled ● 0b1: Effective cycle selection function is enabled	RW
2	GEPERIC	General signal effective period selection C ● 0b0: Effective cycle selection function is disabled ● 0b1: Effective cycle selection function is enabled	RW
1	GEPERIB	General signal effective period selection B ● 0b0: Effective cycle selection function is disabled ● 0b1: Effective cycle selection function is enabled	RW
0	GEPERIA	General signal effective period selection A ● 0b0: Effective cycle selection function is disabled ● 0b1: Effective cycle selection function is enabled	RW

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17.4.16 Status Flag Register (TIM_STFLR)

Offset	Bit Position																													
0x070	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	DIRF	Reserved							VPERNUM			Reserved								CMSBDF	CMSBUF	CMSADF	CMSAUF	DTEF	UDFF	OVFF	Reserved			CMDF	CMCF	CMBF	CMAF
Access	RO								RO											RW	RW	RW	RW	RW	RW	RW				RW	RW	RW	RW

Bit	Name	Functional Description	Access
31	DIRF	Count direction ● 0b0: Decremental counting ● 0b1: Incremental counting	RO
30:24	*Reserved*	-	-
23:21	VPERNUM	Number of cycles When the valid cycle selection function is enabled, it represents the number of cycles after counting.	RO
20:13	*Reserved*	-	-
12	CMSBDF	Down-counting dedicated comparison reference value match B ● 0b0: No match occurred ● 0b1: Match occurred	RW
11	CMSBUF	Up-counting dedicated comparison reference value match B ● 0b0: No match occurred ● 0b1: Match occurred	RW
10	CMSADF	Down-counting dedicated comparison reference value match A ● 0b0: No match occurred ● 0b1: Match occurred	RW
9	CMSAUF	Up-counting dedicated comparison reference value match A ● 0b0: No match occurred ● 0b1: Match occurred	RW
8	DTEF	Dead zone time error ● 0b0: No dead zone time error occurred ● 0b1: Dead zone time error occurred	RW
7	UDFF	Underflow match ● 0b0: No sawtooth wave underflow or triangular wave counting to the valley point occurred ● 0b1: Sawtooth wave underflow or triangular wave counting to the valley point occurred	RW

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Bit	Name	Functional Description	Access
6	OVFF	Overflow match ● 0b0: No sawtooth wave overflow or triangular wave counting to the peak point occurred ● 0b1: Sawtooth wave overflow or triangular wave counting to the peak point occurred	RW
5:4	*Reserved*	-	-
3	CMDF	Count match D ● 0b0: The value in the GCMDR register does not match the count value ● 0b1: The value in the GCMDR register matches the count value	RW
2	CMCF	Count match C ● 0b0: The value in the GCMCR register does not match the count value ● 0b1: The value in the GCMCR register matches the count value	RW
1	CMBF	Count match B ● 0b0: The value of GCMBR register does not match the count value, and no CHB capture completion action has occurred ● 0b1: The value of GCMBR register equals the count value, or a CHB capture completion action occurs	RW
0	CMAF	Count match A ● 0b0: The value of GCMAR register does not match the count value, and no CHA capture completion action has occurred ● 0b1: The value of GCMAR register equals the count value, or a CHA capture completion action occurs	RW

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17.4.17 Hardware Start Event Selection Register (TIM_HSTAR)

Offset	Bit Position																													
0x074	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	STARTS	Reserved															HSTA15	HSTA14	HSTA13	HSTA12	HSTA11	HSTA10	HSTA9	HSTA8	HSTA7	HSTA6	HSTA5	HSTA4	HSTA3	HSTA2	HSTA1	HSTA0
Access	RW																RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31	STARTS	Hardware start enable ● 0b0: Hardware start is disabled ● 0b1: Hardware start is enabled **Note** When the hardware startup is enabled, the setting of SSTAR is disabled.	RW
30:16	*Reserved*	-	-
15	HSTA15	Hardware start condition 15 TIMTRID port is sampled to the falling edge ● 0b0: Hardware start is disabled when the condition is met ● 0b1: Hardware start is enabled when the condition is met	RW
14	HSTA14	Hardware start condition 14 TIMTRID port is sampled to the rising edge ● 0b0: Hardware start is disabled when the condition is met ● 0b1: Hardware start is enabled when the condition is met	RW
13	HSTA13	Hardware start condition 13 TIMTRIC port is sampled to the falling edge ● 0b0: Hardware start is disabled when the condition is met ● 0b1: Hardware start is enabled when the condition is met	RW
12	HSTA12	Hardware start condition 12 TIMTRIC port is sampled to the rising edge ● 0b0: Hardware start is disabled when the condition is met ● 0b1: Hardware start is enabled when the condition is met	RW
11	HSTA11	Hardware start condition 11 TIMTRIB port is sampled to the falling edge ● 0b0: Hardware start is disabled when the condition is met ● 0b1: Hardware start is enabled when the condition is met	RW
10	HSTA10	Hardware start condition 10 TIMTRIB port is sampled to the rising edge ● 0b0: Hardware start is disabled when the condition is met ● 0b1: Hardware start is enabled when the condition is met	RW

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Bit	Name	Functional Description	Access
9	HSTA9	Hardware start condition 9 TIMTRIA port is sampled to the falling edge ● 0b0: Hardware start is disabled when the condition is met ● 0b1: Hardware start is enabled when the condition is met	RW
8	HSTA8	Hardware start condition 8 TIMTRIA port is sampled to the rising edge ● 0b0: Hardware start is disabled when the condition is met ● 0b1: Hardware start is enabled when the condition is met	RW
7	HSTA7	Hardware start condition 7 CHB port is sampled to the falling edge ● 0b0: Hardware start is disabled when the condition is met ● 0b1: Hardware start is enabled when the condition is met	RW
6	HSTA6	Hardware start condition 6 CHB port is sampled to the rising edge ● 0b0: Hardware start is disabled when the condition is met ● 0b1: Hardware start is enabled when the condition is met	RW
5	HSTA5	Hardware start condition 5 CHA port is sampled to the falling edge ● 0b0: Hardware start is disabled when the condition is met ● 0b1: Hardware start is enabled when the condition is met	RW
4	HSTA4	Hardware start condition 4 CHA port is sampled to the rising edge ● 0b0: Hardware start is disabled when the condition is met ● 0b1: Hardware start is enabled when the condition is met	RW
3	HSTA3	Hardware start condition 3 Event trigger 3 from AOS is enabled ● 0b0: Hardware start is disabled when the condition is met ● 0b1: Hardware start is enabled when the condition is met	RW
2	HSTA2	Hardware start condition 2 Event trigger 2 from AOS is enabled ● 0b0: Hardware start is disabled when the condition is met ● 0b1: Hardware start is enabled when the condition is met	RW
1	HSTA1	Hardware start condition 1 Event trigger 1 from AOS is enabled ● 0b0: Hardware start is disabled when the condition is met ● 0b1: Hardware start is enabled when the condition is met	RW
0	HSTA0	Hardware start condition 0 Event trigger 0 from AOS is enabled ● 0b0: Hardware start is disabled when the condition is met ● 0b1: Hardware start is enabled when the condition is met	RW

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17.4.18 Hardware Stop Event Selection Register (TIM_HSTPR)

Offset	Bit Position																													
0x078	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	STOPS	Reserved															HSTP15	HSTP14	HSTP13	HSTP12	HSTP11	HSTP10	HSTP9	HSTP8	HSTP7	HSTP6	HSTP5	HSTP4	HSTP3	HSTP2	HSTP1	HSTP0
Access	RW																RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31	STOPS	Hardware stop enable ● 0b0: Hardware stop is disabled ● 0b1: Hardware stop is enabled **Note** When the hardware stop is enabled, the setting of SSTPR is disabled.	RW
30:16	*Reserved*	-	-
15	HSTP15	Hardware stop condition 15 TIMTRID port is sampled to the falling edge ● 0b0: When the condition is matched, the hardware stop is disabled ● 0b1: When the condition is matched, the hardware stop is enabled	RW
14	HSTP14	Hardware stop condition 14 TIMTRID port is sampled to the rising edge ● 0b0: When the condition is matched, the hardware stop is disabled ● 0b1: When the condition is matched, the hardware stop is enabled	RW
13	HSTP13	Hardware stop condition 13 TIMTRIC port is sampled to the falling edge ● 0b0: When the condition is matched, the hardware stop is disabled ● 0b1: When the condition is matched, the hardware stop is enabled	RW
12	HSTP12	Hardware stop condition 12 TIMTRIC port is sampled to the rising edge ● 0b0: When the condition is matched, the hardware stop is disabled ● 0b1: When the condition is matched, the hardware stop is enabled	RW

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Bit	Name	Functional Description	Access
11	HSTP11	Hardware stop condition 11 TIMTRIB port is sampled to the falling edge ● 0b0: When the condition is matched, the hardware stop is disabled ● 0b1: When the condition is matched, the hardware stop is enabled	RW
10	HSTP10	Hardware stop condition 10 TIMTRIB port is sampled to the rising edge ● 0b0: When the condition is matched, the hardware stop is disabled ● 0b1: When the condition is matched, the hardware stop is enabled	RW
9	HSTP9	Hardware stop condition 9 TIMTRIA port is sampled to the falling edge ● 0b0: When the condition is matched, the hardware stop is disabled ● 0b1: When the condition is matched, the hardware stop is enabled	RW
8	HSTP8	Hardware stop condition 8 TIMTRIA port is sampled to the rising edge ● 0b0: When the condition is matched, the hardware stop is disabled ● 0b1: When the condition is matched, the hardware stop is enabled	RW
7	HSTP7	Hardware stop condition 7 CHB port is sampled to the falling edge ● 0b0: When the condition is matched, the hardware stop is disabled ● 0b1: When the condition is matched, the hardware stop is enabled	RW
6	HSTP6	Hardware stop condition 6 CHB port is sampled to the rising edge ● 0b0: When the condition is matched, the hardware stop is disabled ● 0b1: When the condition is matched, the hardware stop is enabled	RW
5	HSTP5	Hardware stop condition 5 CHA port is sampled to the falling edge ● 0b0: When the condition is matched, the hardware stop is disabled ● 0b1: When the condition is matched, the hardware stop is enabled	RW

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Bit	Name	Functional Description	Access
4	HSTP4	Hardware stop condition 4 CHA port is sampled to the rising edge ● 0b0: When the condition is matched, the hardware stop is disabled ● 0b1: When the condition is matched, the hardware stop is enabled	RW
3	HSTP3	Hardware stop condition 3 Event trigger 3 from AOS is enabled ● 0b0: When the condition is matched, the hardware stop is disabled ● 0b1: When the condition is matched, the hardware stop is enabled	RW
2	HSTP2	Hardware stop condition 2 Event trigger 2 from AOS is enabled ● 0b0: When the condition is matched, the hardware stop is disabled ● 0b1: When the condition is matched, the hardware stop is enabled	RW
1	HSTP1	Hardware stop condition 1 Event trigger 1 from AOS is enabled ● 0b0: When the condition is matched, the hardware stop is disabled ● 0b1: When the condition is matched, the hardware stop is enabled	RW
0	HSTP0	Hardware stop condition 0 Event trigger 0 from AOS is enabled ● 0b0: When the condition is matched, the hardware stop is disabled ● 0b1: When the condition is matched, the hardware stop is enabled	RW

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17.4.19 Hardware Clear Event Selection Register (TIM_HCELR)

Offset	Bit Position																													
0x07C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	CLEARS	Reserved															HCEL15	HCEL14	HCEL13	HCEL12	HCEL11	HCEL10	HCEL9	HCEL8	HCEL7	HCEL6	HCEL5	HCEL4	HCEL3	HCEL2	HCEL1	HCEL0
Access	RW																RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31	CLEARS	Hardware clear enable ● 0b0: Hardware clear is disabled ● 0b1: Hardware clear is enabled **Note** When hardware clear is enabled, the setting of SCLRR is disabled.	RW
30:16	*Reserved*	-	-
15	HCEL15	Hardware clear condition 15 TIMTRID port is sampled to the falling edge ● 0b0: When the condition is matched, the hardware clear is disabled ● 0b1: When the condition is matched, the hardware clear is enabled	RW
14	HCEL14	Hardware clear condition 14 TIMTRID port is sampled to the rising edge ● 0b0: When the condition is matched, the hardware clear is disabled ● 0b1: When the condition is matched, the hardware clear is enabled	RW
13	HCEL13	Hardware clear condition 13 TIMTRIC port is sampled to the falling edge ● 0b0: When the condition is matched, the hardware clear is disabled ● 0b1: When the condition is matched, the hardware clear is enabled	RW
12	HCEL12	Hardware clear condition 12 TIMTRIC port is sampled to the rising edge ● 0b0: When the condition is matched, the hardware clear is disabled ● 0b1: When the condition is matched, the hardware clear is enabled	RW

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Bit	Name	Functional Description	Access
11	HCEL11	Hardware clear condition 11 TIMTRIB port is sampled to the falling edge ● 0b0: When the condition is matched, the hardware clear is disabled ● 0b1: When the condition is matched, the hardware clear is enabled	RW
10	HCEL10	Hardware clear condition 10 TIMTRIB port is sampled to the rising edge ● 0b0: When the condition is matched, the hardware clear is disabled ● 0b1: When the condition is matched, the hardware clear is enabled	RW
9	HCEL9	Hardware clear condition 9 TIMTRIA port is sampled to the falling edge ● 0b0: When the condition is matched, the hardware clear is disabled ● 0b1: When the condition is matched, the hardware clear is enabled	RW
8	HCEL8	Hardware clear condition 8 TIMTRIA port is sampled to the rising edge ● 0b0: When the condition is matched, the hardware clear is disabled ● 0b1: When the condition is matched, the hardware clear is enabled	RW
7	HCEL7	Hardware clear condition 7 CHB port is sampled to the falling edge ● 0b0: When the condition is matched, the hardware clear is disabled ● 0b1: When the condition is matched, the hardware clear is enabled	RW
6	HCEL6	Hardware clear condition 6 CHB port is sampled to the rising edge ● 0b0: When the condition is matched, the hardware clear is disabled ● 0b1: When the condition is matched, the hardware clear is enabled	RW
5	HCEL5	Hardware clear condition 5 CHA port is sampled to the falling edge ● 0b0: When the condition is matched, the hardware clear is disabled ● 0b1: When the condition is matched, the hardware clear is enabled	RW

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Bit	Name	Functional Description	Access
4	HCEL4	Hardware clear condition 4 CHA port is sampled to the rising edge ● 0b0: When the condition is matched, the hardware clear is disabled ● 0b1: When the condition is matched, the hardware clear is enabled	RW
3	HCEL3	Hardware clear condition 3 Event trigger 3 from AOS is enabled ● 0b0: When the condition is matched, the hardware clear is disabled ● 0b1: When the condition is matched, the hardware clear is enabled	RW
2	HCEL2	Hardware clear condition 2 Event trigger 2 from AOS is enabled ● 0b0: When the condition is matched, the hardware clear is disabled ● 0b1: When the condition is matched, the hardware clear is enabled	RW
1	HCEL1	Hardware clear condition 1 Event trigger 1 from AOS is enabled ● 0b0: When the condition is matched, the hardware clear is disabled ● 0b1: When the condition is matched, the hardware clear is enabled	RW
0	HCEL0	Hardware clear condition 0 Event trigger 0 from AOS is enabled ● 0b0: When the condition is matched, the hardware clear is disabled ● 0b1: When the condition is matched, the hardware clear is enabled	RW

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17.4.20 Hardware Capture A Event Selection Register (TIM_HCPAR)

Offset	Bit Position																													
0x080	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																HCPA15	HCPA14	HCPA13	HCPA12	HCPA11	HCPA10	HCPA9	HCPA8	HCPA7	HCPA6	HCPA5	HCPA4	HCPA3	HCPA2	HCPA1	HCPA0
Access																	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15	HCPA15	Hardware capture A condition 15 TIMTRID port is sampled to the falling edge ● 0b0: When the condition is met, hardware capture A is disabled ● 0b1: When the condition is met, hardware capture A is enabled	RW
14	HCPA14	Hardware capture A condition 14 TIMTRID port is sampled to the rising edge ● 0b0: When the condition is met, hardware capture A is disabled ● 0b1: When the condition is met, hardware capture A is enabled	RW
13	HCPA13	Hardware capture A condition 13 TIMTRIC port is sampled to the falling edge ● 0b0: When the condition is met, hardware capture A is disabled ● 0b1: When the condition is met, hardware capture A is enabled	RW
12	HCPA12	Hardware capture A condition 12 TIMTRIC port is sampled to the rising edge ● 0b0: When the condition is met, hardware capture A is disabled ● 0b1: When the condition is met, hardware capture A is enabled	RW
11	HCPA11	Hardware capture A condition 11 TIMTRIB port is sampled to the falling edge ● 0b0: When the condition is met, hardware capture A is disabled ● 0b1: When the condition is met, hardware capture A is enabled	RW
10	HCPA10	Hardware capture A condition 10 TIMTRIB port is sampled to the rising edge ● 0b0: When the condition is met, hardware capture A is disabled ● 0b1: When the condition is met, hardware capture A is enabled	RW
9	HCPA9	Hardware capture A condition 9 TIMTRIA port is sampled to the falling edge ● 0b0: When the condition is met, hardware capture A is disabled ● 0b1: When the condition is met, hardware capture A is enabled	RW

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Bit	Name	Functional Description	Access
8	HCPA8	Hardware capture A condition 8 TIMTRIA port is sampled to the rising edge ● 0b0: When the condition is met, hardware capture A is disabled ● 0b1: When the condition is met, hardware capture A is enabled	RW
7	HCPA7	Hardware capture A condition 7 CHB port is sampled to the falling edge ● 0b0: When the condition is met, hardware capture A is disabled ● 0b1: When the condition is met, hardware capture A is enabled	RW
6	HCPA6	Hardware capture A condition 6 CHB port is sampled to the rising edge ● 0b0: When the condition is met, hardware capture A is disabled ● 0b1: When the condition is met, hardware capture A is enabled	RW
5	HCPA5	Hardware capture A condition 5 CHA port is sampled to the falling edge ● 0b0: When the condition is met, hardware capture A is disabled ● 0b1: When the condition is met, hardware capture A is enabled	RW
4	HCPA4	Hardware capture A condition 4 CHA port is sampled to the rising edge ● 0b0: When the condition is met, hardware capture A is disabled ● 0b1: When the condition is met, hardware capture A is enabled	RW
3	HCPA3	Hardware capture A condition 3 Event trigger 3 from AOS is enabled ● 0b0: When the condition is met, hardware capture A is disabled ● 0b1: When the condition is met, hardware capture A is enabled	RW
2	HCPA2	Hardware capture A condition 2 Event trigger 2 from AOS is enabled ● 0b0: When the condition is met, hardware capture A is disabled ● 0b1: When the condition is met, hardware capture A is enabled	RW
1	HCPA1	Hardware capture A condition 1 Event trigger 1 from AOS is enabled ● 0b0: When the condition is met, hardware capture A is disabled ● 0b1: When the condition is met, hardware capture A is enabled	RW
0	HCPA0	Hardware capture A condition 0 Event trigger 0 from AOS is enabled ● 0b0: When the condition is met, hardware capture A is disabled ● 0b1: When the condition is met, hardware capture A is enabled	RW

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17.4.21 Hardware Capture B Event Selection Register (TIM_HCPBR)

Offset	Bit Position																													
0x084	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																HCPB15	HCPB14	HCPB13	HCPB12	HCPB11	HCPB10	HCPB9	HCPB8	HCPB7	HCPB6	HCPB5	HCPB4	HCPB3	HCPB2	HCPB1	HCPB0
Access																	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15	HCPB15	Hardware capture event B condition 15 TIMTRID port is sampled to the falling edge ● 0b0: When this condition is met, hardware capture B is disabled. ● 0b1: When this condition is met, hardware capture B is enabled	RW
14	HCPB14	Hardware capture event B condition 14 TIMTRID port is sampled to the rising edge ● 0b0: When this condition is met, hardware capture B is disabled ● 0b1: When this condition is met, hardware capture B is enabled	RW
13	HCPB13	Hardware capture event B condition 13 TIMTRIC port is sampled to the falling edge ● 0b0: When this condition is met, hardware capture B is disabled ● 0b1: When this condition is met, hardware capture B is enabled	RW
12	HCPB12	Hardware capture event B condition 12 TIMTRIC port is sampled to the rising edge ● 0b0: When this condition is met, hardware capture B is disabled ● 0b1: When this condition is met, hardware capture B is enabled	RW
11	HCPB11	Hardware capture event B condition 11 TIMTRIB port is sampled to the falling edge ● 0b0: When this condition is met, hardware capture B is disabled ● 0b1: When this condition is met, hardware capture B is enabled	RW
10	HCPB10	Hardware capture event B condition 10 TIMTRIB port is sampled to the rising edge ● 0b0: When this condition is met, hardware capture B is disabled ● 0b1: When this condition is met, hardware capture B is enabled	RW
9	HCPB9	Hardware capture event B condition 9 TIMTRIA port is sampled to the falling edge ● 0b0: When this condition is met, hardware capture B is disabled ● 0b1: When this condition is met, hardware capture B is enabled	RW

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Bit	Name	Functional Description	Access
8	HCPB8	Hardware capture event B condition 8 TIMTRIA port is sampled to the rising edge ● 0b0: When this condition is met, hardware capture B is disabled ● 0b1: When this condition is met, hardware capture B is enabled	RW
7	HCPB7	Hardware capture event B condition 7 CHB port is sampled to the falling edge ● 0b0: When this condition is met, hardware capture B is disabled ● 0b1: When this condition is met, hardware capture B is enabled	RW
6	HCPB6	Hardware capture event B condition 6 CHB port is sampled to the rising edge ● 0b0: When this condition is met, hardware capture B is disabled ● 0b1: When this condition is met, hardware capture B is enabled	RW
5	HCPB5	Hardware capture event B condition 5 CHA port is sampled to the falling edge ● 0b0: When this condition is met, hardware capture B is disabled ● 0b1: When this condition is met, hardware capture B is enabled	RW
4	HCPB4	Hardware capture event B condition 4 CHA port is sampled to the rising edge ● 0b0: When this condition is met, hardware capture B is disabled ● 0b1: When this condition is met, hardware capture B is enabled	RW
3	HCPB3	Hardware capture event B condition 3 Event trigger 3 from AOS is enabled ● 0b0: When this condition is met, hardware capture B is disabled ● 0b1: When this condition is met, hardware capture B is enabled	RW
2	HCPB2	Hardware capture event B condition 2 Event trigger 2 from AOS is enabled ● 0b0: When this condition is met, hardware capture B is disabled ● 0b1: When this condition is met, hardware capture B is enabled	RW
1	HCPB1	Hardware capture event B condition 1 Event trigger 1 from AOS is enabled ● 0b0: When this condition is met, hardware capture B is disabled ● 0b1: When this condition is met, hardware capture B is enabled	RW
0	HCPB0	Hardware capture event B condition 0 Event trigger 0 from AOS is enabled ● 0b0: When this condition is met, hardware capture B is disabled ● 0b1: When this condition is met, hardware capture B is enabled	RW

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17.4.22 Hardware Increment Event Selection Register (TIM_HCUPR)

Offset	Bit Position																													
0x088	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved												HCUP19	HCUP18	HCUP17	HCUP16	HCUP15	HCUP14	HCUP13	HCUP12	HCUP11	HCUP10	HCUP9	HCUP8	HCUP7	HCUP6	HCUP5	HCUP4	HCUP3	HCUP2	HCUP1	HCUP0
Access													RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:20	*Reserved*	-	-
19	HCUP19	Hardware increment condition 19 Event trigger 3 from AOS is enabled ● 0b0: When this condition is met, hardware increment is disabled ● 0b1: When this condition is met, hardware increment is enabled	RW
18	HCUP18	Hardware increment condition 18 Event trigger 2 from AOS is enabled ● 0b0: When this condition is met, hardware increment is disabled ● 0b1: When this condition is met, hardware increment is enabled	RW
17	HCUP17	Hardware increment condition 17 Event trigger 1 from AOS is enabled ● 0b0: When this condition is met, hardware increment is diasbled ● 0b1: When this condition is met, hardware increment is enabled	RW
16	HCUP16	Hardware increment condition 16 Event trigger 0 from AOS is enabled ● 0b0: When this condition is met, hardware increment is disabled ● 0b1: When this condition is met, hardware increment is enabled	RW
15	HCUP15	Hardware increment condition 15 TIMTRID port is sampled to the falling edge ● 0b0: When this condition is met, hardware increment is disabled ● 0b1: When this condition is met, hardware increment is enabled	RW
14	HCUP14	Hardware increment condition 14 TIMTRID port is sampled to the rising edge ● 0b0: When this condition is met, hardware increment is disabled ● 0b1: When this condition is met, hardware increment is enabled	RW
13	HCUP13	Hardware increment condition 13 TIMTRIC port is sampled to the falling edge ● 0b0: When this condition is met, hardware increment is disabled ● 0b1: When this condition is met, hardware increment is enabled	RW

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Bit	Name	Functional Description	Access
12	HCUP12	Hardware increment condition 12 TIMTRIC port is sampled to the rising edge ● 0b0: When this condition is met, hardware increment is disabled ● 0b1: When this condition is met, hardware increment is enabled	RW
11	HCUP11	Hardware increment condition 11 TIMTRIB port is sampled to the falling edge ● 0b0: When this condition is met, hardware increment is disabled ● 0b1: When this condition is met, hardware increment is enabled	RW
10	HCUP10	Hardware increment condition 10 TIMTRIB port is sampled to the rising edge ● 0b0: When this condition is met, hardware increment is disabled ● 0b1: When this condition is met, hardware increment is enabled	RW
9	HCUP9	Hardware increment condition 9 TIMTRIA port is sampled to the falling edge ● 0b0: When this condition is met, hardware increment is diasbled ● 0b1: When this condition is met, hardware increment is enabled	RW
8	HCUP8	Hardware increment condition 8 TIMTRIA port is sampled to the rising edge ● 0b0: When this condition is met, hardware increment is disabled ● 0b1: When this condition is met, hardware increment is enabled	RW
7	HCUP7	Hardware increment condition 7 When the CHB port is high level, the CHA port is sampled to the falling edge ● 0b0: When this condition is met, hardware increment is disabled ● 0b1: When this condition is met, hardware increment is enabled	RW
6	HCUP6	Hardware increment condition 6 When the CHB port is high level, the CHA port is sampled to the rising edge ● 0b0: When this condition is met, hardware increment is disabled ● 0b1: When this condition is met, hardware increment is enabled	RW
5	HCUP5	Hardware increment condition 5 When the CHB port is low level, the CHA port is sampled to the falling edge ● 0b0: When this condition is met, hardware increment is disabled ● 0b1: When this condition is met, hardware increment is enabled	RW
4	HCUP4	Hardware increment condition 4 When the CHB port is low level, the CHA port is sampled to the rising edge ● 0b0: When this condition is met, hardware increment is disabled ● 0b1: When this condition is met, hardware increment is enabled	RW

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Bit	Name	Functional Description	Access
3	HCUP3	Hardware increment condition 3 When the CHA port is high level, the CHB port is sampled to the falling edge ● 0b0: When this condition is met, hardware increment is disabled ● 0b1: When this condition is met, hardware increment is enabled	RW
2	HCUP2	Hardware increment condition 2 When the CHA port is high level, the CHB port is sampled to the rising edge ● 0b0: When this condition is met, hardware increment is disabled ● 0b1: When this condition is met, hardware increment is enabled	RW
1	HCUP1	Hardware increment condition 1 When the CHA port is low level, the CHB port is sampled to the falling edge ● 0b0: When this condition is met, hardware increment is disabled ● 0b1: When this condition is met, hardware increment is enabled	RW
0	HCUP0	Hardware increment condition 0 When the CHA port is low level, the CHB port is sampled to the rising edge ● 0b0: When this condition is met, hardware increment is disabled ● 0b1: When this condition is met, hardware increment is enabled	RW

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17.4.23 Hardware Decrement Event Selection Register (TIM_HCDOR)

Offset	Bit Position																													
0x08C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved												HCDO19	HCDO18	HCDO17	HCDO16	HCDO15	HCDO14	HCDO13	HCDO12	HCDO11	HCDO10	HCDO9	HCDO8	HCDO7	HCDO6	HCDO5	HCDO4	HCDO3	HCDO2	HCDO1	HCDO0
Access													RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:20	*Reserved*	-	-
19	HCDO19	Hardware decrement condition 19 Event trigger 3 from AOS is enabled ● 0b0: Hardware increment is disabled when the condition is met ● 0b1: Hardware increment is enabled when the condition is met	RW
18	HCDO18	Hardware decrement condition 18 Event trigger 2 from AOS is enabled ● 0b0: Hardware increment is disabled when the condition is met ● 0b1: Hardware increment is enabled when the condition is met	RW
17	HCDO17	Hardware decrement condition 17 Event trigger 1 from AOS is enabled ● 0b0: Hardware increment is disabled when the condition is met ● 0b1: Hardware increment is enabled when the condition is met	RW
16	HCDO16	Hardware decrement condition 16 Event trigger 0 from AOS is enabled ● 0b0: Hardware increment is disabled when the condition is met ● 0b1: Hardware increment is enabled when the condition is met	RW
15	HCDO15	Hardware decrement condition 15 TIMTRID port is sampled to the falling edge ● 0b0: Hardware increment is disabled when the condition is met ● 0b1: Hardware increment is enabled when the condition is met	RW
14	HCDO14	Hardware decrement condition 14 TIMTRID port is sampled to the rising edge ● 0b0: Hardware increment is disabled when the condition is met ● 0b1: Hardware increment is enabled when the condition is met	RW
13	HCDO13	Hardware decrement condition 13 TIMTRIC port is sampled to the falling edge ● 0b0: Hardware increment is disabled when the condition is met ● 0b1: Hardware increment is enabled when the condition is met	RW

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Bit	Name	Functional Description	Access
12	HCDO12	Hardware decrement condition 12 TIMTRIC port is sampled to the rising edge ● 0b0: Hardware increment is disabled when the condition is met ● 0b1: Hardware increment is enabled when the condition is met	RW
11	HCDO11	Hardware decrement condition 11 TIMTRIB port is sampled to the falling edge ● 0b0: Hardware increment is disabled when the condition is met ● 0b1: Hardware increment is enabled when the condition is met	RW
10	HCDO10	Hardware decrement condition 10 TIMTRIB port is sampled to the rising edge ● 0b0: Hardware increment is disabled when the condition is met ● 0b1: Hardware increment is enabled when the condition is met	RW
9	HCDO9	Hardware decrement condition 9 TIMTRIA port is sampled to the falling edge ● 0b0: Hardware increment is disabled when the condition is met ● 0b1: Hardware increment is enabled when the condition is met	RW
8	HCDO8	Hardware decrement condition 8 TIMTRIA port is sampled to the rising edge ● 0b0: Hardware increment is disabled when the condition is met ● 0b1: Hardware increment is enabled when the condition is met	RW
7	HCDO7	Hardware decrement condition 7 When the CHB port is high level, the CHA port is sampled to the falling edge ● 0b0: Hardware increment is disabled when the condition is met ● 0b1: Hardware increment is enabled when the condition is met	RW
6	HCDO6	Hardware decrement condition 6 When the CHB port is high level, the CHA port is sampled to the rising edge ● 0b0: Hardware increment is disabled when the condition is met ● 0b1: Hardware increment is enabled when the condition is met	RW
5	HCDO5	Hardware decrement condition 5 When the CHB port is low level, the CHA port is sampled to the falling edge ● 0b0: Hardware increment is disabled when the condition is met ● 0b1: Hardware increment is enabled when the condition is met	RW
4	HCDO4	Hardware decrement condition 4 When the CHB port is low level, the CHA port is sampled to the rising edge ● 0b0: Hardware increment is disabled when the condition is met ● 0b1: Hardware increment is enabled when the condition is met	RW

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Bit	Name	Functional Description	Access
3	HCDO3	Hardware decrement condition 3 When the CHA port is high level, the CHB port is sampled to the falling edge ● 0b0: Hardware increment is disabled when the condition is met ● 0b1: Hardware increment is enabled when the condition is met	RW
2	HCDO2	Hardware decrement condition 2 When the CHA port is high level, the CHB port is sampled to the rising edge ● 0b0: Hardware increment is disabled when the condition is met ● 0b1: Hardware increment is enabled when the condition is met	RW
1	HCDO1	Hardware decrement condition 1 When the CHA port is low level, the CHB port is sampled to the falling edge ● 0b0: Hardware increment is disabled when the condition is met ● 0b1: Hardware increment is enabled when the condition is met	RW
0	HCDO0	Hardware decrement condition 0 When the CHA port is low level, the CHB port is sampled to the rising edge ● 0b0: Hardware increment is disabled when the condition is met ● 0b1: Hardware increment is enabled when the condition is met	RW

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17.4.24 Software Synchronization Start Register (TIM_SSTAR)

Offset	Bit Position																													
0x3F4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																													SSTA2	SSTA1	SSTA0
Access																														RW	RW	RW

Bit	Name	Functional Description	Access
31:3	*Reserved*	-	-
2	SSTA2	Timer6 software start ● 0b0: Software start is disabled ● 0b1: Software start is enabled	RW
1	SSTA1	Timer5 software start ● 0b0: Software start is disabled ● 0b1: Software start is enabled	RW
0	SSTA0	Timer4 software start ● 0b0: Software start is disabled ● 0b1: Software start is enabled	RW

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17.4.25 Software Synchronization Stop Register (TIM_SSTPR)

Offset	Bit Position																													
0x3F8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																													SSTP2	SSTP1	SSTP0
Access																														RW	RW	RW

Bit	Name	Functional Description	Access
31:3	*Reserved*	-	-
2	SSTP2	Timer6 software stop ● 0b0: Software stop is disabled ● 0b1: Software stop is enabled	RW
1	SSTP1	Timer5 software stop ● 0b0: Software stop is disabled ● 0b1: Software stop is enabled	RW
0	SSTP0	Timer4 software stop ● 0b0: Software stop is disabled ● 0b1: Software stop is enabled	RW

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17.4.26 Software Synchronization Clear Register (TIM_SCLRR)

Offset	Bit Position																													
0x3FC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																													SCLR2	SCLR1	SCLR0
Access																														RW	RW	RW

Bit	Name	Functional Description	Access
31:3	*Reserved*	-	-
2	SCLR2	Timer6 software clear ● 0b0: Software clear is disabled ● 0b1: Software clear is enabled	RW
1	SCLR1	Timer5 software clear ● 0b0: Software clear is disabled ● 0b1: Software clear is enabled	RW
0	SCLR0	Timer4 software clear ● 0b0: Software clear is disabled ● 0b1: Software clear is enabled	RW

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17.4.27 Interrupt Flag Register (TIM_IFR)

Offset	Bit Position																													
0x100	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																SAMHF	SAMLF	Reserved					DTEF	UDFF	OVFF	Reserved		CMDF	CMCF	CMBF	CMAF
Access																	RO	RO						RO	RO	RO			RO	RO	RO	RO

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15	SAMHF	CHA/B port high-level interrupt flag ● 0b0: High level not simultaneously present on both CHA and CHB ports ● 0b1: High level simultaneously present on both CHA and CHB ports	RO
14	SAMLF	CHA/B port low-level interrupt flag ● 0b0: Low level not simultaneously present on both CHA and CHB ports ● 0b1: Low level simultaneously present on both CHA and CHB ports	RO
13:9	*Reserved*	-	-
8	DTEF	Dead time error interrupt flag ● 0b0: No dead zone time error occurred ● 0b1: Dead zone time error occurred	RO
7	UDFF	Underflow match interrupt flag ● 0b0: No sawtooth wave underflow or triangular wave counting to the valley point occurred ● 0b1: Sawtooth wave underflow or triangular wave counting to the valley point occurred	RO
6	OVFF	Overflow match interrupt flag ● 0b0: No sawtooth wave overflow or triangular wave counting to the peak point occurred ● 0b1: Sawtooth wave overflow or triangular wave counting to the peak point occurred	RO
5:4	*Reserved*	-	-
3	CMDF	Counting match D interrupt flag ● 0b0: The value in the GCMDR register does not match the count value ● 0b1: The value in the GCMDR register matches the count value	RO

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Bit	Name	Functional Description	Access
2	CMCF	Counting match C interrupt flag ● 0b0: The value in the GCMCR register does not match the count value ● 0b1: The value in the GCMCR register matches the count value	RO
1	CMBF	Counting match B interrupt flag ● 0b0: The value of GCMBR register does not match the count value, and no CHB capture completion action has occurred ● 0b1: The value of GCMBR register equals the count value, or a CHB capture completion action occurs	RO
0	CMAF	Counting match A interrupt flag ● 0b0: The value of GCMAR register does not match the count value, and no CHA capture completion action has occurred ● 0b1: The value of GCMAR register equals the count value, or a CHA capture completion action occurs	RO

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17.4.28 Interrupt Flag Clear Register (TIM_ICLR)

Offset	Bit Position																													
0x104	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000FFFF																															
Name	Reserved																SAMHC	SAMLC	Reserved					DTEC	UDFC	OVFC	Reserved		CMDC	CMCC	CMBC	CMAC
Access																	WO	WO						WO	WO	WO			WO	WO	WO	WO

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15	SAMHC	CHA/B port high-level interrupt flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
14	SAMLC	CHA/B port low-level interrupt flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
13:9	*Reserved*	-	-
8	DTEC	Dead time error interrupt flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
7	UDFC	Underflow match interrupt flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
6	OVFC	Overflow match interrupt flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
5:4	*Reserved*	-	-
3	CMDC	Counting match D interrupt flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
2	CMCC	Counting match C interrupt flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
1	CMBC	Counting match B interrupt flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
0	CMAC	Counting match A interrupt flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO

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17.4.29 Spread Spectrum and Trigger Selection Register (TIM_CR)

Offset	Bit Position																													
0x108	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000300																															
Name	Reserved									DMA_S_CMB	DMA_S_CMA	DMA_G_UDF	DMA_G_OVF	Reserved		DMA_G_CMD	DMA_G_CMC	DMA_G_CMB	DMA_G_CMA	CMSBE	CMSAE	DITENS	DITENB	DITENA	UDFE	OVFE	Reserved		CMDE	CMCE	CMBE	CMAE
Access										RW	RW	RW	RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW			RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:23	*Reserved*	-	-
22	DMA_S_CMB	Dedicated count compare match B enable DMA ● 0b0: Disable ● 0b1: Enabled, this match can trigger DMA **Note** When configuring DMA_S_CMB to trigger DMA, it is also necessary to configure ICONR.INTENSBU or ICONR.INTENSBD according to the counting direction.	RW
21	DMA_S_CMA	Dedicated count compare match A enable DMA ● 0b0: Disable ● 0b1: Enabled, this match can trigger DMA **Note** When configuring DMA_S_CMB to trigger DMA, it is also necessary to configure ICONR.INTENSAU or ICONR.INTENSAD according to the counting direction.	RW
20	DMA_G_UDF	Underflow match enable DMA ● 0b0: Disable ● 0b1: Enabled, this match can trigger DMA	RW
19	DMA_G_OVF	Overflow match enable to DMA ● 0b0: Disable ● 0b1: Enabled, this match can trigger DMA	RW
18:17	*Reserved*	-	-
16	DMA_G_CMD	General counting compare match D enable DMA ● 0b0: Disable ● 0b1: Enabled, this match can trigger DMA	RW
15	DMA_G_CMC	General counting compare match C enable DMA ● 0b0: Disable ● 0b1: Enabled, this match can trigger DMA	RW

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Bit	Name	Functional Description	Access
14	DMA_G_CMB	General counting compare match B enable DMA ● 0b0: Disable ● 0b1: Enabled, this match can trigger DMA	RW
13	DMA_G_CMA	General counting compare match A enable DMA ● 0b0: Disable ● 0b1: Enabled, this match can trigger DMA	RW
12	CMSBE	Dedicated count compare match B enable trigger ADC/AOS ● 0b0: Disable ● 0b1: Enabled, this match can output AOS trigger signal or trigger ADC **Note** When configuring CMSBE to output AOS or trigger ADC, it is also necessary to configure ICONR.INTENSBU or ICONR.INTENSBD according to the counting direction.	RW
11	CMSAE	Dedicated count compare match A enable ADC/AOS trigger ● 0b0: Disable ● 0b1: Enabled, this match can output AOS trigger signal or trigger ADC **Note** When configuring CMSAE to output AOS or trigger ADC, it is also necessary to configure ICONR.INTENSAU or ICONR.INTENSAD according to the counting direction.	RW
10	DITENS	PWM spread spectrum count selection ● 0b0: select underflow ● 0b1: select overflow	RW
9	DITENB	PWM channel B spread spectrum enable ● 0b0: Disable ● 0b1: Enabled, changes the PWM output delay every cycle	RW
8	DITENA	PWM channel A spread spectrum enable ● 0b0: Disable ● 0b1: Enabled, changes the PWM output delay every cycle	RW
7	UDFE	Underflow match enable to trigger ADC/AOS ● 0b0: Disable ● 0b1: Enabled, this match can output AOS trigger signal or trigger ADC	RW
6	OVFE	Overflow match enable to trigger ADC/AOS ● 0b0: Disable ● 0b1: Enabled, this match can output AOS trigger signal or trigger ADC	RW
5:4	*Reserved*	-	-

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Bit	Name	Functional Description	Access
3	CMDE	General count compare match D enable to trigger ADC/AOS ● 0b0: Disable ● 0b1: Enabled, this match can output AOS trigger signal or trigger ADC	RW
2	CMCE	General count compare match C enable to trigger ADC/AOS ● 0b0: Disable ● 0b1: Enabled, this match can output AOS trigger signal or trigger ADC	RW
1	CMBE	General count compare match B enable to trigger ADC/AOS ● 0b0: Disable ● 0b1: Enabled, this match can output AOS trigger signal or trigger ADC	RW
0	CMAE	General count compare match A enable to trigger ADC/AOS ● 0b0: Disable ● 0b1: Enabled, this match can output AOS trigger signal or trigger ADC	RW

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17.4.30 AOS Selection Control Register (TIM_AOSSR)

Offset	Bit Position																													
0x110	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																		SMH2	SMH1	SMH0	SML2	SML1	SML0	SOFTBK	Reserved		BFILTEN	BFILTS		FSAME	FBRAKE
Access																			RW	RW	RW	RW	RW	RW	RW			RW	RW		RO	RO

Bit	Name	Functional Description	Access
31:14	*Reserved*	-	-
13	SMH2	Channel 2 high-level coincidence selection ● 0b0: Selection is disabled ● 0b1: Selection is enabled, AOS_i_odis[1] triggers when high-level coincidence occurs	RW
12	SMH1	Channel 1 high-level coincidence selection ● 0b0: Selection is disabled ● 0b1: Selection is enabled, AOS_i_odis[1] triggers when high-level coincidence occurs	RW
11	SMH0	Channel 0 high-level coincidence selection ● 0b0: Selection is disabled ● 0b1: Selection is enabled, AOS_i_odis[1] triggers when high-level coincidence occurs	RW
10	SML2	Channel 2 low-level coincidence selection ● 0b0: Selection is disabled ● 0b1: Selection is enabled, and AOS_i_odis[1] triggers when high-level coincidence occurs	RW
9	SML1	Channel 1 low-level coincidence selection ● 0b0: Selection is disabled ● 0b1: Selection is enabled, and AOS_i_odis[1] triggers when high-level coincidence occurs	RW
8	SML0	Channel 0 low-level coincidence selection ● 0b0: Selection is disabled ● 0b1: Selection is enabled, and AOS_i_odis[1] triggers when high-level coincidence occurs	RW
7	SOFTBK	Software brake ● 0b0: Disable ● 0b1: Enable	RW
6:5	*Reserved*	-	-
4	BFILTEN	Port brake filter enable ● 0b0: Disable ● 0b1: Enable	RW

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Bit	Name	Functional Description	Access
3:2	BFILTS	Port brake filter clock selection ● 0b00: PCLK0 ● 0b01: PCLK0/4 ● 0b10: PCLK0/16 ● 0b11: PCLK0/64	RW
1	FSAME	High/low coincidence brake flag ● 0b0: No high/low coincidence braking occurred ● 0b1: High/low coincidence braking occurred	RO
0	FBRAKE	Port brake flag ● 0b0: Port braking not occurred ● 0b1: Port braking occurred	RO

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17.4.31 AOS Selection Control Flag Clear Register (TIM_AOSCL)

Offset	Bit Position																													
0x114	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000003																															
Name	Reserved																														FSAME	FBRAKE
Access																															WO	WO

Bit	Name	Functional Description	Access
31:2	*Reserved*	-	-
1	FSAME	High/low coincidence brake flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
0	FBRAKE	Port brake flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO

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17.4.32 Port Brake Control Register (TIM_PTBKS)

Offset	Bit Position																													
0x118	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																	EN14	EN13	EN12	EN11	EN10	EN9	EN8	Reserved	EN6	EN5	EN4	EN3	EN2	EN1	EN0
Access																		RW	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:15	*Reserved*	-	-
14	EN14	PC15 brake port enable ● 0b0: Disable ● 0b1: Enable	RW
13	EN13	PB15 brake port enable ● 0b0: Disable ● 0b1: Enable	RW
12	EN12	PA15 brake port enable ● 0b0: Disable ● 0b1: Enable	RW
11	EN11	PD1 brake port enable ● 0b0: Disable ● 0b1: Enable	RW
10	EN10	PC11 brake port enable ● 0b0: Disable ● 0b1: Enable	RW
9	EN9	PB11 brake port enable ● 0b0: Disable ● 0b1: Enable	RW
8	EN8	PA11 brake port enable ● 0b0: Disable ● 0b1: Enable	RW
7	*Reserved*	-	-
6	EN6	PC7 brake port enable ● 0b0: Disable ● 0b1: Enable	RW
5	EN5	PB7 brake port enable ● 0b0: Disable ● 0b1: Enable	RW

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Bit	Name	Functional Description	Access
4	EN4	PA7 brake port enable ● 0b0: Disable ● 0b1: Enable	RW
3	EN3	PD3 brake port enable ● 0b0: Disable ● 0b1: Enable	RW
2	EN2	PC3 brake port enable ● 0b0: Disable ● 0b1: Enable	RW
1	EN1	PB3 brake port enable ● 0b0: Disable ● 0b1: Enable	RW
0	EN0	PA3 brake port enable ● 0b0: Disable ● 0b1: Enable	RW

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17.4.33 Port Trigger Control Register (TIM_TTRIG)

Offset	Bit Position																													
0x11C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																TRIGDS				TRIGCS				TRIGBS				TRIGAS			
Access																	RW				RW				RW				RW			

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:12	TRIGDS	TIMx triggers D port selection Parameter selection details (see table below)	RW
11:8	TRIGCS	TIMx triggers C port selection Parameter selection details (see table below)	RW
7:4	TRIGBS	TIMx triggers B port selection Parameter selection details (see table below)	RW
3:0	TRIGAS	TIMx triggers A port selection Parameter selection details (see table below)	RW

Table 17-71 Port Trigger Selection

	TRIGD	TRIGC	TRIGB	TRIGA
Select Control Signal	TTRIG.TRIGDS	TTRIG.TRIGCS	TTRIG.TRIGBS	TTRIG.TRIGAS
0b0000	PA3	PA3	PA3	PA3
0b0001	PB3	PB3	PB3	PB3
0b0010	PC3	PC3	PC3	PC3
0b0011	PD3	PD3	PD3	PD3
0b0100	PA7	PA7	PA7	PA7
0b0101	PB7	PB7	PB7	PB7
0b0110	PC7	PC7	PC7	PC7
0b0111	Reserved	Reserved	Reserved	Reserved
0b1000	PA11	PA11	PA11	PA11
0b1001	PB11	PB11	PB11	PB11
0b1010	PC11	PC11	PC11	PC11
0b1011	PD1	PD1	PD1	PD1
0b1100	PA15	PA15	PA15	PA15

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	TRIGD	TRIGC	TRIGB	TRIGA
Select Control Signal	TTRIG.TRIGDS	TTRIG.TRIGCS	TTRIG.TRIGBS	TTRIG.TRIGAS
0b1101	PB15	PB15	PB15	PB15
0b1110	PC15	PC15	PC15	PC15
0b1111	Reserved	Reserved	Reserved	Reserved

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17.4.34 AOS Trigger Control Register (TIM_ITRIG)

Offset	Bit Position																													
0x120	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																IAOS3S				IAOS2S				IAOS1S				IAOS0S			
Access																	RW				RW				RW				RW			

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:12	IAOS3S	TIMx AOS3 trigger source selection Parameter selection details (see table below)	RW
11:8	IAOS2S	TIMx AOS2 trigger source selection Parameter selection details (see table below)	RW
7:4	IAOS1S	TIMx AOS1 trigger source selection Parameter selection details (see table below)	RW
3:0	IAOS0S	TIMx AOS0 trigger source selection Parameter selection details (see table below)	RW

Table 17-74 AOS Source Selection

	AOS_i_trig3	AOS_i_trig2	AOS_i_trig1	AOS_i_trig0
Select Control Signal	ITRIG.IAOS3S	ITRIG.IAOS2S	ITRIG.IAOS1S	ITRIG.IAOS0S
0b0000	TIM0_INT	TIM0_INT	TIM0_INT	TIM0_INT
0b0001	TIM1_INT	TIM1_INT	TIM1_INT	TIM1_INT
0b0010	TIM2_INT	TIM2_INT	TIM2_INT	TIM2_INT
0b0011	LPTIMER_INT	LPTIMER_INT	LPTIMER_INT	LPTIMER_INT
0b0100	TIM4_INTS	TIM4_INTS	TIM4_INTS	TIM4_INTS
0b0101	TIM5_INTS	TIM5_INTS	TIM5_INTS	TIM5_INTS
0b0110	TIM6_INTS	TIM6_INTS	TIM6_INTS	TIM6_INTS
0b0111	UART0_INT	UART0_INT	UART0_INT	UART0_INT
0b1000	UART1_INT	UART1_INT	UART1_INT	UART1_INT
0b1001	LPUART0_INT	LPUART0_INT	LPUART0_INT	LPUART0_INT
0b1010	VC0_INT	VC0_INT	VC0_INT	VC0_INT
0b1011	VC1_INT	VC1_INT	VC1_INT	VC1_INT
0b1100	RTC_INT	RTC_INT	RTC_INT	RTC_INT

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	AOS_i_trig3	AOS_i_trig2	AOS_i_trig1	AOS_i_trig0
Select Control Signal	ITRIG.IAOS3S	ITRIG.IAOS2S	ITRIG.IAOS1S	ITRIG.IAOS0S
0b1101	PCA_INT	PCA_INT	PCA_INT	PCA_INT
0b1110	SPI_INT	SPI_INT	SPI_INT	SPI_INT
0b1111	ADC_INT	ADC_INT	ADC_INT	ADC_INT

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17.4.35 Port Brake Polarity Control Register (TIM_PTBKP)

Offset	Bit Position																													
0x124	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																	POL14	POL13	POL12	POL11	POL10	POL9	POL8	Reserved	POL6	POL5	POL4	POL3	POL2	POL1	POL0
Access																		RW	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:15	*Reserved*	-	-
14	POL14	PC15 brake port polarity selection ● 0b0: High level is enabled ● 0b1: Low level is enabled	RW
13	POL13	PB15 brake port polarity selection ● 0b0: High level is enabled ● 0b1: Low level is enabled	RW
12	POL12	PA15 brake port polarity selection ● 0b0: High level is enabled ● 0b1: Low level is enabled	RW
11	POL11	PD1 brake port polarity selection ● 0b0: High level is enabled ● 0b1: Low level is enabled	RW
10	POL10	PC11 brake port polarity selection ● 0b0: High level is enabled ● 0b1: Low level is enabled	RW
9	POL9	PB11 brake port polarity selection ● 0b0: High level is enabled ● 0b1: Low level is enabled	RW
8	POL8	PA11 brake port polarity selection ● 0b0: High level is enabled ● 0b1: Low level is enabled	RW
7	*Reserved*	-	-
6	POL6	PC7 brake port polarity selection ● 0b0: High level is enabled ● 0b1: Low level is enabled	RW
5	POL5	PB7 brake port polarity selection ● 0b0: High level is enabled ● 0b1: Low level is enabled	RW

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Bit	Name	Functional Description	Access
4	POL4	PA7 brake port polarity selection ● 0b0: High level is enabled ● 0b1: Low level is enabled	RW
3	POL3	PD3 brake port polarity selection ● 0b0: High level is enabled ● 0b1: Low level is enabled	RW
2	POL2	PC3 brake port polarity selection ● 0b0: High level is enabled ● 0b1: Low level is enabled	RW
1	POL1	PB3 brake port polarity selection ● 0b0: High level is enabled ● 0b1: Low level is enabled	RW
0	POL0	PA3 brake port polarity selection ● 0b0: High level is enabled ● 0b1: Low level is enabled	RW

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18 RTC

18.1 Introduction

The Real Time Counter provides seconds, minutes, hours, day, week, month, and year information, and the number of days in a month and leap year can be automatically adjusted. Clock operation can be done in 24 or 12 hour format via the RTC_CR0. AMPM register bit. It provides a periodic interrupt with a minimum period of 0.5s. For shorter interrupt period, please use the LPTIM to generate interrupt.

18.2 Features

Table 18-1 Basic Features of RTC

Basic Features	Description
Clock source	Off-chip low-speed crystal oscillator XTL (32.768kHz) On-chip low-speed oscillator RCL (32.768kHz) Off-chip high-speed crystal oscillator XTH
Basic function	Can calculate seconds, minutes, hours, days, weeks, months, years between 00 and 99
	Automatic leap year adjustment
	Configurable to 24 or 12 hour format
	Programmable start or stop
	Provides alarm functions
	With high-precision 1Hz square wave signal output
Interrupt	Periodic interrupt with a minimum period of 0.5s
	Alarm interrupt with down-to-the-second precision

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18.3 Functional Description

The clock source of the Real Time Counter can be configured as an external low-speed crystal oscillator, an external high-speed crystal oscillator, or the internal low-speed clock RCL; by default, the external low-speed crystal oscillator is used. The control registers RTC_CR0, RTC_CR1 and RTC_COMPEN are only controlled by power-on reset, and other reset sources cannot reset these three control registers. The power-on status of other data registers is uncertain, and needs to be initialized after power-on, and will not be affected by any reset.

All date and time values written to or read from software are in BCD format and do not require hexadecimal-to-decimal conversion.

Any invalid date time will not be able to be written, such as 32nd day, 25th hour, 70th second, month B, etc.

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18.3.1 Function Block Diagram

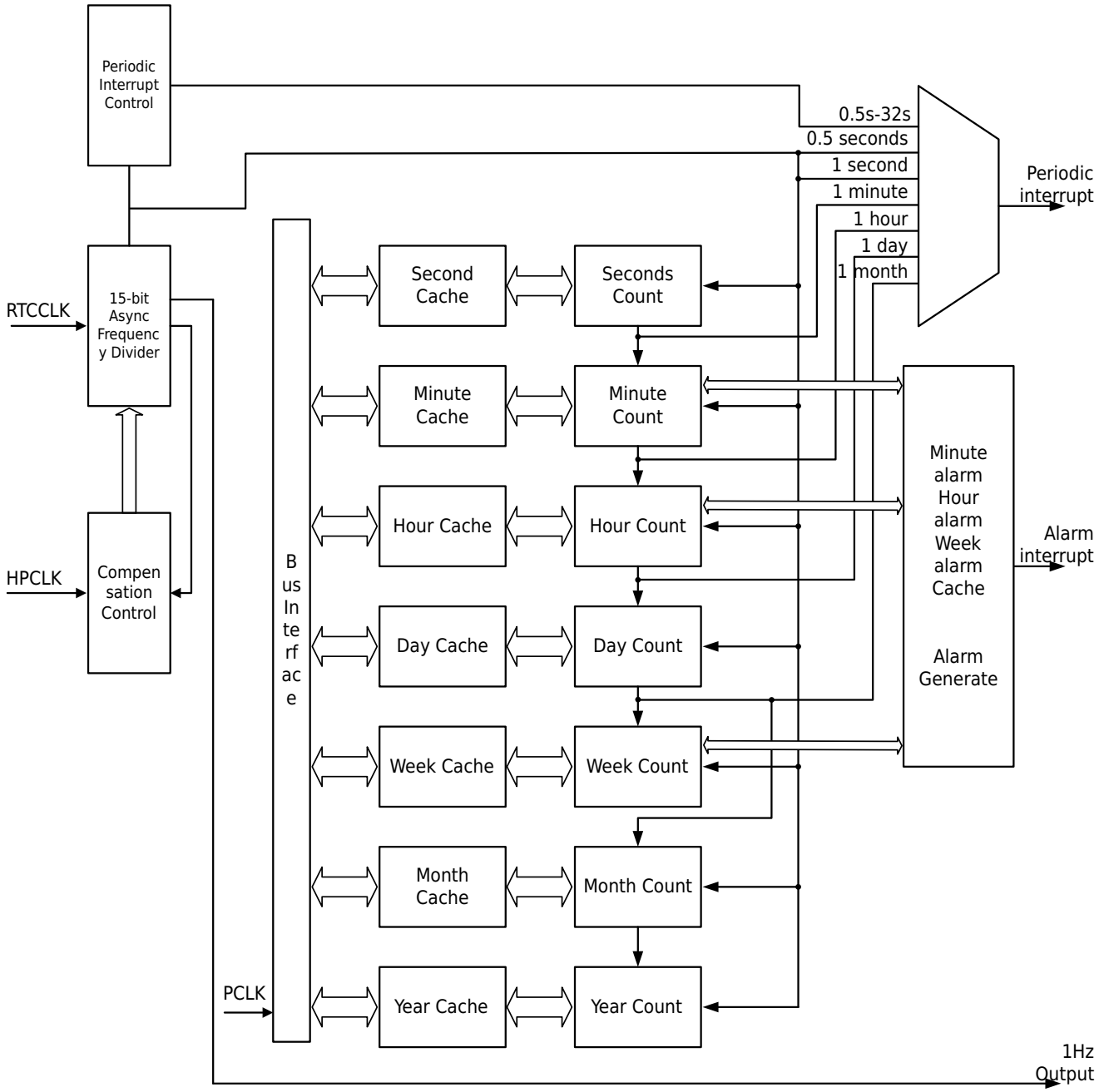

Figure 18-1 RTC Block Diagram

18.3.2 Power-on Setting

The RTC is reset once after power-on. When the system remains powered, no external reset requests can reset the RTC. The RTC will continue counting without interruption. After power-on, configure the initial calendar values, alarm settings, error compensation, and interrupts, and then start the RTC.

18.3.3 System Low Power Mode Switching

After the RTC starts counting, if the system needs to immediately switch to low power mode, please perform any of the following confirmations before switching modes (controlled via the SYSCTRL1.RTC_LPW register):

- After setting RTC_CR0.START=1, switch modes after more than 2 RTC count clocks.

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- After setting RTC_CR0.START=1, set RTC_CR1.WAIT=1, wait until RTC_CR1.WAITF=1, then set RTC_CR1.WAIT=0, and confirm that RTC_CR1.WAITF=0 before switching modes.

In RTC low power mode, RTC registers cannot be read or written. In low power mode, the RTC consumes less current. Switching low power mode while RTC is running does not need to wait.

18.3.4 Clock Error Compensation

Due to the inherent error in the external crystal oscillator, compensation is required to achieve high-precision counting results. Two compensation methods are available: one based on the internal clock RTCCLK error compensation; and the other based on high-speed clock HPCLK error compensation.

Principle and Calculation of Internal Clock Error Compensation

Since the counter uses a 32.768kHz clock to count, if it is necessary to compensate the precision per second, it can only be compensated according to the integer period of 32.768kHz, and the minimum unit of compensation per second is (1/32768) ×10^6=30.5ppm, unable to meet the high precision requirements.

Then, when realizing high-precision clock compensation under the counting clock of 32.768kHz, it is necessary to adjust the algorithm to expand the maximum compensation period by 32 times. Then, when the minimum unit that can only be compensated is 30.5ppm, the average compensation unit per second becomes 30.5ppm/32=0.96ppm. To meet the requirements of higher precision clock compensation and ensure the compensation is distributed evenly within each 32-second interval, this register introduces a setting with 5 fractional bits.

For example, when the 1Hz clock is directly output in the default state, the compensation target value is calculated by measuring the accuracy of the clock.

Assuming that the actual measured value is 1.0000203Hz, then:

Actual Vibration Frequency = 32768 × 1.0000203 ≈ 32768.6651904 (actual oscillation frequency needs to be accurate to at least three decimal places)

$$\begin{aligned}\text{Compensation Target Value} &= (\text{Actual Vibration Frequency} - \text{Target Frequency})/\text{Target Frequency} \times 10^6 \\ &= (32768.6651904 - 32768)/32768 \times 10^6 \\ &= 20.3\text{ppmppm}\end{aligned}$$

Based on the formula:

$$\text{CR}[8:0] = \left(\frac{\text{Compensation Target Value [ppm]} \times 2^{15}}{10^6}\right)_{\text{Take 2's complement}} + 0001.00000B$$

If the compensation target value is +20.3ppm, calculate the corresponding register value as follows:

$$\begin{aligned}\text{CR}[8:0] &= (20.3 \times 2^{15}/10^6)_{\text{Take 2's complement}} + 0001.00000\text{B} \\ &= (0.6651904)_{\text{Take 2's complement}} + 0001.00000\text{B} \\ &= 0000.10101\text{B} + 0001.00000\text{B} \\ &= 0001.10101\text{B}\end{aligned}$$

If the compensation target value is -20.3ppm, calculate the corresponding register value as follows:

$$\begin{aligned}\text{CR}[8:0] &= (-20.3 \times 2^{15}/10^6)_{\text{Take 2's complement}} + 0001.00000\text{B} \\ &= (-0.6651904)_{\text{Take 2's complement}} + 0001.00000\text{B} \\ &= 1111.01011\text{B} + 0001.00000\text{B} \\ &= 0000.01011\text{B}\end{aligned}$$

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Principle and Calculation of Error Compensation Based on High-Speed 24MHz Clock:

The calculation method of this method is the same as the error compensation based on its own clock. Due to the introduction of the high-speed clock HPCLK (XTH external high-speed clock), the 1/32768 second error that originally needs to be accumulated within a maximum of 32 seconds can be dispersed to every 1 second, minimum 0.96ppm (23 clock cycles at 24MHz) compensation for every 1 second, achieving an average high-precision 1Hz clock output per second.

18.3.5 RTC Interrupt

The RTC supports two types of interrupts: alarm interrupt and fixed-period interrupt. The alarm interrupt and the fixed-period interrupt share an interrupt signal.

Alarm Interrupt

When RTC_CR1.ALMIE=1, if the current calendar time is equal to the second alarm register (RTC_ALMSEC), minute alarm register (RTC_ALMMIN), hour alarm register (RTC_ALMHOUR), and weekly alarm register (RTC_ALMWEEK), an alarm interrupt is triggered.

Periodic Interrupt

When RTC_CR1.ALMIE=1, a fixed-period wake-up interrupt is triggered after the selected period occurs. Since the alarm and fixed-period interrupts share the same interrupt, they are distinguished by flag register bits.

18.4 Operation Example

18.4.1 RTC Count Start Setting

Procedure

Step1. Set RTC_CR0.START=0 to stop counting.

Step2. Set RTC_CR0.AMPM and RTC_CR0.PRDS; RTC_CR0.PRDX configures the time format and interrupt period.

Step3. Set RTC_CR1.CKSEL to select the RTC timing clock.

Step4. Set the calendar counter registers for seconds, minutes, hours, week, day, month, and year.

Step5. When clock error compensation is required, set the counting clock error compensation register RTC_COMPEN.

Step6. Clear the interrupt flag bits RTC_CR1.ALMF amd RTC_CR1.PRDF, and enable the interrupts.

Step7. Set RTC_CR0.START=1 to start counting.

18.4.2 Read Count Register

Context

There are three methods to read the count register.

Procedure

- **Read Method 1 at Any Time**

  Step1. Set RTC_CR1.WAIT=1 to stop the calendar register counting and enter read/write mode.

  Step2. Query until RTC_CR1.WAITF=1.

  Step3. Read the values of the second, minute, hour, week, day, month, and year count registers.

  Step4. Set RTC_CR1.WAIT=0 to start the counter counting.

  Step5. Query until RTC_CR1.WAITF=0.

- **Read Method 2 at Any Time**

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Step1. Read minutes, hours, weeks, days, months, and year count register values.

Step2. Read out the second count register value.

Step3. Read the second count register value again.

Step4. Judging whether the reading values of the two seconds are the same, if they are different, start from the first step again, if the same, end read.

- **Interrupt Read Method**

  Read the second, minute, hour, week, day, month, year count register value in the RTC cycle interrupt service. Because after the interrupt occurs, it will take at least 0.5s for the next data change.

18.4.3 Write Count Register

Context

Changing the seconds register in the counting mode will reset the seconds counting, writing minutes, hours, weeks, days, months, years count register values will not affect the RTC counting.

> **Note**
> WAIT is not required to write seconds, minutes, hours, weeks, days, months, and year count registers in RTC disabled mode.

Procedure

Step1. Set RTC_CR1.WAIT=1, stop the calendar register counting, and enter the read and write mode.

Step2. Query until RTC_CR1.WAITF=1.

Step3. Write the second, minute, hour, week, day, month, year count register value.

Step4. Set RTC_CR1.WAIT=0, the counter starts counting again.

> **Notice**
> All write operations must be completed within 1 second.

Step5. Query until RTC_CR1.WAITF=0.

18.4.4 Alarm Clock Setting

Procedure

Step1. Set RTC_CR1.ALMEN=0 to disable the alarm.

Step2. Set RTC_CR1.ALMIE=1 to enable the alarm interrupt.

Step3. Set the second alarm (RTC_ALMSEC), minute alarm (RTC_ALMMIN), hour alarm (RTC_ALM-HOUR), and week alarm (RTC_ALMWEEK).

Step4. Set RTC_CR1.ALMEN=1 to enable the alarm interrupt.

Step5. Wait for an interrupt to occur.

Step6. Since the alarm clock interrupt and the fixed-period interrupt share the interrupt request signal, when RTC_CR1.ALMF=1, enter the alarm clock interrupt processing; otherwise, enter the fixed-period interrupt processing.

18.4.5 1Hz Output

Context

RTC can choose to output three types of 1Hz clocks: general precision, higher precision and high precision. When the clock error compensation function is valid, it outputs a high-precision 1Hz clock; when using HPCLK with different frequencies, it outputs a high-precision 1Hz clock. The system control

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register must be configured according to the HPCLK frequency. The three methods for 1Hz output are as follows:

Procedure

- **General Precision 1Hz Output (without Clock Compensation)**
  - **Step1.** Set RTC_CR0.START=0 to stop counting;
  - **Step2.** RTC output pin setting.
  - **Step3.** Set RTC_CR0.HZ1OE=1 to enable clock output.
  - **Step4.** Set RTC_CR0.START=1, counting starts.
  - **Step5.** Wait for more than 2 count cycles.
  - **Step6.** 1Hz output starts.
- **Higher Precision 1Hz Output (Low-speed Compensation)**
  - **Step1.** Set RTC_CR0.START=0 to stop counting;
  - **Step2.** RTC output pin setting.
  - **Step3.** Set RTC_CR0.HZ1OE=1 to enable clock output.
  - **Step4.** Configure RTC_COMPEN.CR to set the compensation value.
  - **Step5.** Set RTC_COMPEN.EN=1 to enable error compensation.
  - **Step6.** Set RTC_CR0.START=1, counting starts.
  - **Step7.** Wait for more than 2 count cycles.
  - **Step8.** 1Hz output starts.
- **High Precision 1 Hz Output (Based on Higher Precision Output, Providing the RTC with a High-Speed Compensation Clock of 4/6/8/12/16/20/24/32 MHz)**
  - **Step1.** Set RTC_CR0.START=0 to stop counting;
  - **Step2.** RTC output pin setting.
  - **Step3.** Set RTC_CR0.HZ1OE=1 to enable clock output.
  - **Step4.** Set RTC_CR0.HZ1SEL=1, choose to output high-precision 1Hz clock.
  - **Step5.** Configure SYSCTRL1.RTC_FREQ_ADJUST.
  - **Step6.** Configure RTC_COMPEN.CR[8:0] to set the compensation.
  - **Step7.** Set RTC_COMPEN.EN=1 to enable error compensation.
  - **Step8.** Set RTC_CR0.START=1, counting starts.
  - **Step9.** Wait for more than 2 count cycles.
  - **Step10.** 1Hz output starts.

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18.5 Register Description

18.5.1 Register List

Base address: 0x40001400

Table 18-2 Real Time Counter (RTC) Register Offset

Offset	Register	Description	Width
0x000	RTC_CR0	Control Register 0	32
0x004	RTC_CR1	Control Register 1	32
0x008	RTC_SEC	Second Count Register	32
0x00C	RTC_MIN	Minute Count Register	32
0x010	RTC_HOUR	Hour Count Register	32
0x014	RTC_WEEK	Week Count Register	32
0x018	RTC_DAY	Day Count Register	32
0x01C	RTC_MON	Month Count Register	32
0x020	RTC_YEAR	Year Count Register	32
0x024	RTC_ALMMIN	Minute Alarm Register	32
0x028	RTC_ALMHOUR	Hour Alarm Register	32
0x02C	RTC_ALMWEEK	Week Alarm Register	32
0x030	RTC_COMPEN	Clock Error Compensation Register	32
0x034	RTC_ALMSEC	Second Alarm Register	32

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18.5.2 Control Register 0 (RTC_CR0)

Offset	Bit Position																													
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000 (Only a power-on reset is effective for this register reset)																													
Name	Reserved																	PRDSEL	PRDX						START	HZ1SEL	HZ1OE	Reserved	AMPM	PRDS	
Access																		RW	RW						RW	RW	RW		RW	RW	

Bit	Name	Functional Description	Access
31:15	*Reserved*	-	-
14	PRDSEL	Periodic interrupt source selection ● 0b0: Use the periodic interrupt time interval set by PRDS ● 0b1: Use the periodic interrupt time interval set by PRDX	RW
13:8	PRDX	Set the time interval for generating periodic interrupts The settable range is from 0.5 seconds to 32 seconds, and the step is 0.5 seconds. ● 0b000000: 0.5 seconds ● 0b000001: 1 second ● ..... ● 0b111110: 31.5 seconds ● 0b111111: 32 seconds	RW
7	START	RTC count enable ● 0b0: Stop the RTC count ● 0b1: Enable the RTC count	RW
6	HZ1SEL	1Hz output selection ● 0b0: Normal precision 1Hz output ● 0b1: High precision 1Hz output	RW
5	HZ1OE	1Hz output enable ● 0b0: Disabled 1Hz output ● 0b1: Enable 1Hz output	RW
4	*Reserved*	-	-
3	AMPM	Time format selection ● 0b0: 12-hour time format ● 0b1: 24-hour time format	RW

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Bit	Name	Functional Description	Access
2:0	PRDS	Set the time interval for generating interrupts ● 0b000: No periodic interrupt generated ● 0b001: 0.5 seconds ● 0b010: 1 second ● 0b011: 1 minute (At 00 seconds every minute) ● 0b100: 1 hour (At 00:00 every hour) ● 0b101: 1 day (At 00:00:00 every day) ● 0b110/0b111: 1 month (At 00:00:00 on the first day of every month) **Notice** If you need to write and change the time interval of periodic interrupt when START=1, the operation steps are as follows: 1. Turn off the RTC interrupt in the NVIC; 2. Change the time interval of periodic interrupt; 3. Clear the RTC interrupt flag; 4. Enable RTC interrupt.	RW

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18.5.3 Control Register 1 (RTC_CR1)

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000 (Only power-on reset is effective for this register reset)																															
Name	Reserved																						CKSEL		ALMEN	ALMIE	Reserved	ALMF	PRDF	Reserved	WAITF	WAIT
Access																							RW		RW	RW		RW	RW		RO	RW

Bit	Name	Functional Description	Access
31:11	*Reserved*	-	-
10:8	CKSEL	RTC clock selection ● 0b000/0b001: XTL 32.768k ● 0b010/0b011: RCL 32k ● 0b100: XTH/128 (select this option when the crystal oscillator is 4M) ● 0b101: XTH/256 (select this option when the crystal oscillator is 8M) ● 0b110: XTH/512 (select this option when the crystal oscillator is 16M) ● 0b111: XTH/1024 (Select this option when the crystal oscillator is 32M.)	RW
7	ALMEN	Alarm enable ● 0b0: Disable ● 0b1: Enable **Notice** When ALMEN is enabled during START=1 calendar counting process and ALMIE=1 interrupt permission, please disable the system interrupt to prevent malfunction. After enabling, please clear the ALMF flag bit.	RW
6	ALMIE	Alarm/Periodic interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
5	*Reserved*	-	-
4	ALMF	Alarm interrupt flag Write 0 to clear the bit, write 1 has no effect. Read: ● 0b0: No alarm interrupt occurred ● 0b1: Alarm interrupt is occurred **Notice** This bit is valid only when ALMEN=1. When the alarm matches, a clock of 32.768kHz is set to 1.	RW

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Bit	Name	Functional Description	Access
3	PRDF	Periodic interrupt flag Write 0 to clear the bit, write 1 has no effect. Read: ● 0b0: No periodic interrupt occurred ● 0b1: Periodic interrupt is occurred **Notice** Set to 1 after a periodic interrupt occurred.	RW
2	*Reserved*	-	-
1	WAITF	Read and write wait valid flag ● 0b0: Not write/read status ● 0b1: Write/read status **Notice** Flag indicating whether the WAIT bit setting is effective. Please confirm that this bit is set to "1" before writing or reading. During the counting process, the bit is cleared to"0" after the WAIT bit is cleared to"0" and waits for the writing to be completed.	RO
0	WAIT	Read and write wait setting ● 0b0: Normal Counting Mode ● 0b1: Write/read mode **Notice** Please set this bit to "1" when writing/reading. Since the counter is counting continuously, please complete the writing/reading operation within 1 second and clear this bit to "0".	RW

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18.5.4 Second Count Register (RTC_SEC)

Offset	Bit Position																															
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	Reserved																									SECH			SECL			
Access																										RW			RW			

Bit	Name	Functional Description	Access
31:7	*Reserved*	-	-
6:4	SECH	Second count tens digit BCD code of second tens digit count value	RW
3:0	SECL	Second count units digit BCD code of second units digit count value	RW

Indicates 0-59 seconds, using decimal counting. Please write the BCD code in decimal 0 to 59. Values written outside this range will be ignored.

18.5.5 Minute Count Register (RTC_MIN)

Offset	Bit Position																															
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	Reserved																									MINH			MINL			
Access																										RW			RW			

Bit	Name	Functional Description	Access
31:7	*Reserved*	-	-
6:4	MINH	Minute count tens digit BCD code of minute tens digit count value	RW
3:0	MINL	Minute count units digit BCD code of minute units digit count value	RW

Indicates 0-59 points, using decimal counting. Please write the BCD code in decimal 0 to 59. Values written outside this range will be ignored.

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18.5.6 Hour Count Register (RTC_HOUR)

Offset	Bit Position																														
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	Reserved																										HOURH		HOURL			
Access																											RW		RW			

Bit	Name	Functional Description	Access
31:6	*Reserved*	-	-
5:4	HOURH	Hour count tens digit BCD code of hour tens digit count value	RW
3:0	HOURL	Hour count units digit BCD code of hour units digit count value	RW

In 24-hour format, it means 0-23 hours.

In 12-hour format, it means 0-12 hours. Bit5=0 means AM, then 01-12 means morning; Bit5=1 means PM, then 21-32 means afternoon.

Please set the correct decimal BCD code according to the value of the control bit RTC_CR0.AMPM. The value written out of range will be ignored.

For specific time values, please refer to the following table:

24-Hour Clock Format (AMPM=1)		12-Hour Clock Format (AMPM=0)	
Time	Register Value	Time	Register Value
00 o'clock	0x00	AM 12 o'clock	0x12
01 o'clock	0x01	AM 01 o'clock	0x01
02 o'clock	0x02	AM 02 o'clock	0x02
03 o'clock	0x03	AM 03 o'clock	0x03
04 o'clock	0x04	AM 04 o'clock	0x04
05 o'clock	0x05	AM 05 o'clock	0x05
06 o'clock	0x06	AM 06 o'clock	0x06
07 o'clock	0x07	AM 07 o'clock	0x07
08 o'clock	0x08	AM 08 o'clock	0x08
09 o'clock	0x09	AM 09 o'clock	0x09
10 o'clock	0x10	AM 10 o'clock	0x10
11 o'clock	0x11	AM 11 o'clock	0x11
12 o'clock	0x12	PM 12 o'clock	0x32

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24-Hour Clock Format (AMPM=1)		12-Hour Clock Format (AMPM=0)	
Time	Register Value	Time	Register Value
13 o'clock	0x13	PM 01 o'clock	0x21
14 o'clock	0x14	PM 02 o'clock	0x22
15 o'clock	0x15	PM 03 o'clock	0x23
16 o'clock	0x16	PM 04 o'clock	0x24
17 o'clock	0x17	PM 05 o'clock	0x25
18 o'clock	0x18	PM 06 o'clock	0x26
19 o'clock	0x19	PM 07 o'clock	0x27
20 o'clock	0x20	PM 08 o'clock	0x28
21 o'clock	0x21	PM 09 o'clock	0x29
22 o'clock	0x22	PM 10 o'clock	0x30
23 o'clock	0x23	PM 11 o'clock	0x31

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18.5.7 Day Count Register (RTC_DAY)

Offset	Bit Position																													
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	Reserved																										DAYH		DAYL			
Access																											RW		RW			

Bit	Name	Functional Description	Access
31:6	*Reserved*	-	-
5:4	DAYH	Day count tens digit value BCD code of day tens digit count value	RW
3:0	DAYL	Day count units digit BCD code of day units digit count value	RW

Means 1 to 31 days, uses decimal counting, automatically calculates leap year and month. Please write the BCD code in decimal 1 to 31. Values written outside the range will be ignored.

Refer to the table below for the specific range of day values.

Month	Day Count Value
February (normal year)	01-28
February (leap year)	01-29
April, June, September, November	01-30
January, March, May, July, August, October , December	01-31

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18.5.8 Week Count Register (RTC_WEEK)

Offset	Bit Position																													
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	Reserved																													WEEK		
Access																														RW		

Bit	Name	Functional Description	Access
31:3	*Reserved*	-	-
2:0	WEEK	Week count value BCD code of week count value	RW

Decimal 0-6 means Sunday-Saturday. Please write the BCD code in decimal 0 to 6. Values written outside the range will be ignored.

For specific week count values, please refer to the following table:

Week	Week Count Value
Sunday	0x00
Monday	0x01
Tuesday	0x02
Wednesday	0x03
Thursday	0x04
Friday	0x05
Saturday	0x06

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18.5.9 Month Count Register (RTC_MON)

Offset	Bit Position																													
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	Reserved																											MON				
Access																												RW				

Bit	Name	Functional Description	Access
31:5	*Reserved*	-	-
4:0	MON	Month count value BCD code of month count value	RW

Indicates 1-12 months, using decimal counting. Please write the BCD code in decimal 1 to 12. Values written outside the range will be ignored.

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18.5.10 Year Count Register (RTC_YEAR)

Offset	Bit Position																													
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	Reserved																								YEARH				YEARL			
Access																									RW				RW			

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7:4	YEARH	Year conut tens digit BCD code of year tens digit count value	RW
3:0	YEARL	Year conut units digit BCD code of year units digit count value	RW

Indicates 0 to 99 years, using decimal counting, counting according to the month carry. Automatically calculate leap years such as: 00, 04, 08, ..., 92, 96, etc. Please write the BCD code in decimal 0-99. Values written outside the range will be ignored.

18.5.11 Second Alarm Register (RTC_ALMSEC)

Offset	Bit Position																													
0x034	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	Reserved																									ALMSECH			ALMSECL			
Access																										RW			RW			

Bit	Name	Functional Description	Access
31:7	*Reserved*	-	-
6:4	ALMSECH	Second alarm match value tens digit BCD code of the second tens digit alarm match value	RW
3:0	ALMSECL	Second alarm match value units digit BCD code of the second units digit alarm match value	RW

Indicates 0-59 seconds, using decimal counting. Please write the BCD code in decimal 0-59, and the alarm clock matching will not occur if you write the value out of range.

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18.5.12 Minute Alarm Register (RTC_ALMMIN)

Offset	Bit Position																													
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	Reserved																									ALMMINH			ALMMINL			
Access																										RW			RW			

Bit	Name	Functional Description	Access
31:7	*Reserved*	-	-
6:4	ALMMINH	Minute alarm match value tens digit BCD code of the minute tens digit alarm match value	RW
3:0	ALMMINL	Minute alarm match value units digit BCD code of the minute units digit alarm match value	RW

Indicates 0-59 minutes, using decimal counting. Please write the BCD code in decimal 0-59, and the alarm clock matching will not occur if you write the value out of range.

18.5.13 Hour Alarm Register (RTC_ALMHOUR)

Offset	Bit Position																													
0x028	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	Reserved																										ALMHOURH			ALMHOURL		
Access																											RW			RW		

Bit	Name	Functional Description	Access
31:6	*Reserved*	-	-
5:4	ALMHOURH	Hour alarm match value tens digit BCD code of the hour tens digit alarm match value	RW
3:0	ALMHOURL	Hour alarm match value units digit BCD code of the hour units digit alarm match value	RW

Please set the correct decimal BCD code according to the time format. Writing values outside the range will not trigger an alarm match.

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18.5.14 Week Alarm Register (RTC_ALMWEEK)

Offset	Bit Position																													
0x02C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	Reserved																									ALMWEEK						
Access																										RW						

Bit	Name	Functional Description	Access
31:7	*Reserved*	-	-
6:0	ALMWEEK	Week alarm match value Bit0-Bit6 correspond to Sunday-Saturday respectively: When the corresponding bit is set to 1, the alarm is active on that day of the week. For example: ● Setting it to 0b0000001 indicates that the Sunday alarm is enabled. ● Setting it to 0b0000011 means the alarm is enabled for Sunday and Monday. ● Setting it to 0b1000000 indicates that the Saturday alarm is enabled.	RW

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18.5.15 Clock Error Compensation Register (RTC_COMPEN)

Offset	Bit Position																															
0x030	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000020 (Only power-on reset is effective for this register reset)																															
Name	Reserved																EN	Reserved												CR		
Access																	RW													RW		

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15	EN	Compensation enable ● 0b0: Disable clock error compensation ● 0b1: Enable clock error compensation	RW
14:9	*Reserved*	-	-
8:0	CR	Compensation value By setting the compensation value, an accuracy compensation of ±0.96ppm can be performed per second. The compensation value is 9-bit 2's complement code with a decimal point, and the last 5 bits are the decimal part. Compensation range: 274.6ppm to 212.6ppm, with a minimum differential error of ±0.48ppm and a minimum resolution of 0.96ppm.	RW

For more compensation accuracy, see the following table:

Compensation Value Setting										Compensation Value
EN	CR[8:0]									
1	1	0	0	0	0	0	0	0	0	-274.6ppm
	1	0	0	0	0	0	0	0	1	-273.7ppm
	...									...
	0	0	0	0	1	1	1	1	1	-0.96ppm
	0	0	0	1	0	0	0	0	0	0ppm
	...									...
	0	1	1	1	1	1	1	1	0	+211.7ppm
	0	1	1	1	1	1	1	1	1	+212.6ppm
0	X	X	X	X	X	X	X	X	X	Uncompensat-ed

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19 WDT

19.1 Introduction

WDT can be used to detect and resolve failures caused by software errors. When the WDT counter reaches the set overflow time, it will trigger an interrupt or generate a system reset. WDT is driven by a dedicated 10kHz on-chip oscillator.

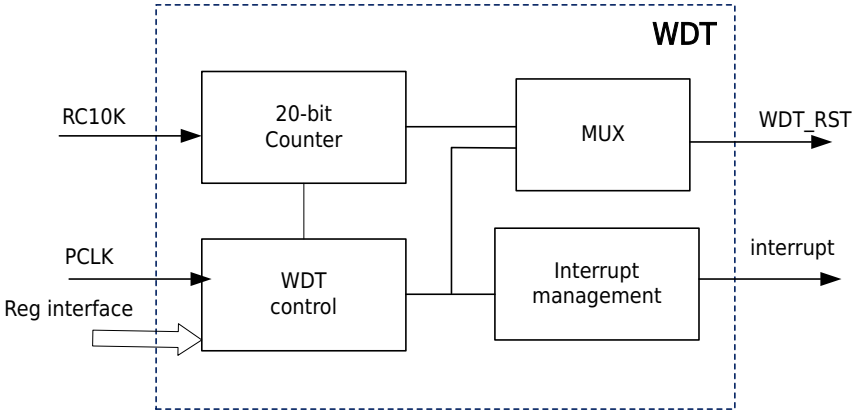

Figure 19-1 WDT Overall Block Diagram

19.2 Functional Description

- A 20-bit freely-running up-counter, whose overflow time can be configured as 1.6ms - 52.4s.
- Action after overflow can be configured as interrupt or reset.
- The WDT clock is provided by an independent RC oscillator, which can work in Sleep and DeepSleep modes.
- WDTCON register can only be modified when the WDT is not started to prevent unintentional modification of the WDT configuration after startup.

19.2.1 Interrupt Generated After WDT Overflow

Context

In this mode, WDT will generate interrupt periodically according to the set time. WDT interrupt flag needs to be cleared in the interrupt service routine.

Notice

Since the WDT oscillator is a low-precision RC oscillator, it is strongly recommended to clear the WDT before the WDT counter count value reaches half of the overflow value.

Procedure

Step1. Configure WDT_CON.WOV, select WDT timing overflow time.

Step2. Set WDT_CON.WINT_EN to 1, an interrupt is generated after WDT overflow is selected.

Step3. Enable the WDT interrupt in the NVIC interrupt vector table.

Step4. Write 0x1E and 0xE1 to the WDT_RST register in sequence to start the WDT timer.

Step5. Write 0x1E and 0xE1 to the WDT_RST register in sequence in the interrupt service routine to clear the interrupt flag.

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19.2.2 Reset Generated After WDT Overflow

Context

In this mode, the Reset signal will be generated after the WDT counter overflows, which will reset the MCU. User program needs to clear the WDT counter before WDT overflow, so as to avoid WDT reset.

Notice

Since the WDT oscillator is a low-precision RC Oscillator, it is strongly recommended to clear the WDT before the WDT counter count value reaches half of the overflow value.

Procedure

Step1. Configure WDT_CON.WOV to select the WDT counter overflow time.

Step2. Set WDT_CON.WINT_EN to 0 to choose a reset upon WDT overflow.

Step3. Write 0x1E and 0xE1 to the WDT_RST register in sequence to start the WDT timer.

Step4. Write 0x1E and 0xE1 to the WDT_RST register in sequence before WDT overflow to clear the WDT counter.

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19.3 Register Description

19.3.1 Register List

Base address: 0x40000F80

Table 19-1 Watchdog Timer (WDT) Register Offset

Offset	Register	Description	Width
0x00	WDT_RST	Clear Control Register	32
0x04	WDT_CON	Control Register	32

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19.3.2 Clear Control Register (WDT_RST)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								RST							
Access																									WO							

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7:0	RST	Watchdog start/clear control ● When the watchdog is not started, write 0x1E and 0xE1 to this register in sequence to start the WDT timer. ● When the watchdog is started, write 0x1E and 0xE1 to this register in sequence to clear the WDT timer and interrupt flag.	WO

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19.3.3 Control Register (WDT_CON)

Notice

This register can only be written when WDT is not running.

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000000F																															
Name	Reserved																WCNTL								INT	Reserved	WINT_EN	R	WOV			
Access																	RO								RO		RW	RO	RW			

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:8	WCNTL	WDT counter low 8 bits	RO
7	INT	WDT interrupt flag ● 0b0: WDT interrupt not occurs ● 0b1: WDT interrupt has occurred, write 0x1E, 0xE1 to the WDT_RST register in sequence to clear the interrupt flag	RO
6	*Reserved*	-	-
5	WINT_EN	Action configuration after WDT overflow ● 0b0: Reset is generated after WDT overflow ● 0b1: Interrupt is generated after WDT overflow	RW
4	R	WDT running flag ● 0b0: WDT stops ● 0b1: WDT is running	RO
3:0	WOV	WDT timing overflow time configuration ● 0b0000: 1.6ms ● 0b0001: 3.2ms ● 0b0010: 6.4ms ● 0b0011: 13ms ● 0b0100: 26ms ● 0b0101: 51ms ● 0b0110: 102ms ● 0b0111: 205ms ● 0b1000: 500ms ● 0b1001: 820ms ● 0b1010: 1.64s ● 0b1011: 3.28s ● 0b1100: 6.55s ● 0b1101: 13.1s ● 0b1110: 26.2s ● 0b1111: 52.4s	RW

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20 WWDT

20.1 Introduction

The window watchdog (WWDT) is often used to monitor software failures triggered by unexpected errors. An interrupt is generated when the counter value is decremented to 0x40, and a reset is generated when the counter value is decremented to 0x3F; if the user program updates the counter value when the counter value is greater than the window value, a reset is generated. So the user program can only update the WWDT counter value within a limited window (the counter value is less than or equal to the window value and greater than 0x3F).

20.2 Features

- 7-bit down counter
- PCLK divided clock as count clock
- When PCLK is 48MHz, its timeout time is 85μs - 699ms
- An interrupt is generated when the count value is decremented to 0x40
- A reset is generated when the count value is decremented to 0x3F
- Update the counter when the count value is greater than the window value, a reset is generated

20.3 Functional Description

20.3.1 Function Block Diagram

After the watchdog is started, the value of the counter WCNT decreases by 1 on each rising edge of WWDTCLK. When the counter is decremented to 0x40, the watchdog will generate a pre-overflow signal POV, enable WWDT_CR1.IE can make the watchdog generate a pre-overflow interrupt; when the counter is decremented to 0x3F, the watchdog will generate a reset signal. User program can write WWDT_CR0.WCNT to update WCNT to prevent watchdog from generating reset signal. If the value of WCNT is greater than the value of WINR when the user updates WCNT, the watchdog will also generate a reset signal.

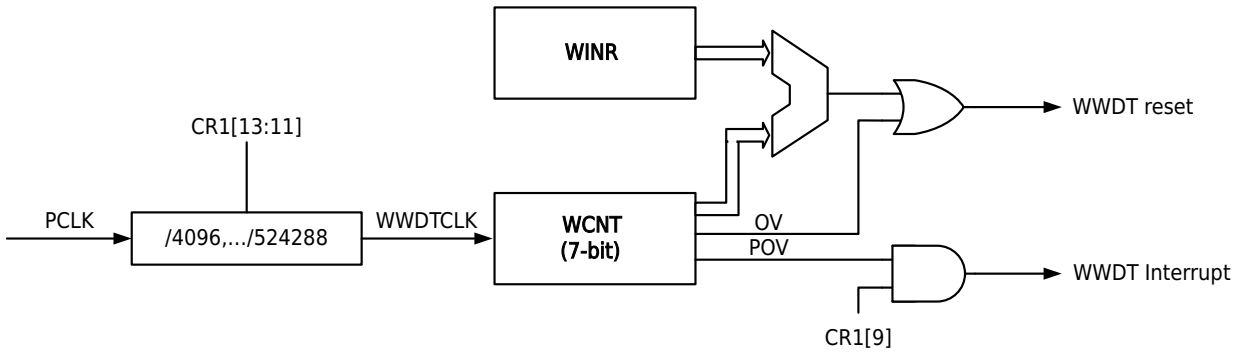

Figure 20-1 WWDT Function Block Diagram

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20.3.2 Enable Watchdog

After the system is reset, the watchdog is turned off. Set WWDT_CR0.EN to 1 to enable the watchdog. The user program cannot disable the enabled watchdog by writing 0 to WWDT_CR0.EN. It is recommended to enable the watchdog by writing 0xFF to WWDT_CR0 to ensure that the reset is not triggered when the watchdog is enabled.

20.3.3 Configure Watchdog Timeout

The required watchdog timeout period can be obtained by properly configuring WWDT_CR0.WCNT and WWDT_CR1.PRS. When PCLK is 48MHz, the range of its timeout period is 85μs - 699ms.

The formula for calculating the timeout is as follows:

$T_{WWDT} = T_{PCLK} \times 4096 \times 2^{CR1.PRS} \times$ (CR0.WCNT-0x3F)

20.3.4 Update Down Counter

Write data to WWDT_CR0.WCNT, and the WWDT down counter can be updated. If the written value is less than or equal to 0x3F, a reset will occur directly; if the current count value is greater than the window value when the counter is updated, a reset will occur directly. Therefore, the user program can only update the down counter when the value of the down counter is less than or equal to the window value and greater than 0x3F.

20.3.5 Pre-overflow Interrupt

If the down counter decrements to 0x40 and WWDT_CR1.IE is 1, the WWDT will generate a pre-overflow interrupt, the user program can update the down counter in the interrupt service routine to prevent the WWDT from generating a reset; before exiting the interrupt service, the user program should write 0x00 to the WWDT_SR register to clear the WWDT pre-overflow flag.

20.4 Operation Example

20.4.1 Example of Configuring Watchdog Window Overflow Period

Context

The following example configures the overflow period of the watchdog as 786432 PCLK, and the window is 1/3 of the overflow period.

Procedure

Step1. Configure WWDT_CR1.PRS to 2, and the counting clock of WWDT is PCLK/16384.

Step2. Configure WWDT_CR1.WINR to 0x4F, and the update window of WWDT is 0x4F - 0x40.

Step3. Configure WWDT_CR0.WCNT to 0x6F, and the overflow period of WWDT is 786432 PCLK.

Step4. Set WWDT_CR0.EN to 1 to start the watchdog.

Step5. When the value of the down counter is less than or equal to the window value and greater than 0x3F, write 0x6F to WWDT_CR0.WCNT to reload the watchdog counter.

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20.5 Register Description

20.5.1 Register List

Base address: 0x40007800

Notice

WWDT affects register value after reset.

Table 20-1 Window Watchdog (WWDT) Register Offset

Offset	Register	Description	Width
0x00	WWDT_CR0	Control Register 0	32
0x04	WWDT_CR1	Control Register 1	32
0x08	WWDT_SR	Status Register	32

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20.5.2 Control Register 0 (WWDT_CR0)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000007F																															
Name	Reserved																								EN	WCNT						
Access																									RW	RW						

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7	EN	WWDT enable control Once this bit is set to 1, it cannot be cleared by software ● 0b0: Disable WWDT ● 0b1: Enable WWDT	RW
6:0	WCNT	Read: WWDT counter current count value Write: Update WWDT counter current count value	RW

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20.5.3 Control Register 1 (WWDT_CR1)

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000007F																															
Name	Reserved																		PRS			Reserved	IE	Reserved				WINR			
Access																			RW				RW						RW			

Bit	Name	Functional Description	Access
31:14	*Reserved*	-	-
13:11	PRS	WWDT count clock configuration ● 0b000: PCLK/4096 ● 0b001: PCLK/8192 ● 0b010: PCLK/16384 ● 0b011: PCLK/32768 ● 0b100: PCLK/65536 ● 0b101: PCLK/131072 ● 0b110: PCLK/262144 ● 0b111: PCLK/524288	RW
10	*Reserved*	-	-
9	IE	WWDT pre-overflow interrupt enable control ● 0b0: Disable pre-overflow interrupt ● 0b1: Enable pre-overflow interrupt	RW
8:7	*Reserved*	-	-
6:0	WINR	Watchdog window value The user program can only update the value of the WWDT counter when the counter value is less than or equal to the window value and greater than 0x3F.	RW

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20.5.4 Status Register (WWDT_SR)

Offset	Bit Position																													
0x08	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																															POV
Access																																RW

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-
0	POV	WWDT pre-overflow flag Write 0 to clear the pre-overflow flag, write 1 has no effect. Read: ● 0b0: No pre-overflow has occurred in WWDT ● 0b1: Pre-overflow has occurred in WWDT	RW

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21 PCNT

21.1 Introduction

The pulse counter (PCNT) module can count the input pulses and supports three pulse modes: single-channel pulse, dual-channel quadrature pulse, and dual-channel non-orthogonal pulse. Counts correctly in low-power modes without software involvement.

21.2 Features

- Supports 16-bit counter supporting reload function
- Single-channel pulse counting
- Dual channel non-intersecting pulse counting
- Two-channel quadrature pulse counting without missing codes
- Up/Down counting overflow interrupt
- Pulse timeout interrupt
- 4 kinds of decoding error interrupt, non-intermittent pulse mode
- 1 direction change interrupt, quadrature pulse mode
- Multi-stage pulse width filtering
- Configurable input pulse polarity
- Support low-power mode counting
- Support waking up MCU in low power mode
- Support any pulse edge spacing not less than 1 count clock cycle
- Support IO input or VC output as pulse input signal
- Support dual-channel pulse signal shaping and output PCNT_S0FO/PCNT_S1FO through IO observation
- With automatic timing wake-up function in low power consumption mode, the maximum timing is 1024 seconds

21.3 Functional Description

21.3.1 Overall Block Diagram

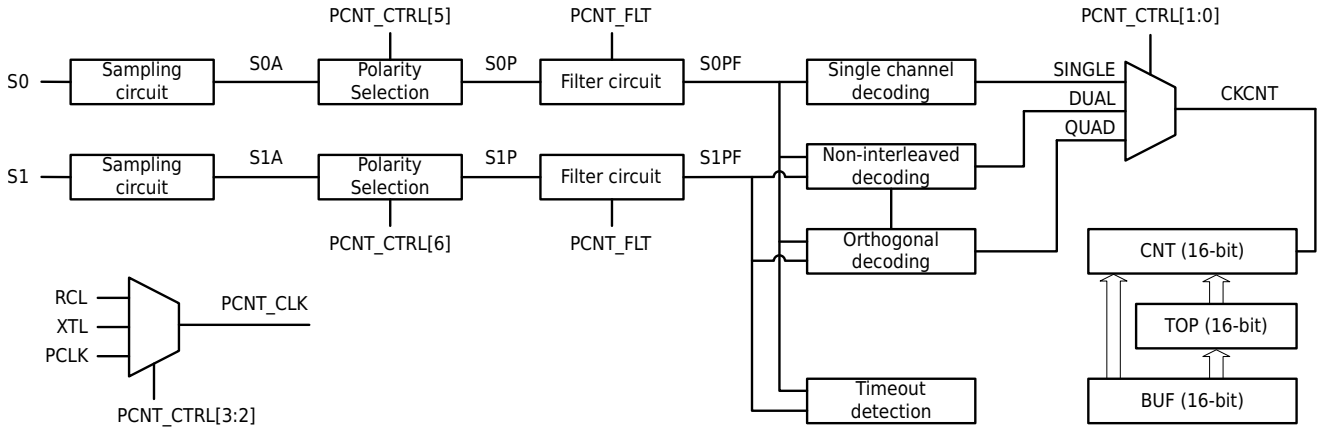

Figure 21-1 Pulse Counter Overall Block Digram

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21.3.2 Signal Description

The following takes the input signal S0 as an example to illustrate the processing flow of the signal in the counter module.

- The S0 signal outputs the S0A signal after the sampling module, and the sampling clock is PCNT_CLK.
- The S0A signal outputs the S0P signal after passing through the polarity selection module.
- The S0P signal outputs the S0PF signal after passing through the pulse width filter module, and the clock of the filter module is PCNT_CLK after frequency division.
- The S0PF signal is decoded by the single-channel decoding module, the dual-channel non-intersection decoding module, and the dual-channel orthogonal decoding module to output corresponding SIGNAL, DUAL, and QUAD signals.
- SIGNAL, DUAL, and QUAD output CKCNT signals after passing through the multiplexer to drive the CNT module to count.

21.3.3 Counting Mode

21.3.3.1 Single Mode

When PCNT_CTRL.MODE is configured to 0x00 or 0x01, the pulse counter operates in single mode. In this mode, the decoding module only counts the S0 pulse signal. When the PCNT_CLK clock is sampled to the falling edge of the S0PF signal, the counter performs an increment or decrement operation according to the configuration of PCNT_CTRL.DIR.

The count range of the counter is from 0x00 to the upper count threshold (PCNT_TOP).

In the up-counting state, when the count value is equal to PCNT_TOP and the falling edge of the S0PF signal is sampled, the counter overflows. The count value returns to 0 and PCNT_IFR.OF is set, and the interrupt flag needs to be cleared by software. The figure below is the timing diagram of PCNT counting up, in which the value of PCNT_TOP is 99.

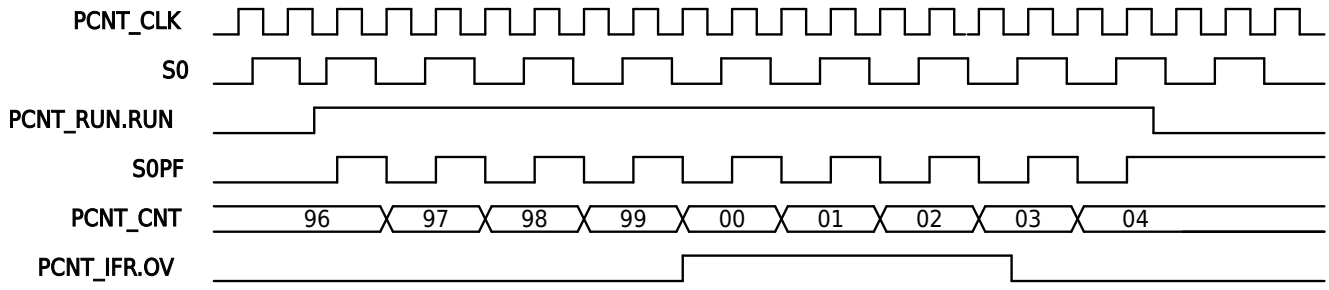

Figure 21-2 Up Counting Waveform in Single Mode

In the down-counting state, when the count value is equal to 0x00 and the falling edge of the S0PF signal is sampled, the counter underflows. The count value returns to PCNT_TOP and PCNT_IFR.UF is set, and the interrupt flag needs to be cleared by software. The following figure is the timing diagram of PCNT counting down, in which the value of PCNT_TOP is 99.

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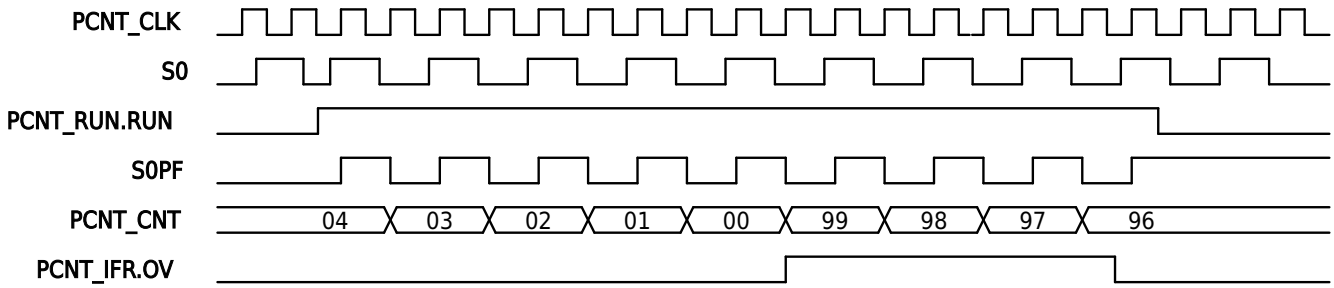


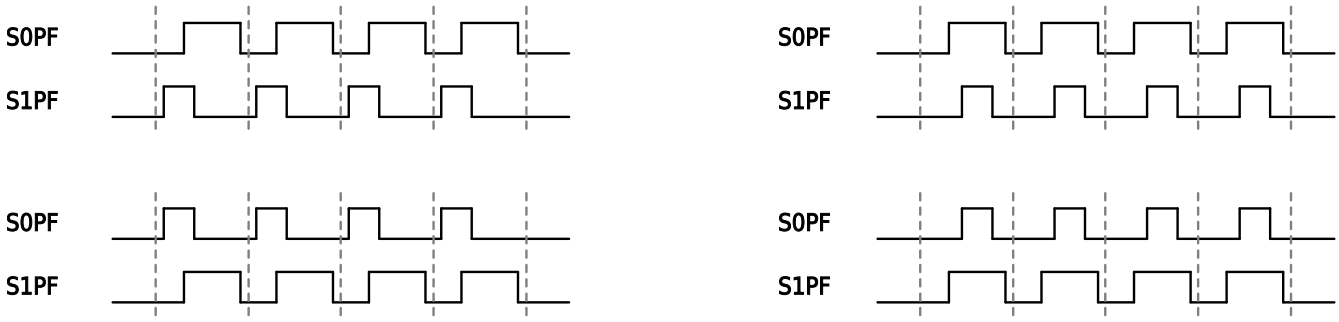
Figure 21-3 Down Counting Waveform in Single Mode

21.3.3.2 Dual Mode

When PCNT_CTRL.MODE is configured to 0x02, the pulse counter operates in dual mode. In this mode, the decoding module decodes and counts S0 and S1 pulse signals. When two positive pulses appear in S0PF and S1PF in sequence, the counter performs an increment or decrement operation according to the configuration of PCNT_CTRL.DIR.

The two waveforms that the decoding module can count correctly are shown below. S0PF and S1PF are not high at the same time.

Several waveforms that the decoding module cannot count correctly are shown below. S0PF and S1PF are high at the same time.



The count range of the counter is from 0x00 to the upper count threshold (PCNT_TOP).

In the up-counting state, when the count value is equal to PCNT_TOP and two positive pulses appear in S0PF and S1PF in sequence, the counter overflows, the count value returns to 0 and PCNT_IFR.OF is set, and the interrupt flag needs to be cleared by software. The figure below is the timing diagram of PCNT counting up, in which the value of PCNT_TOP is 99.

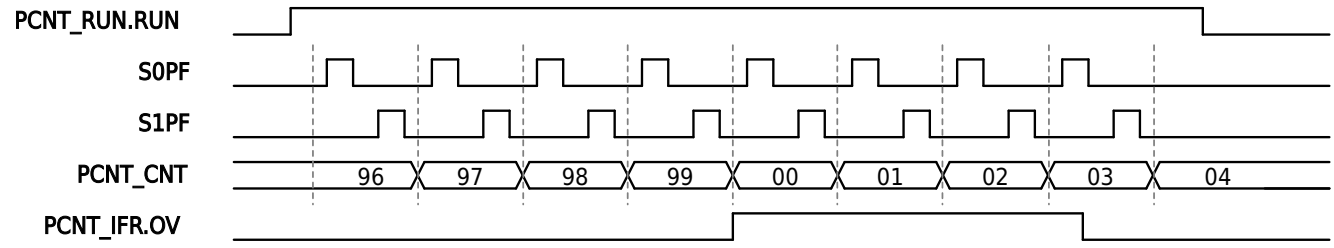


Figure 21-6 Up Counting Waveform in Dual Mode

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In the down-counting state, when the count value is equal to 0x00 and two positive pulses appear in S0PF and S1PF in sequence, the counter underflows, the count value returns to PCNT_TOP and PCNT_IFR.UF is set, and the interrupt flag needs to be cleared by software. The following figure is the timing diagram of PCNT counting down, in which the value of PCNT_TOP is 99.

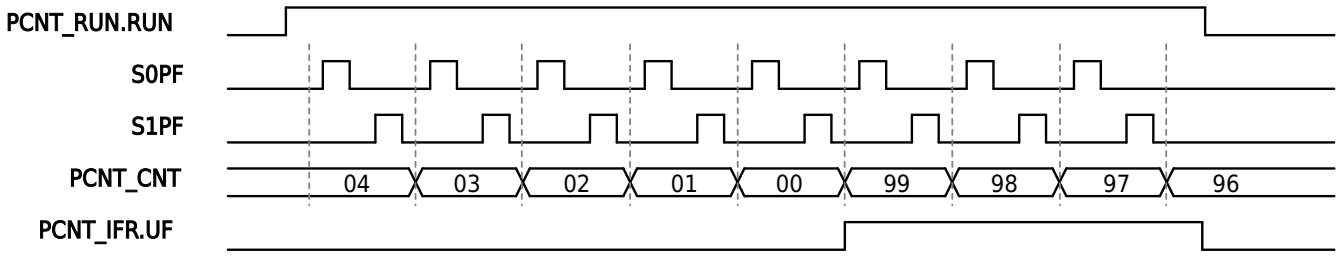

Figure 21-7 Down Counting Waveform in Dual Mode

21.3.3.3 Quad Mode

PCNT_CTRL.MODE is configured as 0x03, the pulse counter works in dual-channel quadrature pulse counting mode. In this mode, the decoding module needs two pulse signals of S0 and S1 for decoding and counting. The counter automatically judges the counting direction according to the phase relationship of S0PF and S1PF pulses, and the physical equipment can count correctly in any forward or reverse rotation. When S0PF and S1PF complete a cycle change, the counter performs an increment or decrement operation according to the counting direction.

The waveform of the decoding module to judge the counting direction is as follows:

The count range of the counter is from 0x00 to the upper count threshold (PCNT_TOP).

In the counting state, when the count value is equal to PCNT_TOP and S0PF and S1PF complete a cycle change, the counter overflows. Tthe count value returns to 0 and PCNT_IFR.OF is set, and the interrupt flag needs to be cleared by software. The figure below is the timing diagram of PCNT counting up, in which the value of PCNT_TOP is 99.

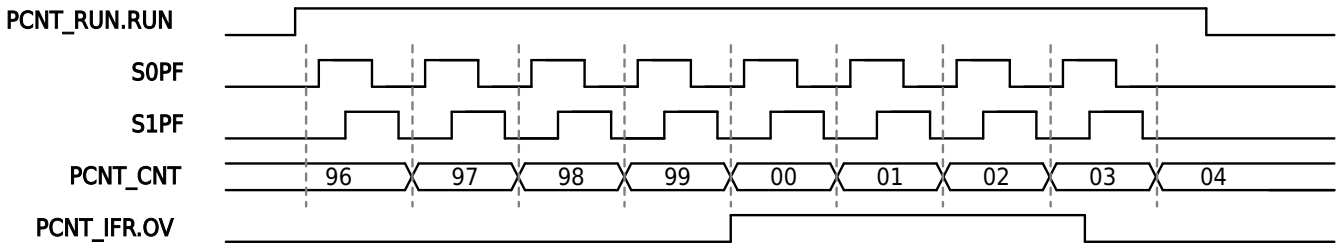

Figure 21-9 Quad Mode-Up-counting Waveform

In the down-counting state, when the count value is equal to 0x00 and S0PF and S1PF complete a cycle change, the counter underflows, the count value returns to PCNT_TOP and PCNT_IFR.UF is set, and the interrupt flag needs to be cleared by software. The following figure is the timing diagram of PCNT counting down, in which the value of PCNT_TOP is 99.

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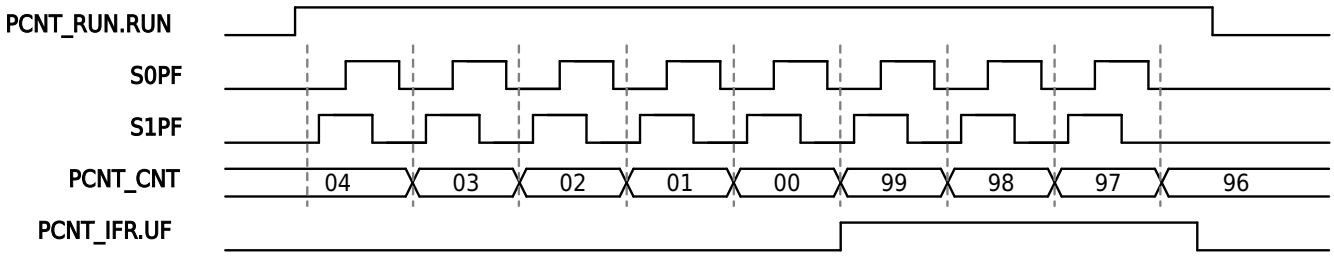

Figure 21-10 Quad Mode-Down-counting Waveform

21.3.4 Pulse Width Filtering

The pulse width filter uses the frequency division of the counting clock as the filter clock, and counts with this to achieve the purpose of pulse debounce. The division factor of the filter clock can be configured from 1 to 8096 times via the register (FLT.CLKDIV). A signal level maintained for more than (FLT.DEBTOP) filter clock cycles (1-7) is considered non-bouncing and can pass through the filter.

The filtering function can be enabled or disabled via the configuration register (FLT.EN). Additionally, the filter counter only starts when the PCNT is enabled (RUN=1).

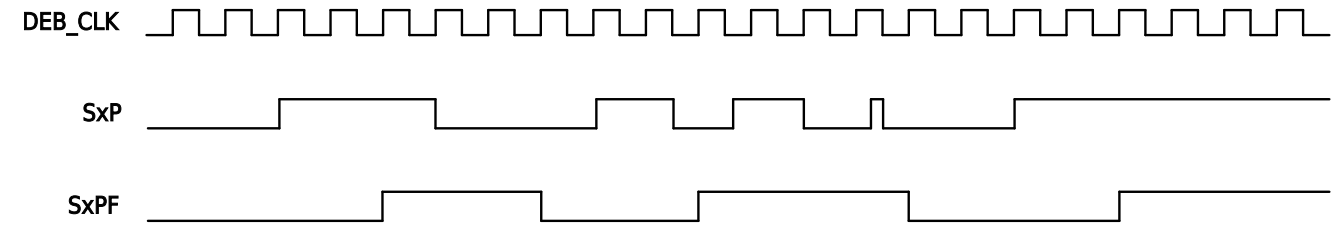

Figure 21-11 Pulse Width Filtering Waveform

The above figure shows the filtering waveform when FLT.DEBTOP=2.

Calculated as follows:

$$f_{DEB\_CLK} = \frac{f_{PCNT\_CLK}}{(\text{FLT.CLKDIV} + 1)}$$

21.3.5 Timeout

Enabling the timeout function (TOCR.EN) will use the filter clock (see Pulse Width Filtering) to incrementally count the duration of the pulse high level starting from 0. When a low level is detected, the counter resets to 0. If the high-level duration reaches the threshold value set by TOCR.TH, an interrupt flag (IF.TO) is generated.

The timeout function uses the filter clock and requires configuration of the division factor (FLT.CLKDIV), but it does not depend on whether the filter is enabled (FLT.EN). The timeout counter is activated only after the PCNT is started (RUN=1).

The overflow time calculation formula is as follows:

$$T_{TO} = \frac{(\text{FLT.CLKDIV} + 1) \times \text{TOCR.CH}}{f_{PCNT\_CLK}}$$

Note

When using the timeout function, refer to the relevant procedures in Automatic Wake-up Timer in Low-power Mode.

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21.3.6 Pulse Input Selection

In addition to supporting IO inputs as pulse inputs for the PCNT, this series also allows the selection of VC outputs as PCNT pulse inputs. The selection is configured through the GPIO_PCNT register. For details, refer to the "Register - Port Auxiliary Register" section in the chapter "General-Purpose I/O (GPIO)".

21.3.7 Debug Observation Output

To verify that the signals entering the pulse decoding module meet expectations, three sets of shaped pulses can be selected via registers for output through IO as PCNT_S0FO/PCNT_S1FO observation signals. These are:

- S0A/S1A
- S0P/S1P
- S0PF/S1PF

By observing the output pulse signal of PCNT_S0FO/PCNT_S1FO, the polarity selection and the configuration of the pulse width filter can be adjusted more intuitively to avoid that the input signal of the decoding circuit does not meet expectations.

21.4 Operation Example

21.4.1 Automatic Wake-Up Timer in Low-Power Mode

Context

Through proper configuration, PCNT can realize automatic wake-up in low power consumption mode, and its longest timing period is 1024 seconds.

Procedure

Step1. Set the GPIO_PCNT register to 0 to select IO as the input source for the PCNT.

Step2. Ensure that no port is configured as PCNT_S0 in the port function selection register (Pxx_SEL).

Step3. Set CTRL.MODE to 0, and select single channel mode.

Step4. Set CTRL.S0P to 1, and select polarity inversion for the S0 input channel.

Step5. Configure CTRL.CLKSEL, select XTL or RCL as the counter clock.

Step6. Configure FLT.CLKDIV to select the clock frequency division factor of the filter.

Step7. Configure TOCR.TH to select the timing period of the timeout timer.

Step8. Set TOCR.EN to 1 to enable the timeout timer.

Step9. Enable PCNT interrupt vector table.

Step10. Write 0 to ICR to clear all interrupt flags of PCNT.

Step11. Set IEN.TO to 1 to enable timeout interrupt.

Step12. Set RUN to 1 and start PCNT.

Step13. Enter low power consumption mode, wait for PCNT timeout interrupt to wake up MCU.

Step14. In the interrupt service routine, perform the following steps in sequence:

a. Set RUN to 0.
b. Write 0 to ICR.TO to clear the timeout interrupt flag.
c. Set PCNT_IEN.TO to 0.
d. Execute the functions required by the user.
e. Query until PCNT_RUN is 0.
f. Query until PCNT_IFR.TO is 0.
g. Exit the interrupt service routine.

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Step15. To start the timer again, repeat steps 11-14.

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21.5 Register Description

21.5.1 Register List

Base address: 0x40005400

Table 21-1 Pulse Counter (PCNT) Register Offset

Offset	Register	Description	Width
0x00	PCNT_RUN	PCNT Start Register (Asynchronous)	32
0x04	PCNT_CTRL	PCNT Control Register (Asynchronous long signal)	32
0x08	PCNT_FLT	PCNT Filter Control Register (Asynchronous long signal)	32
0x0C	PCNT_TOCR	PCNT Timeout Control Register (Asynchronous long signal)	32
0x10	PCNT_CMD	PCNT Command Register (Asynchronous)	32
0x14	PCNT_SR1	PCNT Status Register 1 (Synchronous)	32
0x18	PCNT_CNT	PCNT Count Register (Synchronous)	32
0x1C	PCNT_TOP	PCNT Count Overflow Register (Synchronous)	32
0x20	PCNT_BUF	PCNT Count Overflow Buffer Register (Asynchronous)	32
0x24	PCNT_IFR	PCNT Interrupt Flag Register (Synchronous)	32
0x28	PCNT_ICR	PCNT Interrupt Clear Register (Asynchronous)	32
0x2C	PCNT_IEN	PCNT Interrupt Enable Register (Asynchronous long signal)	32
0x30	PCNT_SR2	PCNT Status Register 2 (Asynchronous)	32
0x34	PCNT_DBG	PCNT Debug Observation Output Selection Register (Asynchronous long signal)	32

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21.5.2 PCNT Start Register (PCNT_RUN)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																															RUN
Access																																RW

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-
0	RUN	PCNT start/stop control ● 0b0: Stop ● 0b1: Start **Note** ● The current module regards the configuration register of the PCLK clock domain as a long signal, and does not synchronize to the PCNT_CLK clock domain. Therefore, when RUN=1 starts PCNT, the configuration register is not allowed to be modified to avoid unknown errors. All configuration register modifications must be performed in the PCNT stopped state (RUN=0). ● After writing a value to the RUN bit, a synchronization process is required to start/stop PCNT counting. Reading the RUN bit before the synchronization is completed will return the RUN status value before writing. Therefore, if you want to start PCNT after stopping PCNT, you need to write 0 to the RUN bit, and then continue other operations after checking that the RUN bit = 0 (including writing 1 to the Run bit to restart PCNT).	RW

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21.5.3 PCNT Control Register (PCNT_CTRL)

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																									S1P	S0P	DIR	CLKSEL		MODE	
Access																										RW	RW	RW	RW		RW	

Bit	Name	Functional Description	Access
31:7	*Reserved*	-	-
6	S1P	S1 channel input polarity selection ● 0b0: Not negated ● 0b1: Negate	RW
5	S0P	S0 channel input polarity selection ● 0b0: Not negated ● 0b1: Negate	RW
4	DIR	Counting direction selection ● 0b0: Count up ● 0b1: Count down **Note** Valid only in single-channel mode and dual-channel non-orthogonal mode.	RW
3:2	CLKSEL	PCNT_CLK count clock selection ● 0b00: PCLK ● 0b01: PCLK ● 0b10: XTL ● 0b11: RCL	RW
1:0	MODE	Pulse counting mode selection ● 0b00: Single channel pulse counting mode ● 0b01: Single channel pulse counting mode ● 0b10: Dual channel non-orthogonal pulse counting mode ● 0b11: Dual channel quadrature pulse counting mode	RW

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21.5.4 PCNT Filter Control Register (PCNT_FLT)

Offset	Bit Position																													
0x08	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00002000																															
Name	Reserved															EN	DEBTOP			CLKDIV												
Access																RW	RW			RW												

Bit	Name	Functional Description	Access
31:17	*Reserved*	-	-
16	EN	Pulse width filter enable control ● 0b0: Disable ● 0b1: Enable	RW
15:13	DEBTOP	Counter threshold Use the filter clock to continuously sample the input pulse. When the continuous level sampling count value reaches the threshold, it is regarded as a normal pulse and can pass through the filter. **0b000: Illegal Value**	RW
12:0	CLKDIV	Filter clock frequency division factor Coefficient = CLKDIV + 1	RW

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21.5.5 PCNT Timeout Control Register (PCNT_TOCR)

Offset	Bit Position																													
0x0C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000FFF																															
Name	Reserved															EN	Reserved				TH											
Access																RW					RW											

Bit	Name	Functional Description	Access
31:17	*Reserved*	-	-
16	EN	Timeout function enable control ● 0b0: Disable ● 0b1: Enable	RW
15:12	*Reserved*	-	-
11:0	TH	Timeout threshold When the pulse high level is filtered by the clock and the continuous sampling count reaches the threshold, an overtime interrupt flag is generated, and the counter restarts counting	RW

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21.5.6 PCNT Command Register (PCNT_CMD)

Offset	Bit Position																													
0x10	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																													B2C	B2T	T2C
Access																														WO	WO	WO

Bit	Name	Functional Description	Access
31:3	*Reserved*	-	-
2	B2C	BUF-to-CNT synchronization control Writing 1 immediately synchronizes the value in BUF to CNT; writing 0 has no effect. The corresponding bit of PCNT_SR2 is 1 during the synchronization process. At this time, the BUF should not be written, and the CNT should not be read.	WO
1	B2T	BUF-to-TOP synchronization control Writing 1 immediately synchronizes the value in BUF to TOP; writing 0 has no effect. The corresponding bit of PCNT_SR2 is 1 during the synchronization process. At this time, BUF should not be written, and TOP should not be read.	WO
0	T2C	TOP-to-CNT synchronization control Writing 1 immediately synchronizes the value in TOP to CNT; writing 0 has no effect. During the synchronization process, the corresponding bit of PCNT_SR2 is 1. At this time, 1 should not be written to B2T, and CNT should not be read.	WO

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21.5.7 PCNT Status Register 1 (PCNT_SR1)

Offset	Bit Position																													
0x14	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																															DIR
Access																																RO

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-
0	DIR	Dual-channel quadrature pulse counting direction indication ● 0b0: Count up ● 0b1: Count down	RO

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21.5.8 PCNT Count Register (PCNT_CNT)

Offset	Bit Position																													
0x18	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																						CNT									
Access																							RO									

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	CNT	Counter Count Value	RO

21.5.9 PCNT Count Overflow Register (PCNT_TOP)

Offset	Bit Position																													
0x1C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000000FF																															
Name	Reserved																						TOP									
Access																							RO									

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	TOP	Counter overflow threshold/counter underflow reload value	RO

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21.5.10 PCNT Count Overflow Buffer Register (PCNT_BUF)

Offset	Bit Position																													
0x20	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000000FF																															
Name	Reserved																BUF															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	BUF	CNT register/TOP register cache	RW

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21.5.11 PCNT Interrupt Flag Register (PCNT_IFR)

Offset	Bit Position																													
0x24	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								S1E	S0E	BB	FE	DIR	TO	OV	UF
Access																									RO	RO	RO	RO	RO	RO	RO	RO

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7	S1E	Pulse decode error interrupt flag In a complete sampling period of non-interlaced coding, the S1 channel does not change. It is only valid in dual-channel non-interlaced encoding mode.	RO
6	S0E	Pulse decode error interrupt flag In a complete sampling period of non-interlaced coding, the S0 channel does not change. It is only valid in dual-channel non-interlaced encoding mode.	RO
5	BB	Pulse decode error interrupt flag Dual-channel pulses are sampled back-to-back as high, with no low state in between. It is only valid in dual-channel non-interlaced encoding mode.	RO
4	FE	Pulse decode error interrupt flag In a complete sampling period of non-intersection coding, what is sampled is not a correct non-interlaced encoding frame. It is only valid in dual-channel non-interlaced encoding mode.	RO
3	DIR	Quadrature pulse direction change interrupt flag Quadrature pulses are interpreted by the decoder as a change in count direction. Valid only for dual-channel quadrature pulses.	RO
2	TO	Timeout interrupt flag	RO
1	OV	Overflow interrupt flag	RO
0	UF	Underflow interrupt flag	RO

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21.5.12 PCNT Interrupt Clear Register (PCNT_ICR)

Offset	Bit Position																													
0x28	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000000FF																															
Name	Reserved																								S1E	S0E	BB	FE	DIR	TO	OV	UF
Access																									WO	WO	WO	WO	WO	WO	WO	WO

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7	S1E	Pulse decode error interrupt flag cleared Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
6	S0E	Pulse decode error interrupt flag cleared Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
5	BB	Pulse decode error interrupt flag cleared Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
4	FE	Pulse decode error interrupt flag cleared Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
3	DIR	Quadrature pulse direction change interrupt flag cleared Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
2	TO	Timeout interrupt flag cleared Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
1	OV	Overflow interrupt flag cleared Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
0	UF	Underflow interrupt flag cleared Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO

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21.5.13 PCNT Interrupt Enable Register (PCNT_IEN)

Offset	Bit Position																													
0x2C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								S1E	S0E	BB	FE	DIR	TO	OV	UF
Access																									RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7	S1E	Pulse decode error interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
6	S0E	Pulse decode error interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
5	BB	Pulse decode error interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
4	FE	Pulse decode error interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
3	DIR	Quadrature pulse direction change interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
2	TO	Timing interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
1	OV	Overflow interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
0	UF	Underflow interrupt enable ● 0b0: Disable ● 0b1: Enable	RW

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21.5.14 PCNT Status Register 2 (PCNT_SR2)

Offset	Bit Position																													
0x30	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																													B2C	B2T	T2C
Access																														RO	RO	RO

Bit	Name	Functional Description	Access
31:3	*Reserved*	-	-
2	B2C	The synchronization status bit when synchronizing the value in BUF to CNT ● 0b0: Synchronization is complete. ● 0b1: Synchronization is in progress and CNT register cannot be read.	RO
1	B2T	The synchronization status bit when synchronizing the value in BUF to TOP ● 0b0: Synchronization is complete. ● 0b1: Synchronization is in progress and TOP register cannot be read.	RO
0	T2C	The synchronization status bit when synchronizing the value in TOP to CTN ● 0b0: Synchronization is complete. ● 0b1: Synchronization is in progress and CNT register cannot be read.	RO

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21.5.15 PCNT Debug Observation Output Selection Register (PCNT_DBG)

Offset	Bit Position																													
0x34	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																														DBG	
Access																															RW	

Bit	Name	Functional Description	Access
31:2	*Reserved*	-	-
1:0	DBG	Select the source of pulse PCNT_S0FO/PCNT_S1FO observation output ● 0b00: Fixed to 0 ● 0b01: Output after pulse synchronization (S0A/S1A) ● 0b10: Output after pulse polarity selection (S0P/S1P) ● 0b11: Output after pulse filtering (S0PF/S1PF)	RW

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22 UART

22.1 Introduction

Universal Asynchronous Receiver/Transmitter (UART) can flexibly perform full-duplex data exchange with external devices. It supports synchronous half-duplex, single-wire half-duplex communication, as well as multi-processor communication. It is often used in short-distance, low-speed serial communication. The UART provides a variety of baud rates through a programmable baud rate generator. UART supports multiple working modes.

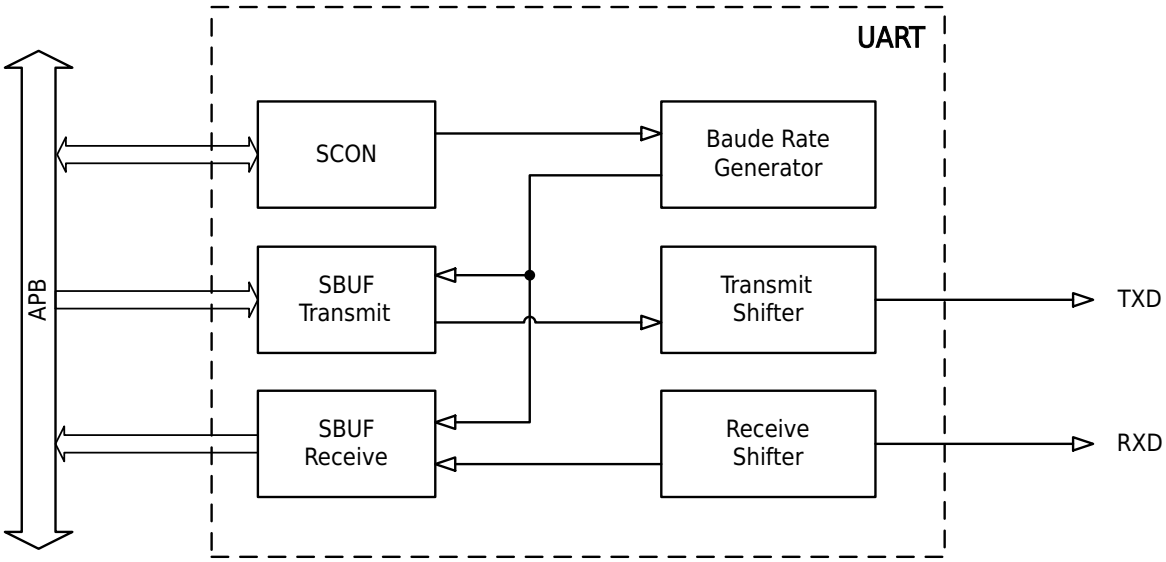

Figure 22-1 UART Structure Diagram

22.2 Features

- Support synchronous half-duplex, asynchronous full-duplex and single-line half-duplex transmission.
- Programmable serial communication function
  - 2 character lengths: 8 bits, 9 bits
  - 3 check methods: no check, odd check, even check
  - 3 stop lengths: 1 bit, 2 bits, 1.5 bits
- 16-bit baud rate counter
- Support hardware flow control (RTS, CTS)
- Support multi-machine communication and automatic address recognition
- Support data transfer via DMA

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22.3 Functional Description

22.3.1 Working Mode

UART supports multiple working modes: synchronous half-duplex mode, asynchronous full-duplex mode, and single-wire half-duplex mode. By matching UART_SCON.SM and UART_SCON.HDSEL, various required working modes can be configured.

22.3.1.1 Mode0-Mode3 Function Comparison

Configure UARTx_SCON.SM to select different transmission modes: Mode0-Mode3. The main function comparison of these four working modes is shown in the table below:

Table 22-1 UART Mode0/1/2/3 Data Structure

Working Mode		Transmission Bit Width	Data Composition	Baud Rate
Mode0	Synchronous half-duplex mode	8-bit	Data (8bits)	$\text{BaudRate} = \frac{f_{PCLK}}{12}$
Mode1	Asynchronous full-duplex mode	10: 11-bit	Start (1bit) + Data (8bits) + Stop (1-2bits)	$\text{BaudRate} = \frac{f_{PCLK}}{\text{OVER} \times \text{SCNT}}$
Mode2	Asynchronous full-duplex mode	11: 12-bit	Start (1bit) + Data (8bits) + B8 (1bit) + Stop (1-2bits)	$\text{BaudRate} = \frac{f_{PCLK}}{\text{OVER}}$
Mode3	Asynchronous full-duplex mode	11: 12-bit	Start (1bit) + Data (8bits) + B8 (1bit) + Stop (1-2bits)	$\text{BaudRate} = \frac{f_{PCLK}}{\text{OVER} \times \text{SCNT}}$

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Note

- Mode0 can only be used as a master to send UART synchronous shift clock, and cannot be used as a slave to receive UART synchronous shift clock input from the outside.
- f_{PCLK} represents the frequency of the current PCLK.
- OVER value:
  - When UART_SCON.OVER = 0b0, in Mode1/3, the value of OVER is 16; in Mode2, the value of OVER is 32.
  - When UART_SCON.OVER = 0b1, in Mode1/3, the value of OVER is 8; in Mode2, the value of OVER is 16.
- For the definition of SCNT, refer to the introduction of the register UART_SCNT.
- The B8 data bit is special and has different meanings in different applications, refer to the following table:

Table 22-2 B8 Data Meaning

Application Scenario	UART_SCON.ADRDET	UART_SCON.B8CONT[1:0]	B8 Data Meaning
Parity check	-	0b01/0b10	When receiving, B8 is the parity bit of the received 8bits data. When transmitting, B8 is the parity bit of the 8bits data to be sent.
Multi-machine communication	0b1	-	B8=1 indicates that the current frame is an address frame. B8=0 indicates that the current frame is a data frame.
Other	0b0	0b00/0b11	Bit8 receiving/sending data.

When the multi-machine communication mode is turned on, the parity check of the received data is automatically closed; the parity check of the sent data is still controlled by B8CONT.

22.3.1.2 Mode0 Data Transmitting and Receiving

- Mode0 Transmit Data

  When transmitting data, clear the UART_SCON.REN bit and write the data into the UART_SBUF register. At this time, the transmitting data is output from RXD (low bit first, high bit later), and the synchronous shift clock is output from TXD.

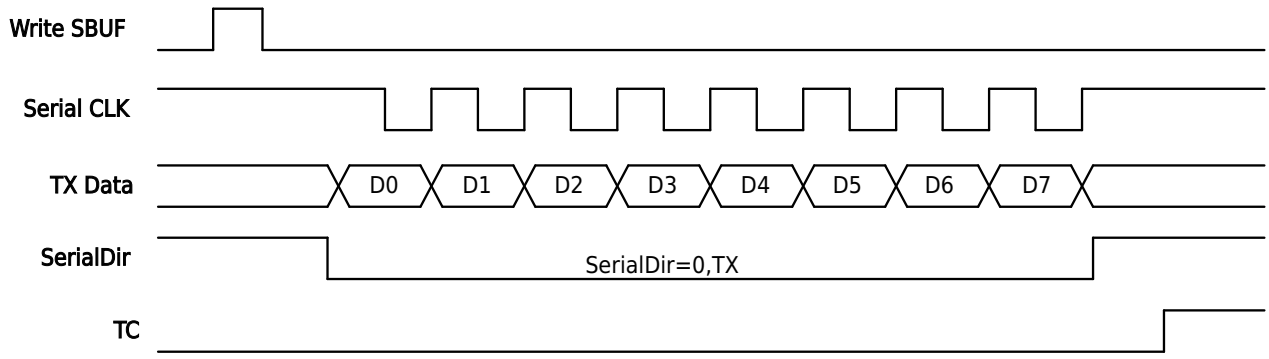

Figure 22-2 Mode0 Transmit Data

- Mode0 Receive Data

  When receiving data, set the UART_SCON.REN bit to 1 and clear the UART_ISR.RC bit. When reception is complete, data can be read from the UART_SBUF register. At this time, the received data is input from RXD (low bit first, high bit later), and the synchronous shift clock is output from TXD.

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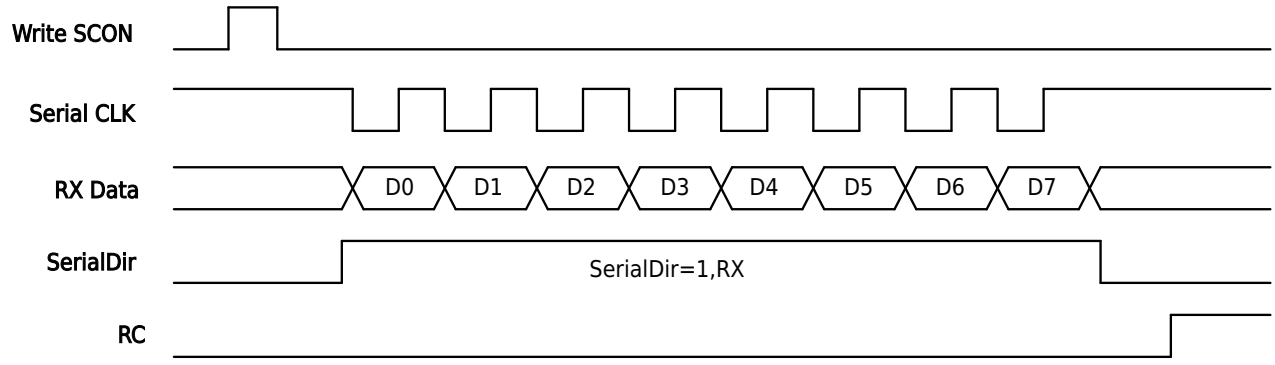

Figure 22-3 Mode0 Receive Data

22.3.1.3 Mode1 Data Transmitting and Receiving

- Mode1 Transmit Data

  When transmitting data, regardless of the UART_SCON.REN bit value, writing the data to be sent into the UART_SBUF register will cause the data to shift out from TXD (low bit first, high bit later).

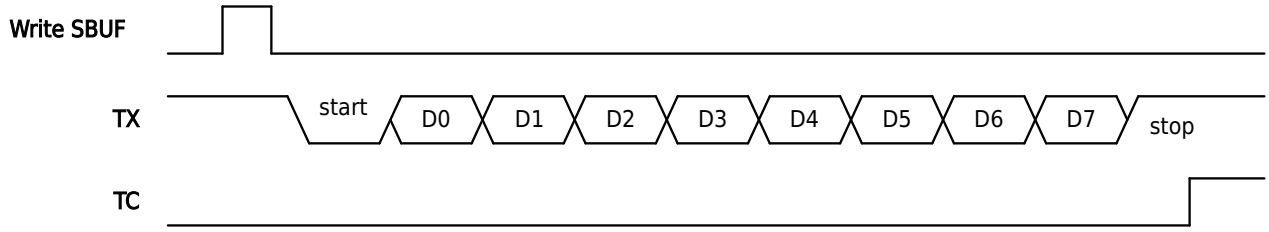

Figure 22-4 Mode1 Transmit Data

- Mode1 Receive Data

  When receiving data, set the UART_SCON.REN bit to 1 and clear the UART_ISR.RC bit to 0. Start to receive the data on RXD (low bit first, high bit later), when the reception is completed, it can be read from the UART_SBUF register.

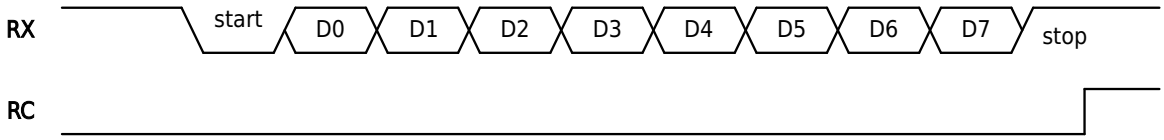

Figure 22-5 Mode1 Receive Data

22.3.1.4 Mode2 Data Transmitting and Receiving

- Mode2 Transmit Data

  When transmitting data, regardless of the UART_SCON.REN bit value, writing the data to be sent into the UART_SBUF register will cause the data to shift out from TXD (low bit first, high bit later).

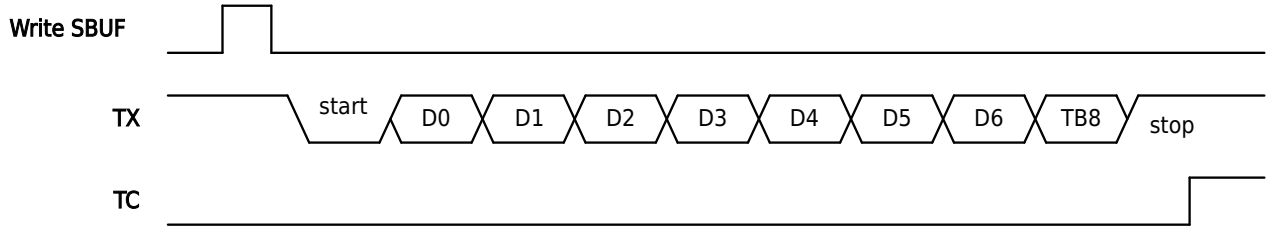

Figure 22-6 Mode2 Transmit Data

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- Mode2 Receive Data

  When receiving data, set the UART_SCON.REN bit to 1 and clear the UART_ISR.RC bit to 0. Start receiving data on RXD (low bit first, high bit later). Upon completion, it can be read from the UART_SBUF register.

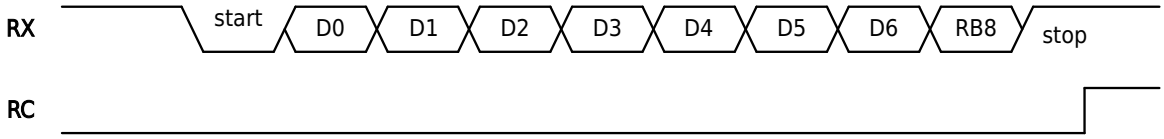

Figure 22-7 Mode2 Receive Data

22.3.1.5 Mode3 Data Transmitting and Receiving

- Mode3 Transmit Data

  When transmitting data, regardless of the UART_SCON.REN bit value, writing the data to be sent into the UART_SBUF register will cause the data to shift out from TXD (low bit first, high bit later).

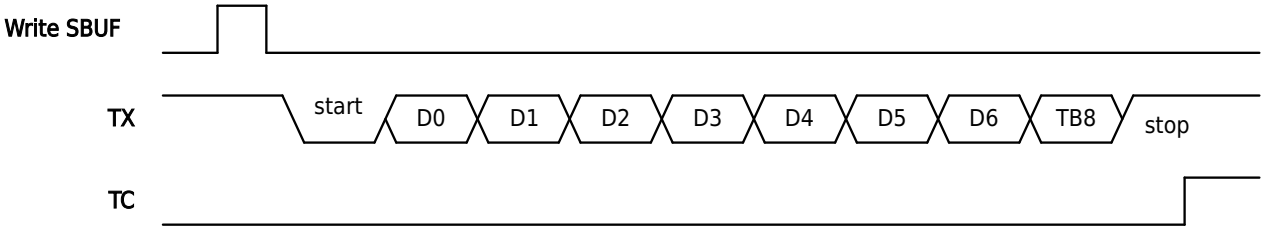

Figure 22-8 Mode3 Transmit Data

- Mode3 Receive Data

  When receiving data, set the UART_SCON.REN bit to 1 and clear the UART_ISR.RC bit to 0. Start to receive the data on RXD (low bit first, high bit later), when the reception is completed, it can be read from the UART_SBUF register.

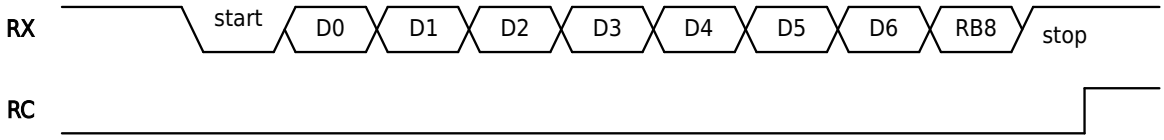

Figure 22-9 Mode3 Receive Data

22.3.1.6 Description of Single-wire Half-duplex Data Transmitting and Receiving

When UART_SCON.HDSEL=0b1, the single-wire half-duplex transmission mode can be enabled:

- The TX and RX signal lines are connected inside the module.
- The RX signal is no longer used, and the received and sent data are all completed through the TX signal. Direction control of TX signal is done by hardware logic without software control.
- When the transmit buffer is empty, the TX signal is always input (receiving state), once a data is filled into the transmit buffer, the TX signal becomes output (transmitting state), when the transmitting is completed, the transmit buffer becomes empty, and the TX signal back to input.
- When there is no data transmission, the TXD pin is always in the input state. The user program needs to configure this pin as an open-drain output and connect an external pull-up resistor.

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Notice

1. Even if the module is in the receiving process, as long as the transmit buffer is filled with data, the TX signal will immediately become output (transmitting state), the receiving process will be interrupted, and an incorrect received data will be obtained.
2. The similarities and differences between single-line half-duplex mode and Mode0 mode:
   - Similarities: Both use one signal to time-division multiplex to complete data transmission and reception.
   - Differences: Mode0 is synchronous transmission with a synchronous clock, while the single-wire half-duplex mode is asynchronous transmission, all baud rate calculations still follow the baud rate formula of Mode1-2-3, only the transceiver function is multiplexed to the TX signal.

22.3.2 Baud Rate Generation

The baud rate generation formulas differ between Mode0 to Mode3:

- Mode0 baud rate generation formula: $\text{BaudRate} = \frac{f_{PCLK}}{12}$
- Mode1 baud rate generation formula: $\text{BaudRate} = \frac{f_{PCLK}}{\text{OVER} \times \text{SCNT}}$
- Mode2 baud rate generation formula: $\text{BaudRate} = \frac{f_{PCLK}}{\text{OVER}}$
- Mode3 baud rate generation formula: $\text{BaudRate} = \frac{f_{PCLK}}{\text{OVER} \times \text{SCNT}}$

Note

- f_{PCLK} represents the frequency of the current PCLK.
- OVER value:
  - When UART_SCON.OVER = 0b0, in Mode1/3, the value of OVER is 16; in Mode2, the value of OVER is 32.
  - When UART_SCON.OVER = 0b1, in Mode1/3, the value of OVER is 8; in Mode2, the value of OVER is 16.
- For the definition of SCNT, refer to the introduction of the register UART_SCNT.

Mode1/Mode3 Baud Rate Setting Example

Table 22-3 PCLK=4MHz Baud Rate Calculation Table

Baud Rate	PCLK=4MHz					
	OVER=8			OVER=16		
	CNT	Actual Baud Rate	Error%	CNT	Actual Baud Rate	Error%
2400	208	2403.85	0.16%	104	2403.85	0.16%
4800	104	4807.69	0.16%	52	4807.69	0.16%
9600	52	9615.38	0.16%	26	9615.38	0.16%
19200	26	19230.77	0.16%	13	19230.77	0.16%
38400	13	38461.54	0.16%	7	35714.29	-6.99%
57600	9	55555.56	-3.55%	4	62500.00	8.51%
76800	7	71428.57	-6.99%	3	83333.33	8.51%
115200	4	125000.00	8.51%	2	125000.00	8.51%
128000	4	125000.00	-2.34%	2	125000.00	-2.34%
250000	2	250000.00	0.00%	1	250000.00	0.00%

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Table 22-4 PCLK=8MHz Baud Rate Calculation Table

Baud Rate	PCLK=8MHz					
	OVER=8			OVER=16		
	CNT	Actual Baud Rate	Error%	CNT	Actual Baud Rate	Error%
2400	417	2398.08	-0.08%	208	2403.85	0.16%
4800	208	4807.69	0.16%	104	4807.69	0.16%
9600	104	9615.38	0.16%	52	9615.38	0.16%
19200	52	19230.77	0.16%	26	19230.77	0.16%
38400	26	38461.54	0.16%	13	38461.54	0.16%
57600	17	58823.53	2.12%	9	55555.56	-3.55%
76800	13	76923.08	0.16%	7	71428.57	-6.99%
115200	9	111111.11	-3.55%	4	125000.00	8.51%
128000	8	125000.00	-2.34%	4	125000.00	-2.34%
256000	4	250000.00	-2.34%	2	250000.00	-2.34%
500000	2	500000.00	0.00%	1	500000.00	0.00%

Table 22-5 PCLK=16MHz Baud Rate Calculation Table

Baud Rate	PCLK=16MHz					
	OVER=8			OVER=16		
	CNT	Actual Baud Rate	Error%	CNT	Actual Baud Rate	Error%
2400	833	2400.96	0.04%	417	2398.08	-0.08%
4800	417	4796.16	-0.08%	208	4807.69	0.16%
9600	208	9615.38	0.16%	104	9615.38	0.16%
19200	104	19230.77	0.16%	52	19230.77	0.16%
38400	52	38461.54	0.16%	26	38461.54	0.16%
57600	35	57142.86	-0.79%	17	58823.53	2.12%
76800	26	76923.08	0.16%	13	76923.08	0.16%
115200	17	117647.06	2.12%	9	111111.11	-3.55%
128000	16	125000.00	-2.34%	8	125000.00	-2.34%
256000	8	250000.00	-2.34%	4	250000.00	-2.34%
500000	4	500000.00	0.00%	2	500000.00	0.00%
1000000	2	1000000.00	0.00%	1	1000000.00	0.00%

Table 22-6 PCLK=24MHz Baud Rate Calculation Table

Baud Rate	PCLK=24MHz					
	OVER=8			OVER=16		
	CNT	Actual Baud Rate	Error%	CNT	Actual Baud Rate	Error%
2400	1250	2400.00	0.00%	625	2400.00	0.00%
4800	625	4800.00	0.00%	313	4792.33	-0.16%
9600	313	9584.66	-0.16%	156	9615.38	0.16%
19200	156	19230.77	0.16%	78	19230.77	0.16%
38400	78	38461.54	0.16%	39	38461.54	0.16%
57600	52	57692.31	0.16%	26	57692.31	0.16%
76800	39	76923.08	0.16%	20	75000.00	-2.34%
115200	26	115384.62	0.16%	13	115384.62	0.16%
128000	23	130434.78	1.90%	12	125000.00	-2.34%
256000	12	250000.00	-2.34%	6	250000.00	-2.34%

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Baud Rate	PCLK=24MHz					
	OVER=8			OVER=16		
	CNT	Actual Baud Rate	Error%	CNT	Actual Baud Rate	Error%
1000000	3	1000000.00	0.00%	2	750000.00	-25.00%
1500000	2	1500000.00	0.00%	1	1500000.00	0.00%

Table 22-7 PCLK=32MHz Baud Rate Calculation Table

Baud Rate	PCLK=32MHz					
	OVER=8			OVER=16		
	CNT	Actual Baud Rate	Error%	CNT	Actual Baud Rate	Error%
2400	1667	2399.52	-0.02%	833	2400.96	0.04%
4800	833	4801.92	0.04%	417	4796.16	-0.08%
9600	417	9592.33	-0.08%	208	9615.38	0.16%
19200	208	19230.77	0.16%	104	19230.77	0.16%
38400	104	38461.54	0.16%	52	38461.54	0.16%
57600	69	57971.01	0.64%	35	57142.86	-0.79%
76800	52	76923.08	0.16%	26	76923.08	0.16%
115200	35	114285.71	-0.79%	17	117647.06	2.12%
128000	31	129032.26	0.81%	16	125000.00	-2.34%
256000	16	250000.00	-2.34%	8	250000.00	-2.34%
1000000	4	1000000.00	0.00%	2	1000000.00	0.00%
2000000	2	2000000.00	0.00%	1	2000000.00	0.00%

Table 22-8 PCLK=48MHz Baud Rate Calculation Table

Baud Rate	PCLK=48MHz					
	OVER=8			OVER=16		
	CNT	Actual Baud Rate	Error%	CNT	Actual Baud Rate	Error%
2400	2500	2400.00	0.00%	1250	2400.00	0.00%
4800	1250	4800.00	0.00%	625	4800.00	0.00%
9600	625	9600.00	0.00%	313	9584.66	-0.16%
19200	313	19169.33	-0.16%	156	19230.77	0.16%
38400	156	38461.54	0.16%	78	38461.54	0.16%
57600	104	57692.31	0.16%	52	57692.31	0.16%
76800	78	76923.08	0.16%	39	76923.08	0.16%
115200	52	115384.62	0.16%	26	115384.62	0.16%
128000	47	127659.57	-0.27%	23	130434.78	1.90%
256000	23	260869.57	1.90%	12	250000.00	-2.34%
1000000	6	1000000.00	0.00%	3	1000000.00	0.00%
2000000	3	2000000.00	0.00%	2	1500000.00	-25.00%
3000000	2	3000000.00	0.00%	1	3000000.00	0.00%

22.3.3 Frame Error Detection

When operating in Mode1/2/3, the UART features frame error detection capability:

- If the hardware fails to identify the stop bit within the expected time during data reception, resulting in synchronization loss or excessive noise, a frame error will be detected
- When a frame error is detected, UART_ISR.FE is set to 1. The UART_ISR.FE must be cleared by software in a timely manner.

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22.3.4 Multi-machine Communication

When working in Mode2/3, set the UART_SCON.ADRDET to 1 to enable the multi-machine communication address automatic identification function. The master can transmit address frames and data frames, and the slave can receive data frames only after receiving matching address frames.

Master Transmitting Address and Data Frame

When UART_SBUF.DATA8 is 1, the address frame is transmitted, UART_SBUF.DATA is the address of the target slave.

When UART_SBUF.DATA8 is 0, the data frame is transmitted, UART_SBUF.DATA is the data to be transmitted.

Slave Receiving Address and Data Frame

When UART_SCON.ADRDET is 1, the slave only receives address frames that match its own address, ignoring data frames and unmatched address frames. When the slave receives the address frame from RXD, the hardware automatically compares the address in the address frame with the local address. Only when the two match, the received address is stored in the UART_SBUF register and UART_ISR.RC is set.

When UART_SCON.ADRDET is 0, the slave only receives data frames and ignores address frames. The user program should set UART_SCON.ADRDET to 0 after the address matches to receive subsequent data frames transmitted by the master.

Slave Address Configuration

The slave address consists of the broadcast address and the user configuration address:

- Broadcast Address: UART_SADDR | UART_SADEN
- User Configuration Address: UART_SADDR & UART_SADEN

When an address frame is received, if the address received from the bus, after being ANDed with the value of UART_SADEN, matches the user-configured address, or if the received address, after being ANDed with the broadcast address, matches the broadcast address, it is considered that an address frame matching the slave address has been received.

Example: UART_SADDR=0x55, UART_SADEN=0xF0, then the slave can match addresses 0xF5, 0xF7, 0xFD, 0xFF (broadcast address) and 0x50~0x5F (user-configured address).

22.3.5 DMAC Hardware Handshake

UART module supports the hardware handshake logic of the DMAC.

- Setting UART_SCON.DMACTXEN to 1 enables the DMAC hardware handshake logic of UART TX.

  When the transmit buffer is empty, the UART will send a data transfer request TX REQ to the DMAC. Upon receiving this signal, the DMAC transfers one frame of transmit data from the source address to the UART_SBUF register. The above steps are repeated until all the data lengths configured in the DMAC are transferred.
- Setting UART_SCON.DMACRXEN to 1 enables the DMAC hardware handshake logic of UART RX.

  When a frame is received, the UART will send a data transfer request RX REQ to the DMAC. When the DMAC receives this signal, it transfers the received data from the UART_SBUF register to the DMAC destination address. The above steps are repeated until all the data lengths configured in the DMAC are transferred.

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22.3.6 Hardware Flow Control

UART hardware flow control can be realized by adding nCTS and nRTS signals, that is, the UART hardware module automatically controls the transmitting and receiving of data according to the high and low levels of nCTS and nRTS, without judging by software. The hardware flow control diagram between two UART modules is shown below:

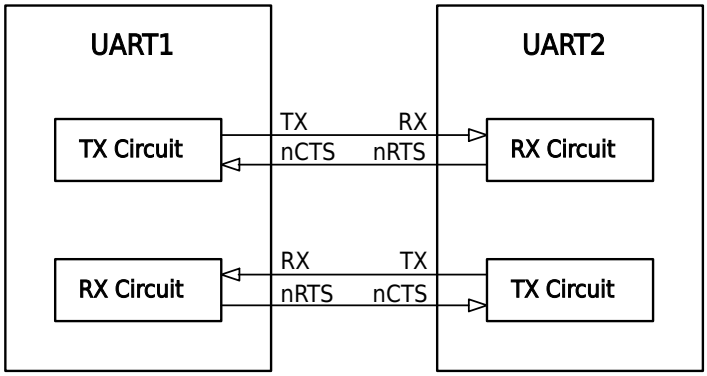

Figure 22-10 UART Hardware Flow Control

nRTS Flow Control

When nRTS flow control is enabled (UART_SCON.RTSEN set to 1):

- When the UART receive buffer is empty, it drives nRTS active (connected to low level).
- When the receive buffer is full, nRTS will become invalid (connected to a high level), indicating that the transmitting process will stop after the end of the current frame.

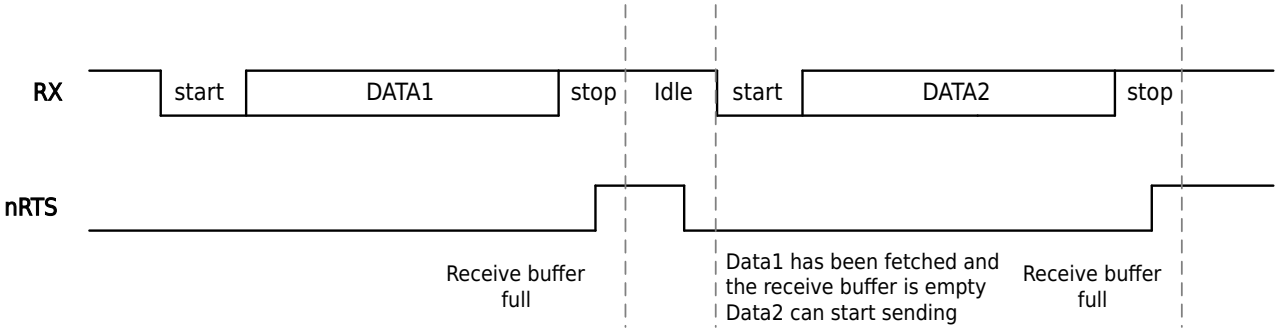

Figure 22-11 nRTS Hardware Flow Control Signal

nCTS Flow Control

When nCTS flow control is enabled (UART_SCON.CTSEN set to 1), the high and low level of the nCTS is determined before the UART transmitting the next frame:

- If nCTS is active (connected to low level), the UART transmits the next frame of data.
- If nCTS is invalid (connected to high level), UART will suspend transmitting the next frame of data after the current frame is sent.

When nCTS flow control is enabled, any inversion of the nCTS signal will trigger hardware to set UART_ISR.CTSIF to 1. If UART_SCON.CTSIE is set to 1, an interrupt will be generated, while the high and low level of the nCTS signal is recorded in the UART_ISR.CTS flag bit.

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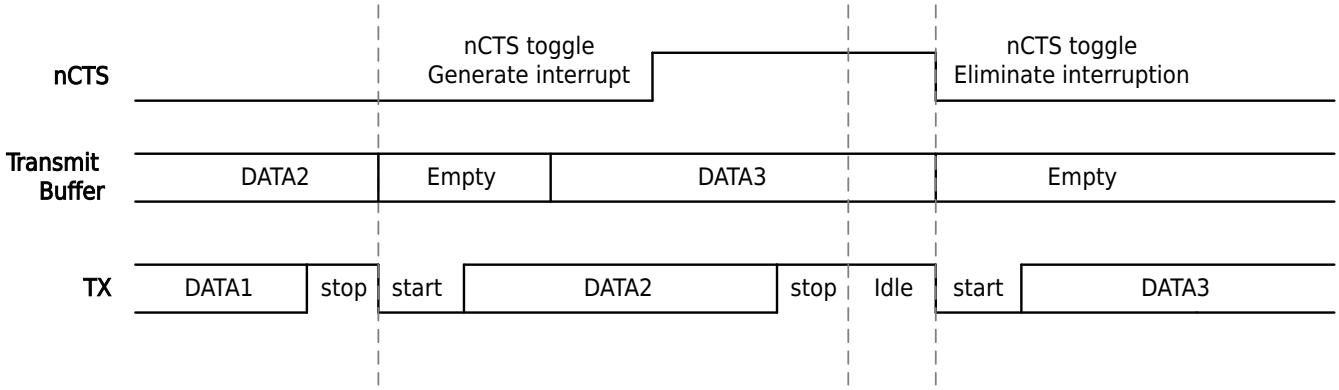

Figure 22-12 nCTS Hardware Flow Control Signal

22.3.7 Receive/Transmit Buffer

Receive Buffer

The UART module's receiver has a one-frame (8bits/9bits) buffer that holds the received data frame until the stop bit of the next frame is received before updating.

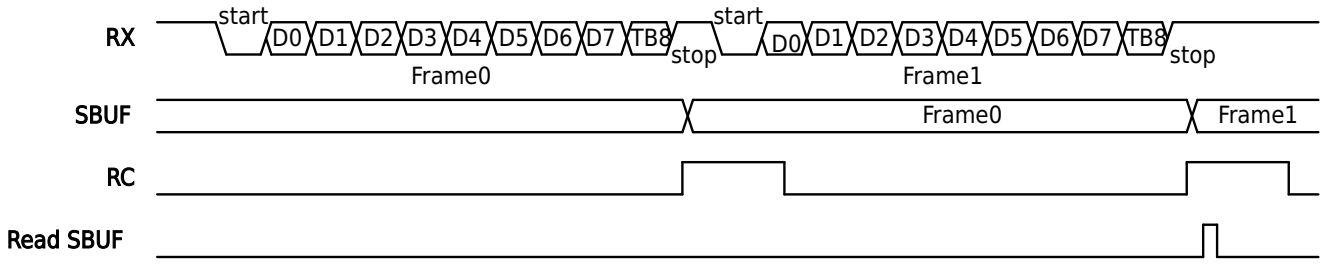

Figure 22-13 Receive Buffer

Transmit Buffer

The UART module's transmitter contains a one-frame (8bits/9bits) buffer. While transmitting the current frame, the next data to be sent can be written to UART_SBUF by software.

When UART_ISR.TXE=0, it indicates the transmit buffer is full, and the next transmit data cannot be written to UART_SBUF.

When UART_ISR.TXE=1, it indicates the transmit buffer is empty, allowing the next transmit data to be written to UART_SBUF. Upon completing the current data transmission, the hardware automatically loads the data from the transmit buffer into the shift register for transmitting.

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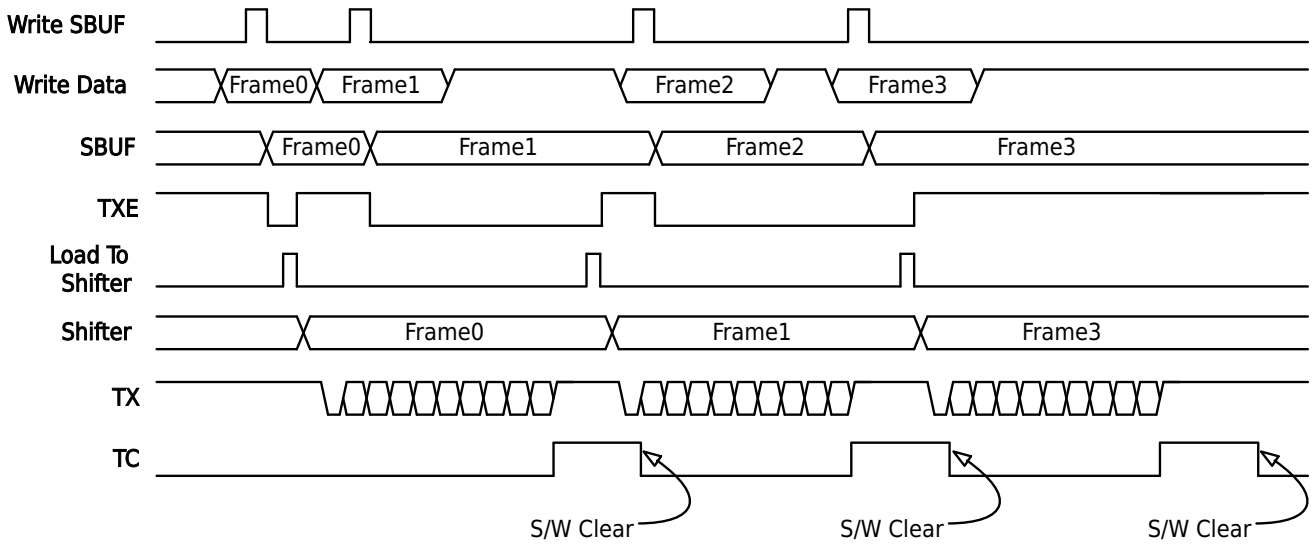

Figure 22-14 Transmit Buffer

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22.4 Register Description

22.4.1 Register List

- UART0 base address: 0x40000000
- UART1 base address: 0x40000100
- UART2 base address: 0x40006000
- UART3 base address: 0x40006400

Table 22-9 Universal Asynchronous Receiver/Transmitter (UART) Register Offset

Offset	Register	Description	Width
0x00	UART_SBUF	Data Register	32
0x04	UART_SCON	Control Register	32
0x08	UART_SADDR	Address Register	32
0x0C	UART_SADEN	Address Mask Register	32
0x10	UART_ISR	Interrupt Flag Register	32
0x14	UART_ICR	Interrupt Flag Clear Register	32
0x18	UART_SCNT	Baud Rate Register	32

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22.4.2 Data Register (UART_SBUF)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																							DATA8	DATA							
Access																								RW	RW							

Bit	Name	Functional Description	Access
31:9	*Reserved*	-	-
8	DATA8	Bit8 data bit ● In Mode0/1, read this bit is 0, write this bit is invalid ● In Mode2/3, there are such situations: ▶ When the hardware parity bit is turned on, this bit is the parity bit of the received data when receiving, and the verification is performed by the hardware. If the verification error occurs, the verification error flag bit PE is set to 1; this bit is invalid when transmitting, the parity bit of the transmit data is calculated and sent by the hardware. ▶ When the hardware parity bit is turned off, this bit is received data Bit8 when receiving; this bit is transmit data Bit8 when transmitting. **Note** When the multi-machine communication mode is turned on, the parity check of the received data is automatically closed; the parity check of the transmit data is still controlled by B8CONT.	RW
7:0	DATA	Data When transmitting data, write the transmit data into this register; when receiving data, read the received data from this register after the reception is complete.	RW

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22.4.3 Control Register (UART_SCON)

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved									HDSEL	FEIE	CTSIE	CTSEN	RTSEN	DMATXEN	DMARXEN	STOPBIT	PEIE	Reserved				OVER	TXEIE	SM		ADRDET	REN		B8CONT	TCIE	RCIE
Access										RW	RW	RW	RW	RW	RW	RW	RW	RW					RW	RW	RW		RW	RW		RW	RW	RW

Bit	Name	Functional Description	Access
31:23	*Reserved*	-	-
22	HDSEL	Single-wire half-duplex mode enable ● 0b0: Disable ● 0b1: Enable	RW
21	FEIE	Frame error interrupt enable ● 0b0: Disable ● 0b1: Enable The data reception flag is generated upon completion of the stop bit reception. The frame error interrupt and the data reception interrupt are different due to different stop bit configurations, the frame error interrupt occurs earlier than the data reception interrupt. When using this interrupt enable, notes as follows: ● Method 1: Disable the FEIE interrupt enable. After receiving a data interrupt, determine whether the data is correct by checking if the ISR.FE frame error flag is set via software. ● Method 2: Disable the FEIE interrupt enable. After receiving a data interrupt, determine data correctness through alternative methods.	RW
20	CTSIE	CTS signal flip interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
19	CTSEN	CTS signal enable control ● 0b0: Disable ● 0b1: Enable	RW
18	RTSEN	RTS signal enable control ● 0b0: Disable ● 0b1: Enable	RW
17	DMATXEN	Enable the hardware handshake signal for TX DMAC ● 0b0: Disable ● 0b1: Enable	RW
16	DMARXEN	Enable the hardware handshake signal for RX DMAC ● 0b0: Disable ● 0b1: Enable	RW

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Bit	Name	Functional Description	Access
15:14	STOPBIT	Stop Bit length selection ● 0b00: 1-bit ● 0b01: 1.5-bit ● 0b10: 2-bit ● 0b11: Setting prohibited **Note** In Mode0, although there is no Stop Bit, the STOPBIT[1:0] must still be set to 0b00.	RW
13	PEIE	Parity error interrupt enable ● 0b0: Disable ● 0b1: Enable The data receiving flag is generated when the data stop bit is received. The hardware parity check and the data receiving interrupt are different due to the stop bit settings. The parity check error interrupt will be ahead of the data receiving interrupt. When using this interrupt enable, notes as follows: ● Method 1: Disable the PEIE interrupt enable, and the software judges whether the ISR.PE parity check is correct after receiving the data interrupt. ● Method 2: Disable the PEIE interrupt enable, receive data interrupt and judge whether the parity is correct by receiving SBUF.DATA8 software.	RW
12:10	*Reserved*	-	-
9	OVER	Oversampling control ● Mode0: invalid ● Mode1/3: ▶ 0b0: 16 sampling frequency division ▶ 0b1: 8 sampling frequency division ● Mode2: ▶ 0b0: 32 sampling frequency division ▶ 0b1: 16 sampling frequency division	RW
8	TXEIE	TX empty interupt enable ● 0b0: Disable ● 0b1: Enable	RW
7:6	SM	Working mode ● 0b00: Mode0 ● 0b01: Mode1 ● 0b10: Mode2 ● 0b11: Mode3	RW
5	ADRDET	Multi-machine communication address automatic recognition enable ● 0b0: Disable ● 0b1: Enable	RW

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Bit	Name	Functional Description	Access
4	REN	Receive enable ● Mode0: ▶ 0b0: Transmit ▶ 0b1: Receive ● Mode1/2/3: ▶ 0b0: Transmit ▶ 0b1: Receive/Transmit	RW
3:2	B8CONT	Bit8 data control bit ● 0b00: Determined by software reading/writing SBUF.DATA8 ● 0b01: Hardware even parity check ● 0b10: Hardware odd parity check ● 0b11: Setting prohibited	RW
1	TCIE	Transmit interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
0	RCIE	Receive interrupt enable ● 0b0: Disable ● 0b1: Enable	RW

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22.4.4 Address Register (UART_SADDR)

Offset	Bit Position																													
0x08	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								SADDR							
Access																									RW							

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7:0	SADDR	Slave device address register	RW

22.4.5 Address Mask Register (UART_SADEN)

Offset	Bit Position																													
0x0C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								SADEN							
Access																									RW							

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7:0	SADEN	Slave device address mask register	RW

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22.4.6 Interrupt Flag Register (UART_ISR)

Offset	Bit Position																													
0x10	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000008																															
Name	Reserved																									CTS	CTSIF	PE	TXE	FE	TC	RC
Access																										RO	RO	RO	RO	RO	RO	RO

Bit	Name	Functional Description	Access
31:7	*Reserved*	-	-
6	CTS	CTS signal flag Can only be cleared through hardware ● 0b0: The CTS signal is low level ● 0b1: The CTS signal is high level	RO
5	CTSIF	CTS interrupt flag ● 0b0: CTS signal does not toggle ● 0b1: CTS signal toggled	RO
4	PE	Parity check error flag ● 0b0: No parity errors occurred ● 0b1: A parity error occurred	RO
3	TXE	Tx Buffer empty flag Can only be cleared through hardware ● 0b0: Tx Buffer is not empty ● 0b1: Tx Buffer is empty	RO
2	FE	Frame error flag ● 0b0: No frame error occurred ● 0b1: A frame error occurred	RO
1	TC	Transmission complete interrupt flag ● 0b0: Transmission not completed ● 0b1: Transmission completed	RO
0	RC	Reception complete interrupt flag ● 0b0: Reception not completed ● 0b1: Reception completed	RO

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22.4.7 Interrupt Flag Clear Register (UART_ICR)

Offset	Bit Position																													
0x14	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000037																															
Name	Reserved																										CTSIFCF	PECF	Reserved	FECF	TCCF	RCCF
Access																											WO	WO		WO	WO	WO

Bit	Name	Functional Description	Access
31:6	*Reserved*	-	-
5	CTSIFCF	CTS interrupt flag clears Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
4	PECF	Parity check error flag clears Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
3	*Reserved*	-	-
2	FECF	Frame error flag clears Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
1	TCCF	Transmission complete interrupt flag clears Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
0	RCCF	Reception complete interrupt flag clears Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO

22.4.8 Baud Rate Register (UART_SCNT)

Offset	Bit Position																													
0x18	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																SCNT															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	SCNT	Baud rate counter	RW

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23 LPUART

23.1 Introduction

The Low Power Universal Asynchronous Receiver/Transmitter (LPUART) is a UART that allows full-duplex communication in the low power mode of MCU. When the MCU is in DeepSleep mode, LPUART can also receive UART data frames normally and wake up the MCU through the reception completion interrupt.

23.2 Features

- Configuration clock PCLK
- Transmission clock SCLK (SCLK can select XTL, RCL and PCLK)
- Support synchronous half-duplex, asynchronous full-duplex and single-wire half-duplex transmission.
- Programmable serial communication function
  - 2 character lengths: 8 bits, 9 bits
  - 3 check methods: no check, odd check, even check
  - 3 stop lengths: 1 bit, 1.5 bits, 2 bits
- Supports transmitting and receiving data in low power mode
- 16-bit baud rate counter
- Support hardware flow control (RTS, CTS)
- Support multi-machine communication and automatic address recognition
- Support data transfer via DMA

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23.3 Functional Description

23.3.1 Function Block Diagram

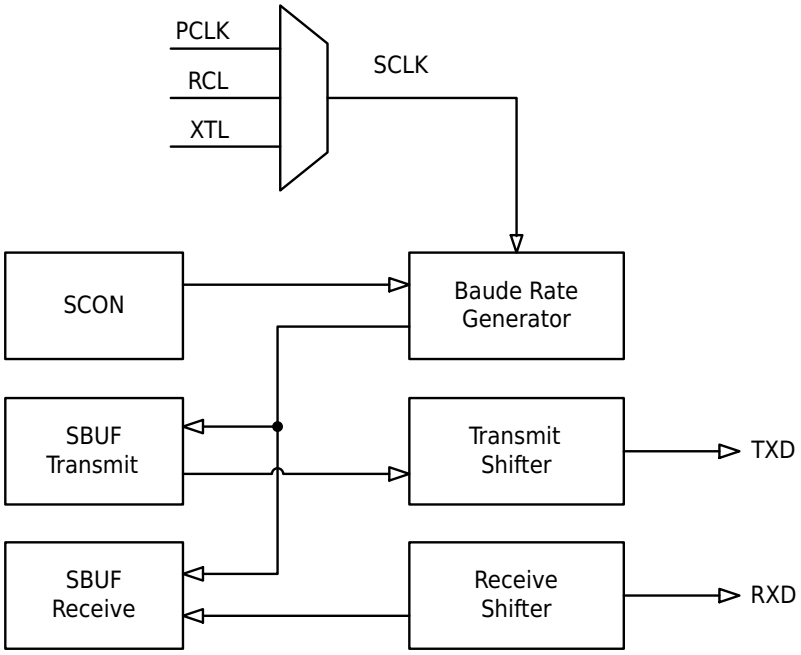

Figure 23-1 LPUART Function Block Diagram

23.3.2 Clock Description

The LPUART module has two clocks:

- Configuration Clock PCLK

  The configuration clock is used for register configuration of the LPUART module by the system APB bus, and the configuration clock is fixed as the APB bus clock PCLK. When the system enters DeepSleep mode, the PCLK clock will stop.

- Transmission Clock SCLK

  The transmission clock is used for LPUART data transceiver logic work, and the clock source can be selected from the external low-speed crystal oscillator clock (XTL), the internal low-speed clock (RCL), and the PCLK clock.

  When the system enters DeepSleep mode, if SCLK selects XTL or RCL, the LPUART can still perform normal data transmission and reception without being affected by the system's DeepSleep mode.

23.3.3 Working Mode

LPUART supports multiple working modes: synchronous half-duplex mode, asynchronous full-duplex mode, and single-wire half-duplex mode.

By combining LPUART_SCON.SM with LPUART_SCON.HDSEL, various required working modes can be configured.

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23.3.3.1 Mode0-Mode3 Function Comparison

Configure LPUART_SCON.SM to select different transmission modes: Mode0-Mode3. The main function comparison of these four working modes is shown in the table below:

Table 23-1 LPUART Mode0/1/2/3 Data Structure

Working Mode		Transmission Bit Width	Data Composition	Baud Rate
Mode0	Synchronous half-duplex mode	8-bit	Data (8bits)	$BaudRate = \frac{f_{SCLK}}{12}$
Mode1	Asynchronous full-duplex mode	10-11-bit	Start (1bit) + Data (8bits) + Stop (1-2bits)	$BaudRate = \frac{f_{SCLK}}{OVER \times SCNT}$
Mode2	Asynchronous full-duplex mode	11-12-bit	Start (1bit) + Data (8bits) + B8 (1bit) + Stop (1-2bits)	$BaudRate = \frac{f_{SCLK}}{OVER}$
Mode3	Asynchronous full-duplex mode	11-12-bit	Start (1bit) + Data (8bits) + B8 (1bit) + Stop (1-2bits)	$BaudRate = \frac{f_{SCLK}}{OVER \times SCNT}$

- When SCLK is selected as XTL (with the frequency of 32.768 kHz), Mode 1/2/3 can support baud rates of 9600/4800. The generation of the baud rate is detailed in the registers LPUART_BSEL/ LPUART_MODU.
- Mode0 can only be used as a master to transmit LPUART synchronous shift clock, and cannot be used as a slave to receive LPUART synchronous shift clock input from the outside.
- f_{SCLK} is the clock frequency of SCLK.
- OVER value:
  - When LPUART_SCON.OVER=0b00, the value of OVER in Mode1/3 mode is 16; and the value of OVER in Mode2 mode is 32.
  - When LPUART_SCON.OVER=0b01, the value of OVER in Mode1/3 mode is 8; and the value of OVER in Mode2 mode is 16.
  - When LPUART_SCON.OVER=0b10, the value of OVER in Mode1/3 mode is 4; and the value of OVER in Mode2 mode is 8.
- The definition of SCNT is detailed in register LPUART_SCNT introduction.
- B8 data bit is special and has different meanings in different applications, please refer to the following table:

Table 23-2 B8 Data Meaning

Application Scenario	LPUART_SCON.ADRDET	LPUART_SCON.B8CONT[1:0]	B8 Data Meaning
Parity check	-	0b01/0b10	When receiving, B8 is the parity check bit of the 8bits of data received. When transmitting, B8 is the parity check bit of the 8bits of data transmitted.
Multi-machine communication	0b1	-	B8=1, it means that it is currently an address frame. B8=0, it means that it is currently a data frame.

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Application Scenario	LPUART_SCON.ADRDET	LPUART_SCON.B8CONT[1:0]	B8 Data Meaning
Other	0b0	0b00/0b11	Bit8 receiving/transmitting data.

When the multi-machine communication mode is turned on, the parity check of the received data is automatically closed; the parity check of the transmitted data is still controlled by B8CONT.

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23.3.3.2 Mode0 Data Transmitting and Reception

- Mode0 Data Transmitting

  When LPUART_SCON.REN set to 0, the LPUART operates in the transmission mode. The data to be transmitted is written into the LPUART_SBUF register, and then the data will be output from the RXD (lower bits first and higher bits later), while the synchronous shift clock is output from the TXD.

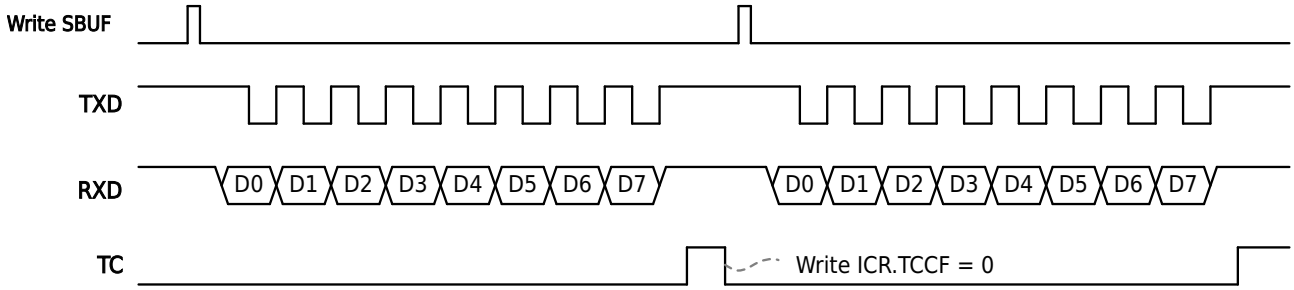

Figure 23-2 Mode0 Data Transmitting

- Mode0 Data Receiving

  When LPUART_SCON.REN is set to 1, the LPUART is in the receiving state. When the LPUART_ISR.RC flag is 0, the TXD pin will output 8 synchronous shift clocks, and data will be input from RXD (lower bits first and higher bits later), each time the LPUART_ISR.RC flag is cleared, the next byte can be received.

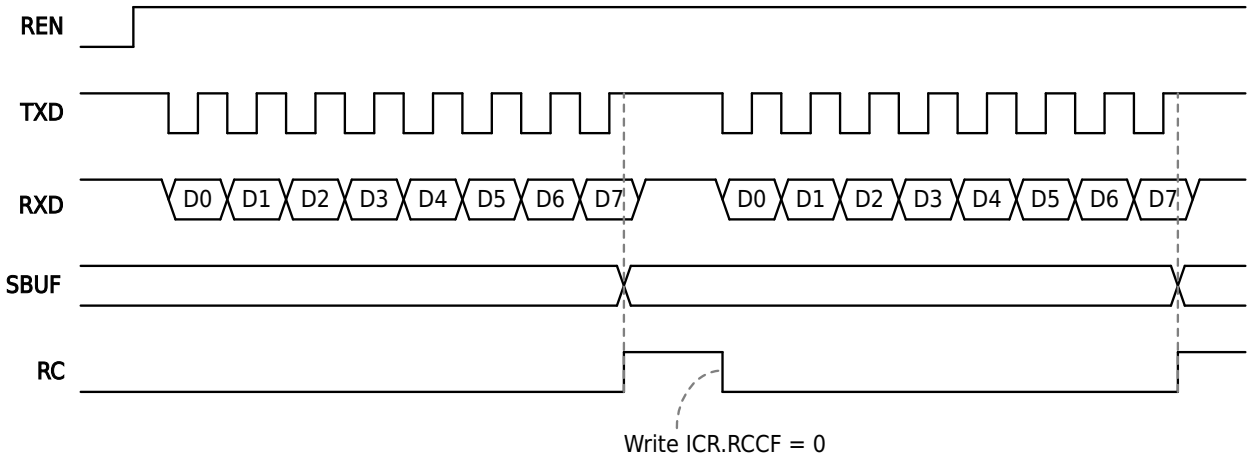

Figure 23-3 Mode0 Data Receiving

23.3.3.3 Mode1 Data Transmitting and Reception

- Mode1 Data Transmitting

  Whether LPUART_SCON.REN is 0 or 1, data can be transmitted normally.

  Write data to LPUART_SBUF, the hardware automatically loads the data into the transmit shift register and shifts the output from the TXD pin (lower bits first and higher bits later), and the LPUART_ISR.TXE flag is set to 1 by the hardware.

  When the user queries that the LPUART_ISR.TXE flag is 1, the next data to be transmitted can be written to the LPUART_SBUF register.

  Whenever the TXD pin completes transmitting a frame of data, the LPUART_ISR.TC flag will be set to 1 by hardware to indicate the current transmitting progress.

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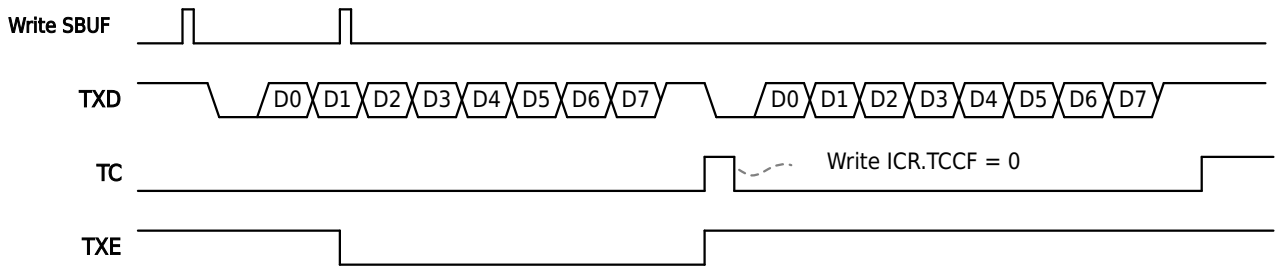

Figure 23-4 Mode1 Data Transmitting

- Mode1 Data Receiving

  When receiving data, set LPUART_SCON.REN to 1, and clear the LPUART_ISR.RC bit to 0.

  When a frame of data reception is completed, LPUART_ISR.RC flag will be set to 1 by hardware, and the received data can be read from LPUART_SBUF register.

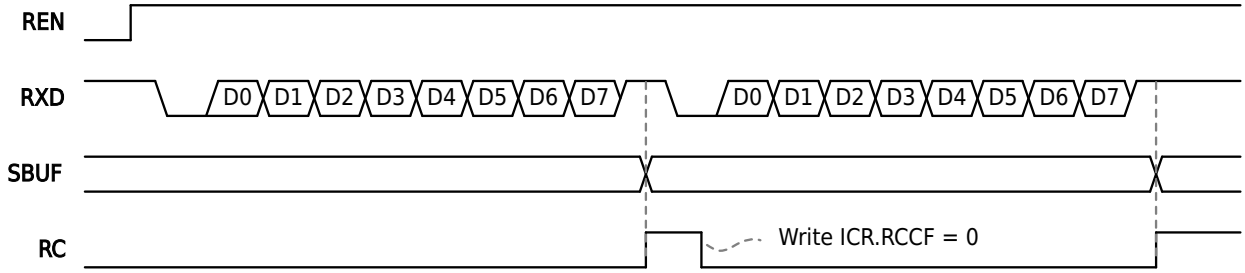

Figure 23-5 Mode1 Data Receiving

23.3.3.4 Mode2/Mode3 Data Transmitting and Reception

- Mode2/3 Data Transmitting

  Whether LPUART_SCON.REN is 0 or 1, data can be transmitted normally.

  Write data to LPUART_SBUF, the hardware automatically loads the data into the transmit shift register and shifts the output from the TXD pin (lower bits first and higher bits later), and the LPUART_ISR.TXE flag is set to 1 by the hardware.

  When the user queries that the LPUART_ISR.TXE flag is 1, the next data to be transmitted can be written to the LPUART_SBUF register.

  Whenever the TXD pin completes transmitting a frame of data, the LPUART_ISR.TC flag will be set to 1 by hardware to indicate the current transmitting progress.

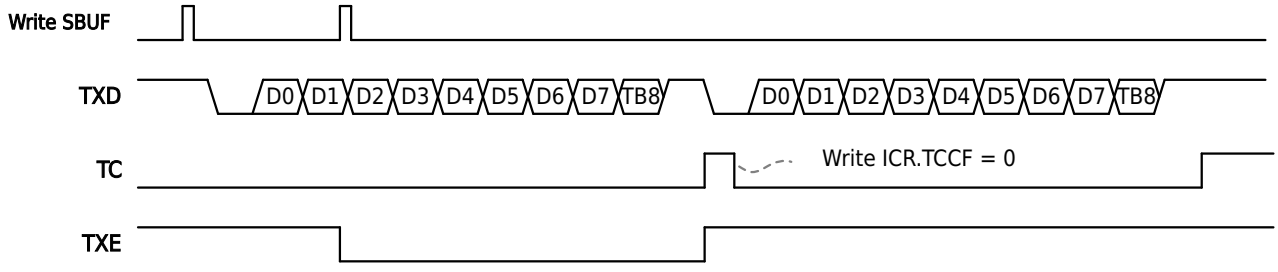

Figure 23-6 Mode2/Mode3 Data Transmitting

- Mode2/3 Data Receiving

  When receiving data, set LPUART_SCON.REN to 1, and clear the LPUART_ISR.RC bit to 0.

  When a frame of data reception is completed, LPUART_ISR.RC flag will be set to 1 by hardware, and the received data can be read from LPUART_SBUF rigester.

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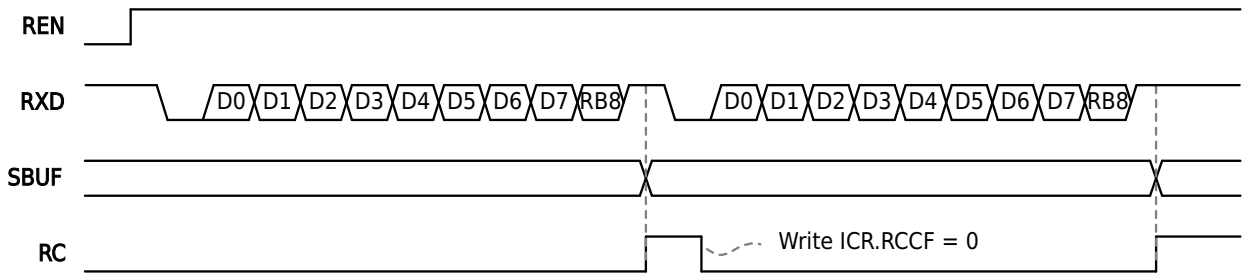

Figure 23-7 Mode2/Mode3 Data Receiving

23.3.3.5 Single-Wire Half-Duplex Data Transmitting and Reception

When LPUART_SCON.HDSEL=0b1, it can enter the single-wire half-duplex transmission mode:

- The TX and RX signal lines are connected inside the module.
- The RX signal is no longer used, and the received and transmitted data are all completed through the TX signal. TX signal is done by hardware logic without software control.
- After configuring LPUART_SCON.HDSEL to 0b1, must wait for the transmission duration of one data bit (i.e., after 1/BaudRate seconds) before normal reception can occur.
- When the transmit buffer is empty, the TX signal is always input (receive state). Once a data is filled into the transmit buffer, the TX signal becomes output (transmit state). When the transmission is complete, the transmit buffer becomes empty and the TX signal returns to input (receive state).
- When there is no data transmission, the TXD pin is always in the input state. The user program needs to configure this pin as an open-drain output and connect an external pull-up resistor.

Notice

1. Even if the module is in the process of receiving, as long as the transmit buffer is filled with data, the TX signal will immediately become output (transmit state). The receiving process will be interrupted and a wrong received data will be obtained.
2. Similarities and differences between single-wire half-duplex mode and Mode0 mode:
   - The same: both use a signal to time-division multiplex to complete data transmission and reception.
   - Different: Mode0 is synchronous transmission, with synchronous clock. The single-wire half-duplex mode is asynchronous transmission, and all baud rate calculations still follow the baud rate formula of Mode1-Mode3, only the transceiver function is multiplexed on the TX signal.

Single-wire half-duplex transmission supports baud rates of 9600/4800. However, it is important to note that when receiving data in single-wire half-duplex mode at baud rates of 9600/4800, the following steps must be followed:

Step1. Refer to the relevant descriptions of pin digital multiplexing functions in the "General-Purpose I/O (GPIO)" chapter to map TXD to the required pin; configure TXD as an open-drain output and enable the pull-up resistor.

Step2. Configure SYSCTRL module register PERI_CLKEN0.LPUARTx to 1 to enable LPUART configuration clock and working clock.

Step3. Configure LPUART_SCON.SCLKSEL to select the transmission clock source for LPUART.

Step4. Set LPUART_SCON.HDSEL to 0b1 to enable single-wire mode.

Step5. Add a delay of at least 500 μs and initialize TXD to the receiving state.

Step6. Configure the LPUART_BSEL and LPUART_MODU registers to enable 9600/4800 baud rate modulation.

Step7. For subsequent steps, refer to the "Receive Data Example" chapter.

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For other scenarios, such as transmitting data in single-wire half-duplex mode at baud rates of 9600/4800, or modulating the baud rate by configuring the LPUART_SCNT register, simply follow the steps outlined in the "Transmit Data Example" or "Receive Data Example" chapters for normal configuration.

23.3.4 Baud Rate Generation

The formula for generating the baud rate in Mode0-Mode3 is as follows:

- Mode0 baud rate generation formula: $\text{BaudRate} = \frac{f_{SCLK}}{12}$
- Mode1 baud rate generation formula: $\text{BaudRate} = \frac{f_{SCLK}}{\text{OVER} \times \text{SCNT}}$
- Mode2 baud rate generation formula: $\text{BaudRate} = \frac{f_{SCLK}}{\text{OVER}}$
- Mode3 baud rate generation formula: $\text{BaudRate} = \frac{f_{SCLK}}{\text{OVER} \times \text{SCNT}}$

Note

- f_{SCLK} is the clock frequency of SCLK.
- OVER value:
  - When LPUART_SCON.OVER = 0b00, the value of OVER in Mode1/3 mode is 16; and the value of OVER in Mode2 mode is 32.
  - When LPUART_SCON.OVER = 0b01, the value of OVER in Mode1/3 mode is 8; and the value of OVER in Mode2 mode is 16.
  - When LPUART_SCON.OVER = 0b10, the value of OVER in Mode1/3 mode is 4; and the value of OVER in Mode2 mode is 8.
- The definition of SCNT is detailed in register LPUART_SCNT introduction.

Mode1/Mode3 Baud Rate Setting Example

Table 23-3 SCLK = 4MHz Baud Rate Calculation Table

Baud Rate	SCLK=4MHz								
	OVER=4			OVER=8			OVER=16		
	SCNT	Actual Baud Rate	Error%	SCNT	Actual Baud Rate	Error%	SCNT	Actual Baud Rate	Error%
2400	417	2398.08	-0.08%	208	2403.85	0.16%	104	2403.85	0.16%
4800	208	4807.69	0.16%	104	4807.69	0.16%	52	4807.69	0.16%
9600	104	9615.38	0.16%	52	9615.38	0.16%	26	9615.38	0.16%
19200	52	19230.77	0.16%	26	19230.77	0.16%	13	19230.77	0.16%
38400	26	38461.54	0.16%	13	38461.54	0.16%	7	35714.29	-6.99%
57600	17	58823.53	2.12%	9	55555.56	-3.55%	4	62500.00	8.51%
76800	13	76923.08	0.16%	7	71428.57	-6.99%	3	83333.33	8.51%
115200	9	111111.11	-3.55%	4	125000.00	8.51%	2	125000.00	8.51%
128000	8	125000.00	-2.34%	4	125000.00	-2.34%	2	125000.00	-2.34%
256000	4	250000.00	-2.34%	2	250000.00	-2.34%	1	250000.00	-2.34%
1000000	1	1000000.00	0.00%	1	/	/	0	/	/

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Table 23-4 SCLK = 8MHz Baud Rate Calculation Table

Baud Rate	SCLK=8MHz								
	OVER=4			OVER=8			OVER=16		
	SCNT	Actual Baud Rate	Error%	SCNT	Actual Baud Rate	Error%	SCNT	Actual Baud Rate	Error%
2400	833	2400.96	0.04%	417	2398.08	-0.08%	208	2403.85	0.16%
4800	417	4796.16	-0.08%	208	4807.69	0.16%	104	4807.69	0.16%
9600	208	9615.38	0.16%	104	9615.38	0.16%	52	9615.38	0.16%
19200	104	19230.77	0.16%	52	19230.77	0.16%	26	19230.77	0.16%
38400	52	38461.54	0.16%	26	38461.54	0.16%	13	38461.54	0.16%
57600	35	57142.86	-0.79%	17	58823.53	2.12%	9	55555.56	-3.55%
76800	26	76923.08	0.16%	13	76923.08	0.16%	7	71428.57	-6.99%
115200	17	117647.06	2.12%	9	111111.11	-3.55%	4	125000.00	8.51%
128000	16	125000.00	-2.34%	8	125000.00	-2.34%	4	125000.00	-2.34%
256000	8	250000.00	-2.34%	4	250000.00	-2.34%	2	250000.00	-2.34%
1000000	2	1000000.00	0.00%	1	1000000.00	0.00%	1	/	/
2000000	1	2000000.00	0.00%	1	/	/	0	/	/

Table 23-5 SCLK = 16MHz Baud Rate Calculation Table

Baud Rate	SCLK=16MHz								
	OVER=4			OVER=8			OVER=16		
	SCNT	Actual Baud Rate	Error%	SCNT	Actual Baud Rate	Error%	SCNT	Actual Baud Rate	Error%
2400	1667	2399.52	-0.02%	833	2400.96	0.04%	417	2398.08	-0.08%
4800	833	4801.92	0.04%	417	4796.16	-0.08%	208	4807.69	0.16%
9600	417	9592.33	-0.08%	208	9615.38	0.16%	104	9615.38	0.16%
19200	208	19230.77	0.16%	104	19230.77	0.16%	52	19230.77	0.16%
38400	104	38461.54	0.16%	52	38461.54	0.16%	26	38461.54	0.16%
57600	69	57971.01	0.64%	35	57142.86	-0.79%	17	58823.53	2.12%
76800	52	76923.08	0.16%	26	76923.08	0.16%	13	76923.08	0.16%
115200	35	114285.71	-0.79%	17	117647.06	2.12%	9	111111.11	-3.55%
128000	31	129032.26	0.81%	16	125000.00	-2.34%	8	125000.00	-2.34%
256000	16	250000.00	-2.34%	8	250000.00	-2.34%	4	250000.00	-2.34%
1000000	4	1000000.00	0.00%	2	1000000.00	0.00%	1	1000000.00	0.00%
2000000	2	2000000.00	0.00%	1	2000000.00	0.00%	1	/	/
4000000	1	4000000.00	0.00%	1	/	/	0	/	/

Table 23-6 SCLK = 24MHz Baud Rate Calculation Table

Baud Rate	SCLK=24MHz								
	OVER=4			OVER=8			OVER=16		
	SCNT	Actual Baud Rate	Error%	SCNT	Actual Baud Rate	Error%	SCNT	Actual Baud Rate	Error%
2400	2500	2400.00	0.00%	1250	2400.00	0.00%	625	2400.00	0.00%
4800	1250	4800.00	0.00%	625	4800.00	0.00%	313	4792.33	-0.16%
9600	625	9600.00	0.00%	313	9584.66	-0.16%	156	9615.38	0.16%
19200	313	19169.33	-0.16%	156	19230.77	0.16%	78	19230.77	0.16%
38400	156	38461.54	0.16%	78	38461.54	0.16%	39	38461.54	0.16%
57600	104	57692.31	0.16%	52	57692.31	0.16%	26	57692.31	0.16%

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Baud Rate	SCLK=24MHz								
	OVER=4			OVER=8			OVER=16		
	SCNT	Actual Baud Rate	Error%	SCNT	Actual Baud Rate	Error%	SCNT	Actual Baud Rate	Error%
76800	78	76923.08	0.16%	39	76923.08	0.16%	20	75000.00	-2.34%
115200	52	115384.62	0.16%	26	115384.62	0.16%	13	115384.62	0.16%
128000	47	127659.57	-0.27%	23	130434.78	1.90%	12	125000.00	-2.34%
256000	23	260869.57	1.90%	12	250000.00	-2.34%	6	250000.00	-2.34%
1000000	6	1000000.00	0.00%	3	1000000.00	0.00%	2	/	/
2000000	3	2000000.00	0.00%	2	/	/	1	/	/
6000000	1	6000000.00	0.00%	1	/	/	0	/	/

Table 23-7 SCLK = 32MHz Baud Rate Calculation Table

Baud Rate	SCLK=32MHz								
	OVER=4			OVER=8			OVER=16		
	SCNT	Actual Baud Rate	Error%	SCNT	Actual Baud Rate	Error%	SCNT	Actual Baud Rate	Error%
2400	3333	2400.24	0.01%	1667	2399.52	-0.02%	833	2400.96	0.04%
4800	1667	4799.04	-0.02%	833	4801.92	0.04%	417	4796.16	-0.08%
9600	833	9603.84	0.04%	417	9592.33	-0.08%	208	9615.38	0.16%
19200	417	19184.65	-0.08%	208	19230.77	0.16%	104	19230.77	0.16%
38400	208	38461.54	0.16%	104	38461.54	0.16%	52	38461.54	0.16%
57600	139	57553.96	-0.08%	69	57971.01	0.64%	35	57142.86	-0.79%
76800	104	76923.08	0.16%	52	76923.08	0.16%	26	76923.08	0.16%
115200	69	115942.03	0.64%	35	114285.71	-0.79%	17	117647.06	2.12%
128000	63	126984.13	-0.79%	31	129032.26	0.81%	16	125000.00	-2.34%
256000	31	258064.52	0.81%	16	250000.00	-2.34%	8	250000.00	-2.34%
1000000	8	1000000.00	0.00%	4	1000000.00	0.00%	2	1000000.00	0.00%
2000000	4	2000000.00	0.00%	2	2000000.00	0.00%	1	2000000.00	0.00%
4000000	2	4000000.00	0.00%	1	4000000.00	0.00%	1	/	/
8000000	1	8000000.00	0.00%	1	/	/	0	/	/

Table 23-8 SCLK = 48MHz Baud Rate Calculation Table

Baud Rate	SCLK=48MHz								
	OVER=4			OVER=8			OVER=16		
	SCNT	Actual Baud Rate	Error%	SCNT	Actual Baud Rate	Error%	SCNT	Actual Baud Rate	Error%
2400	5000	2400.00	0.00%	2500	2400.00	0.00%	1250	2400.00	0.00%
4800	2500	4800.00	0.00%	1250	4800.00	0.00%	625	4800.00	0.00%
9600	1250	9600.00	0.00%	625	9600.00	0.00%	313	9584.66	-0.16%
19200	625	19200.00	0.00%	313	19169.33	-0.16%	156	19230.77	0.16%
38400	313	38338.66	-0.16%	156	38461.54	0.16%	78	38461.54	0.16%
57600	208	57692.31	0.16%	104	57692.31	0.16%	52	57692.31	0.16%
76800	156	76923.08	0.16%	78	76923.08	0.16%	39	76923.08	0.16%
115200	104	115384.62	0.16%	52	115384.62	0.16%	26	115384.62	0.16%
128000	94	127659.57	-0.27%	47	127659.57	-0.27%	23	130434.78	1.90%
256000	47	255319.15	-0.27%	23	260869.57	1.90%	12	250000.00	-2.34%
1000000	12	1000000.00	0.00%	6	1000000.00	0.00%	3	1000000.00	0.00%

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Baud Rate	SCLK=48MHz								
	OVER=4			OVER=8			OVER=16		
	SCNT	Actual Baud Rate	Error%	SCNT	Actual Baud Rate	Error%	SCNT	Actual Baud Rate	Error%
2000000	6	2000000.00	0.00%	3	2000000.00	0.00%	2	1500000.00	-25.00%
4000000	4	3000000.00	0.00%	2	3000000.00	0.00%	1	3000000.00	0.00%
6000000	3	4000000.00	0.00%	2	/	/	1	/	/
12000000	1	12000000.00	0.00%	1	/	/	0	/	/

23.3.5 Frame Error Detection

When LPUART works in Mode1/2/3, it has frame error detection function:

- When receiving data, if the stop bit is not recognized within the expected time, it is a frame error.
- When a frame error is detected, LPUART_ISR.FE will be set to 1 by hardware, and the user program should clear this flag in time.

23.3.6 Multi-Machine Communication

When working in Mode2/3, set the LPUART_SCON.ADRDET to 1 to enable the multi-machine communication address automatic identification function. The master can transmit address frames and data frames, and the slave can receive data frames only after receiving matching address frames.

Master Transmitting Address and Data Frame

When LPUART_SBUF.DATA8 is 1, the address frame is transmitted, LPUART_SBUF.DATA is the address of the target slave.

When LPUART_SBUF.DATA8 is 0, the data frame is transmitted, LPUART_SBUF.DATA is the data to be transmitted.

Slave Receiving Address and Data Frame

When LPUART_SCON.ADRDET is 1, the slave only receives address frames that match its own address, ignoring data frames and unmatched address frames. When the slave receives the address frame from RXD, the hardware automatically compares the address in the address frame with the local address. Only when the two match, the received address is stored in the LPUART_SBUF register and LPUART_ISR.RC is set.

When LPUART_SCON.ADRDET is 0, the slave only receives data frames and ignores address frames. The user program should set LPUART_SCON.ADRDET to 0 after the address matches to receive subsequent data frames transmitted by the master.

Slave Address Configuration

The slave address consists of the broadcast address and the user configuration address:

- Broadcast Address: LPUART_SADDR | LPUART_SADEN
- User Configuration Address: LPUART_SADDR & LPUART_SADEN

When an address frame is received, if the address received from the bus, after being ANDed with the value of LPUART_SADEN, matches the user-configured address, or if the received address, after being ANDed with the broadcast address, matches the broadcast address, it is considered that an address frame matching the slave address has been received.

Example: LPUART_SADDR=0x55, LPUART_SADEN=0xF0, then the slave can match addresses 0xF5, 0xF7, 0xFD, 0xFF (broadcast address) and 0x50~0x5F (user-configured address).

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23.3.7 Hardware Flow Control

The hardware flow control function can be realized by adding CTS and RTS signals, the LPUART module will automatically control the transmitting and receiving of data based on the high and low levels of CTS and RTS without the need for software judgment.

The hardware flow control diagram between two LPUART modules is as follows:

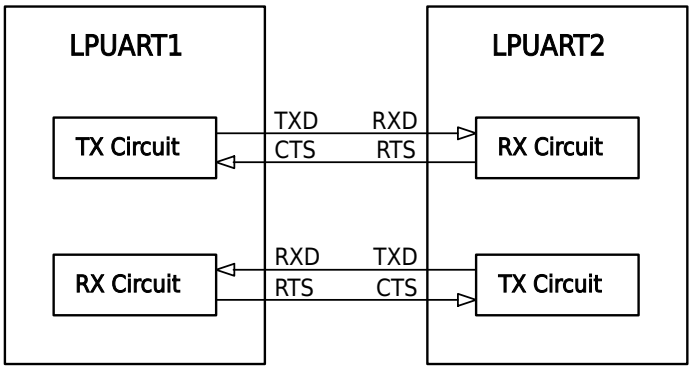

Figure 23-8 LPUART Hardware Flow Control

RTS Flow Control

When RTS flow control is enabled (LPUART_SCON.RTSEN is 1), the RTS pin indicates the receiving status of this module:

- When the receive buffer is empty, the RTS pin turns low level to notify the transmitting end to send the next frame of data.
- When the receive buffer is full, the RTS pin turns to high level, notifying the transmitting end to pause sending the next frame of data.

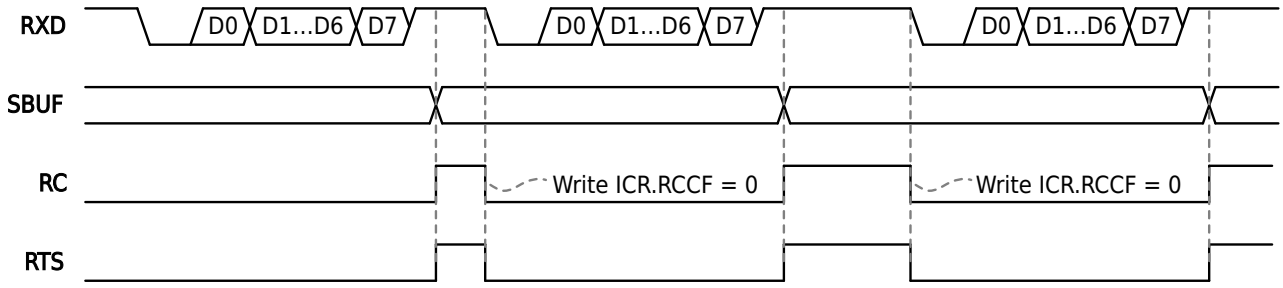

Figure 23-9 RTS Hardware Flow Control Signal

CTS Flow Control

When CTS flow control is enabled (LPUART_SCON.CTSEN is set to 1), the CTS pin instructs this module to transmit the next frame of data:

- If CTS is low level, LPUART transmits the next frame of data.
- If CTS is high level, after LPUART finishes transmitting the current frame, it waits for CTS to become low level before sending the next frame.

When the CTS level changes, LPUART_ISR.CTSIF is automatically set to 1. Read LPUART_ISR.CTS to obtain the current CTS pins level value.

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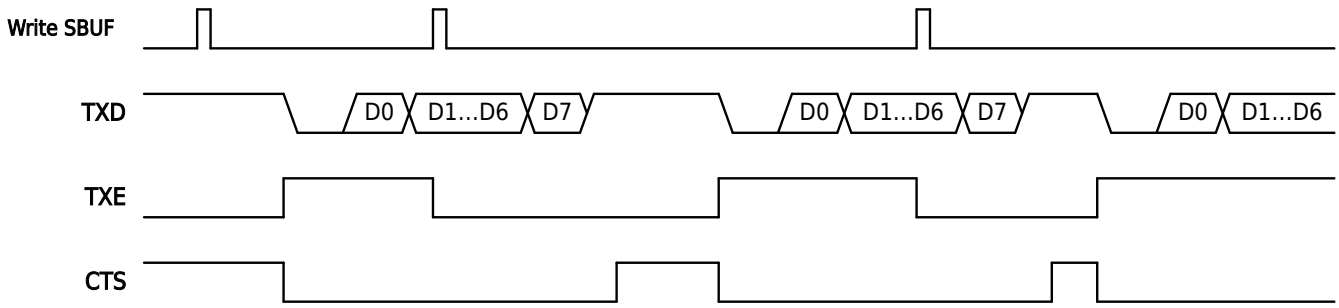

Figure 23-10 CTS Hardware Flow Control Signal

23.3.8 DMA Transmission

The LPUART module supports the DMA handshake protocol and can transmit data through DMA.

- When LPUART_SCON.DMATXEN is set to 1, DMA can be used to control the LPUART to transmit data externally.

  Whenever LPUART_ISR.TXE is 1, DMA will write a frame of data to be transmit to LPUART_SBUF until all data configured in DMA is transferred. When starting to use this function, please first configure the various registers of DMA and enable DMA, and then configure the various registers of LPUART. When you want to end this function, please first disable LPUART_SCON.DMATXEN, and then disable DMA (if the disabling of DMA uses the DMA hardware self-clearing, then as soon as it is detected that the enable of DMA has been cleared by hardware, immediately disable LPUART_SCON.DMATXEN).
- When setting, LPUART_SCON.DMARXEN to 1, DMA can be used to read and save the data received by LPUART.

  Whenever LPUART_ISR.RC is 1, DMA will read out one frame of received data from LPUART_SBUF, until all data configured in DMA is transferred.

23.3.9 Receive/Transmit Buffer

Receive Buffer

The receive end of the LPUART module has a frame (8bits/9bits) receive buffer, which retains the received data frame until the Stop bit of the next data frame is received before updating the current data frame.

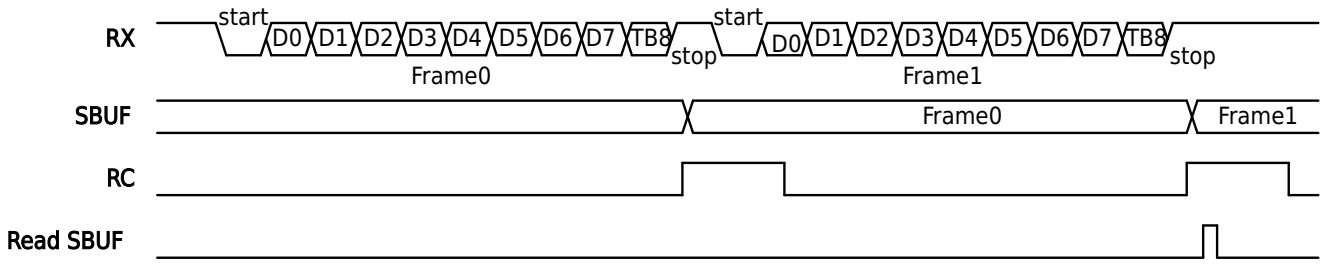

Figure 23-11 Receive Buffer

Transmit Buffer

The transmit end of LPUART module has a frame (8bits/9bits) transmit buffer. When the LPUART is transmitting the current frame, the software for the next transmitting data will be written into LPUART_SBUF.

- When LPUART_ISR.TXE = 0, it indicates that the current transmit buffer is full, LPUART_SBUF cannot write the next transmit data.

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- When LPUART_ISR.TXE = 1, it indicates that the current transmit buffer is empty, LPUART_SBUF can write the next transmit data. After the current data transmission is completed, the hardware automatically loads the data in the transmit buffer into the shift register and sends it out.

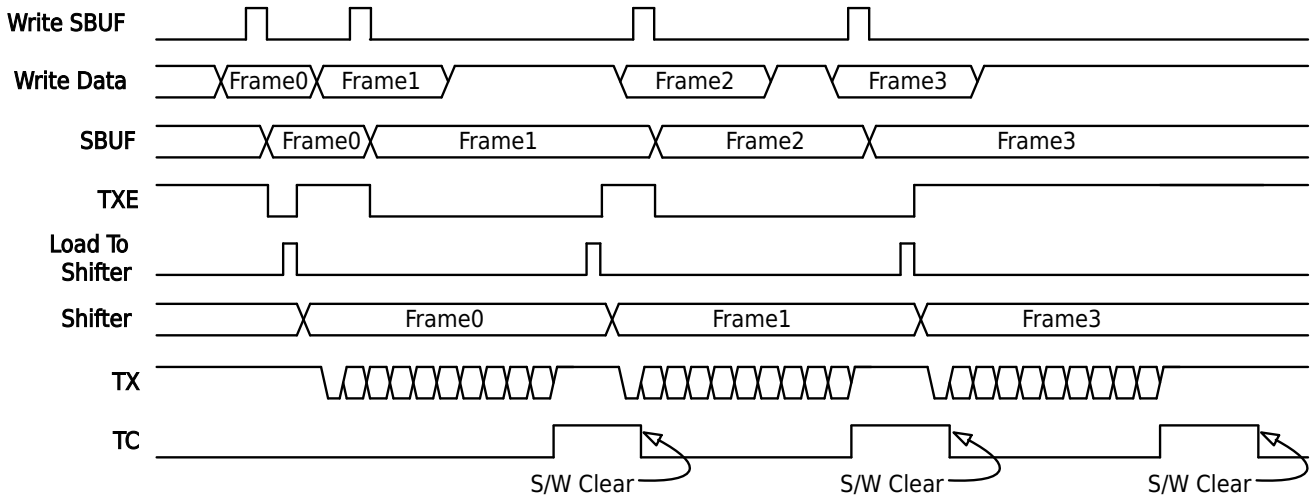

Figure 23-12 Transmit Buffer

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23.4 Operation Example

23.4.1 Transmit Data Example

Procedure

Step1. Refer to the relevant description of the port digital multiplexing function in the "General-Purpose I/O (GPIO)" chapter, map TXD to the required pin; and configure TXD to CMOS output.

Step2. Configure SYSCTRL module register PERI_CLKEN0.LPUARTx to 1 to enable LPUART configuration clock and working clock.

Step3. Configure LPUART_SCON.SCLKSEL to select the transmission clock source for LPUART.

Step4. Configure LPUART_SCON.SM to select the working mode of LPUART.

Step5. Configure LPUART_SCON.OVER and LPUART_SCNT register to configure the communication baud rate.

Step6. Configure LPUART_SCON.STOPBIT, LPUART_SCON.B8CONT, to configure the STOP length and parity mode of LPUART.

Step7. Write 0x00 to the ICR register to clear all status flags.

Step8. When the value of ISR.TXE is is queried for 1, write a frame of data to be transmitted to the LPUART_SBUF register.

Step9. The query waits for ISR.TC to become 1 and the data frame written this time is sent.

Step10. Write 0x00 to ICR.TCCF to clear the transmitting completion flag.

Step11. If the data to be transmitted is not completed, then jump to step8.

23.4.2 Receive Data Example

Procedure

Step1. Refer to the relevant description of the port digital multiplexing function in the "General-Purpose I/O (GPIO)" chapter. Map the RXD to the required pin; and configure RXD as an input and enable the pull-up resistor.

Step2. Configure SYSCTRL module register PERI_CLKEN0.LPUARTx to 1 to enable LPUART configuration clock and working clock.

Step3. Configure LPUART_SCON.SCLKSEL to select the transmission clock source for LPUART.

Step4. Configure LPUART_SCON.SM to select the working mode of LPUART.

Step5. Configure LPUART_SCON.OVER and LPUART_SCNT register to configure the communication baud rate.

Step6. Configure LPUART_SCON.STOPBIT, LPUART_SCON.B8CONT, to configure the STOP length and parity mode of LPUART.

Step7. Write 0x00 to the ICR register to clear all status flags.

Step8. Set LPUART_SCON.REN to 1 to enable RXD data reception.

Step9. The query waits for ISR.RC to become 1, and one frame of data is received.

Step10. Query the ISR.PE and ISR.FE to confirm whether the received data frame is valid. If it is invalid, perform error handling, if it is valid, read the data from the LPUART_SBUF register and save it .

Step11. Write 0x00 to ICR.RCCF to clear the reception completion flag.

Step12. If the data to be received is not completed, jump to step9.

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23.5 Register Description

23.5.1 Register List

- LPUART0 base address: 0x40000200
- LPUART1 base address: 0x40004000

Table 23-9 Low Power Universal Asynchronous Receiver/Transmitter (LPUART) Register Offset

Offset	Register	Description	Width
0x00	LPUART_SBUF	Data Register	32
0x04	LPUART_SCON	Control Register	32
0x08	LPUART_SADDR	Address Register	32
0x0C	LPUART_SADEN	Address Mask Register	32
0x10	LPUART_ISR	Interrupt Flag Bit Register	32
0x14	LPUART_ICR	Interrupt Flag Bit Clear Register	32
0x18	LPUART_SCNT	Baud Rate Register	32
0x1C	LPUART_BSEL	Baud Rate Generate Register	32
0x20	LPUART_MODU	9600/4800 Baud Rate Modulator Register	32

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23.5.2 Data Register (LPUART_SBUF)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																							DATA8	DATA							
Access																								RW	RW							

Bit	Name	Functional Description	Access
31:9	*Reserved*	-	-
8	DATA8	Bit8 Data Bit ● In Mode 0/1, read this bit is 0, write this bit is invalid ● Under Mode 2/3, there are such situations: ▶ When the hardware parity bit is turned on, this bit is the parity bit of the received data when receiving, and the verification is performed by the hardware. If the verification error occurs, the verification error flag bit PE is set to 1; this bit is invalid when transmitting, the parity bit of the transmitted data is calculated and transmitted by the hardware. ▶ When the hardware parity bit is turned off, this bit is received data Bit8 when receiving; this bit is sent data Bit8 when transmitting. **Note** When the multi-machine communication mode is turned on, the parity check of the received data is automatically closed; the parity check of the transmitted data is still controlled by B8CONT.	RW
7:0	DATA	Data When transmitting data, write the data to be transmitted into this register; when receiving data, read the received data from this register.	RW

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23.5.3 Control Register (LPUART_SCON)

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved									HDSEL	FEIE	CTSIE	CTSEN	RTSEN	DMATXEN	DMARXEN	STOPBIT		PEIE	SCLKSEL		OVER	TXEIE	SM	ADRDET	REN	B8CONT		TCIE	RCIE
Access										RW	RW	RW	RW	RW	RW	RW	RW		RW	RW		RW	RW	RW	RW	RW	RW		RW	RW

Bit	Name	Functional Description	Access
31:23	*Reserved*	-	-
22	HDSEL	Single-wire half-duplex function enable ● 0b0: Disable ● 0b1: Enable	RW
21	FEIE	Frame error interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
20	CTSIE	CTS signal flip interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
19	CTSEN	CTS signal enable control ● 0b0: Disable ● 0b1: Enable	RW
18	RTSEN	RTS signal enable control ● 0b0: Disable ● 0b1: Enable	RW
17	DMATXEN	DMA transmit data enable control ● 0b0: Disable ● 0b1: Enable	RW
16	DMARXEN	DMA receive data enable control ● 0b0: Disable ● 0b1: Enable	RW
15:14	STOPBIT	STOPBIT duration configuration ● 0b00: 1-bit ● 0b01: 1.5-bit ● 0b10: 2-bit ● 0b11: Setting prohibited **Notice** In Mode 0, this bit must be set to 0b00.	RW

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Bit	Name	Functional Description	Access
13	PEIE	Parity error interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
12:11	SCLKSEL	Transmission clock SCLK source selection ● 0b00: PCLK ● 0b01: Setting prohibited ● 0b10: XTL ● 0b11: RCL	RW
10:9	OVER	Oversampling control ● Mode0: Invalid ● Mode1/3: ▶ 0b00: 16 sampling frequency division ▶ 0b01: 8 sampling frequency division ▶ 0b10: 4 sampling frequency division ▶ 0b11: Setting prohibited ● Mode2: ▶ 0b00: 32 sampling frequency division ▶ 0b01: 16 sampling frequency division ▶ 0b10: 8 sampling frequency division ▶ 0b11: Setting prohibited	RW
8	TXEIE	TX Buf empty interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
7:6	SM	Working mode ● 0b00: Mode0, synchronous half-duplex, Data (8bits) ● 0b01: Mode1, asynchronous full-duplex, Start (1bit) + Data (8bits) + Stop (1-2bits) ● 0b10: Mode2, asynchronous full-duplex, Start (1bit) + Data (8bits) + B8 (1bit) + Stop (1-2bits) ● 0b11: Mode3, asynchronous full-duplex, Start (1bit) + Data (8bits) + B8 (1bit) + Stop (1-2bits)	RW
5	ADRDET	Multi-machine address automatic recognition enable ● 0b0: Disabled ● 0b1: Enabled	RW
4	REN	Receive enable ● Mode0: ▶ 0b0: Transmit ▶ 0b1: Receivie ● Mode1/2/3: ▶ 0b0: Transmit ▶ 0b1: Receive/Transmit	RW

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Bit	Name	Functional Description	Access
3:2	B8CONT	DATA8 data bit function configuration ● 0b00: Deciding by software read/write LPUART_SBUF.DATA8 ● 0b01: Hardware even parity check ● 0b10: Hardware odd parity check ● 0b11: Setting prohibited	RW
1	TCIE	Transmit complete interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
0	RCIE	Receive complete interrupt enable ● 0b0: Disable ● 0b1: Enable	RW

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23.5.4 Address Register (LPUART_SADDR)

Offset	Bit Position																													
0x08	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								SADDR							
Access																									RW							

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7:0	SADDR	Slave device address register	RW

23.5.5 Address Mask Register (LPUART_SADEN)

Offset	Bit Position																													
0x0C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								SADEN							
Access																									RW							

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7:0	SADEN	Slave device address mask register Each bit corresponds to an address bit: ● 0b0: Does not participate in address matching ● 0b1: Participates in address matching	RW

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23.5.6 Interrupt Flag Bit Register (LPUART_ISR)

Offset	Bit Position																													
0x10	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000008																															
Name	Reserved																									CTS	CTSIF	PE	TXE	FE	TC	RC
Access																										RO	RO	RO	RO	RO	RO	RO

Bit	Name	Functional Description	Access
31:7	*Reserved*	-	-
6	CTS	CTS signal flag Can only be cleared through hardware ● 0b0: CTS signal is low level ● 0b1: CTS signal is high level	RO
5	CTSIF	CTS signal flip flag ● 0b0: CTS signal does not flip ● 0b1: CTS signal fliped	RO
4	PE	Parity check error flag ● 0b0: No parity errors occurred ● 0b1: A parity error occurred	RO
3	TXE	Tx Buffer empty flag Can only be cleared through hardware ● 0b0: Tx Buffer is not empty ● 0b1: Tx Buffer is empty	RO
2	FE	Frame error flag ● 0b0: No frame error occurred ● 0b1: A frame error occurred	RO
1	TC	Transmit completion flag ● 0b0: Transmission not completed ● 0b1: Transmission completed	RO
0	RC	Receive completion flag ● 0b0: Reception not completed ● 0b1: Reception completed	RO

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23.5.7 Interrupt Flag Bit Clear Register (LPUART_ICR)

Offset	Bit Position																													
0x14	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000037																															
Name	Reserved																										CTSIFCF	PECF	Reserved	FECF	TCCF	RCCF
Access																											WO	WO		WO	WO	WO

Bit	Name	Functional Description	Access
31:6	*Reserved*	-	-
5	CTSIFCF	ISR.CTSIF flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
4	PECF	ISR.PE flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
3	*Reserved*	-	-
2	FECF	ISR.FE flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
1	TCCF	ISR.TC flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
0	RCCF	ISR.RC flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO

23.5.8 Baud Rate Register (LPUART_SCNT)

Offset	Bit Position																													
0x18	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																SCNT															
Access																	RW															

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:0	SCNT	Baud rate counter	RW

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23.5.9 Baud Rate Generate Register (LPUART_BSEL)

Offset	Bit Position																													
0x1C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																														BSEL	
Access																															RW	

Bit	Name	Functional Description	Access
31:2	*Reserved*	-	-
1:0	BSEL	Baud rate generation way ● 0b00-0b01: Generate baud rate using OVER and SCNT (the same as before) ● 0b10: When SCLK is selected as XTL (LPUART_SCON.SCLKSEL=0b10), generate a baud rate of 9600 using modulation method ● 0b11: When SCLK is selected as XTL (LPUART_SCON.SCLKSEL=0b10), generate a baud rate of 4800 using modulation method	RW

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23.5.10 9600/4800 Baud Rate Modulator Register (LPUART_MODU)

Offset	Bit Position																															
0x20	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000054A																															
Name	Reserved																				MODU											
Access																					RW											

Bit	Name	Functional Description	Access
31:12	*Reserved*	-	-
11:0	MODU	9600/4800 baud rate modulator When SCLK is selected as XTL (LPUART_SCON.SCLKSEL=0b10) and BSEL.BSEL = 0b10/0b11, this register is valid: ● When BSEL.BSEL = 0b10, the modulation settings required for a 9600 baud rate are generated, and the value to be set in this register should be 0x54A. ● When BSEL.BSEL = 0b11, the modulation settings required for a 4800 baud rate are generated, and the value to be set in this register should be 0xEFB.	RW

Principle of Generating 9600 Baud Rate

When SCLK is selected as XTL (LPUART_SCON.SCLKSEL=0b10), and the SCLK frequency is 32768. The baud rate of LPUART is 9600 (BSEL.BSEL = 0b10). Each bit requires 32768/9600 = 3.413 SCLKs. If each bit uses 3 SCLKs, the error of each bit is -0.413 SCLKs. If each bit uses 4 SCLKs, the error of each bit is +0.587 SCLKs.

Bit	Name	Number of SCLK	LPUART_MODU	Final Inaccuracy (Number of SCLK)
0	Start	3	0	-0.413
1	DATA[0]	4	1	+0.174(=-0.413+0.587)
2	DATA[1]	3	0	-0.239(=+0.174-0.413)
3	DATA[2]	4	1	+0.348(=-0.239+0.587)
4	DATA[3]	3	0	-0.065(=+0.348-0.413)
5	DATA[4]	3	0	-0.478(=-0.065-0.413)
6	DATA[5]	4	1	+0.109(=-0.478+0.587)
7	DATA[6]	3	0	-0.304(=+0.109-0.413)
8	DATA[7]	4	1	+0.283(=-0.304+0.587)
9	Parity/stop1	3	0	-0.130(=+0.283-0.413)
10	Stop1/stop2	4	1	+0.457(=-0.13+0.587)
11	Stop2	3	0	+0.044(=+0.457-0.413)

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Principle of Generating 4800 Baud Rate

When SCLK is selected as XTL (LPUART_SCON.SCLKSEL=0b10), and the SCLK frequency is 32768. The baud rate of LPUART is 4800 (BSEL.BSEL = 0b11). Each bit requires 32768/4800 = 6.827 SCLKs. If each bit uses 6 SCLKs, the error of each bit is -0.827 SCLKs. If each bit uses 7 SCLKs, the error of each bit is +0.173 SCLKs.

Bit	Name	Number of SCLK	LPUART_MODU	Final Inaccuracy (Number of SCLK)
0	Start	7	1	+0.173
1	DATA[0]	7	1	+0.346(=+0.173+0.173)
2	DATA[1]	6	0	-0.481(=+0.346-0.827)
3	DATA[2]	7	1	-0.308(=-0.481+0.173)
4	DATA[3]	7	1	-0.135(=-0.308+0.173)
5	DATA[4]	7	1	+0.038(=-0.135+0.173)
6	DATA[5]	7	1	+0.211(=+0.038+0.173)
7	DATA[6]	7	1	+0.384(=+0.211+0.173)
8	DATA[7]	6	0	-0.443(=+0.384-0.827)
9	Parity/stop1	7	1	-0.270(=-0.443+0.173)
10	Stop1/stop2	7	1	-0.097(=-0.270+0.173)
11	Stop2	7	1	+0.076(=-0.097+0.173)

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24 CRC

24.1 Introduction

CRC calculation unit takes data stream or block as input and generates output number controlled by generator polynomial. This output number is typically used to verify correctness and integrity of data transmission or storage. This module supports CRC value calculation and verification.

24.2 Features

- One implementation standard: ISO/IEC13239
- Two encoding methods: CRC-16, CRC-32
- Three write bit widths: 8-bit, 16-bit, 32-bit
- Two working modes: CRC encoding mode, CRC check mode
- CRC-16 polynomial: $x^{16}+ x^{12}+ x^5+ 1$
- CRC-32 polynomial: $x^{32}+ x^{26}+ x^{23}+ x^{22}+ x^{16}+ x^{12}+ x^{11}+ x^{10}+ x^8+ x^7+ x^5+ x^4+ x^2+ x + 1$

24.3 Functional Description

24.3.1 Working Mode

This module supports two working modes: CRC encoding mode and CRC check mode.

CRC encoding mode inputs a certain amount of original data to CRC module and obtains output value (CRC_RESULT). CRC check mode inputs a certain amount of encoded data sequence (original data + CRC check value) to verify match between original data and CRC check value (CRC_CR.FLAG).

24.3.2 Encoding Method

This module supports two encoding methods CRC-16 and CRC-32, with 16-bit and 32-bit results respectively, CRC_CR.CR configurable as needed.

CRC-16 Encoding

In this mode, the CRC algorithm model is CRC-16-X25:

- Polynomial: $x^{16}+x^{12}+x^5+1$;
- Initial value: 0xFFFFu;
- Result XOR value: 0xFFFFu;
- Input data inversion: True;
- Output data inversion: True.

CRC-32 Encoding

In this mode, the CRC algorithm model is CRC-32;

- Polynomial: $x^{32}+ x^{26}+ x^{23}+ x^{22}+ x^{16}+ x^{12}+ x^{11}+ x^{10}+ x^8+ x^7+ x^5+ x^4+ x^2+ x + 1$;
- Initial value: 0xFFFFFFFFu;
- Result XOR value: 0xFFFFFFFFu;
- Input data inversion: True;
- Output data inversion: True.

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24.3.3 Write Bit Width

This module supports three write bit widths: 8-bit, 16-bit, 32-bit. Different bit width writes must follow "bit width consistency, low-to-high" principle: "each write must use register matching data width, with lower bits written before higher bits".

Below demonstrates same data sequence written in three bit widths with identical output results.

- 8-bit width write: 0x00, 0x11, 0x22, 0x33, 0x44, 0x55, 0x66, 0x77
- 16-bit width write: 0x1100, 0x3322, 0x5544, 0x7766
- 32-bit width write: 0x33221100, 0x77665544

24.4 Operation Example

24.4.1 CRC-16 Encoding Mode

Procedure

Step1. Write CRC_CR.CR as 0b0 to select CRC-16.

Step2. Write CRC_RESULT[15:0] as 0xFFFF to initialize CRC calculation.

Step3. Write the raw data to be encoded sequentially to the CRC_DATA register, with selectable write bit width of 8-bit, 16-bit, or 32-bit.

Step4. Read CRC_RESULT[15:0] to obtain the CRC-16 calculation result.

24.4.2 CRC-16 Check Mode

Procedure

Step1. Write CRC_CR.CR as 0b0 to select CRC-16.

Step2. Write CRC_RESULT [15:0] as 0xFFFF to initialize CRC calculation.

Step3. Write the encoded data sequence (original data + CRC check value) into CRC_DATA register in sequence, with selectable write bit width of 8-bit, 16-bit, or 32-bit.

Step4. Determine whether the encoded data sequence has been tampered based on the value of CRC_CR.FLAG.

24.4.3 CRC-32 Encoding Mode

Procedure

Step1. Write CRC_CR.CR as 0b1 to select CRC-32.

Step2. Write CRC_RESULT[31:0] as 0xFFFFFFFF to initialize CRC calculation.

Step3. Write the raw data to be encoded sequentially to the CRC_DATA register, with selectable write bit width of 8-bit, 16-bit, or 32-bit.

Step4. Read CRC_RESULT[31:0] to obtain the CRC-32 calculation result.

24.4.4 CRC-32 Check Mode

Procedure

Step1. Write CRC_CR.CR as 0b1 to select CRC-32.

Step2. Write CRC_RESULT[31:0] as 0xFFFFFFFF to initialize CRC calculation.

Step3. Write the encoded data sequence (original data + CRC check value) into CRC_DATA register in sequence, with selectable write bit width of 8-bit, 16-bit, or 32-bit.

Step4. Determine whether the encoded data sequence has been tampered based on the value of CRC_CR.FLAG.

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24.5 Register Description

24.5.1 Register List

Base address: 0x40020900

Table 24-1 Cyclic Redundancy Check (CRC) Register Offset

Offset	Register	Description	Width
0x00	CRC_CR	Control Register	32
0x04	CRC_RESULT	Result Register	32
0x80	CRC_DATA	Data Register	32

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24.5.2 Control Register (CRC_CR)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000001																															
Name	Reserved																													FLAG	CR	
Access																														RO	RW	

Bit	Name	Functional Description	Access
31:2	*Reserved*	-	-
1	FLAG	CRC Check Result ● 0b0: Current CRC check error ● 0b1: Current CRC check correct	RO
0	CR	CRC Encoding Method Selection ● 0b0: CRC-16 code ● 0b1: CRC-32 code	RW

24.5.3 Result Register (CRC_RESULT)

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	RESULT																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	RESULT	CRC Calculation Result Read RESULT[15:0] to obtain the CRC-16 calculation result. Read RESULT[31:0] to obtain the CRC-32 calculation result. Write 0xFFFF to RESULT[15:0] to initialize CRC-16 calculation. Write 0xFFFFFFFF to RESULT[31:0] to initialize CRC-32 calculation.	RW

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24.5.4 Data Register (CRC_DATA)

Offset	Bit Position																													
0x80	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	DATA																															
Access	WO																															

Bit	Name	Functional Description	Access
31:0	DATA	Data for Operation Used to write the data to be operated on, supporting 3 write bit widths: ● 8-bit write mode: * ((uint8_t *)0x40020980) = 0xXX ● 16-bit write mode: * ((uint16_t *)0x40020980) = 0xXXXX ● 32-bit write mode: * ((uint32_t *)0x40020980) = 0xXXXXXXXX	WO

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25 TRNG

25.1 Introduction

The true random number module generates 64-bit true random numbers.

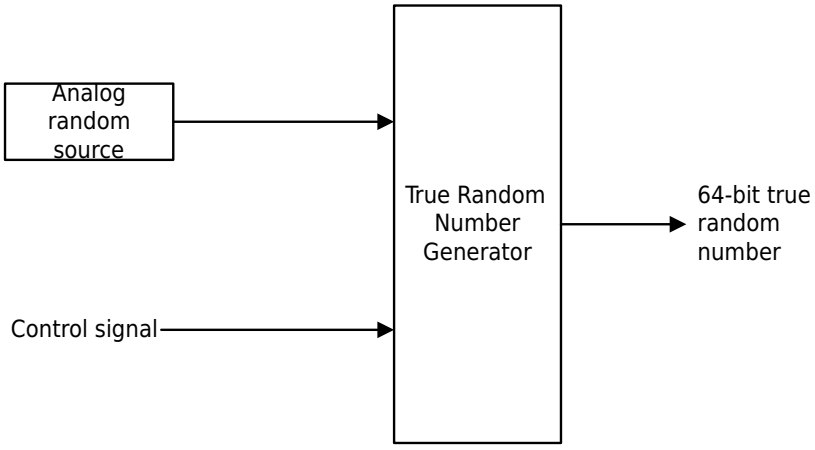

Figure 25-1 True Random Number Generator Function Block Diagram

25.2 Functional Description

25.2.1 True Random Number Generation Principle

This module uses an internal analog random source, which can generate 64bits true random numbers every time it is started. In addition, software configuration can be performed on the way of true random number generation. For details, refer to the Register Description section. The generated 64-bit true random numbers are stored in DATA0 and DATA1 registers respectively.

25.3 Operation Example

25.3.1 Generating 64bits True Random Number (The First Time After Power-On)

Procedure

Step1. Enable the random source circuit: Set TRNG_CR.TRNGCIR_EN to 0b1 to start the random source circuit, which begins outputting serial true random numbers.

Step2. Select reload initial value: Set TRNG_MODE.LOAD to 0b1 so that the initial value of newly generated true random numbers is obtained from the random source.

Step3. Select direct feedback mode for PRNG64: Set TRNG_MODE.FDBK to 0b1 to XOR the feedback signal with the random source before inputting it into the PRNG.

Step4. Select the shift count for PRNG64: Set TRNG_MODE.CNT to 0b110 to choose 256 shifts.

Step5. Generate true random numbers: Set TRNG_CR.TRNG_RUN to 0b1, and the hardware performs operations based on the true random number generation configuration. Upon completion, the hardware automatically clears TRNG_CR.TRNG_RUN.

Step6. Select not to reload the initial value: Set TRNG_MODE.LOAD to 0b0.

Step7. Select direct feedback mode for PRNG64: Set TRNG_MODE.FDBK to 0b0 to directly input the feedback signal into the PRNG.

Step8. Select the shift count for PRNG64: Set TRNG_MODE.CNT to 0b100 to choose 64 shifts.

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Step9. Generate true random numbers: Set TRNG_CR.TRNG_RUN to 0b1, and the hardware performs operations based on the true random number generation configuration. Upon completion, the hardware automatically clears TRNG_CR.TRNG_RUN.

Step10. Read true random numbers: After detecting that TRNG_CR.TRNG_RUN has changed to "0," the software reads TRNG_DATA0 and TRNG_DATA1 to obtain a 64-bit true random number.

Step11. After completing the generation of true random numbers, it is recommended to disable the random source circuit to save power: Set TRNG_CR.TRNGCIR_EN to 0b0 to turn off the random source circuit.

25.3.2 Generating 64bits True Random Number (Not Generated for the First Time After Power-on)

Procedure

Step1. Enable the random source circuit: Set TRNG_CR.TRNGCIR_EN to 0b1 to start the random source circuit, which begins outputting serial true random numbers.

Step2. Select not to reload the initial value: Set TRNG_MODE.LOAD to 0b0.

Step3. Select direct feedback mode for PRNG64: Set TRNG_MODE.FDBK to 0b1 to XOR the feedback signal with the random source before inputting it into the PRNG.

Step4. Select the shift count for PRNG64: Set TRNG_MODE.CNT to 0b110 to choose 256 shifts.

Step5. Generate true random numbers: Set TRNG_CR.TRNG_RUN to 0b1, and the hardware performs operations based on the true random number generation configuration. Upon completion, the hardware automatically clears TRNG_CR.TRNG_RUN.

Step6. Select direct feedback mode for PRNG64: Set TRNG_MODE.FDBK to 0b0 to directly input the feedback signal into the PRNG.

Step7. Select the shift count for PRNG64: Set TRNG_MODE.CNT to 0b100 to choose 64 shifts.

Step8. Read true random numbers: After detecting that TRNG_CR.TRNG_RUN has changed to "0," the software reads TRNG_DATA0 and TRNG_DATA1 to obtain a 64-bit true random number.
If new true random numbers need to be generated continuously, proceed to step 2 until the requirements are met.

Step9. After completing the generation of true random numbers, it is recommended to disable the random source circuit to save power: Set TRNG_CR.TRNGCIR_EN to 0b0 to turn off the random source circuit.

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25.4 Register Description

25.4.1 Register List

Base address: 0x40004C00

Table 25-1 True Random Number Generator (TRNG) Register Offset

Offset	Register	Description	Width
0x00	TRNG_CR	Control register	32
0x04	TRNG_MODE	Mode Register	32
0x0C	TRNG_DATA0	Data Register 0	32
0x10	TRNG_DATA1	Data Register 1	32

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25.4.2 Control Register (TRNG_CR)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																														TRNG_RUN	TRNGCIR_EN
Access																															RW	RW

Bit	Name	Functional Description	Access
31:2	*Reserved*	-	-
1	TRNG_RUN	True random number generation control The software writes "1" and starts to generate a new 64bits random number; after the operation is completed, the hardware is cleared; ● 0b0: The random number generation is completed ● 0b1: Write 1 to start random number generation, read 1 to indicate that random number is being generated	RW
0	TRNGCIR_EN	Random source circuit enable ● 0b0: Turn off the random source ● 0b1: Turn on the random source	RW

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25.4.3 Mode Register (TRNG_MODE)

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000010																															
Name	Reserved																											CNT			FDBK	LOAD
Access																												RW			RW	RW

Bit	Name	Functional Description	Access
31:5	*Reserved*	-	-
4:2	CNT	Feedback shift times of 64-bit TRNG ● 0b000: Shift 0 times (that is, output the sampling value of the random source) ● 0b001: Shift 8 times ● 0b010: Shift 16 times ● 0b011: Shift 32 times ● 0b100: Shift 64 times ● 0b101: Shift 128 times ● 0b110: Shift 256 times ● 0b111: Setting prohibited	RW
1	FDBK	During the shift operation, whether the feedback signal of the 64-bit TRNG is XORed with the random source ● 0b0: Do not perform XOR operation ● 0b1: Perform XOR operation	RW
0	LOAD	When generating a new random number, whether the 64-bit TRNG obtains a new initial value from the random source ● 0b0: Do not load new initial values (generating pseudo-random numbers) ● 0b1: Load a new initial value (generating true random numbers)	RW

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25.4.4 Data Register 0 (TRNG_DATA0)

Offset	Bit Position																													
0x0C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	DATA0																															
Access	RO																															

Bit	Name	Functional Description	Access
31:0	DATA0	Low 32-bit random number	RO

25.4.5 Data Register 1 (TRNG_DATA1)

Offset	Bit Position																													
0x10	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	DATA1																															
Access	RO																															

Bit	Name	Functional Description	Access
31:0	DATA1	High 32-bit random number	RO

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26 AES

26.1 Overview

AES (The Advanced Encryption Standard) is a new data encryption standard officially announced by the National Institute of Standards and Technology (NIST) on October 2, 2000.

The block size of AES is fixed at 128 bits, while the key length supports 128, 192, and 256 bits. For encryption, the input is a plaintext block and a key, and the output is a ciphertext block; for decryption, the input is a ciphertext block and a key, and the output is a plaintext block. The process is as follows:

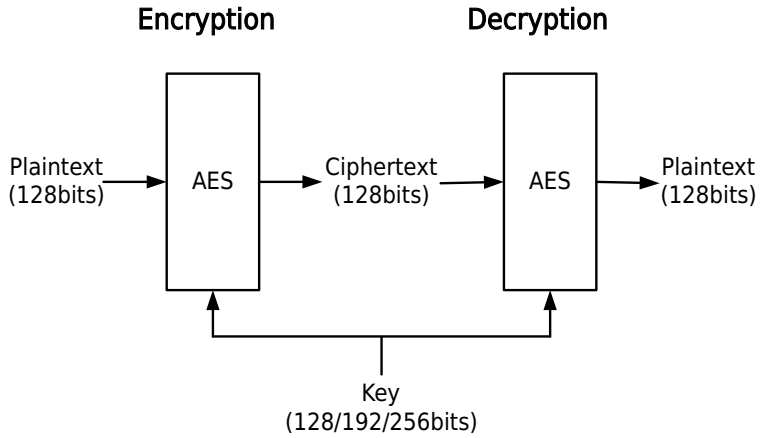

Figure 26-1 AES Encryption and Decryption Schematic Diagram

The basic unit of processing in the AES algorithm is the byte. A 128-bit message is divided into 16 bytes, which are copied into a 4×4 matrix called the state. All transformations in AES are based on transformations of the state matrix, which holds the intermediate results of the computation.

AES is a key-iterated block cipher that involves repeated applications of a round function to the state. The round transformations in AES consist of four operations: SubBytes, ShiftRows, MixColumns, and AddRoundKey. Specifically, SubBytes involves finding the modular inverse of each byte in GF(2^8) and an affine transformation; ShiftRows is a byte substitution that cyclically shifts the rows in the state by different offsets; MixColumns performs a linear transformation on each column of the state; and AddRoundKey performs a bitwise XOR operation between each byte in the state and the round key. The encryption process of AES is as follows:

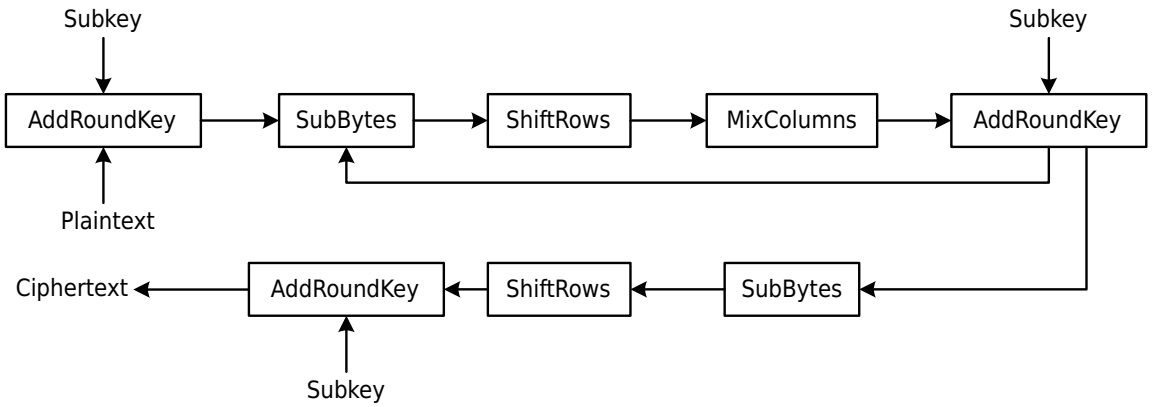

Figure 26-2 AES Encryption Flowchart

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The subkeys used in the diagram need to be derived from the initial key expansion, and the key expansion process is synchronized with the encryption process.

Since the plaintext is fixed at 128 bits, the number of rounds in the encryption process depends on the length of the key. For example, when the key is 128 bits, there are 10 rounds; when the key is 192 bits, there are 12 rounds; and when the key is 256 bits, there are 14 rounds. Except for the last round, which lacks the MixColumns transformation, all other rounds perform the complete round transformation operations.

The decryption process differs from the encryption process. First, all key expansions must be completed, and the decryption process starts from the last round subkey of the expansion and proceeds backward. Then, the four operations of the round transformation become their corresponding inverse operations: InvSubBytes, InvShiftRows, InvMixColumns, and AddRoundKey. The modular inverse operation in InvSubBytes remains unchanged, but the affine transformation is changed to inverse transformation; InvShiftRows and InvMixColumns become corresponding inverse transformations; AddRoundKey remains unchanged.

In the direct decryption process, the call order of the four operations in the round transformation is: InvShiftRows, InvSubBytes, AddRoundKey, InvMixColumns, which is inconsistent with the call order in the encryption process, but the keys used are the same as in the encryption process. In the equivalent decryption process, the call order of the four operations in the round transformation is: InvSubBytes, InvShiftRows, InvMixColumns, AddRoundKey, which is exactly the same as the call order in the encryption process, except that the subkey of each round needs to undergo the InvMixColumns operation.

For detailed algorithm descriptions, refer to the standard "FIPS PUB 197".

26.2 Features

- The execution results of the encryption and decryption processes of the AES algorithm standard fully comply with the description of the algorithm principles in "FIPS PUB 197".
- Supports 128-bit, 192-bit and 256-bit keys

26.3 Functional Description

26.3.1 Exception Mechanism

- Only 32-bit access is supported. Access with other bit widths will cause a system exception and enter the hardware exception interrupt.
- Accessing the AES module with an offset greater than or equal to 0x80 will cause a system exception and enter the hardware exception interrupt.

26.3.2 Runtime Instructions

The time required for the module to complete an operation (AES_CR.START written to 1) to the end of the operation (AES_CR.START restored to 0) is shown in the table below:

Table 26-1 AES Encryption and Decryption Running Time

Operation	128-Bit Key	192-Bit Key	256-Bit Key
Encryption	220 cycles	260 cycles	300 cycles
Decryption	290 cycles	332 cycles	398 cycles

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26.4 Operation Example

This module has two functions: encryption and decryption. The operations of these two functions share some common characteristics. Below, we will first introduce their common points, and then separately introduce the standard operating procedures for each function.

26.4.1 Common Points of Encryption and Decryption Operations

1. During AES encryption and decryption, the data register will change. If the data to be operated on next time is the result of the current operation, there is no need to rewrite the data.
2. Supports 128-bit, 192-bit, and 256-bit keys. A 128-bit key is written to the offset 0x20-0x2C, a 192-bit key is written to the offset 0x20-0x34, and a 256-bit key is written to the offset 0x20-0x3C.
3. Method to determine the end of the module's operation: Continuously read AES_CR.START. If its value becomes 0, it indicates the end of the operation.

26.4.2 Encryption Operation Procedures

Procedure

Step1. Write the 128-bit data to be encrypted into the data register (AES_DATA).

Step2. Write the encryption key into the key register (AES_KEY).

Step3. Set AES_CR.KEYSIZE according to the key length.

Step4. Set AES_CR.MODE to 0 to start encryption mode.

Step5. Write 1 to AES_CR.START in the control register to start the module's operation. Steps3-5 can be performed simultaneously.

Step6. Query AES_CR.START and wait for AES_CR.START to revert to 0, indicating the end of the module's operation.

Step7. Read the data register (AES_DATA) to obtain the 128-bit ciphertext.

26.4.3 Decryption Operation Procedures

Procedure

Step1. Write 128-bit data to be decrypted into the data register (AES_DATA).

Step2. Write the decryption key into the key register (AES_KEY).

Step3. Set AES_CR.KEYSIZE according to the key length.

Step4. Set AES_CR.MODE to 1 to enable decryption mode.

Step5. Write 1 to AES_CR.START in the control register to start the module's operation. Steps3-5 can be performed simultaneously.

Step6. Query AES_CR.START and wait for AES_CR.START to revert to 0, indicating the end of the module's operation.

Step7. Read the data register (AES_DATA) to obtain the 128-bit plaintext.

26.4.4 Data Example

128-Bit Key

128-bit plaintext: 0xFFEEDDCCBBAA99887766554433221100

128-bit key: 0x0F0E0D0C0B0A09080706050403020100

128-bit ciphertext: 0x5AC5B47080B7CDD830047B6AD8E0C469

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Table 26-2 128-Bit Operation Register Example

Before Encryption			
Register	Value (Key)	Register	Value (Plaintext)
AES_KEY0	0x03020100	AES_DATA0	0x33221100
AES_KEY1	0x07060504	AES_DATA1	0x77665544
AES_KEY2	0x0B0A0908	AES_DATA2	0xBBAA9988
AES_KEY3	0x0F0E0D0C	AES_DATA3	0xFFEEDDCC
After Encryption			
Register	Value (Key)	Register	Value (Ciphertext)
AES_KEY0	0x03020100	AES_DATA0	0xD8E0C469
AES_KEY1	0x07060504	AES_DATA1	0x30047B6A
AES_KEY2	0x0B0A0908	AES_DATA2	0x80B7CDD8
AES_KEY3	0x0F0E0D0C	AES_DATA3	0x5AC5B470

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192-Bit Key

128-bit plaintext: 0xFFEEDDCCBBAA99887766554433221100

192-bit key: 0x17161514131211100F0E0D0C0B0A09080706050403020100

128-bit ciphertext: 0x91710DECA070AF6EE0DF4C86A47CA9DD

Table 26-3 192-Bit Operation Register Example

Before Encryption			
Register	**Value (Key)**	**Register**	**Value (Plaintext)**
AES_KEY0	0x03020100	AES_DATA0	0x33221100
AES_KEY1	0x07060504	AES_DATA1	0x77665544
AES_KEY2	0x0B0A0908	AES_DATA2	0xBBAA9988
AES_KEY3	0x0F0E0D0C	AES_DATA3	0xFFEEDDCC
AES_KEY4	0x13121110		
AES_KEY5	0x17161514		
After Encryption			
Register	**Value (Key)**	**Register**	**Value (Ciphertext)**
AES_KEY0	0x03020100	AES_DATA0	0xA47CA9DD
AES_KEY1	0x07060504	AES_DATA1	0xE0DF4C86
AES_KEY2	0x0B0A0908	AES_DATA2	0xA070AF6E
AES_KEY3	0x0F0E0D0C	AES_DATA3	0x91710DEC
AES_KEY4	0x13121110		
AES_KEY5	0x17161514		

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256-Bit Key

128-bit plaintext: 0xFFEEDDCCBBAA99887766554433221100

256-bit key: 0x1F1E1D1C1B1A191817161514131211100F0E0D0C0B0A09080706050403020100

128-bit ciphertext: 0x8960494B9049FCAEBF456751CAB7A28E

Table 26-4 256-Bit Operation Register Example

Before Encryption			
Register	Value (Key)	Register	Value (Plaintext)
AES_KEY0	0x03020100	AES_DATA0	0x33221100
AES_KEY1	0x07060504	AES_DATA1	0x77665544
AES_KEY2	0x0B0A0908	AES_DATA2	0xBBAA9988
AES_KEY3	0x0F0E0D0C	AES_DATA3	0xFFEEDDCC
AES_KEY4	0x13121110		
AES_KEY5	0x17161514		
AES_KEY6	0x1B1A1918		
AES_KEY7	0x1F1E1D1C		
After Encryption			
Register	Value (Key)	Register	Value (Ciphertext)
AES_KEY0	0x03020100	AES_DATA0	0xCAB7A28E
AES_KEY1	0x07060504	AES_DATA1	0xBF456751
AES_KEY2	0x0B0A0908	AES_DATA2	0x9049FCAE
AES_KEY3	0x0F0E0D0C	AES_DATA3	0x8960494B
AES_KEY4	0x13121110		
AES_KEY5	0x17161514		
AES_KEY6	0x1B1A1918		
AES_KEY7	0x1F1E1D1C		

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26.5 Register Description

26.5.1 Register List

Base address: 0x40021400

Table 26-5 Advanced Encryption Standard Module (AES) Register Offset

Offset	Register	Description	Width
0x00	AES_CR	Control Register	32
0x10+0x4*n	AES_DATAn	Data Register n (n=0-3)	32
0x20+0x4*n	AES_KEYn	Key Register n (n=0-7)	32
0x40	AES_CRDM	Control Register Mapping Address	32

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26.5.2 Control Register (AES_CR)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																											KEYSIZE		Reserved	MODE	START
Access																												RW			RW	RW

Bit	Name	Functional Description	Access
31:5	*Reserved*	-	-
4:3	KEYSIZE	Key length ● 0b00: Key length is 128 bits ● 0b01: Key length is 192 bits ● 0b10: Key length is 256 bits ● 0b11: Key length is 128 bits	RW
2	*Reserved*	-	-
1	MODE	Operation mode ● 0b0: Encryption operation ● 0b1: Decryption operation	RW
0	START	Operation start control ● 0b0: Operation ended or not started ● 0b1: Start operation	RW

Note

- The operation method for the AES_CR.START bit is: After software writes 1 to this bit, the module will start running. After the current operation ends, the module's hardware will automatically clear this bit to 0. When software queries this bit and finds it to be 0, it indicates that the current operation is complete.
- Writes to this register can only be performed when the module is not in an operation state (for example, when AES_CR.START=0). Otherwise, the hardware will automatically ignore the write operation. Read operations are not subject to this restriction.
- The AES_CR register bit is located at the AES base address with an offset of 0. The mapping address for the AES_CR register is at an offset of 0x40 from the base address, with the same access and operation permissions as the AES_CR register.

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26.5.3 Data Register (AES_DATAn) (n=0-3)

Offset: 0x10+0x4*n

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	DATA																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	DATA	Plaintext/ciphertext data Stores 128-bit plaintext/ciphertext for the AES algorithm	RW

The data register consists of four 32-bit registers that form a 128-bit data used to store plaintext to be encrypted or ciphertext to be decrypted before the module's operation, and to store the encrypted ciphertext or decrypted plaintext after the operation is completed.

Encryption Operation		Decryption Operation	
Before Operation	After Operation	Before Operation	After Operation
128-bit Plaintext	128-bit Ciphertext	128-bit Ciphertext	128-bit Plaintext

The four 32-bit registers are concatenated to form a 128-bit data. Read and write operations require separate operations on each of the four registers. The fill-in data for the data register is as follows (using the data 0xFFEEDDCCBBAA99887766554433221100 as an example):

Table 26-11 Fill-in data for Register

AES_DATA0	AES_DATA1	AES_DATA2	AES_DATA3
0x33221100	0x77665544	0xBBAA9988	0xFFEEDDCC

Note

- Writes to this register can only be performed when the module is not in an operation state (for example, when AES_CR.START=0). Otherwise, the hardware will automatically ignore writes to this register.
- Reads from this register can only be performed when the module is not in an operation state (for example, when AES_CR.START=0). Otherwise, reads from this register will result in all zeros.

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26.5.4 Key Register (AES_KEYn) (n=0-7)

Offset: 0x20+0x4*n

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	KEY																															
Access	RW																															

Bit	Name	Functional Description	Access
31:0	KEY	AES key Stores 128 (KEY0-KEY3), 192 (KEY0-KEY5), 256 (KEY0-KEY7)-bit keys for the AES algorithm	RW

The key register consists of eight 32-bit registers that store the input initial key. Write operations require separate operations on each of the eight 32-bit registers. The corresponding fill-in data for register is shown in the examples below.

Example of 128-bit key: 0x0F0E0D0C_0B0A0908_07060504_03020100

Table 26-14 Fill-in data for Register - 128-bit key

AES_KEY0	AES_KEY1	AES_KEY2	AES_KEY3
0x03020100	0x07060504	0x0B0A0908	0x0F0E0D0C

Example of 192-bit key: 0x17161514_13121110_0F0E0D0C_0B0A0908_07060504_03020100

Table 26-15 Fill-in data for Register - 192-bit key

AES_KEY0	AES_KEY1	AES_KEY2	AES_KEY3	AES_KEY4	AES_KEY5
0x03020100	0x07060504	0x0B0A0908	0x0F0E0D0C	0x13121110	0x17161514

Example of 256-bit key:
0x1F1E1D1C_1B1A1918_17161514_13121110_0F0E0D0C_0B0A0908_07060504_03020100

Table 26-16 Fill-in data for Register - 256-bit key

AES_KEY0	AES_KEY1	AES_KEY2	AES_KEY3	AES_KEY4	AES_KEY5	AES_KEY6	AES_KEY7
0x03020100	0x07060504	0x0B0A0908	0x0F0E0D0C	0x13121110	0x17161514	0x1B1A1918	0x1F1E1D1C

Note

- Writes to this register can only be performed when the module is not in an operation state (for example, when AES_CR.START=0). Otherwise, the hardware will automatically ignore writes to this register.
- Reads from this register can only be performed when the module is not in an operation state (for example, when AES_CR.START=0). Otherwise, reads from this register will result in all zeros.

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26.5.5 Control Register Mapping Address (AES_CRDM)

Offset	Bit Position																													
0x40	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																											KEYSIZE		Reserved	MODE	START
Access																												RW			RW	RW

Bit	Name	Functional Description	Access
31:5	*Reserved*	-	-
4:3	KEYSIZE	Key length ● 0b00: Key length is 128 bits ● 0b01: Key length is 192 bits ● 0b10: Key length is 256 bits ● 0b11: Key length is 128 bits	RW
2	*Reserved*	-	-
1	MODE	Operation mode ● 0b0: Encryption operation ● 0b1: Decryption operation	RW
0	START	Operation start control ● 0b0: Operation ended or not started ● 0b1: Start operation	RW

Note

- The operation method for the AES_CR.START bit is: After software writes 1 to this bit, the module will start running. After the current operation ends, the module's hardware will automatically clear this bit to 0. When software queries this bit and finds it to be 0, it indicates that the current operation is complete.
- Writes to this register can only be performed when the module is not in an operation state (for example, when AES_CR.START=0). Otherwise, the hardware will automatically ignore the write operation. Read operations are not subject to this restriction.

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27 LCD

27.1 Introduction

The LCD controller is a digital controller/driver designed for monochrome passive liquid crystal display (LCD), featuring up to 8 common terminals (COM) to drive 188 (4x47), 270 (6x45) or 344 (8x43) LCD pixel elements. The exact number of terminals depends on the device pinout as stated in the Datasheet.

LCDs are made up of segments (either pixels or complete symbols) that can be either on or off. Each segment contains a layer of liquid crystal molecules aligned between two electrodes. When a voltage higher than the threshold voltage is applied to the liquid crystal, the corresponding segment becomes visible. The segment voltage must be AC to avoid electrophoretic effects in the liquid crystal (which will affect the display). Afterwards, waveforms must be generated across the segment to avoid DC.

Glossary

- Liquid Crystal Display(LCD): A passive display panel with terminals leading directly to the segment.
- Common (COM): Electrical connection terminals connected to multiple sections.
- Bias (BIAS): The voltage level used when driving the LCD, defined as 1/(the number of voltage levels that drive the LCD display-1).
- Segment (SEG): The smallest visual unit (the smallest constituent element, line or point on an LCD display).
- Duty Cycle (DUTY): A number defined as 1/(number of common terminals on the LCD display).
- Frame: One period of the waveform written to the segment.
- Frame Rate: Frames per second, ie the number of times an LCD segment is excited per second.

27.2 Features

- Highly flexible frame rate control
- Support static, 1/2, 1/3, 1/4, 1/6 and 1/8 duty cycle
- Support 1/2, 1/3 offset
- LCD data RAM with up to 16 registers
- The contrast of LCD can be configured through software
- Three drive waveform generation methods
  - Internal resistor divider, external resistor divider, external capacitor divider method
  - The power consumption of the internal resistor divider method can be configured through software to match the capacitive charge required by the LCD panel
- Support low power mode: LCD controller can display in Active, Sleep, DeepSleep mode
- Configurable frame interrupt
- Support LCD blinking function and configurable multiple blinking frequencies
- The unused LCD segments and common pins can be configured as digital or analog functions

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27.3 Functional Description

27.3.1 Function Block Diagram

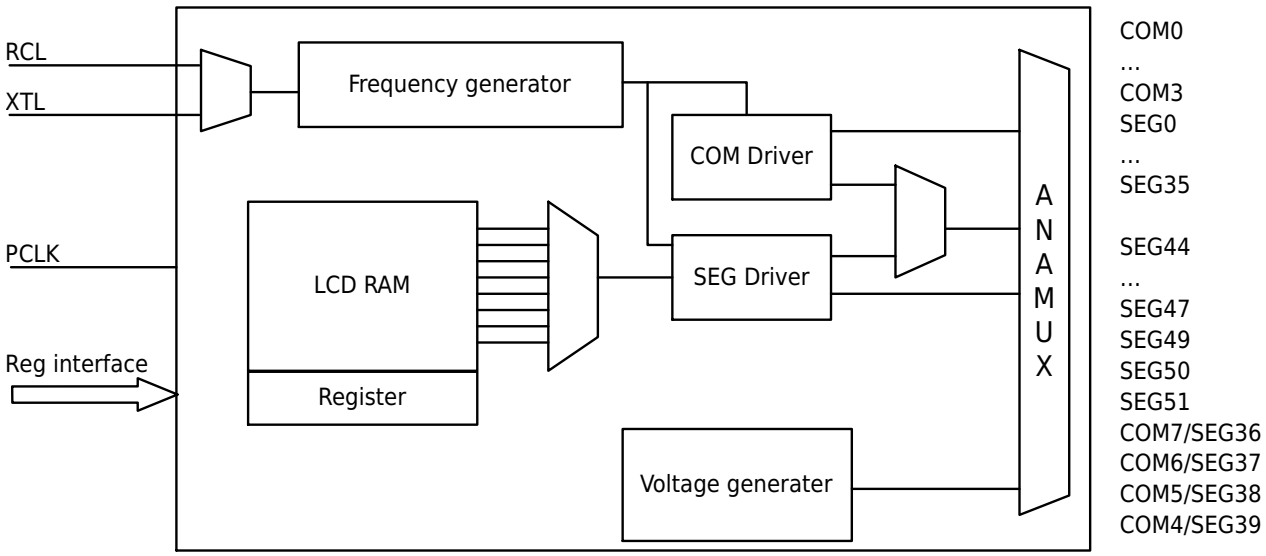

Figure 27-1 LCD Function Block Diagram

27.3.2 LCD Driving Waveform

LCD supports 6 driving waveforms with duty cycle (Duty): Static, 1/2, 1/3, 1/4, 1/6 and 1/8, which are set by LCD_CR0.DUTY. LCD supports 2 types of bias drive waveforms: 1/2, 1/3, configured via the LCD_CR0.BIAS register. The suggested combinations are shown in the table below:

	1/2 Duty	1/3 Duty	1/4 Duty	1/6 Duty	1/8 Duty
1/2 Bias	✔	✔	Not Recommended	Not Recommended	Not Recommended
1/3 Bias	Not Recommended	Not Recommended	✔	✔	✔

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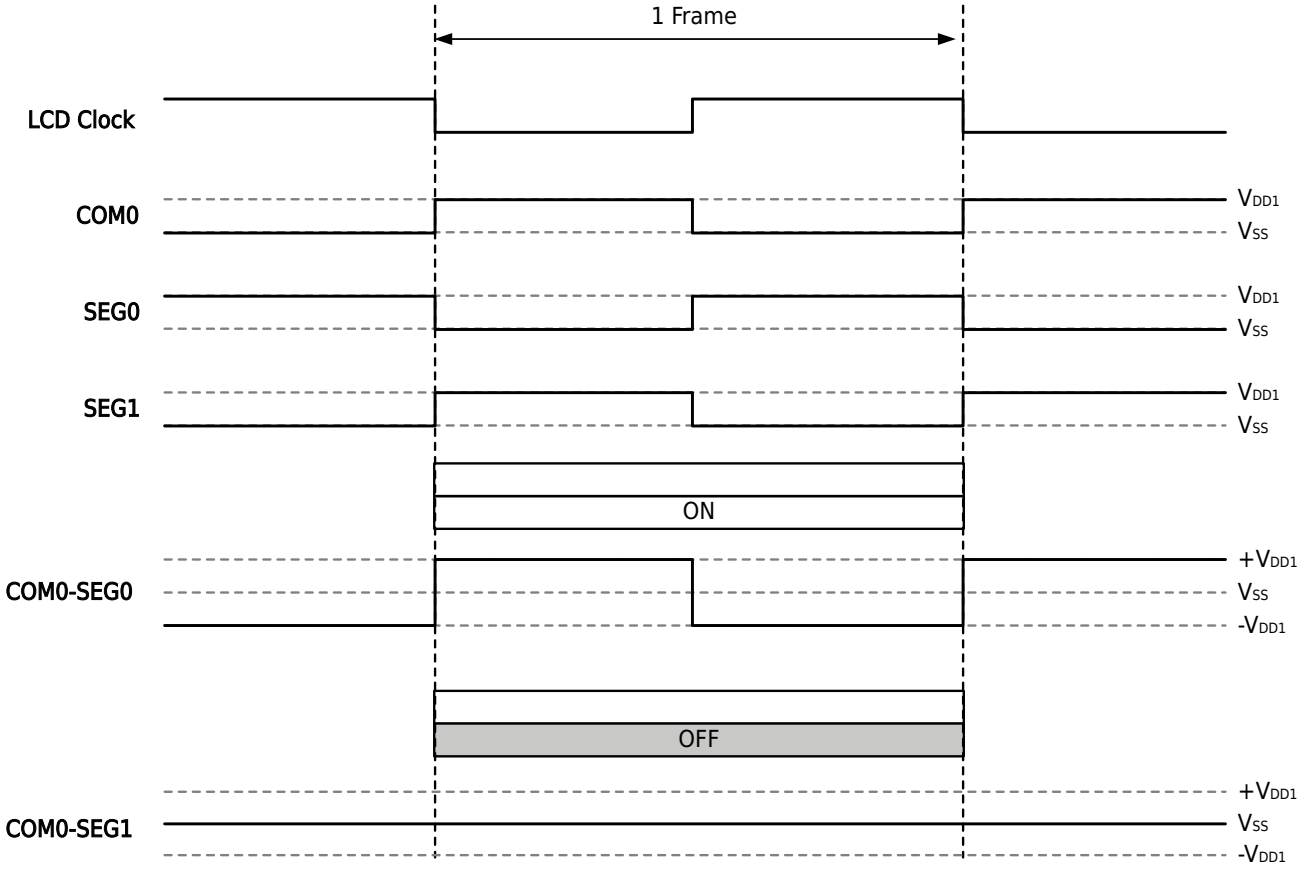
Static Drive Waveform



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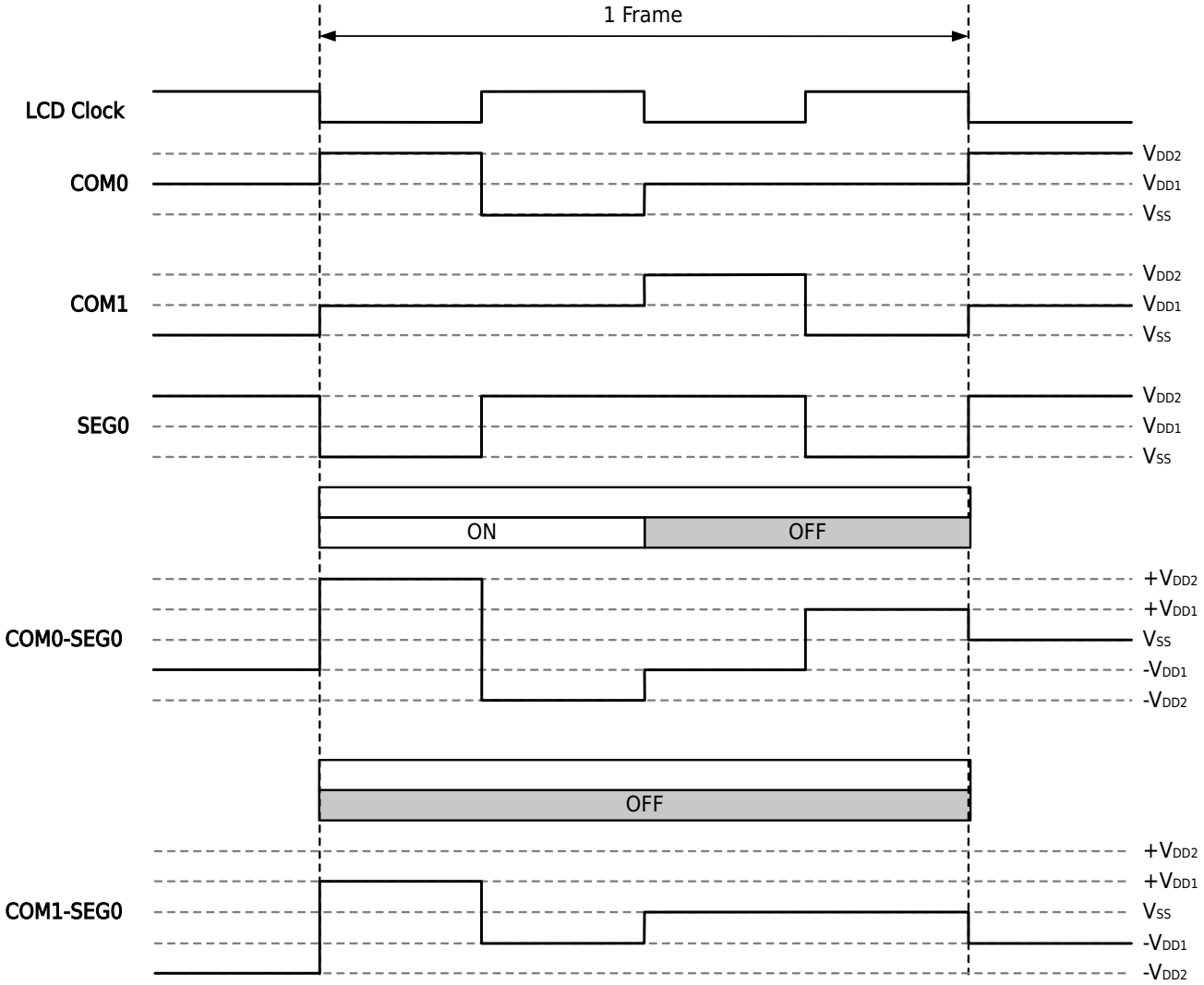
1/2Duty 1/2Bias Drive Waveform



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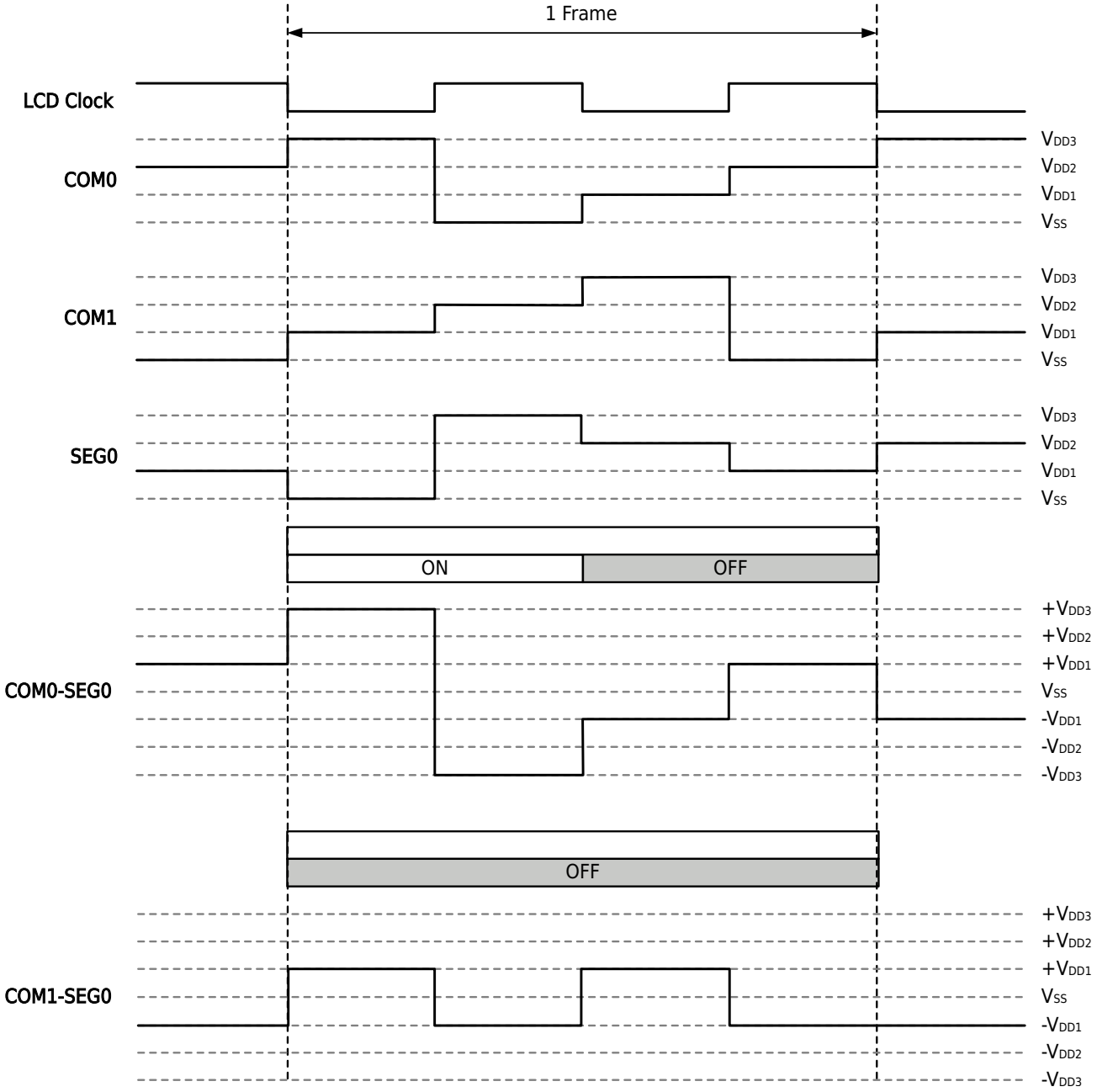
1/2Duty 1/3Bias Drive Waveform



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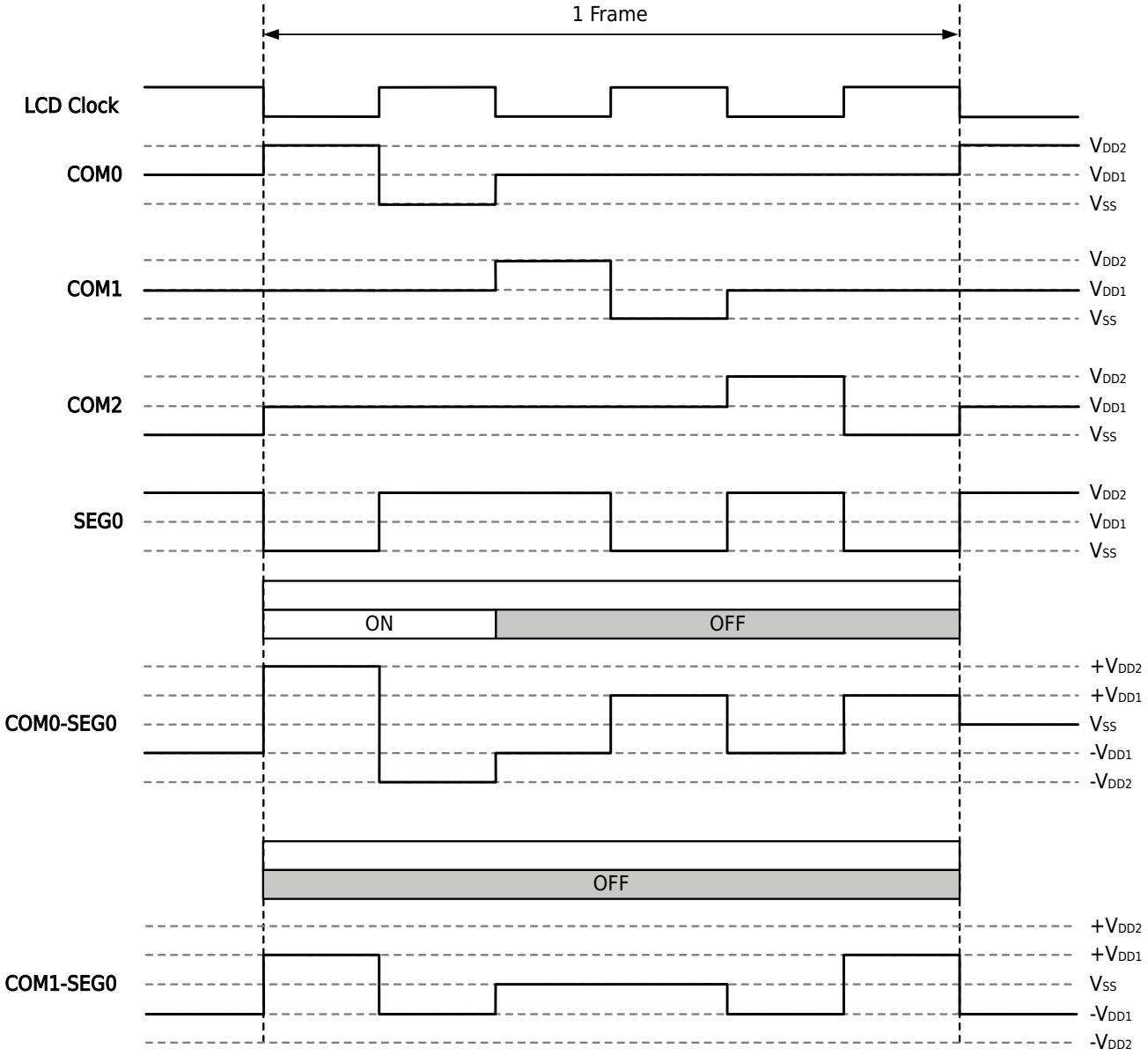
1/3Duty 1/2Bias Drive Waveform



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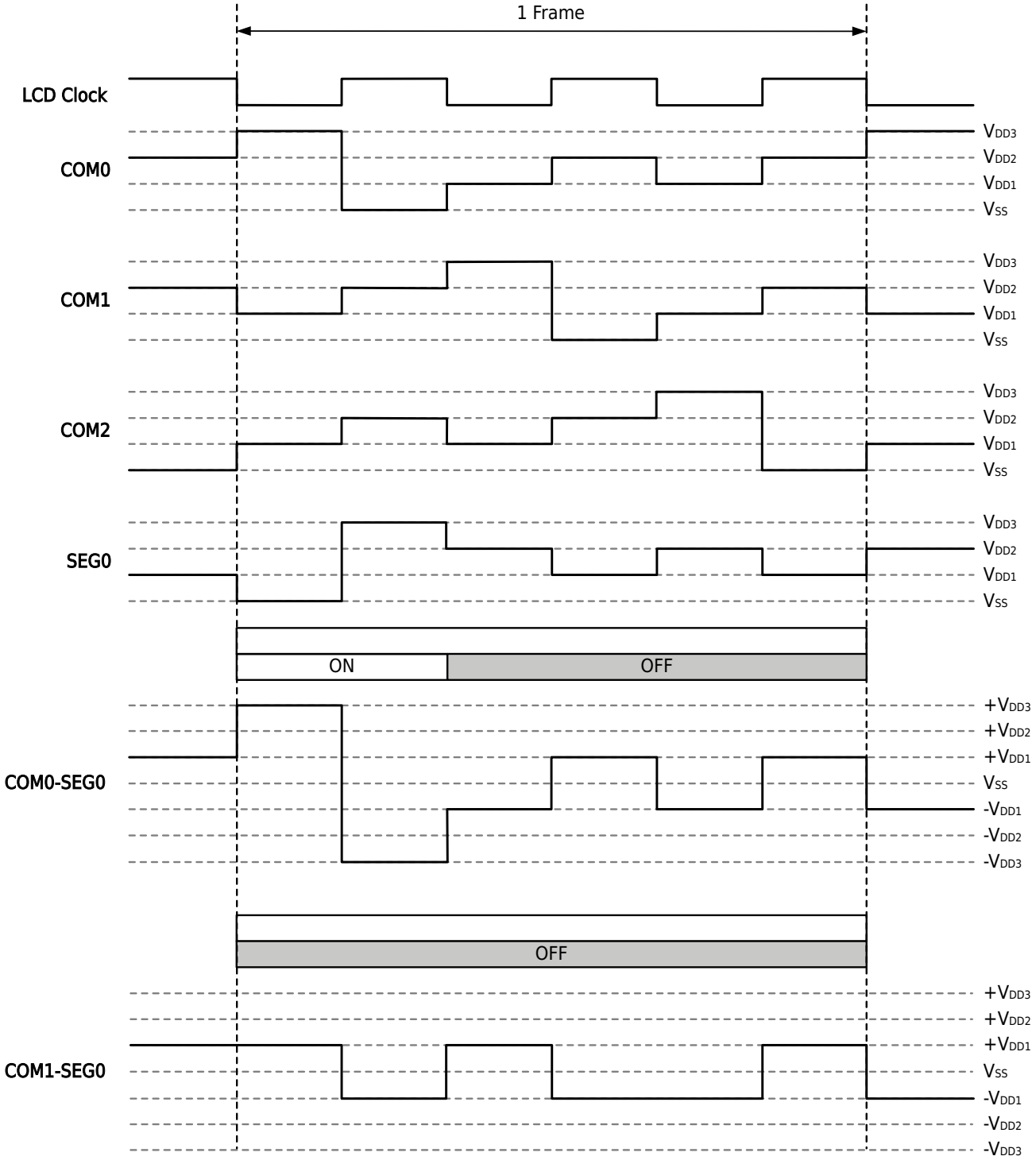
1/3Duty 1/3Bias Drive Waveform



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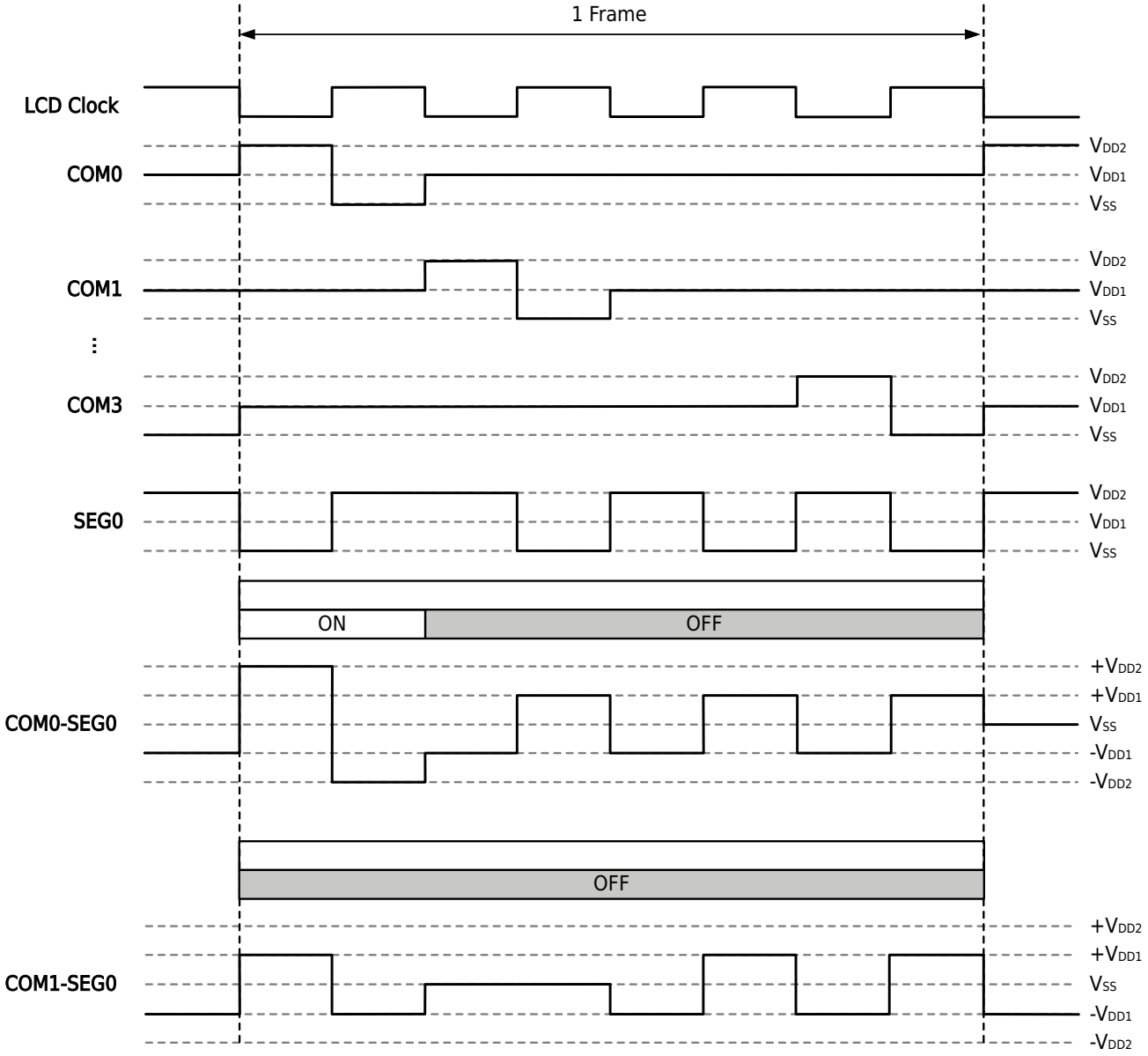
1/4Duty 1/2Bias Drive Waveform



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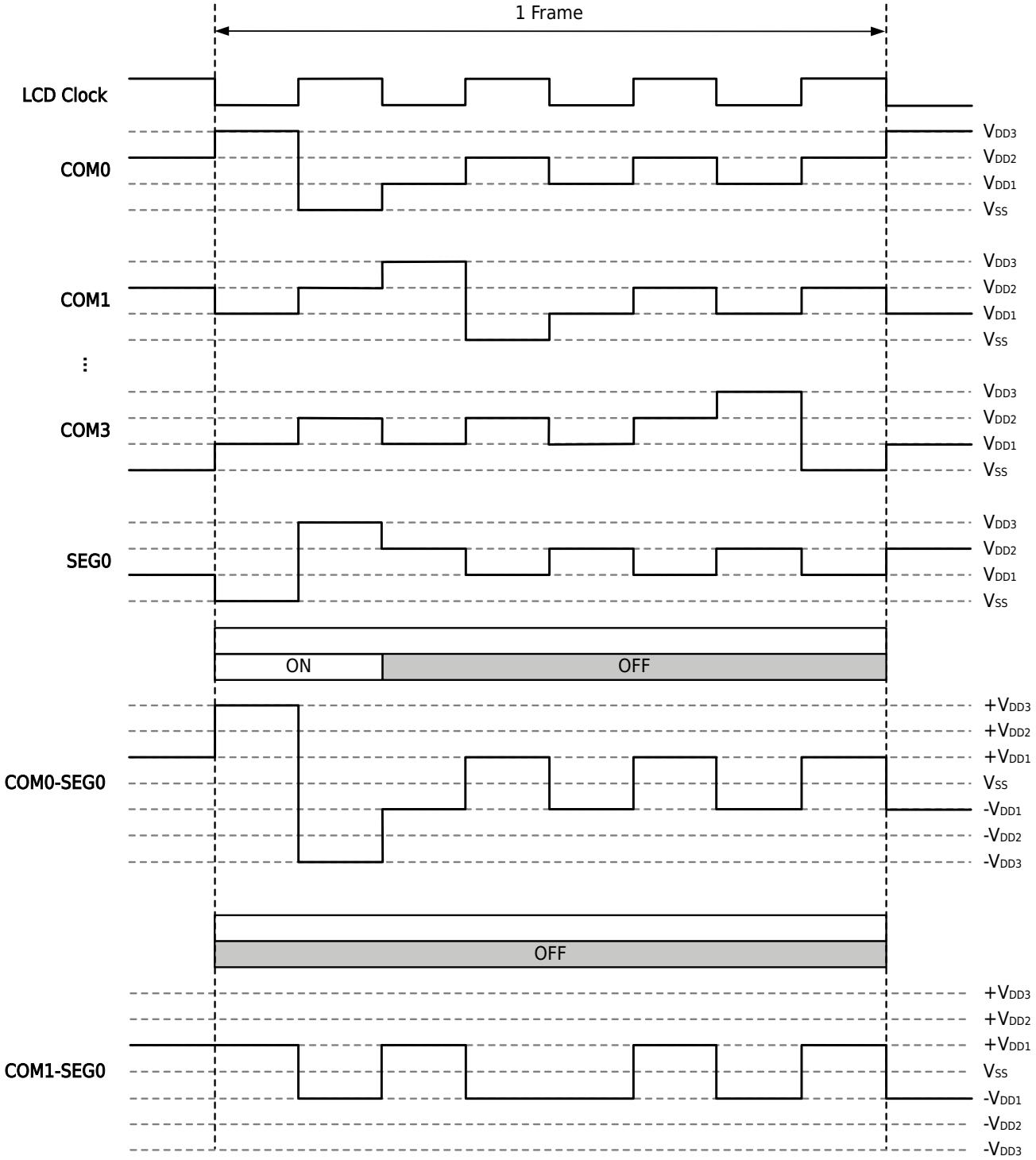
1/4Duty 1/3Bias Drive Waveform



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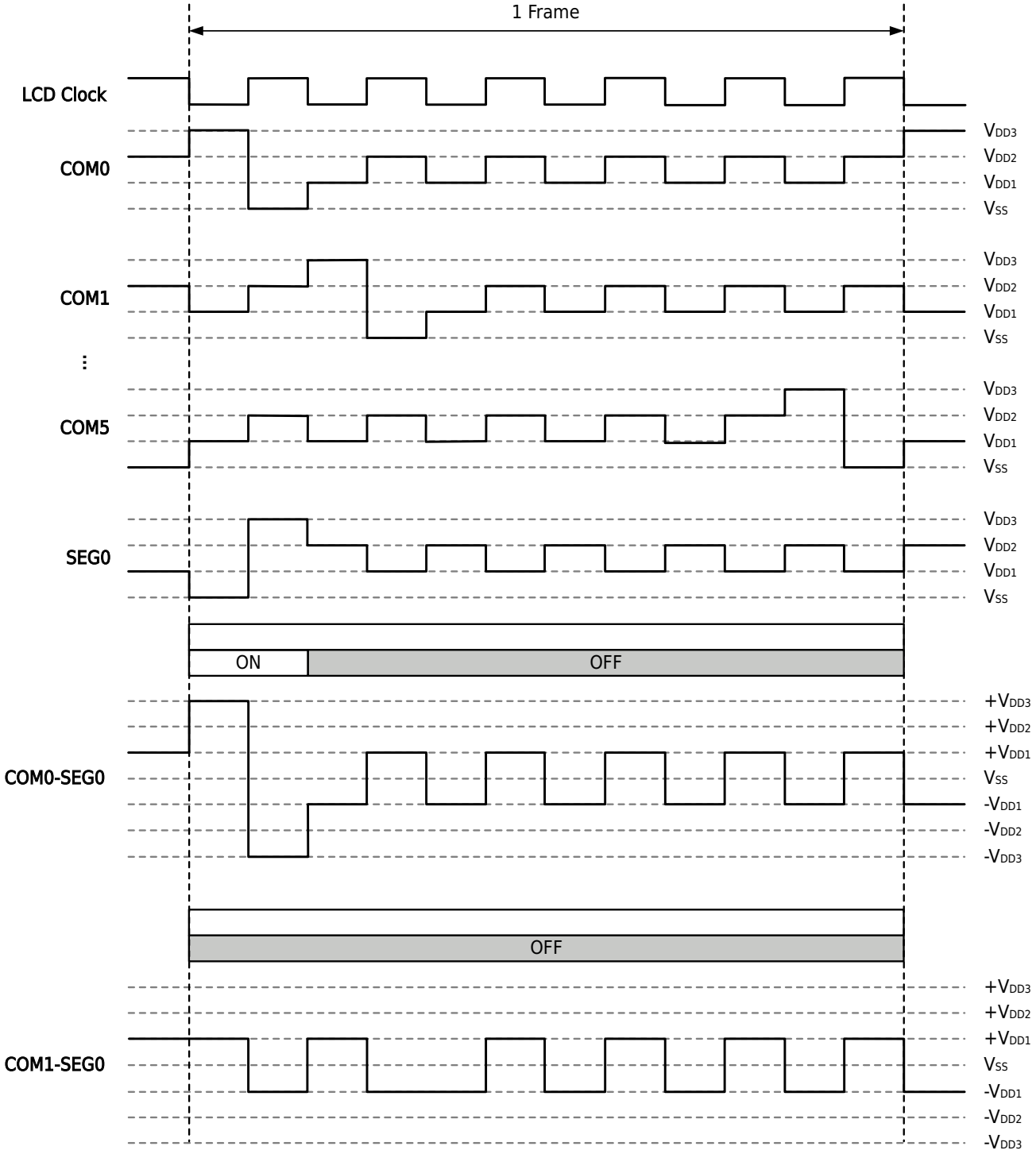
1/6Duty 1/3Bias Drive Waveform



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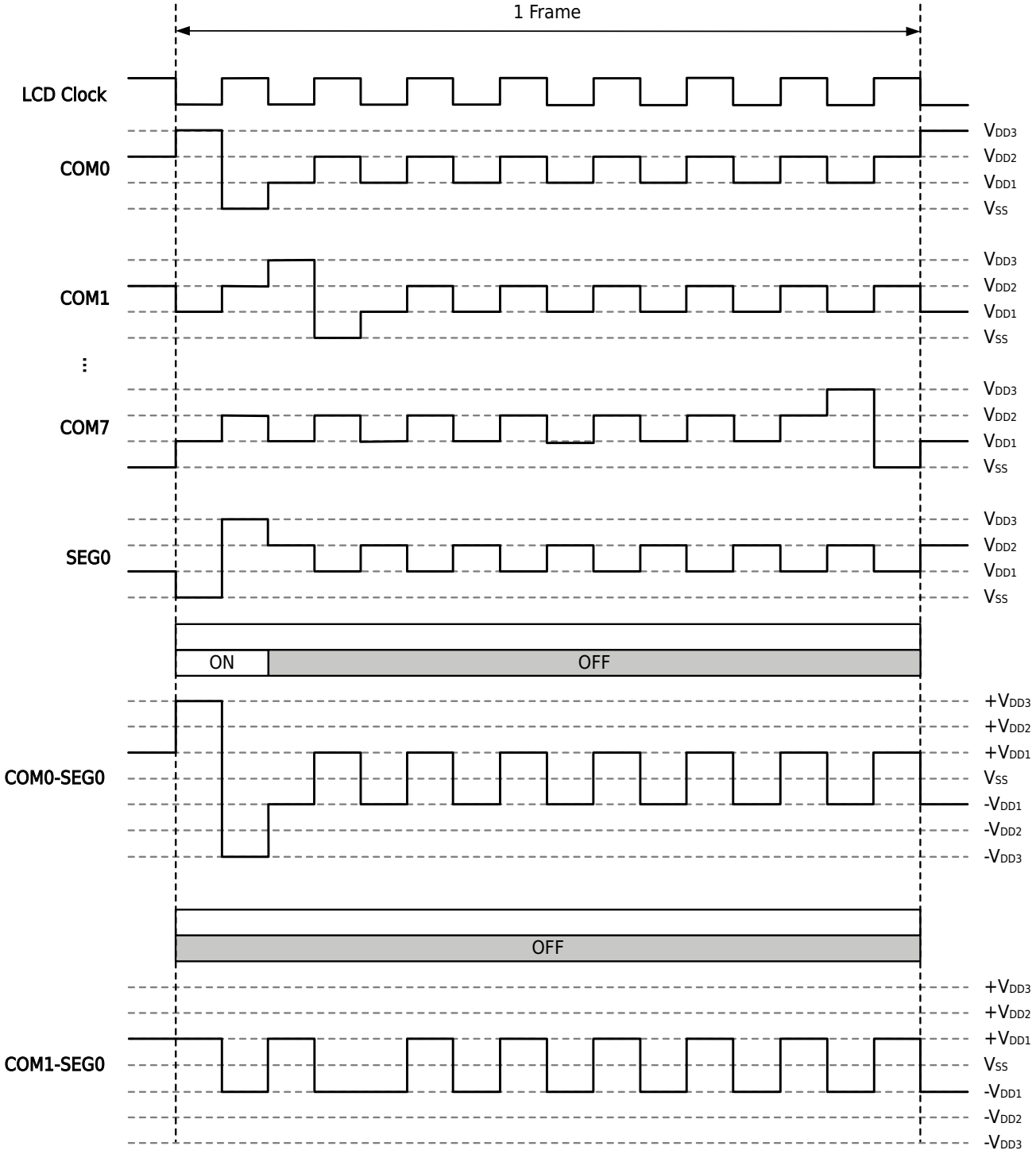
1/8Duty 1/3Bias Drive Waveform



27.3.3 LCD Bias Generation Circuit

LCD Bias voltage has three sources: internal resistor divider, external resistor divider, and external capacitor divider.

1. When the internal resistance voltage division is selected, the chip will automatically switch to the internal circuit, and the driving capability of this mode is weak. If the LCD screen to be driven is large, it is recommended to select the external resistor voltage division or external capacitor voltage division mode. Drive capability can also be enhanced by configuring the LCD_CR1.DRVRES register. When 1/2 bias is selected, resistances for high/medium/low power consumption are 240kΩ/360kΩ/

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720kΩ respectively; when 1/3 bias is selected, resistances for high/medium/low power consumption are 360kΩ/540kΩ/1080kΩ respectively.

2. When selecting an external resistor to divide the voltage, adjust the resistance value according to the system power consumption and LCD driving capability, and it is recommended to use a 500kΩ resistor. When selecting an external capacitor for voltage division, the drive capability is stronger, and a 100nF capacitor is recommended. However, these two circuits require users to build related circuits on the peripheral pins of the chip and occupy 4 IO ports.

Internal Resistance Mode

Internal resistance mode VLCDH, VLCD1-VLCD3 can be used as LCD SEG output or IO port.

In internal resistance mode, the driving voltage of LCD is controlled by CR0.CONTRAST, as shown in the table below:

CR0.CONTRAST	VLCD(1/3 bias)	VLCD(1/2 bias)
0	1.00*VCC	1.00*VCC
1	0.94*VCC	0.92*VCC
2	0.9*VCC	0.85*VCC
3	0.85*VCC	0.8*VCC
4	0.81*VCC	0.75*VCC
5	0.78*VCC	0.70*VCC
6	0.75*VCC	0.66*VCC
7	0.72*VCC	0.63*VCC
8	0.70*VCC	0.61*VCC
9	0.67*VCC	0.58*VCC
10	0.65*VCC	0.55*VCC
11	0.63*VCC	0.53*VCC
12	0.61*VCC	0.51*VCC
13	0.59*VCC	0.48*VCC
14	0.57*VCC	0.47*VCC
15	0.55*VCC	0.45*VCC

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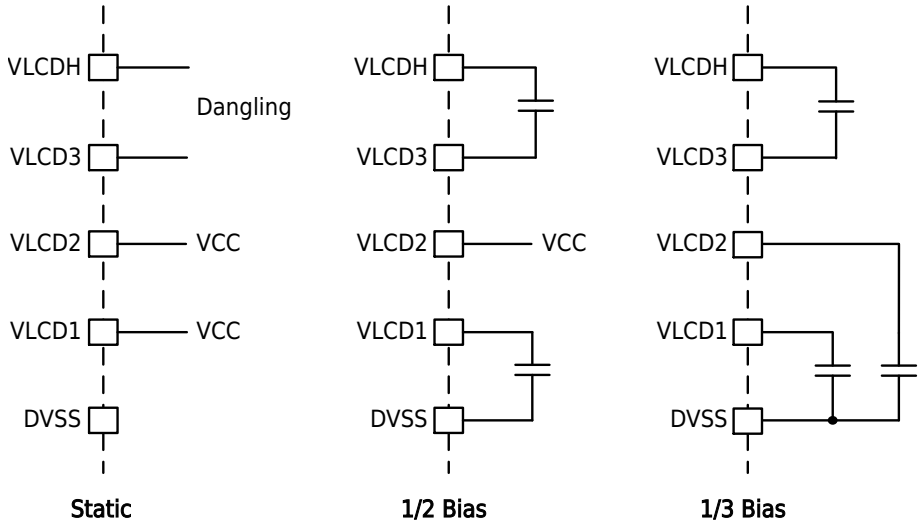
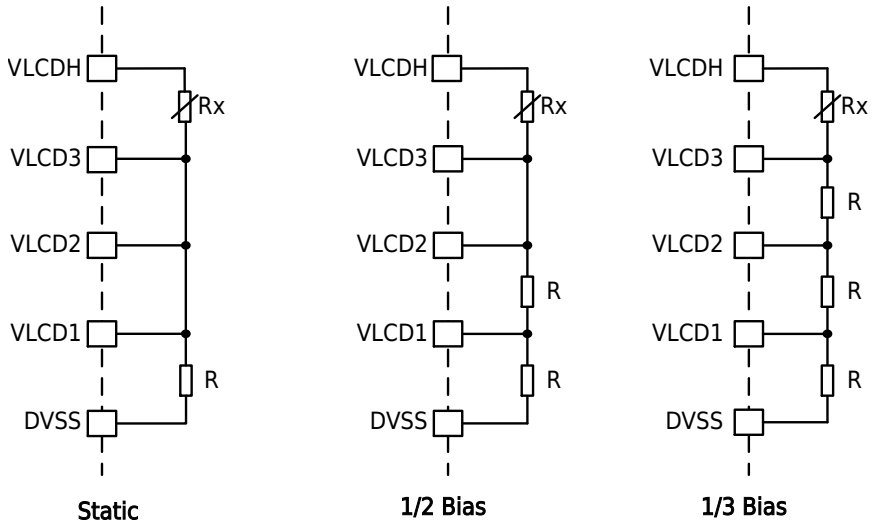
External Capacitor Mode



External Resistor Mode



Note

- Rx is an adjustable resistor for adjusting the contrast of LCD display.
- Select the proper resistor R according to the LCD screen used.

27.3.4 DMA

LCD supports software and hardware to trigger DMA data transmission, which can automatically move the content to be displayed from RAM or ROM to LCD display RAM. The hardware trigger uses the frame interrupt signal.

27.3.5 Interrupt

When the LCD setting is valid, the LCD interrupt can be configured to generate an interrupt for the frame number.

27.3.6 LCD Display Mode

The LCD supports two display modes. One uses COM as the display unit, and all COM segments of the same SEG are in the same byte (mode 0). The other is that different SEG of the same COM are in the

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same byte (mode 1). Selecting the appropriate display mode according to the LCD panel can simplify the program operation.

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LCD Display Mode 1 (MODE=1)

1/8 Duty

	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15	Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31	
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16	SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24	SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	
COM0																																	LCDRAM0
COM1																																	LCDRAM1
COM2																																	LCDRAM2
COM3																																	LCDRAM3
COM4																																	LCDRAM4
COM5																																	LCDRAM5
COM6																																	LCDRAM6
COM7																																	LCDRAM7
	SEG32	SEG33	SEG34	SEG35									SEG44	SEG45	SEG46	SEG47		SEG49	SEG50	SEG51													
COM0																																	LCDRAM8
COM1																																	LCDRAM9
COM2																																	LCDRAMA
COM3																																	LCDRAMB
COM4																																	LCDRAMC
COM5																																	LCDRAMD
COM6																																	LCDRAME
COM7																																	LCDRAMF

1/6 Duty

	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15	Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31	
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16	SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24	SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	
COM0																																	LCDRAM0
COM1																																	LCDRAM1
COM2																																	LCDRAM2
COM3																																	LCDRAM3
COM4																																	LCDRAM4
COM5																																	LCDRAM5
																																	LCDRAM6
																																	LCDRAM7
	SEG32	SEG33	SEG34	SEG35	SEG36	SEG37							SEG44	SEG45	SEG46	SEG47		SEG49	SEG50	SEG51													
COM0																																	LCDRAM8
COM1																																	LCDRAM9
COM2																																	LCDRAMA
COM3																																	LCDRAMB
COM4																																	LCDRAMC
COM5																																	LCDRAMD
																																	LCDRAME
																																	LCDRAMF

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1/4 Duty

	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15	Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31	
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16	SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24	SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	
COM0																																	LCDRAM0
COM1																																	LCDRAM1
COM2																																	LCDRAM2
COM3																																	LCDRAM3
																																	LCDRAM4
																																	LCDRAM5
																																	LCDRAM6
																																	LCDRAM7
	SEG32	SEG33	SEG34	SEG35	SEG36	SEG37	SEG38	SEG39					SEG44	SEG45	SEG46	SEG47		SEG49	SEG50	SEG51													
COM0																																	LCDRAM8
COM1																																	LCDRAM9
COM2																																	LCDRAMA
COM3																																	LCDRAMB
																																	LCDRAMC
																																	LCDRAMD
																																	LCDRAME
																																	LCDRAMF

1/3 Duty

	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15	Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31	
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16	SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24	SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	
COM0																																	LCDRAM0
COM1																																	LCDRAM1
COM2																																	LCDRAM2
																																	LCDRAM3
																																	LCDRAM4
																																	LCDRAM5
																																	LCDRAM6
																																	LCDRAM7
	SEG32	SEG33	SEG34	SEG35	SEG36	SEG37	SEG38	SEG39					SEG44	SEG45	SEG46	SEG47		SEG49	SEG50	SEG51													
COM0																																	LCDRAM8
COM1																																	LCDRAM9
COM2																																	LCDRAMA
																																	LCDRAMB
																																	LCDRAMC
																																	LCDRAMD
																																	LCDRAME
																																	LCDRAMF

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1/2 Duty

	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15	Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31	
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16	SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24	SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	
COM0																																	LCDRAM0
COM1																																	LCDRAM1
																																	LCDRAM2
																																	LCDRAM3
																																	LCDRAM4
																																	LCDRAM5
																																	LCDRAM6
																																	LCDRAM7
	SEG32	SEG33	SEG34	SEG35	SEG36	SEG37	SEG38	SEG39					SEG44	SEG45	SEG46	SEG47		SEG49	SEG50	SEG51													
COM0																																	LCDRAM8
COM1																																	LCDRAM9
																																	LCDRAMA
																																	LCDRAMB
																																	LCDRAMC
																																	LCDRAMD
																																	LCDRAME
																																	LCDRAMF

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LCD Display Mode 0 (MODE=0)

1/8 Duty

Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15	Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31	
COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7	COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7	COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7	COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7	
SEG0								SEG1								SEG2								SEG3								LCDRAM0
SEG4								SEG5								SEG6								SEG7								LCDRAM1
SEG8								SEG9								SEG10								SEG11								LCDRAM2
SEG12								SEG13								SEG14								SEG15								LCDRAM3
SEG16								SEG17								SEG18								SEG19								LCDRAM4
SEG20								SEG21								SEG22								SEG23								LCDRAM5
SEG24								SEG25								SEG26								SEG27								LCDRAM6
SEG28								SEG29								SEG30								SEG31								LCDRAM7
SEG32																																LCDRAM8
SEG33																SEG49																LCDRAM9
SEG34																SEG50																LCDRAMA
SEG35																SEG51																LCDRAMB
								SEG44																								LCDRAMC
								SEG45																								LCDRAMD
								SEG46																								LCDRAME
								SEG47																								LCDRAMF

1/6 Duty

Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15	Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31	
COM0	COM1	COM2	COM3	COM4	COM5			COM0	COM1	COM2	COM3	COM4	COM5			COM0	COM1	COM2	COM3	COM4	COM5			COM0	COM1	COM2	COM3	COM4	COM5			
SEG0								SEG1								SEG2								SEG3								LCDRAM0
SEG4								SEG5								SEG6								SEG7								LCDRAM1
SEG8								SEG9								SEG10								SEG11								LCDRAM2
SEG12								SEG13								SEG14								SEG15								LCDRAM3
SEG16								SEG17								SEG18								SEG19								LCDRAM4
SEG20								SEG21								SEG22								SEG23								LCDRAM5
SEG24								SEG25								SEG26								SEG27								LCDRAM6
SEG28								SEG29								SEG30								SEG31								LCDRAM7
SEG32																																LCDRAM8
SEG33																SEG49																LCDRAM9
SEG34																SEG50																LCDRAMA
SEG35																SEG51																LCDRAMB
SEG36								SEG44																								LCDRAMC
SEG37								SEG45																								LCDRAMD
								SEG46																								LCDRAME
								SEG47																								LCDRAMF

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1/4 Duty

Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15	Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31	
COM0	COM1	COM2	COM3					COM0	COM1	COM2	COM3					COM0	COM1	COM2	COM3					COM0	COM1	COM2	COM3					
SEG0								SEG1								SEG2								SEG3								LCDRAM0
SEG4								SEG5								SEG6								SEG7								LCDRAM1
SEG8								SEG9								SEG10								SEG11								LCDRAM2
SEG12								SEG13								SEG14								SEG15								LCDRAM3
SEG16								SEG17								SEG18								SEG19								LCDRAM4
SEG20								SEG21								SEG22								SEG23								LCDRAM5
SEG24								SEG25								SEG26								SEG27								LCDRAM6
SEG28								SEG29								SEG30								SEG31								LCDRAM7
SEG32																																LCDRAM8
SEG33																SEG49																LCDRAM9
SEG34																SEG50																LCDRAMA
SEG35																SEG51																LCDRAMB
SEG36								SEG44																								LCDRAMC
SEG37								SEG45																								LCDRAMD
SEG38								SEG46																								LCDRAME
SEG39								SEG47																								LCDRAMF

1/3 Duty

Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15	Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31	
COM0	COM1	COM2						COM0	COM1	COM2						COM0	COM1	COM2						COM0	COM1	COM2						
SEG0								SEG1								SEG2								SEG3								LCDRAM0
SEG4								SEG5								SEG6								SEG7								LCDRAM1
SEG8								SEG9								SEG10								SEG11								LCDRAM2
SEG12								SEG13								SEG14								SEG15								LCDRAM3
SEG16								SEG17								SEG18								SEG19								LCDRAM4
SEG20								SEG21								SEG22								SEG23								LCDRAM5
SEG24								SEG25								SEG26								SEG27								LCDRAM6
SEG28								SEG29								SEG30								SEG31								LCDRAM7
SEG32																																LCDRAM8
SEG33																SEG49																LCDRAM9
SEG34																SEG50																LCDRAMA
SEG35																SEG51																LCDRAMB
SEG36								SEG44																								LCDRAMC
SEG37								SEG45																								LCDRAMD
SEG38								SEG46																								LCDRAME
SEG39								SEG47																								LCDRAMF

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1/2 Duty

Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15	Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31	
COM0	COM1							COM0	COM1							COM0	COM1							COM0	COM1							
SEG0								SEG1								SEG2								SEG3								LCDRAM0
SEG4								SEG5								SEG6								SEG7								LCDRAM1
SEG8								SEG9								SEG10								SEG11								LCDRAM2
SEG12								SEG13								SEG14								SEG15								LCDRAM3
SEG16								SEG17								SEG18								SEG19								LCDRAM4
SEG20								SEG21								SEG22								SEG23								LCDRAM5
SEG24								SEG25								SEG26								SEG27								LCDRAM6
SEG28								SEG29								SEG30								SEG31								LCDRAM7
SEG32																																LCDRAM8
SEG33																SEG49																LCDRAM9
SEG34																SEG50																LCDRAMA
SEG35																SEG51																LCDRAMB
SEG36								SEG44																								LCDRAMC
SEG37								SEG45																								LCDRAMD
SEG38								SEG46																								LCDRAME
SEG39								SEG47																								LCDRAMF

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27.4 Operation Example

27.4.1 Basic Configuration Process

Procedure

Step1. Enable the LCD clock and GPIO clock.

Step2. Configure the pins used by the LCD as analog functions.

Step3. Configure the LCD_POEN0 and LCD_POEN1 registers: Enable output for used COM and SEG lines, and disable output for unused ports.

Step4. Configure the Bias voltage source, Duty, Bias, voltage pump clock frequency, scan frequency, LCD RAM display mode, and LCD clock source.

Step5. If the LCD Bias voltage source is an internal resistor, configure appropriate contrast and strong-drive pulse control parameters as needed.

Step6. Enable the LCD.

Step7. Write the display content to the LCD RAM.

27.4.2 DMA Data Transfer Configuration Process

Procedure

Step1. Open LCD DMA hardware trigger enable

Step2. Enable DMA

Step3. Set the transmission type, transmission length, transmission method

Step4. Set source start address, destination start address

Step5. Set the increment mode of source address and destination address

Step6. Enable DMA interrupts as needed

Step7. Selects LCD as DMA trigger source

Step8. Enable DMA channel

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27.5 Register Description

27.5.1 Register List

Base address: 0x40005C00

Table 27-13 Liquid Crystal Display Controller (LCD) Register Offset

Offset	Register	Description	Width
0x000	LCD_CR0	LCD Configuration Register 0	32
0x004	LCD_CR1	LCD Configuration Register 1	32
0x008	LCD_INTCLR	LCD Interrupt Clear Register	32
0x00C	LCD_POEN0	LCD Output Configuration Register 0	32
0x010	LCD_POEN1	LCD Output Configuration Register 1	32
0x040	LCD_RAM0	LCD RAM0	32
0x044	LCD_RAM1	LCD RAM1	32
0x048	LCD_RAM2	LCD RAM2	32
0x04C	LCD_RAM3	LCD RAM3	32
0x050	LCD_RAM4	LCD RAM4	32
0x054	LCD_RAM5	LCD RAM5	32
0x058	LCD_RAM6	LCD RAM6	32
0x05C	LCD_RAM7	LCD RAM7	32
0x060	LCD_RAM8	LCD RAM8	32
0x064	LCD_RAM9	LCD RAM9	32
0x068	LCD_RAMA	LCD RAM10	32
0x06C	LCD_RAMB	LCD RAM11	32
0x070	LCD_RAMC	LCD RAM12	32
0x074	LCD_RAMD	LCD RAM13	32
0x078	LCD_RAME	LCD RAM14	32
0x07C	LCD_RAMF	LCD RAM15	32

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27.5.2 Configuration Register 0 (LCD_CR0)

Offset	Bit Position																													
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000000DA																															
Name	Reserved																CONTRAST				BSEL			DUTY			BIAS		CPCLK		LCDCLK	EN
Access																	RW				RW			RW			RW		RW		RW	RW

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:12	CONTRAST	LCD contrast adjustment The larger the CONTRAST value is, the smaller the amplitude of the LCD waveform will be. ● 0b0000: The LCD waveform has the largest amplitude and the largest contrast ● ..... ● 0b1111: The LCD waveform amplitude is the smallest, and the contrast is the smallest **Note** It is only valid when the BIAS voltage source selects internal resistor voltage divider.	RW
11:9	BSEL	BIAS voltage source selection ● 0b000: External resistance mode,requires external circuit cooperation ● 0b001: Capacitive voltage divider mode, requires external circuit cooperation ● 0b010: Internal resistor divider, medium power consumption mode ● 0b011: Setting prohibited ● 0b100: Internal resistor divider, low power consumption mode ● 0b101: Setting prohibited ● 0b110: Internal resistor divider, high power consumption mode ● 0b111: Setting prohibited	RW
8:6	DUTY	LCD duty configuration ● 0b000: Static ● 0b001: 1/2 duty ● 0b010: 1/3 duty ● 0b011: 1/4 duty ● 0b100: Setting prohibited ● 0b101: 1/6 duty ● 0b110: Setting prohibited ● 0b111: 1/8 duty	RW

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<table>
<tr><th>Bit</th><th>Name</th><th>Functional Description</th><th>Access</th></tr>
<tr><td>8:6</td><td>DUTY</td><td>Table 27-16 Configuration of COMy/SEGx PAD Functions Under Different Duty Ratios
<table>
<tr><th>PAD</th><th>1/4 duty</th><th>1/6 duty</th><th>1/8 duty</th></tr>
<tr><td>COM4/SEG39</td><td>SEG39</td><td>COM4</td><td>COM4</td></tr>
<tr><td>COM5/SEG38</td><td>SEG38</td><td>COM5</td><td>COM5</td></tr>
<tr><td>COM6/SEG37</td><td>SEG37</td><td>SEG37</td><td>COM6</td></tr>
<tr><td>COM7/SEG36</td><td>SEG36</td><td>SEG36</td><td>COM7</td></tr>
</table></td><td>RW</td></tr>
<tr><td>5</td><td>BIAS</td><td>LCD BIAS configuration
● 0b0: 1/3 bias
● 0b1: 1/2 bias</td><td>RW</td></tr>
<tr><td>4:3</td><td>CPCLK</td><td>Voltage pump clock frequency selection
● 0b00: 2kHz
● 0b01: 4kHz
● 0b10: 8kHz
● 0b11: 16kHz</td><td>RW</td></tr>
<tr><td>2:1</td><td>LCDCLK</td><td>LCD scan frequency selection
● 0b00: 64Hz
● 0b01: 128Hz
● 0b10: 256Hz
● 0b11: 512Hz
Note
LCD frame frequency = LCD scanning frequency × Duty</td><td>RW</td></tr>
<tr><td>0</td><td>EN</td><td>LCD enable control
● 0b0: Disable
● 0b1: Enable</td><td>RW</td></tr>
</table>

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27.5.3 Configuration Register 1 (LCD_CR1)

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																		DRVRES		INTF	DMAEN	IE	MODE	CLKSRC	BLINKEN	BLINKCNT					
Access																			RW		RO	RW	RW	RW	RW	RW	RW					

Bit	Name	Functional Description	Access
31:14	*Reserved*	-	-
13:12	DRVRES	Internal resistor mode enhanced drive pulse control ● 0b00: OFF, disable enhanced drive pulse ● 0b01: 16μs, low-level enhanced drive pulse ● 0b10: 32μs, medium-level enhanced drive pulse ● 0b11: 64μs, high-level enhanced drive pulse	RW
11	INTF	Interrupt flag ● 0b0: No interrupt generated ● 0b1: Generate an interrupt	RO
10	DMAEN	DMA hardware trigger enable ● 0b0: Disable ● 0b1: Enable	RW
9	IE	Interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
8	MODE	LCD RAM display mode selection ● 0b0: Mode 0 ● 0b1: Mode 1	RW
7	CLKSRC	LCD clock source selection ● 0b0:RCL ● 0b1:XTL	RW
6	BLINKEN	LCD splash screen configuration ● 0b0: Disable ● 0b1: Enable	RW
5:0	BLINKCNT	Splash screen frequency and LCD interrupt interval setting LCD blinking frequency = LCD frame frequency/(BlinkCnt + 1) LCD interrupt interval = (1/LCD frame frequency) × (BlinkCnt + 1)	RW

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27.5.4 Interrupt Clear Register (LCD_INTCLR)

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																					INTF	Reserved									
Access																						WO										

Bit	Name	Functional Description	Access
31:11	*Reserved*	-	-
10	INTF	Interrupt flag clear Write 0 to clear Interrupt flag, write 1 has no effect; read always returns 0.	WO
9:0	*Reserved*	-	-

27.5.5 Output Configuration Register 0 (LCD_POEN0)

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFFFFFFFF																															
Name	S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:0	Sx (x = 31-0)	SEGx output control bit ● 0b0: SEG output enable ● 0b1: SEG output is off, you can use other functions, such as IO, analog input and output	RW

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27.5.6 Output Configuration Register 1 (LCD_POEN1)

Offset	Bit Position																															
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x01FFFFFF																															
Name	Reserved							C3	C2	C1	C0	S51	S50	S49	S48	S47	S46	S45	S44	MUX	S43	S42	S41	S40	S39C4	S38C5	S37C6	S36C7	S35	S34	S33	S32
Access								RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:25	*Reserved*	-	-
24:21	Cx (x = 3-0)	COMx output control bit ● 0b0: COM output enable ● 0b1: COM output is off, you can use other functions, such as IO, analog input and output	RW
20:13	Sx (x = 51-44)	SEGx output control bit ● 0b0: SEG output enable ● 0b1: SEG output is off, you can use other functions, such as IO, analog input and output	RW
12	MUX	SEG32-SEG35 port function selection Parameter selection details (See table below)	RW
11:8	Sx (x = 43-40)	SEGx output control bit ● 0b0: SEG output enable ● 0b1: SEG output is off, you can use other functions, such as IO, analog input and output	RW
7	S39C4	SEG39/COM4 output control bit SEG/COM pin function selection is determined by CR0.DUTY ● 0b0: SEG/COM output enable ● 0b1: SEG/COM output is off, you can use other functions, such as IO, analog input and output	RW
6	S38C5	SEG38/COM5 output control bit SEG/COM pin function selection is determined by CR0.DUTY ● 0b0: SEG/COM output enable ● 0b1: SEG/COM output is off, you can use other functions, such as IO, analog input and output	RW
5	S37C6	SEG37/COM6 output control bit SEG/COM pin function selection is determined by CR0.DUTY ● 0b0: SEG/COM output enable ● 0b1: SEG/COM output is off, you can use other functions, such as IO, analog input and output	RW

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Bit	Name	Functional Description	Access
4	S36C7	SEG36/COM7 output control bit SEG/COM pin function selection is determined by CR0.DUTY ● 0b0: SEG/COM output enable ● 0b1: SEG/COM output is off, you can use other functions, such as IO, analog input and output	RW
3:0	Sx (x = 35-32)	SEGx output control bit ● 0b0: SEG output enable ● 0b1: SEG output is off, you can use other functions, such as IO, analog input and output	RW

VLCDy/SEGx PAD State Description						Register configuration				
Status		VLCDH/ SEG35	VLCD3/ SEG34	VLCD2/ SEG33	VLCD1/ SEG32	MUX	S <35:32>	BSEL		
When VLCDy/SEGx PAD selects GPIO and LCD disable (LCD_ON=0)		IO	IO	IO	IO	1	0b1111	-	-	-
VLCDy/SEGx PAD selects GPIO and LCD enable (LCD_ON=1), only the internal resistance working mode can be selected at this time	Small resistance (high current) mode	IO	IO	IO	IO	1	0b1111	1	1	0
	Medium resistance (medium current) mode	IO	IO	IO	IO	1	0b1111	0	1	0
	Large resistance (low current) mode	IO	IO	IO	IO	1	0b1111	1	0	0
Select the external resistor working mode, the internal resistor is disconnected		VOUT	VLCD3	VLCD2	VLCD1	0	0b0000	0	0	0
Select internal resistor operation mode	Small resistance (high current) mode	SEG35/IO	SEG34/IO	SEG33/IO	SEG32/IO	0	-	1	1	0
	Medium resistance (medium current) mode	SEG35/IO	SEG34/IO	SEG33/IO	SEG32/IO	0	-	0	1	0
	Large resistance (low current) mode	SEG35/IO	SEG34/IO	SEG33/IO	SEG32/IO	0	-	1	0	0
Select the external capacitor working mode, and the internal resistor is disconnected		DH1	DH2	VLCD2	VLCD1	0	0b0000	0	0	1

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27.5.7 LCD_RAMx (x=0-7)

Offset: 0x040 (LCDRAM0), 0x044 (LCDRAM1), 0x048 (LCDRAM2), 0x04C (LCDRAM3), 0x050 (LCDRAM4), 0x054 (LCDRAM5), 0x058 (LCDRAM6), 0x05C (LCDRAM7)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:0	Dn (n = 31-0)	LCD point output For specific display, refer to the description of LCD Display Mode. ● 0b0: Corresponding SEG-COM crossover point not lit ● 0b1: Corresponding SEG-COM crossover point lit	RW

27.5.8 LCD_RAMx (x=8-F)

Offset: 0x060 (LCDRAM8), 0x064 (LCDRAM9), 0x068 (LCDRAMA), 0x06C (LCDRAMB), 0x070 (LCDRAMC), 0x074 (LCDRAMD), 0x078 (LCDRAME), 0x07C (LCDRAMF)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	Reserved								D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access									RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:24	*Reserved*	-	-
23:0	Dn (n = 23-0)	LCD point output For specific display, refer to the description of LCD Display Mode. ● 0b0: Corresponding SEG-COM crossover point not lit ● 0b1: Corresponding SEG-COM crossover point lit	RW

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28 ADC

28.1 Introduction

External analog signals need to be converted into digital signals to be further processed by the MCU. This product integrates an 12-bit high-precision, high-speed successive approximation register (SAR ADC) module.

28.2 Features

- 12-bit conversion accuracy
- 1Msps conversion speed
- Up to 28 input channels are supported, including 25 external pin inputs, 1 internal temperature sensor voltage, 1 1/3 AVCC voltage, 1 DAC internal output
- 4 reference sources: AVCC voltage, EXVREF pins, internal 1.5V reference voltage, internal 2.5V reference voltage
- ADC voltage input range: 0-Vref
- Built-in signal follower, which can convert high-impedance signals
- Multiple conversion modes: single conversion, SQR scan continuous conversion, JQR scan conversion, continuous conversion accumulation
- Software can configure ADC conversion rate
- Support on-chip peripherals to automatically trigger ADC conversion, effectively reducing chip power consumption and improving real-time conversion
- Input channel voltage threshold monitoring

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28.3 Functional Description

28.3.1 ADC Block Diagram

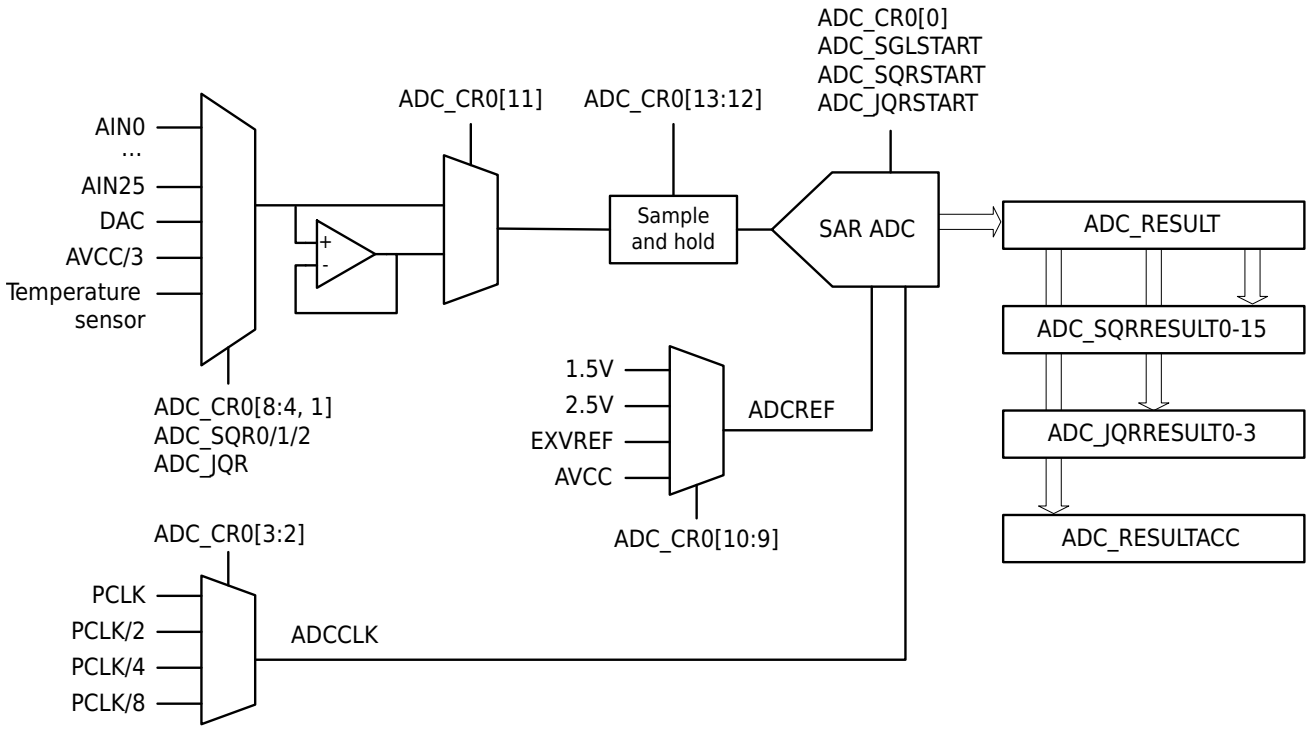

Figure 28-1 ADC Block Diagram

28.3.2 Conversion Timing and Conversion Speed

The ADC conversion timing is shown in the figure below: a complete ADC conversion consists of a sampling process and a successive comparison process. The sampling process requires 4-12 ADCCLK cycles, configured by ADC_CR0.SAM; the successive comparison process requires 16 ADCCLK cycles. Therefore, an ADC conversion requires a total of 20-28 ADCCLK cycles.

The ADC conversion speed is measured in sps (samples per second), indicating how many ADC conversions are performed per second. The ADC conversion speed is: the frequency of ADCCLK/the number of ADCCLKs required for one ADC conversion.

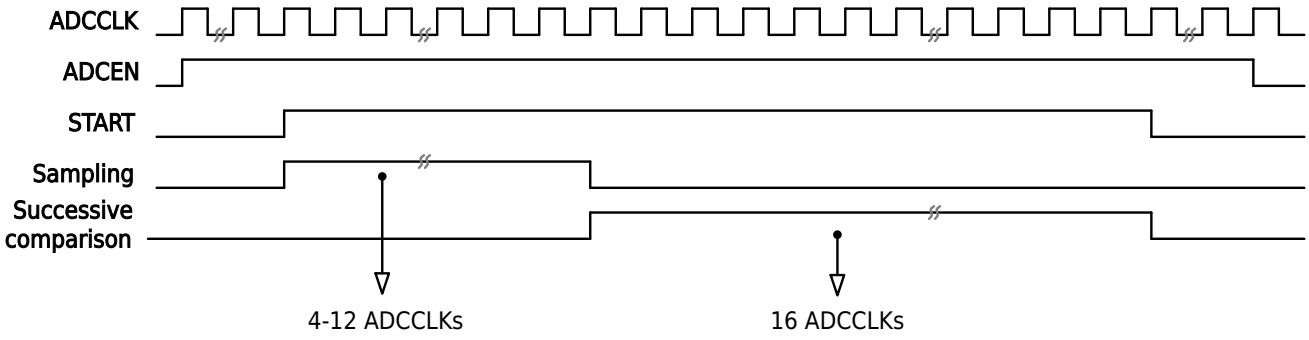

Figure 28-2 ADC Conversion Timing Diagram

The ADC conversion speed is related to the ADC reference voltage and AVCC voltage. The maximum conversion speed is shown in the following table:

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ADC Reference Voltage	AVCC Voltage	Maximum Conversion Speed	Maximum ADCCLK Frequency
Internal 1.5V	1.8-5.5V	200ksps	4MHz
Internal 2.5V	2.8-5.5V	200ksps	4MHz
AVCC/EXVREF	1.8-2.4V	200ksps	4.8MHz
AVCC/EXVREF	2.4-2.7V	500ksps	12MHz
AVCC/EXVREF	2.7-5.5V	1Msps	24MHz

28.3.3 Single Conversion Mode

In the single conversion mode, after ADC startup, only one sampling conversion is performed, which can convert all ADC channels. This mode can be started either by setting the ADC_SGLSTART.START bit for software trigger or by configuring an external trigger via ADC_EXTTRIGGER0. Once the ADC conversion of the selected channel is completed, ADC_IFR.SGLIF bit is automatically set to 1, and the conversion result is saved in the ADC_RESULT register.

If continuous conversion is required, set the ADC_ALLSTART.START bit to 1.

28.3.4 Scan Conversion Mode

Scan conversion mode is divided into two types: SQR scan conversion and JQR scan conversion. When operating independently, both modes can continuously perform multiple conversions on multiple channels. However, the two modes cannot be started simultaneously; when one mode is active, the other cannot be started.

SQR Scan Conversion Mode

SQR Scan conversion mode supports up to 16 consecutive conversions. The total number of conversions is configured by ADC_SQR2.CNT, and all channels can be configured for conversion through ADC_SQRx.CHxMUX. This mode can be started either by setting the ADC_SQRSTART.START bit or by configuring an external trigger via ADC_EXTTRIGGER0. After the conversion is started, the ADC module sequentially converts the channels configured in CHxMUX-CH0MUX until the total number of conversions is completed. After the ADC module completes the total number of conversions, the ADC_IFR.SQRIF bit will be automatically set to 1, and the conversion result will be saved in the ADC_SQRRESULTx-ADC_SQRRESULT0 register corresponding to the conversion channel. The following diagram illustrates the SQR scan conversion process for performing 8 conversions on AIN0, AIN1, and AIN5. In this configuration, SQR scan conversion channels 7/4/1 are set to AIN1, channels 6/3/0 are set to AIN0, and channels 5/2 are set to AIN5. ADC_SQRSTART.START is set to 1, the ADC module will sequentially perform conversions on SQR scan conversion channels 7 to 0.

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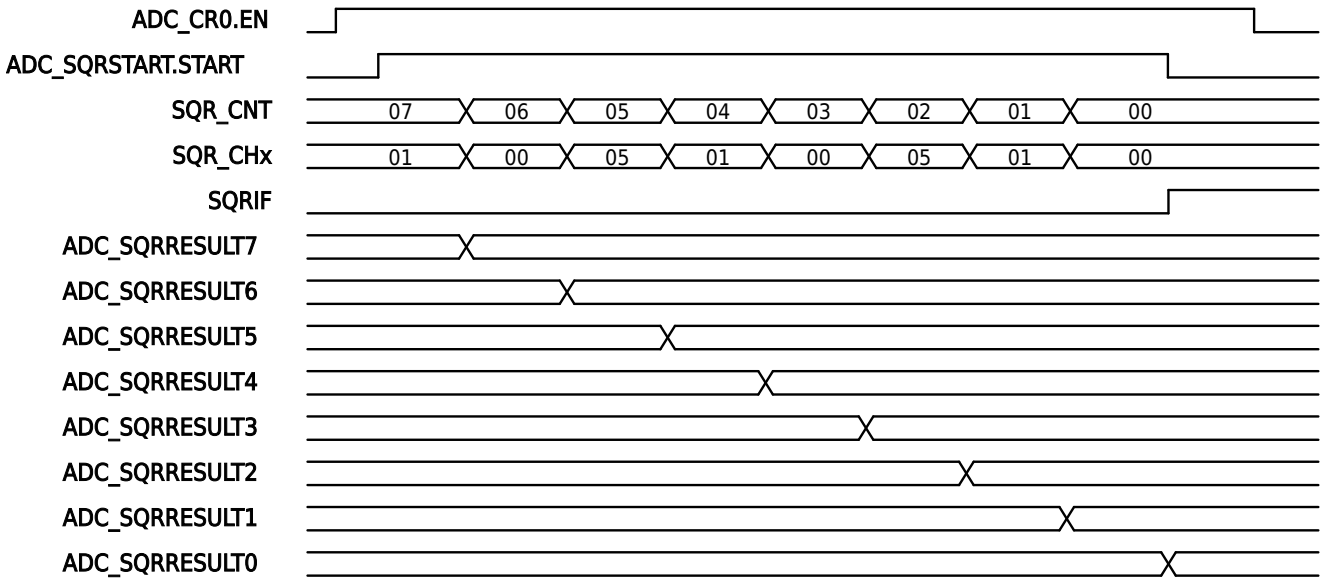

Figure 28-3 Examples of ADC SQR Scan Conversion Process

JQR Scan Conversion Mode

JQR scan conversion mode can perform up to 4 consecutive conversions, and the total number of conversions is configured by ADC_JQR.CNT; all channels can be configured for conversion, and the channel to be converted is configured by ADC_JQR.CHxMUX. This mode can be started either by setting the the ADC_JQRSTART.START bit or by configuring an external trigger via ADC_EXTTRIGGER1. After starting the conversion, the ADC module sequentially converts the channels configured from CHxMUX-CH0MUX, until the total number of conversions is completed. After the ADC module completes the total conversion count, the ADC_IFR.JQRIF bit is automatically set to 1, and the conversion results are stored in the corresponding ADC_JQRRESULTx-ADC_JQRRESULT0 registers. The figure below demonstrates the process of performing 4 conversions of AIN0, AIN1, and AIN5 in the JQR scan conversion process. JQR scan conversion channels 3, 2, 1, and 0 are configured as AIN5, AIN0, AIN1, and AIN5, respectively. After ADC_JQRSTART.START is set to 1, the ADC module will sequentially convert the JQR scanning conversion channels 3 to 0.

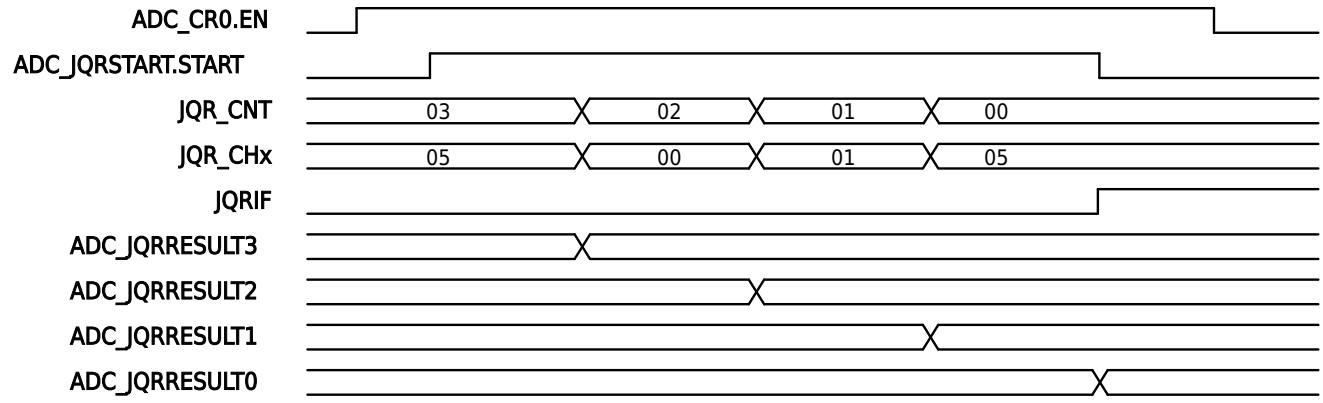

Figure 28-4 Examples of ADC JQR Scan Conversion Process

Note

JQR scan conversion cannot be started while SQR scan conversion is in progress; SQR scan conversion cannot be started while JQR scan conversion is in progress.

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Scan Conversion Triggers DMA Read

After SQR scan and JQR scan conversions are completed, DMA can be automatically triggered to read the conversion results. In SQR scan mode, enable the function by setting ADC_CR1.DMASQR to 1; in JQR scan mode, enable the function by setting ADC_CR1.DMAJQR to 1.

28.3.5 Continuous Conversion Accumulation Mode

In the continuous conversion and accumulation mode, starting the ADC once can perform multiple conversions on multiple channels and accumulate the results of each conversion; all channels can be configured to convert. The total number of ADC conversions is configured by ADC_SQR2.CNT; the channel to be converted is configured by ADC_SQRx.CHxMUX. This mode can be initiated either by setting the ADC_SQRSTART.START bit or by setting the external trigger of ADC_EXTTRIGGER0. After the continuous conversion is started, the ADC module sequentially converts the channels configured in CHxMUX-CH0MUX until the total number of conversions is completed. After the ADC module completes the total number of conversions, the ADC_IFR.SQRIF bit will be automatically set to 1, and the accumulated value of the conversion result will be saved in the ADC_RESULTACC register.

The figure below demonstrates the process of accumulating 10 consecutive conversions of AIN0, AIN1, and AIN5. SQR scan conversion channels 9/6/3/0 are configured as AIN0; channels 8/5/2 as AIN1; channels 7/4/1 as AIN5. After ADC_SQRSTART.START is set to 1, the ADC module will sequentially perform conversions according to the SQR scan channel configuration until the SQR_CNT count reaches 0. The ADC_RESULTACC register is automatically accumulated each time a conversion is completed. The conversion results of AIN0, AIN1, and AIN5 given in the figure are 0x010, 0x020, and 0x040 in turn.

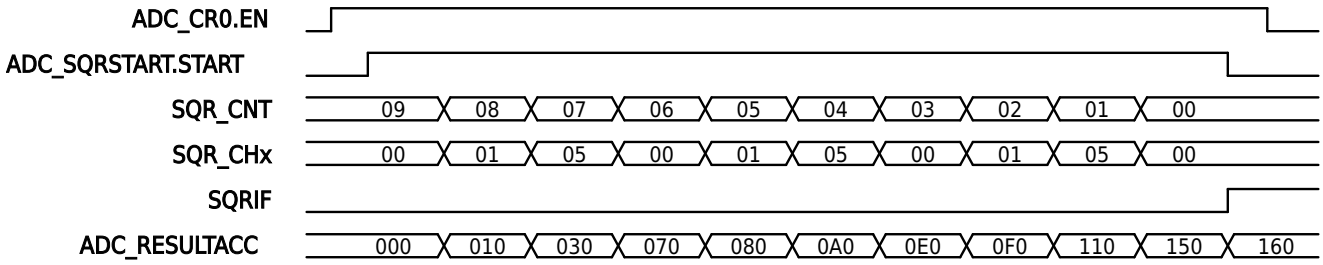

Figure 28-5 Examples of Continuous ADC Conversion Accumulation Process

28.3.6 ADC Conversion External Trigger Source

ADC conversions can be initiated either by software configuration or by an external trigger.

The ADC_EXTTRIGGER0 registers can be configured to set the external trigger source for single or SQR scan conversions.

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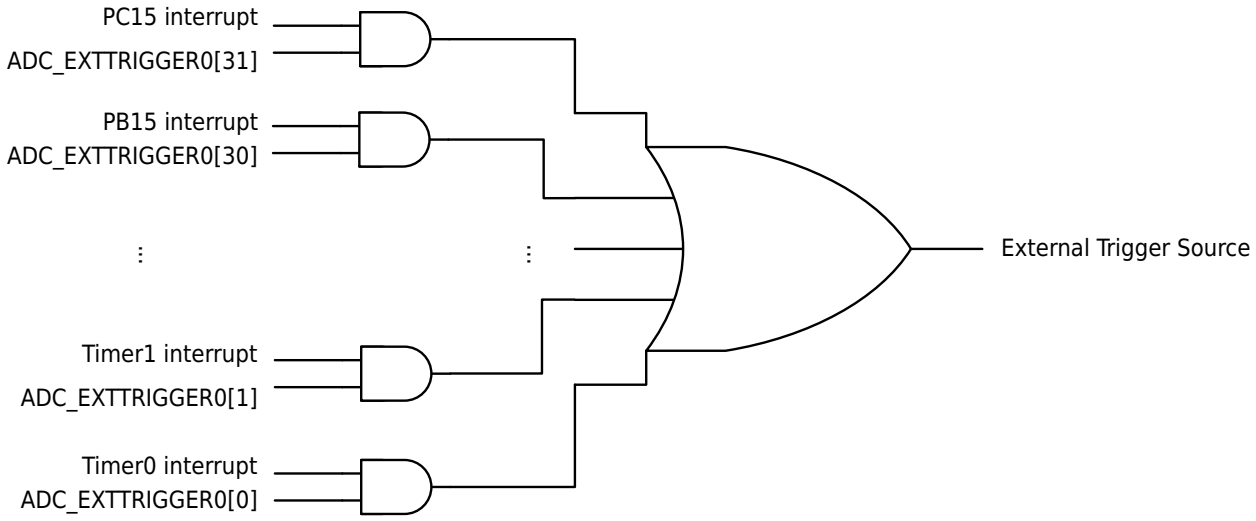

Figure 28-6 Diagram of External Trigger Sources for ADC Single and SQR Scan Conversions

The ADC_EXTTRIGGER1 register can be configured to set the external trigger source for ADC JQR scan conversions.

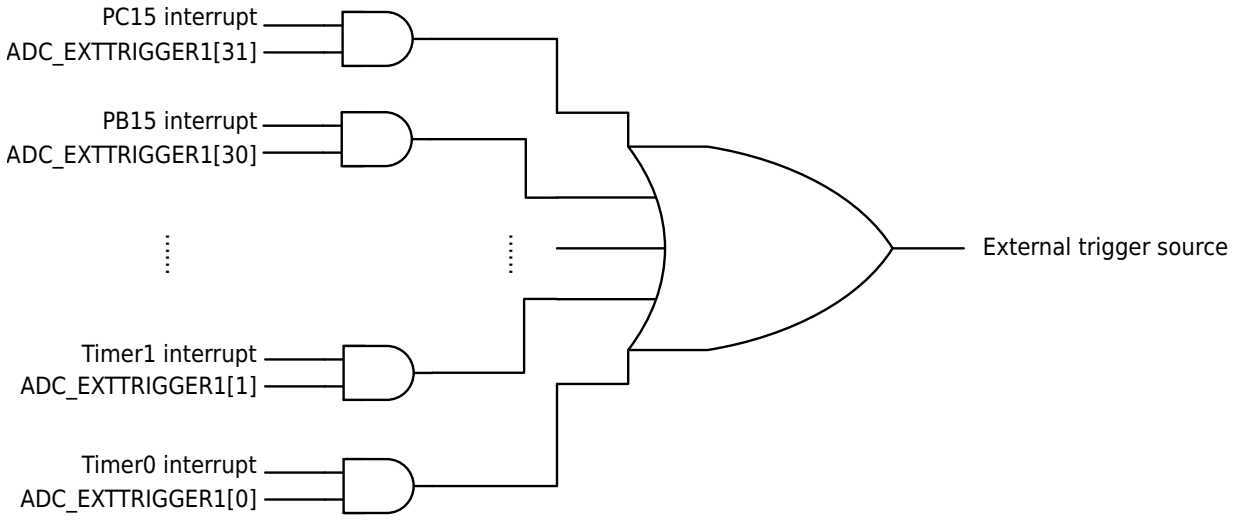

Figure 28-7 Diagram of External Trigger Sources for ADC JQR Scan Conversion

28.3.7 ADC Conversion Result Comparison

When the ADC conversion is completed, the ADC conversion result can be compared with the threshold set by the user, supporting high threshold comparison, low threshold comparison, and interval value comparison. This function requires setting the corresponding control bits ADC_CR1.HTCMP, ADC_CR1.LTCMP and ADC_CR1.REGCMP to 1. This function can realize the automatic monitoring of the analog quantity, until the ADC conversion result meets the user's expectations, an interrupt is generated to apply for user program interface entry. Monitoring channel selection is configured through ADC_CR1.THCH.

- High Threshold Comparison: When the ADC conversion result falls within the range [ADC_HT, 4095], the ADC_IFR.HTIF bit is set to 1; writing 0 to ADC_ICR.HTIC clears ADC_IFR.HTIF.
- Low Threshold Comparison: If the ADC conversion result falls within the range [0, ADC_LT), ADC_IFR.LTIF is set to 1; writing 0 to ADC_ICR.LTIC clears ADC_IFR.LTIF.

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- Interval Value Comparison: If the ADC conversion result falls within the range [ADC_LT, ADC_HT), ADC_IFR.REGIF is set to 1; writing 0 to ADC_ICR.REGIC clears ADC_IFR.REGIF.

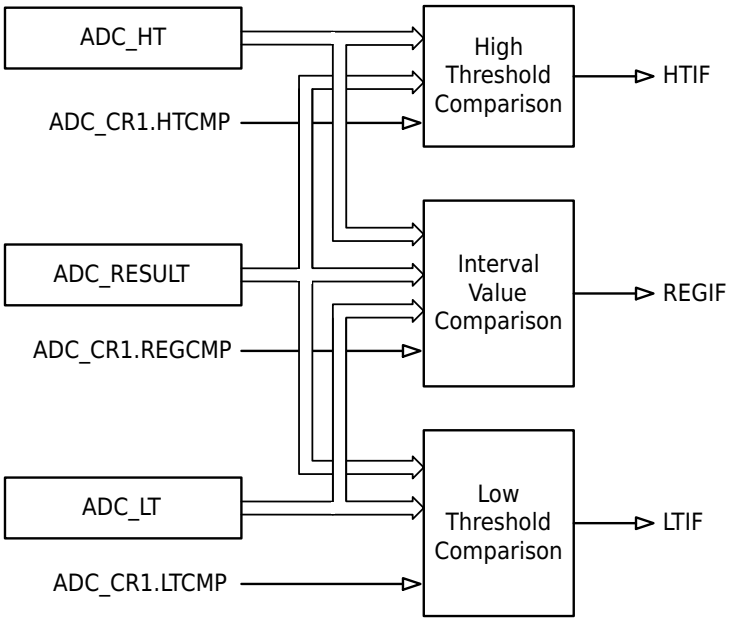

Figure 28-8 ADC Conversion Result Comparison Diagram

28.3.8 ADC Interrupt

The ADC interrupt request is shown in the table below:

Table 28-2 ADC Interrupt

Interrupt Source	Interrupt Flag	Interrupt Enable
ADC JQR scan conversion complete	ADC_IFR.JQRIF	ADC_CR0.IE
ADC SQR scan conversion complete	ADC_IFR.SQRIF	
ADC conversion result is within the range (greater than or equal to the low threshold and less than the high threshold)	ADC_IFR.REGIF	
ADC conversion result is within the high threshold region (greater than or equal to the high threshold)	ADC_IFR.HTIF	
ADC conversion result is within the low threshold region (less than the low threshold)	ADC_IFR.LTIF	
ADC single conversion completed	ADC_IFR.SGLIF	

28.3.9 Measure Ambient Temperature Using a Temperature Sensor

The output voltage of the temperature sensor will change with the change of the ambient temperature, so the corresponding ambient temperature can be calculated according to the output voltage of the temperature sensor. When the measurement channel of the ADC module selects the output voltage of the temperature sensor, the ambient temperature can be measured.

The calculation formula of ambient temperature T_A is as follows:

$$T_A(℃) = \frac{1}{16} * [T_N + \frac{T_H + T_L}{D_{H15} - D_{L15}} * (D_{ADC} - D_{N15})], \ldots\ldots\ldots (V_{ref} = 1.5\ V)$$

$$T_A(℃) = \frac{1}{16} * [T_N + \frac{T_H + T_L}{D_{H25} - D_{L25}} * (D_{ADC} - D_{N25})], \ldots\ldots\ldots (V_{ref} = 2.5\ V)$$

Where:

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- Vref is the reference voltage of the current ADC module, with typical values of 1.5V or 2.5V.
- D_{ADC} is the result of the ADC module measuring the output voltage of the temperature sensor, and the value is 0-4095.
- T_L, T_N, T_H are representative values of the ambient temperature recorded during the temperature test, and their values are 16 times the absolute value of the actual temperature value.
- D_{L15},D_{L25},D_{N15},D_{N25},D_{H15},D_{H25},T_L,T_N,T_H are calibration values obtained from temperature testing. These values need to be read from Flash memory during calculation. Their storage addresses and bit widths are detailed in the table below.

Table 28-3 Temperature Sensor Calibration Value Information List

Temperature	Calibration Value Name	Calibration Value Storage Address	Width
Low temperature	D_{L15}	0x00101634-0x00101635	12 bits
	D_{L25}	0x00101636-0x00101637	12 bits
	T_L	0x0010163A-0x0010163B	16 bits
Room temperature	D_{N15}	0x00101BBC-0x00101BBD	12 bits
	D_{N25}	0x00101BBE-0x00101BBF	12 bits
	T_N	0x00101BC0-0x00101BC1	16 bits
High temperature	D_{H15}	0x00101834-0x00101835	12 bits
	D_{H25}	0x00101836-0x00101837	12 bits
	T_H	0x0010183A-0x0010183B	16 bits

An Example Calculation is as Follows:

Condition 1: Vref=2.5V, T_L=640, T_N=400, T_H=1680, D_{L25}=1130, D_{N25}=1455, D_{H25}=1825, D_{ADC}=1250:

Temperature 1:

$$T_A(℃) = \frac{1}{16} * [T_N + \frac{T_H + T_L}{D_{H25} - D_{L25}} * (D_{ADC} - D_{N25})] = \frac{1}{16} * [400 + \frac{1680 + 640}{1825 - 1130} * (1250 - 1455)] = -17.8\ ℃$$

Condition 2: Vref=1.5V, T_L=640, T_N=400, T_H=1680, D_{L15}=1880, D_{N15}=2425, D_{H15}=3040, D_{ADC}=2800:

Temperature 2:

$$T_A(℃) = \frac{1}{16} * [T_N + \frac{T_H + T_L}{D_{H15} - D_{L15}} * (D_{ADC} - D_{N15})] = \frac{1}{16} * [400 + \frac{1680 + 640}{3040 - 1880} * (2800 - 2425)] = 71.9\ ℃$$

28.4 Operation Example

28.4.1 Start the ADC Single Conversion Operation Process through the ADC_SGLSTART.START Bit

Procedure

Step1. Configure the corresponding bits of PAADS-PEADS, and configure the ADC channel to be converted as an analog port.

Step2. Set PBADS[1] to 1 to configure the ADC external reference voltage pin as an analog port.

> **Note**
> If the ADC reference voltage does not select an external reference voltage pin, this step can be skipped.

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Step3. Set BGR_CR.BGR_EN to 1, to enable the BGR module.

Step4. Set ADC_CR0.EN to 1 to enable the ADC module.

Step5. Delay for the longer of $T_{ADCSTART}$ and $T_{stable(BGR)}$ (refer to the "Electrical CharacteristicsOperating ConditionsInternal Reference Voltage/ADC Characteristics" section in the "Datasheet" for specific values), and wait for the ADC and BGR module to complete startup.

Step6. Set ADC_CR1.MODE to 0 to select single conversion mode.

Step7. Configure ADC_CR0.REF and select the reference voltage of the ADC.

Step8. Set ADC_CR0.INREFEN to 1 to enable ADC internal reference voltage.

> **Note**
> If the ADC reference voltage does not select the internal reference voltage, this step can be skipped.

Step9. Configure ADC_CR0.SAM and ADC_CR0.CLKDIV to set the conversion speed of ADC.

Step10. Configure ADC_CR0.SGLMUX to select the channel to be converted.

Step11. Set ADC_ICR.SGLIC to 0, and clear ADC_IFR.SGLIF flag.

Step12. Set ADC_SGLSTART.START to 1 to start ADC single conversion. If continuous conversion is still needed, set ADC_ALLSTART.START to 1.

Step13. Wait for ADC_IFR.SGLIF to become 1, read the ADC_RESULT register to get the ADC conversion result.

Step14. To convert other channels, repeat steps10-13. If continuous conversion has been enabled, set ADC_ALLSTART.START to 0 to stop it before performing conversions on other channels, then repeat steps10-13.

Step15. Set ADC_CR0.EN and BGR_CR.BGR_EN to 0, turn off ADC module and BGR module.

28.4.2 ADC Single Conversion Operation Process through an External Trigger

Procedure

Step1. Configure the corresponding bits of PAADS-PEADS, and configure the ADC channel to be converted as an analog port.

Step2. Set PBADS[1] to 1 to configure the ADC external reference voltage pin as an analog port.

> **Note**
> If the ADC reference voltage does not select an external reference voltage pin, this step can be skipped.

Step3. Set BGR_CR.BGR_EN to 1, to enable the BGR module.

Step4. Set ADC_CR0.EN to 1 to enable the ADC module.

Step5. Delay for the longer of $T_{ADCSTART}$ and $T_{stable(BGR)}$ (refer to the "Electrical CharacteristicsOperating ConditionsInternal Reference Voltage/ADC Characteristics" section in the "Datasheet" for specific values), and wait for the ADC and BGR module to complete startup.

Step6. Set ADC_CR1.MODE to 0 to select single conversion mode.

Step7. Set ADC_CR0.IE to 1 to enable ADC interrupt.

Step8. Enable the ADC interrupt in the NVIC interrupt vector table.

Step9. Configure ADC_CR0.REF and select the reference voltage of the ADC.

Step10. Set ADC_CR0.INREFEN to 1 to enable ADC internal reference voltage.

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> **Note**
> If the ADC reference voltage does not select the internal reference voltage, this step can be skipped.

Step11. Configure ADC_CR0.SAM and ADC_CR0.CLKDIV to set the conversion speed of ADC.

Step12. Configure ADC_CR0.SGLMUX to select the channel to be converted.

Step13. Set ADC_ICR to 0x0, clear the ADC interrupt flag.

Step14. Configure ADC_EXTTRIGGER0 to select the external trigger condition.

Step15. When an external trigger condition triggers the ADC to complete the conversion, the ADC module will generate an interrupt. The user can read the ADC_RESULT register in the ADC interrupt service program to obtain the ADC conversion result.

Step16. To convert other channels, repeat steps12-15.

Step17. Set ADC_CR0.EN and BGR_CR.BGR_EN to 0, turn off ADC module and BGR module.

28.4.3 Start the ADC SQR Scan Conversion Operation Process through the ADC_SQRSTART.START Bit

Procedure

Step1. Configure the corresponding bits of PAADS-PEADS, and configure the ADC channel to be converted as an analog port.

Step2. Set PBADS[1] to 1 to configure the ADC external reference voltage pin as an analog port.

> **Note**
> If the ADC reference voltage does not select an external reference voltage pin, this step can be skipped.

Step3. Set BGR_CR.BGR_EN to 1, to enable the BGR module.

Step4. Set ADC_CR0.EN to 1 to enable the ADC module.

Step5. Delay for the longer of $T_{ADCSTART}$ and $T_{stable(BGR)}$ (refer to the "Electrical CharacteristicsOperating ConditionsInternal Reference Voltage/ADC Characteristics" section in the "Datasheet" for specific values), and wait for the ADC and BGR module to complete startup.

Step6. Set ADC_CR1.MODE to 1 to select scan conversion mode.

Step7. Configure ADC_CR0.REF and select the reference voltage of the ADC.

Step8. Set ADC_CR0.INREFEN to 1 to enable ADC internal reference voltage.

> **Note**
> If the ADC reference voltage does not select the internal reference voltage, this step can be skipped.

Step9. Configure ADC_CR0.SAM and ADC_CR0.CLKDIV to set the conversion speed of ADC.

Step10. Configure ADC_SQR0.CHxMUX or ADC_SQR1.CHxMUX or ADC_SQR2.CHxMUX, and select SQR scan conversion channels.

Step11. Configure ADC_SQR2.CNT, and select the total number of conversions for SQR scan conversions.
The total number of conversions needs to be consistent with the number of conversion channels configured in step10.

Step12. Set ADC_ICR.SQRIC to 0, clear ADC_IFR.SQRIF flag.

Step13. Set ADC_SQRSTART.START to 1 to start ADC SQR scan conversion.

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Step14. Wait for ADC_IFR.SQRIF to become 1, read ADC_SQRRESULTx-ADC_SQRRESULT0 registers to obtain the conversion result of the corresponding channel.

Step15. To convert other channels, repeat steps10-14.

Step16. Set ADC_CR0.EN and BGR_CR.BGR_EN to 0, turn off ADC module and BGR module.

28.4.4 External Trigger Start ADC SQR Scan Conversion Operation Flow

Procedure

Step1. Configure the corresponding bits of PAADS-PEADS, and configure the ADC channel to be converted as an analog port.

Step2. Set PBADS[1] to 1 to configure the ADC external reference voltage pin as an analog port.

> **Note**
> If the ADC reference voltage does not select an external reference voltage pin, this step can be skipped.

Step3. Set BGR_CR.BGR_EN to 1, to enable the BGR module.

Step4. Set ADC_CR0.EN to 1 to enable the ADC module.

Step5. Delay for the longer of $T_{ADCSTART}$ and $T_{stable(BGR)}$ (refer to the "Electrical CharacteristicsOperating ConditionsInternal Reference Voltage/ADC Characteristics" section in the "Datasheet" for specific values), and wait for the ADC and BGR module to complete startup.

Step6. Set ADC_CR1.MODE to 1 to select scan conversion mode.

Step7. Set ADC_CR0.IE to 1 to enable ADC interrupt.

Step8. Enable the ADC interrupt in the NVIC interrupt vector table.

Step9. Configure ADC_CR0.REF and select the reference voltage of the ADC.

Step10. Set ADC_CR0.INREFEN to 1 to enable ADC internal reference voltage.

> **Note**
> If the ADC reference voltage does not select the internal reference voltage, this step can be skipped.

Step11. Configure ADC_CR0.SAM and ADC_CR0.CLKDIV to set the conversion speed of ADC.

Step12. Configure ADC_SQR0.CHxMUX or ADC_SQR1.CHxMUX or ADC_SQR2.CHxMUX, and select SQR scan conversion channels.

Step13. Configure ADC_SQR2.CNT, and select the total number of conversions for SQR scan conversions.
The total number of conversions needs to be consistent with the number of conversion channels configured in step12.

Step14. Set ADC_ICR to 0x0, clear the ADC interrupt flag.

Step15. Configure ADC_EXTTRIGGER0 to select the external trigger condition.

Step16. When an external trigger condition triggers the ADC to complete the conversion, the ADC module will generate an interrupt. Users can read ADC_SQRRESULTx-ADC_SQRRESULT0 registers in the ADC interrupt service routine to get the conversion result of the corresponding channel.

Step17. To convert other channels, repeat steps12-16.

Step18. Set ADC_CR0.EN and BGR_CR.BGR_EN to 0, turn off ADC module and BGR module.

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28.4.5 Start ADC JQR Scan Conversion Operation Flow via ADC_JQRSTART.START Bit

Procedure

Step1. Configure the corresponding bits of PAADS-PEADS, and configure the ADC channel to be converted as an analog port.

Step2. Set PBADS[1] to 1 to configure the ADC external reference voltage pin as an analog port.

> **Note**
> If the ADC reference voltage does not select an external reference voltage pin, this step can be skipped.

Step3. Set BGR_CR.BGR_EN to 1, to enable the BGR module.

Step4. Set ADC_CR0.EN to 1 to enable the ADC module.

Step5. Delay for the longer of $T_{ADCSTART}$ and $T_{stable(BGR)}$ (refer to the "Electrical CharacteristicsOperating ConditionsInternal Reference Voltage/ADC Characteristics" section in the "Datasheet" for specific values), and wait for the ADC and BGR module to complete startup.

Step6. Set ADC_CR1.MODE to 1 to select scan conversion mode.

Step7. Configure ADC_CR0.REF and select the reference voltage of the ADC.

Step8. Set ADC_CR0.INREFEN to 1 to enable ADC internal reference voltage.

> **Note**
> If the ADC reference voltage does not select the internal reference voltage, this step can be skipped.

Step9. Configure ADC_CR0.SAM and ADC_CR0.CLKDIV to set the conversion speed of ADC.

Step10. Configure ADC_JQR.CHxMUX and select the JQR scan conversion channel.

Step11. Configure ADC_JQR.CNT to select the total number of conversions for the JQR scan conversion. The total number of conversions needs to be consistent with the number of conversion channels configured in step10.

Step12. Set ADC_ICR.JQRIC to 0, clear ADC_IFR.JQRIF flag.

Step13. Set ADC_JQRSTART.START to 1 to start ADC JQR scan conversion.

Step14. Wait for ADC_IFR.JQRIF to become 1, read ADC_JQRRESULTx-ADC_JQRRESULT0 registers to obtain the conversion result of the corresponding channel.

Step15. To convert other channels, repeat steps10-14.

Step16. Set ADC_CR0.EN and BGR_CR.BGR_EN to 0, turn off ADC module and BGR module.

28.4.6 External Trigger Start ADC JQR Scan Conversion Operation Flow

Procedure

Step1. Configure the corresponding bits of PAADS-PEADS, and configure the ADC channel to be converted as an analog port.

Step2. Set PBADS[1] to 1 to configure the ADC external reference voltage pin as an analog port.

> **Note**
> If the ADC reference voltage does not select an external reference voltage pin, this step can be skipped.

Step3. Set BGR_CR.BGR_EN to 1, to enable the BGR module.

Step4. Set ADC_CR0.EN to 1 to enable the ADC module.

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Step5. Delay for the longer of $T_{ADCSTART}$ and $T_{stable(BGR)}$ (refer to the "Electrical CharacteristicsOperating ConditionsInternal Reference Voltage/ADC Characteristics" section in the "Datasheet" for specific values), and wait for the ADC and BGR module to complete startup.

Step6. Set ADC_CR1.MODE to 1 to select scan conversion mode.

Step7. Set ADC_CR0.IE to 1 to enable ADC interrupt.

Step8. Enable the ADC interrupt in the NVIC interrupt vector table.

Step9. Configure ADC_CR0.REF and select the reference voltage of the ADC.

Step10. Set ADC_CR0.INREFEN to 1 to enable ADC internal reference voltage.

> **Note**
> If the ADC reference voltage does not select the internal reference voltage, this step can be skipped.

Step11. Configure ADC_CR0.SAM and ADC_CR0.CLKDIV to set the conversion speed of ADC.

Step12. Configure ADC_JQR.CHxMUX and select the JQR scan conversion channel.

Step13. Configure ADC_JQR.CNT to select the total number of conversions for the JQR scan conversion. The total number of conversions needs to be consistent with the number of conversion channels configured in step12.

Step14. Set ADC_ICR to 0x0, clear the ADC interrupt flag.

Step15. Configure ADC_EXTTRIGGER1 to select the external trigger condition.

Step16. When an external trigger condition triggers the ADC to complete the conversion, the ADC module will generate an interrupt. Users can read the ADC_JQRRESULTx-ADC_JQRRESULT0 registers in the ADC interrupt service routine to obtain the conversion results of the corresponding channels.

Step17. To convert other channels, repeat steps12-16.

Step18. Set ADC_CR0.EN and BGR_CR.BGR_EN to 0, turn off ADC module and BGR module.

28.4.7 Start the ADC Continuous Conversion Accumulation Operation Process through the ADC_SQRSTART.START Bit

Procedure

Step1. Configure the corresponding bits of PAADS-PEADS, and configure the ADC channel to be converted as an analog port.

Step2. Set PBADS[1] to 1 to configure the ADC external reference voltage pin as an analog port.

> **Note**
> If the ADC reference voltage does not select an external reference voltage pin, this step can be skipped.

Step3. Set BGR_CR.BGR_EN to 1, to enable the BGR module.

Step4. Set ADC_CR0.EN to 1 to enable the ADC module.

Step5. Delay for the longer of $T_{ADCSTART}$ and $T_{stable(BGR)}$ (refer to the "Electrical CharacteristicsOperating ConditionsInternal Reference Voltage/ADC Characteristics" section in the "Datasheet" for specific values), and wait for the ADC and BGR module to complete startup.

Step6. Set ADC_CR1.MODE to 1 to select scan conversion mode.

Step7. Set ADC_CR1.RACCEN to 1 to enable the automatic accumulation function of ADC conversion.

Step8. Configure ADC_CR0.REF and select the reference voltage of the ADC.

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Step9. Set ADC_CR0.INREFEN to 1 to enable ADC internal reference voltage.

> **Note**
> If the ADC reference voltage does not select the internal reference voltage, this step can be skipped.

Step10. Configure ADC_CR0.SAM and ADC_CR0.CLKDIV to set the conversion speed of ADC.

Step11. Configure ADC_SQR0.CHxMUX or ADC_SQR1.CHxMUX or ADC_SQR2.CHxMUX, and select SQR scan conversion channels.

Step12. Configure ADC_SQR2.CNT, and select the total number of conversions for SQR scan conversions.
The total number of conversions needs to be consistent with the number of conversion channels configured in step11.

Step13. Set ADC_ICR.SQRIC to 0, clear ADC_IFR.SQRIF flag.

Step14. Set ADC_CR1.RACCCLR to 0 and clear the ADC_RESULTACC register.

Step15. Set ADC_SQRSTART.START to 1 to start ADC SQR scan conversion.

Step16. Wait for ADC_IFR.SQRIF to become 1, read ADC_RESULTACC registers to obtain accumulated value of the conversion result.

Step17. To convert other channels, repeat steps11-16.

Step18. Set ADC_CR0.EN and BGR_CR.BGR_EN to 0, turn off ADC module and BGR module.

28.4.8 Start ADC Continuous Conversion Accumulation Operation Process through External Trigger

Procedure

Step1. Configure the corresponding bits of PAADS-PEADS, and configure the ADC channel to be converted as an analog port.

Step2. Set PBADS[1] to 1 to configure the ADC external reference voltage pin as an analog port.

> **Note**
> If the ADC reference voltage does not select an external reference voltage pin, this step can be skipped.

Step3. Set BGR_CR.BGR_EN to 1, to enable the BGR module.

Step4. Set ADC_CR0.EN to 1 to enable the ADC module.

Step5. Delay for the longer of $T_{ADCSTART}$ and $T_{stable(BGR)}$ (refer to the "Electrical CharacteristicsOperating ConditionsInternal Reference Voltage/ADC Characteristics" section in the "Datasheet" for specific values), and wait for the ADC and BGR module to complete startup.

Step6. Set ADC_CR1.MODE to 1 to select scan conversion mode.

Step7. Set ADC_CR0.IE to 1 to enable ADC interrupt.

Step8. Enable the ADC interrupt in the NVIC interrupt vector table.

Step9. Set ADC_CR1.RACCEN to 1 to enable the automatic accumulation function of ADC conversion.

Step10. Configure ADC_CR0.REF and select the reference voltage of the ADC.

Step11. Set ADC_CR0.INREFEN to 1 to enable ADC internal reference voltage.

> **Note**
> If the ADC reference voltage does not select the internal reference voltage, this step can be skipped.

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Step12. Configure ADC_CR0.SAM and ADC_CR0.CLKDIV to set the conversion speed of ADC.

Step13. Configure ADC_SQR0.CHxMUX or ADC_SQR1.CHxMUX or ADC_SQR2.CHxMUX, and select SQR scan conversion channels.

Step14. Configure ADC_SQR2.CNT, and select the total number of conversions for SQR scan conversions.
The total number of conversions needs to be consistent with the number of conversion channels configured in step13.

Step15. Set ADC_ICR to 0x0, clear the ADC interrupt flag.

Step16. Set ADC_CR1.RACCCLR to 0 and clear the ADC_RESULTACC register.

Step17. Configure ADC_EXTTRIGGER0 to select the external trigger condition.

Step18. When an external trigger condition triggers the ADC to complete the conversion, the ADC module will generate an interrupt. The user can read the ADC_RESULTACC register in the ADC interrupt service routine to obtain the accumulated value of the conversion result.

Step19. To convert other channels, repeat steps13-18.

Step20. Set ADC_CR0.EN and BGR_CR.BGR_EN to 0, turn off ADC module and BGR module.

28.4.9 Operation Process of Measuring Ambient Temperature through ADC

Procedure

Step1. Set BGR_CR to 3, enable BGR module and temperature sensor module.

Step2. Set ADC_CR0.EN to 1 to enable the ADC module.

Step3. Delay for the longer of $T_{ADCSTART}$ and $T_{stable(BGR)}$ (refer to the "Electrical CharacteristicsOperating ConditionsInternal Reference Voltage/ADC Characteristics" section in the "Datasheet" for specific values), and wait for the ADC and BGR module to complete startup.

Step4. Set ADC_CR1.MODE to 0 to select single conversion mode.

Step5. Set ADC_CR0.INREFEN to 1 to enable ADC internal reference voltage.

Step6. Configure ADC_CR0.REF, select the reference voltage of ADC as internal 1.5V or internal 2.5V.

Step7. Configure ADC_CR0.SAM and ADC_CR0.CLKDIV to set the conversion speed of ADC.

Step8. Set ADC_CR0.SGLMUX to 0x1C, select the channel to be converted as the output of the temperature sensor.

Step9. Set ADC_CR0.BUF to 1 to enable the input signal amplifier.

Step10. Set ADC_ICR.SGLIC to 0, and clear ADC_IFR.SGLIF flag.

Step11. Set ADC_SGLSTART.START to 1 to start ADC single conversion.

Step12. Wait for ADC_IFR.SGLIF to become 1, read ADC_RESULT registers to obtain accumulated value of the conversion result.

Step13. Set ADC_CR0.EN and BGR_CR to 0, turn off the ADC module, BGR module, and temperature sensor module.

Step14. Read the calibration value of the temperature sensor and calculate the current ambient temperature according to the formula.

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28.5 Register Description

28.5.1 Register List

Base address: 0x40002400

Table 28-4 Analog-to-Digital Converter (ADC) Register Offset

Offset	Register	Description	Width
0x004	ADC_CR0	ADC Basic Configuration Register 0	32
0x008	ADC_CR1	ADC Basic Configuration Register 1	32
0x040	ADC_SQR0	ADC SQR Scan Conversion Channel Configuration Register 0	32
0x044	ADC_SQR1	ADC SQR Scan Conversion Channel Configuration Register 1	32
0x048	ADC_SQR2	ADC SQR Scan Conversion Channel Configuration Register 2	32
0x04C	ADC_JQR	ADC JQR Scan Conversion Channel Configuration Register	32
0x050	ADC_SQRRESULT0	ADC SQR Scan Conversion Channel Configuration Register 0	32
0x054	ADC_SQRRESULT1	ADC SQR Scan Conversion Channel Configuration Register 1	32
0x058	ADC_SQRRESULT2	ADC SQR Scan Conversion Channel Configuration Register 2	32
0x05C	ADC_SQRRESULT3	ADC SQR Scan Conversion Channel Configuration Register 3	32
0x060	ADC_SQRRESULT4	ADC SQR Scan Conversion Channel Configuration Register 4	32
0x064	ADC_SQRRESULT5	ADC SQR Scan Conversion Channel Configuration Register 5	32
0x068	ADC_SQRRESULT6	ADC SQR Scan Conversion Channel Configuration Register 6	32
0x06C	ADC_SQRRESULT7	ADC SQR Scan Conversion Channel Configuration Register 7	32
0x070	ADC_SQRRESULT8	ADC SQR Scan Conversion Channel Configuration Register 8	32
0x074	ADC_SQRRESULT9	ADC SQR Scan Conversion Channel Configuration Register 9	32
0x078	ADC_SQRRESULT10	ADC SQR Scan Conversion Channel Configuration Register 10	32

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Offset	Register	Description	Width
0x07C	ADC_SQRRESULT11	ADC SQR Scan Conversion Channel Configuration Register 11	32
0x080	ADC_SQRRESULT12	ADC SQR Scan Conversion Channel Configuration Register 12	32
0x084	ADC_SQRRESULT13	ADC SQR Scan Conversion Channel Configuration Register 13	32
0x088	ADC_SQRRESULT14	ADC SQR Scan Conversion Channel Configuration Register 14	32
0x08C	ADC_SQRRESULT15	ADC SQR Scan Conversion Channel Configuration Register 15	32
0x090	ADC_JQRRESULT0	ADC JQR Scan Conversion Channel Configuration Register 0	32
0x094	ADC_JQRRESULT1	ADC JQR Scan Conversion Channel Configuration Register 1	32
0x098	ADC_JQRRESULT2	ADC JQR Scan Conversion Channel Configuration Register 2	32
0x09C	ADC_JQRRESULT3	ADC JQR Scan Conversion Channel Configuration Register 3	32
0x0A0	ADC_RESULT	ADC Conversion Results Register	32
0x0A4	ADC_RESULTACC	Accumulated Value of ADC Conversion Result Register	32
0x0A8	ADC_HT	ADC Comparison High Threshold Register	32
0x0AC	ADC_LT	ADC Comparison Low Threshold Register	32
0x0B0	ADC_IFR	ADC Interrupt Flag Register	32
0x0B4	ADC_ICR	ADC Interrupt Clear Register	32
0x0B8	ADC_EXTTRIGGER0	ADC External Interrupt Trigger Source Configuration Register for Single or SQRScan Conversion	32
0x0BC	ADC_EXTTRIGGER1	ADC JQR Scan Conversion External Interrupt Trigger Source Configuration Register	32
0x0C0	ADC_SGLSTART	ADC Single Conversion Start Control Register	32
0x0C4	ADC_SQRSTART	ADC SQR Scan Conversion Start Control Register	32
0x0C8	ADC_JQRSTART	ADC JQR Scan Conversion Start Control Register	32
0x0CC	ADC_ALLSTART	ADC Continuous Conversion Start/Stop Control Register	32

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28.5.2 ADC Basic Configuration Register 0 (ADC_CR0)

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x000067F0																															
Name	Reserved																IE	INREFEN	SAM		BUF	REF	SGLMUX				CLKDIV			Reserved	EN
Access																	RW	RW	RW		RW	RW	RW				RW				RW

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15	IE	ADC interrupt control ● 0b0: Disable ● 0b1: Enable	RW
14	INREFEN	ADC internal reference voltage enable ● 0b0: Disable ● 0b1: Enable **Notice** This bit must be set to 1 when using the internal 1.5V/2.5V as the ADC reference voltage.	RW
13:12	SAM	ADC sampling period selection ● 0b00: 4 ADCCLK cycles ● 0b01: 6 ADCCLK cycles ● 0b10: 8 ADCCLK cycles ● 0b11: 12 ADCCLK cycles **Note** The successive comparison process alone requires 16 ADCCLK cycles.	RW
11	BUF	Built-in follower enable control ● 0b0: Disable the follower, and the external input signal is directly connected to the ADC ● 0b1: Turn on the follower, and the external input signal is connected to the ADC after passing through the follower to measure high-impedance signals **Note** When this function is enabled, the maximum rate is 200ksps. The following conditions must enable this function: ● The output impedance of the signal to be converted is high ● The signals to be converted are: AVCC/3, internal temperature sensor output voltage, DAC output.	RW

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Bit	Name	Functional Description	Access
10:9	REF	ADC reference voltage selection ● 0b00: Internal 1.5V ● 0b01: Internal 2.5V (power supply voltage must exceed 2.8V) ● 0b10: External reference voltage EXVREF (PB01) ● 0b11: AVCC voltage	RW
8:4	SGLMUX	Single conversion mode conversion channel selection ● 0b00000: AIN0 (PA00) ● 0b00001: AIN1 (PA01) ● 0b00010: AIN2 (PA02) ● 0b00011: AIN3 (PA03) ● 0b00100: AIN4 (PA04) ● 0b00101: AIN5 (PA05) ● 0b00110: AIN6 (PA06) ● 0b00111: AIN7 (PA07) ● 0b01000: AIN8 (PB00) ● 0b01001: AIN9 (PB01) ● 0b01010: AIN10 (PC00) ● 0b01011: AIN11 (PC01) ● 0b01100: AIN12 (PC02) ● 0b01101: AIN13 (PC03) ● 0b01110: AIN14 (PC04) ● 0b01111: AIN15 (PC05) ● 0b10000: AIN16 (PB02) ● 0b10001: AIN17 (PB10) ● 0b10010: AIN18 (PB11) ● 0b10011: AIN19 (PB12) ● 0b10100: AIN20 (PB13) ● 0b10101: AIN21 (PB14) ● 0b10110: AIN22 (PB15) ● 0b10111: Setting prohibited ● 0b11000: AIN24 (PE14) ● 0b11001: AIN25 (PE13) ● 0b11010: DAC output ● 0b11011: AVCC/3 ● 0b11100: Internal temperature sensor output voltage ● 0b11101: Setting prohibited **Note** When set to 0b11010-0b11100, ADC_CR0.BUF must be 1.	RW
3:2	CLKDIV	ADC clock selection ● 0b00: PCLK clock ● 0b01: PCLK clock divided by 2 ● 0b10: PCLK clock divided by 4 ● 0b11: PCLK clock divided by 8	RW
1	*Reserved*	-	-

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Bit	Name	Functional Description	Access
0	EN	ADC enable control ● 0b0: Disable ● 0b1: Enable	RW

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28.5.3 ADC Basic Configuration Register 1 (ADC_CR1)

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00008000																															
Name	Reserved																RACCCLR	REGCMP	HTCMP	LTCMP	RACCEN	MODE	DMAJQR	DMASQR	THCH				ALIGN	Reserved		
Access																	WO	RW	RW	RW	RW	RW	RW	RW	RW				RW			

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15	RACCCLR	ADC conversion result accumulation register is cleared Write 0 to clear the ADC_RESULTACC register, write 1 has no effect; read always returns 1.	WO
14	REGCMP	ADC interval comparison control ● 0b0: Disable ● 0b1: Enable	RW
13	HTCMP	ADC high threshold compare control ● 0b0: Disable ● 0b1: Enable	RW
12	LTCMP	ADC low threshold compare control ● 0b0: Disable ● 0b1: Enable	RW
11	RACCEN	ADC conversion result automatic accumulation control ● 0b0: Disable ● 0b1: Enable	RW
10	MODE	ADC conversion mode selection ● 0b0: Single conversion mode ● 0b1: Scan conversion mode	RW
9	DMAJQR	JQR scan trigger DMA read control ● 0b0: Disable ● 0b1: Enable	RW
8	DMASQR	SQR scan trigger DMA read control ● 0b0: Disable ● 0b1: Enable	RW
7:3	THCH	Threshold comparison channel selection For more information, see ADC_CR0.SGLMUX	RW
2	ALIGN	Conversion result alignment control ● 0b0: Conversion result stored as 16-bit right-aligned ● 0b1: Conversion result stored as 16-bit left-aligned	RW

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Bit	Name	Functional Description	Access
1:0	*Reserved*	-	-

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28.5.4 ADC SQR Scan Conversion Channel Configuration Register 0 (ADC_SQR0)

Offset	Bit Position																													
0x040	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved	CH5MUX						CH4MUX					CH3MUX					CH2MUX					CH1MUX					CH0MUX			
Access		RW						RW					RW					RW					RW					RW			

Bit	Name	Functional Description	Access
31:30	*Reserved*	-	-
29:25	CH5MUX	SQR scan conversion channel 5 selection For more information, see ADC_CR0.SGLMUX	RW
24:20	CH4MUX	SQR scan conversion channel 4 selection For more information, see ADC_CR0.SGLMUX	RW
19:15	CH3MUX	SQR scan conversion channel 3 selection For more information, see ADC_CR0.SGLMUX	RW
14:10	CH2MUX	SQR scan conversion channel 2 selection For more information, see ADC_CR0.SGLMUX	RW
9:5	CH1MUX	SQR scan conversion channel 1 selection For more information, see ADC_CR0.SGLMUX	RW
4:0	CH0MUX	SQR scan conversion channel 0 selection For more information, see ADC_CR0.SGLMUX	RW

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28.5.5 ADC SQR Scan Conversion Channel Configuration Register 1 (ADC_SQR1)

Offset	Bit Position																													
0x044	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved	CH11MUX						CH10MUX					CH9MUX					CH8MUX					CH7MUX					CH6MUX			
Access		RW						RW					RW					RW					RW					RW			

Bit	Name	Functional Description	Access
31:30	*Reserved*	-	-
29:25	CH11MUX	SQR scan conversion channel 11 selection For more information, see ADC_CR0.SGLMUX	RW
24:20	CH10MUX	SQR scan conversion channel 10 selection For more information, see ADC_CR0.SGLMUX	RW
19:15	CH9MUX	SQR scan conversion channel 9 selection For more information, see ADC_CR0.SGLMUX	RW
14:10	CH8MUX	SQR scan conversion channel 8 selection For more information, see ADC_CR0.SGLMUX	RW
9:5	CH7MUX	SQR scan conversion channel 7 selection For more information, see ADC_CR0.SGLMUX	RW
4:0	CH6MUX	SQR scan conversion channel 6 selection For more information, see ADC_CR0.SGLMUX	RW

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28.5.6 ADC SQR Scan Conversion Channel Configuration Register 2 (ADC_SQR2)

Offset	Bit Position																													
0x048	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved								CNT				CH15MUX					CH14MUX					CH13MUX					CH12MUX			
Access									RW				RW					RW					RW					RW			

Bit	Name	Functional Description	Access
31:24	*Reserved*	-	-
23:20	CNT	Number of SQR scan conversions The actual number of conversions is CNT + 1. Channels selected by CHxMUX-CH0MUX are scanned by SQR in sequence (where x=CNT).	RW
19:15	CH15MUX	SQR scan conversion channel 15 selection For more information, see ADC_CR0.SGLMUX	RW
14:10	CH14MUX	SQR scan conversion channel 14 selection For more information, see ADC_CR0.SGLMUX	RW
9:5	CH13MUX	SQR scan conversion channel 13 selection For more information, see ADC_CR0.SGLMUX	RW
4:0	CH12MUX	SQR Scan conversion channel 12 selection For more information, see ADC_CR0.SGLMUX	RW

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28.5.7 ADC JQR Scan Conversion Channel Configuration Register (ADC_JQR)

Offset	Bit Position																													
0x04C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved										CNT		CH3MUX					CH2MUX					CH1MUX					CH0MUX			
Access											RW		RW					RW					RW					RW			

Bit	Name	Functional Description	Access
31:22	*Reserved*	-	-
21:20	CNT	Number of JQR scan conversions The actual number of conversions is CNT + 1. Channels selected by CHxMUX-CH0MUX (x=CNT) are scanned by JQR in sequence.	RW
19:15	CH3MUX	JQR scan conversion channel 3 selection For more information, see ADC_CR0.SGLMUX	RW
14:10	CH2MUX	JQR scan conversion channel 2 selection For more information, see ADC_CR0.SGLMUX	RW
9:5	CH1MUX	JQR scan conversion channel 1 selection For more information, see ADC_CR0.SGLMUX	RW
4:0	CH0MUX	JQR scan conversion channel 0 selection For more information, see ADC_CR0.SGLMUX	RW

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28.5.8 ADC SQR Scan Conversion Channel x Result Register (ADC_SQRRESULTx) (x=0-15)

Offset: 0x050 (SQRRESULT0), 0x054 (SQRRESULT1), 0x058 (SQRRESULT2), 0x05C (SQRRESULT3), 0x060 (SQRRESULT4), 0x064 (SQRRESULT5), 0x068 (SQRRESULT6), 0x06C (SQRRESULT7), 0x070 (SQRRESULT8), 0x074 (SQRRESULT9), 0x078 (SQRRESULT10), 0x07C (SQRRESULT11), 0x080 (SQRRESULT12), 0x084 (SQRRESULT13), 0x088 (SQRRESULT14), 0x08C (SQRRESULT15)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																				RESULT											
Access																					RO										

Bit	Name	Functional Description	Access
31:12	*Reserved*	-	-
11:0	RESULT	ADC SQR scan conversion channelx conversion result	RO

28.5.9 ADC JQR Scan Conversion Channel x Result Register (ADC_JQRRESULTx) (x=0-3)

Offset: 0x090 (JQRRESULT0), 0x094 (JQRRESULT1), 0x098 (JQRRESULT2), 0x09C (JQRRESULT3)

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																				RESULT											
Access																					RO										

Bit	Name	Functional Description	Access
31:12	*Reserved*	-	-
11:0	RESULT	ADC JQR scan conversion channelx conversion result	RO

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28.5.10 ADC Conversion Result Register (ADC_RESULT)

Offset	Bit Position																													
0x0A0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																				RESULT											
Access																					RO										

Bit	Name	Functional Description	Access
31:12	*Reserved*	-	-
11:0	RESULT	ADC conversion results	RO

28.5.11 ADC Conversion Result Accumulation Value Register (ADC_RESULTACC)

Offset	Bit Position																													
0x0A4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved												RESULTACC																			
Access													RO																			

Bit	Name	Functional Description	Access
31:20	*Reserved*	-	-
19:0	RESULTACC	ADC conversion accumulated value	RO

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28.5.12 ADC Compare High Threshold Register (ADC_HT)

Offset	Bit Position																													
0x0A8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000FFF																															
Name	Reserved																				HT											
Access																					RW										

Bit	Name	Functional Description	Access
31:12	*Reserved*	-	-
11:0	HT	ADC conversion result comparison high threshold	RW

28.5.13 ADC Compare Low Threshold Register (ADC_LT)

Offset	Bit Position																													
0x0AC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																				LT											
Access																					RW										

Bit	Name	Functional Description	Access
31:12	*Reserved*	-	-
11:0	LT	ADC conversion result comparison low threshold	RW

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28.5.14 ADC Interrupt Flag Register (ADC_IFR)

Offset	Bit Position																													
0x0B0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																										JQRIF	SQRIF	REGIF	HTIF	LTIF	SGLIF
Access																											RO	RO	RO	RO	RO	RO

Bit	Name	Functional Description	Access
31:6	*Reserved*	-	-
5	JQRIF	ADC JQR scan conversion complete flag ● 0b0: Conversion not complete ● 0b1: Conversion complete	RO
4	SQRIF	ADC SQR scan conversion complete flag ● 0b0: Conversion not complete ● 0b1: Conversion complete	RO
3	REGIF	ADC conversion result comparison interval flag ● 0b0: ADC conversion result is outside the [ADC_LT, ADC_HT) range ● 0b1: ADC conversion result is within the range of [ADC_LT, ADC_HT)	RO
2	HTIF	ADC conversion result comparison upper threshold flag ● 0b0: ADC conversion result is outside [ADC_HT, 4095] range ● 0b1: ADC conversion result is within the range [ADC_HT, 4095]	RO
1	LTIF	ADC conversion result comparison lower threshold flag ● 0b0: ADC conversion result is outside the interval [0, ADC_LT) ● 0b1: ADC conversion result is within the range [0, ADC_LT)	RO
0	SGLIF	ADC single conversion complete flag ● 0b0: Conversion not complete ● 0b1: Conversion complete	RO

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28.5.15 ADC Interrupt Clear Register (ADC_ICR)

Offset	Bit Position																													
0x0B4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000003F																															
Name	Reserved																										JQRIC	SQRIC	REGIC	HTIC	LTIC	SGLIC
Access																											WO	WO	WO	WO	WO	WO

Bit	Name	Functional Description	Access
31:6	*Reserved*	-	-
5	JQRIC	ADC JQR scan conversion complete flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
4	SQRIC	ADC SQR scan conversion complete flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
3	REGIC	ADC conversion result comparison interval flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
2	HTIC	ADC conversion result comparison upper threshold flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
1	LTIC	ADC conversion result comparison lower threshold flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO
0	SGLIC	ADC single conversion complete flag clear Write 0 to clear flag, write 1 has no effect; read always returns 1.	WO

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28.5.16 ADC Single or SQR Scan Conversion External Interrupt Trigger Source Configuration Register (ADC_EXTTRIGGER0)

Offset	Bit Position																													
0x0B8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	PC15	PB15	PA15	PC11	PB11	PA11	Reserved	PC07	PB07	PA07	PD03	PC03	PB03	PA03	DMA	SPI1	SPI0	PCA	RTC	VC1	VC0	LPUART1	LPUART0	UART1	UART0	TIM6	TIM5	TIM4	TIM3	TIM2	TIM1	TIM0
Access	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31	PC15	PC15 interrupt triggers ADC conversion	RW
30	PB15	PB15 interrupt triggers ADC conversion	RW
29	PA15	PA15 interrupt triggers ADC conversion	RW
28	PC11	PC11 interrupt triggers ADC conversion	RW
27	PB11	PB11 interrupt triggers ADC conversion	RW
26	PA11	PA11 interrupt triggers ADC conversion	RW
25	*Reserved*	-	-
24	PC07	PC07 interrupt triggers ADC conversion	RW
23	PB07	PB07 interrupt triggers ADC conversion	RW
22	PA07	PA07 interrupt triggers ADC conversion	RW
21	PD03	PD03 interrupt triggers ADC conversion	RW
20	PC03	PC03 interrupt triggers ADC conversion	RW
19	PB03	PB03 interrupt triggers ADC conversion	RW
18	PA03	PA03 interrupt triggers ADC conversion	RW
17	DMA	DMA interrupt triggers ADC conversion	RW
16	SPI1	SPI1 interrupt triggers ADC conversion	RW
15	SPI0	SPI0 interrupt triggers ADC conversion	RW
14	PCA	PCA interrupt triggers ADC conversion	RW
13	RTC	RTC interrupt triggers ADC conversion	RW
12	VC1	VC1 interrupt triggers ADC conversion	RW
11	VC0	VC0 interrupt triggers ADC conversion	RW
10	LPUART1	LPUART1 interrupt triggers ADC conversion	RW
9	LPUART0	LPUART0 interrupt triggers ADC conversion	RW
8	UART1	UART1 interrupt triggers ADC conversion	RW
7	UART0	UART0 interrupt triggers ADC conversion	RW

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Bit	Name	Functional Description	Access
6	TIM6	Timer6 interrupt triggers ADC conversion	RW
5	TIM5	Timer5 interrupt triggers ADC conversion	RW
4	TIM4	Timer4 interrupt triggers ADC conversion	RW
3	TIM3	Timer3 interrupt triggers ADC conversion	RW
2	TIM2	Timer2 interrupt triggers ADC conversion	RW
1	TIM1	Timer1 interrupt triggers ADC conversion	RW
0	TIM0	Timer0 interrupt triggers ADC conversion	RW

Note

- TIM0/1/2/3/4/5/6 trigger ADC automatic conversion without the need to enable the corresponding interrupt. Simply configure the corresponding trigger enable registers of the TIM modules. For detailed operation, see the "Function Description Timer Trigger ADC" chapter in the "General Timers TIM0/1/2/3" and the "Function Description Internal Interconnection" chapter in the "Advanced Timer TIM4/5/6".
- Except for TIM0/1/2/3/4/5/6, other peripherals trigger the ADC using the rising edge of their respective interrupt flags. If repeated triggering is required, the interrupt flag needs to be cleared. If the interrupt service routine is not required, the NVIC interrupt enable shall not be enabled.

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28.5.17 ADC JQR Scan Conversion External Interrupt Trigger Source Configuration Register (ADC_EXTTRIGGER1)

Offset	Bit Position																													
0x0BC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	PC15	PB15	PA15	PC11	PB11	PA11	Reserved	PC07	PB07	PA07	PD03	PC03	PB03	PA03	DMA	SPI1	SPI0	PCA	RTC	VC1	VC0	LPUART1	LPUART0	UART1	UART0	TIM6	TIM5	TIM4	TIM3	TIM2	TIM1	TIM0
Access	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31	PC15	PC15 interrupt triggers ADC conversion	RW
30	PB15	PB15 interrupt triggers ADC conversion	RW
29	PA15	PA15 interrupt triggers ADC conversion	RW
28	PC11	PC11 interrupt triggers ADC conversion	RW
27	PB11	PB11 interrupt triggers ADC conversion	RW
26	PA11	PA11 interrupt triggers ADC conversion	RW
25	*Reserved*	-	-
24	PC07	PC07 interrupt triggers ADC conversion	RW
23	PB07	PB07 interrupt triggers ADC conversion	RW
22	PA07	PA07 interrupt triggers ADC conversion	RW
21	PD03	PD03 interrupt triggers ADC conversion	RW
20	PC03	PC03 interrupt triggers ADC conversion	RW
19	PB03	PB03 interrupt triggers ADC conversion	RW
18	PA03	PA03 interrupt triggers ADC conversion	RW
17	DMA	DMA interrupt triggers ADC conversion	RW
16	SPI1	SPI1 interrupt triggers ADC conversion	RW
15	SPI0	SPI0 interrupt triggers ADC conversion	RW
14	PCA	PCA interrupt triggers ADC conversion	RW
13	RTC	RTC interrupt triggers ADC conversion	RW
12	VC1	VC1 interrupt triggers ADC conversion	RW
11	VC0	VC0 interrupt triggers ADC conversion	RW
10	LPUART1	LPUART1 interrupt triggers ADC conversion	RW
9	LPUART0	LPUART0 interrupt triggers ADC conversion	RW
8	UART1	UART1 interrupt triggers ADC conversion	RW
7	UART0	UART0 interrupt triggers ADC conversion	RW

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Bit	Name	Functional Description	Access
6	TIM6	Timer6 interrupt triggers ADC conversion	RW
5	TIM5	Timer5 interrupt triggers ADC conversion	RW
4	TIM4	Timer4 interrupt triggers ADC conversion	RW
3	TIM3	Timer3 interrupt triggers ADC conversion	RW
2	TIM2	Timer2 interrupt triggers ADC conversion	RW
1	TIM1	Timer1 interrupt triggers ADC conversion	RW
0	TIM0	Timer0 interrupt triggers ADC conversion	RW

Note

- TIM0/1/2/3/4/5/6 trigger ADC automatic conversion without the need to enable the corresponding interrupt. Simply configure the corresponding trigger enable registers of the TIM modules. For detailed operation, see the "Function Description Timer Trigger ADC" section in the "General Timers TIM0/1/2/3" and the "Function Description Internal Interconnection" section in the "Advanced Timer TIM4/5/6".
- Except for TIM0/1/2/3/4/5/6, other peripherals trigger the ADC using the rising edge of their respective interrupt flags. If repeated triggering is required, the interrupt flag needs to be cleared. If the interrupt service routine is not required, the NVIC interrupt enable shall not be enabled.

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28.5.18 ADC Single Conversion Start Control Register (ADC_SGLSTART)

Offset	Bit Position																													
0x0C0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																															START
Access																																RW

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-
0	START	ADC Single conversion start control ● 0b0: Stop ● 0b1: Start	RW

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28.5.19 ADC SQR Scan Conversion Start Control Register (ADC_SQRSTART)

Offset	Bit Position																													
0x0C4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																															START
Access																																RW

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-
0	START	ADC SQR scan conversion start control ● 0b0: Stop ● 0b1: Start	RW

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28.5.20 ADC JQR Scan Conversion Start Control Register (ADC_JQRSTART)

Offset	Bit Position																													
0x0C8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																														START	
Access																															RW	

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-
0	START	ADC JQR scan conversion start control ● 0b0: Stop ● 0b1: Start	RW

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28.5.21 ADC Continuous Conversion Start/Stop Control Register (ADC_ALLSTART)

Offset	Bit Position																													
0x0CC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																															START
Access																																RW

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-
0	START	ADC continuous start of single conversion control ● 0b0: Stop ADC conversion and need to wait until the end of the current conversion ● 0b1: Start ADC to convert all the time Reading 0 indicates no conversion; reading 1 indicates conversion in progress.	RW

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29 DAC

29.1 Introduction

The DAC module is a 12-bit voltage output digital-to-analog converter. The DAC can be configured in 8-bit or 12-bit mode; in 12-bit mode, it can be left alignment or right alignment. The DAC can operate with the DMA controller and utilize the external input reference voltage EXVREF (shared with the ADC) for more precise conversion results. The output of the DAC is connected to the OPA module for higher drive capability.

29.2 Features

- One data holding register
- Two data bit width: 8-bit, 12-bit
- Two alignment methods: left alignment, right alignment, valid only when the width is 12 bits
- Two math waveforms: Noise, triangle
- Four reference voltages: AVCC, EXVREF pin, built-in 1.5V, built-in 2.5V
- Conversion via external trigger signal
- DMA function

29.3 Functional Description

29.3.1 Function Block Diagram

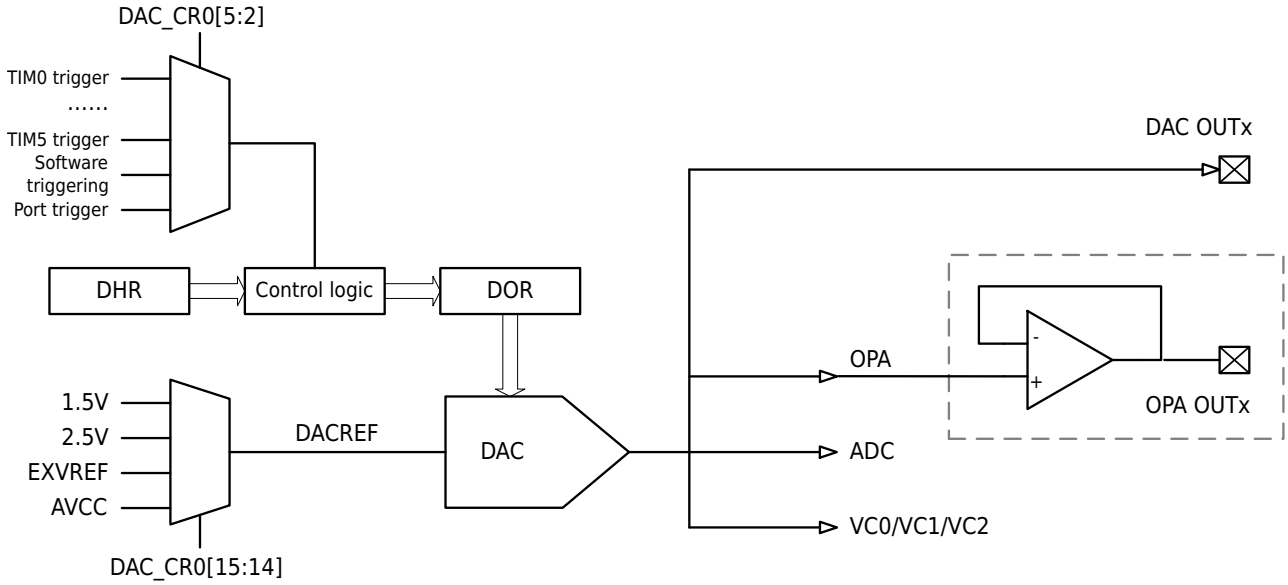

Figure 29-1 DAC Functional Block Diagram

29.3.2 Output Voltage Formula

After linearly converted, the value of the DOR register is changed to an output voltage ranging from 0 to DACREF.

The output voltage is determined by the following formula:

$$DAC_{out} = \frac{V_{ref} \times DOR}{4096}$$

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29.3.3 Output Voltage Conversion

The DAC module converts the value of the DAC_DOR0 register into an analog voltage in real time, which can be output to the DAC_OUT port, ADC, VC, and OPA. The voltage signal output by the DAC_OUT port basically has no driving capability, it is recommended to use the OPA_OUTx port as the output of the DAC.

When DAC_DOR0 is loaded with DAC_DHR0 content, the analog output voltage will be available after a period of time ($T_{DACSETTLE}$), depending on the supply voltage and analog output load.

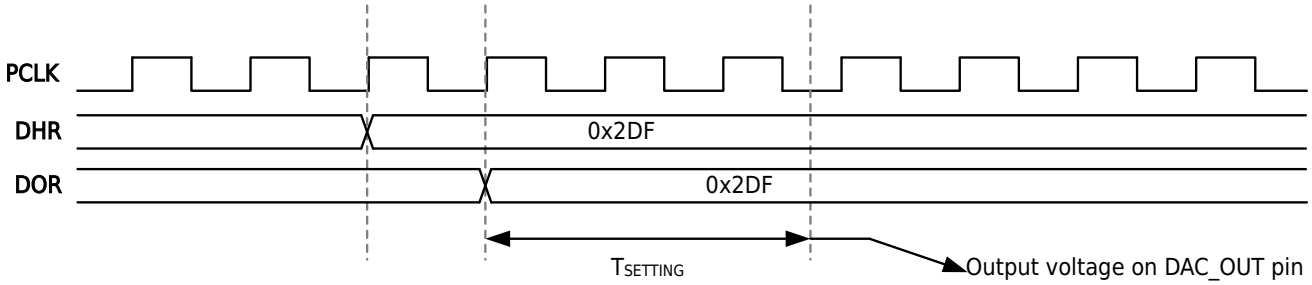

Figure 29-2 Timing Diagram of DAC Conversion When Trigger is Disabled

The DAC_DOR0 register is not directly accessible, any data must pass through the DAC_DHR0 register to be transferred to the DAC_DOR0 register. If DAC_CR0. TEN0 is 0, the data in the DAC_DHR0 register will be automatically transferred to the DAC_DOR0 register when each PCLK clock occurs. If DAC_CR0. TEN0 is 1, the value of the DAC_DHR0 register will be transferred to the DAC_DOR0 register only when the trigger signal appears.

When the DAC operates in trigger mode, configuring DAC_CR0[7:6] allows the DAC output voltage to superimpose noise or a triangular wave. The amplitude of the superimposed waveform can be set via DAC_CR0[11:8].

29.3.4 Output Buffer

Set DAC_CR0. BOFF0 to 0, that is, the OPA can be used as the output buffer of the DAC to reduce the output impedance of the DAC and increase the driving capability of the DAC. The voltage signal output by the DAC is output to the port after passing through the OPA.

Notice

The OPA needs to be configured in DAC output follower mode.

29.3.5 Trigger Selection

If DAC_CR0. TEN0 is 0, the value written to the DAC_DHR register arrives at the DAC_DOR register one PCLK later.

If DAC_CR0. TEN0 is 1, the value written to the DAC_DHR register is transferred to the DAC_DOR register after the trigger condition is generated, and the transfer process takes a certain amount of time. The DAC output can be refreshed under specified conditions through the trigger function.

DAC supports three trigger conditions: TIM output TRGO signal, rising edge of trigger port and software trigger. Among them, the TIM trigger signal and the port trigger signal can update DAC_DOR for 3 PCLKs, and the software trigger signal can update DAC_DOR for 1 PCLK.

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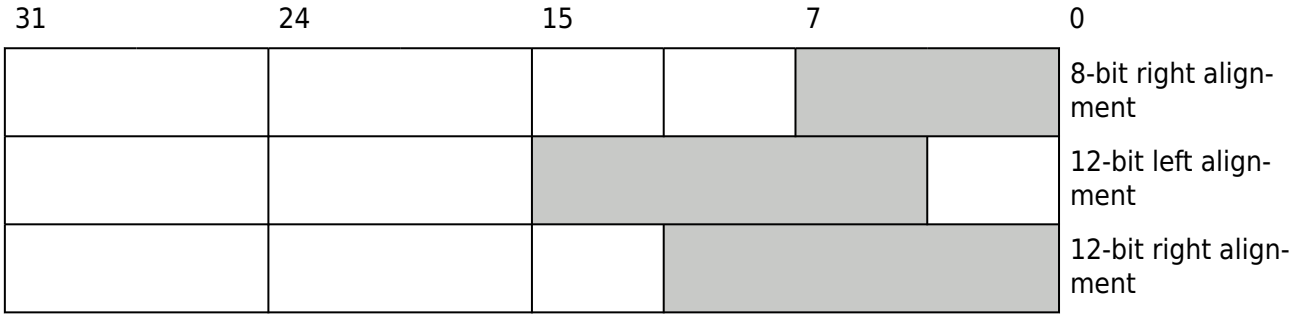
Notice

When DAC is enabled, the contents of DAC_CR0[5:3] cannot be changed.

29.3.6 Data Alignment

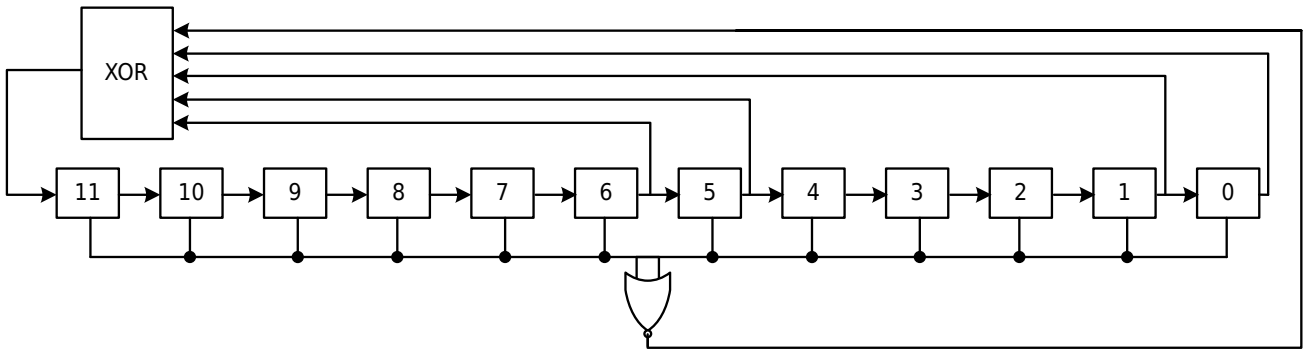
This module supports three data alignment methods, and the configured data alignment method must be consistent with the written data alignment method.

- 8-bit right alignment: software must load data into DAC_DHR8R0[7:0] bits (actually stored into DHR0[11:4] bits)
- 12-bit left alignment: software must load data into DAC_DHR12L0[15:4] bits (actually stored into DHR0[11:0] bits)
- 12-bit right alignment: software must load data into DAC_DHR12R0[11:0] bits (actually stored into DHR0[11:0] bits)



29.3.7 Noise Generation

To generate pseudo noise of variable amplitude, LFSRs (Linear feedback shift registers) are used. Set WAVE0[1:0] to "01" to select to generate noise. The pre-load value in LFSR is 0xAAA. After each trigger event, the register will update according to a specific calculation algorithm within three PCLK clock cycles.



The LFSR value can be partially or completely masked by the MAMP0[3:0] bits in the DAC_CR0 register, and the resulting value will be added to the content of DAC_DHR0 and then stored in the DAC_DOR0 register. If overflow occurs, the overflow bit will be discarded.

If LFSR is 0x000, "1" will be injected into it (anti-lock mechanism).

The LFSR waveform generation function can be disabled by resetting the WAVE0[1:0] bits.

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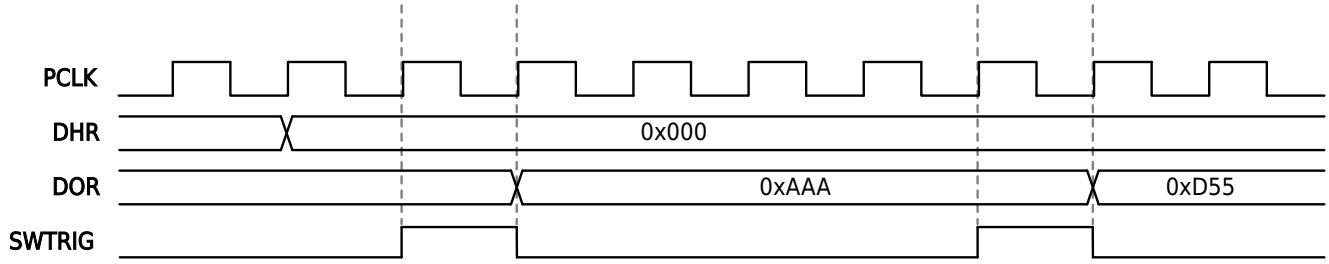

Figure 29-4 DAC Conversion of LFSR Generated Waveform (Using Software Trigger)

29.3.8 Triangle Wave Generation

A small amplitude triangle wave can be superimposed on a DC or slowly varying signal. Set WAVE0[1:0] to "10" to select DAC to generate triangle wave. The amplitude is configured via the MAMP0[3:0] bits in the DAC_CR0 register. After each trigger event, the internal triangle counter will increment within three PCLK clock cycles.. In case overflow does not occur, the value of this counter is added to the contents of the DAC_DHR0 register and the sum is stored in the DAC_DOR0 register. As long as it is less than the maximum amplitude defined by the MAMP0[3:0] bits, the triangle wave counter will keep incrementing. Once the configured amplitude is reached, the counter is decremented to zero, then incremented, and so on.

The triangle wave generation function can be disabled by resetting the WAVE0[1:0] bits.

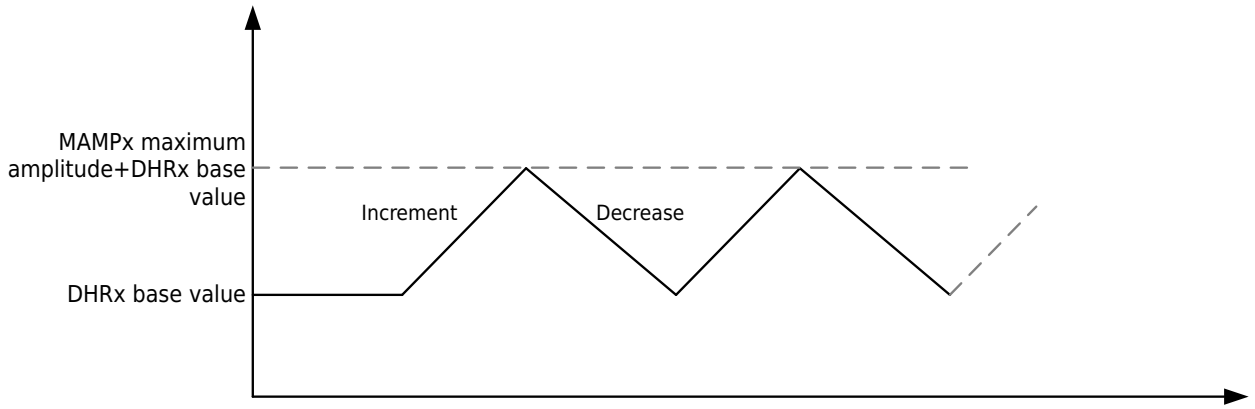

Figure 29-5 Generate DAC Triangle Wave

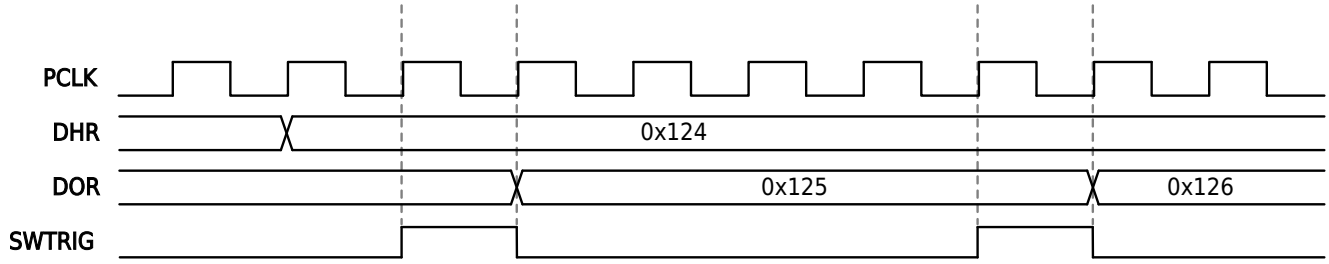

Figure 29-6 DAC Conversion to Generate Triangle Waveform (Software Trigger Enabled)

29.3.9 DMA Request

DAC channel has DMA function. The DMA channel is used to handle the DMA request of the DAC channel.

When the DMAEN0 bit is set to 1, a DAC DMA request will be generated if a trigger occurs. The value of the DAC_DHR0 register is then transferred to the DAC_DOR0 register.

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DMA Underflow

The DAC DMA request has no buffer queue. If a second external trigger arrives before the first trigger is acknowledged, no new request will be issued, and the DMAUDR0 (DMA underflow flag) in the DAC_SR register will be set to 1 to report this error condition. DMA data transfers are then disabled and no other DMA requests are processed. The DAC channel will still continue to convert legacy data.

Software should clear the DMAUDR0 flag by writing a "0", clear the DMAEN bit for the DMA data stream being used, and reinitialize the DMA and DAC channels to properly restart the DMA transfer. Software should modify the frequency of DAC trigger conversions or reduce the DMA workload to avoid DMA underflow from happening again. Finally, DAC conversions can be continued by enabling DMA data transfers and conversion triggers.

For DAC channels, an interrupt will also be generated if the DMAUDRIE0 bit in the DAC_CR0 register is enabled.

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29.4 Register Description

29.4.1 Register List

Base address: 0x40002500

Table 29-2 Digital-to-Analog Converter (DAC) Register Offset

Offset	Register	Description	Width
0x000	DAC_CR0	Control Register	32
0x004	DAC_SWTR	Software Trigger Register	32
0x008	DAC_DHR12R0	DAC 12-bit Right Alignment Data Holding Register	32
0x00C	DAC_DHR12L0	DAC 12-bit Left Alignment Data Holding Register	32
0x010	DAC_DHR8R0	DAC 8-bit Right Alignment Data Holding Register	32
0x02C	DAC_DOR0	DAC Data Output Register	32
0x034	DAC_SR	Status Register	32
0x038	DAC_ETRS	DAC Test Register/External Trigger Select Register	32

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29.4.2 DAC Control Register (DAC_CR0)

Offset	Bit Position																													
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0000C000																															
Name	Reserved																SREF0		DMAUDRIE0	DMAEN0	MAMP0				WAVE0		TSEL0			TEN0	BOFF0	EN0
Access																	RW		RW		RW				RW		RW				RW	

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:14	SREF0	DAC reference voltage selection ● 0b00: Internal 1.5V ● 0b01: Internal 2.5V ● 0b10: External reference voltage EXVREF (PB01) ● 0b11: AVCC voltage	RW
13	DMAUDRIE0	DAC DMA underflow interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
12	DMAEN0	DAC channel DMA enable ● 0b0: Disable ● 0b1: Enable	RW
11:8	MAMP0	DAC channel mask/amplitude selector ● 0b0000: Do not mask bit 0 of LFSR/triangle wave amplitude equal to 1 ● 0b0001: Do not mask bit [1:0] of LFSR/triangle wave amplitude equal to 3 ● 0b0010: Do not mask bit [2:0] of LFSR/triangle wave amplitude equal to 7 ● 0b0011: Do not mask bit [3:0] of LFSR/triangle wave amplitude equal to 15 ● 0b0100: Do not mask bit [4:0] of LFSR/triangle wave amplitude equal to 31 ● 0b0101: Do not mask bit [5:0] of LFSR/triangle wave amplitude equal to 63 ● 0b0110: Do not mask bit [6:0] of LFSR/triangle wave amplitude equal to 127 ● 0b0111: Do not mask bit [7:0] of LFSR/triangle wave amplitude equal to 255 ● 0b1000: Do not mask bit [8:0] of LFSR/triangle wave amplitude equal to 511 ● 0b1001: Do not mask bit [9:0] of LFSR/triangle wave amplitude equal to 1023 ● 0b1010: Do not mask bit [10:0] of LFSR/triangle wave amplitude equal to 2047	RW

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Bit	Name	Functional Description	Access
11:8	MAMP0	● 0b1011-0b1111: Do not mask bit [11:0] of LFSR/triangle wave amplitude equal to 4095	
7:6	WAVE0	DAC channel noise/triangular wave generation enable ● 0b00: Disable wave generation ● 0b01: Enable noise waves generation ● 0b10/0b11: Enable triangle wave generation	RW
5:3	TSEL0	DAC channel trigger selection ● 0b000: TIM0 TRADC trigger ● 0b001: TIM1 TRADC trigger ● 0b010: TIM2 TRADC trigger ● 0b011: TIM3 TRADC trigger ● 0b100: TIM4 TRADC trigger ● 0b101: TIM5 TRADC trigger ● 0b110: Software trigger ● 0b111: External port trigger	RW
2	TEN0	DAC channel trigger enable ● 0b0: Disable ● 0b1: Enable	RW
1	BOFF0	DAC channel output buffer disabled ● 0b0: Enable DAC channel output buffer ● 0b1: Disable DAC channel output buffer **Notice** The buffer needs to be enabled in the application, otherwise the output of the DAC basically has no driving capability.	RW
0	EN0	DAC enable control ● 0b0: Disable ● 0b1: Enable	RW

29.4.3 DAC Software Trigger Register (DAC_SWTR)

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																															SWTRIG0
Access																																WO

Bit	Name	Functional Description	Access
31:1	*Reserved*	-	-

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Bit	Name	Functional Description	Access
0	SWTRIG0	DAC software trigger Auto-clearing, writing 1 generates a software trigger, writing 0 has no effect	WO

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29.4.4 DAC 12-bit Right Alignment Data Holding Register (DAC_DHR12R0)

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																				DHR0											
Access																					RW											

Bit	Name	Functional Description	Access
31:12	*Reserved*	-	-
11:0	DHR0	DAC channel 12-bit right-aligned data These bits are written by software to specify the 12-bit data for the DAC channel	RW

29.4.5 DAC 12-bit Left Alignment Data Holding Register (DAC_DHR12L0)

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																				DHR0											
Access																					RW											

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15:4	DHR0	DAC channel 12-bit left-aligned data These bits are written by software to specify the 12-bit data for the DAC channel	RW
3:0	*Reserved*	-	-

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29.4.6 DAC 8-bit Right Alignment Data Holding Register (DAC_DHR8R0)

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																								DHR0							
Access																									RW							

Bit	Name	Functional Description	Access
31:8	*Reserved*	-	-
7:0	DHR0	DAC channel 8-bit right-aligned data These bits are written by software to specify the 8-bit data for the DAC channel	RW

29.4.7 DAC Data Output Register (DAC_DOR0)

Offset	Bit Position																													
0x02C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																				DOR0											
Access																					RO											

Bit	Name	Functional Description	Access
31:12	*Reserved*	-	-
11:0	DOR0	DAC channel data output	RO

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29.4.8 DAC Status Register (DAC_SR)

Offset	Bit Position																													
0x034	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																		DMAUDR0	Reserved											
Access																			RW												

Bit	Name	Functional Description	Access
31:14	*Reserved*	-	-
13	DMAUDR0	DAC channel DMA underflow flag Write 0 to clear the bit, write 1 has no effect. Read: ● 0b0: No DMA underflow error occurred on the DAC channel ● 0b1: A DMA underflow error occurs on the DAC channel (the currently selected trigger source drives the DAC channel conversion at a frequency higher than the DMA service capability)	RW
12:0	*Reserved*	-	-

29.4.9 DAC Test Register/External Trigger Select Register (DAC_ETRS)

Offset	Bit Position																													
0x038	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																									PTRIGSEL			Reserved			
Access																										RW						

Bit	Name	Functional Description	Access
31:7	*Reserved*	-	-
6:4	PTRIGSEL	Port trigger selection ● 0b000: PA09 ● 0b001: PB09 ● 0b010: PC09 ● 0b011: PD09 ● 0b1xx: Setting prohibited	RW
3:0	*Reserved*	-	-

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30 VC

30.1 Introduction

The analog voltage comparator VC is used to compare the size of two input analog voltages, and output high/low level according to the comparison result.

- When the "+" input voltage is higher than the "-" input voltage, the voltage comparator output is high;
- When the "+" input voltage is lower than the "-" input voltage, the voltage comparator output is low.

30.2 Features

- Support voltage comparison function
- Support internal 64-stage VCC voltage divider (use the voltage divider source voltage to be greater than 1.8V)
- Support 16 internal and external signals as the input of the positive and negative terminals of the voltage comparator.
- Support 3 interrupt trigger mode: high-level trigger/rising edge trigger/falling edge trigger
- The output of the voltage comparator can be used as general timer and low-power timer control input
- The output of the voltage comparator can be used as brake input or capture input for advanced timer and general timers;
- Support working in the DeepSleep mode. The interrupt output of the voltage comparator can wake up the chip from the DeepSleep mode
- Provide software configurable filter time to enhance the anti-interference ability of the chip.

Note

BGR needs to be enabled when using VC see "Other Analog Registers" chapter to BGR register related description.

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30.3 Functional Description

30.3.1 Function Block Diagram

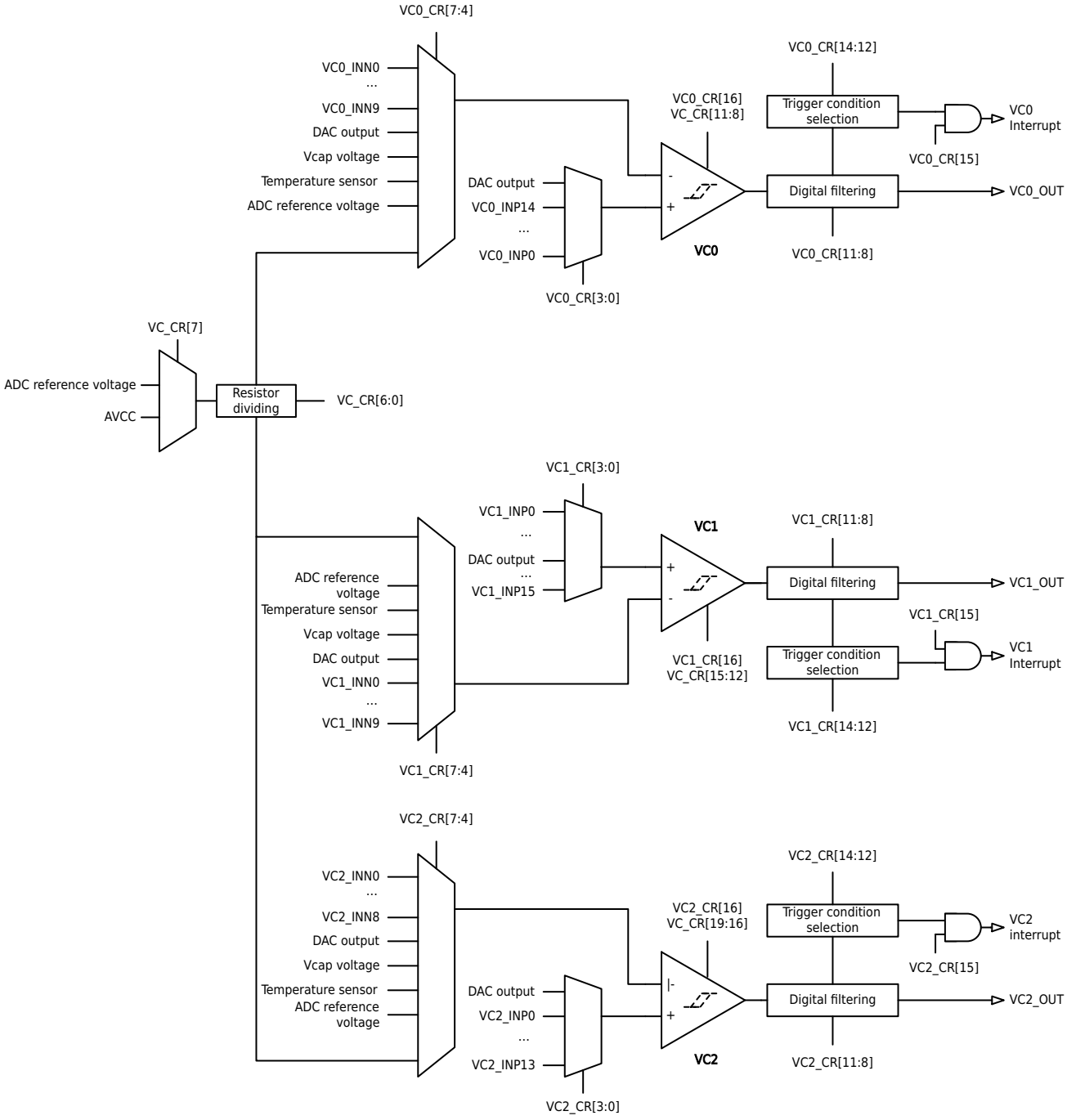

Figure 30-1 VC Function Block Diagram

30.3.2 Setup/Response Time

When using a voltage comparator, the time from when VC is enabled or when the input voltage at both ends of VC changes to when correct result is output is determined by the VC_CR.VCx_BIAS_SEL bit. The larger the current, the faster the VC response. For the specific time, see the description in the "Electrical Specifications-Operating Conditions-VC Features" chapter of the "Datasheet".

When the ADC reference voltage (1.5V or 2.5V) is used as the comparison reference voltage, or when VC_CR.VCx_BIAS_SEL=0b10/0b11, the BGR needs to be started (For the stabilization time T_{warmup} after

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the BGR is started, see the description in the "Electrical Specifications-Operating Conditions-VC Features" chapter of the "Datasheet"). The voltage comparator needs to wait until the internal BGR is stable before it can output normally.

30.3.3 Digital Filtering

In addition to the inherent setup/response time of the voltage comparator, the user can set a longer filter time to filter out system noise, such as high current noise when the motor stops.

The digital filtering signal level can be read from the register VC_IFR.VCx_FILTER; when the GPIO function is configured as VCx_OUT, the digital filtering signal can be output from the GPIO for easy measurement.

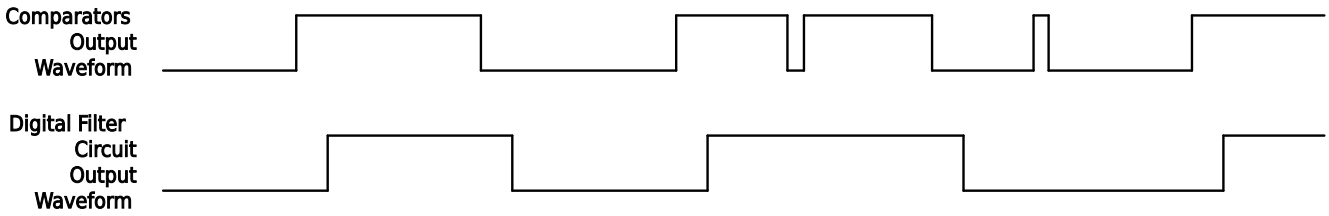

Figure 30-2 VC Filter Response Time

30.3.4 Hysteresis Function

The hysteresis function can be selected for the voltage comparator, and the diagram after the hysteresis function is enabled is as follows:

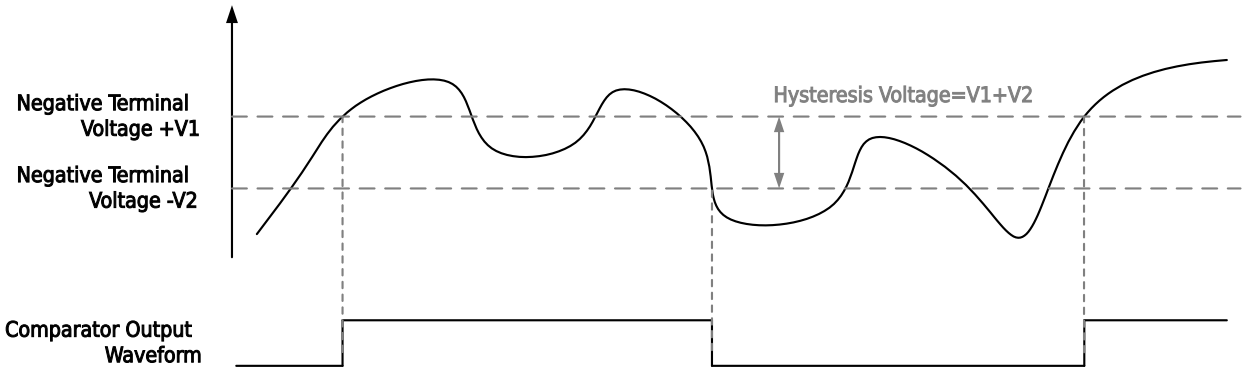

Figure 30-3 VC Hysteresis Function

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30.4 Register Description

30.4.1 Register List

Base address: 0x40002400

Table 30-1 Analog Voltage Comparator (VC) Register Offset

Offset	Register	Description	Width
0x010	VC_CR	VC Configuration Register	32
0x014	VC0_CR	VC0 Configuration Register	32
0x018	VC1_CR	VC1 Configuration Register	32
0x01C	VC0_OUT_CFG	VC0 Output Configuration Register	32
0x020	VC1_OUT_CFG	VC1 Output Configuration Register	32
0x024	VC_IFR	VC Interrupt Register	32
0x150	VC2_CR	VC2 Configuration Register	32
0x154	VC2_OUT_CFG	VC2 Output Configuration Register	32

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30.4.2 VC Configuration Register (VC_CR)

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000020																															
Name	Reserved												VC2_HYS_SEL		VC2_BIAS_SEL		VC1_HYS_SEL		VC1_BIAS_SEL		VC0_HYS_SEL		VC0_BIAS_SEL		REF2P5_SEL	DIV_EN	DIV					
Access													RW		RW		RW		RW		RW		RW		RW	RW	RW					

Bit	Name	Functional Description	Access
31:20	*Reserved*	-	-
19:18	VC2_HYS_SEL	VC2 hysteresis selection ● 0b00: No hysteresis ● 0b01: Hysteresis voltage about 10mV ● 0b10: Hysteresis voltage about 20mV ● 0b11: Hysteresis voltage about 30mV	RW
17:16	VC2_BIAS_SEL	VC2 power consumption selection The greater the power consumption, the faster the response ● 0b00: 300nA ● 0b01: 1.2μA ● 0b10: 10μA (The BGR needs to be enabled and wait for the T_{warmup} time. For the specific value, see the description in the "Electrical Specifications-Operating Conditions-VC Features" chapter of the "Datasheet". ● 0b11: 20μA (The BGR needs to be enabled and wait for the T_{warmup} time. For the specific value, see the description in the "Electrical Specifications-Operating Conditions-VC Features" chapter of the "Datasheet".	RW
15:14	VC1_HYS_SEL	VC1 hysteresis selection ● 0b00: No hysteresis ● 0b01: Hysteresis voltage about 10mV ● 0b10: Hysteresis voltage about 20mV ● 0b11: Hysteresis voltage about 30mV	RW

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Bit	Name	Functional Description	Access
13:12	VC1_BIAS_SEL	VC1 power consumption selection The greater the power consumption, the faster the response ● 0b00: 300nA ● 0b01: 1.2μA ● 0b10: 10μA (The BGR needs to be enabled and wait for the T_{warmup} time. For the specific value, see the description in the "Electrical Specifications-Operating Conditions-VC Features" chapter of the "Datasheet". ● 0b11: 20μA (The BGR needs to be enabled and wait for the T_{warmup} time. For the specific value, see the description in the "Electrical Specifications-Operating Conditions-VC Features" chapter of the "Datasheet".	RW
11:10	VC0_HYS_SEL	VC0 hysteresis selection ● 0b00: No hysteresis ● 0b01: Hysteresis voltage about 10mV ● 0b10: Hysteresis voltage about 20mV ● 0b11: Hysteresis voltage about 30mV	RW
9:8	VC0_BIAS_SEL	VC0 power consumption selection The greater the power consumption, the faster the response ● 0b00: 300nA ● 0b01: 1.2μA ● 0b10: 10μA (The BGR needs to be enabled and wait for the T_{warmup} time. For the specific value, see the description in the "Electrical Specifications-Operating Conditions-VC Features" chapter of the "Datasheet". ● 0b11: 20μA (The BGR needs to be enabled and wait for the T_{warmup} time. For the specific value, see the description in the "Electrical Specifications-Operating Conditions-VC Features "chapter of the "Datasheet".	RW
7	REF2P5_SEL	VC_DIV reference voltage Vref selection ● 0b0: AVCC ● 0b1: The reference voltage selected by ADC_CR0.REF	RW
6	DIV_EN	6-bit resistor voltage-dividing enabled ● 0b0: Disable ● 0b1: Enable	RW
5:0	DIV	6-bit resistor voltage-dividing configuration ● 0b000000: 1/64 Vref ● 0b000001: 2/64 Vref ● 0b000010: 3/64 Vref ● 0b000011: 4/64 Vref ● ... ● 0b111110: 63/64 Vref ● 0b111111: Vref	RW

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30.4.3 VC0 Configuration Register (VC0_CR)

Offset	Bit Position																													
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved															EN	IE	LEVEL	RISING	FALLING	DEBOUNCE_TIME			FLTEN	N_SEL			P_SEL			
Access																RW	RW	RW	RW	RW	RW			RW	RW			RW			

Bit	Name	Functional Description	Access
31:17	*Reserved*	-	-
16	EN	Voltage comparator enable ● 0b0: Disable ● 0b1: Enable	RW
15	IE	VC interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
14	LEVEL	VC output signal triggers interrupt selection ● 0b0: Disable high level trigger INT flag ● 0b1: Enable high level trigger INT flag	RW
13	RISING	VC output signal triggers interrupt selection ● 0b0: Disable rising edge trigger INT flag ● 0b1: Enable rising edge trigger INT flag	RW
12	FALLING	VC output signal triggers interrupt selection ● 0b0: Disable falling edge trigger INT flag ● 0b1: Enable falling edge trigger INT flag	RW
11:9	DE-BOUNCE_TIME	VC output filter time configuration ● 0b000: The filtering time is about 7μs ● 0b001: The filtering time is about 14μs ● 0b010: The filtering time is about 28μs ● 0b011: The filtering time is about 112μs ● 0b100: The filtering time is about 450μs ● 0b101: The filtering time is about 1.8ms ● 0b110: The filtering time is about 7.2ms ● 0b111: The filtering time is about 28.8ms **Note** The filter time configuration is only valid when FLTEN=0b1.	RW

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Bit	Name	Functional Description	Access
8	FLTEN	VC filter enable ● 0b0: Disable ● 0b1: Enable	RW
7:4	N_SEL	Voltage comparator "-" terminal input selection ● 0b0000: Select channel 0 input PA0 ● 0b0001: Select channel 1 input PA1 ● 0b0010: Select channel 2 input PA2 ● 0b0011: Select channel 3 input PA3 ● 0b0100: Select channel 4 input PA4 ● 0b0101: Select channel 5 input PA5 ● 0b0110: Select channel 6 input PA6 ● 0b0111: Select channel 7 input PA7 ● 0b1000: Select channel 8 input PC4 ● 0b1001: Select channel 9 input PC5 ● 0b1010: DAC ● 0b1011: Resistor voltage dividing output voltage ● 0b1100: Internal temperature sensor output voltage ● 0b1101: Setting prohibited ● 0b1110: ADC's REF (ADC needs to be enabled for use) ● 0b1111: VCAP pin voltage	RW
3:0	P_SEL	Voltage comparator "+" terminal input selection ● 0b0000: Select channel 0 input PC0 ● 0b0001: Select channel 1 input PC1 ● 0b0010: Select channel 2 input PC2 ● 0b0011: Select channel 3 input PC3 ● 0b0100: Select channel 4 input PA0 ● 0b0101: Select channel 5 input PA1 ● 0b0110: Select channel 6 input PA2 ● 0b0111: Select channel 7 input PA3 ● 0b1000: Select channel 8 input PA4 ● 0b1001: Select channel 9 input PA5 ● 0b1010: Select channel 10 input PA6 ● 0b1011: Select channel 11 input PA7 ● 0b1100: Select channel 12 input PB4 ● 0b1101: Select channel 13 input PB5 ● 0b1110: Select channel 14 input PB6 ● 0b1111: DAC	RW

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30.4.4 VC1 Configuration Register (VC1_CR)

Offset	Bit Position																													
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved															EN	IE	LEVEL	RISING	FALLING	DEBOUNCE_TIME			FLTEN	N_SEL		P_SEL				
Access																RW	RW	RW	RW	RW	RW			RW	RW		RW				

Bit	Name	Functional Description	Access
31:17	*Reserved*	-	-
16	EN	Voltage comparator enable ● 0b0: Disable ● 0b1: Enable	RW
15	IE	VC interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
14	LEVEL	VC output signal triggers interrupt selection ● 0b0: Disable high level trigger INT flag ● 0b1: Enable high level trigger INT flag	RW
13	RISING	VC output signal triggers interrupt selection ● 0b0: Disable rising edge trigger INT flag ● 0b1: Enable rising edge trigger INT flag	RW
12	FALLING	VC output signal triggers interrupt selection ● 0b0: Disable falling edge trigger INT flag ● 0b1: Enable falling edge trigger INT flag	RW
11:9	DE-BOUNCE_TIME	VC output filter time configuration ● 0b000: The filtering time is about 7μs ● 0b001: The filtering time is about 14μs ● 0b010: The filtering time is about 28μs ● 0b011: The filtering time is about 112μs ● 0b100: The filtering time is about 450μs ● 0b101: The filtering time is about 1.8ms ● 0b110: The filtering time is about 7.2ms ● 0b111: The filtering time is about 28.8ms **Note** The filter time configuration is only valid when FLTEN=0b1.	RW

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Bit	Name	Functional Description	Access
8	FLTEN	VC filter enable ● 0b0: Disable ● 0b1: Enable	RW
7:4	N_SEL	Voltage comparator "-" terminal input selection ● 0b0000: Select channel 0 input PC0 ● 0b0001: Select channel 1 input PC1 ● 0b0010: Select channel 2 input PC2 ● 0b0011: Select channel 3 input PC3 ● 0b0100: Select channel 4 input PA0 ● 0b0101: Select channel 5 input PA1 ● 0b0110: Select channel 6 input PB0 ● 0b0111: Select channel 7 input PB1 ● 0b1000: Select channel 8 input PB2 ● 0b1001: Select channel 9 input PB3 ● 0b1010: DAC ● 0b1011: Resistor voltage dividing output voltage ● 0b1100: Internal temperature sensor output voltage ● 0b1101: Setting prohibited ● 0b1110: ADC's REF (ADC needs to be enabled for use) ● 0b1111: VCAP pin voltage	RW
3:0	P_SEL	Voltage comparator "+" terminal input selection ● 0b0000: Select channel 0 input PA0 ● 0b0001: Select channel 1 input PA1 ● 0b0010: Select channel 2 input PA2 ● 0b0011: Select channel 3 input PA3 ● 0b0100: Select channel 4 input PA4 ● 0b0101: Select channel 5 input PA5 ● 0b0110: Select channel 6 input PB1 ● 0b0111: Select channel 7 input PB2 ● 0b1000: Select channel 8 input PB10 ● 0b1001: Select channel 9 input PB12 ● 0b1010: Select channel 10 input PB13 ● 0b1011: Select channel 11 input PB14 ● 0b1100: Select channel 12 input PB4 ● 0b1101: DAC ● 0b1110: Select channel 14 input PB6 ● 0b1111: Select channel 15 input PB7	RW

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30.4.5 VC0 Output Configuration Register (VC0_OUT_CFG)

Offset	Bit Position																													
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																BRAKE	TIM6	INV_TIM6	TIM5	INV_TIM5	TIM4	INV_TIM4	Reserved			TIMBK	TIM3RCLR	TIM2RCLR	TIM1RCLR	TIM0RCLR	INV_TIMER
Access																	RW	RW	RW	RW	RW	RW	RW				RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15	BRAKE	VC0 as Advanced Timer brake control ● 0b0: Disable ● 0b1: Enable	RW
14	TIM6	VC0 filter result output to TIM6 capture input CHA enable ● 0b0: Disable ● 0b1: Enable	RW
13	INV_TIM6	VC0 filter result output to TIM6 inverted enable ● 0b0: Disable reverse, the input and VC output are in the same direction ● 0b1: Enable reverse	RW
12	TIM5	VC0 filter result output to TIM5 capture input CHA enable ● 0b0: Disable ● 0b1: Enable	RW
11	INV_TIM5	VC0 filter result output to TIM5 inverted enable ● 0b0: Disable reverse, the input and VC output are in the same direction ● 0b1: Enable reverse	RW
10	TIM4	VC0 filter result output to TIM4 capture input CHA enable ● 0b0: Disable ● 0b1: Enable	RW
9	INV_TIM4	VC0 filter result output to TIM4 inverted enable ● 0b0: Disable reverse, the input and VC output are in the same direction ● 0b1: Enable reverse	RW
8:6	*Reserved*	-	-
5	TIMBK	VC0 filter result output to Timer0/1/2/3 brake control ● 0b0: Disable ● 0b1: Enable	RW

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Bit	Name	Functional Description	Access
4	TIM3RCLR	VC0 filter result output to TIM3 REFCLR enable control ● 0b0: Disable ● 0b1: Enable	RW
3	TIM2RCLR	VC0 filter result output to TIM2 REFCLR enable control ● 0b0: Disable ● 0b1: Enable	RW
2	TIM1RCLR	VC0 filter result output to TIM1 REFCLR enable control ● 0b0: Disable ● 0b1: Enable	RW
1	TIM0RCLR	VC0 filter result output to TIM0 REFCLR enable control ● 0b0: Disable ● 0b1: Enable	RW
0	INV_TIMER	VC0 filter result output inverted to TIM0/1/2/3 ● 0b0: Disable reverse, the input and VC output are in the same direction ● 0b1: Enable reverse	RW

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30.4.6 VC1 Output Configuration Register (VC1_OUT_CFG)

Offset	Bit Position																													
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																BRAKE	TIM6	INV_TIM6	TIM5	INV_TIM5	TIM4	INV_TIM4	Reserved			TIMBK	TIM3RCLR	TIM2RCLR	TIM1RCLR	TIM0RCLR	INV_TIMER
Access																	RW	RW	RW	RW	RW	RW	RW				RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15	BRAKE	VC1 as Advanced Timer brake control ● 0b0: Disable ● 0b1: Enable	RW
14	TIM6	VC1 filter result output to TIM6 capture input CHB enable ● 0b0: Disable ● 0b1: Enable	RW
13	INV_TIM6	VC1 filter result output to TIM6 inverted enable ● 0b0: Disable reverse, the input and VC output are in the same direction ● 0b1: Enable reverse	RW
12	TIM5	VC1 filter result output to TIM5 capture input CHB enable ● 0b0: Disable ● 0b1: Enable	RW
11	INV_TIM5	VC1 filter result output to TIM5 inverted enable ● 0b0: Disable reverse, the input and VC output are in the same direction ● 0b1: Enable reverse	RW
10	TIM4	VC1 filter result output to TIM4 capture input CHB enable ● 0b0: Disable ● 0b1: Enable	RW
9	INV_TIM4	VC1 filter result output to TIM4 inverted enable ● 0b0: Disable reverse, the input and VC output are in the same direction ● 0b1: Enable reverse	RW
8:6	*Reserved*	-	-
5	TIMBK	VC1 filter result output to Timer0/1/2/3 brake control ● 0b0: Disable ● 0b1: Enable	RW

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Bit	Name	Functional Description	Access
4	TIM3RCLR	VC1 filter result output to TIM3 REFCLR enable control ● 0b0: Disable ● 0b1: Enable	RW
3	TIM2RCLR	VC1 filter result output to TIM2 REFCLR enable control ● 0b0: Disable ● 0b1: Enable	RW
2	TIM1RCLR	VC1 filter result output to TIM1 REFCLR enable control ● 0b0: Disable ● 0b1: Enable	RW
1	TIM0RCLR	VC1 filter result output to TIM0 REFCLR enable control ● 0b0: Disable ● 0b1: Enable	RW
0	INV_TIMER	VC1 filter result output inverted to TIM0/1/2/3 ● 0b0: Disable reverse, the input and VC output are in the same direction ● 0b1: Enable reverse	RW

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30.4.7 VC Interrupt Register (VC_IFR)

Offset	Bit Position																													
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																										VC2_FILTER	VC2_INTF	VC1_FILTER	VC0_FILTER	VC1_INTF	VC0_INTF
Access																											RO	RW	RO	RO	RW	RW

Bit	Name	Functional Description	Access
31:6	*Reserved*	-	-
5	VC2_FILTER	Status after VC2 filter	RO
4	VC2_INTF	VC2 interrupt flag Write 0 to clear the interrupt flag, write 1 has no effect. Read: ● 0b0: No interrupt occurred ● 0b1: Interrupt occurred	RW
3	VC1_FILTER	Status after VC1 filter	RO
2	VC0_FILTER	Status after VC0 filter	RO
1	VC1_INTF	VC1 interrupt flag Write 0 to clear the interrupt flag, write 1 has no effect. Read: ● 0b0: No interrupt occurred ● 0b1: Interrupt occurred	RW
0	VC0_INTF	VC0 interrupt flag Write 0 to clear the interrupt flag, write 1 has no effect. Read: ● 0b0: No interrupt occurred ● 0b1: Interrupt occurred	RW

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30.4.8 VC2 Configuration Register (VC2_CR)

Offset	Bit Position																													
0x150	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved															EN	IE	LEVEL	RISING	FALLING	DEBOUNCE_TIME			FLTEN	N_SEL			P_SEL			
Access																RW	RW	RW	RW	RW	RW			RW	RW			RW			

Bit	Name	Functional Description	Access
31:17	*Reserved*	-	-
16	EN	Voltage comparator enable ● 0b0: Disable ● 0b1: Enable	RW
15	IE	VC interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
14	LEVEL	VC output signal triggers interrupt selection ● 0b0: Disable high level trigger INT flag ● 0b1: Enable high level trigger INT flag	RW
13	RISING	VC output signal triggers interrupt selection ● 0b0: Disable rising edge trigger INT flag ● 0b1: Enable rising edge trigger INT flag	RW
12	FALLING	VC output signal triggers interrupt selection ● 0b0: Disable falling edge trigger INT flag ● 0b1: Enable falling edge trigger INT flag	RW
11:9	DE-BOUNCE_TIME	VC output filter time configuration ● 0b000: The filtering time is about 7μs ● 0b001: The filtering time is about 14μs ● 0b010: The filtering time is about 28μs ● 0b011: The filtering time is about 112μs ● 0b100: The filtering time is about 450μs ● 0b101: The filtering time is about 1.8ms ● 0b110: The filtering time is about 7.2ms ● 0b111: The filtering time is about 28.8ms **Note** The filter time configuration is only valid when FLTEN = 0b1.	RW

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Bit	Name	Functional Description	Access
8	FLTEN	VC filter enable ● 0b0: Disable ● 0b1: Enable	RW
7:4	N_SEL	Voltage comparator "-" terminal input selection ● 0b0000: Select channel 0 input PA5 ● 0b0001: Select channel 1 input PB1 ● 0b0010: Select channel 2 input PE11 ● 0b0011: Select channel 3 input PE15 ● 0b0100: Select channel 4 input PB11 ● 0b0101: Select channel 5 input PB14 ● 0b0110: Select channel 6 input PD10 ● 0b0111: Select channel 7 input PD11 ● 0b1000: Select channel 8 input PC7 ● 0b1001: DAC ● 0b1010: DAC ● 0b1011: Resistor voltage dividing output voltage ● 0b1100: Internal temperature sensor output voltage ● 0b1101: Setting prohibited ● 0b1110: ADC's REF (ADC needs to be enabled for use) ● 0b1111: VCAP pin voltage	RW
3:0	P_SEL	Voltage comparator "+" terminal input selection ● 0b0000: Select channel 0 input PA5 ● 0b0001: Select channel 1 input PB1 ● 0b0010: Select channel 2 input PE9 ● 0b0011: Select channel 3 input PE10 ● 0b0100: Select channel 4 input PE11 ● 0b0101: Select channel 5 input PE13 ● 0b0110: Select channel 6 input PE14 ● 0b0111: Select channel 7 input PE15 ● 0b1000: Select channel 8 input PB11 ● 0b1001: Select channel 9 input PB14 ● 0b1010: Select channel 10 input PD9 ● 0b1011: Select channel 11 input PD10 ● 0b1100: Select channel 12 input PD11 ● 0b1101: Select channel 13 input PC7 ● 0b1110: DAC ● 0b1111: DAC	RW

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30.4.9 VC2 Output Configuration Register (VC2_OUT_CFG)

Offset	Bit Position																													
0x154	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																BRAKE	TIM6	INV_TIM6	TIM5	INV_TIM5	TIM4	INV_TIM4	Reserved			TIMBK	TIM3RCLR	TIM2RCLR	TIM1RCLR	TIM0RCLR	INV_TIMER
Access																	RW	RW	RW	RW	RW	RW	RW				RW	RW	RW	RW	RW	RW

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15	BRAKE	VC2 as Advanced Timer brake control ● 0b0: Disable ● 0b1: Enable	RW
14	TIM6	VC2 filter result output to TIM6 capture input CHB enable ● 0b0: Disable ● 0b1: Enable	RW
13	INV_TIM6	VC2 filter result output to TIM6 inverted enable ● 0b0: Disable reverse, the input and VC output are in the same direction ● 0b1: Enable reverse	RW
12	TIM5	VC2 filter result output to TIM5 capture input CHB enable ● 0b0: Disable ● 0b1: Enable	RW
11	INV_TIM5	VC2 filter result output to TIM5 inverted enable ● 0b0: Disable reverse, the input and VC output are in the same direction ● 0b1: Enable reverse	RW
10	TIM4	VC2 filter result output to TIM4 capture input CHB enable ● 0b0: Disable ● 0b1: Enable	RW
9	INV_TIM4	VC2 filter result output to TIM4 inverted enable ● 0b0: Disable reverse, the input and VC output are in the same direction ● 0b1: Enable reverse	RW
8:6	*Reserved*	-	-
5	TIMBK	VC2 filter result output to Timer0/1/2/3 brake control ● 0b0: Disable ● 0b1: Enable	RW

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Bit	Name	Functional Description	Access
4	TIM3RCLR	VC2 filter result output to TIM3 REFCLR enable control ● 0b0: Disable ● 0b1: Enable	RW
3	TIM2RCLR	VC2 filter result output to TIM2 REFCLR enable control ● 0b0: Disable ● 0b1: Enable	RW
2	TIM1RCLR	VC2 filter result output to TIM1 REFCLR enable control ● 0b0: Disable ● 0b1: Enable	RW
1	TIM0RCLR	VC2 filter result output to TIM0 REFCLR enable control ● 0b0: Disable ● 0b1: Enable	RW
0	INV_TIMER	VC2 filter result output inverted to TIM0/1/2/3 ● 0b0: Disable reverse, the input and VC output are in the same direction ● 0b1: Enable reverse	RW

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31 LVD

31.1 Introduction

LVD can be used to monitor the voltage of VCC and chip pins. When the comparison result of the monitored voltage and the LVD threshold meets the trigger condition, the LVD will generate an interrupt or reset signal, and the user can perform some urgent tasks according to the signal.

31.2 Features

- 4 monitoring sources: AVCC, PC13, PB08, PB07
- 16-stage threshold voltage, 1.8-3.3V optional
- 8 trigger conditions, combinations of high level, rising edge and falling edge
- 2 trigger results: reset and interrupt
- 8-stage filter configuration to prevent false triggering
- With hysteresis function, strong anti-interference

31.3 Functional Description

31.3.1 LVD Block Diagram

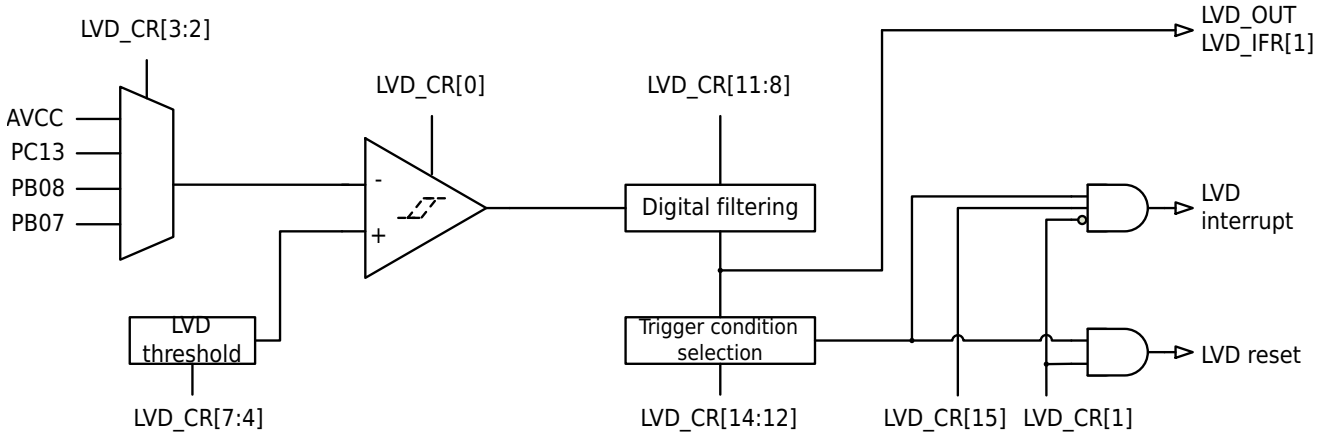

Figure 31-1 LVD Block Diagram

31.3.2 Digital Filtering

If the working environment of the chip is bad, the output of the hysteresis comparator will appear noise signal. The noise signal whose pulse width is less than LVD_CR.DEBOUNCE_TIME in the output waveform of the hysteresis comparator can be filtered out. If the digital filter module is disabled, the input and output signals of the digital filter module are the same.

The digitally filtered signal level can be read from the register LVD_IFR[1]; when the GPIO function is configured as LVD_OUT, the digitally filtered signal can be output from the GPIO for easy measurement.

Enable the digital filter module, the filter illustration is as follows:

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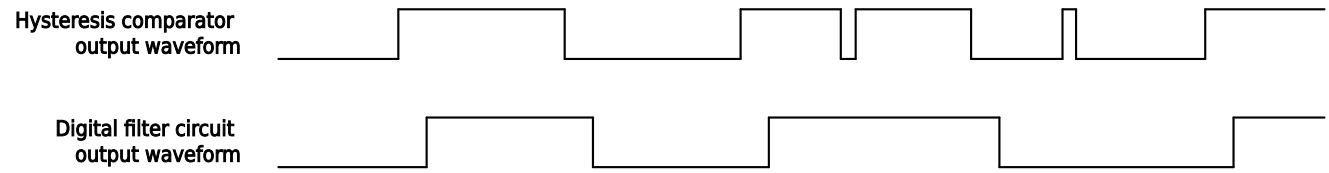

Figure 31-2 LVD Filter Output

31.3.3 Hysteresis Function

The built-in voltage comparator of LVD has a hysteresis function, which can enhance the anti-interference ability of the chip. The output signal of LVD will not flip until the input signal is higher or lower than the threshold voltage by the hysteresis voltage/2. The input and output signal diagram of LVD is as follows:

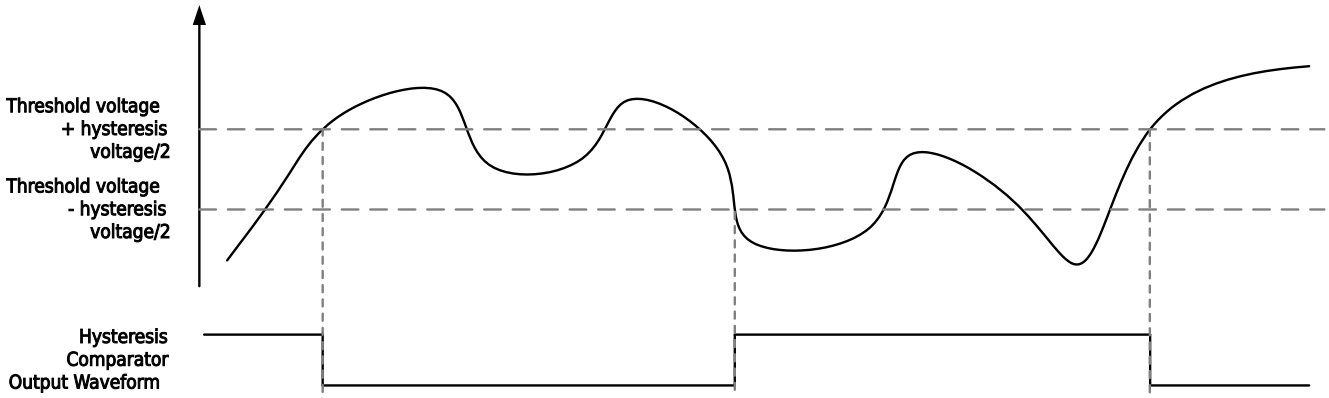

Figure 31-3 LVD Hysteresis Response

31.4 Operation Example

31.4.1 LVD Configured as Low Voltage Reset

Context

In this mode, the MCU is reset when the monitored voltage is lower than the threshold voltage.

Procedure

Step1. Configure LVD_CR.SOURCE_SEL to select the voltage source to be monitored.

Step2. Configure LVD_CR.VTDS to select the threshold voltage of LVD.

Step3. Configure LVD_CR.DEBOUNCE_TIME to select the LVD filter time.

Step4. Set LVD_CR.FLTEN to enable LVD filtering.

Step5. Set LVD_CR.HTEN to 1, select high level to trigger LVD action.

Step6. Set LVD_CR.ACT to 1, select LVD action as reset.

Step7. Set LVD_CR.LVDEN to 1 to enable LVD.

31.4.2 LVD Configured as Voltage Change Interrupt

Context

In this mode, an interrupt is generated when the monitored voltage goes above or below the threshold voltage.

Procedure

Step1. Configure LVD_CR.SOURCE_SEL to select the voltage source to be monitored.

Step2. Configure LVD_CR.VTDS to select the threshold voltage of LVD.

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Step3. Configure LVD_CR.DEBOUNCE_TIME to select the LVD filter time.

Step4. Set LVD_CR.FLTEN to enable LVD filtering.

Step5. Set LVD_CR.RTEN and LVD_CR.FTEN to 1, select level change to trigger LVD action.

Step6. Set LVD_CR.ACT to 0, select LVD action as interrupt.

Step7. Set LVD_CR.IE to 1 to enable LVD interrupt.

Step8. Enable the LVD interrupt in the NVIC interrupt vector table.

Step9. Set LVD_CR.LVDEN to 1 to enable LVD.

Step10. Execute the operations required by the user in the LVD interrupt service routine; write 0x00 to LVD_IFR to clear the interrupt flag before exiting the interrupt service routine.

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31.5 Register Description

31.5.1 Register List

Base address: 0x40002400

Table 31-1 Low Voltage Detector (LVD) Register Offset

Offset	Register	Description	Width
0x028	LVD_CR	LVD Configuration Register	32
0x02C	LVD_IFR	LVD Interrupt Flag Register	32

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31.5.2 LVD Configuration Register (LVD_CR)

Offset	Bit Position																													
0x028	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																IE	HTEN	RTEN	FTEN	DEBOUNCE_TIME			FLTEN	VTDS			SOURCE_SEL		ACT	LVDEN
Access																	RW	RW	RW	RW	RW			RW	RW			RW		RW	RW

Bit	Name	Functional Description	Access
31:16	*Reserved*	-	-
15	IE	LVD interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
14	HTEN	High level trigger enable The monitored voltage is lower than the threshold voltage ● 0b0: Disable ● 0b1: Enable	RW
13	RTEN	Rising edge trigger enable The monitored voltage changes from above the threshold voltage to below the threshold voltage ● 0b0: Disable ● 0b1: Enable	RW
12	FTEN	Falling edge trigger enable The monitored voltage changes from below the threshold voltage to above the threshold voltage ● 0b0: Disable ● 0b1: Enable	RW
11:9	DE-BOUNCE_TIME	Digital filter time configuration ● 0b000: The filtering time is about 7μs ● 0b001: The filtering time is about 14μs ● 0b010: The filtering time is about 28μs ● 0b011: The filtering time is about 112μs ● 0b100: The filtering time is about 450μs ● 0b101: The filtering time is about 1.8ms ● 0b110: The filtering time is about 7.2ms ● 0b111: The filtering time is about 28.8ms **Note** The filter time configuration is only valid when FLTEN = 0b1.	RW

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Bit	Name	Functional Description	Access
8	FLTEN	Digital filtering enable ● 0b0: Disable ● 0b1: Enable	RW
7:4	VTDS	LVD threshold voltage selection ● 0b0000: 1.8V ● 0b0001: 1.9V ● 0b0010: 2.0V ● 0b0011: 2.1V ● 0b0100: 2.2V ● 0b0101: 2.3V ● 0b0110: 2.4V ● 0b0111: 2.5V ● 0b1000: 2.6V ● 0b1001: 2.7V ● 0b1010: 2.8V ● 0b1011: 2.9V ● 0b1100: 3.0V ● 0b1101: 3.1V ● 0b1110: 3.2V ● 0b1111: 3.3V	RW
3:2	SOURCE_SEL	LVD monitoring source selection ● 0b00: AVCC power voltage ● 0b01: PC13 port input voltage ● 0b10: PB08 port input voltage ● 0b11: PB07 port input voltage	RW
1	ACT	LVD trigger action selection ● 0b0: NVIC interrupt ● 0b1: System reset	RW
0	LVDEN	LVD enable control ● 0b0: Disable ● 0b1: Enable	RW

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31.5.3 LVD Interrupt Flag Register (LVD_IFR)

Offset	Bit Position																													
0x02C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																														FILTER	INTF
Access																															RO	RW

Bit	Name	Functional Description	Access
31:2	*Reserved*	-	-
1	FILTER	Level value of digital filter output ● 0b0: Digital filter output low level ● 0b1: Digital filter output high level	RO
0	INTF	LVD interrupt flag Write 0 to clear the interrupt flag, write 1 has no effect. Read: ● 0b0: No interrupt occurred ● 0b1: Interrupt occurred	RW

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32 OPA

32.1 Introduction

This product has a built-in general-purpose operational amplifier OPA, which is suitable for simple voltage amplification and voltage follower applications. Its output can be flexibly configured to several different pins. The OPA can also be configured as an output follower of a DAC to enhance the drive capability of the DAC output signal.

32.2 Features

- 1 independent operational amplifiers
- Input voltage range: 0.2V to AVCC-0.2V
- Output voltage range: 0.2V to AVCC-0.2V
- Output signal pins: OPA_OUT0 to OPA_OUT4
- Two working modes: General purpose OPA, DAC output follower mode

32.3 Functional Description

32.3.1 General-Purpose Operational Amplifier Mode

When OPA_CR0. OPA_EN is 1 and OPA_CR0.OPABUFEN is 0, OPA works in general operational amplifier mode, and can realize various functions of general operational amplifier with external circuits. OPA has 5 output ports in this mode, 4 of which can be closed. OPA_OUT0 is directly connected to the port of this product, which has the highest driving capability; OPA_OUT1 - OPA_OUT4 is connected to the port of this product after passing a program-controlled switch, with an internal resistance of several hundred ohms. The block diagram in this mode is as follows:

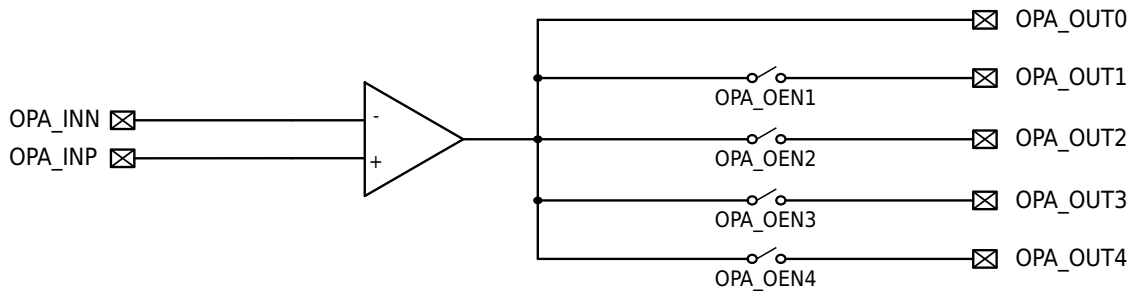

Figure 32-1 OPA General-Purpose Operational Amplifier Mode Block Diagram

32.3.2 DAC Output Follower Mode

When OPA_CR0. OPA_EN is 0 and OPA_CR0.OPABUFEN is 1, OPA works in DAC voltage follower mode, which is used to enhance the output capability of DAC. The block diagram in this mode is as follows:

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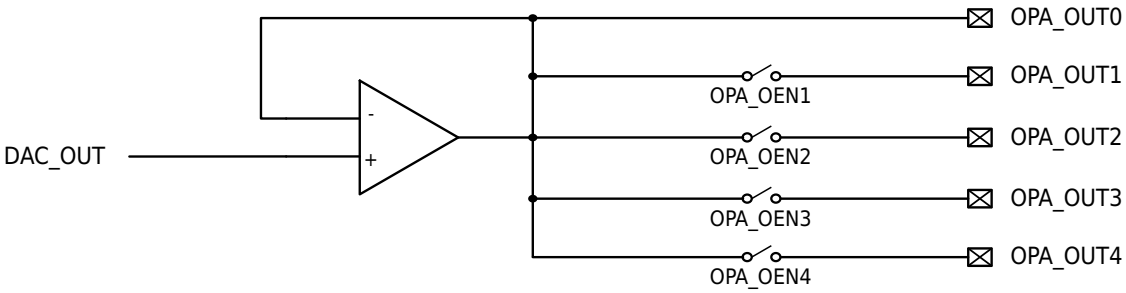

Figure 32-2 OPA DAC Output Follower Mode Block Diagram

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32.4 Register Description

32.4.1 Register List

Base address: 0x40002430

Table 32-1 Operational Amplifier (OPA) Register Offset

Offset	Register	Description	Width
0x00	OPA_CR0	OPA Configuration Register	32

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32.4.2 OPA Configuration Register (OPA_CR0)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000180																															
Name	Reserved																						BIASSEL			OEN4	OEN3	OEN2	OEN1	BUFEN	Reserved	EN
Access																							RW			RW	RW	RW	RW	RW		RW

Bit	Name	Functional Description	Access
31:10	*Reserved*	-	-
9:7	BIASSEL	Debug Control Bit Must retain the default value	RW
6	OEN4	OPA_OUT4 output enable control ● 0b0: OPA_OUT4 is disconnected from the OPA output signal ● 0b1: OPA_OUT4 is connected to the OPA output signal	RW
5	OEN3	OPA_OUT3 output enable control ● 0b0: OPA_OUT3 is disconnected from the OPA output signal ● 0b1: OPA_OUT3 is connected to the OPA output signal	RW
4	OEN2	OPA_OUT2 output enable control ● 0b0: OPA_OUT2 is disconnected from the OPA output signal ● 0b1: OPA_OUT2 is connected to the OPA output signal	RW
3	OEN1	OPA_OUT1 output enable control ● 0b0: OPA_OUT1 is disconnected from the OPA output signal ● 0b1: OPA_OUT1 is connected to the OPA output signal	RW
2	BUFEN	DAC output follower mode control ● 0b0: Disable ● 0b1: Enable	RW
1	*Reserved*	-	-
0	EN	General purpose OPA Mode Enable Control ● 0b0: Disable ● 0b1: Enable	RW

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33 Other Analog Registers

33.1 Register List

Base address: 0x40002400

Table 33-1 Other Analog Registers Offset

Offset	Register	Description	Width
0x000	BGR_CR	BGR Control Register	32

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33.2 BGR Control Register (BGR_CR)

Offset	Bit Position																													
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved																														TS_EN	BGR_EN
Access																															RW	RW

Bit	Name	Functional Description	Access
31:2	*Reserved*	-	-
1	TS_EN	Built-in temperature sensor enable control ● 0b0: Disable internal temperature sensor ● 0b1: Enable internal temperature sensor, and BGR must be enabled **Note** After the temperature sensor is enabled for 20μs, it can output a stable signal.	RW
0	BGR_EN	BGR enable control ● 0b0: Disable BGR ● 0b1: Enable BGR **Note** ● This register can only be operated when PERI_CLKEN0.ADC is 1. ● The BGR outputs a stable high-precision reference voltage only after the $T_{stable\ (BGR)}$ time is enabled (for specific values, see the "Electrical Specifications Operating Conditions Internal Reference Voltage" section in the *Datasheet*). After the BGR is stable, it can be used by other modules, so the steps of waiting for the BGR to be stable should be added in the user operation. ● When using ADC/OPA/PLL, the BGR must be enabled. ● When using VC, it is necessary to decide whether to enable BGR according to the configuration of the VC register.	RW

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34 SWD Debug Interface

34.1 Introduction

This series of products uses an ARM Cortex-M0+ core, which features a hardware debugging module SWD that supports complex debugging operations. The hardware debug module allows the core to stop when fetching instructions (instruction breakpoints) or accessing data (data breakpoints). When the core is stopped, both the internal state of the core and the external state of the system can be queried in the IDE. After the query is complete, the core and peripherals can be restored and program execution continues. When this series of MCUs are connected to a debugger and start debugging, the debugger will use the hardware debugging module of the core to perform debugging operations.

Note

SWD can wake up DeepSleep, please be careful not to disconnect the SWD interface as the state of Deep-Sleep.

34.2 Functional Description

34.2.1 Debug System Diagram

This product uses an ARM Cortex-M0+ core and includes hardware extensions for advanced debugging function; therefore, the debugging function of this product are consistent with Cortex-M0+. Debug extensions allow the core to halt the core when fetching instructions (instruction breakpoints) or fetching accessing data (data breakpoints). When the core stops, you can query the internal state of the core and the external state of the system. After querying, the core and system are resumed, and program execution is restored.

When the debug host is connected to the MCU and debugged, the debug function will be used.

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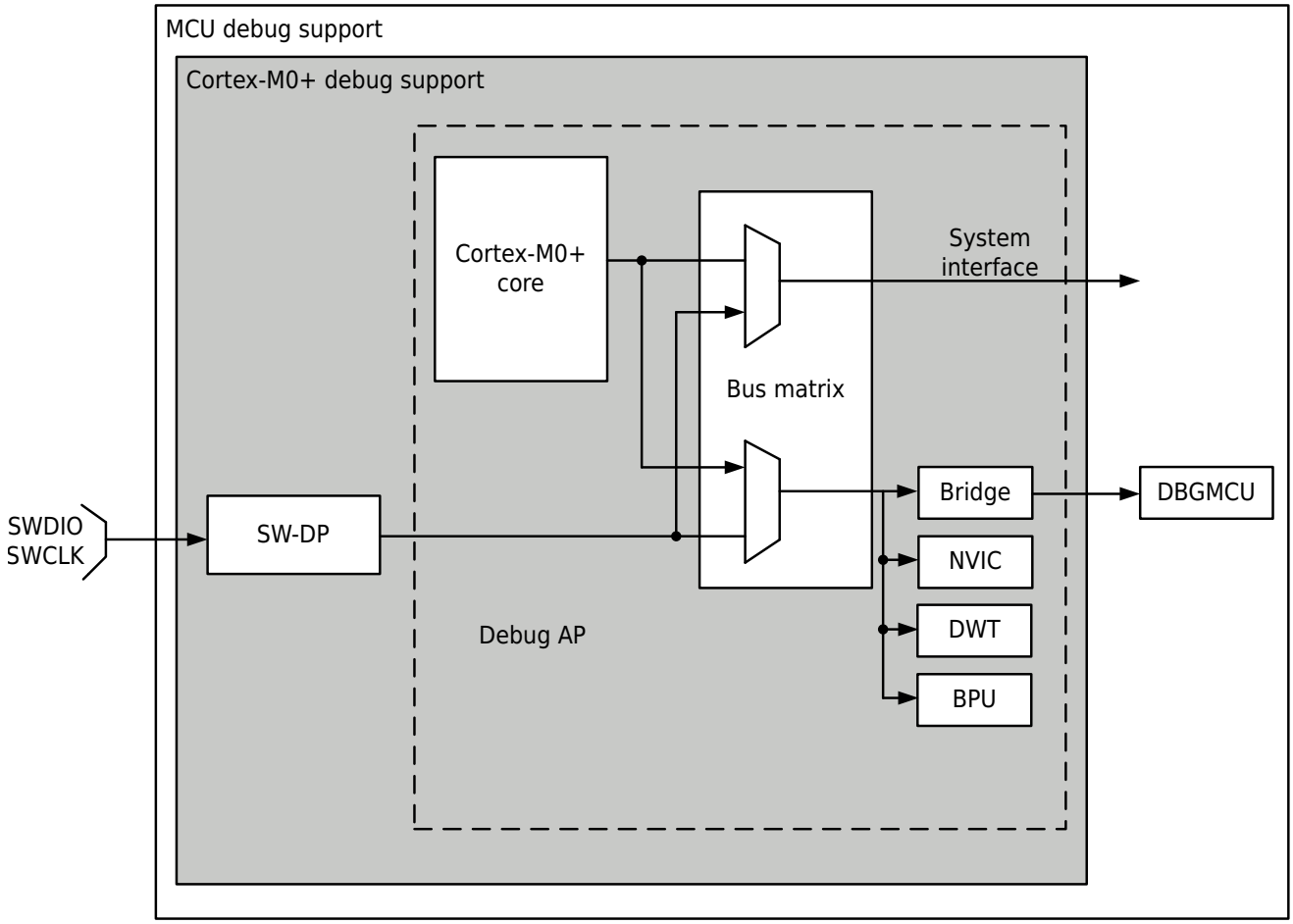

Figure 34-1 Debug Support Block Diagram

The built-in debugging function in the Cortex-M0+ core are part of the ARM® CoreSight design suite.

ARM® Cortex-M0+ core provides integrated on-chip debugging support, including:

- SW-DP: Serial line
- BPU: Breakpoint unit
- DWT: Data watchpoint trigger

Note

For detailed information on the debugging function supported by the ARM® Cortex-M0+ core, see "Cortex-M0+ Technical Reference Manual".

34.2.2 ARM® Reference Documentation

- Cortex-M0+ Technical Reference Manual (TRM)
  Available at developer.arm.com.
- ARM® debug interface V5
- ARM® CoreSight Design Suite Version r1p1 Technical Reference Manual
- ARMv6-M Architecture Reference Manual

34.2.3 Debug Port Pins

SWD Port Pins

The SWD interface of this series requires 2 pins, as shown in the table below.

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SWD Port Name	Debugging Function	Pin Assignment
SWCLK	Serial clock	PA14
SWDIO	Serial data input/output	PA13

SW-DP Pin Assignment

If the [Encryption Chip] option is enabled when programming the program, the SWD debugging function will be disabled after power-on. If the [Encryption Chip] option is not enabled during programming, the PA13/PA14 pins will be initialized as dedicated pins for debugger use after power-on. Users can set SYSCTRL1.SWD_USE_IO register to disable the SWD pin debugging function, and the SWD pin will be released to be used as a normal GPIO. The configuration and function of SWD pins are summarized in the following table:

[Encryption Chip] Option	SWD_USE_IO Configuration	PA13/PA14 Function
Encryption	0	-
Encryption	1	GPIO
No encryption	0	SWD
No encryption	1	GPIO

Internal Pull-Up on SWD Pins

After the user software releases the SW I/O, the GPIO controller takes control of these pins. The reset state of the GPIO control register will put the I/O into the equivalent state:

- SWDIO: input pull-up
- SWCLK: input pull-up

No external resistors need to be added due to built-in pull-up and pull-down resistors.

34.2.4 SWD Port

34.2.4.1 Introduction to SWD Protocol

This synchronous serial protocol uses two pins:

- SWCLK: Clock from host to target
- SWDIO: Bidirectional

Using this protocol, two register sets (DPACC register set and APACC register set) can be read and written simultaneously. LSB is ahead when transferring data.

For SWDIO bidirectional management, the line must be pulled up on the circuit board (ARM® recommends using 100k). These pull-up resistors can be configured internally, so external pull-up resistors are not required.

Every time the SWDIO direction is changed in the protocol, the conversion time is inserted, and the line is not driven by the host or the target. By default, this conversion time is one bit time, but can be adjusted by configuring the SWCLK frequency.

34.2.4.2 SWD Protocol Sequence

Each sequence consists of three phases:

1. Host transmitted data packet request (8-bit)

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2. Target transmitted acknowledgment response (3-bit)
3. Data transfer phase transmitted by host or target (33-bit)

Table 34-3 Host Transmitted Data Packet Request

Bit	Name	Description
0	Start	Must be 0b1
1	APnDP	● 0b0: DP access ● 0b1: AP access
2	RnW	● 0b0: Write request ● 0b1: Read request
4:3	A[3:2]	Address field of DP or AP register
5	Parity check	Unit parity for the first few bits
6	Stop	0b0
7	Reside	Not driven by the host. Due to the presence of the pull-up, the target must read it as 0b1.

For detailed information on the DPACC and APACC registers, please refer to "Cortex-M0+ Technical Reference Manual".

The packet request is always followed by a conversion time (1 bit by default), at which point neither the host nor the target will drive.

Table 34-4 Target Transmitted Acknowledgment Response

Bit	Name	Description
2:0	ACK	● 0b001: FAULT ● 0b010: WAIT ● 0b100: OK

The ACK response must be followed by conversion time only when a READ transaction occurs or a WAIT or FAULT acknowledgment is received.

Table 34-5 Data Transfers Transmitted by Host or Target

Bit	Name	Description
31:0	WDATA or RDATA	Write or read data
32	Parity check	Single parity for 32 data bits

The conversion time must be after the DATA transfer only when a READ transaction occurs.

34.2.4.3 SW-DP State Machine (Reset, Idle State, ID Code)

The SW-DP state machine includes an internal ID code to identify the SW-DP. This code complies with the JEP-106 standard and is set to the default ARM® code **0x0BC11477** (which corresponds to the Cortex®-M0+).

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Note

The SW-DP state machine is inactive until the target reads the ID code.

- The SW-DP state machine is in reset state after power-on reset or after the line has been at high level for more than 50 cycles.
- If the line is low for at least two cycles after the reset state, the SW-DP state machine is in the idle state.
- After the reset state, the state machine must first enter the idle state and then perform a read access to the DP-SW ID CODE register. FAULT acknowledgment response on another transaction.

For more detailed information about the SW-DP state machine, please refer to "Cortex-M0+ Technical Reference Manual" and "ARM® CoreSight Design Suite Version r1p1 Technical Reference Manual".

34.2.4.4 DP and AP Read/Write Access

- Read access to DP is not delayed: the target response can be sent immediately (if ACK=OK) or delayed (if ACK=WAIT).
- Delay read access to AP. This means that access results will be returned on the next transfer. If the next access to be performed is not an AP access, the DP-RDBUFF register must be read to obtain the result.
- Every time an AP read access or RDBUFF read request is made, the READOK flag of the DP-CTRL/STAT register will be updated to know whether the AP read access is successful.
- SW-DP has a write buffer (for DP or AP writes) so that write operations can be accepted even while other operations are still pending. If the write buffer is full, the target acknowledgment response is WAIT. Except for IDCODE read, CTRL/STAT read or ABORT write, these operations will also be accepted when the write buffer is full.
- Due to the asynchronous clock domains SWCLK and HCLK, two additional SWCLK cycles are required after the write operation (after the parity bit) for the write operation to take effect internally. These cycles should be applied while the line is being driven low (idle state).

This is especially important when writing to the CTRL/STAT register to initiate a power-on request. Otherwise the next operation (one that is only valid after the core is powered on) will be executed immediately, which will cause a failure.

34.2.4.5 SW-DP Register

These registers can be accessed when APnDP=0:

A[3:2]	RW	CTRLSEL Bit of the SELECT Register	Register	Description
0b00	Read	-	IDCODE	The manufacturer code is set to the default ARM® code for Cortex®-M0+. **0x0BC11477** (identifies SW-DP)
0b00	Write	-	ABORT	-
0b01	Read/ write	0	DP-CTRL/STAT	Purpose: ● Request system or debug power-on ● Configure transport operations for AP access ● Control compare and verify operations ● Read some status flags (overflow and power-on acknowledgment)

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A[3:2]	RW	CTRLSEL Bit of the SELECT Register	Register	Description
0b01	Read/ write	1	WIRE CON-TROL	Used to configure the physical serial port protocol (such as switching time duration)
0b10	Read	-	READ RESEND	Allow recovery of reads data from corrupt-ed debug software transfers without re-peating the original AP transmission.
0b10	Write	-	SELECT	4-word register window used to select the currently accessed port and active
0b11	Read/ write	-	READ BUFFER	Since an AP access has been issued, this read buffer is very useful (it provides the result of the AP read request during the execution of the next AP transaction). This read buffer captures data from the AP and displays the result of the previous read without requiring a new operation to be initiated

34.2.4.6 SW-AP Register

These registers can be accessed when APnDP=1:

There are multiple AP registers, which are addressed in the following combinations:

- Shift value A[3:2]
- Current value of DP SELECT register

Address	A[3:2] Value	Description
0x0	0b00	Reserved, must be kept at the reset value.
0x4	0b01	DP CTRL/STAT register. Used for: ● Request system or debug power-on ● Configure transport operations for AP access ● Control compare and verify operations ● Read some status flags (overflow and power-on ac-knowledgment)
0x8	0b10	DP SELECT register: used to select the currently accessed port and active 4-word register window. ● Bit[31:24]: APSEL, select the current AP ● Bit[23:8]: Reserved ● Bit[7:4]: APBANKSEL, select the active 4-word register window within the current AP ● Bit[3:0]: Reserved
0xC	0b11	DP RDBUFF Register: Used by the debugger to retrieve the final result after performing a series of operations (without initiating a new JTAG-DP request).

34.2.5 Core Debugging

Debug the core through the core debug registers. Debug access to these registers is through the debug access port. It consists of four registers:

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Register	Description
DHCSR	32-bit debug stop control and status register This register provides information about the state of the processor, enables the core to enter a debug stop state, and provides processor stepping capabilities.
DCRSR	17-bit debug core register selector registers This register selects the processor register to be read or written.
DCRDR	32-bit debug core register data registers This register holds data read and written between the register and the processor selected by the DCRSR (selector) register.
DEMCR	32 -bit debug exception and monitor control registers This register provides vector capture and debug monitor control.

These registers are not reset on system reset. They can only be reset by a power-on reset. For more information, see "Cortex-M0+ Technical Reference Manual".

In order to put the core into the debug stop state immediately after reset, it is necessary to:

- Enable Debug and Exception Monitoring Control Register bit 0 (VC_CORRESET)
- Enable Debug Halt Control and Status Register bit 0 (C_DEBUGEN)

34.2.6 BPU (Breakpoint Unit)

Cortex-M0+ BPU implementation provides 4 breakpoint registers.

Processor breakpoint implements PC-based breakpoint functionality.

For more information about the BPU CoreSight identification registers, including their addresses and access types, please see "ARMv6-M Architecture Reference Manual" and "ARM® CoreSight Component Technical Reference Manual".

34.2.7 DWT (Data Watchpoint)

The Cortex-M0+ DWT implementation provides 2 watchpoint register groups.

DWT Function

The processor watchpoint implements data address and PC-based watchpoint functions (i.e., PC sampling registers) and includes comparator address masking. For detailed information, please refer to the "ARMv6-M Architecture Reference Manual".

DWT Program Counter Sampling Register

Processors implementing the data watchpoint unit also implement the ARMv6-M optional DWT Program Counter Sampling Register (DWT_PCSR). This register allows the debugger to periodically sample the PC without stopping the processor, enabling coarse-grained analysis. For more information, see "ARMv6-M Architecture Reference Manual".

Cortex-M0+ DWT_PCSR records instructions that pass condition codes as well as instructions that do not pass condition codes.

34.2.8 MCU Debug Component (DBG)

MCU debug component helps the debugger provide support for:

- Low power mode
- Timer and watchdog clock control during breakpoints

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Debug Support for Low Power Mode

To enter low power mode, the instruction WFI or WFE must be executed.

The MCU supports several low power modes that disable the CPU clock or reduce CPU power consumption.

The core does not allow FCLK or HCLK to be turned off during a debugging session. They must remain active as they are required for debug connections during debugging. The MCU incorporates special methods that allow users to debug software in low power mode.

Debug Support for Timer and Watchdog

During a breakpoint, the behavior of the counters of the timer and watchdog must be selected:

- The counter continues to count while the breakpoint is generated. This method is required when using PWM to control motors.
- The counter stops to count while the breakpoint is generated. This method is required when using the watchdog.

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35 Device Electronic Signature

35.1 Introduction

The electronic signature is stored in the system storage area of the flash memory module and can be read by SWD or CPU. The chip identification information is programmed during manufacturing. User firmware or external devices can read the electronic signature to automatically match MCUs with different configurations.

35.2 Functional Description

35.2.1 Product Unique Identifier (UID)

Typical application scenarios for unique identifier (UID):

- Used as a serial number
- UID is used as a security key when used in conjunction with software cryptographic primitives and protocols to increase the security of code in Flash prior to programming the internal Flash
- Activation of the secure bootstrap process, etc.

The UID provides a reference number that is unique to any device and in any context. The user can never change these bits. The UID can also be read in different ways like single byte/halfword/word and then concatenated using a custom algorithm.

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35.3 Register Description

35.3.1 Product Unique Identifier (UID) Register (80 bits)

Base address: 0x00101E94

Offset	Description	UID Bits (80bits)							
		7	6	5	4	3	2	1	0
0	Y Coordinate on the wafer	UID[7:0]							
1	X Coordinate on the wafer	UID[15:8]							
2	Wafer Number	UID[23:16]							
3	Lot Number	UID[31:24]							
4		UID[39:32]							
5		UID[47:40]							
6		UID[55:48]							
7		UID[63:56]							
8		UID[71:64]							
9		UID[79:72]							

35.3.2 Product Model Register

0x00101B40-0x00101B4F store the ASCII code representing the product model. If the product model is less than 16 bytes, fill it with 0x00.

Example: The product model represented by 484333324C3136364D43544100000000 is HC32L166MCTA.

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35.3.3 FLASH Capacity Register

Base address: 0x00101B60

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	-																															
Name	FLASHSIZE																															
Access	RO																															

Bit	Name	Functional Description	Access
31:0	FLASHSIZE	Product built-in Flash capacity In unit of Byte 0x00020000 means the Flash capacity is 128K Byte	RO

35.3.4 RAM Capacity Register

Base address: 0x00101B64

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	-																															
Name	RAMSIZE																															
Access	RO																															

Bit	Name	Functional Description	Access
31:0	RAMSIZE	Product built-in RAM capacity In unit of Byte 0x00004000 means the RAM capacity is 16K Byte 0x00008000 means the RAM capacity is 32K Byte	RO

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35.3.5 Pin Count/Flash Sector Size Configuration Register

Base address: 0x00101B68

Offset	Bit Position																													
-	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	-																															
Name	PINCOUNT																FLASHSECTORSIZE															
Access	RO																RO															

Bit	Name	Functional Description	Access
31:16	PINCOUNT	Product pins count 0x0020 means the number of product pins is 32 0x0030 means the number of product pins is 48 0x0050 means the number of product pins is 80	RO
15:0	FLASHSEC-TORSIZE	Flash sector size In unit of Byte 0x0200 represents 512Byte.	RO

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36 SysTick Timer

36.1 Introduction

If the OS wants to support multitasking, it needs to perform context switching periodically, so hardware resources such as timers are needed to interrupt program execution. When the timer interrupt is generated, the processor will perform OS task scheduling in exception handling, and will also perform OS maintenance work at the same time. The Cortex-M0+ processor includes a simple timer called SysTick, which is used to generate periodic interrupt requests.

SysTick is a 24-bit timer and counts down. After the count of the timer is reduced to 0, a programmable value will be reloaded, and a SysTick exception (exception number 15) will be generated at the same time. This abnormal event will cause the execution of SysTick exception handling, which is a part of the OS.

For systems that do not require an OS, the SysTick timer can also be used for other purposes, such as timing, time-counting, or providing an interrupt source for tasks that need to be executed periodically. The generation of SysTick exception is controllable. If the exception is disabled, the SysTick timer can still be used by polling, such as checking the current count value or polling the count flag.

36.2 Operation Example

36.2.1 Set SysTick

Context

Since the reload value and current value of the SysTick timer are undefined at reset, in order to prevent abnormal results, the configuration of SysTick needs to follow a certain process.

Procedure

Step1. Configure SysTick->CTRL.ENABLE to 0, disable SysTick.

Step2. Configure SysTick->CTRL.CLKSOURCE to select the clock source of SysTick.

Step3. Configure SysTick->LOAD, select the overflow period of SysTick.

Step4. Writing any value to SysTick->VAL, clear both SysTick->VAL and the SysTick->CTRL.COUNTFLAG.

Step5. Configure SysTick->CTRL.TICKINT to 1, enable SysTick interrupt.

Step6. Configure SysTick->CTRL.ENABLE to 1, enable SysTick.

Step7. Read SysTick->CTRL in the interrupt service routine to clear the overflow flag.
The SysTick overflow period is SysTick->LOAD + 1. The configuration example is as follows:

Clock Source	SysTick->LOAD	Overflow Period
HCLK 4MHz	3999	1ms
XTL 32.768kHz	327	10.01ms

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36.3 Register Description

36.3.1 Register List

Base address: 0xE000E010

Table 36-2 SysTick Timer Register Offset

Offset	Register	CMSIS Symbol	Description	Width
0x00	SYS_CSR	SysTick->CTRL	SysTick Control and Status Register	32
0x04	SYS_RVR	SysTick->LOAD	SysTick Reload Register	32
0x08	SYS_CVR	SysTick->VAL	SysTick Current Value Register	32
0x0C	SYS_CALIR	SysTick->CALIB	SysTick Calibration Value Register	32

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36.3.2 SysTick Control and Status Register (CTRL)

Offset	Bit Position																													
0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x00000000																															
Name	Reserved															COUNTFLAG	Reserved													CLKSOURCE	TICKINT	ENABLE
Access																RO														RW	RW	RW

Bit	Name	Functional Description	Access
31:17	*Reserved*	-	-
16	COUNTFLAG	SysTick timer overflow flag Reading this register can clear COUNTFLAG flag ● 0b0: SysTick timer has not overflowed ● 0b1: SysTick timer has underflowed	RO
15:3	*Reserved*	-	-
2	CLKSOURCE	SysTick clock source selection ● 0b0: Use reference clock (XTL) ● 0b1: Use core clock (HCLK) **Note** When the reference clock is selected as the SysTick clock source, the XTL clock source and the SYSCTRL module register PERI_CLKEN0.TICK must be enabled synchronously.	RW
1	TICKINT	SysTick interrupt enable ● 0b0: Disable ● 0b1: Enable	RW
0	ENABLE	SysTick timer enable ● 0b0: Disable ● 0b1: Enable	RW

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36.3.3 SysTick Reload Register (LOAD)

Offset	Bit Position																													
0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	Reserved																RELOAD															
Access																	RW															

Bit	Name	Functional Description	Access
31:24	*Reserved*	-	-
23:0	RELOAD	SysTick timer reload value	RW

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36.3.4 SysTick Current Value Register (VAL)

Offset	Bit Position																													
0x08	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	Reserved																CURRENT															
Access																	RW															

Bit	Name	Functional Description	Access
31:24	*Reserved*	-	-
23:0	CURRENT	Current count value of the SysTick timer Read the register to obtain the current count value of the SysTick timer. Writing any value to the register will clear both the register itself and the COUNTFLAG.	RW

36.3.5 SysTick Calibration Value Register (CALIB)

Offset	Bit Position																													
0x0C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xXXXXXXXX																															
Name	NOREF	SKEW	Reserved														TENMS															
Access	RO	RO															RO															

Bit	Name	Functional Description	Access
31	NOREF	Whether the SysTick count clock supports the reference clock flag ● 0b0: Support reference clock (XTL) ● 0b1: Does not support reference clock (XTL) **Note** When this bit is set to 1, CTRL.CLKSOURCE must be set to 1.	RO
30	SKEW	TENMS accuracy indication ● 0b0: TENMS value represents an exact 10ms ● 0b1: TENMS value represents an approximate 10ms	RO
29:24	*Reserved*	-	-
23:0	TENMS	10 millisecond calibration value	RO

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A Glossary

Terminology	Full Name	description
Byte	-	Bytes, 8-bit data
Half Word	-	Half word, 16-bit data
Word	-	Words, 32-bit data
Double Word	-	Double word, 64 -bit data.
IAP	-	It refers to reprogram the MCU's Flash during the running of a user program (programming in the application).
ICP	-	It means that the MCU's Flash of the MCU can be programmed by using JTAG protocol, SWD protocol or bootstrap program when the device is installed on the user application circuit board (in-circuit/online programming).
AHB	Advanced High-performance Bus	Advanced High-Performance Bus
APB	Advanced Peripheral Bus	Advanced peripheral bus
DMA	Direct Memory Access	Direct memory access
TIM/TMR	-	Timer

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Revision History

Revision/Date	Changes
Rev1.30 Aug. 28, 2026	1. UART: In the "Multi-Machine Communication" chapter, the description is optimized. 2. LPUART: In the "Multi-Machine Communication" chapter, the description of Slave Address Configuration is optimized. 3. TIM0/1/2/3: In the "Mode2/3 Compare Capture Mode - Capture Input" chapter, the capture input description of CH0B is optimized. When MSCR.IB0S is configured to 1, MSCR.TS does not support selecting the CH0B filter signal. 4. SWD Debug Interface: The internal ID of SW-DP is modified to "0x0BC11477".
Rev1.20 Feb. 12, 2026	1. SYSCTRL: In the "PLL Control Register (PLL_CR)" chapter, Bit[12:11]'s and Bit[10:9]'s functional description is updated from "Recommended to retain the default value" to "Must retain the default value"; In the "Reset Flag Register (RESET_FLAG)" chapter, add note "The reset value is 0x03 at power-on reset. After the program determines the reset source, it should clear the register so that it can determine the reset source the next time a reset occurs", simultaneously optimize the functional descriptions of each bit. 2. FLASH: In the "FLASH Security Protection" chapter, the Read-only FLASH_LOCK_ST register is removed from "Registers Can Be Changed After a Write Sequence" list. 3. TIM0/1/2/3: In the "Mode 0 Counting Timer Function" chapter, the GATEP polarity in the functional block diagram is modified, counting function description is optimized, and ETR clock frequency constraints are added; in the "Mode 2/3 Compare-Capture Mode - Single Pulse Output" chapter, the pulse counting timing diagram details are optimized with additional explanations; in the "Master-Slave Mode Control Register (TIM_MSCR)" chapter, the Bit12 functional description removes the statement "Automatically selects GATE port as CH0B input when PWM center-aligned complementary output is enabled"; in the "Mode 2/3 Compare-Capture Mode Registers - Master-Slave Mode Control Register (TIM_MSCR)" chapter, the Bit[2:0] functional description adds support for "Software update TG, write M23CR.TG" when MMS=0 for TIM3; 4. RTC: In the "Control Register 0 (RTC_CR0)" chapter, supplement the specific time descriptions for setting PRDS to 1 minute or 1 hour or 1 day or 1 month. 5. LPUART: In the "Single-Wire Half-Duplex Data Transmitting and Reception" chapter, the description "After configuring LPUART_SCON.HDSEL to 0b1, must wait for the transmission duration of one data bit (i.e., after 1/BaudRate seconds) before normal reception can occur" is added, Additionally, add configuration guidance for receiving data in single-wire half-duplex mode at baud rates of 9600/4800. 6. OPA: In the "OPA Configuration Register (OPA_CR0)" chapter, Bit[9:7]'s functional description is updated from "Recommended to retain the default value" to "Must retain the default value";
Rev1.03 May 12, 2025	1. Register bit/bit field function description: The value "Reserved" is modified to "Setting prohibited".

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Revision/Date	Changes
Rev1.03 May 12, 2025	2. SYSCTRL: The original "Reset Control" chapter content has been moved into this chapter; in the "System Control Register 1 (SYSCTRL1)" chapter, the Bit2 function description adds "When using PF00 as clock input, SYSCTRL0.WAKE-UP_BYRCH must be configured as 1, otherwise abnormal current will occur in low-power mode"; in the "Peripheral Module Reset Control Register 0 (PERI_RE-SET0)" chapter, the Bit17 description is changed from "VC, LVD module reset enable" to "VC module reset enable"; 3. GPIO: In the "Port Alternate Function Timer Gate Selection (GPIO_TIMGS)" chap-ter, the description for TIM3_G values 0b011/0b100 is changed from "UART2/ UART3" to "LPUART0/LPUART1"; 4. SPI: The description regarding maximum communication speed for master/slave modes is deleted from the "Features" section. 5. CTRIM: In the "Operation Example - RCH/RC48M Clock Auto-Calibration Example" chapter, the RCH-related descriptions are removed, retaining only RC48M con-tent; 6. DMAC: The description of DMA-supported hardware request signals in the "Hard-ware Block Transfer Mode" and "Hardware Burst Transfer Mode" chapters is opti-mized. 7. TIM0/1/2/3: The description in the "Input Interconnection" chapter is simplified (detailed information refers to the corresponding GPIO registers); the description in the "DMA" chapter is changed from table format to an implementation block diagram; 8. LPTIM: Adjusted content layout and added new "Functional Block Diagram" and "Operating Modes" chapters; added new "Features" chapter; optimized the LPTimer operating mode diagram in the "Operating Modes" chapter; simplified descriptions in the "GATE Interconnection" and "ETR Interconnection" chapters (detailed information refers to the corresponding GPIO registers); unified the Bit0 name as "OV" in both the "Interrupt Flag Register (LPTIM_IFR)" and "Interrupt Flag Clear Register (LPTIM_ICLR)" chapters; 9. RTC: The clock error compensation accuracy is modified from "0.95ppm" to "0.96ppm"; the reset value writing format for counter registers is optimized, changed from binary to hexadecimal. 10. LCD: In the "DMA" chapter, the description "The DMA channel number used by LCD is [6]" is deleted; 11. VC: In the "Functional Block Diagram" chapter, the voltage comparator input signal labels are refreshed to maintain consistency with the datasheet. 12. SysTick: In the "SysTick Calibration Value Register (CALIB)" chapter, the Bit31 name description and functional explanation language are optimized.
Rev1.02 Jan. 6, 2025	1. SYSCTRL: In the "Clock Architecture Diagram" chapter, the external crystal oscil-lator (XTH) frequency range is modified to 8M-32M; the diagram in the "Clock Start Process" chapter is optimized; in the "Standard Clock Switching Procedure" chapter, the descriptions of steps 4 and 7 are updated from "FLASH_WAIT regis-ter" to "FLASH_CR.WAIT".

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Revision/Date	Changes
Rev1.02 Jan. 6, 2025	2. NVIC: In the "Interrupt Input and Pending Behavior" chapter, the description is changed from "NVIC_CLRPEND register" to "NVIC_ICPR register"; in the "Interrupt Pending" chapter, the description is modified from "SCS_PRIMASK" to "PRIMASK"; in the "Interrupt Structure Diagram" chapter, the description is updated from "SCS_SEPEND" to "NVIC_ISPR"; in the "NVIC Interrupt Mask" chapter, the register is revised from "SCS_PRIMASK" to "PRIMASK"; 3. GPIO: Optimized register writing format, merged port function selection registers; 4. I2C: In the "Status Code Expression" chapter, the description of 0x38 is changed from "Arbitration lost in non-ACK" to "Arbitration lost in NACK (i.e., the master finds SDA has been pulled low by another device when replying ACK)"; in the "Operation Example" chapter, the description "I2C_CR.EN" is modified to "I2C_CR.ENS"; in the "Master Transmit Example" and "Master Receive Example" chapters, step 8 description is updated from "Start signal has been sent to the bus" to "Start signal has been sent to the bus, set I2C_CR.STA to 0"; in the "Configuration Register (I2C_CR)" chapter, the Bit5 description adds "After START transmission is completed, the user program should set this bit to 0", and the Bit4 description adds "This bit is automatically set to 0 by hardware after STOP transmission is completed"; in the "Status Register (I2C_STAT)" chapter, the bit name is changed from "STA" to "STAT". 5. CLKTRIM: In the "Interrupt Flag Clear Register (CLKTRIM_ICLR)" chapter, the reset value is changed from "0x0000001F" to "0x0000000F", and the functional description of Bit4 is modified accordingly. 6. CTRIM: In the "RCH/RC48M Clock Auto-Calibration Example" and "RCL Clock Auto-Calibration Example" chapters, the description of step 6 is changed from "CTRIM_CR0.FLIM" to "CTRIM_FLIM"; the CTRIM_TVAL register name is modified from "TrimCode Register" to "TRIM Result Register", with added description in the bit name explanation stating "If read by software during TRIM process, two identical reads are required for validity", while deleting the related description in the register summary table. 7. FLASH: In the "Continuous Write Operation (Cont-Program)" chapter, the description is changed from "User software should wait for the operation to complete (FLASH_IFR.BUSY becomes 0)" to "User software should wait for the operation to complete (FLASH_CR.BUSY becomes 0)". 8. TIM0/1/2/3: In the "Mode 0 Counting Timer Function" chapter, the register name CR is changed to M0CR; in the "Mode 0 Counting Timer Free Counting Block Diagram" and "Mode 0 Counting Timer Reload Counting Block Diagram" sections, the description is updated from "PRS[2:0]" to "M0CR.PRS"; in the "Mode 2/3 Compare-Capture Mode", "Mode 2/3 Slave Mode", "Timer Triggers ADC", "Cycle-by-Cycle Current Limiting and Brake Control", "Mode 2/3 Compare-Capture Mode Configuration Example", "Simultaneous PWM Output Startup Configuration for TIM0/1/2 (Using TIM0's CTEN to Trigger TIM1/2) Example", "Simultaneous PWM Output Startup Configuration for TIM0/1/2 (Using TIM1's UG to Trigger TIM0/2) Example" and "Master-Slave Mode Control Register (TIM_MSCR)" chapters, the register name CR is modified to M23CR; in the "Independent PWM Output"

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Rev1.02 Jan. 6, 2025	chapter, the description is changed from "CRCHx" to "FLTR"; in the "Mode 2/3 Compare-Capture Mode Registers - 16-bit Counter Register (TIM_CNT)" chapter, the bit description is updated from "When using PWM compare output, the initial CNT value must be less than the ARR value" to "When using PWM compare output, triangle-wave mode, or sawtooth-wave mode up-counting, the initial CNT value must be less than the ARR value"; in the "Control Register (TIM_M23CR)" chapter, Bits [22:21] are renamed from "Center-Aligned A Compare Match Mode" to "Channel A Compare Match Mode" with added description "Channel B Compare Match Mode is controlled by the CISB bit in the CRCHx register"; in the "Master-Slave Mode Control Register (TIM_MSCR)" chapter, Bit 12's functional description is updated from "Automatically selects GATE port as CH0B input when PWM complementary output is enabled" to "Automatically selects GATE port as CH0B input when PWM center-aligned complementary output is enabled" and Bit 11's functional description is changed from "CH0A ETR GATE XOR (TIM0)" to "CH0A ETR GATE XOR (TIM0/1/2)"; in the "Channel 0 Control Register (TIM_CRCH0)", "Channel 1 Control Register (TIM_CRCH1)" and "Channel 2 Control Register (TIM_CRCH2)" chapters, the reset value is updated from "0x00000000" to "0x00003000"; in the "Repetition Counter Register (TIM_RCR)" chapter, the RCR bit description is modified from "Generates update event after RCR+1 periods of overflow/underflow" to "Generates update event after RCR+1 periods, with overflow controlled by bits [9:8]". 9. TIM4/5/6: In the "Quadrature Encoder Counting - Position Counting Mode" section, the figure captions for "Position Mode Phase Difference Counting Operation Setting (2x)" and "Position Mode Phase Difference Counting Operation Setting (4x)" are modified from "HCUPR.HCDO" to "HCDOR.HCDO"; the diagram in the "Cycle Interval Response" chapter is optimized. 10. RTC: In the "1Hz Output" chapter, step 3 register is changed from "1HZOE" to "HZ1OE", and step 4 register is modified from "1HZSEL" to "HZ1SEL"; in the "Hour Counter Register (RTC_HOUR)" chapter, the 12-hour format description is updated from "HOURH[5]=0 indicates AM; HOURH[5]=1 indicates PM" to "Bit5=0 indicates AM (01-12 represents morning); Bit5=1 indicates PM (21-32 represents afternoon)". 11. LPUART: In the "Mode0 Data Transmission and Reception" chapter, the description in the Mode0 Receive Data diagram is changed from "Write ICR.TCCF=0" to "Write ICR.RCCF=0"; in the "Multi-Device Communication" chapter, the description is modified from "ADEDET" to "ADRDET"; in the "Control Register (LPUART_SCON)" chapter, the functional description format of Bits [10:9] is optimized into a list, and the 0b1 value of Bit[12:11] is changed from "PCLK" to "Reserved". 12. AES: In the "Features" chapter, the description "The AES encryption algorithm provides various working modes, but this IP only supports ECB mode" is deleted; in the "Data Example" chapter, the ciphertext for the 192-bit key is changed from "0x5AC5B47080B7CDD830047B6AD8E0C469" to "0x91710DECA070AF6EE0DF4C86A47CA9DD", and the ciphertext for the

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Rev1.02 Jan. 6, 2025	256-bit key is modified from "0x5AC5B47080B7CDD830047B6AD8E0C469" to "0x8960494B9049FCAEBF456751CAB7A28E". 13. ADC: In the "ADC Block Diagram" chapter, the graphic description is changed from "ANx" to "AINx"; in the "Operation Flow for Starting ADC Single Conversion via External Trigger" chapter step 13, "Operation Flow for Starting ADC SQR Scan Conversion via External Trigger" chapter step 14, and "Operation Flow for Starting ADC JQR Continuous Conversion Accumulation via External Trigger" chapter step 15, the description is modified from "Set ADC_IFR to 0x0" to "Set ADC_ICR to 0x0"; in the "ADC Basic Configuration Register 1 (ADC_CR1)" chapter, the Bit15 function description is updated to "Writing 0 clears the ADC_RESULTACC register, writing 1 has no effect; reading always returns 1". 14. LVD: In the "Hysteresis Function" chapter, the high and low levels of the output waveform in the diagram are swapped.
Rev1.01 May 17, 2024	Added: 1. "GPIO" chapter "Description-Port Digital Multiplexing Function". Add PF11 port; "Register-Port PF function selection register" adds the "Port PF11 Function Configuration Register (PF11_SEL)". Modified: 1. "SWD Debug Interface" chapter "Peripheral Debug Function Enable Register (DEBUG_ACTIVE)" Bit3 name is modified to LPTIM0. 2. "ADC" chapter "ADC Basic Configuration Register 0 (ADC_CR0)" Bit14 INREFEN adds the description "This bit must be set to 1 when using internal 1.5V/2.5V as ADC reference voltage".
Rev1.00 Apr. 22, 2024	First official release.

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